Investigation into the design domains' interdependencies of an inverter

case study of an aerospace inverter for extreme conditions

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Abstract

The continuous development of power electronic converters has opened new opportunities for the More-Electrical Aircraft (MEA) concept, where the conventional power sources (pneumatic, hydraulic, mechanical) are replaced with electric sources to support secondary loads in the aircrafts. It is expected that more efficient, lighter and lower maintenance solutions can be obtained with high power density power electronics. In order to obtain optimal designs for power system integration, new methodologies employing multi-objective optimization have been reported. However, the application of multi-objective optimization is more powerful with multi-domain modeling, which is not always a straightforward task. The reason is that power electronics design is a complex design problem, mainly because of the multi-disciplinary nature of its physical aspects (domains), including electric circuit behavior, thermal performance, electromagnetic compatibility issues and packaging constraints. Therefore, a subsequent modeling effort for the power electronics design is necessary to fully exploit the advantages of optimization techniques. To obtain a comprehensive insight in the system behavior, the mutual dependencies of the power electronics' design domains need to be characterized and quantified. This thesis investigates into the interdependencies between the design domains of an inverter for aerospace applications.

In this thesis project a design methodology is developed based on the multi-domain approach. The converter design is treated as a system in a top level design aspect, leading to the selection of a topology, modulation and control strategy. In addition, the circuit level design is effectively decoupled into the electrical, EMI, thermal and mechanical design domains, which are treated independently. The boundaries of the design levels and domains are determined and the links between the design domains are established though their mutual dependencies. Based on this methodology, a design framework for an aerospace inverter is realized in software using analytical modeling. This framework is used to investigate the mutual dependencies of the design domains and the impact of the design choices on the inverter performance. The interdependencies of the design domains are manipulated using design variables, similar to an optimization problem, by employing parametric sweep. A high efficiency and high power density aerospace inverter is designed, according to the specifications of Aeronamic B.V. and aerospace regulations.

Keywords: multi-domain modeling, aerospace, inverter, design domains, boundaries, interdependencies, power density

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Chapter 1

Introduction

1-1 Problem statement

The design of high performance power electronic converters is a challenging and complex task. The main reason is that the design considerations are spanning various physical domains, for example electrical, thermal, etc. The complexity results to a high cost and time consuming design process, which often require iterations; design of a first prototype, manufacture it, characterize it and then conclude to a final design. In order to tackle this problem, a virtual prototype by the means of analytical models and/or simulations can help engineers in a pre-design level as well as in the validation steps of the design process. New methodologies employing virtual prototyping in combination with multi-objective optimization are becoming increasingly mature. These methodologies are gradually penetrating the industrial power electronic design process. The application of multi-objective optimization is more powerful with multi-domain modeling, which by means is not always a straightforward task. As a result it is interesting to explore how to research a modular, systematic and scalable methodology.

Moreover, the aerospace industry is placing great emphasis in technologies which can reduce the overall costs and fuel consumption. For this reason, the continuous development of power electronic converters has opened new opportunities to the trend for the More-Electrical Aircraft (MEA), where the conventional power sources (pneumatic, hydraulic, mechanical) are replaced with electric sources to support secondary loads in the aircrafts. The electric systems are expected to lead to more efficient, lighter and lower maintenance solutions by using high power density power electronics and electrical machines. However, the extreme operating conditions and strict reliability regulations in aerospace applications constrain the maximum power density which can be achieved in these applications. In this direction, these challenges need to be met for the electronic devices, in order to obtain optimal designs for power system integration in More-Electrical Aircraft.

Consequently, the problem of optimally designing a motor drive for aerospace applications is gaining more attention. To this regard, applying multi-objective optimization is expected to be crucial towards achieving the stringent requirements that are present. Therefore, a subsequent modeling effort for the inverter and motor is necessary to fully exploit

the advantages of optimization techniques. This thesis work will focus on the design of an inverter for aerospace applications.

1-2 Thesis objective

This thesis project is conducted in collaboration with Aeronamic B.V. in order to develop a design framework for an inverter which will constitute the basis and support the design for a high-speed PMSM drive system optimization. The primary objective of this thesis is to investigate the interdependencies of the design domains of an inverter for aerospace applications, targeting to design an inverter with minimum volume and weight. In order to achieve the main objective of the thesis, a design method must be developed and the following aspects must be answered:

- Which are the considerations to decouple the design aspects related to power electronics design?
- How are the boundaries of the design aspects defined?
- Which are the interdependencies between the design aspects?
  - How can the interdependencies be manipulated to achieve optimal designs?
- Which modeling method is suitable for this study?
  - How is the modeling effort determined by the design objectives?

1-3 Thesis contribution

A design methodology is developed in this project thesis, based on multi-domain design. The converter design is decoupled regarding the system and individual component performance and treated in a top-level and circuit-level. In the top-level design, the selection process of a topology, modulation and control strategy takes place. In the circuit-level, the converter is designed regarding the component behavior, with respect to the physical domains that describe the converter operation. The design domains are distinguished in electrical, EMI, thermal and mechanical, and are treated independently. The boundaries of the design levels and domains are determined and the links between the design domains are established though their mutual dependencies.

Based on this methodology, a virtual prototype of an aerospace inverter is realized in software using analytical modeling. In the top level design the inverter is designed for minimum current rating, based on the operation of the inverter-PMSM system under the drive limitations. In the circuit level, the interdependencies of the design domains are manipulated using design variables, similar to an optimization problem, by employing parametric sweep. A high efficiency and high power density aerospace inverter is designed to drive the PMSM load, according to the specifications of Aeronamic B.V. and aerospace regulations.

1-4 Thesis outline

Apart from the present introductory chapter, the thesis contents are organized as follows.

In Chapter 2, first the background of this work regarding virtual prototyping and multi-domain modeling methods is described. The reasoning for choosing a mutli-domain design approach using analytical models is described. Then the methodology developed in this thesis project is described. The converter is considered in a top level and circuit level design domain, which are designed autonomously. Then the design domains of the circuit level design are distinguished, namely electrical, EMI, thermal and mechanical, and their couplings are investigated. In addition, some modeling considerations regarding each domain are briefly addressed.

The design approach is then applied to the design of an aerospace inverter and a design framework in software is developed. First, in Chapter 3, the specifications and application specific constraints of the inverter are addressed. Then the topology selection follows, based on a classification of the available topologies and comparison of the suitable candidates. In addition, a modulation technique is selected for the design based on a classification of the available modulation techniques. Finally, the control strategy is selected and the inverter-PMSM operating points are obtained. The control strategy is selected for a minimum current sizing of the inverter and the operation of the system under drive limitations is investigated.

In Chapter 4, the circuit level design takes place. Here, the objective is to estimate the converter circuit performance and design the main components. The proposed design method is followed for the modeling and linking of the electrical, EMI, thermal and mechanical design domains. Regarding the modeling choices, the reasoning and limitations of the models are addressed and the respective mathematical background is shown.

Chapter 5 presents the results obtained with the design framework which is developed in this thesis. A parametric sweep is used to manipulate the interdependencies of the design domains. First, the results regarding the interdependencies of the design domains are presented and discussed and the trade-offs of the design choices are explained. Finally, a set of inverter designs is presented, from which the best candidate regarding power density and efficiency is be selected.

The conclusions of this thesis project and some recommendations for future research are summarized in Chapter 6.

Chapter 2

Power electronics converter design – a systematic approach

2-1 Introduction

In this chapter a multi-domain design approach for power electronic converters is discussed. In the first part of this chapter, the concept of virtual prototyping in power electronics and a review of the related work on multi-domain design methods regarding power electronic converters are presented, which constitute the basis for the design method of this work. The second part addresses the design method developed in this thesis, which will be discussed in detail. Specifically, the key aspects of the converter design problem are analyzed, namely design levels and domains, and the interdependencies between them are investigated. Based on this analysis, a design methodology is developed targeting to establish a complete framework for power electronics design. This framework will be later applied to the design of an aerospace inverter, which will be presented in the next chapters.

2-2 Background and motivation

The multi-disciplinary nature of power electronics increases the complexity in the design process, since design in many physical domains is required, regarding the power circuit's operation and environment. These domains are distinguished from each other according to the physical principles that they address, specifically electrical, electromagnetic, thermal and mechanical. Moreover, they are coupled to each other, for example in electro-thermal coupling the links are the component losses and temperature, the mechanical and electrical domain are linked through the component volume and layout (spatial design and parasitics) etc. Thus, a change in a parameter in one domain can affect the converter behavior in other domains and shape the designer's choices in different directions. Furthermore, the impact of the design choices on the converter behavior is not always straightforward and often comes with a price;

for instance, an increase in switching frequency can reduce the volume of the passives but will increase the heatsink volume due to increased losses in the semiconductors [2].

As a result, the development of power electronics poses challenges regarding the design approach. To begin with, even though a comprehensive design requires knowledge on multiple disciplines, the designer's expertise typically does not cover all areas. Also, these areas can be studied as separate domains with respect to the physical principles that define them (eg. electromagnetic, fluid dynamics, mechanical stresses etc.) so that the design process is simplified; however, they are strongly coupled to each other and it is essential that the links are included, to account for the coupled phenomena. Finally, it is often required that competing performance objectives are met simultaneously, for instance maximum efficiency and minimum volume, so the best trade-off between the objectives must be obtained for an optimal performance.

2-2-1 Virtual prototyping in power electronics

There are many ways to design a power electronics system, including empirical equations, analytical models, simulation techniques etc. However, it is important that the design process meets the following general requirements:

- Gives information on the converter behavior regarding the given specifications
- Provides feedback on the design choices
- Reduces the time and effort of the design cycle: predesign, verification and validation

Also, depending on the application or the industry specifications, additional, more specific, requirements are imposed on the design approach, such as to be used for optimization or to be valid for a wide range of operating conditions and so forth. A very useful tool that meets these requirements, is virtual prototyping [2]. A virtual prototype of a converter is a representation of the physical behavior of the converter in a virtual environment, for instance modeling with analytical equations, numerical simulations or a combination of both. In this case, the designer has access to valuable information for the converter performance and reduces the design time process of a prototype as well as the cost; simulations and analytical models are faster to realize with computer-aided design, than to implement and test a prototype in hardware. It also offers flexibility regarding topologies comparison, testing of new concepts and identification of the influence of a parameter in a design.

For these reasons, and more [2], virtual prototyping has been proven beneficial for power electronics design in the literature. To begin with, great level of accuracy is achievable [2] between calculated and experimental results with minimal calculation effort. In this direction, [11] focused on losses calculation to obtain maximum power density for a nine switches matrix converter[12], employing optimization. The design results showed a 2.77% total loss error between calculated and experimental results. In addition, the reliability of power electronics can be estimated. The work in [13] proposed a systematic method for reliability-oriented design of power electronics converter, with emphasis on the reliability of IGBT modules. In the virtual prototype, the lifetime models they presented, revealed the impact of temperature and temperature cycling on 1.6kA/1.7kV/125^{o}C and 2.4kA/1.7kV/150^{o}C IGBT modules based

on the mission profile of a 2.3 MW wind power converter. Since their method is independent from the input, it can be used to test different mission profiles. Furthermore, comparison of different converter topologies is possible. This was the case in [14], where different DC/AC [12] converter topologies were compared with respect to the influence of switching frequency on maximum power per weight value. Finally, the virtual prototype can show the possibility of new R&D opportunities at the device level, to support optimized converters. A characteristic example is the work of [15], where a descriptive language method for renewable system inverters optimization was proposed. In that model, the component parameters were used as design variables for energy loss models of semiconductors, capacitors and inductors; hence, commercial availability was not a limiting factor in this case. To summarize, due to the advantages that virtual prototyping brings in the power electronics design, it is the basis for the methodology in this work as well.

2-2-2 The multi-domain modeling approach

The design methods presented in 2-2-1 are very successful for designs in their area of focus, but none of them includes all aspects involved in a converter design, eg. electromagnetic interference (EMI) and spatial design, or they do not link the electrical and thermal behavior of the converters. To obtain comprehensive insight in the system behavior and achieve better designs, novel approaches using multi-domain modeling([4-7][20][22]) include several physical domains in the design process. This has the advantage of eliminating the risk for multiple iterations in the design or verification stages and avoids unexpected behavior of the prototype converter if the influence between the domains is neglected. As a result, the design process becomes more powerful since the mutual coupling of the domains is accounted for from the beginning of the design. This concept was the focus of [1], where the significance of the electrical-thermal-mechanical domains interdependencies for better designs was shown. Instead of being a limiting factor, the interdependencies were used to an advantage for the design of high-power density high-temperature automotive DC/DC converters, resulting to a 170W/in^3 at 85^{o}C [16] and 120W/in^3 at 110^{o}C [17] prototypes. The interdependencies between the electrical, thermal and mechanical domains of [1] are visualized in Figure 2-1.

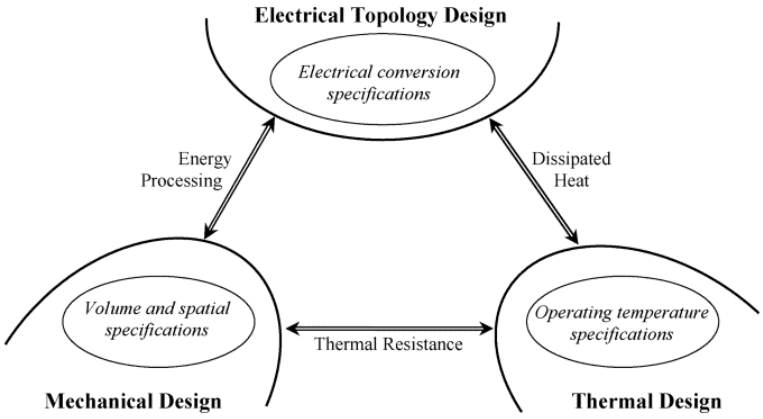


Figure 2-1: Electrical, thermal and mechanical interconnections overview by [1].

In addition, the benefits of linking the design domains regarding the future development of

power electronics employing optimization techniques were discussed in [2]. In this work it was shown that the design process effort is expected to be minimized by coupling the engineering tools according to the domains mutual coupling, as illustrated in Figure 2-2. This justifies the fact that multi-domain approaches have become particularly useful in designs employing optimization techniques [18][19].

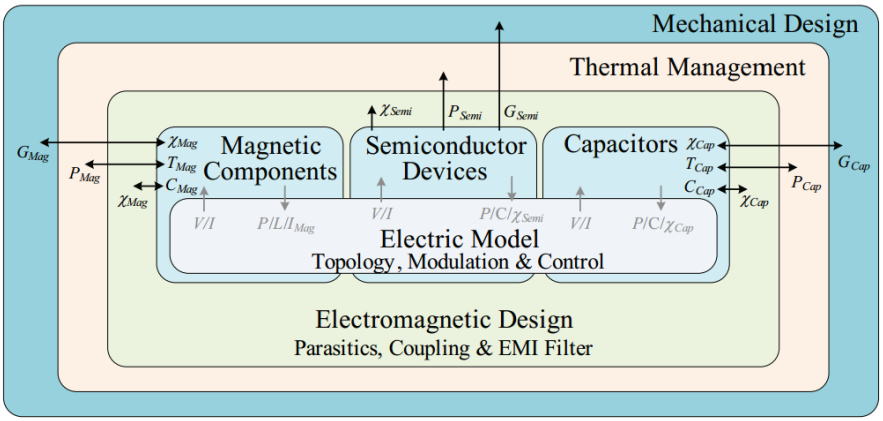


Figure 2-2: Multi-domain interdependencies at circuit level design by [2].

The need for optimization arises by the market requirements for more efficient, compact, reliable converters and cost-effective solutions, not to mention that such performance objectives is often required to be met simultaneously. As a result, multi-objective optimization is used. Specifically, two techniques can be identified. First, the optimization problem can be transformed into a single objective function with predefined weights for the respective objectives (aggregate technique). Alternatively, Pareto optimization [19] can be used that reveals the best trade-offs between the objectives, where no other optimal solution is obtained without deteriorating a parameter to optimize another. Since the Pareto analysis does not select weights for the optimization targets, it has the advantage of calculating all possible alternatives and is thus often preferred. The outcome of this process is the Pareto frontier of a design, which indicates the optimal solutions and allows comparison of different concepts in terms of multiple performance indexes. An example of this concept is shown in Figure 2-3, for a PFC converter comparison that was performed in [3].

The objective of this thesis project is to arrive at a design method with complete coverage of the physical domains of the converter and their interdependencies. For this reason, this work is based on design methods that employ multi-domain approaches for power electronics, since multi-domain modeling gives insight to the inter-domain dependences and design choices trade-offs. In addition, this work aims to support the integrated design by optimization of an inverter-machine drive system, hence the design approach is based on methods that are suitable for optimization techniques. Two trends of multi-domain design for converters optimization have been identified; simulation-based and analytical equations-based. The suitability of these methods for this work depends on their characteristics, advantages and shortcomings. A short review of these two methods, together with suitability justification for this thesis is following.

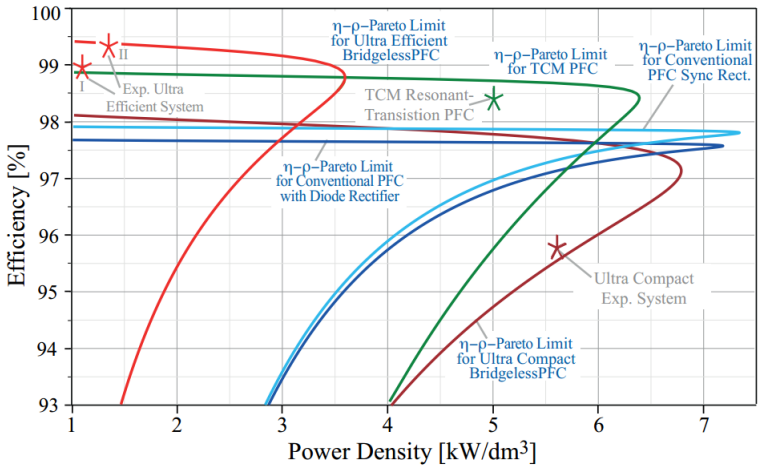


Figure 2-3: PFC converters comparison using Pareto frontiers [3].

Simulation-based methods

Multi-domain modeling approaches have been used for power electronics design by employing simulations on either specific components or converter system design. A systematic simulation approach was followed in [20] with coupled electrical and thermal models. Their focus was on the calculation of transient temperatures of IGBT modules and short-term overload conditions analysis; this is particularly useful for optimizing module technology and reliability, and their method can be used to create thermal macro-models for system evaluation. The work in [4] also focused on IGBT modules, using multi-domain modeling for electro-thermal simulations with a feedback loop for thermo-mechanical behavior. Their concept is illustrated in Figure 2-4. However, both these methods are limited to the electro-thermal behavior of semiconductor modules. On the other hand, in [5] a simulation platform was presented, which is illustrated in Figure 2-5, for the design of DC/DC converters with focus on power density. The design tool that was developed, except from electrical and thermal domains simulation, estimates the layout parasitics, linking the electrical to the mechanical domain. It does not however include calculations for the EMI noise or filtering.

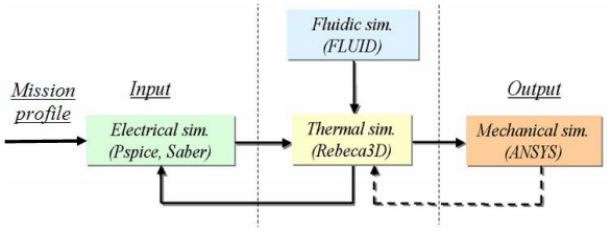


Figure 2-4: The IGBT modules design approach using simulations by [4].

These approaches require transfer of simulation data between the different physical domains or between the tools that deal with simulations within different domains. This is inherently problematic due to the coupling challenges of design tools [2][21]. Towards solving this issue, in [20] a new circuit simulator was built to solve the problems of a) connecting the

electrical losses to the thermal network and b) poor scaling performance of existing simulators for large impedance matrices for the equivalent thermal networks. Also, in [4] a central program was built to connect the simulation tools, since each physics domain specialist created the simulation models in a tool of their choice. A similar approach was followed in [5]. Since multi-domain modeling requires linking of the different physical domains, if simulation tools are used, either the user has to extend a tool to cover all domains or develop a platform, which translates and transfers the data between the different tools. Due to the limitations of simulation-based methods, combined with the fact that simulations require a substantial calculation effort, simulation-based design is not considered suitable for the work in this thesis project.

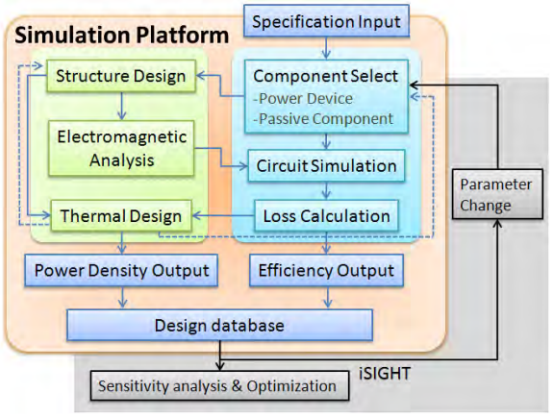


Figure 2-5: Simulation based design process of a DC/DC converter by [5].

Analytical equations-based methods

Multi-domain analytical models are also used for the design of power electronic converters, often in combination with optimization techniques. In [6] an evaluation of DC-DC multilevel [12] topologies is performed using electro-thermal analytical models. The design process, shown in Figure 2-6, demonstrated the sensitivity of the power density with respect to changes in design variables and proved scalability of the method to other power levels. The conclusions for the best topology were drawn by comparison of Pareto frontiers for each topology. It was proven that the greatest improvement for the system power density can be achieved by investing in better cooling methods and decreasing the semiconductor losses, which were the dominant contributor to the system losses. Also, they used interleaved [6] converters to obtain the required power output, which in turn eliminated the need for an input filter. These results however did not include the derivation of the EMI input noise, and thus the elimination for EMI filtering, or detailed spatial design.

A similar design process was also followed in [22], where analytical modeling with optimization was used for the electrical, thermal and mechanical domains, to compare DC/DC converters for telecom applications. In this study, the trade-offs required for power density over efficiency were shown and the influence of device parameters on the converter power density, considering the net volume of the main components (EMI filter was not considered). Since the volume requirements were the design constraint in this study, special attention was

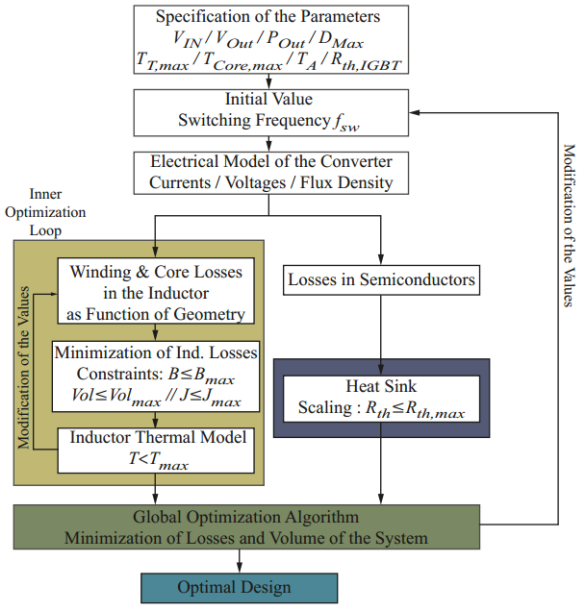


Figure 2-6: Electo-thermal domain modeling and optimization process by [6].

given to the component volume distribution with respect to the switching frequency. To obtain a continuous relation to power density, their model considered a scaling method to calculate the size of the passives and the type of semiconductor switch, and the losses for the semiconductors were calculated from measurements of specific components.

Meanwhile, [7] followed a systematic approach for evaluation of AC/AC topologies, including electrical, thermal and EMI domains. The main objective was to compare the front-end rectifier topologies of AC/AC converters with respect to minimum converter weight. As a

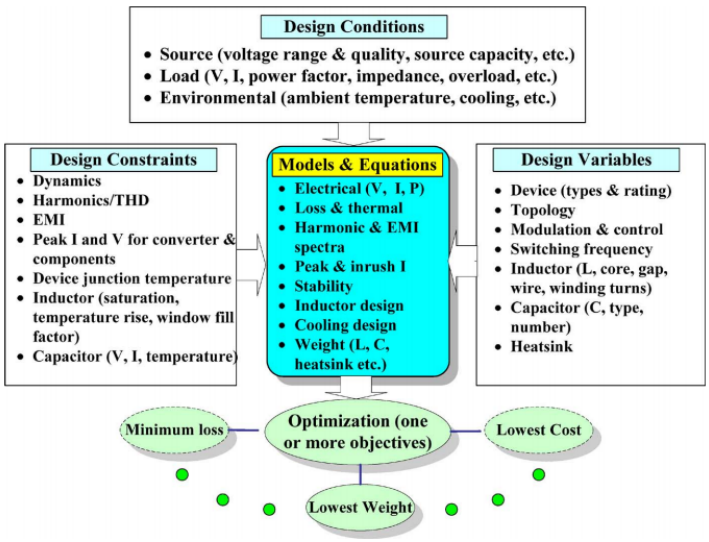


Figure 2-7: Multi-domain design approach overview by [7].

result, the mechanical domain in their approach considered only the components weight and

spatial design was not included. The impact of the switching frequency regarding the EMI filter design [23] was also studied, which played an important role in selecting the switching frequency of the converter. However, the effect of the circuit and machine parasitics in their design process were neglected. Their design method clearly distinguishes the specifications, boundaries and variables based on which the design process is developed, and is scalable in terms of different topologies design. As a result it can be used for optimization, as noted in Figure 2-7.

With analytical modeling, complex models are required to increase the accuracy of the calculations, which in turn increases the modeling effort. However, the tools linking problem of simulation-based methods does not occur, since the multi-domain aspects were represented with equivalent models and a single modeling tool can be used in this case. Thus, the evaluation of different topologies and concepts is easier to achieve, and optimization can be employed to achieve the best possible performance of the virtual prototype. For these reasons, analytical modeling was decided to be used in the work of this thesis.

From the presented prior art, the following points can be identified. First of all, even though multi-domain modeling is used, not all domains are included in the design, for example EMI. In addition, the modeling does not always include all the contributing parameters, for example the EMI models and spatial design in [7]. Moreover, the mutual coupling is demonstrated with the analytical models, but the interdependencies are not clearly defined. On the other hand, this thesis focuses on the interdependencies of the design domains. For this reason, a complete coverage of the physical domains is needed, which can be effectively decoupled in order to investigate their interdependencies. Thus, a design methodology will be developed in this direction. This methodology is presented in the following section.

2-3 Design methodology

In this section a design approach for power electronic converters based on multi-domain modeling is discussed. The objective is the development of a systematic design method that is expandable in terms of application requirements and modeling accuracy. For this reason, the effective separation of the design problem into independent design tasks and subtasks is investigated. At the same time, the coupling of the respective design aspects is identified, which in combination with the design domains constitutes a complete framework for power electronic converters development.

To meet the objective, the design tasks of the converter system are identified and modeled according to the following characteristics:

- physical behavior
- role in the system

An overview of the concept is shown in Figure 2-8, demonstrating the key design aspects and their links, which will be identified in the following sections. The source of the process is the application *boundaries and requirements*, which refer to the converter specifications, constraints and environment that shape the decision making process and modeling of the converter. Their significance in the design is discussed in section 2-3-1. Then the design

problem is separated into two independent design levels. The objective of this distinction is to decouple design decisions for the performance of the converter as a system and as individual components in the circuit. The first design level is the *Top-level design*. It refers to the converter as a system and involves decisions regarding the selection of appropriate topologies, modulation strategies and control techniques, as well as the converter system operating points. As a result, in this design level only the electrical parameters of the converter as a system are included. The design principles of the *Top-level design* are presented in section 2-3-2. The second design level is the *Circuit-level design*. Here the converter is designed regarding

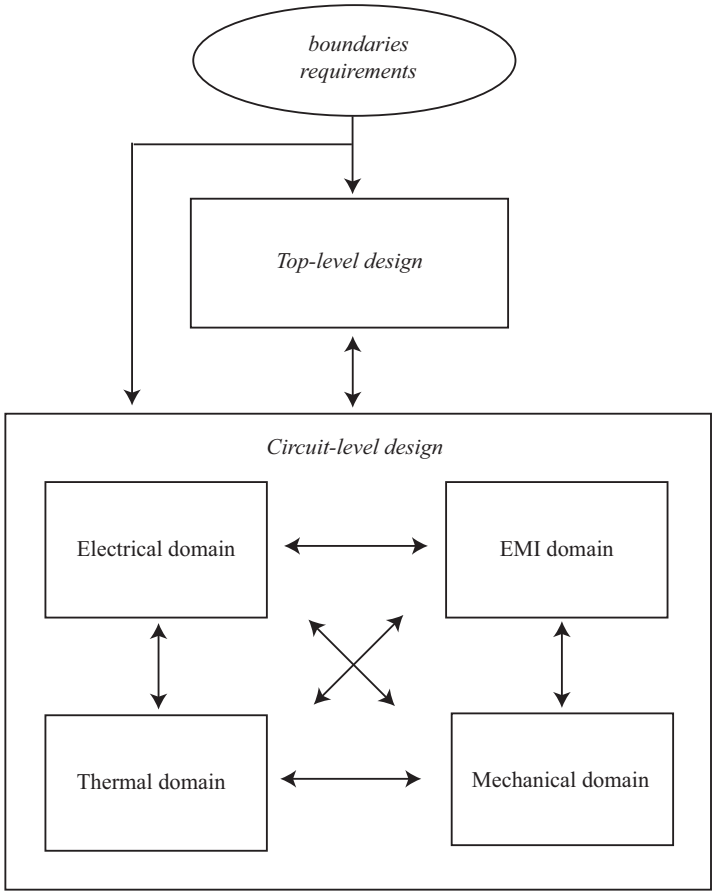


Figure 2-8: Multi-domain design overview

the component behavior, with respect to the physical domains that describe the converter operation, namely *Electrical*, *EMI*, *Thermal* and *Mechanical domains*. In sections 2-3-3 to 2-3-6 the *Circuit-level design* domains are presented respectively, where the design aspects of each domain and its dependencies to the other domains are investigated. In addition, some design considerations are addressed considering modeling methods of adequate accuracy and high calculating speed for the design process. The methodology is completed in section 2-3-7, where interdependencies between the design levels and domains are established.

2-3-1 Boundaries and requirements

The design requirements and boundaries are defined based on the application specifications and environment. Since power electronics are part of greater systems (motor drives, power amplifiers, power supplies etc), it is important to consider any subsystems that have a strong influence in the operation of the converter.

In [24] the significance of the system boundaries definition was discussed, by comparing the results of a permanent magnet BLDC machine design when the inverter was included or not in the machine design process. The results showed that when the inverter model was ignored then the machine design led to misleading results, whereas when the inverter model was considered, the torque specifications were always met. In the first modeling case, the electrical boundary of the machine included only the machine related parameters. However, in the second modeling case, the electric properties of the converter which affected the machine design were included. Thus, the electrical boundary of the machine was extended to the related electric properties of the converter. In this case, the boundaries refer to properties of the same physical domain between two different systems. As a result, the contributing parameters to the operation of the converter as a system will also be included in this work. This way their effect at the system operating points can be accounted for.

In addition, the physical environment and its properties determine the boundaries between the design domains of the converter (parameters inside the converter system). This can be demonstrated by the following case study. First of all, similar to the previous example, the thermal boundary of the DC/DC converter design in [1] included the high temperature environment of the combustion engine compartment, in which the converter was placed. In this case, the converter thermal boundary included the properties of the same design domain which were external to the converter system. Moreover, in [1] the converter individual design domains also included parameters from different physical domains within the converter system. Specifically, the boundary of the design domains was extended to the others by considering the interdependencies between them. In this thesis work, the boundary between the converter and the external environment parameters is defined in the *Boundaries and requirements* space and is illustrated in Figure 2-9. On the other hand, the interdependencies between the converter design domains which are investigated in this chapter, will define how the design domains' boundaries are extended to each other within the converter system.

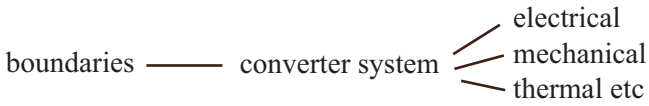


Figure 2-9: Converter system boundaries

Considering the converter design requirements, the application specifications determine the output power of the converter, type of the input source and the load, the mission profile, operating frequency, performance regarding efficiency and power density, current and voltage ripple, and other parameters related to the characteristics of the converter that define it as a system. In addition, the application area comes with related reliability standards, EMI noise constraints etc. that further reduce the design space (Figure 2-10). Regardless of the application, it is also required that the performance of the converter must be within the temperature limitations of the components, voltage and current ratings etc. These requirements

are connected to the component level performance criteria. Non compliance with any of the requirements obviously leads to different design decisions.

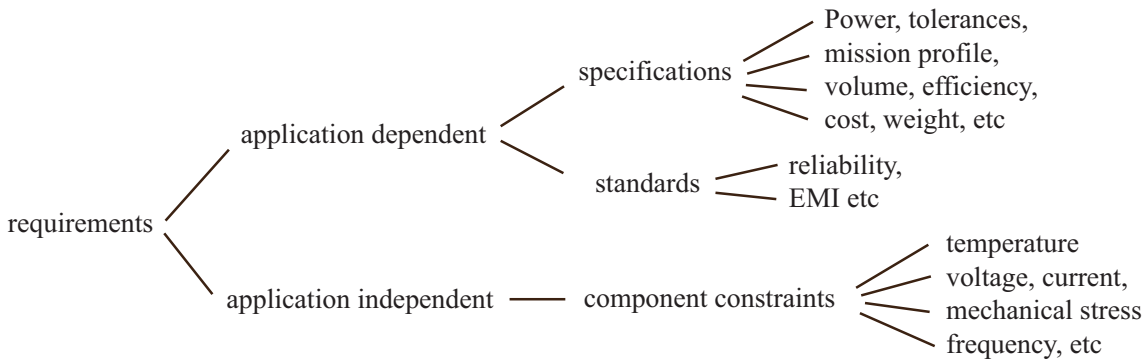


Figure 2-10: Application dependent and independent requirements for power electronics design

The definition of clear requirements and system boundaries helps the design process, since it gives a comprehensive overview of the system to be designed and allows a better approximation of the real system. Whether they will influence the *Top-level* or *Circuit-level design*, depends on the nature of the boundaries and purpose of the design task, as will be shown in the following sections.

2-3-2 Top level design

At the beginning of the design process, decisions regarding the converter design in the context of a system are the subject of the *Top-level* design. Here, the design considers the electrical parameters of the converter as a system. The objective is to determine the appropriate topologies, modulation and control strategies, which can be employed. In this section, the dependencies of the *Top-level* to other converter aspects are addressed, followed by considerations regarding the design process in this stage.

Top level dependencies

The design space regarding converter topologies, modulation and control strategies is very broad, considering their advantages and shortcomings and their suitability for a specific application. The main aspects which influence the selection process are the application specifications and component ratings (Figure 2-11). The application specifications refer to the converter power, source type and load type. These parameters determine the type of converter and suitable topologies, considering the type of the converter elements and their circuit connections. In addition, the voltage and current ratings of the available components from the database affect the selection process of appropriate topologies as well.

The outcome of this process is a number of feasible topologies, modulation and control techniques. From this selection the voltage and current rating of the converter and converter system operating points (input and output current and voltage) are obtained. The suitability of the selected options for the application is fed from the *Circuit-level design* after the

design process is complete. Specifically, the feedback considers the converter performance and determines if the selected design is acceptable according to the specified requirements (Figure 2-11). If optimization is employed, then the feedback loop closes from the outcome of the optimization block.

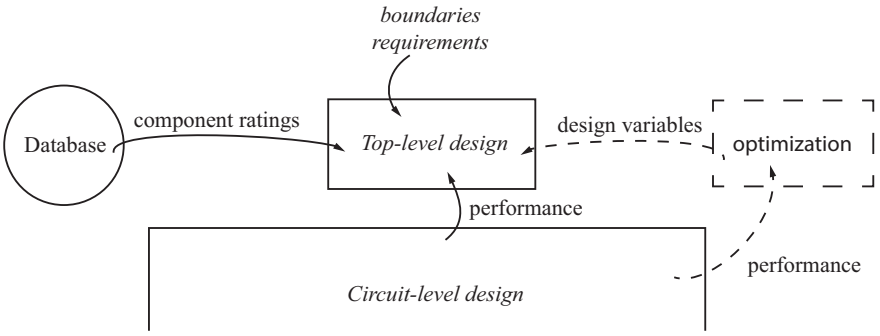


Figure 2-11: Top-level design dependencies

Top level design considerations

Depending on the application, a search in the design space is required so that the appropriate topologies are selected. For this reason, the available topologies are classified regarding the arrangement and number of semiconductors and passive components. Similarly, a classification of the modulation techniques and control strategies can be applied according to the switching characteristics. The criteria for the candidate options selection depend on the requirements of the application, for example constant load, high power, isolation etc. For the final selection of a potentially optimal choice, a comparison based on performance metrics takes place, such as efficiency, volume, cost etc. In some cases the comparison of topologies and switching schemes combination is employed before the *Circuit-level design* to select one option, such as in [25]. In other cases, for example in [7], the candidate topologies are compared from the results of the design process. Choosing whether the topology, modulation and control will be design variables, depends on the application, experience and objectives of the designer.

2-3-3 Electrical domain

In the *Circuit-level design* the electrical performance of the converter is analyzed in the *Electrical domain*. The objective is to determine the electrical characteristics of the elements of the power circuit and use them for the design of the components according to the application specifications. In this section, the parameters which influence the converter electrical behavior are addressed and the dependencies from the other domains are established. Finally, some considerations for the electric circuit design are discussed.

Electric circuit and component design coupling

In the design process, the circuit's electrical performance and efficiency are estimated. Regarding the analysis of the electric circuit, the converter input and output voltages and currents

are obtained for the evaluation of the converter power. The current and voltage stresses on each of the converter elements are also calculated for the performance evaluation of each converter element (Figure 2-12). Specifically, regarding the semiconductor elements, the design is based on the operating points at the switching instances and during the on- and off-state periods. Similarly, in the circuit analysis, the value of the passive elements is also calculated with respect to the specified requirements.

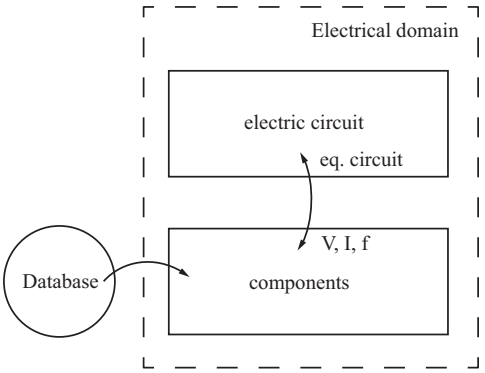


Figure 2-12: Electric circuit and component design coupling in the *Electrical domain*.

Furthermore, the operating points and stresses are used for the sizing and design of the respective components. From the component design, the electrical parameters of the components (required values and parasitics) are obtained and the result is an equivalent circuit of each element. The complete electric circuit can be represented more accurately if the equivalent circuits are included, hence the component design and electric circuit coupling is used in the *Electrical domain* (Figure 2-12). It should be noted that the component design in this work is considered as a part of the *Electrical domain*. However, the design of the components also depends on parameters which are obtained form the other domains, as will be discussed in following sections.

Circuit operation dependencies

Calculation of the component stresses depends on the operating points of the converter and the component parameters. These values are influenced by the following factors (Figure 2-13):

- **Electric boundaries and requirements**
  These factors are determined from converter power specifications and the electric boundary is extended to include the source and load connection of the converter. In the design process the voltage and current component constraints are taken into account to form the component design space.

- **Topology, modulation and control**
  The circuit voltages and currents are shaped by the converter topology (component arrangement) and the switching strategy selected in the *Top level design*. They affect the operating points based on which the circuit characteristics are dependent, for example the parasitic capacitances of the switches depend on the voltage.

- **Temperature**
  Many electrical circuit level parameters of the components (eg. on-resistance of semiconductors, parasitic capacitance) are temperature dependent. The operating temperature of each component is obtained in the *Thermal domain*.

- **Layout parasitics**
  The parasitic inductances and capacitances of the layout interconnections can resonate with the semiconductor device and package parasitics, resulting in voltage and current overshoot and ringing at the switching instances [26]. These parasitics are determined by the spatial design conducted in the *Mechanical domain*.

- **EMI design**
  The design process in the *EMI domain* determines the passive components required for the filtering of the EMI noise. These components are part of the electric circuit and hence, their design depends on the V-I characteristics.

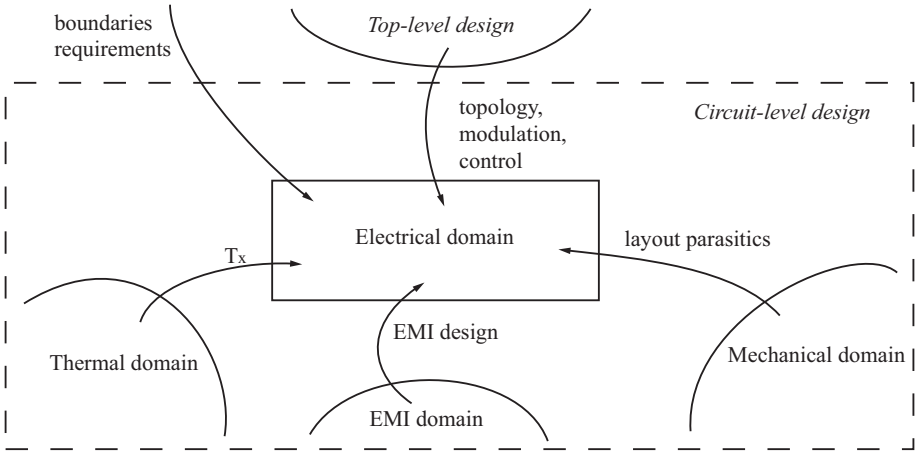


Figure 2-13: Electrical domain dependencies

Electrical modeling considerations

The purpose of the electric circuit model is to estimate the electrical characteristics of the converter, determine the passive elements and determine the electrical properties used in the design of the appropriate components. From this information, the power density and efficiency can be evaluated.

Regarding the modeling of the semiconductor parameters, a time domain representation of the switching behavior will give the current and voltage values at the switching instances and during conduction, in order to obtain the operating points which define the semiconductor parasitics. Assuming the piecewise linear model of the switching waveforms of the active semiconductors [12] (see Figure 2-14), the waveforms over the shaded areas represent the operating points used for the di/dt and dv/dt transients and losses calculations. The model will require the device characteristics and the dependence of the parasitics on voltage and current, which can be obtained from the manufacturer datasheet or measurements.

The semiconductor technology will determine the parasitics of the device and the switching pattern will be shaped by choices regarding the switching frequency, layout parasitics and gate drive circuit parameters, for instance the external resistor connected at the gate of the switch. As a result, the time domain modeling of the switching and losses calculations are driven by the design variables referring to component technology, switching frequency and gate drive. However, the losses and switching times can also be obtained directly from the manufacturer's datasheet, when given. In this case, scaling of the given data is required according to the application operating points. This method gives good accuracy for a first order estimation, since the test circuit of the measured data is different from the circuit in the application. However, the parameter scaling must include the design variables values to achieve more accurate results for the application.

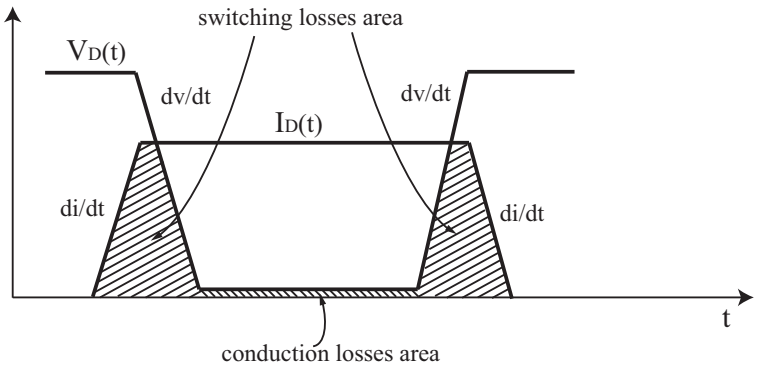


Figure 2-14: Piecewise linear approximation of the semiconductor switching waveform for transients and losses calculation.

On the other hand, higher accuracy is achieved with detailed analytical models, such as in [26], where the parasitics of the circuit and the device packaging are included in the models, to account for the overshoot and ringing phenomena. However, such modeling is powerful only if the parasitic components of the circuit are known, hence it is more useful to be used at a second stage in design, where the converter circuit is fully defined.

Furthermore, the semiconductors switching waveform contains the information needed for the calculation of the currents and voltages for the sizing of the passive components. For the passives calculation, representation of the circuit in the frequency domain is particularly handy. For the frequency domain modeling the fast Fourier transform (FFT) can be used. With computer-aided tools, such as MATLAB [27], both the FFT and the inverse FFT (IFFT) can be calculated, to convert the signals back to the time domain if required. As a result, the capacitor and magnetics values and losses can be calculated in the frequency domain by modeling the excitation and parameter values for every harmonic.

Specifically, the frequency dependence of the capacitors' losses is determined the equivalent series resistance (ESR) of the capacitor, expressed by two general terms: an ohmic term (R_Ω) due to the resistive losses in the metallic parts and dielectric losses represented by the dissipation factor $\tan\delta$ of the dielectric material divided by a factor of frequency ωC [15]. The values of ESR and $\tan\delta$ are given for a frequency range, which gives very good accuracy for the losses. However, better accuracy can be obtained if the geometry and material characteristics of the capacitor metallic parts are taken into account [15] or from test measurements of the capacitors parameters, as was discussed in [28].

Finally, both winding and core losses of the magnetic components are frequency dependent. The losses in the magnetic core material are derived from empirical equations [29][30] for different material types, which are based on curve fitting of measurements to derive the flux, temperature and frequency dependency of the losses. Considering the winding losses, the dependency on the high-frequency content of the current can be modeled analytically by considering the skin and proximity effect in the conductors [29].

2-3-4 EMI domain

The *EMI domain* deals with the physical phenomena related to the electromagnetic compatibility (EMC) of the converters. The switching operation of power electronics produces EMI noise that is emitted through the free space to other equipment (radiated EMI) and transmitted through the circuit connections (conducted EMI) [31]. As a result, high frequency currents coming from the converter operation interfere with the utility and affect the operation of other equipment connected to the same power bus, or interfere with signaling and communication systems.

The radiated EMI is difficult and impractical to predict. On the other hand, conducted EMI can be estimated, if the defining aspects of the electromagnetic perturbations are known. The objective of the *EMI domain*, is to identify the sources and propagation paths of conducted EMI, investigate the key parameters that influence the converter behavior in this domain and take the appropriate measures in order to suppress the noise to the levels specified by the conducted emission regulatory limits.

EMI noise source and propagation

When the switches are fast switched on and off, PWM voltages appear at the semiconductors as the result of the high dv/dt transitions. In addition, fast di/dts are also created as a result of the switching operation, that imply many high frequency components. The outcome is capacitive coupling between adjacent conductors and inductive coupling through the mutual inductance of the source and victim current loop [32]. As a result, the fast voltage and current transients propagate in the circuit through the coupling of parasitic capacitances and inductances. To simplify the conducted EMI, two mechanisms are considered [33]: the common-mode (CM) noise and differential-mode (DM).

CM is the noise flowing from the power lines to the ground and back to the power lines, and is evenly distributed between the phases, as shown in Figure 2-15. The source of this mechanism is defined as a voltage source, based on the voltage transients waveform of the switches. Depending on the grounding, the propagation path of CM changes and so does the CM noise. The DM noise is circulating through the power leads of the converter, hence is independent of the grounding and does not make any contribution to the noise flowing through the ground. It is considered a current source that consists of the converter input current. In the end, the total EMI noise is a combination of CM and DM components and is unbalanced between the phase lines.

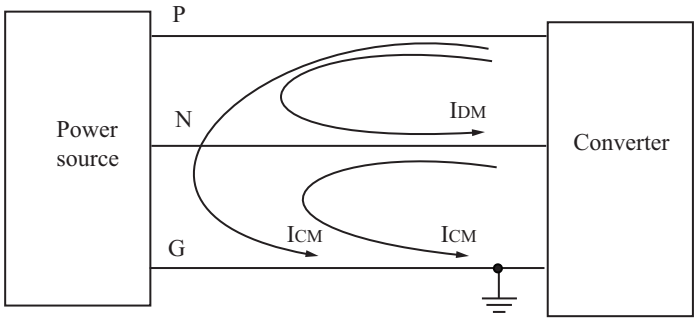


Figure 2-15: Common mode and differential mode EMI noise paths

EMI noise source dependencies

The CM and DM noise sources are defined by the transients that are shaped by the operation of the converter. The resulting switching operation affects the slope and magnitude of the current and voltage waveform at the switching instances, as well as the switching pattern of the pulses and the harmonic spectrum of the voltage and current. All this information is obtained in the *Electrical domain* and is summarized in the voltage and current transients waveforms which are an input to the *EMI domain*.

EMI propagation path dependencies

The generated EMI noise propagates in the circuit through the circuit impedances and parasitic capacitances and inductances which form a low impedance path for the CM or DM current at the coupling points. These parasitics are categorized as follows [34][32]:

- **Switch package parasitics**
  It is common to ground the heatsink and casing of the converter for safety reasons. As a result the die-heatsink-ground connection forms a parasitic capacitance to the ground, noted in Figure 2-16. This parasitic capacitance is considered through the *Thermal domain*. In addition, if discrete semiconductors or modules are used, stray inductances between the semiconductor die and packaging pins are also part of the EMI noise path. These parasitics are an input from the *Electrical domain*.

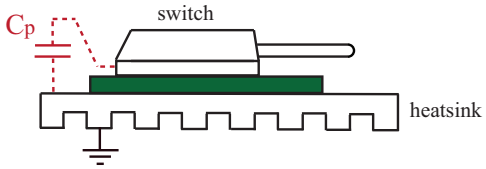


Figure 2-16: Switch parasitic capacitance to the ground.

- **Layout parasitics**
  These are stray inductances and capacitances depending on the circuit layout conducted in the *Mechanical domain* design.

- **Load parasitics**
  These parasitics depend on the wiring connection at the converter output and the structure of the load, which form a low impedance path for EMI. Typical cases include the parasitic components of cabling and machine impedances. Here, boundary of the *EMI domain* is extended to the load.

- **High frequency parasitics of passive components**
  At high frequencies, the inductive and capacitive behavior of the passive components is altered by their parasitics, as shown in Figure 2-17. For this reason, a parallel connection of capacitors is usually employed to obtain a large equivalent capacitance with low parasitic inductance. For magnetics (transformers and inductors), careful design is required to achieve a low parasitic capacitance.

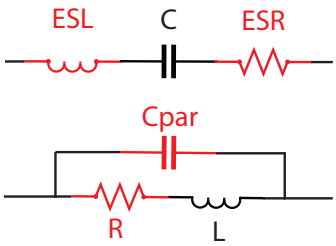


Figure 2-17: Capacitor (top) and inductor (bottom) lumped high frequency equivalent circuit.

Depending on the location, either between the phase lines or coupled to the ground connection, the impedances shape the CM or DM propagation path. By extending the boundary of the *EMI domain* to the *Electrical*, *Thermal* and *Mechanical domains*, the inter-linking of the domains is obtained (Figure 2-18). Taking these dependencies into account, the design of an EMI suppression filter can be included in the design process before the manufacturing stage.

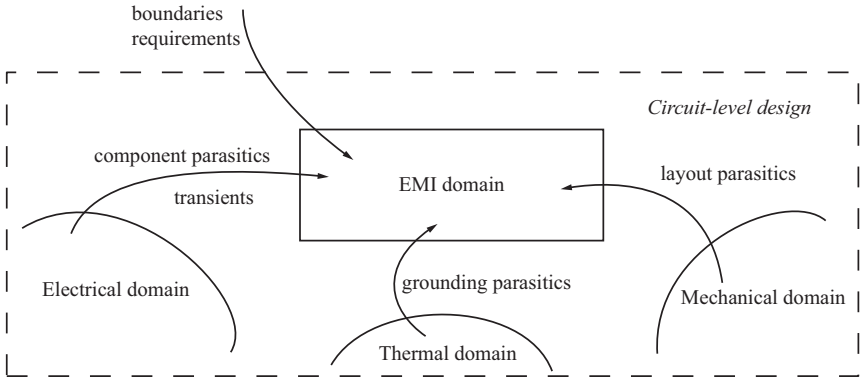


Figure 2-18: EMI domain dependencies

Suppression requirements and the Line Impedance Stabilization Network (LISN)

The requirement regarding the noise level at the power cords is that it is below the conducted emission regulatory limits for the application, as specified by the International Electromechanical Commission (IEC), the Federal Communications Commission (FCC) and the International Special Committee on Radio Interference (CISPR). Figure 2-19 presents some of these EMI standards, where the noise limit is expressed in dBuV. The aerospace standards for EMI are determined by the Radio Technical Commission for Aeronautics (RTCA), and are expressed in dBuA, which indicates the stringing requirements compared to other applications. To verify compliance to the EMI standards, the conducted emissions are measured using a standard network, known as Line Impedance Stabilization Network (LISN).

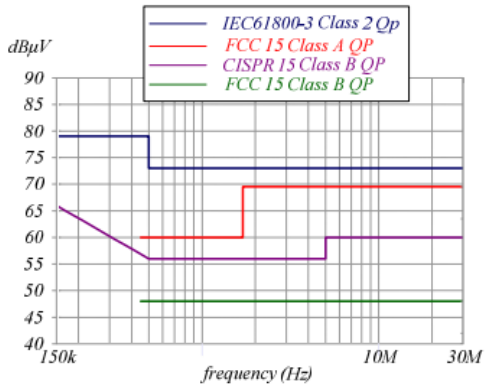


Figure 2-19: Conducted EMI standards [8].

The noise currents that exit the equipment under test (EUT) power cord conductors are measured with the conducted emission test [33]. However, the impedance seen looking into the power source varies over the measurement frequency range and affects the amount of noise exiting the EUT's power cord. Similarly, the amount of noise present in the measurement site varies as well and affects the measurement. For this reason the measurement of conducted EMI noise involves a standard network, known as Line Impedance Stabilization Network (LISN), that has a twofold role [33]:

- present a constant impedance (50 Ω) to the EUT's power cord outlet over the frequency range of the conducted emission test and
- block conducted emissions that are not due to the EUT, so that only the EMI of the product under test is measured

In Figure 2-20 the connection of the LISN for the conducted emission test in a 2-phase system for commercial applications is shown as an example. The power passes through the LISN to power the product and the conducted EMI is the voltage measured on the 50 Ω load by a spectrum analyzer connected to the LISN.

Using the ideal behavior of the LISN for any application, over the conducted emission regulatory limit, the compliance with the regulatory limits can already be included in the design process of the power electronic converter. This way a first estimation of the EMI noise

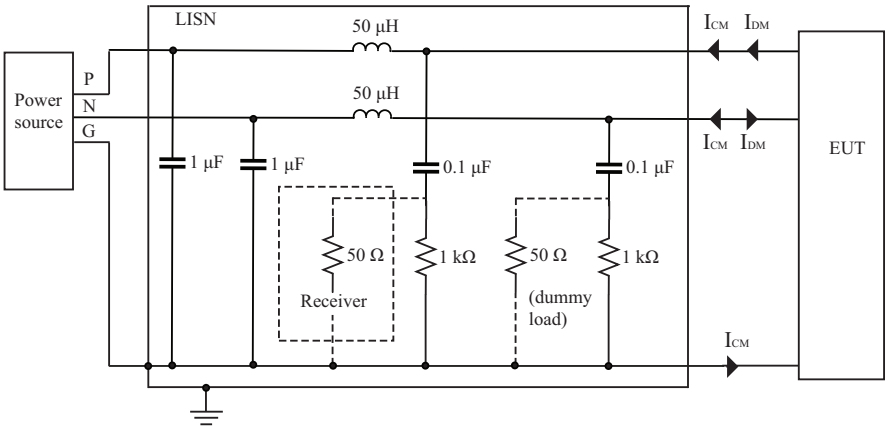


Figure 2-20: The LISN connection circuit in a 2-phase system.

can be made. The LISN can be represented by the ideal impedance of 50 Ω and the whole system can be simplified as an equivalent noise source, noise path and load, where the LISN serves as the load [35].

EMI filter design considerations

Having defined the EMI noise sources and propagation paths in terms of CM and DM components, the noise mechanisms are decoupled and can be studied separately. The CM and DM suppression filters can be easily designed, considering the respective EMI circuit as an equivalent network, shown in Figure 2-21. This network has the following characteristics:

- All contributing elements are represented by an equivalent impedance or admittance two-port network
- The noise source is the input in the global network
- The LISN is the load at the global network
- The model is developed in the frequency domain

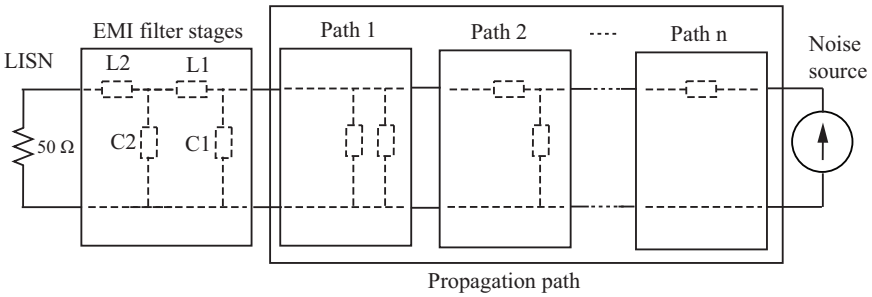


Figure 2-21: Cascaded two-port network conficuration for the CM and DM filter design.

The network of Figure 2-21 represents the single-phase equivalent with respect to the 50Ω resistor of the LISN, so that the calculated noise on the LISN can be directly compared

to the regulatory limits. To obtain the transfer function of the noise source to the measured noise on the LISN, the two-port configuration is used for the equivalent impedance and admittance components, shown in Figure 2-22. With this configuration the input is related to the output in a simple matrix form for the impedance and admittance with equations (2-1a) and (2-1b) respectively. This configuration is particularly useful when the two-port networks are connected in cascade, since the output port variables of one network are the input-port variables for the next network. As a result the transmission matrix of the overall network is the matrix product of the transmission matrices of the individual two-port networks in the cascade connection.

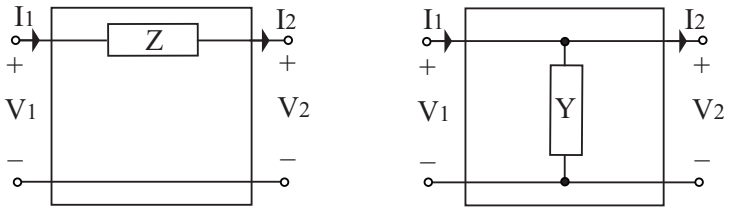


Figure 2-22: Two-port networks for equivalent impedance (left) and admittance (right).

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{2-1a}$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{2-1b}$$

With this simple configuration all passive elements of a sector are cascaded to obtain a local impedance matrix. In turn, the local impedance matrices are cascaded to obtain the global impedance matrix. The same principle is used to include the filter impedance network in the global matrix as unknown variables. Considering representation of the system in the frequency domain, the modeling offers simplicity and fast calculations compared to the time domain representation. Now the system can be easily solved to obtain the filter element values. The result of the design is fed to the *Electrical domain*, as was shown in section 2-3-3, to design the filter components and obtain their equivalent circuit and parasitics.

If greater accuracy for the parasitic networks is needed, larger cascaded networks can describe each block. In addition, the calculation effort is not increased dramatically since frequency domain calculations (FFT) are used, however, the resolution bandwidth of the FFT must be high enough to account for the high frequency transients. The filter component parasitics can also be included in the network, by replacing the component impedances in Figure 2-22 with the high frequency equivalent circuit. Finally, it is easier to consider different filter stages; the next stage is simply a new two-port network in cascade with the filter block.

2-3-5 Mechanical domain

The scope of the *Mechanical domain* involves the individual geometrical characteristics of the converter elements (volume and weight), their relative position in space and the circuit interconnections. The content of this domain includes the spatial design of the converter,

the effect of the domain dependencies on the design choices and evaluation of the converter regarding volume and weight.

Spatial design dependencies and considerations

The spatial design refers to the volumetric distribution of the components and their circuit interconnections. It is affected by a number of parameters regarding the geometrical characteristics of the converter components and environment, identified as:

- **Mechanical requirements and boundaries**
  The spatial design is constrained by mechanical system requirements that involve the geometry and mechanical characteristics of the physical environment outside of the converter. For example, the available space for the converter placement, vibrations, shock, mounting surfaces etc. This includes volume constraints for the total converter as a system.

- **Electric components geometrical features**
  Since the converter consists of discrete components which have different shapes and packaging parts and they do not fit with each other. This results to unoccupied space in the converter enclosure and non-optimal geometrical distribution or layout that unnecessarily decreases the power density. The geometrical characteristics of the components are obtained from the design in the *Electrical domain*.

- **Circuit connections**
  The circuit connections defined in the *Electrical domain* drive the design of the converter layout.

- **Thermal management geometrical features**
  The spatial design includes the geometrical characteristics of the heat dissipation mechanisms designed in the *Thermal domain*, which also contribute to the total volume and weight of the converter.

- **Connection equipment**
  The mechanical connection and stresses of the components are determined by the available parts (bolts, springs etc) from the database.

Taking into account these dependencies, the spatial design is conducted to determine the relative position of the components, the layout interconnections and the packaging connections. The objective is to place the components such that the layout parasitics are minimized and a minimum volume of the system is obtained. In addition, previous work shows that manipulation of the heat path by optimizing the spatial layout of components leads to high power density designs [36][37][1]. In addition the converter can be evaluated regarding volume and weight. However, these objectives are hindered by the non-optimal fitting of the components.

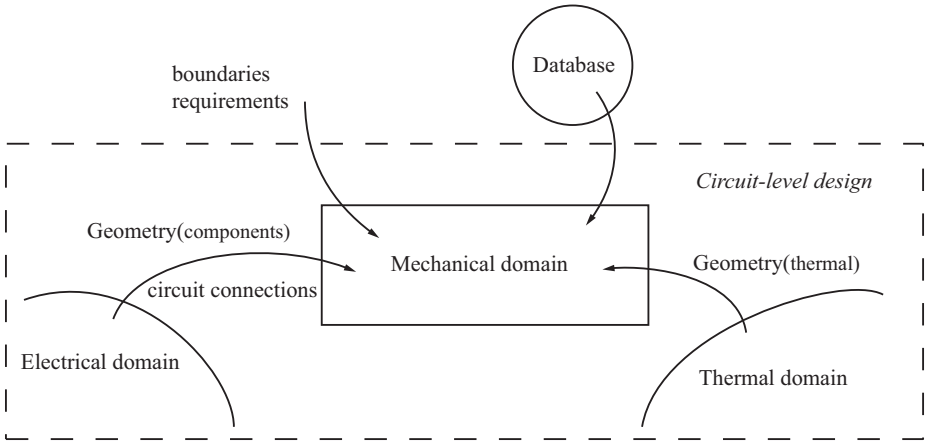


Figure 2-23: Mechanical domain dependencies

2-3-6 Thermal domain

In the *Thermal domain* the heat transfer phenomena of the converter are considered. The converter operation comes with losses which result to a temperature rise of the components. However, the converter must operate bellow the components' maximum operating temperature, hence a thermal management is required that is effective for all operating points, steady-state conditions and transient thermal behavior. The objective of this domain is to determine the heat transfer mechanisms of the converter, define the key factors which affect the thermal behavior and design a heat transfer path such that the converter operates within the temperature limits.

Heat transfer mechanisms

The heat generated by an element can be transfered to the element's environment by three heat transfer mechanisms: conduction, convection and radiation. The principles and physical laws that define these mechanisms are briefly described as follows.

- **Conduction heat transfer**
  It is the energy transfer from a high temperature region to a low temperature region of a body along a temperature gradient [30], as shown in Figure 2-24. The heat transfer rate q [W] is proportional to the body thermal conductivity λ [W/m^{o}C], the cross-sectional area A [m^2] through which the heat is transfered and the temperature gradient $\frac{\partial T}{\partial x}$ in the direction x [m] of the heat flow, according to Fourier's law:

$$q = -\lambda \cdot A \cdot \frac{\partial T}{\partial x} \tag{2-2}$$

- **Convection heat transfer**
  The physical mechanism of convection is related to heat conduction through a thin boundary layer of fluid (air, water, etc) adjacent to the heated body surface [30], shown

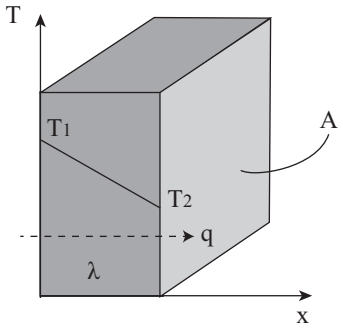


Figure 2-24: Conduction heat transfer

in Figure 2-25. A simple expression of the convection heat transfer is given by Newton's law of cooling:

$$q = h_c \cdot A \cdot (T_s - T_a) \tag{2-3}$$

where h_c [W/m$^2{}^o$C] is the convection heat transfer coefficient of the fluid, T_s [^{o}C] is the surface temperature of the body and T_a [^{o}C] is the ambient (fluid) temperature.

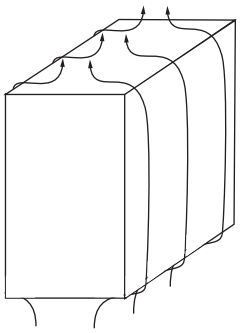


Figure 2-25: Thin boundary layer in the convection heat transfer mechanism

If the movement of the fluid is caused only by the density gradients at the boundary surface then the convection is called *free* or *natural convection*. If there is an external source of movement, eg. a fan blowing air, then heat transfer mechanism is called *forced convection*. The type of convection in combination with the temperature and the fluid properties determine the convection heat transfer coefficient h_c. Specifically, this relationship can be expressed with empirical functions of a set of characteristic dimensionless numbers, namely the Nusselt number (Nu), Grashof number (Gr), Prandtl number (Pr) and Rayleigh number (Ra) [38]:

$$h_c = f(Nu, Gr, Pr, Ra) \tag{2-4}$$

- **Radiation heat transfer**
  In the case of heat transfer by radiation, no intermediate medium is needed, but the heat transfer is electromagnetic radiation. The Stefan-Boltzmann law of thermal radiation describes this heat transfer mechanism [30]:

$$q = \epsilon \cdot \sigma \cdot A(T_1^4 - T_2^4) \tag{2-5}$$

where ϵ is the emissivity of the radiating surface, σ is the Stefan-Boltzmann constant, A is the radiating area and T_1, T_2 are the absolute temperatures of the hot body and the enclosing body respectively.

The key parameters in every mechanism are the material heat conductivity in conduction, the fluid properties expressed by the heat transfer coefficient in convection and the material emissivity for radiation heat transfer. In addition, heat transfer is always proportional to the body area. The dependencies of these parameters on converter design aspects, as well as the links to other factors which determine the thermal behavior of the converter are discussed in the following paragraph.

Thermal management dependencies

In order to obtain the temperature difference ΔT between a component in the converter and the ambient, it is required to identify the heat transfer, source and path properties. These properties depend on the following factors:

- **Component losses**
  The heat transfer rate q in (2-2), (2-3) and (2-5) represents the heat source of the converter components. It consists of the component losses determined in the *Electrical domain*.

- **Ambient environment**
  The characteristics of the converter ambient are the thermal boundary of the converter as a system and are defined by the application requirements. They are reflected on the heat transfer coefficients.

- **Spatial design**
  The heat path is determined by the geometries of the components and their relative position [1] and is obtained from the spatial design in the *Mechanical domain*. These parameters consist the thermal coupling of the components, where the heat generated by an element affects others adjacent to it.

- **Material thermal properties**
  The heat path manipulation also involves selection of the thermal conducting materials from the database and heat transfer mechanism, for example heatsink, fans, thermal paste etc. Their properties determine the coefficients of the heat transfer equations, but also the geometries of the respective elements which are linked to the *Mechanical domain* and included in the spatial design.

By linking the *Thermal domain* with the electrical and mechanical parameters, the boundary of this domain is extended, so that a comprehensive view of the system thermal behavior is achieved. The designed heat transfer mechanism in this domain will determine the component temperatures and the geometrical characteristics of the thermal management.

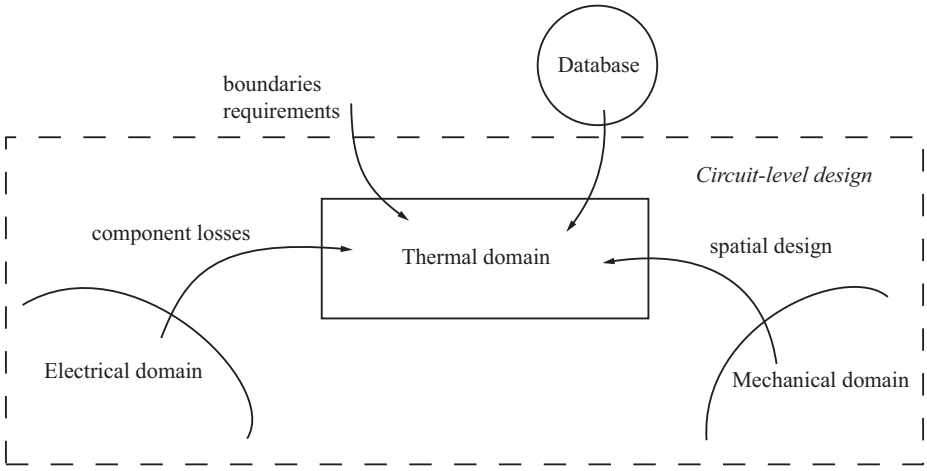


Figure 2-26: Dependencies of the Thermal domain.

Thermal modeling considerations

In the modeling of the thermal behavior of the converter, electrical and mechanical aspects are included. The geometries of the elements are incorporated to the heat transfer coefficients (thermal-mechanical coupling). In addition, the heat transfer mechanism considers equivalent resistor networks [37] (electrical-thermal coupling), as illustrated in Figure 2-27. In this model an arbitrary number of nodes of constant temperature is considered, assuming that the temperature is unequally distributed. The resistor is determined considering thermal-electrical analogy to Ohm's law

$$R_{th} = \frac{\Delta T}{\Sigma P} \tag{2-6}$$

where ΔT is the difference between the two nodes and ΣP is the sum of losses through the element.

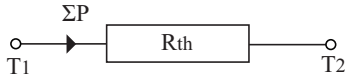


Figure 2-27: Electric equivalent model of the convective heat transfer mechanism

Specifically for the conduction heat transfer, from (2-2) and (2-6), considering a simple cuboid structure shown in Figure 2-24, the equivalent thermal resistor R_{th} between two nodes is obtained:

$$R_{th} = \frac{l}{A\lambda} \tag{2-7}$$

Considering the thermal coupling between all nodes in space, the two-dimensional model can be extended to three dimensions, illustrated in Figure 2-28. This 3D system can be developed for any number of x, y, z nodes, if it is brought to the matrix form

$$\left[\ P\ \right]_{(xyz)\times 1} = \left[\ \tfrac{1}{R}\ \right]_{(xyz)\times(xyz)} \left[\ T\ \right]_{(xyz)\times 1} \tag{2-8}$$

where P is the vector of power dissipated at each node, T is the vector of temperature at each node and R is the map of the thermal resistors between the nodes. Solving 2-8, the

temperature at each node in the component can be easily obtained and compared to the maximum allowed operating temperature.

The accuracy of the thermal modeling depends on the resolution of the temperature nodes in the components regarding conduction heat transfer. Moreover, the accuracy of the thermal conductivity of materials and pressure applied on them affect the accuracy of the calculations. In addition, a capacitive equivalent model[12] can be used to consider the transient thermal response during overload conditions or power-up and -down of the converter.

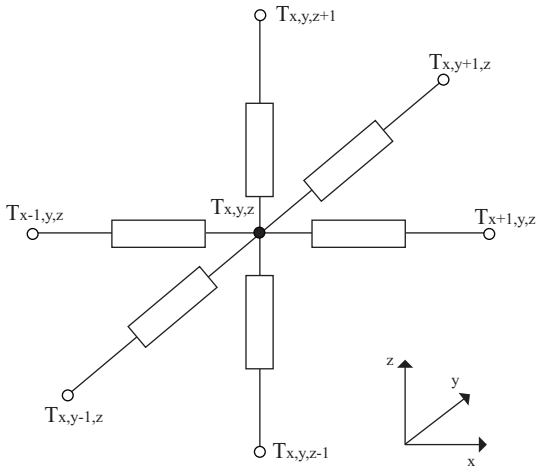


Figure 2-28: 3D thermal resistor network

2-3-7 Summarizing the interdependencies in the converter design

In sections 2-3-1 to 2-3-6 the links between the converter design aspects have been investigated. These links constitute the interdependencies between the design levels and domains, based on which the converter design methodology is developed. The interdependencies are demonstrated in Figure 2-29.

Looking from a top-down view, the application *boundaries* and *requirements* are introduced to both *Top-* and *Circuit-levels*, implying also connection to each of the design domains in *Circuit-level design*. The same principle follows the connection from the component *Database*. The coupling between *Top-level* and *Circuit-level desing* refers to the topology, modulation and control selection and the feedback regarding the performance of the design. If optimization is employed, the loop is closed by the values of design variables selected in the optimization, which refer to both design levels. In the *Circuit-level design*, the electro-thermal coupling is determined by the losses and temperatures of the components. The interdependencies between the *Electrical* and *EMI domains* consist of the transients and parasitics from the electrical side, and the EMI design (L and C components) from the EMI side. In addition, the dependency of the *EMI domain* on the layout parasitics from the *Mechanical domain* is included. Moreover, the grounding parasitics are an input to the *EMI domain* from the *Thermal domain*. The thermo-mechanical coupling is shown from the linking of the geometrical characteristics of the heat dissipation mechanism and the spatial design between the *Thermal* and *Mechanical domains*. The electro-mechanical interdependencies consist of the electric circuit connections and layout parasitics. In addition, the geometrical characteristics

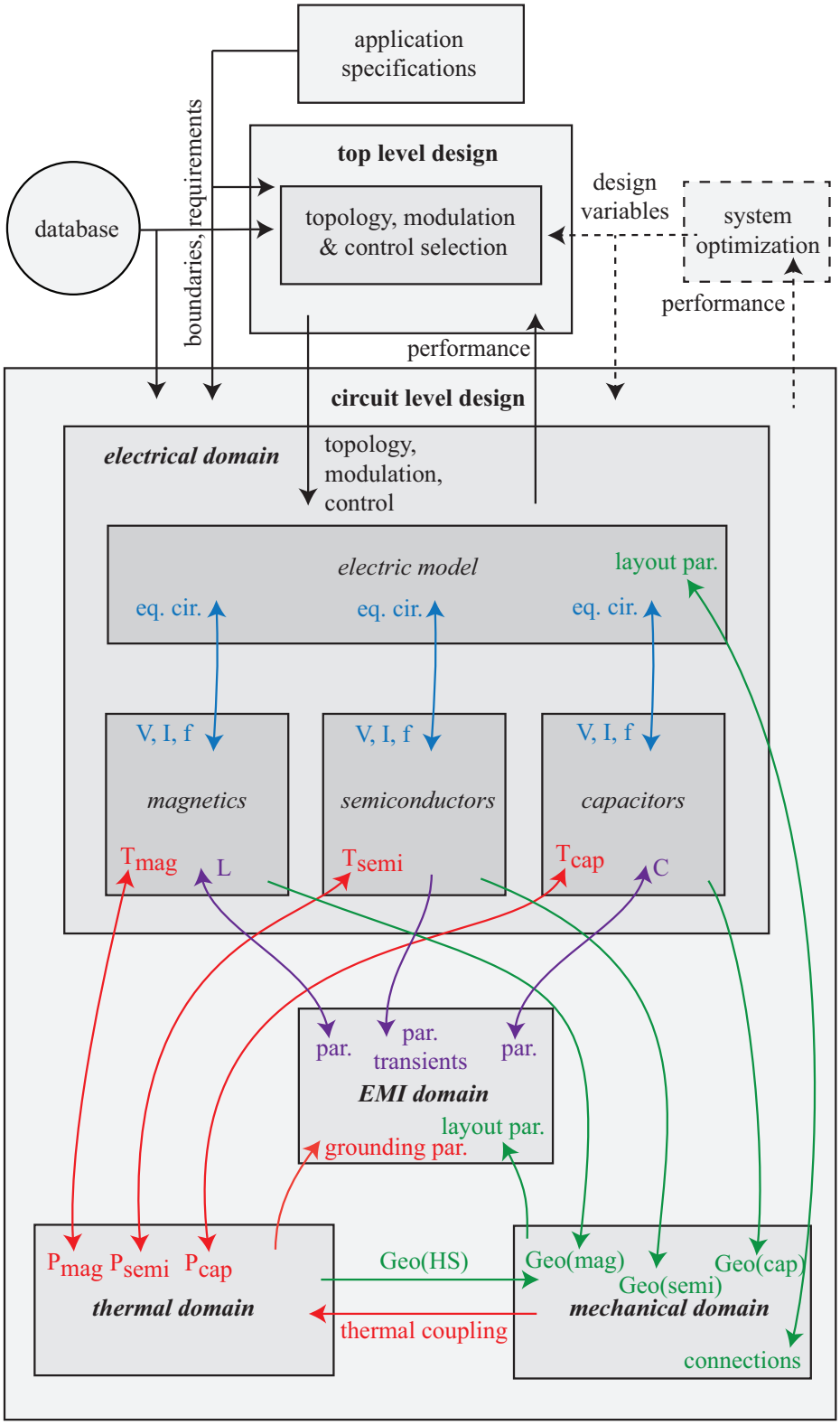


Figure 2-29: Converter design interdependences.

of the components are connected to the *Mechanical design*. Finally, the coupling between the component parameters and the electric circuit stresses is shown in the *Electrical domain*.

Design aspects in this work

Based on the presented methodology, the design of a power electronics converter is scalable in terms of application taking advantage of the design interdependencies. In the following chapters, the interdependencies will be shown qualitatively from the design of an aerospace inverter. Since optimization is not in the scope of this work, the design will be based on a parametric sweep of design variables, from which a set of final designs will be generated. Specifically, the design variables refer to switching frequency, gate resistor, semiconductor technology, which describe the *Circuit-level* design. The outcomes of the *Top-level design* will be considered fixed, hence the topology, modulation and control will not be considered as design variables, compared to the case in [7].

For the inverter design, the modeling methodology follows the considerations discussed in this chapter. The models are build such that scalability regarding the accuracy is possible. In addition, the analytical modeling is developed in a single computer-aided design tool, so that the transfer of the data between the domains is fast and no translation is needed. A tool which offers these features is MATLAB [27] and is chosen for this work.

2-4 Summary

In this chapter the background and motivation of this thesis is discussed. The advantages of virtual prototyping for power electronics design are addressed. The concept of multi-domain modeling is introduced and its advantages when used with optimization techniques. The related work on simulation-based and analytical equations-based multi-domain design methods is also discussed and compared. These methods constitute the basis for the design methodology for power electronic converters developed this thesis.

The multi-domain design methodology in this work is discussed in detail. The design levels and domains are identified and their dependencies are investigated. The role of the application boundaries and requirements is discussed and the link to the database is addressed. Moreover, design and modeling considerations regarding each domain are proposed. The interdependencies of the converter design are determined, showing the links and boundaries for each of the design aspects.

The methodology discussed in this chapter will be applied to the case study of an aerospace inverter. Based on this methodology, the *Top-level design* of the inverter will be described in Chapter 3. In Chapter 4, the *Circuit-level design* of the inverter will be described in detail.

Chapter 3

Aerospace inverter - top level design

3-1 Introduction

In the previous chapter, a design methodology for power electronics was discussed. Based on this methodology, the design of an inverter has been conducted. The specifications for this inverter are set by Aeronamic.

This chapter focuses on the *Top-level design* of the inverter, while the *Circuit-level design* is presented in the following chapter. Initially, the specifications and constraints of the application are presented and the boundaries and requirements for the design are determined. After that, the selection process of the appropriate topology is presented, based on a classification of the available topologies. Hereafter, the selection of the modulation for the semiconductors switching is discussed, followed by the description of the control strategy of the converter. The latter is based on the operation of the load under the inverter limitations. The criteria and choosing process in each stage will be described in detail. The outcome of the design process in this chapter is a final design selection. This design will be considered fixed and will constitute the input to the *Circuit-level design*.

3-2 Case study - specifications and application constraints

The system to be designed is an inverter for a three-phase non-salient two-pole permanent magnet synchronous machine (PMSM) [39]. The design objective is to achieve a high power density design at minimum weight. The output power and load profile of the PMSM refer to a single operating point of 5 kW power at 150 krpm. The drive input voltage is a DC voltage source of 540 V grounded at 270 V. To achieve a fairly constant DC-link voltage, the input peak-to-peak voltage ripple is chosen at 0.5% of the DC-link voltage.

The machine characteristics are not set explicitly, but it is required that the short-circuit current in the windings is less than 5 times the nominal current. In addition, to prevent transferring power to the DC link in case of a failure of the inverter switches, the rectified

no-load back-emf voltage at maximum speed must be less than the DC link voltage. Hence, the machine inductance L_s and back-emf voltage V_{emf} are to be included as variables in the inverter design.

The EMI requirements for airborne equipment which apply to this project refer to the DO-160G category P standard of the Radio Technical Commission for Aeronautics (RTCA), which is illustrated in Figure 3-1. Furthermore, the DO-160G standard specifies a maximum current ripple of 14% of the DC-link current at the inverter input. The electrical requirements for the inverter are summarized in Table 3-1.

Table 3-1: Inverter drive specifications

Maximum speed	150 krpm
Maximum power @ maximum speed	5 kW
DC link voltage	540 V
DC-link voltage ripple	0.5% V_{dc}
DC-link current ripple	14% I_{dc}
Short-circuit current limit factor (I_{sc}/I_{rated})	≤ 5
Rectified back-emf voltage limit	$\leq 540\ V$

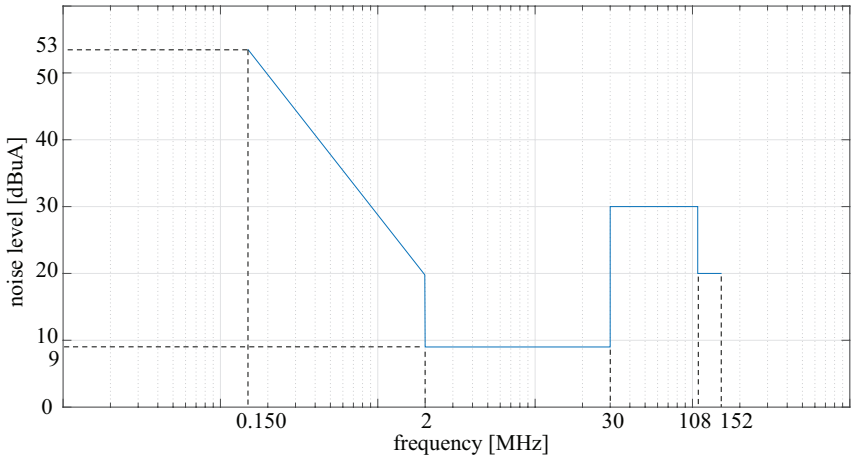


Figure 3-1: The RTCA/DO-160 Category P standard for EMI noise in airborne equipment.

In addition, the thermal environment of the inverter refers to operation at (-40, 70) ^oC ambient temperature, while the air pressure is considered at sea surface level. There are no constraints regarding the mechanical environment of the converter, hence the mechanical design is affected only by the power density and weight requirements. Moreover, the aerospace applications area poses additional constraints regarding the technology of components and materials that can be used. Electrolytic capacitors are not suitable for low pressure environments, have low life time and low reliability, which conflict with aircraft safety standards. Thermal paste is also not allowed as a high thermal conducting material for reliability reasons.

The block diagram of the considered system is illustrated in Figure 3-2, including the EMI filter, DC-link, inverter topology, power source and load connection. The reasoning behind the decision making process at each step will be presented in detail in the following paragraphs, starting from the topology selection.

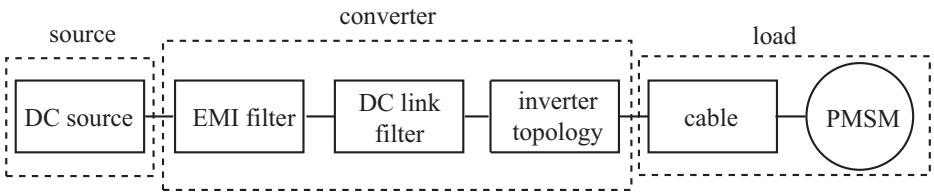


Figure 3-2: Block diagram of the inverter system, including source and load connections.

3-3 Topology selection

There is a wide variety of inverter topologies available, each suitable for specific applications. The objective of this section is to identify the available topologies, determine the candidate topologies for the application and choose the most appropriate for the specifications of the thesis project. In the first part of this section the inverter topologies are classified according to their operational characteristics, and the candidate topologies are selected with respect to the application requirements. In the second part, the basic characteristics of the candidate topologies are presented. Finally, the candidate topologies are compared according to more specific criteria and a final topology is selected to be designed in this thesis project.

3-3-1 Classification of the available topologies

The most suitable topologies will be chosen from a bank of the basic circuits of available inverters [9][40][41]. The circuits are classified with respect to the circuit connections and the switching operation. The selection for the candidate topologies will be performed based on the following general criteria, which come from the application requirements:

- appropriate for motor load
- low voltage and low power operation

The inverter topologies classification with respect to circuit connections is based on [9] and is conducted according to two parameters: the number of levels and the load requirements. The classification of the inverters based on the switching conditions of the power semiconductors, distinguishes the topologies in hard switching and soft switching. For the soft switching topologies the classification is based on the analysis in [40]. In the following paragraphs the main characteristics of each topology are briefly discussed and the reasoning for the candidate topologies selection is presented.

Circuit topology classification

The topologies regarding the voltage levels are distinguished in 2-level and multi-level converters. The number of levels refers to the waveform of the output voltage, where the fundamental sinusoid is obtained by a stepped waveform coming from a division of the DC link voltage in steps (levels) according to the designated topology of the circuit. The load requirements refer to the inductive or capacitive nature of the load. The number of levels defines the inverters as

two-level and multi-level inverters and the load requirements define voltage source inverters (VSI) and current source inverters (CSI).

2-level inverters

The 2-level inverter topology is the fundamental inverter topology (see Figure 3-3 (a)). It consists of two switches on each inverter leg and produces an output voltage waveform with two values. In this case the switches must withstand the full DC link voltage and the output voltage has high dv/dt. It is an inverter widely used for low power operation and motor drivers, hence it is considered a candidate topology for the application.

Multi-level inverters

The multi-level topology [9] includes an array of semiconductors and capacitors and generates an output voltage with a stepped waveform, e.g. a three-level inverter generates three values of voltages and so on. The main multi-level topologies are distinguished in diode-clamped, capacitor-clamped and cascaded multicell inverters (see Figure 3-3 (b), (c) and (d)). These topologies generate a staircase output waveform, whose harmonic distortion is low. Furthermore, multi-level inverters have very low common-mode voltage and can operate with a lower switching frequency. However, the control is more complex as the number of levels increases and voltage imbalance problems appear [9]. The main advantage of multi-level inverters is that, by increasing the number of levels, the power semiconductors will withstand reduced voltages. For this reason, they are oriented for medium and high power applications, where the breakdown voltage limit of the semiconductors makes the usage of the 2-level inverter impossible. However, for the low power requirements of the case study, the 2-level inverter meets better the placed criteria, hence multi-level inverters not considered.

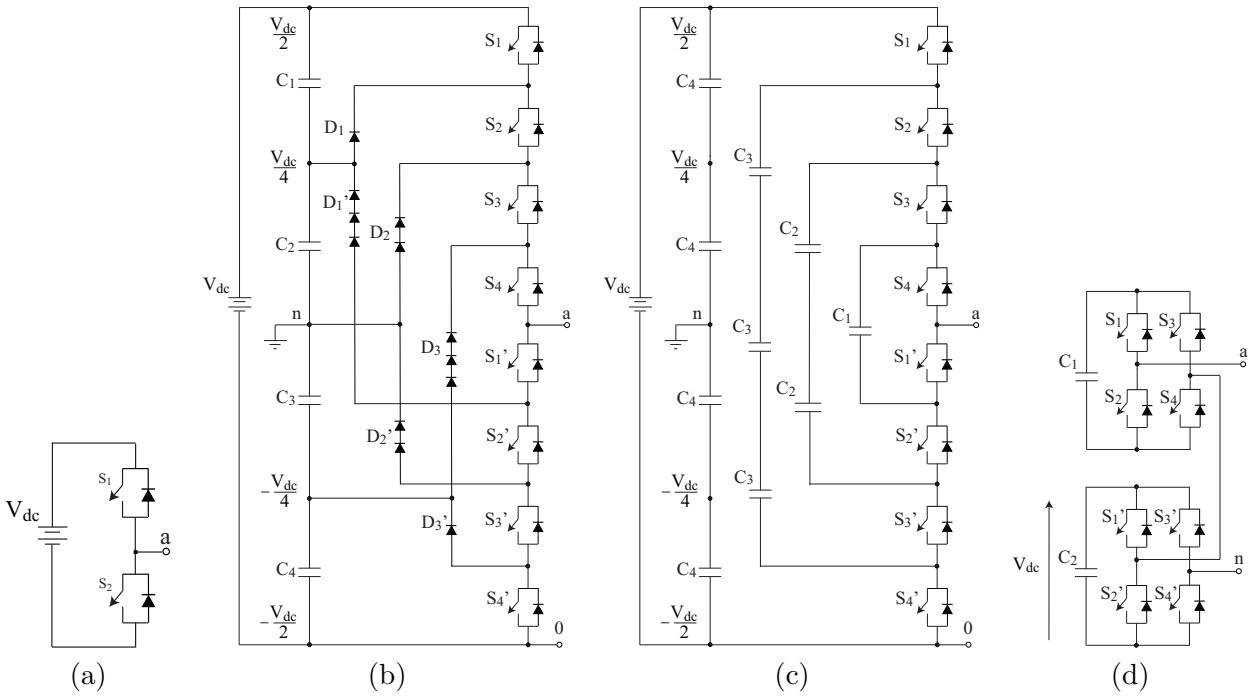


Figure 3-3: Phase leg of the 2-level inverter (a) and the multi-level inverter topologies diode-clamped (b) capacitor-clamped and (c) cascaded multicell 5-level (d) inverters [9].

VSI and CSI topologies
In cases where the DC supplies are derived from a source such as a battery or a rectified voltage supply, the inverter is designated as a VSI. This type of inverter is preferred for inductive loads. In case a capacitive load is driven by a VSI, additional inductive filters must be added to the output of the inverter. If the switches are connected to a stiff current source, then the inverter is determined as a CSI. Capacitive loads require CSI topologies. However, filters in the output for both cases reduce the performance of the system. As a result, the VSI inverter configuration for inductive load is the suitable candidate regarding the application load conditions.

Based on the previous discussion, the 2-level VSI configuration has been chosen regarding the circuit connections classification of the inverter topologies. This configuration is suitable for the low power requirements of the application and the motor load specifications. The classification presented in this paragraph is summarized in Figure 3-4.

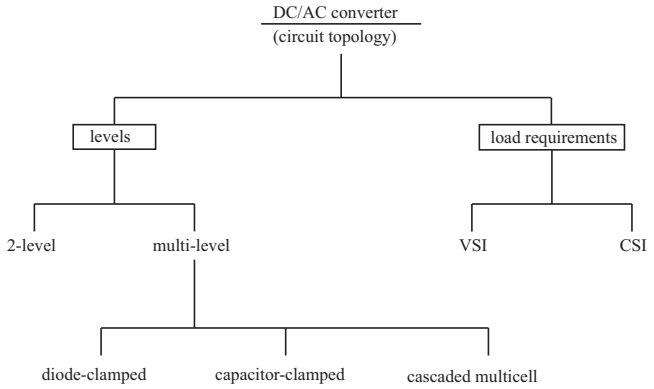


Figure 3-4: Inverter topologies classification regarding the circuit topology.

Switching conditions classification

The classification of inverters regarding the switching conditions of the active semiconductors distinguishes the topologies in hard switching [12] and soft switching [40], illustrated in Figure 3-5. The reasoning for the suitability of each category for the application is briefly discussed in this paragraph.

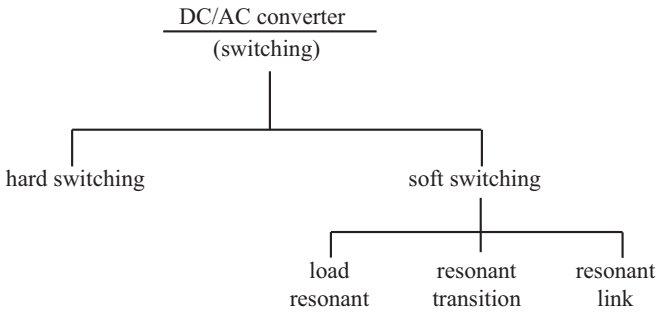


Figure 3-5: Inverter topologies classification regarding switching.

Hard switching topology
In hard switching topologies, the power semiconductors turn on and off at full voltage and current conditions. Hence, the voltage stresses and losses can be significant for high power applications. Since the output power specification for our application is low, and the hard switching topology can be used as a motor driver, it is considered a candidate topology.

Soft switching topologies
Soft-switching [40] aims to utilize high-frequency switching in order to use the advantages of reduced audible noise and easily filtering of higher harmonics, while reducing switching losses and EMI. In the soft-switched topologies, a high-frequency resonant network is added to the conventional hard-switching pulse width modulation (PWM) topology. The resonant network consists of passive elements L and C, or it can also include auxiliary diode(s) and switch(es). As a result, the switch voltage or current swings and crosses zero points and thus creates the soft-switching conditions for the power devices: switching at zero voltage conditions, referred to as zero voltage switching (ZVS), and at zero current conditions, referred to as zero-current switching (ZCS). The ZVS and ZCS mode is defined by the topology of the soft-switching converter.

The classification of the soft-switching topologies is based on the location of the resonant network with respect to the hard switching topology. Hence, the topologies are defined as load resonant, resonant transition and resonant link inverters [40].

- Load resonant inverters
  An LC resonant tank is added at the load side in a series, parallel or in a combination of series and parallel schemes [40]. Since the resonant network is connected in the main power transfer path, the components must be rated for high voltage and high current, hence are not suitable for compact designs. This type of converter is intended for constant load applications and is not suitable for motor drives, hence is excluded.

- Resonant transition inverters
  A resonant tank is connected to the inverter bridge creating the ZVS or ZCS conditions. They are defined as:

  - Resonant pole inverters (RPI)
    The resonant circuit creates ZVS turn-off conditions for the switches with an LC configuration at the inverter leg output. However, the current rating for the switches is 1.2 times the rated load current. For motor drive applications, the machine load inductance provides the output filter, hence the RPI is impractical [42][43]. However, it is suitable for UPS applications where an output filter is a requirement. As a result, RPI is not considered among the candidates.
  - Resonant snubber-based inverters
    In this converter the resonant circuit is assisted by auxiliary switches, hence the converter is referred to as auxiliary switch commutated resonant pole inverter (ASCRPI). It can be used for motor load applications, so it is a candidate topology.
  - Quasi-resonant ZCS inverter
    This topology is the duality of the RPI. It is suitable for induction heating and constant load applications and as a result it is excluded from the candidate topologies.

  - Soft-transition PWM inverter
    The most representative converter of this category is the clamped mode resonant pole inverter (CMRPI). It is an improvement of the ASCRPI, and it is suitable for motor drive applications, hence it is a candidate topology.

- Resonant link inverters
  The resonant network is connected between the input dc source and the inverter bridge; hence, the input bus is oscillating. This type of converters are designated into parallel resonant and series resonant DC-link converters.

  - Parallel resonant DC-link inverter
    This category has many variations and improved topologies regarding control, however only the actively clamped resonant DC-link (ACRDCL) topology [42] will be considered as the most representative of this category. It is suitable for motor drives and is among the candidate topologies for the application.
  - Series resonant DC-link inverter
    It requires capacitive load hence additional components are needed. It is not considered among the candidate topologies, since its dual topology, the parallel resonant DC-link inverter matches better the placed criteria.

The resulting candidate topologies for the application are the hard switching, ASCRPI, CMRPI and ACRDCL 2-level voltage source inverters. The principles of operation of these topologies are briefly described in the following section.

3-3-2 The candidate topologies

Hard switching VSI (HSVSI)

The hard switching VSI is the fundamental inverter topology. It is a simple topology, composed of the fewest components possible. The three-phase circuit consists of a bridge of 6 switches and 6 antiparallel diodes [41], as shown in Figure 3-6. Usually the voltage is supplied

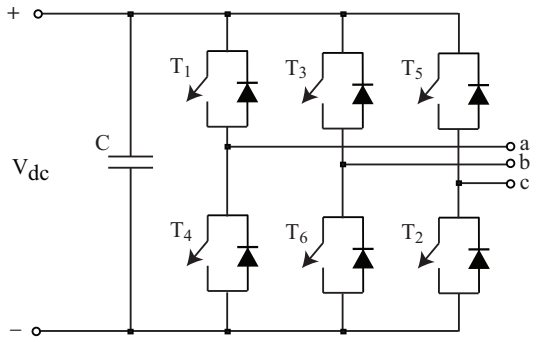


Figure 3-6: Topology of the hard switching VSI inverter.

by a large DC-link capacitor C. The voltage and current rating of the switches and diodes refers to the DC-link voltage and load current conditions. The switching operation involves switching at full voltage and current, including the reverse recovery current from the diodes during the turn-on instances.

Actively clamped resonant DC-link inverter (ACRDCL)

In this topology the resonant network is connected between the the DC voltage source and the inverter bridge and makes the link oscillate [42]. The result is ZVS soft-switching of the switches. An auxiliary switch S_r and a store voltage capacitor C_c are included in the conventional parallel resonant DC-link circuit. The oscillation between the resonant inductor L_r and capacitor C_r creates a resonant voltage higher than the DC source V_{dc}. Hence, the voltage at the C_c capacitor is $(k-1)\cdot V_{dc}$, where k is the clamping factor (typically 1.2 – 1.4). The schematic of the ACRDCL topology is illustrated in Figure 3-7.

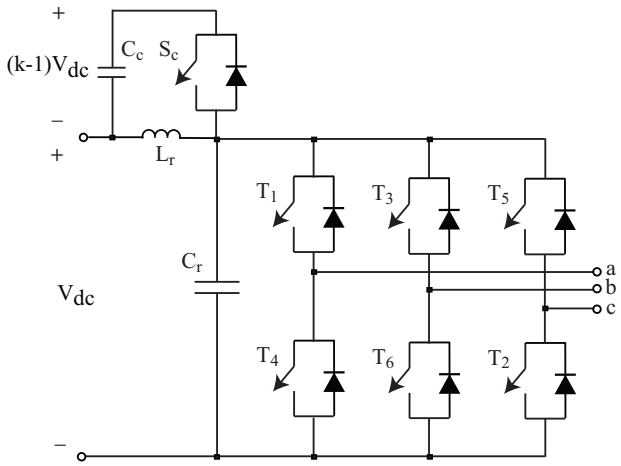


Figure 3-7: Topology of the ACRDCL soft switching inverter.

Clamped mode resonant pole inverter (CMRPI)

The CMRPI topology [44] utilizes a diode bridge as the auxiliary circuit in combination to the resonant circuit (L_r and C_r) to achieve ZVS conditions for the main switches. In this topology the switches' parasitic capacitance can also be used as part of the resonant capacitor C_r. The clamp diodes D_r clamp the voltage across the resonant capacitor and free-wheel the resonant current. The CMRPI circuit topology is illustrated in Figure 3-8.

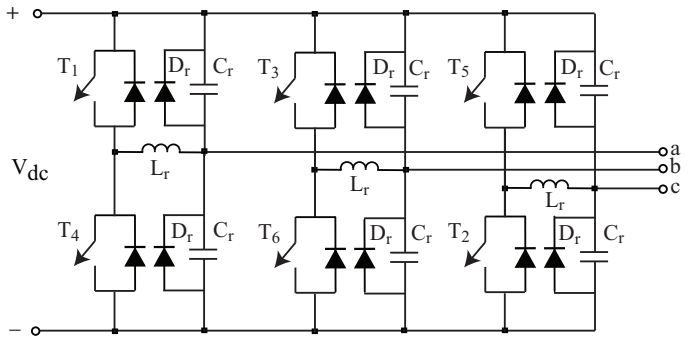


Figure 3-8: Topology of the CMPRI soft switching inverter.

Auxiliary switch commutated resonant pole inverter (ASRCPI)

The ASCRPI implements ZVS with three independent controllable resonant circuits [45]. The resonant circuit for each phase leg consists of an auxiliary control switch, the resonant inductor L_r in series with the control switch and resonant capacitor C_r in parallel with the main switch. In this case, the resonant inductor L_r is not part of the main power flow. The control switches (S_c) are bidirectional with reverse blocking diodes and control the direction of the resonant energy transfer. Since the auxiliary switches are not part of the main energy transfer, they have smaller power rating than the main switches. However, the antiparallel diodes of the main switches process both the load and resonant currents. The ARCPI circuit is shown in Figure 3-9.

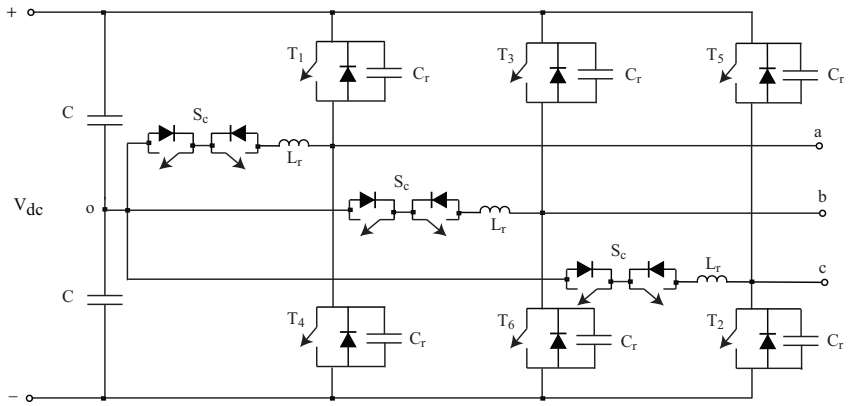


Figure 3-9: Topology of the ASCRPI soft switching inverter.

3-3-3 Selection of the appropriate topology

The selection process of the most suitable inverter will be discussed in detail in this section. The criteria for the topology selection are determined by the thesis objectives and application, and are summarized from most to least important as:

- efficiency
- complexity
- cost

The comparison of the four topologies is based on calculations for the efficiency and qualitative analysis for the complexity and cost. Regarding efficiency comparison, a first order estimation of the losses in each topology is conducted with analytical equations. The complexity comparison refers to the circuit and control required in each case, based on the characteristics of the respective circuits. In addition, a qualitative analysis is conducted for the cost of each topology, based on the components needed and their rating. A comprehensive comparison of the topologies would require a complete design of the converters, but this is outside of the scope of this section.

The selection process will be conducted by comparing the performance of the topologies with respect to each criterion individually. The results from each performance criterion will be summarized in the end and a final conclusion will be drawn for the selection of the most suitable topology.

Efficiency comparison

The comparison includes switching and conduction losses in the semiconductors and conduction of the passive components. Since the losses in the capacitors are negligible compared to the inductor losses in this case, only the inductors are taken into account. A first order estimation of the losses is possible by using simplified models of the components and the switching operation [44].

A preliminary calculation of the machine back-emf voltage and frequency is first conducted, according to specifications of Table 3-1. The back-emf voltage V_{emf} is calculated according to the rectifier operation limit of the inverter [12] and the frequency refers to the rated speed operation:

$$V_{emf} = \frac{V_{dc}}{\sqrt{3}\sqrt{2}} \tag{3-1}$$

$$f = \frac{p\ n_{rat}}{60} \tag{3-2}$$

where V_{dc} is the DC-link voltage, p is the pole pairs and n is the rated speed in rpm. The resulting machine parameters are 220.45 Vms back-emf voltage and 2.5 kHz operating frequency. These parameters will also be used later to determine the system operating points.

For comparison purposes, off-the-shelf IGBT switches and diodes from Semikron at rated power are used (see Appendix A). For the soft-switching topologies switches with larger semiconductor area are used compared to the hard switching topology, in order to reduce the conduction losses; the penalty for larger parasitic capacitance does not affect the switching losses in this case. This way, the advantages of each topology are utilized and the comparison is more clear. Assuming sinusoidal PWM [46], the switching frequency is chosen 10 times greater than the fundamental frequency, at 25kHz. The analysis is based on [44] and [47] and the models for the comparison, along with the passive component values, are summarized in Appendix A. Table 3-2 compares the efficiency for the candidate inverters at rated speed and power conditions. The respective losses per converter topology are illustrated in Figure 3-10.

Table 3-2: Efficiency comparison for 5 kW

HSVSI	ACRDCL	CMRPI	ASCRPI
97.94 %	91.76 %	94.04 %	97.74 %

The outcome of the losses comparison is that the HSVSI and ASCRPI topologies have the highest efficiency for the application. However they are comparable and it is difficult to conclude which inverter is more efficient. The ACRDCL and CMRPI topologies turn out to be inefficient, which comes from the fact that conduction losses are dominant in soft-switching topologies. On the other hand, the switching losses in all soft-switching topologies are negligible as expected, whereas they dominate in the HSVSI topology.

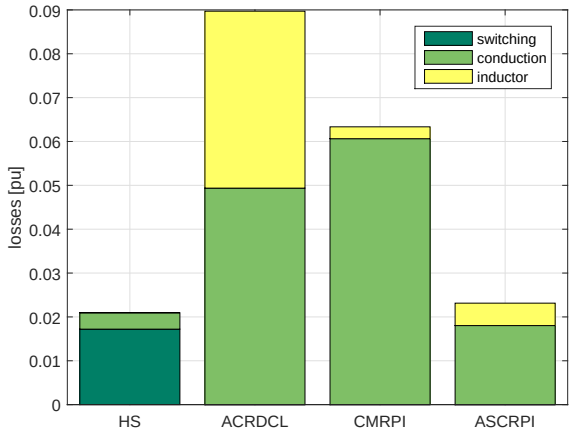


Figure 3-10: Comparison of the topologies' losses at rated operating conditions (5 kW).

The benefit from soft-switching is obvious at higher power levels, where the switching losses are more severe. A scaling of the application power level at 50 kW with increased current rating for the candidate topologies shows a clear disadvantage of the hard switching topology, as illustrated in Figure 3-11. In this case, the HSVSI losses are increased by 19% whereas the decrease in *pu* for the soft-switching topologies is around 70% (the efficiency is decreased by 0.5% for the HSVSI and increased approximately by 4% for the soft-switching inverters); hence the soft-switching topologies would be preferable for the high power range, as shown in Table 3-3.

Table 3-3: Efficiency comparison for 50 kW

HSVSI	ACRDCL	CMRPI	ASCRPI
97.5 %	98.24 %	98.23 %	98.85 %

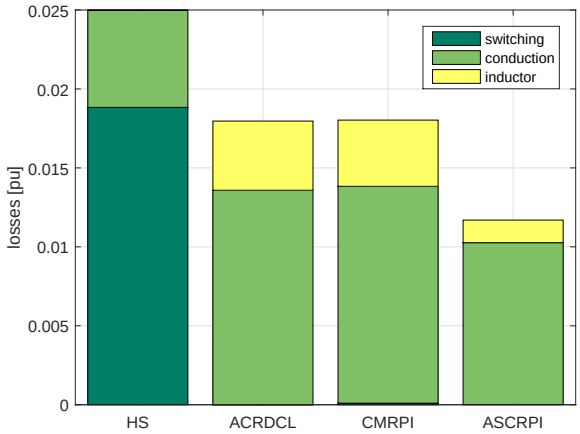


Figure 3-11: Comparison of the topologies' losses at 50 kW output power.

In conclusion, the low power application requirements designate the HSVSI and ASCRPI topologies as the most suitable. Since they have comparable efficiencies, either one can be selected with respect to efficiency performance.

Complexity comparison

The selection process regarding complexity of the topology includes the power circuit and control complexity. For the circuit comparison, the number of components and design effort are taken into account. As a result, the LC circuit design and sizing of the additional semiconductors for the soft-switching topologies increase the complexity. Moreover, the circuit analysis and calculation effort is more complex as the connections and switches increase.

In soft-switching, the control includes detection of the zero crossing points, hence it is more complicated. In addition, when the ASCRPI is used, the conduction times of the auxiliary switches are varied in each switching cycle, which makes the control of ASCRPI even more complex [40]. As a result, the most appealing solution considering complexity is the HSVSI topology. The comparative evaluation is noted in Table 3-4, where the number of dots represents the complexity scale.

Table 3-4: Complexity comparison

	HSVSI	ACRDCL	CMRPI	ASCRPI
circuit	•	• •	• • •	• • • •
control	•	• •	• •	• • •

Cost comparison

A first comparison regarding the components in the schematics presented for the candidate topologies is possible. The total requirement for passive components in the CMRPI topology is greater than the others (see Appendix A). However, the ASCRPI topology requires bidirectional switches hence its cost is increased. The most cost effective choice is the HSVSI which requires the least components. In addition, the efficiency comparison indicates less heat dissipation effort for the HSVSI and ASCRPI topologies. As a result these topologies are more appealing regarding thermal requirements. The relative cost performance of the basic circuit and thermal requirements for the topologies is summarized in Table 3-5. The comparison shows that in terms of cost the HSVSI topology is superior.

Table 3-5: Cost comparison

	HSVSI	ACRDCL	CMRPI	ASCRPI
circuit	•	• •	• • • •	• • • •
thermal	•	• •	• •	•

Conclusion

From the previous discussion it is shown that the most efficient topologies are the HSVSI and ASCRPI. Regarding circuit and control complexity and the cost performance, the HSVSI

topology has a clear advantage over the other candidates. It should be noted that this comparison considers only the main circuit elements. The design of the required EMI filter components is not included in the selection process. However, the soft-switching topologies have less requirement for EMI filtering due to smoothened transients, which in turn means less losses and lower cost of the EMI filter compared to the HSVSI. Such an evaluation is not possible at this stage, since a complete design of all the converters should be conducted. However, this is not the objective of this section. As a result, based on the previous discussion and the thesis objectives the HSVSI topology is selected for this project.

3-4 Modulation selection

The inverter must control the magnitude and the frequency of the AC output voltages. This is obtained by the switching operation which is determined by the modulation strategy [46]. The objective of this section is to present the key aspects of the modulation strategies regarding the reference signal and the carrier interval and select the most suitable technique for the application.

3-4-1 Classification of the modulation strategies

In order to produce a sinusoidal output voltage waveform at a desired frequency, pulse width modulation (PWM) [12] can be used. This technique varies the duty cycle of the converter switches at a high switching frequency f_s to achieve a target average low-frequency f output voltage. The AC voltage output amplitude is controlled by the modulation ratio m_a, defined as the ratio of the control signal amplitude to the carrier signal amplitude [12]. If sinusoidal PWM (SPWM) is used, a sinusoidal target reference waveform of low frequency f is compared against the high-frequency carrier waveform. This technique is simple and has minimum calculation effort because it only requires a comparison of two signals.

$$m_a = \frac{\widehat{V}_{control}}{\widehat{V}_{carrier}} \tag{3-3}$$

The same effect in switching times can be obtained by space vector modulation (SVM) [46]. The principle of space vector modulation is based on the fact that there are only eight possible switch combinations for a three-phase 2-level inverter. These combinations form the stationary vectors from which an arbitrary target output voltage vector can be formed by a summation of a number of these space vectors within one switching period $\Delta T/2$. SVM has the advantage of explicit identification of pulse placement as an additional degree of freedom that can be exploited to achieve harmonic performance gains. However, the switching times t_{on} and t_{off} of the switches must be calculated in each cycle for the reference vector and as the number of levels in the inverter or the switching frequency f_s increases, the complexity and computation effort increase dramatically.

The aforementioned modulation strategies usually use a fixed frequency carrier. However, programmed modulation strategies [46] can be used where the individual pulses are no longer constrained within a clock pulse window but can vary in width and position over a much wider interval. Because the computational effort needed to compute the switching angles

increases greatly with the number of switching angles to be calculated, these methods are combined with SPWM or SVM to complement these optimal methods. A classification of the modulation strategies with respect to the carrier interval and control reference signal is shown in Figure 3-12.

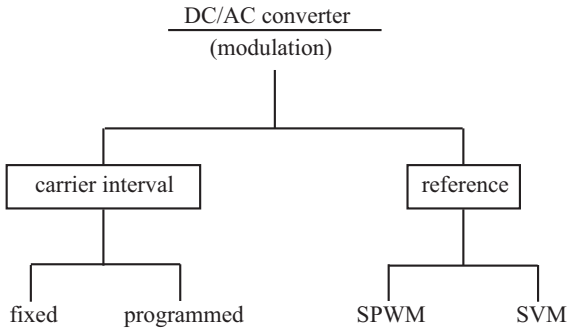


Figure 3-12: Modulation schemes classification.

3-4-2 Selection of modulation strategy

The control loop for the operation of the PMSM that is subject to the design, favors minimization of the calculation effort in the modulation strategy implementation. The reason for this is the high speed operation of the PMSM. As a result, the criterion for the selection of the modulation strategy refers to the complexity of the calculation. Choosing between SPWM and SVM, the high speed operation of the machine poses a constraint in using SVM, so SPWM is the obvious choice. For the same reason, programmed strategies will unnecessarily increase the computation effort and they can be inefficient, hence such modulation strategies will not be used in this thesis. In conclusion, the SPWM modulation strategy with fixed carrier will be used for the design of the inverter.

It should be noted that the modulation strategy can be used as a design variable in the design process. However, this is out of the scope of this work, hence the selected modulation will be considered fixed for the next steps of the design.

3-5 Control and system level operating point

The control has to ensure that the reference values for voltage and current are not exceeded and that the mission profile is achieved. In this section, the machine operation under drive limitations is investigated, leading to the inverter sizing and control requirements for the specified mission profile. The criteria and design process for the inverter system level sizing will then be discussed. From this process, the control needed for the machine and the system level operating points will be presented.

3-5-1 Machine operation under drive limitations

To investigate the machine operation under the inverter limitations it is convenient to use the rotor reference frame (dq reference frame) for the machine quantities, because the current

contribution and control is more straightforward. With the rotor reference frame, the three-phase quantities are transformed to a synchronized reference frame linked to the load vector of the machine: the direct d-axis is aligned to the machine flux vector and the quadrature q-axis is aligned to the load vector. In the dq coordinate system the current vector can be thus expressed in terms of i_d and i_q components. A complete analysis can be found in [39]; here only the design aspects related to the project will be outlined. Considering steady state operation, the system is described in the rotor reference frame by

$$\overrightarrow{V_s}^{dq} \simeq \overrightarrow{I_s}^{dq} R_s + j\omega_s \overrightarrow{\psi_s}^{dq} \tag{3-4a}$$

$$\overrightarrow{\psi}_s^{dq} = \psi_f + \overrightarrow{I}_s^{dq} L_s \tag{3-4b}$$

$$T_e = \psi_f I_{sq} \tag{3-4c}$$

where $\overrightarrow{V_s}^{dq}$ is the stator voltage, ${I_s}^{dq}$ is the stator current, R_s is the stator resistance, $\overrightarrow{\psi_s}^{dq}$ is the stator flux linkage, L_s is the stator inductance, ψ_f is the rotor flux linkage, T_e is the torque and ω_s is the rotating speed.

The first limit of the machine operation refers to the maximum current of the inverter. Thus, the operation region is constrained to

$$|\overrightarrow{I_s}^{dq}| \leq I_s^{max} \tag{3-5}$$

which gives the inverter current limit (CL). It can be represented by a circle of radius I_s^{max}, as shown in Figure 3-13.

The second limit involves the maximum available stator flux linkage due to voltage drive limitations, which arises from the voltage constraint V_s^{max}. Assuming that the dominant term in (3-4a) is formed by the induced voltage, for a maximum stator voltage, the maximum stator flux linkage can be written as

$$\psi_s^{max} = \frac{V_s^{max}}{\omega_s} \tag{3-6}$$

As a result, the maximum speed which can be achieved is restricted by the available stator voltage and the stator flux linkage. Specifically, the stator voltage is limited by the DC-link bus voltage. Considering $|\overrightarrow{\psi_s}^{dq}| = \psi_s^{max}$, (3-4b) and (3-6), the stator current limit can be expressed by:

$$(I_{sd} + I_s^{sc})^2 + I_{sq}^2 = (\frac{\psi_s^{max}}{L_s}) \tag{3-7}$$

where I_s^{sc} is the machine short circuit current, if ohmic losses are neglected. Equation (3-7) shows the voltage limit (VL) operating region due to the maximum flux linkage. It is a circle with its origin at $(-I_s^{sc}, 0)$ and radius $V_s^{max}/\omega_s L_s$, as shown in Figure 3-13. For increasing speeds, the radius of the VL circle decreases.

Given (3-5) and (3-7), the inverter operating region can be fully described by the CL and VL limits, as shown in Figure 3-13. To achieve the highest torque with maximum efficiency,

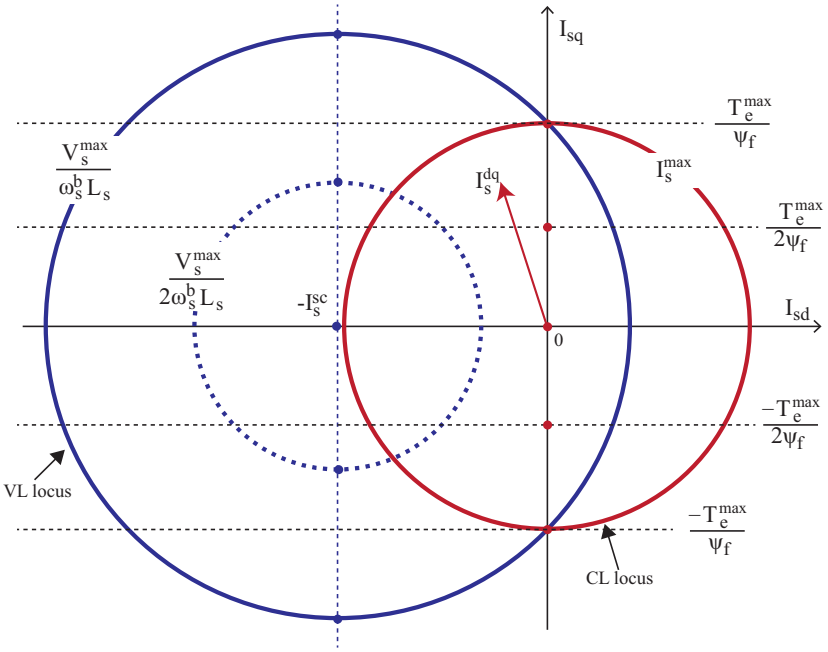


Figure 3-13: Machine operation under drive limitations.

the lowest available I_s^{dq} current is chosen. This corresponds to a current vector along the q-axis, since torque production is independent of the d-axis current (see (3-4c)). Hence, the horizontal dotted lines in Figure 3-13 represent constant torque operating points.

The maximum speed at which nominal torque can be produced before the V_s^{max} limit is reached, is called the base speed ω_s^b. Beyond the base speed, the maximum achievable torque T_e^{max} is obtained where the CL and VL circles intersect. For constant torque operation above the base speed, field weakening control is employed: the direct axis current i_{sd} is used to produce a flux linkage component that opposes the magnet flux linkage and thus reduces the back-emf.

The operating points at higher speeds depend on the short-circuit current ratio $k = I_s^{sc}/I_s^{max}$. This ratio is determined by the current rating of the machine and the inverter. If $k < 1$, for higher speed the maximum torque is limited by the VL locus which lies within the CL circle. If $k > 1$, there is a point where maximum torque can be produced along the limit of the CL circle.

The machine operation under drive limitations shows that the machine-inverter system operating points are determined by the inverter current rating (I_s^{max}), the inverter voltage rating (V_s^{max}), the short circuit ratio (k) and the machine flux linkage (ψ_s). Manipulation of these parameters will determine the machine and inverter sizing and the control strategy needed for the mission profile. If the inverter current rating is increased, the region of the CL circle is increased and the requested torque can be obtained below the base speed limit. However in this case, the inverter can be oversized. On the other hand, having a short-circuit ratio $k > 1$, the inverter current rating can be reduced by using field weakening to achieve the required torque.

As was presented in 3-2, the main application objective is to achieve maximum power

density for the inverter. Since the voltage level of the application is low, it is meaningful to take advantage of the maximum output voltage from the inverter system. This leads to a smaller current stress in the inverter and sets a minimum current sizing objective of the system. The previous discussion showed that minimum current sizing is possible by applying field weakening control for the PMSM [39]. Utilization of this technique is justified by the fact that machine operation is constrained by the inverter drive limitations. By employing field weakening and manipulating the inverter and machine parameters a minimized system can be derived. The performance of this technique for a minimum current sizing will thus be investigated.

3-5-2 Minimum current sizing

The mission profile of the application refers to a single operating point (see Table 3-1). The starting process of the machine and transient conditions are not of interest. Thus, the current minimization is conducted for the system operating point for 5 kW output power at 150 krpm, for steady state operation.

The inverter can be modeled as an equivalent voltage source $\overrightarrow{V_s}$ and the machine can be represented by the induced back-emf voltage $\overrightarrow{V_{emf}}$ and main inductance L_s, as shown in Figure 3-14. No saturation and no ohmic losses are assumed. As a result the system model can be described by

$$\overrightarrow{V_s} = j\omega_s L_s \overrightarrow{I_s} + \overrightarrow{V_{emf}} \tag{3-8}$$

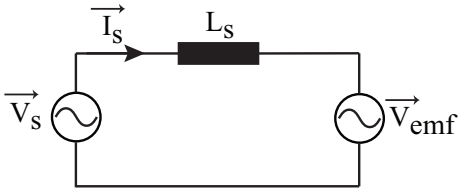


Figure 3-14: System model at steady state operation.

For any machine parameters, (3-8) can be used to minimize the current vector $\overrightarrow{I_s}$ by maximizing the inverter voltage. However, the machine characteristics are not fixed in this case study, thus they will be considered as a degree of freedom in the design. As a result, the $\overrightarrow{V_s}$, L_s and $\overrightarrow{V}_{emf}$ parameters are used as design variables for the current minimization. The design space for each of the parameters is determined from the application requirements as follows.

Inverter and machine limitations

- **Inverter voltage limit**
  The inverter voltage is limited by the DC-link and is determined by the selected modulation strategy. For SPWM the rms output voltage is defined as:

$$|\overrightarrow{V_s}| = m_a \frac{V_{dc}}{2\sqrt{2}} \tag{3-9}$$

where m_a is the modulation ratio. The DC-link is fixed at 540 V. The modulation ratio range varies from 0 to 1 for linear modulation and reaches a maximum value $\frac{4}{\pi}$ for overmodulation [12].

- **Machine voltage and current rating**
  The machine parameters are constrained by the application requirements (see Table 3-1). Specifically, the $|\overrightarrow{V_{emf}}|$ limit for the rectified back-emf was calculated using (3-1). Considering the short-circuit model shown in Figure 3-15, the machine inductance design space is determined by the machine current rating limitations, given by the short-circuit factor k from the following system of equations

$$\overrightarrow{V}_{emf} = j\omega \overrightarrow{I_s^{sc}} L_s \tag{3-10a}$$

$$k = \frac{|\overrightarrow{I_s^{sc}}|}{|\overrightarrow{I_s}|} \leq 5 \tag{3-10b}$$

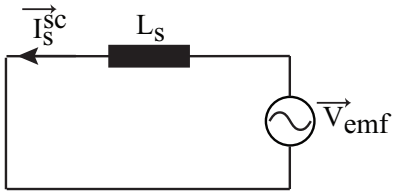


Figure 3-15: System model equivalent at short-circuit conditions.

- **Power requirements**
  Finally, the power balance equation must be fulfilled. Since the ohmic losses in the machine have been neglected, all real power is transferred to machine. This is described by (3-11), where ϕ is the current angle and δ is the load angle, illustrated in Figure 3-16.

$$P = 3V_s I_s \cos\phi = 3V_{emf} I_s \cos(\phi + \delta) \tag{3-11}$$

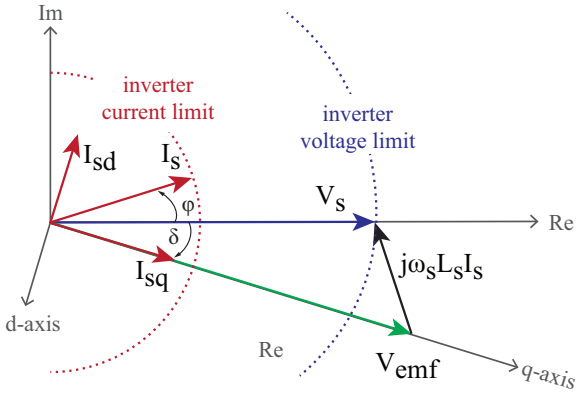


Figure 3-16: Vectors diagram for the steady state model equivalent.

Optimal operating point

From the system of equations (3-8) - (3-11), all combinations of I_s and L_s which fulfill the power requirements can be obtained. From these results, the optimal point for the inverter current and machine inductance will be chosen. The system is parameterized by the load angle δ and modulation ratio m_a. Specifically, δ is varied in the range $(-\pi/2, 0)$. For the modulation ratio, three representative cases within the range of m_a are considered:

- **Linear modulation $\mathbf{m_a \leq 1}$**
  Here m_a is smaller than one. This region has the advantages of linear modulation, however the phase output voltage is limited to a maximum value of half the DC link voltage.

- **Third harmonic injection ($1 < m_a \leq 2/\sqrt{3}$)**
  The maximum modulation index of a three-phase system is increased by including a common mode third-harmonic term into the target reference waveform of each phase leg. This third harmonic component reduces the peak size of the envelope of each phase leg voltage. By including a 1/6 value of third harmonic the maximum possible increase in fundamental component can be achieved, with a modulation ratio of $2/\sqrt{3}$.

- **Overmodulation ($2/\sqrt{3} < m_a \leq 4/\pi$)**
  With further increase of the modulation index over $2/\sqrt{3}$ the overmodulation region is entered, where the reference waveform magnitudes exceed the carrier peak at various times during the fundamental cycle. Here the linear control of the voltage amplitude with the modulation ratio is lost. The limit of the overmodulation region is at $m_a = 4/\pi$ where the result is the six-step waveform corresponding to simple square wave operation of each phase leg.

The current minimization results for varying load angle and modulation ratio are presented in Figure 3-17. For practical reasons, the modulation ratio is factorized by 0.85 of

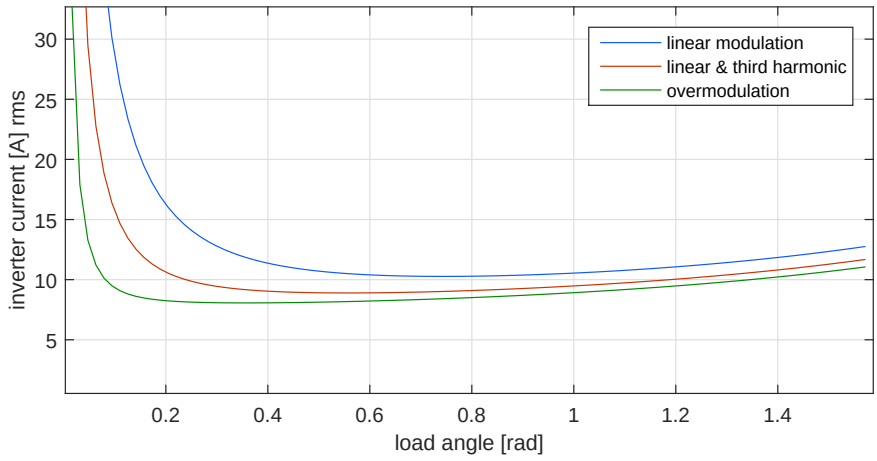


Figure 3-17: Inverter current minimization for SPWM with linear modulation, third-harmonic injection and overmodulation.

the maximum value. Higher values of m_a give greater output voltage, hence the current requirement for the inverter is lower. As a result, overmodulation offers the smallest current rating. On the other hand, overmodulation causes the output voltage to contain many more harmonics in the sidebands as compared with the linear modulation. On the other hand, the modulation strategy with third harmonic injection offers linear modulation, where the modulation index can be increased beyond 1.0. In addition, it does not affect the line-to-line fundamental output voltage, since the common mode voltages cancel between the phase legs. Due to these advantages, it is preferred for the design of the inverter.

Figure 3-18 shows the design space of the machine inductance, calculated at the system operating point. The inductance values are shown with respect to the short-circuit requirements. All values comply with the power requirements, however, only the values for $k \leq 5$ are valid options for the design. As a result, the inverter current rating will be derived from this set of inductances. The minimum inverter current is obtained for a short circuit factor $k = 1.914$ and inductance $L_s = 0.824$ mH and is equal to 8.89 A.

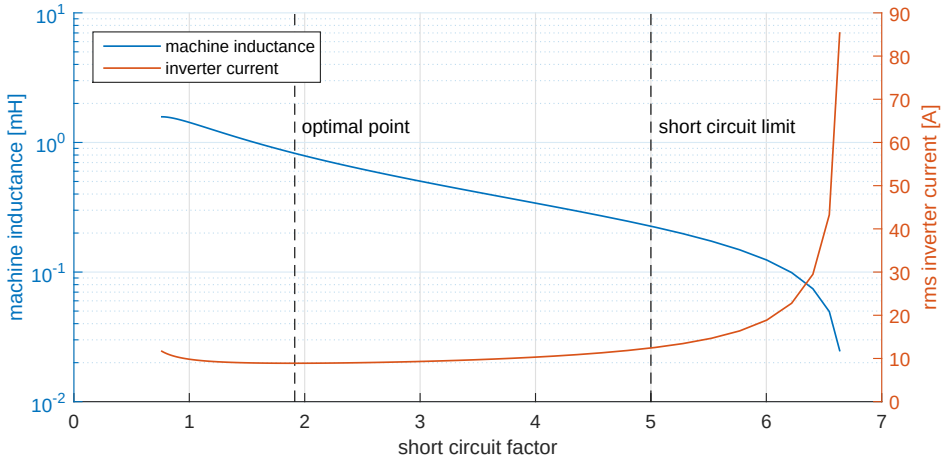


Figure 3-18: Machine inductance design space for minimum current rating.

The output of the minimum current sizing process is the inverter and machine parameters. Along with the topology, modulation and control selection, the inverter parameters at the system operating point are the output of the *Top-level* design and are used as input in the *Electrical domain* of the *Circuit-level* design. The inverter and machine system level results are summarized in Table 3-6 and Table 3-7 respectively. In case the inverter boundary is extended to the load for the *Circuit-level* design, the machine parameters are included in the design.

Table 3-6: Inverter operating point

P	$5kW$
V_s	187.386 V_{rms}
I_s	8.894 A_{rms}
η_{inv}	1
f	2.5 kHz

Table 3-7: Machine operating point

n_{max}	150 krpm
L_s	0.824 mH
k	1.914
V_{emf}	220.4541 V rms
η_m	0.85

The minimum inverter sizing for this system that was obtained, favors the inverter power factor, thus the regenerative power has to be provided from the PMSM. This is illustrated in Figure 3-19, where the maximum power factor is obtained at the minimum current. Even though this process gives maximum power factor for the inverter-machine system, the results are optimal only from the inverter point of view. By employing optimization techniques, an optimal inverter-machine system can be obtained.

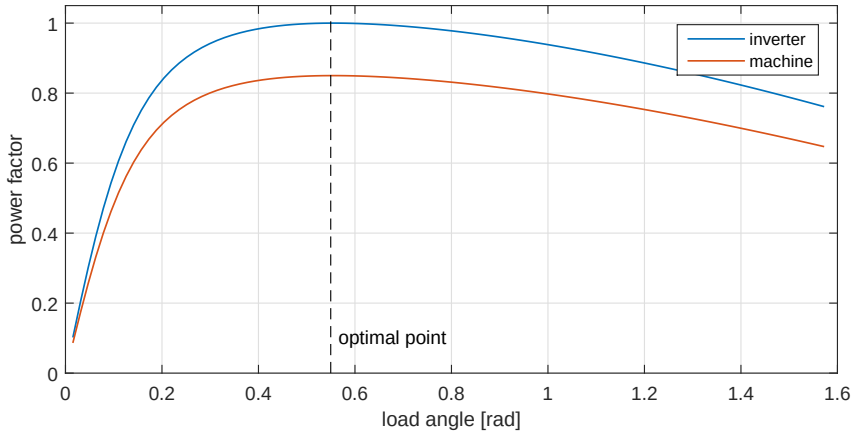
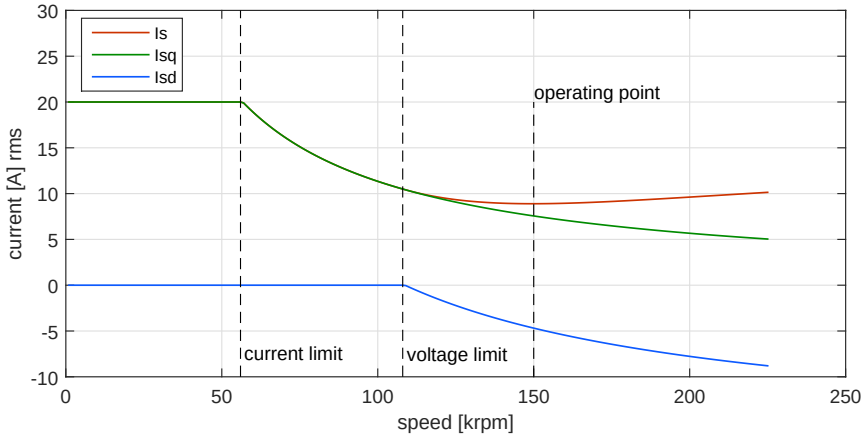


Figure 3-19: Inverter and machine power factor.

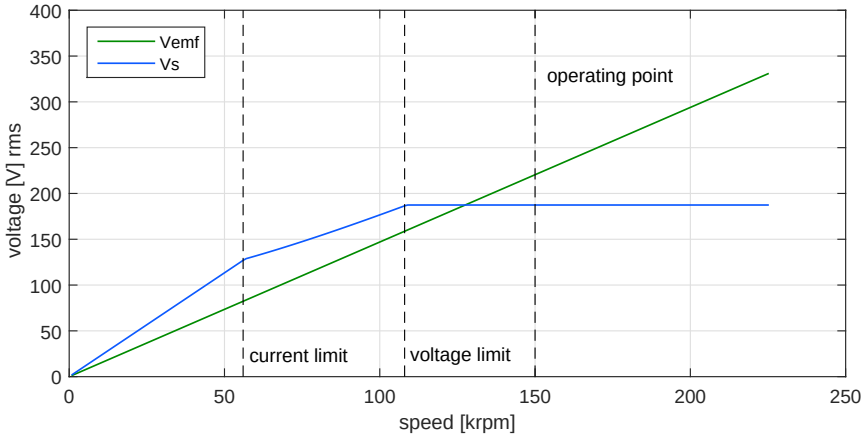
3-5-3 Drive limitations of the designed system

The effect of field weakening on the designed system is demonstrated by the following case study. The system is controlled such to achieve constant power operation at the specified operating point of 5 kW at 150 krpm. The inverter behavior with respect to increasing speed is visualized in Figure 3-20.

The current is limited by the control at 20 A. Thus, constant torque operation is achieved under the current limit. The voltage is increased until the required power of 5 kW is achieved. When the target power is obtained, the voltage is further increased until the inverter voltage limit is reached. In turn, the current drops to keep constant power operation. Until this point, only q-axis current is used. Beyond the inverter voltage limit, field weakening is used and the machine reaches the target operating point at steady state. As shown in Figure 3-20, the minimum total current is obtained at the specified operating point.



(a)



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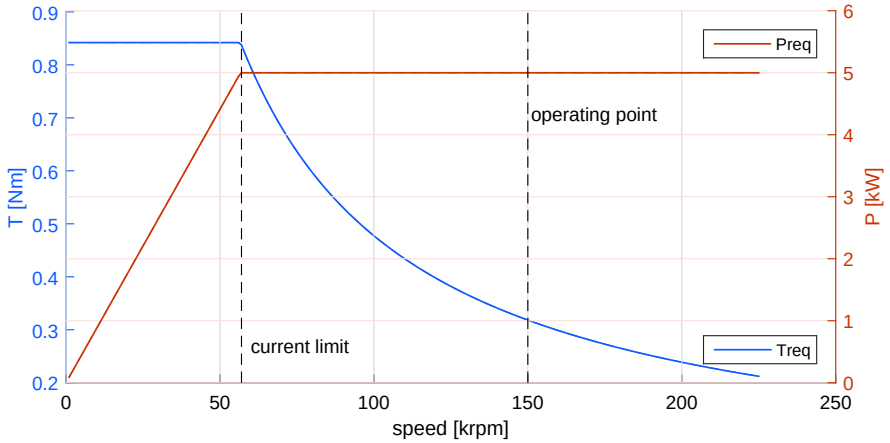


(c)

Figure 3-20: Operation of the designed system under drive limitations.

3-5-4 Top-level design points of the inverter

The inverter chosen for the case study is a 2-level hard switched voltage source inverter. The modulation technique selected for the inverter operation is linear modulation with 1/6 third harmonic injection. The inverter has been designed for a minimum current requirement, taking into account the PMSM operation under drive limitations and short-circuit requirements. From the design process, minimum current rating was obtained for a 0.824 mH machine inductance, which corresponds to a 1.914 short-circuit factor. The design process lead to a unity power factor operation for the inverter and 0.85 power factor for the PMSM. The RMS output current and voltage of the inverter drive is thus 8.894 A and 187.386 V for operation at 5 kW.

3-6 Summary

In this chapter, the *Top-level design* for the case study of an inverter for aerospace applications was presented, based on the design methodology developed in Chapter 2. Initially, the boundaries and requirements for the application were outlined. These were shaped by the specifications set by Aeronamic and the requirements related to aerospace regulations. The objective of the application was to design an inverter for a PMSM load with minimum volume and weight.

The second part of this chapter regards the *Top-level design* process, for the inverter under consideration. First, the candidate topologies for the application were selected, based on a classification of the available topologies. Then the selection process of the most suitable topology followed, including quantitative and qualitative analysis for the topologies' performance. In addition, a modulation strategy was selected for the application, based on a classification and comparison of the available modulation techniques. Finally, the operation of the machine load under the inverter drive limitations was discussed. From this discussion, the system level operating points and control for the inverter system were obtained.

Following the design methodology of Chapter 2, the topology, modulation and control selection are linked as inputs to the *Circuit-level design*, which will be presented in Chapter 4. These parameters will be considered fixed for the design thereof, for the objectives of this thesis. For the case of a comprehensive comparison of different topologies and modulation techniques, these parameters would be considered as design variables in the process.

Chapter 4

Aerospace inverter - circuit level design

4-1 Introduction

This chapter focuses on the *Circuit-level design* of the inverter. The objective is to estimate the converter circuit performance and design the components. Following the methodology discussed in Chapter 2, the design aspects of each domain are presented in a respective section. However, the coupling between the design domains affects the design choices for elements of the converter which are present in different domains. As a result, the design choices and process will be addressed in the section where the relevance of the design is considered more straightforward.

In this direction, the contents of this chapter are organized as follows. Initially, the design considerations of the *Electrical domain* are presented. In this section, the power circuit components are selected and designed. In addition, the losses of the semiconductors and passive components are modeled and the transients of the switches are estimated. Then the *EMI domain* is described, which includes the noise and propagation paths as well as the design of the EMI filter. In the last section, the *Mechanical* and *Thermal domains* are presented together. First, a preliminary layout and spatial design is described. Then, the thermal models of the inverter components are developed, including the thermal coupling between them. In every section, the reasoning for the design choices and modeling will be discussed in detail.

4-2 Electrical domain

The electric model includes calculation of the current and voltage stresses in the circuit and sizing of the power circuit components. The modeling follows a linear design process. First, the inverter bridge electric model is developed, from which the output current is obtained.

The semiconductor components are selected, followed by the calculation of their operating points. In addition, the input current of the inverter is determined and afterwards the power circuit components are designed. Having determined the components and their stresses, the losses are estimated and the switching transients are modeled. Consequently, the output of the *Electrical domain* modeling will be the designed components and their losses, the input and output currents and the switching transients.

The models consider the steady state operation of the inverter at the system operating point, which was defined in the *Top-level* design. Hence, the inverter is modeled for one fundamental period of operation. In addition, the component worst case temperature is assumed; thus, the temperature is considered fixed. Finally, in this work the sizing of the power components considers their ideal value, hence the inductive and capacitive parasitics are not included in the models. However, the electrical model is expandable towards this direction.

4-2-1 Inverter bridge electric model

The topology, modulation and control determined in Chapter 3 are linked as inputs to the electrical model of the converter. Thus, the switching operation of the inverter is modeled: the PWM signal is obtained by comparing the control signal, given in (4-1), with the sawtooth carrier signal in the time domain, as shown in Figure 4-1. When the control signal of a phase is greater than the carrier signal, then the upper switch in the respective inverter leg is turned on and the lower switch is turned off. In the opposite case, the switching operation is reversed. The result for the voltage of each switch is the PWM voltage waveform shown in Figure 4-2. To achieve realistic switching times for the semiconductors, the modulation ratio m_a is reduced to 0.85 (same as in section 3-5-2).

$$V_{ref} = m_a \frac{2}{\sqrt{3}} \{\sin(2\pi f t + \theta) + \frac{1}{6}\sin[3(2\pi f t + \theta)]\} \tag{4-1}$$

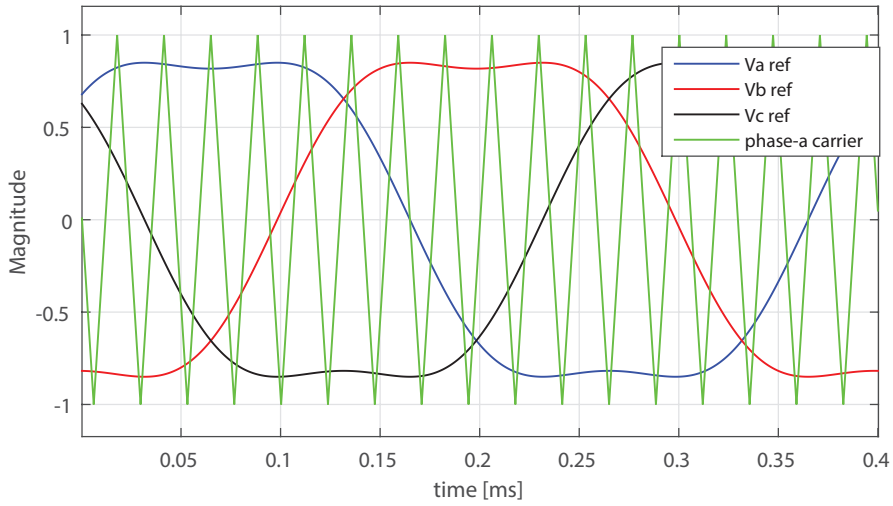


Figure 4-1: SPWM with third harmonic injection.

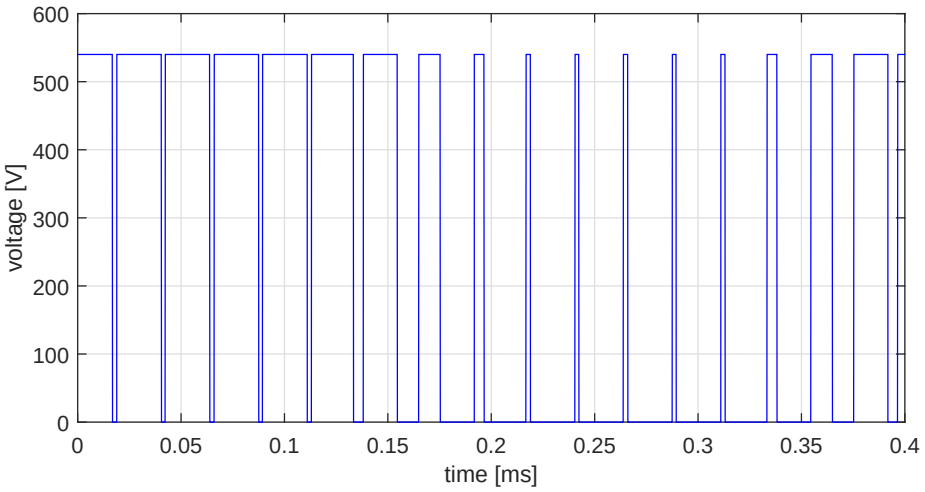


Figure 4-2: Switch PWM voltage waveform.

Output current

To obtain the output current of the inverter, the circuit is solved in the frequency domain. Thus, the output phase currents can be acquired by solving (3-8), where V_s is the PWM waveform of the inverter voltage. Here the electric boundary of the inverter is extended to the electrical properties of the load. The resulting phase current is shown in Figure 4-3; it corresponds to the inverter current stress.

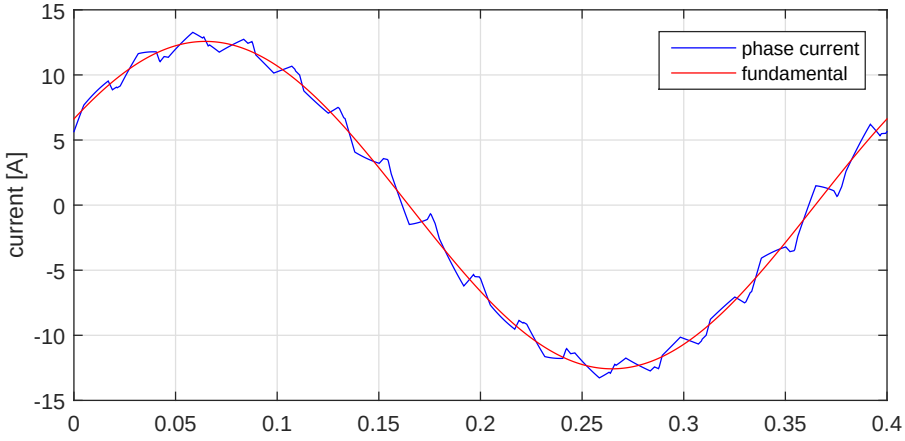


Figure 4-3: Inverter phase output current.

Semiconductor components selection: Switches

For the power level in this case study, two types of switches are widely applicable: Si MOSFETs and Si IGBTs [41]. Typical MOSFET switches have higher switching speeds than

IGBTs [12], thus can operate at higher switching frequencies. In addition, MOSFETs do not have the turn-off current tail typically observed in IGBTs (see Figure 4-4), which is a major contributor to the IGBT switching losses. However, IGBTs have smaller on-state voltage drop, shown in Figure 4-4, and allow higher power ratings than MOSFETs [10]. On the other hand, new wide-bandgap (WBG) semiconductors, such as SiC and GaN, have high temperature capabilities, fast switching speeds, smaller voltage drop and high-voltage potential [48] compared to Si. SiC MOSFETs and Schottky diodes are commercially available for low power applications, such as for the case study of this thesis, for breakdown voltages up to 1200 V in contrast to GaN which is rated for 600 V. However, this technology is still expensive compared to Si and there is a need for high-temperature packaging to exploit the high-temperature capabilities of SiC. In addition, the fast switching transitions obtained with WBG require low layout parasitic parameters [26]. The performance of the Si MOSFET, Si IGBT and SiC MOSFET technologies with respect to the aforementioned parameters is summarized in Table 4-1. The trade-offs between the advantages and disadvantages of these technologies will thus be investigated and the switch technology will be used as design variable.

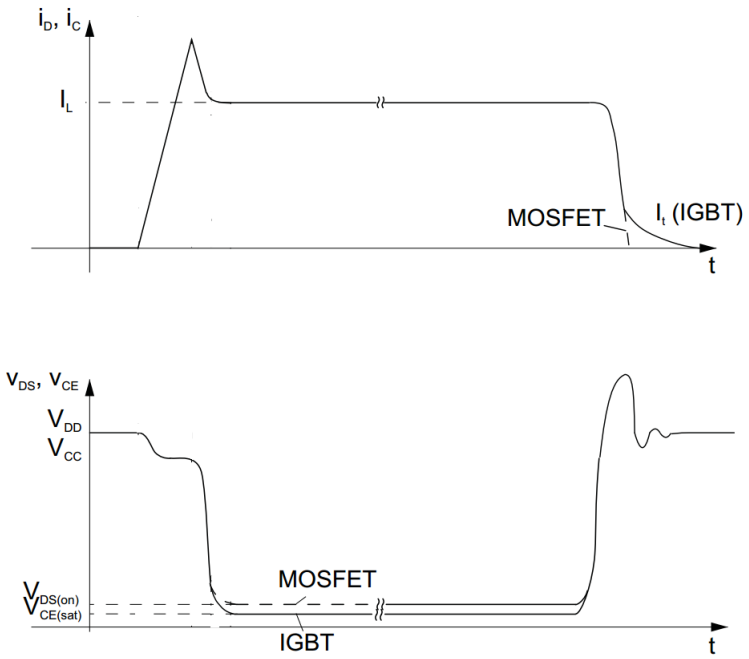


Figure 4-4: Si MOSFET and IGBT hard-switching behavior [10].

The current and voltage stresses, calculated from the electrical model, indicate the power rating of the components which can be used in the application. The breakdown voltage V_{BD} of the semiconductors is chosen such that the DC-link voltage V_{dc} does not exceed $0.8 \cdot V_{BD}$. This margin is justified by the fact that voltage transients occur during switching. The current rating for the switches is determined by the semiconductor area. Larger semiconductor area has lower on-resistance which in turn indicates low conduction losses and operation within the temperature limits; however, it has higher parasitic capacitance which indicates higher switching losses. Hence, a compromise has to be made between on-resistance and parasitic capacitance. The switches selected for the design will be presented in Chapter 5.

Table 4-1: Switches technology comparison

Performance parameter	Si MOSFET	Si IGBT	SiC MOSFET
Switching frequency	●●	●	●●●
EMI	●●	●●●	●
Max. temperature	●	●	●●
Cost	●●	●●	●
On-state performance	●	●●	●●
Switching performance	●●	●	●●
Power capability	●	●●	●●
Insensitivity to parasitics	●●	●●	●

Semiconductor operating points

In every switching interval, the direction of the current determines which device will carry the load. If during the on-state the current is positive, then the switch carries the current, otherwise the current path is closed by the inverse diode of the switch, as illustrated in Figure 4-5. Hence, the usage of an external inverse diode with IGBT switches is inevitable, since IGBTs cannot conduct current for negative voltage [41]. On the other hand, the inverse parasitic diode of MOSFETs can carry the reverse current, hence no external diode is required in this case. However, the on-state losses due to conduction of the inverse diode are higher compared

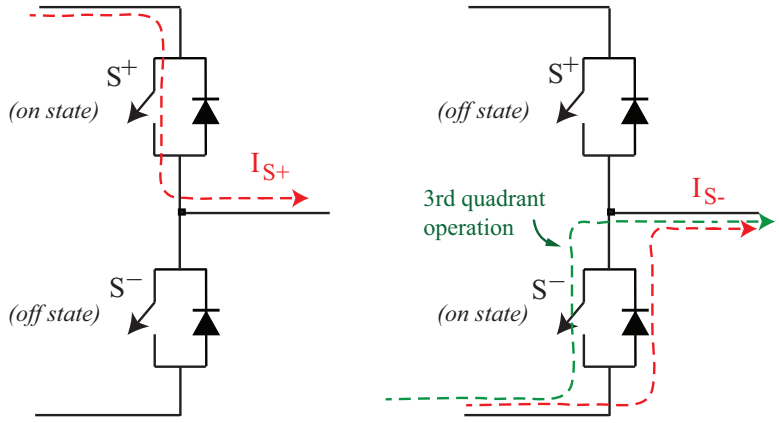


Figure 4-5: Load carrying devices during on-state operation.

to the MOSFET on-losses. To take advantage of the MOSFET conduction characteristics, 3rd quadrant operation can be utilized [10]: the drain-source voltage of the MOSFET is externally limited, for example with a Schottky diode, to values below the threshold voltage of the MOSFET inverse diode, thus the inverse diode is disabled and the operation corresponds to MOSFET conduction (see Figure 4-5). The switching losses in this operating mode are minimal, since the MOSFET drain-source voltage is clamped at the diode on-voltage. As a result, this switching operation is chosen for MOSFETs, and the role of the external diode is to conduct the current during the dead-time between switching; the conduction losses for the diode in this case are negligible. It should be noted that this switching operation for the MOSFETs brings an additional control requirement, which is related to the component technology.

As a result, the conduction and switching operating points of the semiconductors are determined, illustrated in Figure 4-6. Here, the current operating points are determined by the switching instances and the phase current. The voltage operating points correspond to the PWM waveform shown in Figure 4-2 for each phase leg. These operating points will be used in the time domain for the semiconductor switching transients and losses, as will be discussed in the following paragraphs.

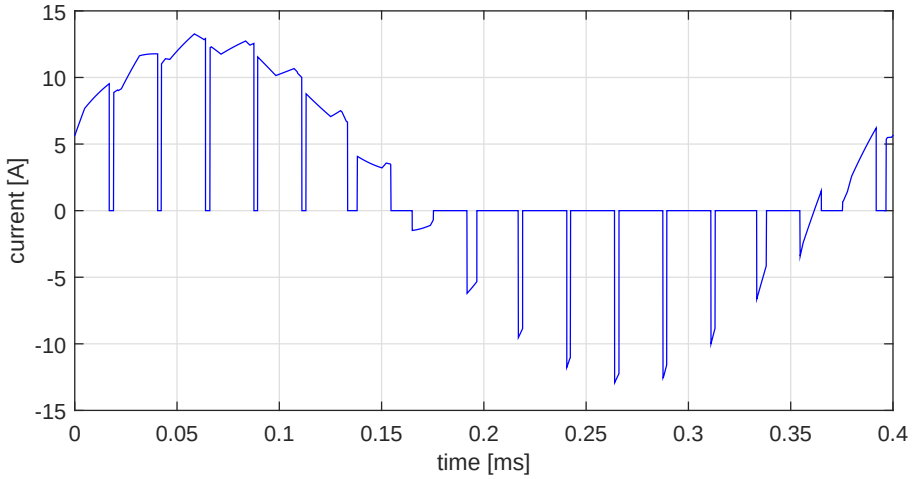


Figure 4-6: Current operating points of the phase leg semiconductors. The positive current points correspond to the switch and the negative points correspond to the inverse diode conduction (or 3rd quadrant operation).

Semiconductor components selection: Diodes

A single diode type, namely a SiC Schottky diode, is selected to be used as an external inverse diode for all switch types. It has the advantage of negligible reverse recovery [48] compared to the Si technology, whose effect can be neglected from the switching losses and transients calculations. As a result, the design trade-offs regarding the switches technology will not be affected by the diode performance. The voltage and current rating is the same with the switches. In addition, the on-state voltage of the diode is chosen lower than the on-state voltage of the MOSFET body diodes, so that 3rd quadrant operation is obtained. The characteristics of the selected diode are presented in Chapter 5.

Input current

Finally, the electric model gives the inverter input current, which is defined as the sum of the input current of each phase leg (see (4-2)). For each phase, the input current corresponds to the sum of the current of the upper semiconductor pair S (noted with +) visualized in Figure 4-5, which is the phase current shown in Figure 4-6. As a result, the DC-link current has a pulsating component added to the DC component, which is illustrated in Figure 4-7. This pulsating current will determine the design of the DC-link filter, as will be discussed in

the following paragraphs.

$$i_{dc} = i_{Sa}^{+} + i_{Sb}^{+} + i_{Sc}^{+} \tag{4-2}$$

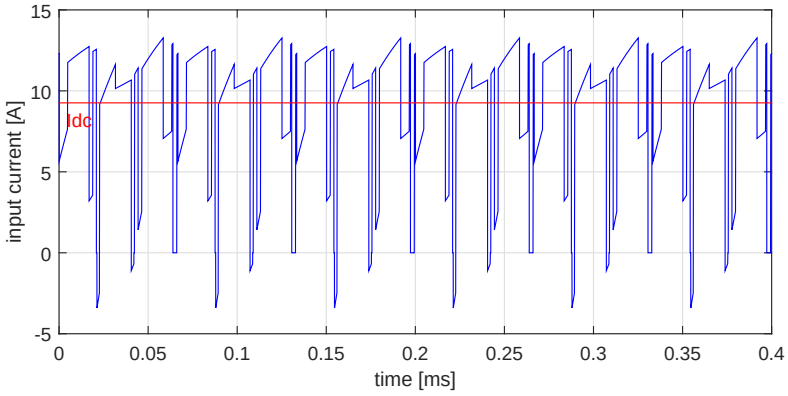


Figure 4-7: Inverter input current.

4-2-2 DC-link filter design

For a good system performance the pulsating components of the input voltage and current must be reduced to acceptable levels. These objectives are met by the use of a DC-link filter, which consists of a capacitor and an inductor, as shown in Figure 5-7. The design process of the DC-link filter in this work is based on the work in [49].

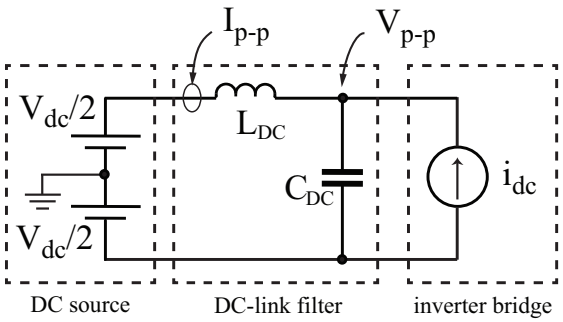


Figure 4-8: DC-link filter model.

Filter requirements

The filter is designed using the equivalent circuit of Figure 5-7, where the inverter input DC-current is modeled as a current source. The components are designed for the voltage ΔV_{pp} and current ΔI_{pp} peak-to-peak ripple levels specified by the application requirements (see Table 3-1). Moreover, the LC resonant frequency of the filter is chosen empirically 5 times

less than the switching frequency, as defined for the PWM operation [49]. Hence, the filter requirements are determined as:

$$V_{pp} \leq \Delta V_{pp} \cdot V_{dc} \tag{4-3a}$$

$$I_{pp} \leq \Delta I_{pp} \cdot I_{dc} \tag{4-3b}$$

$$f_0 < 1/5 \cdot 2 \cdot N \cdot f_s \tag{4-3c}$$

where V_{pp} is the peak-to-peak voltage ripple, I_{pp} is the peak-to-peak current ripple, N is the pulses per half cycle of the line-line output voltage, f_0 is the resonant frequency, f_s is the switching frequency, V_{dc} is the inverter input voltage source and I_{dc} is the inverter input current.

Design process

The filter is designed assuming an ideal voltage source V_{dc}. The inductor is assumed infinitely large so that the current ripple I_{pp} at the input can be neglected for the capacitor design. Hence, the capacitor ac current i_C is given from the input current:

$$i_C(t) = i_{dc}(t) - \overline{i_{dc}(t)} \tag{4-4}$$

The minimum capacitance which fulfills the voltage ripple requirements is thus obtained as

$$C_{min} = \frac{\Delta Q_{max}}{\Delta V_{pp}} \tag{4-5}$$

where ΔQ_{max} is the worst case charge, which is obtained by a numerical calculation of the maximum integral area of $i_C(t)$.

Having determined the capacitor value, the inductor can be calculated. It is assumed that the inverter current waveform is not affected by the voltage ripple on the DC-link capacitor. By using FFT and IFFT the capacitor voltage $u_C(t)$ is calculated. Thus, the voltage across the inductor can be obtained:

$$u_L(t) = u_C(t) - V_{dc} \tag{4-6}$$

Thus, the minimum required inductance can be given from the maximum integral area of the inductor voltage $\Delta V_{A,max}$ as:

$$L_{min} = \frac{\Delta V_{A,max}}{\Delta I_{pp}} \tag{4-7}$$

The accuracy of the calculated LC values is limited because the voltage ripple was neglected in the process so far, hence, greater values are required. To avoid unnecessary oversizing of the filter, the capacitor and inductor values are increased in a loop, in which the actual voltage ripple is accounted for, until the requirements are met. Finally, the resonance frequency requirement is checked. If it is not fulfilled, then the DC-link capacitance is increased. The design process for the DC-link filter is summarized in Figure 4-9.

Compared to the analysis in [49], this process favors larger values for capacitor. The reason for this choice is that the inductor is in the main power path and will suffer from larger losses. Moreover, the equivalent circuit is solved in the frequency domain and the ripple is calculated in the time domain. Thus, FFT and IFFT are used interchangeably. This way, greater accuracy is achieved and oversizing of the filter is avoided.

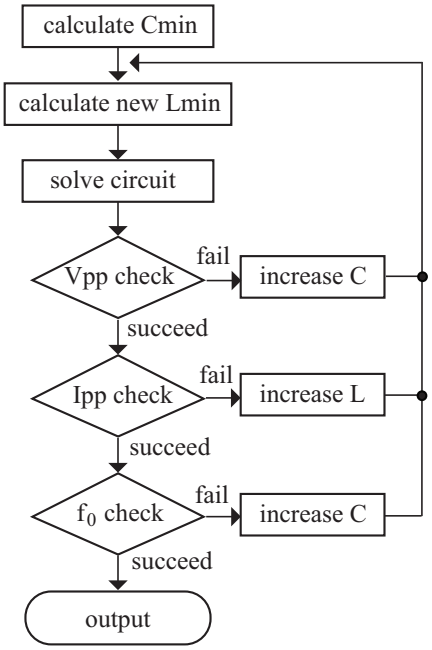


Figure 4-9: DC-link filter design process.

Component design

- DC-link capacitor
  The application requirements forbid the use of electrolytic capacitors. Hence, metallized polypropylene film capacitors for DC-link filtering [50] are used, because of their advantageous characteristics [51][52]: high reliability, self-healing properties and reduced weight. The capacitor bank will consist of a parallel configuration of capacitors, so that smaller ESR is achieved. However, the total capacitance must be calculated according to the RMS limit of the current, to maintain the component temperature within the limits. This might result in a larger capacitor compared to the calculated value; in turn the inductor will be smaller in this case.

- DC-link inductor
  In this work, the same inductor for the DC-link harmonic suppression and EMI filtering will be used. Hence, the component design will not be presented here. The reasoning for the integrated inductor and the respective design will be presented in section 4-3, where the *EMI domain* modeling is discussed.

4-2-3 Semiconductors electrical model

In this section, the current I and voltage V operating points calculated in section 4-2-1 are used to estimate the losses and switching times in the semiconductor components. The dependency of the devices parameters on the operating points is obtained from the manufacturer's datasheet measurements. Thus, the modeling is based on analytical equations and datasheet parameters.

Previous work shows that the switching behavior of MOSFETs can be easily calculated; for a first order estimation of the losses based on empirical equations [53], or using a simple analytical model [54] or comprehensive analysis [55][26] with complicated models including device and circuit parasitics. On the other hand, modeling of the IGBT switching with analytical equations is more cumbersome, due to the complicated physical behavior of the device [12]. Thus, empirical equations can be used for the losses estimation, such as in [10], or simulation tools; a review of IGBT models is presented in [56]. In this thesis, the switching behavior of the semiconductors is described by the piece-wise linear model shown in Figure 4-10. Since Schottky diodes are used, the reverse recovery is neglected and not shown in Figure 4-10. Specifically for the switching losses in IGBTs and SiC MOSFETs, the switching energies during turn-on and turn-off are provided from the manufacturers, thus the modified empirical equation of [10] are used. On the other hand, the switching energies are not provided for Si MOSFET, hence they will be calculated analytically, based on the work of [54]. In addition, the piece-wise linear model is also used for the transients calculations. For MOSFETs, the work of [54] is followed for the switching times and for IGBTs the calculations are based on [32], where the slow tails of transients (see Figure 4-4) are ignored, since they do not have a significant contribution to the noise.

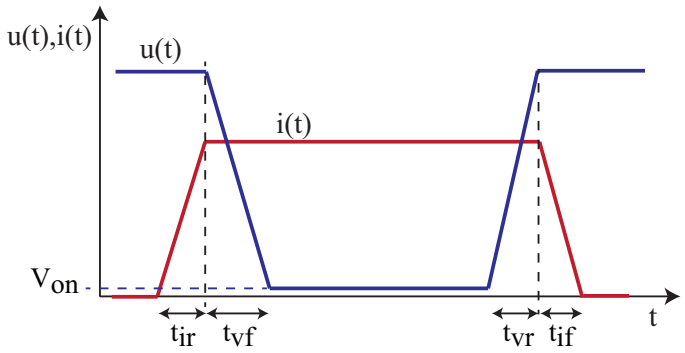


Figure 4-10: Switching losses calculation using the piecewise linear approximation.

Conduction losses

The losses during on-state for diodes and IGBTs are calculated by linearizing the output characteristic, to obtain the on-state voltage V_{on} and resistance R_{on}. Thus, the conduction losses can be calculated numerically:

$$P_c = \frac{1}{y}\sum_{n=1}^{y}[V_{on}I(n) + R_{on}I^2(n)] \tag{4-8}$$

where y is the resolution of the time domain current and n are the on-state operating points. However, R_{on} also depends on the load current. For this reason the linearization is conducted around the operating area determined by the current stress.

MOSFET's conduction losses are determined by the on-state resistance [10]. In this case, R_{on} is given as a function of the load current I. Thus, the conduction losses are described for MOSFETs as:

$$P_c = \frac{1}{y}\sum_{n=1}^{y}[R_{on}(I(n))I^2(n)] \tag{4-9}$$

Switching losses

The switching losses for Si MOSFETs are calculated using the piece-wise linear approximation [54], shown in Figure 4-10, for current and voltage fall and rise times. The model gives the switch-on E_{on} and switch-off E_{off} energies for the n^{th} switching interval:

$$E_{on}(n) = \frac{1}{2}V(n) \cdot I(n) \cdot [t_{ir}(n) + t_{vf}(n)] \tag{4-10a}$$

$$E_{off}(n) = \frac{1}{2}V(n) \cdot I(n) \cdot [t_{if}(n) + t_{vr}(n)] \tag{4-10b}$$

The rise and fall times are calculated for the operating points provided from the inverter electrical model, and are given in equations (4-11) to (4-14) [54], where their dependency on the gate resistance, device parasitics and operating points is shown.

$$t_{ir} = R_g \cdot C_{iss} \cdot \log\left(\frac{V_{gs,on} - V_{th}}{V_{gs,on} - V_{plateau}}\right) \tag{4-11}$$

$$t_{vf} = \frac{R_g \cdot Q_{gd,on}}{V_{gs,on} - V_{plateau}} \tag{4-12}$$

$$t_{vr} = \frac{R_g \cdot Q_{gd,off}}{V_{plateau}} \tag{4-13}$$

$$t_{if} = R_g \cdot C_{iss} \cdot \log\left(\frac{V_{plateau}}{V_{th}}\right) \tag{4-14}$$

where R_g is the sum of the external and internal resistance, C_{iss} is the input capacitor, $V_{gs,on}$ and $V_{gs,off}$ are the on-state and off-state gate voltage respectively, V_{th} is the threshold voltage, $Q_{gd,on}$ and $Q_{gd,off}$ are the gate charge at on-state and off-state and $V_{plateau}$ is the gate-source voltage V_{GS}. $V_{plateau}$ is obtained from the transfer characteristic of the MOSFET for a load current I and Q_{gd} is obtained from the gate charge characteristic for the respective $V_{plateau}$ voltage, shown in Figure 4-11. The input capacitor C_{iss} is fairly constant with respect to the drain-source voltage V_{DS}.

For the switching losses of the IGBT switches, the empirical equation of [10] is modified to obtain the the actual switching energy E_x from the reference E_{ref} given in the datasheet:

$$E_x = \left(\frac{V_{dc}}{V_{ref}}\right)^{1.4} \cdot \; [E_x(I) + E_x(R_g) - E_x^{ref}] \tag{4-15}$$

where x indicates turn-on or turn-off energies and V_{ref} is the reference voltage. The dependency on the operating points is indicated by the DC-link voltage V_{dc} and the switching energies $E(I)$ and $E(R_g)$ for the load current I and gate resistance R_g, obtained by curve fitting.

Having determined the switching energies per switch technology, the switching losses are given by the following well known equation [12], as a function of the switching frequency:

$$P_{sw} = f_{sw} \cdot \sum_{n=1}^{m} [E_{on}(n) + E_{off}(n)] \tag{4-16}$$

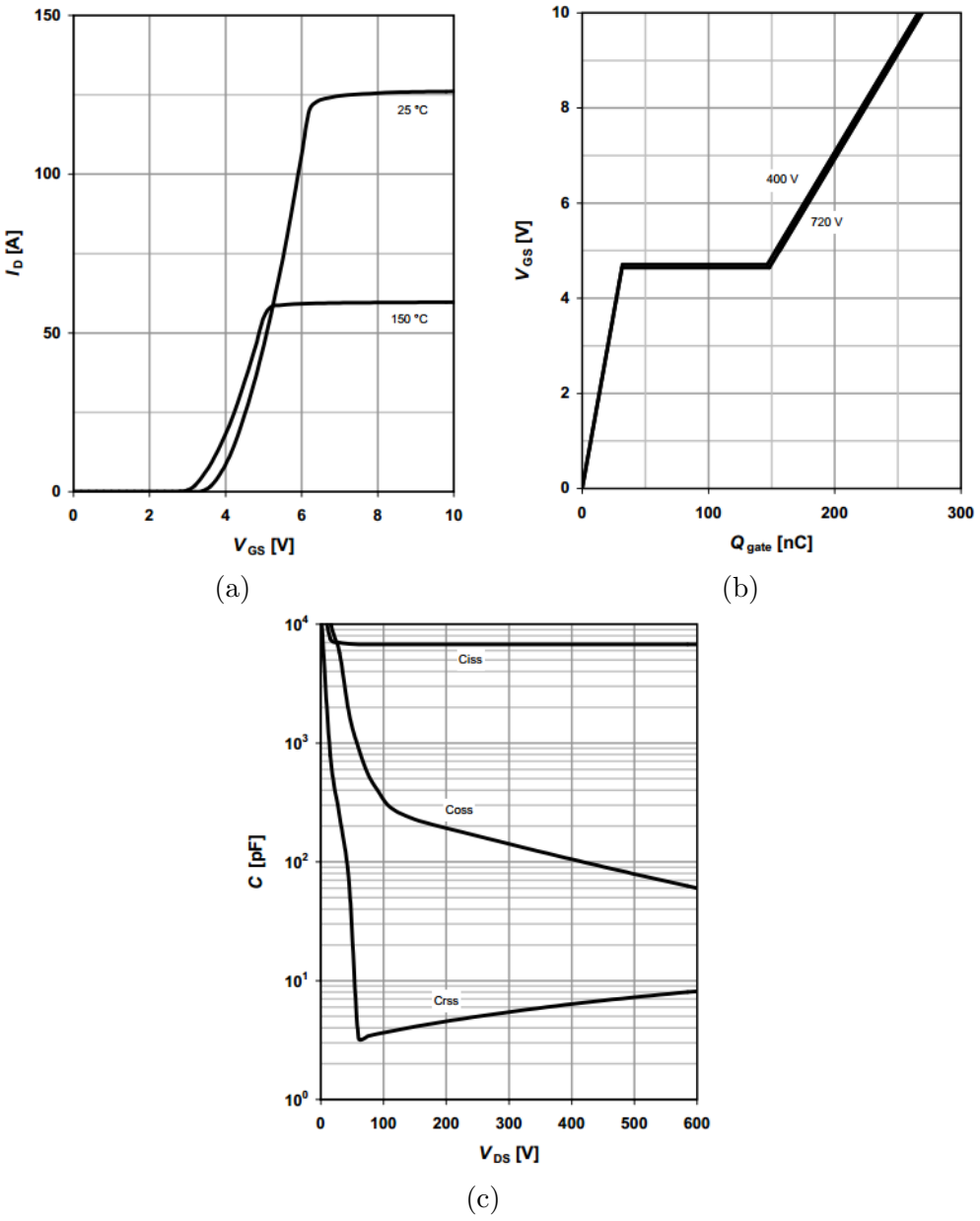


Figure 4-11: Transfer characteristic (a), gate-charge characteristic (b) and parasitic capacitances (c) of the IPW90R120C3 MOSFET switch.

where $E_{on}(n)$ is the turn-on energy and $E_{off}(n)$ is the turn-off energy at the n^{th} switching instance within a fundamental period of operation.

Equation (4-15) for the IGBTs model gives very good accuracy for the switching losses; hence it is required that the accuracy of the MOSFETs' model must be in similar levels to make a comparison between the switch technologies possible. Since the measured energies were not available for Si MOSFETs, the model results were compared to the measured switching energies of SiC MOSFETs. In Figure 4-12 it is shown that the error for the total losses calculation with respect to load current and gate resistance is well bellow 25%, even though

the individual E_{on} and E_{off} energies are over- or underestimated in the model. The major cause of the calculation error is that the non-linear behavior of the switch characteristics was neglected in the model. However, the model accuracy is in acceptable levels and will be used for the Si MOSFETs losses. For the case of SiC MOSFETs the switching energies were provided, so (4-15) was used to increase the accuracy of the results.

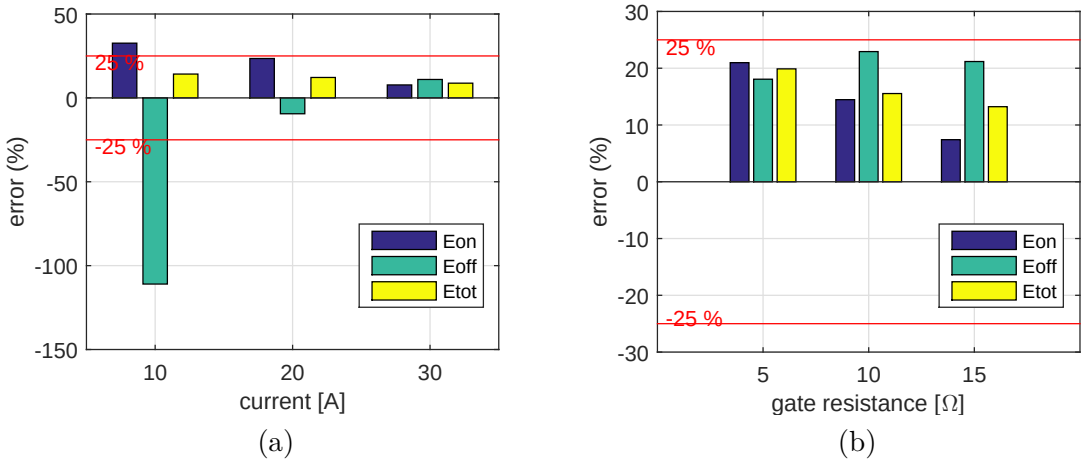


Figure 4-12: Accuracy of the MOSFET analytical model for switching energies calculation, using the SiC MOSFET C3M0065090D of CREE as a reference.

Finally, it is obvious that the switching losses are linearly dependent to the switching frequency and consequently the switching frequency must be treated as a design variable. In addition, the previously described models for the switching losses reveal their strong dependency on the gate resistance R_g. As a result, R_g will also be treated as a design variable.

Switching transients

The switching transients which are provided the EMI model are calculated in this paragraph. For MOSFET switches they are well described by the piece-wise linear model and correspond to the switching times calculated with (4-11)-(4-14). For IGBT switches, the model shown in Figure 4-10 gives the switching times [32], ignoring the slow tails:

$$\left(\frac{di}{dt}\right)_{on} = \frac{g_m \cdot (V_{ge,on} - V_{th})}{R_g \cdot C_{ies}} \tag{4-17a}$$

$$t_{ir} = I / \left(\frac{di}{dt}\right)_{on} \tag{4-17b}$$

$$\left(\frac{dv}{dt}\right)_{on} = \frac{-1}{C_{res}} \cdot \left\{ \frac{V_{ge,on} - V_{th} - I/g_m}{R_g} + \frac{C_{ge}}{g_m} \cdot \left(\frac{di}{dt}\right)_{on} \right\} \tag{4-18a}$$

$$t_{vf} = -V_{dc} / \left(\frac{dv}{dt}\right)_{on} \tag{4-18b}$$

$$\left(\frac{dv}{dt}\right)_{off} = \frac{V_{th} - V_{ge,off} + I/g_m}{R_g \cdot C_{res}} \tag{4-19a}$$

$$t_{vr} = V_{dc} / \left(\frac{dv}{dt}\right)_{off} \tag{4-19b}$$

$$\left(\frac{di}{dt}\right)_{off} = g_m \cdot \frac{V_{ge,off} - V_{th} - I/g_m}{R_g \cdot C_{ies}} \tag{4-20a}$$

$$t_{if} = -I / \left(\frac{di}{dt}\right)_{off} \tag{4-20b}$$

where C_{ies} is the input capacitance, C_{res} is the gate-collector capacitance, C_{ge} is the gate emitter capacitance and g_m is the transconductance. The parasitic capacitances have a non-linear relation to the collector-emitter voltage V_{CE} (similar to MOSFET shown in Figure 4-11(c)). In the models, the capacitors' value at $V_{CE} = V_{dc}$ is used to give an approximation of the switching transients. The rest parameters are used in a similar manner as for the MOSFET model calculations. The previously described model for the transients reveals the dependency of the switching times of IGBTs on the gate resistance R_g. Hence, the fact that R_g will constitute a design variable is again justified. Finally, the switching times calculated in this paragraph are used in the *EMI domain* according to the identified noise source in each case, as will be shown in the section 4-3-1.

4-2-4 Passive components losses

The current stresses of the passive components are obtained using the two-port configuration which was described in section 2-3-4. Since steady state operation is considered, the circuit is solved in the frequency domain. In the following paragraphs, the losses models are described.

- **Capacitor losses**
  The capacitor losses P_{cap} are obtained by using the ESR of the respective component and the RMS current stress $I_{RMS,cap}$ of the respective component, thus

  $$P_{cap} = ESR \cdot I^2_{RMS,cap} \tag{4-21}$$

  ESR is obtained by the manufacturer datasheet and is given for a frequency range up to 100 kHz. For the purposes of this thesis this value gives a good approximation.

- **Inductor losses**
  The inductor losses are modeled including the losses in the core material and ohmic losses. These parameters depend on the specific inductor design: materials, winding structure etc. The inductor used in the circuit was chosen to have a ferrite core and a single layer winding (see design in section 4-3). As a result, the losses for ferrite core are based on the Steinmetz equation [29]

  $$\overline{P_v} = k \cdot f^{\alpha} \cdot \hat{B}^{\beta} \tag{4-22}$$

  where $\overline{P_v}$ is the time-average power loss per unit volume, $\hat{B}$ is the peak flux amplitude, f is the frequency of the sinusoid excitation, and k, α, β are constants found by curve fitting. For sinusoidal excitation and a first order estimation of the core losses, equation (4-22) is widely used. New approaches of (4-22) have been developed, namely the Modified Steinmetz equation (MSE)[57], Generalized Steinmezt Equation (GSE)[58] and

improved GSE (iGSE)[59], to achieve better approximation for non-sinusoidal excitation in different frequency ranges [59]. However, these methods require measurements of the core material losses to fully exploit their advantages and will not be considered in this work.

Regarding the winding losses, since single layer winding is used, proximity effects can be neglected. Thus, the ohmic losses are modeled empirically based on [29], taking into account only the skin effect:

$$P_w = \sum_{n=1}^{\infty} (R_{ac,n} \cdot I_n^2) \tag{4-23a}$$

$$R_{ac,n} = R_{dc} \cdot (1 + F_n) \tag{4-23b}$$

where I_n is the current through the conductor, $R_{ac,n}$ is the ac resistance an F_n is the skin effect factor [29] for the increase of the conductor resistance due to skin effect for the n^{th} harmonic. The temperature variation of the DC resistance can be included in the model according to:

$$R_{dc}(T) = \rho_{20} \cdot [1 + a \cdot (T - 20)] \cdot \frac{MLT \cdot N}{\pi \cdot r_{wire}^2} \tag{4-24a}$$

where $\rho(T)$ is the wire resistivity at temperature T, MLT is the mean length per turn, N is the number of turns, r_{wire} is the wire conductor radius, and a is the temperature coefficient. For copper wire $a = 3.86\ 10^{-3}$ [ohm· m/^{o}C] and $\rho_{20} = 1.68\ 10^{-8}$ [ohm·m]. In the design process, a worst case temperature of 100 ^{o}C is assumed.

4-3 EMI domain

This section addresses the modeling of the *EMI domain*. It includes estimation of the EMI noise on the LISN and design of the CM and DM EMI filter elements. Following the methodology developed in 2-3-7, the noise source and propagation paths are identified and modeled, considering however only the capacitive coupling mechanism in this work. The design of the respective components is also described in this section, because it depends on the values calculated by the EMI model.

4-3-1 Noise source and propagation path

Common mode noise

The noise source is the CM voltage between the machine neutral point and the DC source ground connection and is given by [12]:

$$V_{CM} = \frac{V_{ao} + V_{bo} + V_{co}}{3} \tag{4-25}$$

where V_{ao}, V_{bo} and V_{co} are the PWM voltage waveforms of the inverter phases. Hence, the CM voltage is a pulsed waveform of steps of $V_{dc}/3$, as shown in Figure 4-13. The actual noise

waveform is obtained by including the dv/dt transients of turn-on and turn-off calculated from the electric model. Thus a trapezoidal voltage waveform is acquired by adding the voltage rise and fall slopes to the square-wave waveform (see Figure 4-14), based on the analysis of [32].

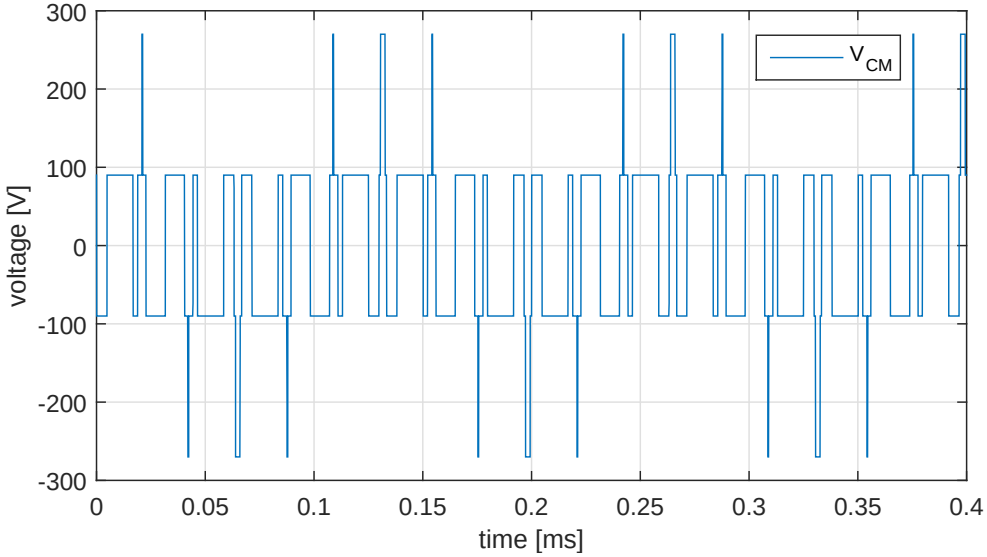


Figure 4-13: CM noise source PWM waveform.

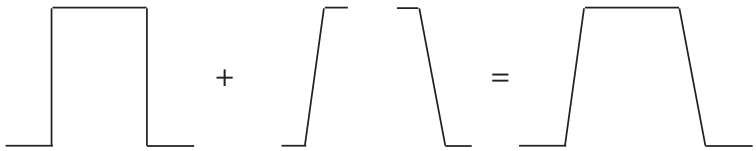


Figure 4-14: CM noise source model where the transient consists of the PWM and dv/dt signals.

Except from the CM noise source, the CM inverter model includes the switch parasitic capacitance to the ground C_p. This capacitance is calculated considering the parallel plate equivalent of a capacitor, where the dielectric is the thermal-conducting material between the switch die and heatsink. The CM model of the inverter is shown in Figure 4-15, where V_{CM} is the noise source.

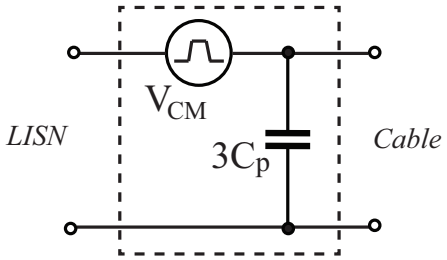


Figure 4-15: CM noise phase equivalent circuit of inverter bridge.

V_{CM} propagates to the ground connection through the parasitic capacitances of the load and inverter circuit. On the load side, the propagation path consists of the cable connection and PMSM parasitics. The Π equivalent circuit with lumped parameters can be used to model the cable effect on CM noise. The per phase equivalent is shown in Figure 4-16, where C_{cg}, L_c and R_c are the parasitic capacitance, inductance and conductor resistance of each phase. The cable parameters used in this work consider conventional values and are included in Appendix C.

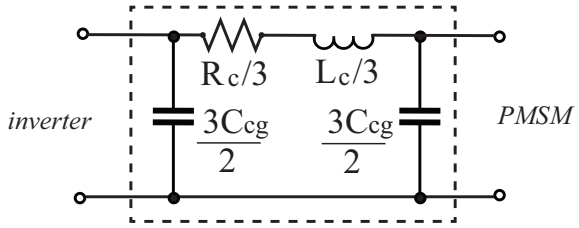


Figure 4-16: CM noise phase equivalent circuit of cable connection to the PMSM.

The PMSM high frequency model for the CM noise can be represented by an equivalent circuit of lumped components [60]. The model considers the winding parasitic capacitance to the ground C_{wg}, the machine inductance L_s and the machine resistance R_s at high frequencies. In addition, the PMSM is expected to have tightly wound conductors so that minimum volume is achieved, hence the high frequency model includes a C_s component for the mutual capacitances between the windings. The single phase equivalent of the PMSM is illustrated in Figure 4-17. Accurate impedance values can be obtained by measurements with an impedance analyzer, however they were not available. Hence, conventional values for PMSM parasitics were used, which are included in Appendix C.

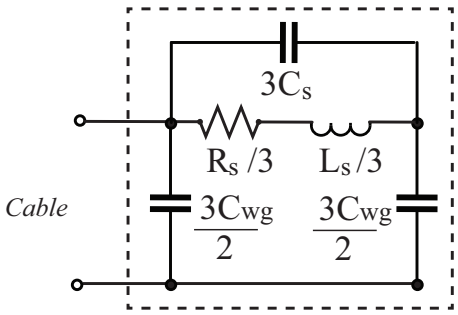


Figure 4-17: CM noise phase equivalent circuit of the PMSM.

Having determined the noise source and propagation path parameters, the model for the CM noise is summarized in Figure 4-18. It can be simplified by reducing the propagation path impedances to an equivalent impedance Z_{CM} by using the two-port cascaded circuits, which were discussed in 2-3-4. As a result, the CM noise can be represented by the Norton equivalent circuit shown in Figure 4-19, where $I_{CM} = V_{CM}/Z_{CM}$.

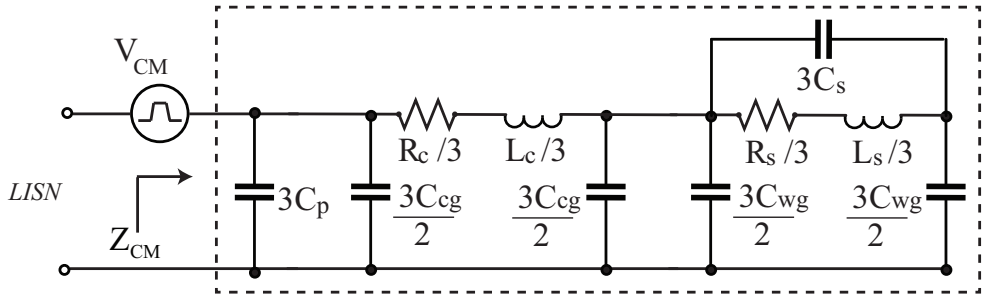


Figure 4-18: Single phase equivalent circuit of the CM noise source and propagation path.

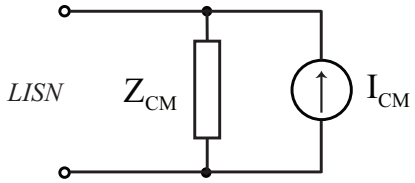


Figure 4-19: Reduced model of the CM noise.

Differential mode noise

The DM noise source is related to the PWM switching pattern and is composed by the current commutation between the phases and the additional current spikes imposed by the diode reverse recovery [31] (in this case these spikes are negligible). Hence, this noise refers to the DC-link input current, which has been already calculated in 4-2-1, and it can be modeled as a current source. Since, the DM noise propagates between the input phases, the DC-link filter is part of the DM propagation path. Hence, the DM noise is suppressed by the DC-link filter to some extent. To create a symmetrical impedance path between the input phases for the analysis, the DC-link inductor can be represented by an equivalent coupled inductor for DM filtering, as shown in Figure 4-20. Using the notation *DM* instead of *DC* for the passive components, the DM noise and propagation path can be modeled as shown in Figure 4-20.

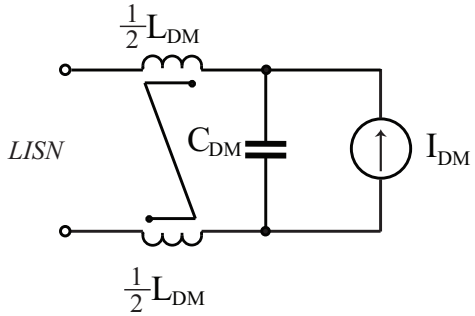


Figure 4-20: DM noise source and propagation path single-phase equivalent circuit.

4-3-2 Design of the EMI filter

Filter circuit

The EMI filter designed in this project considers the Π configuration shown in Figure 4-21. The C_{CR} and C_{CL} capacitors are connected between the DC-link and the ground to divert CM currents [33]. C_{DR} and C_{DL} are included between the phase and neutral lines to divert the DM currents (C_{DR} is the DC-link capacitor). The CM choke L_{CM} is used to block CM noise. By using coupled inductor for the CM choke, as shown in Figure 4-21, a higher effective inductance is obtained to filter the CM noise. In addition the CM choke does not affect the DM noise filtering. The same principle applies to the coupled inductor for the DM noise.

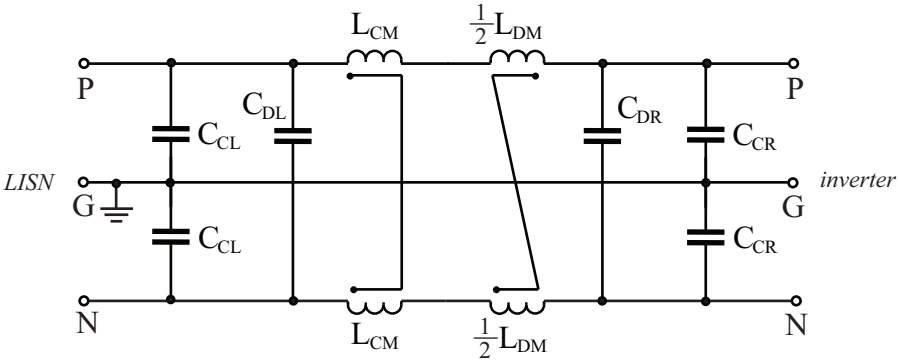


Figure 4-21: Π configuration of the EMI suppression filter.

Considering the filter configuration in Figure 4-21, it is obvious that the CM capacitors are part of the DM noise path. Including the 50 Ω resistor of the LISN in the circuit, the single-phase equivalent circuits for the filter design, can be obtained as shown in Figure 4-22.

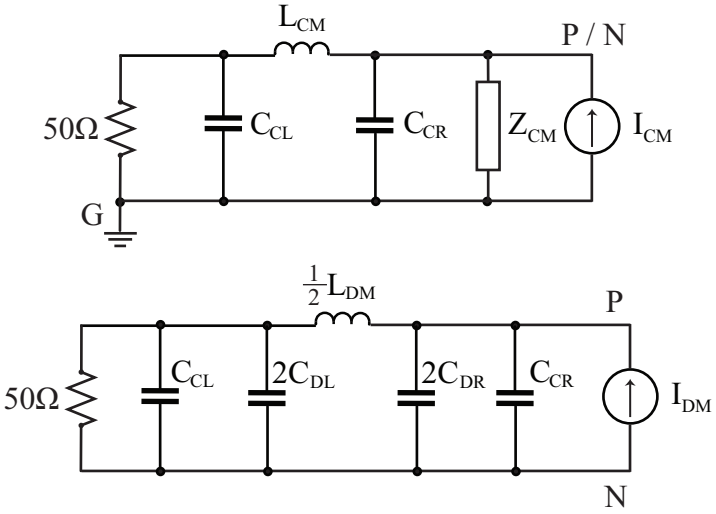


Figure 4-22: CM (top) and DM (bottom) equivalent circuits for EMI filter design.

Solving the circuits of Figure 4-22, the total noise on the LISN is obtained, represented by

the current measured on the 50 Ω resistor (Figure 4-23). Initially, the equivalent circuits are solved without the filter elements in order to characterize the actual noise on the LISN. Given this noise and the EMI standards, the attenuation requirements are specified and afterwards the filter elements are sized based on the requirements that were obtained. However since the component and layout parasitics have been neglected from the propagation path, the model accuracy concerns the low frequency range up to 1 MHz. By including those parasitics, the model accuracy will concern the full EMI noise spectrum.

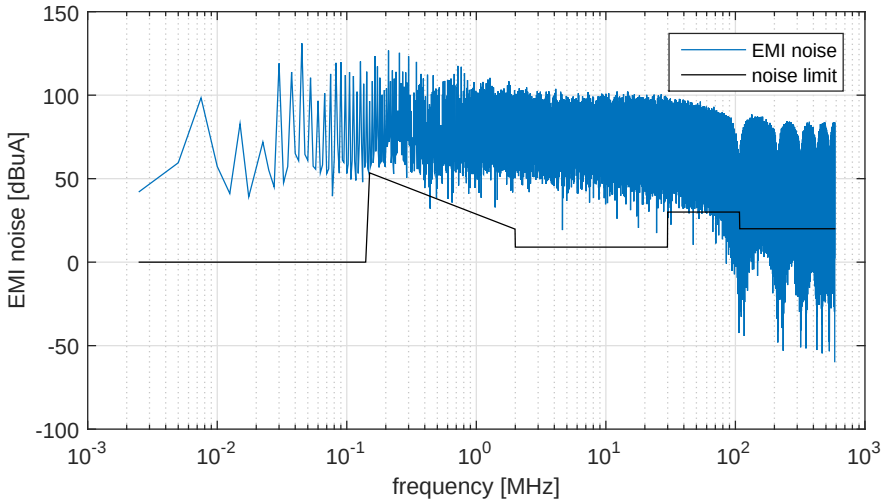


Figure 4-23: EMI noise measured on the LISN prior to filter design.

Common-mode inductor design

By using a coupled inductor for the CM choke (Figure 4-24), a higher effective inductance is obtained to filter the CM noise. In addition, the leakage inductance of the CM choke can be effectively used as the DM filter inductance. In this way a single component is used to filter both CM and DM noise [7]. As a result, the CM inductor is designed so that the main inductance and leakage inductance fulfill the calculated L_{CM} and L_{DM} values.

In this case study, a toroidal ferrite core is considered with single layer winding, shown in Figure 4-24. The advantage of toroidal coils is that they have negligible stray fields [30], hence they are ideal for EMI fitlering. Ferrite cores have high permeability and low core losses for high frequency excitation [30], which is preferable for EMI filters. Moreover, a single layer winding is used to achieve a low parasitic capacitance. The core properties are given in Appendix C.

The inductor is designed such that the core volume is minimized. The inductor design must fulfill the following constraints:

- *Inductance*
  The first constraint refers to the inductance L_{CM} per winding, from which the required number of turns N is acquired:

$$N = \sqrt{L_{CM} \cdot R_m} \tag{4-26a}$$

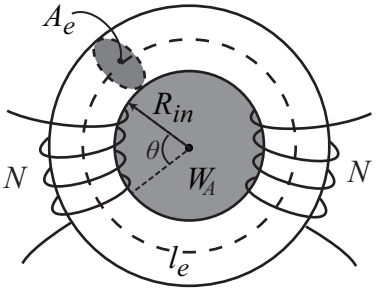


Figure 4-24: Coupled inductor for CM choke design.

$$R_m = \frac{l_e}{\mu_0 \cdot \mu_r \cdot A_e} \tag{4-26b}$$

where R_m is the core reluctance, A_e is the toroid cross-sectional area, l_e is the core effective length, $\mu_0 = 4\pi \times 10^{-7} N/A^2$ is the vacuum permeability and μ_r is the magnetic material permeability.

- *Maximum flux density*
  For operation at the linear region of the core, the maximum operating magnetic flux must be kept below the saturation B_{sat}. Given a peak excitation current I_{max}, the saturation constraint is expressed as:

$$B_{max} = 2 \cdot \frac{N \cdot I_{max}}{A_e \cdot R_m} < 0.9 \cdot B_{sat} \tag{4-27}$$

  A 0.9 margin factor is used so that the inductor can operate safely in the linear region. Since the flux of the CM currents adds in the core, the resulting flux is doubled.

- *Winding area*
  The inductor design is constrained by the available window area W_A. Hence,

$$A_{bw} \cdot 2 \cdot N < K_W \cdot W_A \tag{4-28}$$

  where $A_{bw} = I_{RMS}/J_{max}$ is the wire conductor area for the RMS current I_{RMS} and current density J_{max} and K_W is the window fill factor. For toroids, typically $K_W = 0.4$. Here single core wires are used because the current harmonic content is much lower than the DC component. It is assumed $J_{max} = 5A/mm^2$.

- *Single layer winding*
  Here, an additional constraint for the winding area due to single layer winding is imposed, so that the winding number of turns N must be less than the maximum number of turns N_{max} which fit within the core for a single layer:

$$N \leq N_{max} = \frac{\pi}{2} \cdot \arcsin\left(\frac{r_{wire}}{R_{in} - r_{wire}}\right) \tag{4-29}$$

  where R_{in} is the inner radius of the core and r_{wire} is the wire radius (conductor and insulation).

- *Leakage inductance*
  The leakage inductance L_σ is calculated using the empirical equation discussed in [61][62]. This inductance must suffice to filter the DM noise, but also it must not saturate the core. Hence two constraints are imposed:

$$L_\sigma \cong 2.5 \cdot \mu_0 \cdot N^2 \cdot \frac{A_e}{l_{eff}} \cdot \left[\frac{l_e}{2} \cdot \sqrt{\frac{\pi}{A_e}}\right]^{1.45} \geq L_{DM} \tag{4-30a}$$

$$I_{L\sigma,max} = \frac{B_{sat} \cdot N \cdot A_e}{L_\sigma} > I_{DM,max} \tag{4-30b}$$

  where $l_{eff} \approx l_e \cdot \sqrt{\theta \sin(\theta/2)/(2\pi^2)}$ is the leakage flux effective path length.

- *Temperature*
  The core and winding temperature must be lower then the maximum allowed temperature for the respective core material and insulation. This information is related to the losses and is obtained by the design in the *Thermal domain*.

Selection of EMI suppression capacitors

Similarly as for the DC-link capacitors, metalized polypropylene film capacitors are used for the EMI filter. The insulation properties for the CM capacitors require high electrical and mechanical reliability to prevent short-circuits in the capacitors in the line-to-ground connection; they are referred to as "Class Y" capacitors [63]. The DM capacitor on the power source side, is connected between the mains terminals; it is referred to as "Class X" capacitor. The requirements for Class X is that their failure will not lead to danger of electrical shock for the user [63]. Hence, the filter capacitors are chosen from the respective class. Again, a parallel connection of smaller capacitors will give lower parasitic inductance and ESR.

4-4 Thermal and mechanical domain

This section describes the modeling for the *Thermal* and *Mechanical domains*. The two domains were chosen to be treated together because of the strong coupling between the spatial design on the heat dissipation path. In the first part of this section, the spatial design of the inverter is presented. This includes a preliminary layout and relative placement of the components. Hence, actual routing is not conducted and the layout parasitics are not taken into account in this case study. The outcome of the design process in the *Mechanical domain* will thus be the spatial design and the component volume and weight, which will be a defining factor for the power density of the application.

In the second part, the thermal modeling of the inverter is described. The heat dissipation is considered for steady state operation, hence the modeling does not consider temperature transients. First, the thermal models of each component individually are discussed, followed by the thermal coupling between them. Here, a heatsink is used to dissipate the heat from the semiconductors and the inductor. The heatsink is forced-cooled in order to achieve high power density. Since the capacitors are not in the power path, their losses are not significant; thus natural cooling is used. The thermal models are developed following the heat mechanisms' principles discussed in section 2-3-6. The output of thermal modeling is the operating temperature of the components and the cooling mechanism volume and weight.

4-4-1 Spatial design

The objectives of the spatial design are to create the circuit interconnections between the semiconductors as small as possible, obtain a symmetrical configuration of the components in each phase-leg, and develop a symmetrical cooling mechanism. This will achieve a low parasitic inductance, will facilitate equal switching times and equal switching losses and will allow equal heat distribution between the components. In addition, the components' maximum temperature level is different, thus the cooling mechanism must assure that the thermal coupling between the components will not stress components with lower operating temperature. Finally, the inverter volume and weight is calculated by the net sum of individual volumes and weights of the components respectively.

According to the above objectives, the main components are arranged as shown in Figure 4-25. The semiconductors are placed horizontally in a symmetrical manner on the heatsink. In addition, the CM inductor is mounted horizontally on the same heatsink, to achieve better cooling of the core and windings. The dimensions of the heatsink length and width are determined by the semiconductor package dimensions and the inductor dimensions. The heatsink is forced cooled by a fan which blows air through the heatsink channels. In order, to decouple the heatsink front area dimensions with the fan area, a diffuser is used between the two. The DC-link, CM and DM capacitors are placed above the power semiconductors and naturally cooled. This way a smaller box volume is achieved.

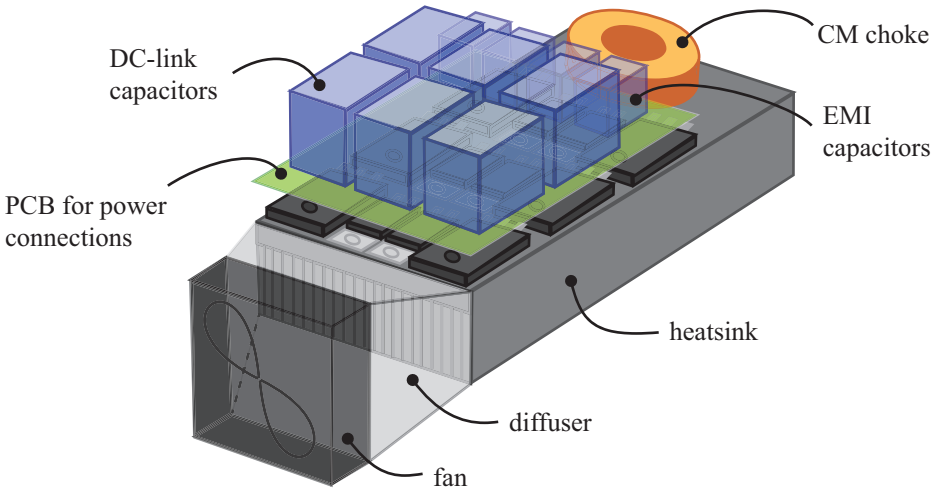


Figure 4-25: Spatial design of the inverter circuit, including the cooling mechanism.

The electrical connections of the capacitors and through-hole semiconductors are considered through the PCB between them. The gate drive and control electronics can be placed on top of the semiconductors, to achieve a symmetrical circuit. However, the main power components and heatsink are the major volume contributors. As a result, their volume will determine the power density of the inverter system. The secondary electronics are considered to occupy the same space for all designs, hence, they are not included in the spatial design for the comparison purposes.

4-4-2 Component thermal design

Heatsink thermal model

The proposed heatsink thermal model calculates the temperature distribution along the heatsink body as a function of the geometrical and environmental characteristics. It involves the convective heat transfer mechanism, from which the fluid dynamics are determined, and the conductive heat transfer mechanism, which accounts for the thermal coupling between different components mounted on the heatsink.

The convective heat transfer is calculated taking into account the heatsink geometry, the diffuser geometry and the fan characteristic. Specifically, the fan pressure ΔP_{fan} depends on the diffuser and the heatsink channels pressure difference [64]. This is expressed by (4-31), which determines the fan operating point, shown in Figure 4-26. Thus, the convective heat transfer coefficient can be calculated as a function of the channel air pressure, given by (4-32), where Nu is the Nusselt number, λ_{air} is the air conductivity and d_h is the hydraulic diameter of the heatsink channels. The fluid dynamic characteristics of the forced convective system are well defined in the literature [64] and they are presented in detail in Appendix B.

$$\Delta P_{fan} - \Delta P_{diff} = \Delta P_{chan} \tag{4-31}$$

$$h_{air} = \frac{Nu(\Delta P_{chan}) \cdot \lambda_{air}}{d_h} \tag{4-32}$$

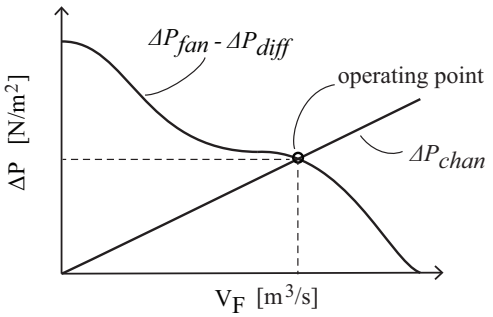


Figure 4-26: Heatsink-fan operating point.

The temperature distribution in the heatsink is described by the conductive heat transfer; here the model considers heat transfer in the 3 dimensions, based on the work of [65]. The heatsink structure is divided into many smaller sections, which are described by the h_{air} coefficient calculated from (4-32) and an equivalent resistor network. The final temperature distribution is calculated by combining all the sections. Such a model can give very good accuracy for the temperature distribution in the heatsink, as has been shown in [37].

The thermal resistance model is shown in Figure 4-27. The heatsink fins are partitioned to 3 sections and the partitioning in the x dimension is equal to the channel number. The y dimension segments depend on the final heatsink length. By combining the thermal resistor in parallel and series connection, a reduced model can be obtained, as shown in Figure 4-28. With the reduced model, the temperature calculation for each segment is simplified to:

$$P_{x,y} = \frac{T_{x,y} - T_{x-1,y}}{2R_x} + \frac{T_{x,y} - T_{x+1,y}}{2R_x} + \frac{T_{x,y} - T_{x,y-1}}{2R_y} + \frac{T_{x,y} - T_{x,y+1}}{2R_y} + \frac{T_{x,y} - T_{x,y}^{air}}{R_z} \tag{4-33a}$$

$$(T^{air}_{x,y-1} - Tx, y^{air})(c_p \cdot \rho \cdot V) = \frac{T^{air}_{x,y} - T_{x,y}}{R_z} \tag{4-33b}$$

where $c_p = 1009$ [J/kg·K] is the specific heat for air and $\rho = 1$ [kg/m^3] is the density of air at 70 ^{o} C, $P_{x,y}$ is the loss input at each segment and V is the air flow determined by the fan operating point. Using (4-33) the temperature distribution can be obtained by the matrix form given in (2-8). The calculation of the thermal resistors is based on (2-7). It is presented in detail in Appendix B.

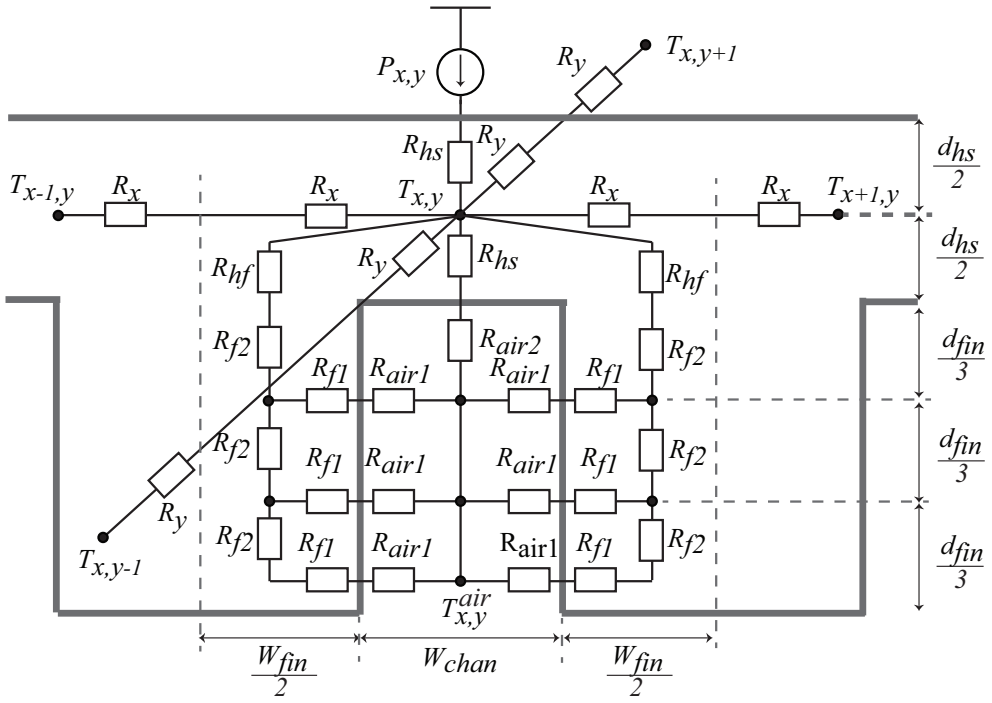


Figure 4-27: 3D equivalent resistor model of the heatsink structure.

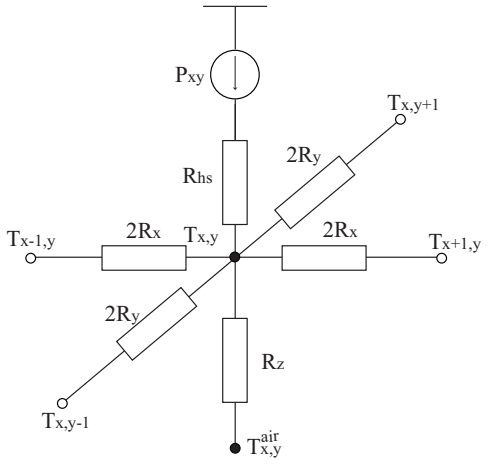


Figure 4-28: Simplified 3D resistor network of the heatsink elementary segment.

Semiconductor thermal model

The equivalent thermal resistor model of the semiconductor components is illustrated in Figure 4-29. It calculates the temperature at the junction of the semiconductor, based on the package dimensions and thermal conducting material properties. Considering the conductive heat transfer mechanism, the equivalent resistor network is composed by the junction-to-case thermal resistance R_{jc} and the case-to-heatsink thermal resistance R_{cs}. Since thermal paste cannot be used for aerospace applications, Sil-Pad material [66], specified for aerospace applications, is used; it provides electrical insulation and a high thermal-conducting interface between the semiconductors and the heatsink (see Appendix C). Figure 4-29 shows that the model can be expanded to n equivalent networks, assuming uniform temperature distribution, where n is the number of heatsink segments under the semiconductor. The uniform distribution of the losses is justified by the fact that the discrete packages are designed to support uniform heat distribution.

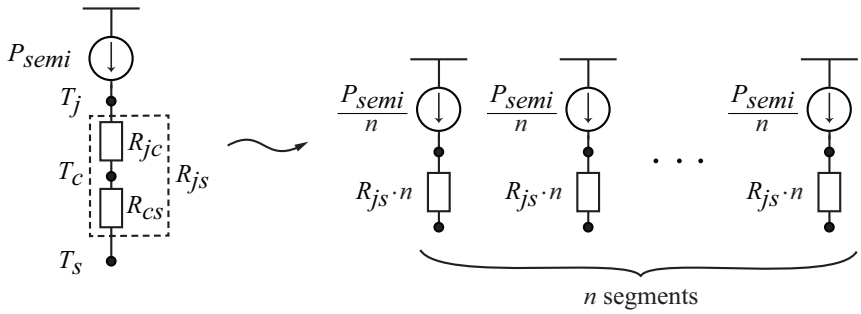


Figure 4-29: 3D equivalent resistor model of the semiconductor components.

Inductor thermal model

The inductor thermal models calculates the temperature distribution inside the core and windings as a function of the inductor geometry and materials (core, wire, insulation, thermal conducting interface) properties. Here, conduction heat transfer is considered. The symmetry

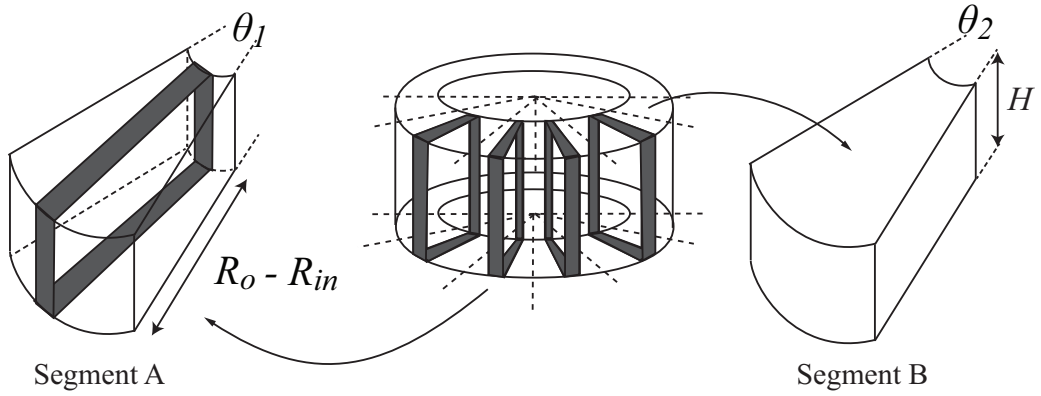


Figure 4-30: 3D partitioning of the inductor thermal model.

of the toroid geometry can be used to model the heat distribution in 3 dimensions, as has been

shown in [67]. Figure 4-30 illustrates how the toroid is partitioned into several elementary segments. For each segment, an equivalent resistor network is developed. In Figure 4-30 a modified partitioning from [67] is shown, where two areas of uniform temperature distribution in the core are considered: $SegmentA$ refers to the segments under the winding turns and $SegmentB$ refers to the bare-core area. The respective resistor networks for each segment,

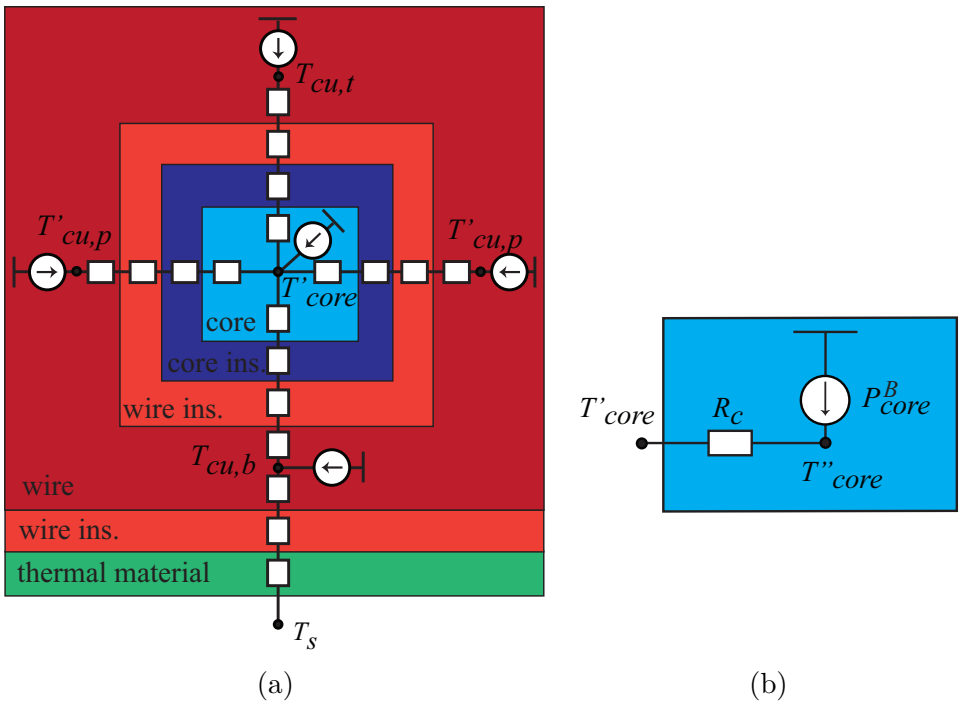


Figure 4-31: Inductor 3D thermal model: (a) segment A, (b) segment B, (c) simplified model.

and the simplified model corresponding to n heatsink segments, including the heat sources, are presented in Figure 4-31. Considering the inductor geometry and material properties, different conduction resistances are taken into account. In addition, the thermal conducting material selected for the toroid-heatsink interface is a Gap-Pad [66] material for uneven surfaces.

The simplified model in Figure 4-31(c) refers to a quarter section of the toroid, according to the toroid symmetry and temperature distribution assumptions; the heat transfer between the two segment types is achieved by the thermal resistor R_c. This model applies to tightly wound turns in the core. If the winding turns are placed far from each other, then the assumption for uniform temperature distribution in the core is not valid. In that case, the resistor network must include thermal resistors connecting the center points of $SegmentsA$, to include heat transfer between them. The detailed derivation of the inductor thermal model and model order reduction can be found in Appendix B.

Capacitor thermal model

The capacitor thermal model calculates the temperature at the surface area of the capacitor component. It considers natural cooling and radiation heat transfer mechanisms. From the

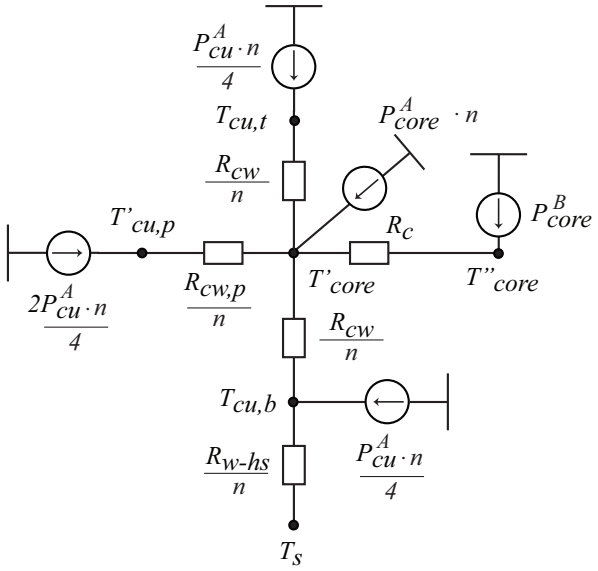


Figure 4-32: Simplified thermal model of the inductor.

calculations, the temperature difference ΔT between the capacitor surface and the ambient is obtained. The ΔT must be bellow the specified limit from the manufacturer.

The thermal models for the capacitor cooling are based on the analysis given in [68]. The convective heat transfer coefficient is calculated as a function of the Nusselt number Nu, air conductivity λ_{air} and the characteristic length s for the air flow, for the horizontal and vertical surfaces of the capacitor:

$$h_c = \frac{Nu \cdot \lambda_{air}}{s} \tag{4-34}$$

The radiation heat transfer can be obtained by

$$h_{rad} = \epsilon \cdot \sigma \cdot \frac{(TK + T_s)^4 - (TK + T_{air})^4}{T_s - T_{air}} \tag{4-35}$$

where $TK = 273^oC$, $\sigma = 5.67 \cdot 10^{-8}$ [W m^{-2} K^{-4}] is the Stefan-Boltzmann constant, T_s is the surface temperature, T_{air} is the ambient temperature and ϵ is the surface emissivity, considered $\epsilon = 0.8$ for the capacitor surface. Thus, the resulting heat transfer coefficient is obtained by the individual heat transfer coefficients and the temperature difference can be calculated as:

$$P_{cap} = (h_{c,ver}A_{ver} + h_{c,hor}A_{hor} + h_{rad}A_{rad}) \cdot \Delta T \tag{4-36}$$

where A_{ver}, A_{hor} and A_{rad} are the surfaces for vertical convection, horizontal convection and radiation heat transfer respectively, P_{cap} is the capacitor electrical losses and $h_{c,ver}$ and $h_{c,hor}$ are calculated from (4-34) for convection over the vertical and horizontal capacitor surfaces. The derivation of heat transfer coefficients is presented in detail in Appendix B.

4-4-3 Thermal coupling

Following the spatial design presented in section 4-4-1, the heat sources $P_{x,y}$ on the heatsink surface are determined as illustrated in Figure 4-33. According to the geometry and loca-

tion of the components on the heatsink, the losses of each component are distributed to the heatsink segments under the component. To obtain the operating temperature of the components, the thermal models are solved as follows. First the component losses are fed

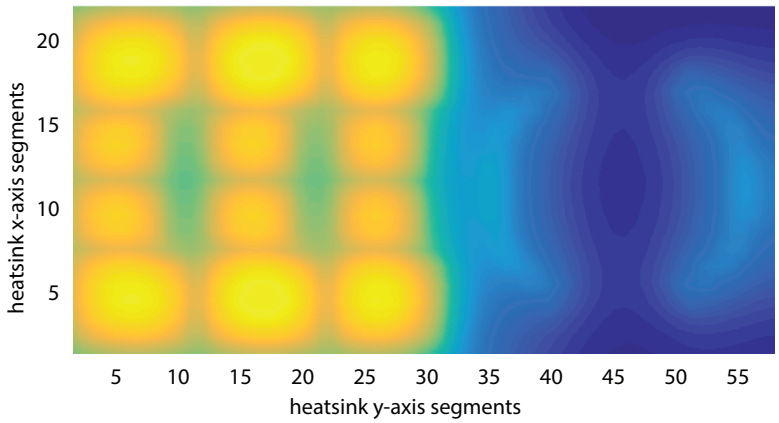


Figure 4-33: Spatial arrangement of the heat sources (semiconductors and inductor) mounted onto the heatsink.

as input to the heatsink thermal model at the respective segment locations as illustrated in Figure 4-33, the heatsink model is solved and the temperature for each heatsink segment is obtained. Then the semiconductor and inductor models are solved, using as input the heatsink temperature and respective losses. With this arrangement, the thermal models are decoupled and the calculation process is simplified. Thus, the dependency of the temperature of individual components to their adjacent components is obtained. The thermal coupling of the semiconductors and the inductor is achieved by their connection to the heatsink surface.

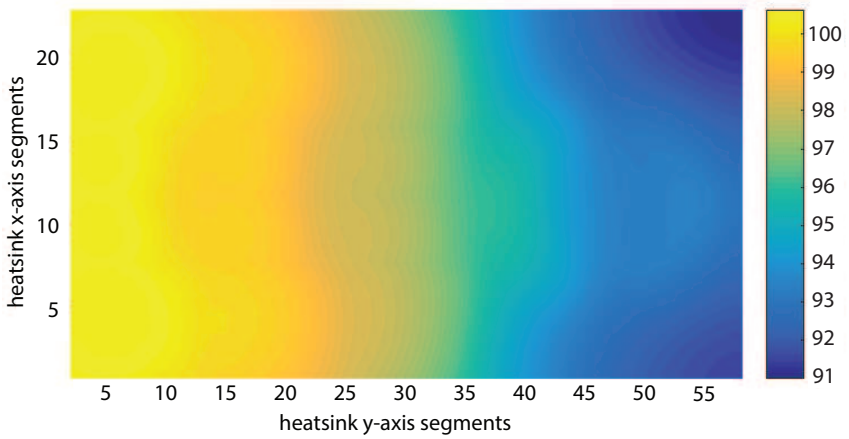


Figure 4-34: Thermal coupling of semiconductors and inductor components through the heatsink body. The fan is cooling the heatsink from the left side.

Specifically, the heat is spread between the heatsink base-plate segments, as shown for example in Figure 4-34, through the thermal resistors R_x and R_y of the heatsink model. The temperature distribution shown in Figure 4-34 indicates that the cooling effort requirement in the design will be determined from the semiconductor losses. In addition, the thermal limit of

the semiconductors will be determined by the components which are more thermally stressed, which are located at the edge of the heatsink. As fas as the capacitors are concerned, the thermal coupling between them and the rest components is not considered significant in the modeling; hence their temperature is dependent on the ambient temperature only.

4-5 Summary

This chapter presented the modeling and design process of the case study, regarding the *Circuit-level design*. The modeling of the *Electrical*, *EMI*, *Thermal* and *Mechanical domains* was presented with analytical equations. Specifically, the electrical model included the modeling of the inverter circuit, semiconductors behavior, design procedure of the DC-link filter and calculation of losses for semiconductors and passive components. In addition, the calculation procedure of switching transients, which are used in the *EMI domain* model, was outlined. Moreover, the models of EMI noise source and propagation paths were presented, for the CM and DM noise. Hereafter, the procedure for sizing and design of the EMI filter elements was addressed. Finally, the inverter spatial design was conducted and thermal models were developed for all components to account for the thermal coupling between them and estimation of their operating temperature.

The outcome of Chapter 3 regarding topology, modulation and control was considered as a fixed input for the *Circuit-level* design process. However, the switch technology, switching frequency and gate resistance were chosen as design variables for the work in this chapter. These variables will be used in Chapter 5 to manipulate the links between the design domains so as to obtain the trade-offs between different designs and achieve a design with minimum volume and weight.

Chapter 5

Results and discussion

The presented models in Chapter 3 and Chapter 4 have been developed in software and a virtual prototype of the aerospace inverter of the case study has been made. This virtual prototype was used to investigate the interdependencies of the design domains, and design an inverter with minimum volume and weight. The interdependencies of the design domains were manipulated by a parametric sweep of the design variables discussed in Chapter 4.

In this chapter, the results obtained by the multi-domain modeling in this work will be presented and discussed. In the first part of this chapter, the design variables used in the virtual prototype will be addressed in detail, followed by some design considerations of the thermal and EMI designs. In the second part, the results of the parametric sweep will be discussed. First, the results regarding the interdependencies of the design domains will be presented and the trade-offs of the design choices will be explained. In addition, the modeling accuracy used in this work will be discussed. Finally, a set of possible designs for the aerospace inverter will be presented, which will be compared and the best candidate will be chosen.

5-1 Aerospace inverter virtual prototype

The analytical models were developed in Matlab software. In the algorithm, each domain and design task was represented by a function, so that the inputs and outputs would represent the links between them. In addition, a database of semiconductors, passive components, thermal conducting components, fans and a heatsink was made and used in the design process.

The interdependencies of the design domains were manipulated by a parametric sweep of three design variables: semiconductor technology, switching frequency and gate resistance. In the following paragraph the design variables will be described.

5-1-1 The design variables

Switching frequency

The switching frequency ratio m_f to the fundamental frequency is chosen an odd multiple of the fundamental frequency f, so that the output PWM is a symmetrical signal. In addition, since the third harmonic is injected in the reference signal, the multiples of the third harmonic are not used so as not to excite them in higher frequencies. As a result, the switching frequency consists of prime odd multiples of the fundamental frequency. Five switching frequencies were used in this work and are summarized in Table 5-1.

Table 5-1: Switching frequency parameters

m_f	11	13	17	19	23
f_s [kHz]	27.5	32.5	42.5	47.5	57.5

Semiconductor technology

As was discussed in section 4-2-1, the semiconductor technology will be treated as a design variable. Five off-the-shelf discrete components were selected from the Si MOSFET, SiC MOSFET and Si IGBT technologies. The criteria for the selection was the power rating, parasitic capacitances and on-state voltage drop. For IGBTs and Si MOSFETs, switches with small parasitic capacitance were chosen, so as to reduce the switching losses. However, the power rating of the Si MOSFETs is smaller than the others. The reason for this selection is that Si MOSFETs have lower breakdown voltage than SiC MOSFETs and IGBTs, which would lead to higher current rating if the same power rating is required. Hence smaller current rating is chosen so as to reduce the switching losses coming from the device parasitic capacitances.

The power rating and switching characteristics of the selected components are summarized in Table 5-2. For IGBTs , the maximum operating frequency for the switches refers to the data given from the manufacturer. However, this information was not directly given for MOSFETs. Hence the switching frequency was roughly estimated so that the sum of the switching transitions would have 1/50 duration of the switching period. Thus, the estimated switching frequencies are noted with a star $*$.

Gate resistance

The external gate resistance of the switches was also used as a variable in the parametric sweep. The values varied within the range specified by the manufacturer for each switch. As a result, the gate resistance for each switch is different. The values used vary from 0 to 25 Ω, where five different values are used for each case.

Table 5-2: Semiconductors devices

Device	V_{BD}	I	R_{on}	T_{max}	f_{sw}	t_{don}	t_r	t_{doff}	t_f	C_{iss}	C_{oss}	C_{rss}	Package
	[V]	[A]	[mΩ]	[^{o}C]	[kHz]	[ns]	[ns]	[ns]	[ns]	[pF]	[pF]	[pF]	
Si MOSFET													
IPW90R120C3[69]	900	36	120	150	50*	70	20	400	25	6800	70	7.5	TO-247
STW20N95K5[70]	950	17.5	275	150	>100*	17	12	70	20	1600	60	6.5	TO-247
STW22N95K5[70]	950	17.5	280	150	>100*	18	9	65	18	1800	95	4	TO-247
STW23N85K5[70]	850	19	200	150	>100*	22	14	55	8	1800	75	4.25	TO-247
STW40N95K5 [70]	950	38	110	150	>100*	33.50	51	91.5	10	3200	145	6	TO-247
SiC MOSFET													
C3M006590D[71]	900	36	65	150	>100*	21	36	28	25	660	64	4.3	TO-247-3
C3M006590J[71]	900	35	65	150	>100*	7.2	6.5	15	5	660	64	4.3	7LD2PAK
SCH2080KE[72]	1200	40	80	175	>100*	37	33	70	28	1850	177.5	20.75	TO-247
SCT2080KE[72]	1200	40	80	175	>100*	35	36	76	22	2100	82.5	17.5	TO-247
C2M0080120D[71]	1200	42	82	135	>100*	11	20	23	19	950	82.5	7.8	TO-247-3
Si IGBT													
STGW25H120F2[70]	1200	25	–	175	50	27.5	13.5	139	200	2000	50	18	TO-247
STGW15H120F2[70]	1200	15	–	175	50	23.5	8	118	253	1300	38.5	12.5	TO-247
IGW25N120H3[69]	1200	25	–	175	100	26	35	347	50	1715	442.5	435	PG-TO-247-3
IGW15N120H3[69]	1200	15	–	175	100	19	30	327	43	1050	275	270	PG-TO-247-3
SGW25N120[69]	1200	25	–	150	40	50	36	820	42	2150	190	100	PG-TO-247-3
SiC Schottky Diode													
C4D20120A[71]	1200	25.5	–	175	–	–	–	–	–	–	–	–	TO-220-2

5-1-2 Other design considerations

Operation at maximum temperature

In order to achieve maximum power density, the heatsink is designed so that the components would operate at their maximum temperature. Hence, the results of the thermal models are used to verify if the maximum temperature operating limit is reached or not. The heatsink used in this work is the Ultra-Fin heatsink [73] for aerospace applications. The geometry of this heatsink is modified, so that the components fit on the base plate area and the fin height is enough to keep the components temperature just below the maximum limit.

Initially, the modeling showed that the switches with very low losses operated well below their maximum temperature with the standard heatsink geometry. In order to reach the thermal limit of the switches, a modified heatsink geometry was considered, where every second fin was removed. This way, the heat transfer surface of the heatsink was reduced, thus achieving higher temperatures for the components. The modified heatsink was used in combination with the 09P412M701 fan [74], hereafter referred as configuration HDF1. If HDF1 was not enough to reduce the components' temperature then the standard heatsink geometry with four 9GA0412G7001 fans [74] was used to achieve better cooling, hereafter referred as configuration HDF2. For both configurations the height of the fins is increased in the algorithm from 12 mm to 32 mm. Hence both heatsinks can have the same box volume, however HDF1 is lighter because it has half number of fins.

Finally, the parametric sweep for high values of switching frequency and gate resistance showed that some designs failed the temperature limits with the HDF2 configuration. As a result, a larger heatsink would be required for safe operation in those cases. However, the volume and weight would increase and the efficiency would decrease significantly, as will be shown in the following sections. Since the design objective is to obtain an inverter with maximum power density, those designs do not add value to the best design selection and thus, will not be shown in the results.

EMI filter design

The attenuation requirement used for the EMI filter considers a 6 dB margin for CM and DM noise from the RTCA/DO-160 standard. It is preferred that the design favors larger capacitance values compared to the inductance, because the capacitors are not in the main power path and will have less losses than the inductor. However, the results showed that the capacitors' volume would become very high for the application. Thus, the C_{CR} CM capacitor (see Figure 4-21) is calculated such that the minimum capacitor is obtained which can withstand the respective current. The C_{CL} capacitor is then considered $1/100 \cdot C_{CL}$, and both capacitor values are kept constant for all designs. As a result, the design of the CM filter is simplified to the sizing of the CM inductance. For the DM filter, only the C_{DL} capacitor on the LISN side is calculated, since the inductor and capacitor on the inverter side have already been calculated from the DC-link filter design process.

5-2 Investigation of the domain interdependencies

5-2-1 Thermo - mechanical interdependencies

The thermo-mechanical dependencies discussed in this paragraph consider the thermal coupling of the components. Here, for comparison purposes the inverters are operated at 27.5kHz and the switches are driven with minimum gate resistance. Regarding each semiconductor technology, the losses and temperature of the semiconductors for the most efficient inverter are summarized in Table 5-3. The diode conduction losses are zero for the inverters with MOSFETs, because 3rd quadrant operation is used. On the other hand, the diodes conduct the inverse current in the inverters with IGBTs, hence conduction losses are present. The thermal coupling of the components through the heatsink base-plate is clear when the inverters with MOSFETs are considered: even though the diodes have zero losses, their temperature is increased above the ambient temperature, due to the heat transfered from the MOSFET switches. This is the reason for the increased temperature of the diodes, in all designed inverters.

Table 5-3: Semiconductors thermal coupling

Switch	STW20N95K5	C3M0065090J	IGW25N120H3
Technology	Si MOSFET	SiC MOSFET	IGBT
Switch losses [W]	15.6	5.4	15.1
Diode losses [W]	0	0	0.66
Switch temperature [^{o}C]	148.3	121	162.8
Diode temperature [^{o}C]	131.4	106.5	148.4

5-2-2 Electro - thermal interdependencies

The dependency between electrical and thermal domain will be shown from the heatsink requirement point of view, since the heastink is designed for maximum operating temperature. The cooling effort required in each case will be quantified via the volume of the heatsink-diffuser-fan configuration that is used.

First of all, the relative loss distribution between the inverter components is considered. Figure 5-1 shows the distribution of losses in the inverter components, when different semiconductors are used. For comparison purposes, the minimum switching frequency and minimum gate resistance are used, since this choice results in the lowest losses. It is observed that the passive components' losses are very small compared to the semiconductor losses. Thus, the cooling effort will be determined mainly by the semiconductors' losses. This results to operation at the thermal limit for the semiconductors and well below the maximum temperature for the passive components. For this reason, only the dependency of the heatsink design on the semiconductors' losses will be discussed in the next paragraphs.

In addition, from Figure 5-1, the advantage of the SiC technology regarding the conduction and switching losses is obvious, thus these inverters will require the least cooling effort. Inverters with IGBT and Si MOSFETs switches have comparable performance, with IGBTs showing an advantage in conduction losses. This is expected, since IGBTs have lower on-state

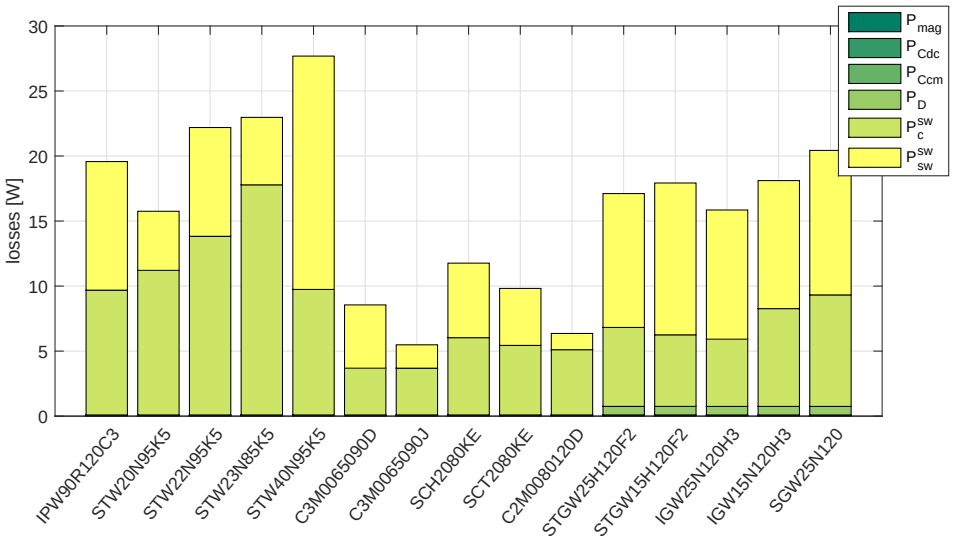


Figure 5-1: Losses distribution in the inverter components for $f_s = 27.5$ kHz and minimum gate resistance.

voltage drop than MOSFETs. In addition, the higher conduction losses for Si MOSFETs are justified by the fact that these switches have smaller power rating than the rest, which turns out to be a limit of the Si MOSFET technology for the power rating of the case study.

The dependency of the cooling effort on the semiconductors losses is investigated as a function of the switching frequency and gate resistance variation. In Figure 5-2, the heatsink volume is shown as a function of the switching frequency for the selected semiconductors. The presented results show that the inverters with SiC MOSFETs have the smallest heatsink volume. This is expected, since these switches have generally the lowest losses. However, the SiC MOSFETs which have higher losses than Si MOSFETs, also require less cooling effort. The reason is that these switches are the SCT2080KE and SCH2080KE which have higher temperature limit (175 ^{o}C). The higher temperature limit of IGBTs is also the reason why these switches have smaller heatsink than the Si MOSFETs, despite their higher losses.

The points where the heatsink volume decreases significantly with increasing losses in Figure 5-2 (b), correspond to the transition to the HDF2 heatsink configuration, which was discussed in section 5-1-2. In addition, a small decrease in volume for some SiC MOSFETs at 57.5 kHz is observed. This is due to the CM inductor core used in these designs, which has a larger height and smaller radius; hence the heatsink total length is smaller. This result shows the effect of the discrete nature of the components dimensions on the design outcome.

Figure 5-3 illustrates how the switching losses are affected by the gate resistance manipulation, for each semiconductor technology. The SiC MOSFETs show a better performance compared to the others due to their lower parasitics. This results to a lower cooling requirement, as shown in Figure 5-4, which shows the heatsink volume for each semiconductor as a function of R_g. In addition, in Figure 5-4 the effect of the temperature limitations of the semiconductors is also shown. First of all, the high losses and lower temperature limit of the Si MOSFETs result to higher heatsink volume. Similarly, the high temperature limit of the IGBTs allows lower cooling effort from the Si MOSFETs with comparable losses. Finally, it

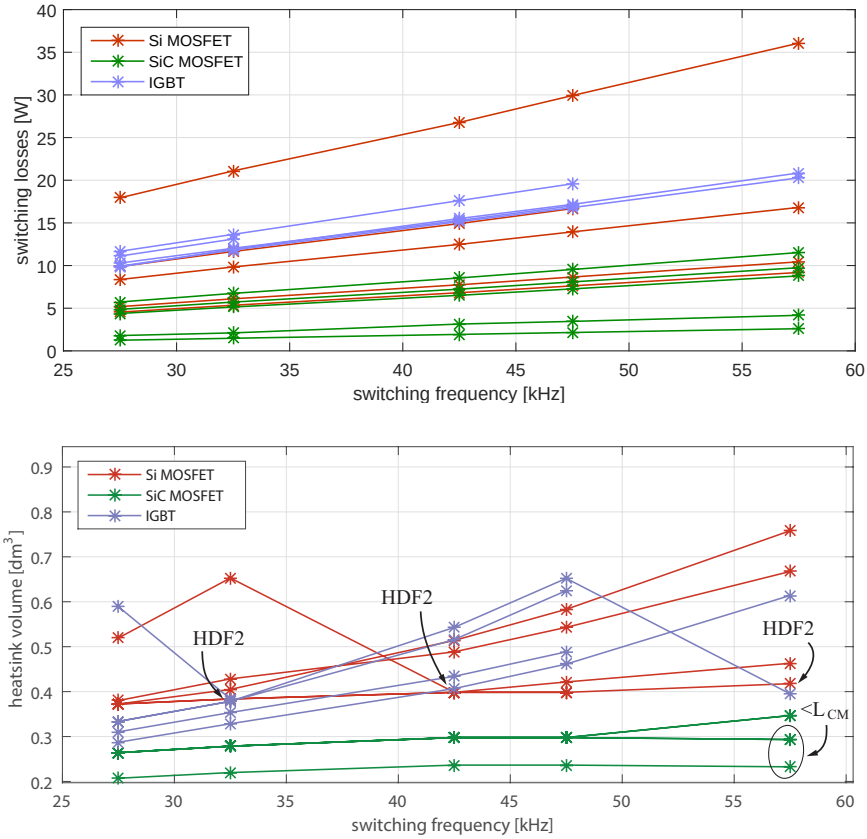


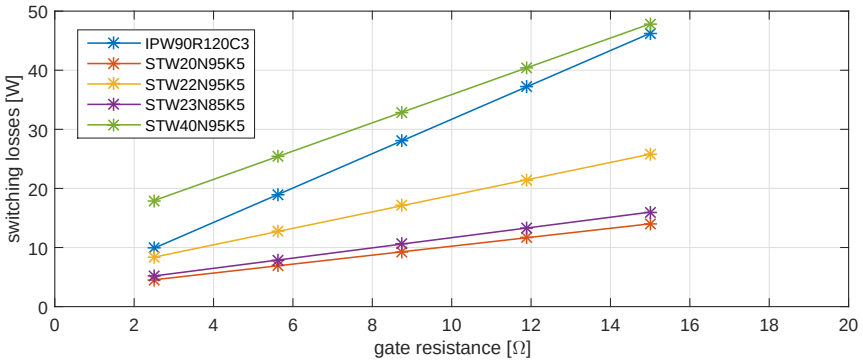
Figure 5-2: Switching losses, and heatsink volume dependency on the semiconductors losses as a function of the switching frequency (R_g = min.).

is observed that the SiC MOSFET technology leads to better performance when the switches are driven with low gate resistance. Similar to Figure 5-2 (b) the decrease in volume observed in some cases for increasing losses is due to the different heatsink-fan configurations used.

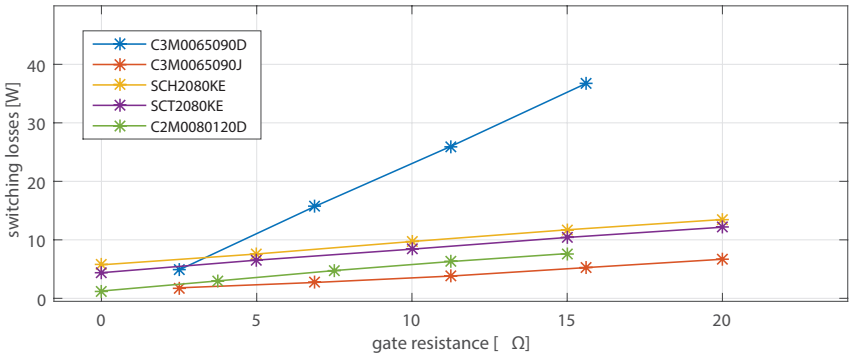
The presented results show an increase of the switching losses for all switches, when the gate resistance is increased. This is not an unexpected outcome since charge and discharge time of the input capacitance at turn-on and turn-off is increased. Specifically for the Si MOSFETs the increase is linear, which is justified by the linear model that is used to calculate the switching losses. On the other hand, for SiC MOSFETs and IGBTs the models include the non linear behavior of the switches, taken from the measured data from the manufacturer. Thus, the non linear relation is observed in the results. Moreover, the linear model used for the switching losses as a function of the switching frequency, also justifies the linear increase of the losses in this case.

5-2-3 Electrical - Package parasitics interdependencies

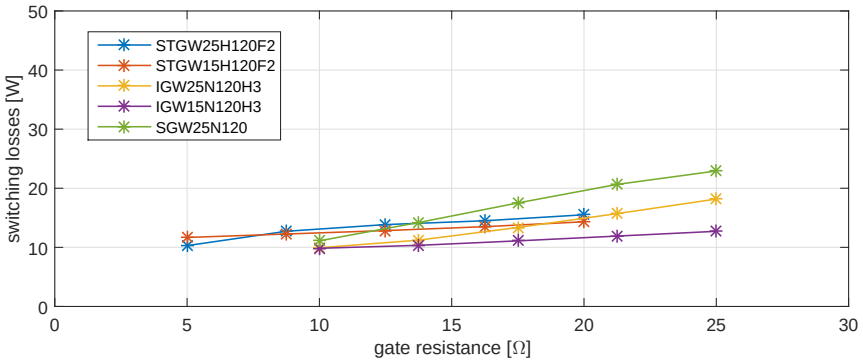
An interesting behavior of the SiC C3M0065090D switch is observed in Figure 5-6 (b), where it is greatly affected by the gate resistance. A closer look at Table 5-2 shows that C3M0065090D and C3M0065090J switches have the same device parasitics but different switching times and



(Si MOSFET)



(SiC MOSFET)



(IGBT)

Figure 5-3: Switching losses as a function of the gate resistance R_g ($f_s = 27.5$ kHz).

packaging. This leads to the conclusion that the packaging parasitics for C3M0065090D are worse and deteriorate significantly the performance of this switch; the switching losses are more than double as the gate resistance increases. On the other hand, it appears that C3M0065090J has very low packaging parasitics and as a result, faster switching times and superior performance. If the modeling would be based only on the device parasitics, the two switches should have the same performance. This observation stresses the importance of including the packaging parasitics in the modeling for the switching behavior.

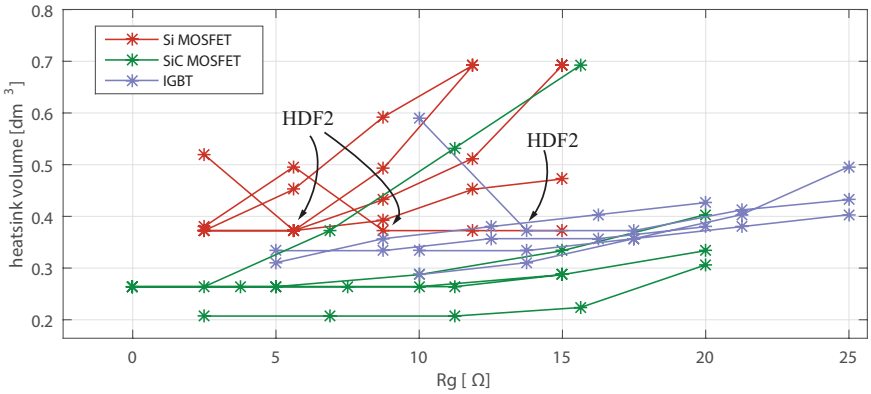


Figure 5-4: Heatsink volume dependency on the semiconductors losses as a function of the gate resistance R_g ($f_s = 27.5$ kHz).

5-2-4 EMI - Electrical interdependencies

The dependency of the EMI filter on the transients will be observed via the CM inductance requirement for the EMI filter. First, the CM inductance for inverters with different switches is calculated with respect to the switching frequency, as shown in Figure 5-5 the CM inductance variation with the switching frequency is shown. The relation between the switching frequency and EMI filtering is not monotonous. From the presented results it is observed that higher switching frequencies do not always lead to a smaller filter. The reason is that the harmonic spectrum of the CM noise changes, leading to local optimal points for different switching ranges. Thus there are some preferred switching frequencies switching frequencies, as was shown in [23], which result to a smaller filter. In this case study, these frequencies are 27.5 kHz at the 27.5 - 42.5 kHz range and 47.5 kHz at the 47.5 - 57.5 kHz range. As was mentioned before, there is a small variation in the CM inductance for different switches, which is also obvious in the results shown in Figure 5-5.

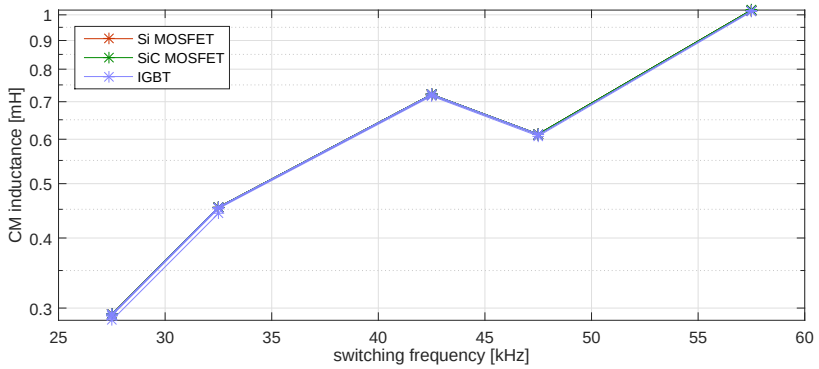
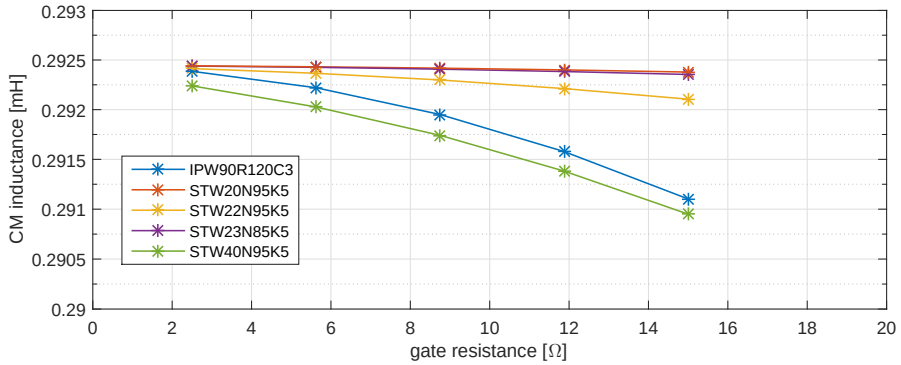
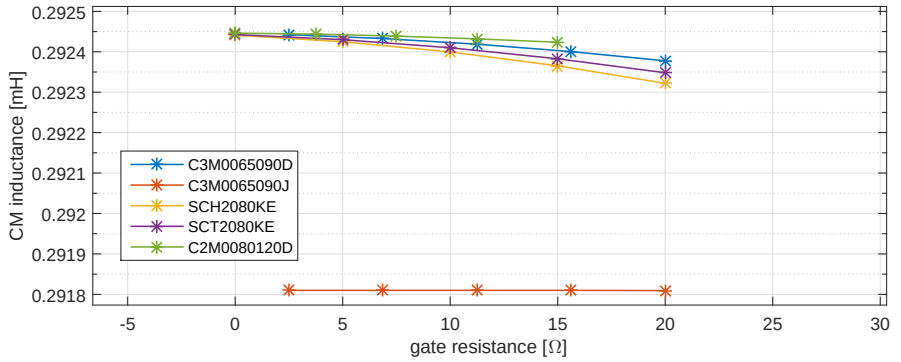


Figure 5-5: CM inductance variation with respect to the switching frequency.

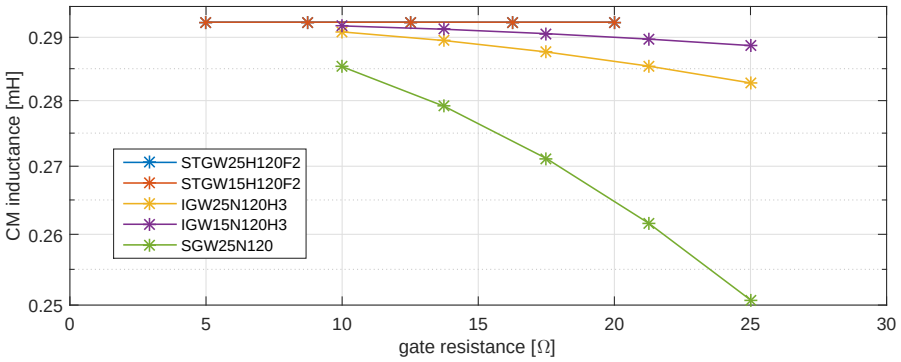
Next, the dependency of the CM inductance on the gate resistance will be explored. In Figure 5-6 the CM inductance variation with the gate resistance is shown. As a consequence of the slower switching times with increased R_g, the requirement for CM EMI filtering is relaxed.



(Si MOSFET)



(SiC MOSFET)



(IGBT)

Figure 5-6: CM inductance as a function of the gate resistance R_g ($f_s = 27.5$ kHz).

However, the effect of the gate resistance is very small on the noise source, which is reflected to the small variation of the CM inductance values. This is expected, since the EMI models do not consider the component and layout parasitics in the propagation path. The resonance of these parasitics would cause a lower impedance path at high frequencies, which would change the attenuation target; thus the filter corner frequency changes. Consequently, the results of the EMI modeling in this work are valid only for the low frequencies, below 1 MHz. For a comprehensive analysis of the EMI noise in the high frequency range, the layout and component parasitics should be included.

Regarding the DM noise suppression, the parametric sweep results showed that the C_{DL} capacitor (see Figure 4-21) is not required for the filter on the LISN side. The reason is that the DM noise is filtered by both the DC-link capacitor and the CM capacitors, because they are in the DM propagation path. However, with increasing switching frequency, lower filtering requirement is obtained for the DC-link filter, as illustrated in Figure 5-7. As a result, it is possible that for higher frequencies than the ones used in this work, the C_{DL} capacitor will have to be sized according to the EMI requirements.

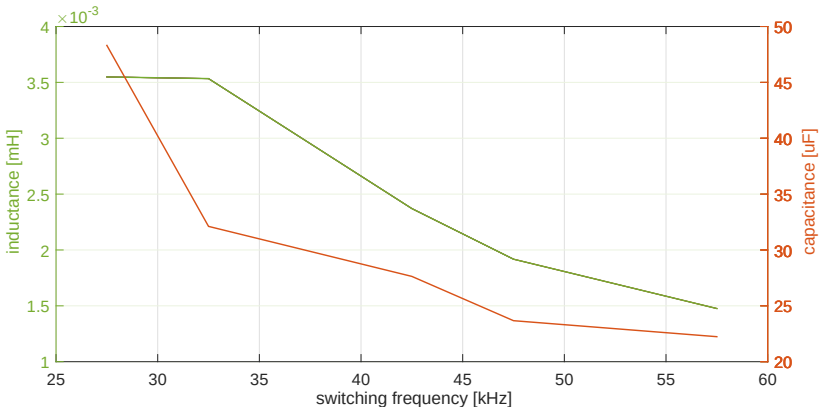


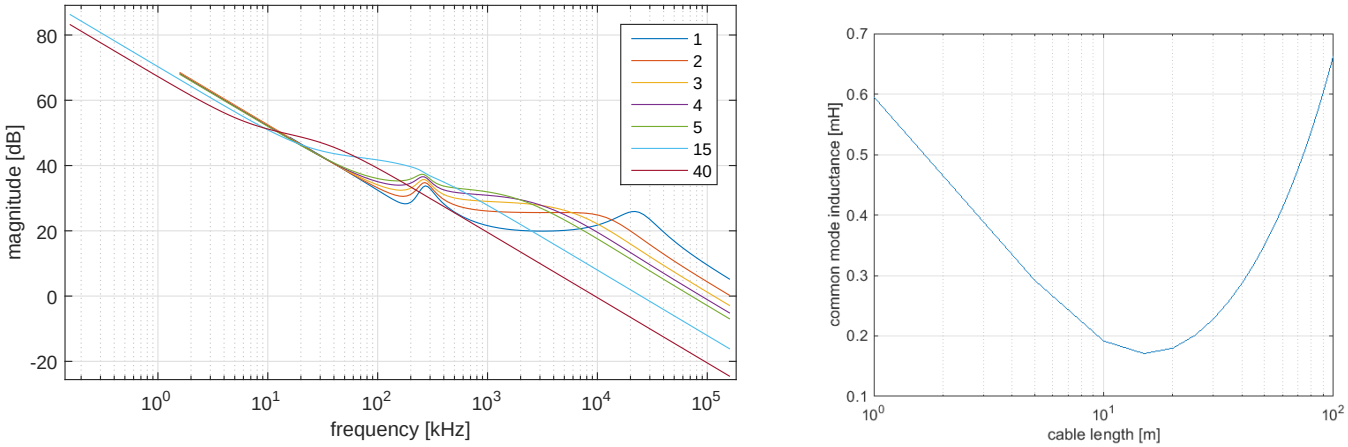
Figure 5-7: Capacitance and inductance variation of the DC-link filter with switching frequency.

5-2-5 EMI - Inverter parasitics interdependencies

It would be expected that the inverter with the SiC C3M0065090J switch would have the greatest requirement for CM inductance (see Figure 5-6 (b)), since this switch is the fastest. However, for that inverter the propagation path is different from the others, due to the switch parasitic capacitance through the heatsink grounding. Specifically, the package 7LD2PAK has a smaller area than the TO-247 packages, which results to a parasitic capacitance C_p of 15.17 μF and 45.79 μF for each package respectively. This smaller C_p provides a higher impedance path for the CM EMI, which results to lower CM noise on the LISN and thus lower EMI filtering requirement.

5-2-6 EMI - Load parasitics interdependencies

The dependence of the EMI filtering on the load parasitics is investigated by a variation of the cable length. Specifically, the machine and inverter impedances are kept constant, and the cable impedance is altered by increasing the cable length. The effect of the cable length on the CM EMI filter is illustrated in Figure 5-8. For the considered parasitic parameters of the machine and cable, the presented results show that there cable impedance dominates for cable lengths larger than 15 m. For longer cables the resonant frequency of the cable impedance is smaller than the machine impedance resonant frequency, hence larger filter is required. Specifically, for longer cables the CM impedance becomes smaller at the 150 kHz limit and thus the noise is worse. However, such lengths are extreme, since realistic cable



(a) (b)

Figure 5-8: Cable length effect on EMI filtering: (a) CM propagation path impedance, (b) CM inductance dependence on the cable length.

lengths are below 5 m. Thus, the results of Figure 5-8 can be used only for comparison of the relative impedances on the load path. In addition, the two resonance points correspond to the machine and cable parasitics resonance, because the lumped components Π model has been used for the propagation path. As a result, only a first order estimation is possible with this model. The actual parasitics should be measured with an impedance analyzer and included in the model. This requires a more complex model with distributed parasitic elements, so that the effect of resonances at higher frequencies can be accounted for.

5-3 System performance

Having determined the interdependencies of the design domains with the models, a parametric sweep for the selected switches, switching frequency and gate resistance is conducted. The result is a set of possible designs which fulfill the power requirements. The performance of these designs is evaluated by means of the following performance indexes: efficiency η, power density ρ [kW/dm^3] and power per unit weight γ in [kW/kg]. The power density and power per unit weight are very useful metrics for aerospace applications, since converters with minimum size are required. Here, ρ and γ refer to the rated output power over the net volume and weight of the components. Using these performance indexes the designs can be directly compared and the best design can be chosen.

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \tag{5-1}$$

$$\rho = \frac{P_{out}}{volume} \tag{5-2}$$

$$\gamma = \frac{P_{out}}{weight} \tag{5-3}$$

Figure 5-9 shows the system performance of the designs generated by the parametric sweep. Since discrete steps are used to increase the volume of the heatsink, vertical lines

with the same volume are observed for different designs. Specifically, the concentration of designs around $\rho = 7.8$ corresponds to the transition in the algorithm from one heatsink configuration to the next. In addition, the passives volumes are not optimized. If a linear model or estimation for the heatsink and passives volume would be used, then a smooth decrease in volume and weight would be observed. Nevertheless, the results prove that the links can be manipulated with the design variables. As a result, this process would be more powerful with optimization techniques. In the presented results, the passives volume did not decrease significantly with increasing switching frequency. Thus, the parametric sweep shows that the trends of the designs for operation at maximum temperature are dominated by the increase of the heatsink volume for increasing switching frequency and gate resistances. Since the semiconductor losses are dominant in the designs, the power density limit of the inverters is determined by these losses.

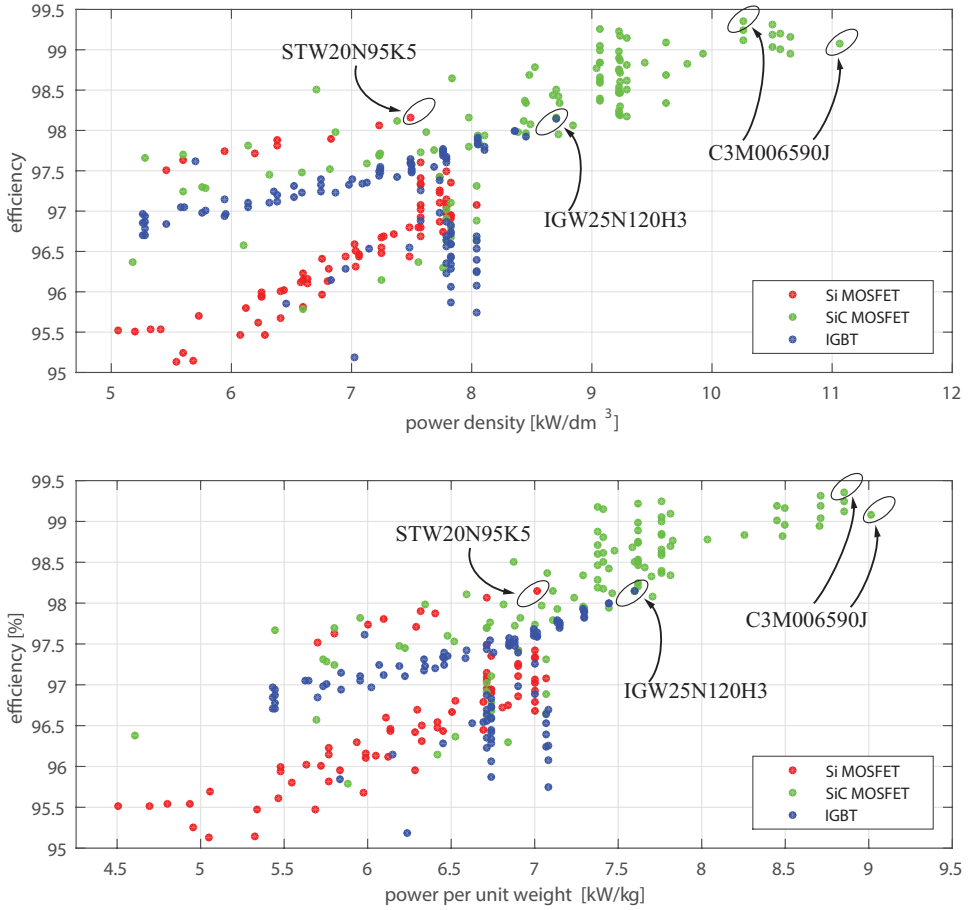


Figure 5-9: System performance evaluation with respect to efficiency versus power density and efficiency versus power per weight.

From the presented results in Figure 5-9, it is obvious that the inverters with SiC MOSFETs have superior performance. In addition, the lower power rating and operating temperature of Si MOSFETs results to lower efficiency and bulkier designs compared to SiC MOSFETs and IGBTs. For inverters with IGBTs, larger heatsink is required due to the increased losses,

leading to lower power densities. In Figure 5-9 the inverters with maximum power density and maximum power per unit weight for each semiconductor technology are noted. Specifically, two inverters with SiC MOSFETs are illustrated, sine the one gives maximum efficiency and the other maximum power density. The metrics for these designs are summarized in Table 5-4.

Table 5-4: Best designs comparison

switch	η	volume	weight	ρ	γ	parameters
	[%]	[dm^3]	[kg]	[kW/dm^3]	[kW /kg]	
C3M006590J	99.08	0.452	0.555	**11.07**	**9.01**	f_s = 57.5 kHz, R=min.
C3M006590J	**99.36**	0.487	0.5917	10.57	8.45	f_s = 27.5 kHz, R=min.
IGW25N120H3	98.14	0.575	0.658	8.7	7.6	f_s = 27.5 kHz, R=min.
STW20N95K5	98.15	0.668	0.713	7.49	7.01	f_s = 27.5 kHz, R=min.

The outcome of this table is that the increase in power density and power per unit weight is significant when the SiC MOSFET is used. Even though the efficiency is increased about 1% by using SiC MOSFETs, the power density improvement is around 47% and 41% compared to the Si MOSFET, and 27% and 22% compared to the IGBT, for operation at 57.5 and 27.5 kHz respectively. A similar improvement in power per unit weight is observed. Specifically, operation at 57 kHz gives 28% increase and operation at 27.5 kHz a 20% increase in γ, compared to the Si MOSFET.

The differences between the two designs with the C3M006590J switch are due to the relative volume and weight of the heatsink and capacitor bank. Figure 5-10 shows the volume distribution between these designs. As was shown in the previous paragraphs, higher switching frequencies result to smaller DC-link capacitor bank but higher CM inductor. However the relation between the two is in favor of the capacitor decrease. Thus, considering the CM capacitors are kept constant, the passives overall volume is lower. In addition, the heatsink

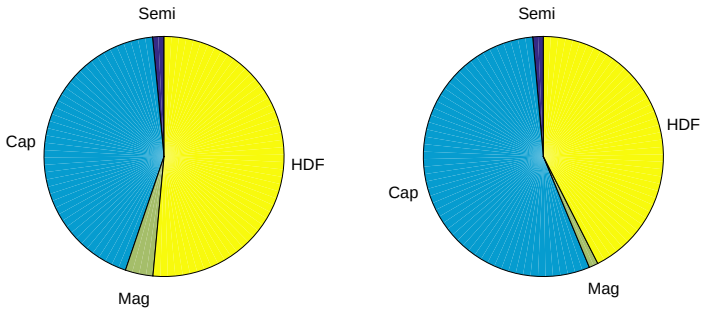


Figure 5-10: Overview of the components volume distribution for the C3M006590J switch inverter at 57.5 (left) and 27.5 kHz (right).

used for both designs corresponds to the minimum volume. The result is 121 ^{o}C and 139 ^{o}C operating temperature for the switches at 27.5 and 57.5 kHz respectively. For the considered heatsink, the design with the C3M006590J switch at 57.5 kHz and 2.5 Ω resistance is the best candidate. The design parameters of this inverter are summarized in Table 5-5. If a different

heatsink would be used, then it is expected that higher power density for the same efficiency could be obtained at 27.5 kHz operation. This would be possible if optimization would be employed.

Table 5-5: Inverter parameters

Parameter	Value
η	99.08%
ρ	11.07 [kW/dm^3]
γ	9.01 [kW/kg]
Switch	C3M006590J
Diode	C4D20120A
C_{CR}	2.82 [μF]
C_{CL}	0.282 [nF]
L_{CM} (L_σ)	1.1 [mH] 18.46 [μH]
C_{DR}	22.238 [μF]
Heatsink	76.2 $\times$ 20 $\times$ 98.5 (w$\times$h$\times$l)[mm]
Fan	109P412M701

5-4 Summary

In this chapter, the results of the design framework developed in this thesis project were discussed. The interdependencies of the design domains were demonstrated by manipulating the links with a parametric sweep of the selected design variables, namely switch technology, switching frequency and gate resistance.

The thermo-mechanical dependencies were quantified by the thermal coupling of the semiconductors due to the spatial design considerations and heat transfer through the heatsink base-plate. The parametric sweeps were conducted considering heatsink design for maximum operating temperature of the components. Thus the electro-thermal dependencies were quantified by the losses and cooling effort, which was expressed by the heatsink volume for maximum temperature operation. In addition the results showed the importance of including the package parasitics in the switching losses models. Specifically, two semiconductors with same device characteristics but different packaging showed a significant difference in switching losses.

The dependencies of the EMI and electrical domains were quantified by the CM inductance for the EMI filtering requirement. For increasing gate resistance the filtering requirement was reduced. However, the relation of the filter to the switching frequency was not monotonous, leading to selection of optimal switching frequency areas. In addition, the dependency of the EMI noise on the package parasitics was also quantified by the CM inductance. Smaller semiconductor packages lead to higher impedance path for the EMI noise. Finally, the dependency of the EMI noise on the load parasitics was quantified by the effect of the cable length on the designed filter. From the presented results regarding the EMI domain dependencies, it is concluded that neglecting the package, component and layout parasitics limits the accuracy of the filter design to low frequencies below 1 MHz.

In the last part of this chapter, the system performance of the generated designs from the parametric sweep was discussed. The performance of the designs was evaluated by efficiency, power density and power per unit weight metrics. The inverters obtained with SiC MOSFET technology showed superior performance compared to inverters with Si MOSFETs and Si IGBTs. Thus this technology looks promising for high power density designs in aerospace applications.

From the set of the generated designs, the best designs obtained with each semiconductor technology were compared. With the SiC MOSFET inverter a 47% and 27% increased power density was achieved compared to the Si MOSFET and IGBT inverters. Hence, this inverter was selected as the preferred choice, where 99.08% efficiency, 11.07 [kW/dm^3] power density and 9.01 [kW/kg] power per unit weight was achieved, considering net component volume and weight.

Chapter 6

Conclusions and suggestions for future work

6-1 Conclusions

The main objective of this master thesis is the investigation of the interdependencies in the design domains of an inverter for aerospace applications. A design methodology was developed using the multi-domain design approach for power electronic converters and the links between the design domains were established. Based on this methodology, a virtual prototype of an inverter was realized in software using analytical modeling and a high power density aerospace inverter was designed to drive a PMSM load, according to the specifications of Aeronamic B.V. Following the discussions and results presented in this thesis, the most important elements are summarized as follows:

- The design methodology developed in this work focuses on determining the boundaries of the design aspects and formulating the relationships between the design objectives, requirements and variables. The converter design is treated as a system from a top level point of view, leading to the selection of a topology, modulation and control strategy. The circuit level design is effectively decoupled into the electrical, EMI, thermal and mechanical design domains, which are treated independently. The links between the design domains are established though their mutual dependencies, leading to reduced complexity in the design process.
  - By using the proposed methodology, full control is achieved over the design process. The interdependencies of the design domains can be manipulated using design variables, similar to an optimization problem. This can be used to determine the impact of the design choices in the converter performance.
  - As regards the modeling accuracy, the methodology is independent of the modeling effort. For a selected model, the results can be used to conclude on the modeling effort needed for different design objectives.

- A design framework has been developed in Matlab software, using analytical models. The interdependencies between the design domains were partially manipulated by a parametric sweep of the selected design variables. Even though the obtained designs may be preferred rather than optimal, the results showed the trade-offs between different design choices which can be applied to an aerospace inverter. Thus the proposed framework can form a basis for a complete manipulation of the interdependencies by optimization techniques.

  - With the models developed in the design framework, an estimation of the inverter's performance was obtained for a preliminary design stage. From the presented results, the performance trends for different semiconductor technologies were obtained. Moreover, it was possible to discard low performance designs from the design space.
  - The results showed that with the models used for the semiconductors' losses, a good comparison can be made between different switch technologies. The accuracy of the modeling of the passive losses proved to be less significant in this work, since the semiconductors are the major losses contributor and the passive components are operated below their thermal limit. In extreme thermal operating conditions, a higher accuracy of the passive component losses would be required. In addition, the thermal coupling between the components is well established by the proposed thermal models and spatial design in this work. Finally, it was concluded that neglecting the layout, component and package parasitics, brings a limiting factor for the accuracy of the EMI noise in the high frequencies. Therefore, further improvement is required in this direction.

- An aerospace inverter was designed achieving 99.08% efficiency and 11.07 kW/dm^3 power density for net component volume. The design of this inverter was obtained by using SiC MOSFET as the main power switches operating at 57.5 kHz. This design achieved a 47% and 27% higher power density from the best designs obtained with Si MOSFET and Si IGBT switches respectively. These results suggest that the SiC technology can be beneficial for aerospace applications, where high power density is a major performance index in this area.

- Compared to prior art, the interdependencies of the design domains were investigated in this thesis project. In addition, all design domains were included in this work and a design framework was developed for systematic inverter design. In contrast to other works which focus mostly on the circuit level design aspects of the inverter, a minimum current sizing design for the inverter was proposed, based on the operation of the PMSM load under drive limitations. A previously proposed scaling method for the sizing of the passives and semiconductors, could not be used because the database it was based on was not available; thus analytical equations were used to model the physical behavior of actual components. The spatial design and comprehensive thermal models were developed and discussed. Moreover, the load parasitics of the EMI propagation path were considered in the design, however the component parasitics were not included. Thus, further development is needed regarding the modeling of the layout and package parasitics. Finally, optimization was not in the scope of this thesis, thus the design interdependencies were manipulated with parametric sweep of the design variables. It

is expected that multi-objective optimization will more effectively manipulate the links and thus better performance metrics will be achieved.

6-2 Suggestions for future work

Over the course of this thesis a number of possible areas of further investigation have been determined.

- First of all, it would be interesting to implement the designed inverter in order to compare the estimated performance with experimental results. Moreover, the effect of the layout and component parasitics on the semiconductor losses and on the design of the EMI filter can be examined.
- Secondly, the design framework developed in this work generates designs for a selected topology using a parametric sweep. This framework can be extended employing an optimization algorithm so that the optimal design of the topology can be obtained and the performance limitations of different inverter topologies can be examined.
- In addition, the switching behavior of the semiconductors could be further modeled so that the layout and package parasitics can be included in the behavioral models. It is expected that such models will increase the accuracy in the switching losses and transients estimation.
- Moreover, a limitation of the modeling in this work was observed regarding the EMI filter design in high frequencies. The models can be further improved by considering the effect of the layout, semiconductor package and passive component parasitics.
- Furthermore, comprehensive thermal models were developed in this work for steady state operation of the components. For design objectives where there are requirements for transient thermal behavior, dynamic models of the heat transfer can improve the accuracy.
- Finally, the proposed design methodology in this study has been applied to an aerospace inverter design. However, it can be used to investigate how the application boundaries and requirements will affect the design of a different converter type.

Appendix A

Topology comparison analytical models

The analytical models of the switching behavior for the following topologies are based on the analysis of [44] and [47].

The semiconductors used for the hard switching and soft-switcihng topologies are the SK35GAR12T4 and SKM50GAL12T4 modules respectively for 5 kW, and the SKM100GB12V and SKM150GAR12T4 modules for 50 kW from SEMIKRON. The circuit resonant parameters are summarized in Table A-1.

Table A-1: Resonant circuit parameters

component	ARCDCL	CMRPI	ASCRPI
C_r	4.4 μF	0.05μF	0.3μF
L_r	6.4 μH	45μH	7.5μH

In the following models, the variables used are:

- ϕ: machine power factor angle
- θ: inverter current angle
- m: modulation ratio
- f_s: switching frequency
- I_m: peak load current
- V_{dc}: DC-link voltage
- $V_{f,sw}$: IGBT on-state voltage
- $V_{f,D}$: diode on-state voltage

- R_{ce}: IGBT on-state resistance
- R_{ak}: diode on-state resistance
- t_f: voltage fall time
- L_r: resonant inductance
- C_r: resonant capacitance
- Z_r: resonant impedance
- R_r: inductor resistance
- I_r: peak resonant current

Semiconductor on-state models

$$V_{ce} = V_{f,sw} + IR_{ce} \tag{A-1}$$

$$V_{ak} = V_{f,D} + IR_{ak} \tag{A-2}$$

Hard switching inverter (HSVSI)

- Main switch conduction losses

$$P_{c,sw} = \frac{1}{2} I_m V_{f,sw} \left(\frac{1}{\pi} + \frac{m}{4} \cos(\phi) \right) + I_m^2 R_{ce} \left(\frac{\sqrt{3}}{8\sqrt{\pi}} + \frac{m}{3\pi} cos(\phi) \right) \tag{A-3}$$

- Main diode conduction losses

$$P_{c,D} = \frac{1}{2} I_m V_{f,sw} \left(\frac{1}{\pi} - \frac{m}{4} \cos(\phi) \right) + I_m^2 R_{ce} \left(\frac{\sqrt{3}}{8\sqrt{\pi}} - \frac{m}{3\pi} cos(\phi) \right) \tag{A-4}$$

- Main switch switching losses

$$P_{sw,sw} = \frac{1}{\pi} f_s (E_{on} + E_{off} + E_{rr}) \frac{V_{dc}}{V_{ref}} \frac{I_m}{I_{ref}} \tag{A-5}$$

Actively lamped resonant DC-link inverter (ACRDCL)

- Main switch conduction losses
  same as in (A-3)
- Main diode conduction losses
  same as in (A-4)
- Main switch switching losses

$$P_{sw,sw} = \left(\frac{1}{2} \frac{I_m^2 \; t_f^2}{24 \; C_r} f_s \right) \tag{A-6}$$

- Clamp device conduction losses

$$P_{c,cl} = \frac{k(2-k)}{k-1} V_d V_{dc} C_r f_s \tag{A-7a}$$

$$V_d = V_{ce} + V_{ak})/2 \tag{A-7b}$$

- Clamp device switching losses

$$P_{sw,cl} = \frac{k(2-k)}{24 L_r} t_f \ V_{dc}^2 \ f_s \tag{A-8}$$

- Inductor ohmic losses

$$P_{Lr} = \left(\frac{P_{inv}}{V_s}\right)^2 R_r + \frac{C_r}{2L_r} V_s^2 R_{\ r} \tag{A-9}$$

where V_{ref} is the losses reference voltage, I_{ref} is the losses reference current and E_{on}, E_{off} and E_{rr} are the on-, off-state and reverse recovery energies.

Clamped mode resonant pole inverter (CMRPI)

- Main switch conduction losses

$$P_{c,sw} = \frac{1}{2} I_r (V_{f,sw} + I_r R_{ce}) + \frac{I_m^2}{4} R_{ce} + \frac{1}{\pi} I_m (V_{f,sw} + 2 I_r R_{ce}) \tag{A-10}$$

- Main diode conduction losses

$$P_{c,D} = \tfrac{1}{4} I_r (V_{f,D} + I_r R_{ak}) + \tfrac{I_m^2}{8} R_{ak} + \tfrac{1}{2\pi} I_m (V_{f,D} + 2 I_r R_{ak}) - \ldots$$

$$m \cos(\phi) \left[\frac{I_r}{2\pi} (V_{f,D} + I_r R_{ak}) + \frac{I_m}{8} (V_{f,D} + 2 I_r R_{ak}) + \frac{I_m^2}{3\pi} R_{ak} \right] \tag{A-11}$$

- Clamping diode conduction losses

$$P_{c,cl} = \left(\frac{1}{4} + \frac{m \cos(\theta)}{2\pi} \right) I_r (V_{f,D} + I_r R_{ak}) \tag{A-12}$$

- Main switch switching losses
  same as in (A-6)

- Inductor ohmic losses

$$P_{Lr} = \frac{3}{2} \left(1 - 2\frac{f_s}{f_r}\right) \left(\frac{1}{\pi} + \frac{m}{\pi} \cos(\phi) \right) \left(I_m + \frac{V_{dc}}{Z_r} \right)^2 R_r \tag{A-13}$$

Auxiliary switch commutated resonant pole inverter (ASRCPI)

- Main switch conduction losses
  same as in (A-3)
- Main diode conduction losses
  same as in (A-4)
- Main switch switching losses
  same as in (A-6)
- Auxiliary switch conduction losses

$$P_{c,Sr} = \frac{3}{2}\left(I_m + \frac{V_s}{Z_r}\right)(V_{ce} + V_{ak})T_p f_s \tag{A-14a}$$

$$T_p = \pi\sqrt{2C_r L_r} \tag{A-14b}$$

- Inductor ohmic losses

$$P_{Lr} = \frac{3}{\pi}\left(I_m + \frac{V_s}{Z_r}\right)^2 R_r T_p f_s \tag{A-15}$$

Appendix B

Thermal models

Heatsink convective heat transfer

The convective heat transfer mechanism is determined by the operating point of the fan, which is obtained according to the following equation

$$\Delta P_{fan} - \Delta P_{diff} = \Delta P_{chan} \tag{B-1}$$

where ΔP_{fan} is the fan pressure, ΔP_{diff} is the diffuser pressure and ΔP_{chan} is the pressure drop in the heatsink channels. The left part of (B-1) can be calculated by combining the Bernoulli's equation (B-2a) and continuity equation (B-2b), considering the system as an expanding contracting pipe, shown in Figure B-1.

$$\frac{p_1}{\rho g} + \frac{u_1^2}{2g} + z_1 = \frac{p_2}{\rho g} + \frac{u_2^2}{2g} + z_2 \tag{B-2a}$$

$$A_1 u_1 = A_2 u_2 = \dot{V} \tag{B-2b}$$

where ρ is the medium density, $g = 9.8196\ m/s^2$ is the gravity constant, u is the flow speed, p is the pressure and z is the height, $\dot{V}$ is the flow rate and A is the cross-sectional area. Here, the subscripts 1 and 2 refer to the fan- and heatsink-end of the diffuser respectively.

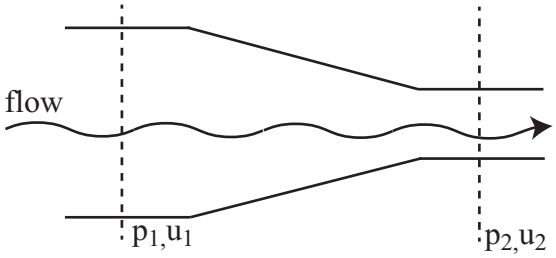


Figure B-1: An expanding contracting pipe.

Along the heatsink length L, the airflow creates a pressure drop ΔP, which is dependent on the heatsink operating point. Based on the analysis of [64], the pressure drop in the heatsink channels can be calculated with empirical equations. For this problem, the average Reynolds number Re_m is defined as follows

$$Re_m = 2 \cdot \frac{\dot{V}}{N_x \cdot c_v \cdot (s + c)} \tag{B-3}$$

If $Re_m \leq 2300$ the air-flow is defined as laminar, otherwise it is defined as tubular. In turbulent flow oscillations in the air particles are amplified, whereas in laminar flow they are damped out. Hence, with turbulent flow the heat transfer is better, however the pressure drop is increased [64]. Defining the hydraulic diameter of on channel as

$$dh = \frac{2 \cdot s \cdot c}{s + c} \tag{B-4}$$

the pressure drop along the heatsink channels and the characteristic Nusselt number Nu can now be calculated, for laminar or turbulent flow:

- Laminar flow

$$\Delta P_{chann}(\dot{V}) = 1.5 \frac{\cdot 32 \cdot \rho \cdot c_v \cdot l \cdot}{N_x \cdot s \cdot c \cdot dh^2} \cdot \dot{V} \tag{B-5a}$$

$$X = \frac{L}{dh \cdot Re_m \cdot Pr} \tag{B-5b}$$

$$Nu = \frac{3.657 \cdot \left(tanh(2.264 \cdot X^{1/3} + 1.7 \cdot X^{2/3}) \right)^{-1} + \frac{0.0499}{X} \cdot \tanh(X)}{\tanh(2.432 \cdot Pr^{1/6} \cdot X^{1/6})} \tag{B-5c}$$

- Turbulent flow

$$\Delta P_{chann}(\dot{V}) = \frac{L \cdot \frac{s+c}{2s \cdot c} \cdot \rho \frac{1}{2} (\frac{\dot{V}}{N_x \cdot s \cdot c})^2}{\left(0.79 \cdot \ln \left(\frac{2\dot{V}}{N_x \cdot (s+c) \cdot c_v)} \right) - 1.64 \right)^2} \tag{B-6a}$$

$$Nu = \frac{\{8 \cdot (0.79 \cdot \ln(Re_m) - 1.64)^2\}^{-1} \cdot (Re_m - 1000) \cdot Pr}{1 + 12.7 \cdot \sqrt{\{8 \cdot (0.79 \cdot \ln(Re_m) - 1.64)^2\}^{-1}} \cdot (pr^{2/3} - 1)} \left(1 + (\frac{d_h}{L})^{2/3} \right) \tag{B-6b}$$

where c_v is the cinematic viscosity of the air, ρ is the density of the air, N_x is the number of channels, c is the height of fins and $s = width_{channel} + width_{fin}$ is the effective channel width. The above set of equations is used in the pressure difference equation (B-1) and the operating point is obtained. Having determined the Nusselt number for the fan operating point, the convective heat transfer coefficient h_{air} is given:

$$h_{air} = \frac{Nu(\Delta P_{op.point}) \cdot \lambda_{air}}{d_h} \tag{B-7}$$

h_{air} will be used for the calculations of the thermal resistance from the heatsink fins and base plate to the air, as will be shown in the following paragraph.

Heatsink conductive heat transfer equivalent

Based on the convective heat transfer mechanism presented in 2-3-7, the thermal resistor values for the heatsink model are calculated as follows:

$$R_{hs} = \frac{\frac{1}{2} \cdot d_{hs}}{\lambda_{hs} \cdot W_{chan} \cdot \frac{L}{N_y}} \tag{B-8}$$

$$R_x = \frac{\frac{1}{2} \cdot (W_{chan} + W_{fin})}{\lambda_{hs} \cdot d_{hs} \cdot \frac{L}{N_y}} \tag{B-9}$$

$$R_y = \frac{\frac{1}{2} \cdot \frac{L}{N_y}}{\lambda_{hs} \cdot (W_{chan} + W_{fin}) \cdot d_{hs}} \tag{B-10}$$

$$R_{f1} = \frac{\frac{1}{2} \cdot W_{fin}}{\lambda_{fin} \cdot \frac{L}{N_y} \cdot \frac{d_{fin}}{N_z}} \tag{B-11}$$

$$R_{air1} = \frac{1}{h_{air} \cdot \frac{L}{N_y} \cdot \frac{d_{fin}}{N_z}} \tag{B-12}$$

$$R_{f2} = \frac{\frac{d_{fin}}{N_z}}{\lambda_{fin} \cdot \frac{W_{fin}}{2} \cdot \frac{L}{N_y}} \tag{B-13}$$

$$R_{hf} = \frac{\frac{1}{2} d_{hs}}{\lambda_{hs} \cdot \frac{W_{fin}}{2} \cdot \frac{L}{N_y}} \tag{B-14}$$

$$R_{air2} = \frac{1}{h_{air} \cdot W_{chan} \cdot \frac{L}{N_y}} \tag{B-15}$$

where L is the heatsink length, d_{hs} is the base-plate thickness, W_{chann} is the channel width, W_{fin} is the fin width, d_{fin} is the fin height, λ_{hs} is the base-plate conductivity, λ_{fin} is the fin conductivity, N_y is the number of segments in the y-axis along the heatsink length, N_z is the number of segments in the z-axis along the fin height and h_{air} is the convective transfer coefficient calculated form (4-32). In the models $N_z = 3$ and the partitioning in the y-axis depends on the heatsink length.

The system is simplified with equivalent resistor networks in series and parallel connection as follows.

$$R_1 = R_{f1} + R_{air1} \tag{B-16}$$

$$R_3 = R_{hf} + R_{f2} \tag{B-17}$$

$$R_c = R_{hs} + R_{air2} \tag{B-18}$$

$$R_2 = R_{f2} \tag{B-19}$$

$$R_F = ((((R_1 + R_2)//R_1) + R_2)//R_1) + R_3 \tag{B-20}$$

$$R_z = R_F//R_F//R_c \tag{B-21}$$

where R_F is calculated for 3 segments on the z axis.

Toroid thermal model equivalent

The elementary thermal resistors are determined according to (2-2). In the following equations the subscripts *core*, *ins*, *core*, *ins*, *cu*, *cu* and *paste* refer to the properties of the magnetic core, core insulation, wire insulation, copper wire and thermal conducting material properties.

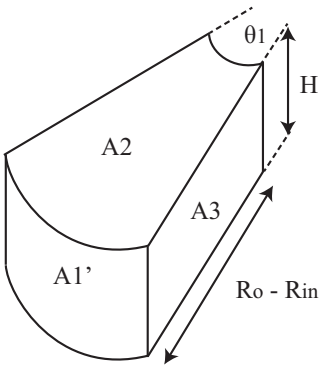


Figure B-2: 3D representation of toroid elementary Segment A.

$$A_1 = H \cdot R_{in} \cdot \theta_1 \tag{B-22}$$

$$A_1' = H \cdot R_o \cdot \theta_1 \tag{B-23}$$

$$A_2 = \frac{1}{2} \cdot \theta_1 \cdot (R_o^2 - R_{in}^2) \tag{B-24}$$

$$A_3 = H \cdot (R_o - R_{in}) \tag{B-25}$$

$$R_{mid} = \frac{R_o - R_{in}}{2} + R_{in} \tag{B-26}$$

- Segment A

$$R_1 = \frac{H/2}{\lambda_{core} \cdot A_2} \tag{B-27}$$

$$R_2 = \frac{\ln(R_{mid}/R_{in})}{\lambda_{core} \cdot H \cdot \theta_1} \tag{B-28}$$

$$R_2' = \frac{\ln(R_o/R_{mid})}{\lambda_{core} \cdot H \cdot \theta_1} \tag{B-29}$$

$$R_3 = \frac{d_{ins,core}}{\lambda_{ins,core} \cdot A_2} \tag{B-30}$$

$$R_4 = \frac{d_{ins,core}}{\lambda_{ins,core} \cdot A_1} \tag{B-31}$$

$$R_4' = \frac{d_{ins,core}}{\lambda_{ins,core} \cdot A_1'} \tag{B-32}$$

$$R_5 = \frac{d_{ins,cu}}{\lambda_{ins,cu} \cdot \pi \cdot r_{wire} \cdot (R_o - R_{in})} \tag{B-33}$$

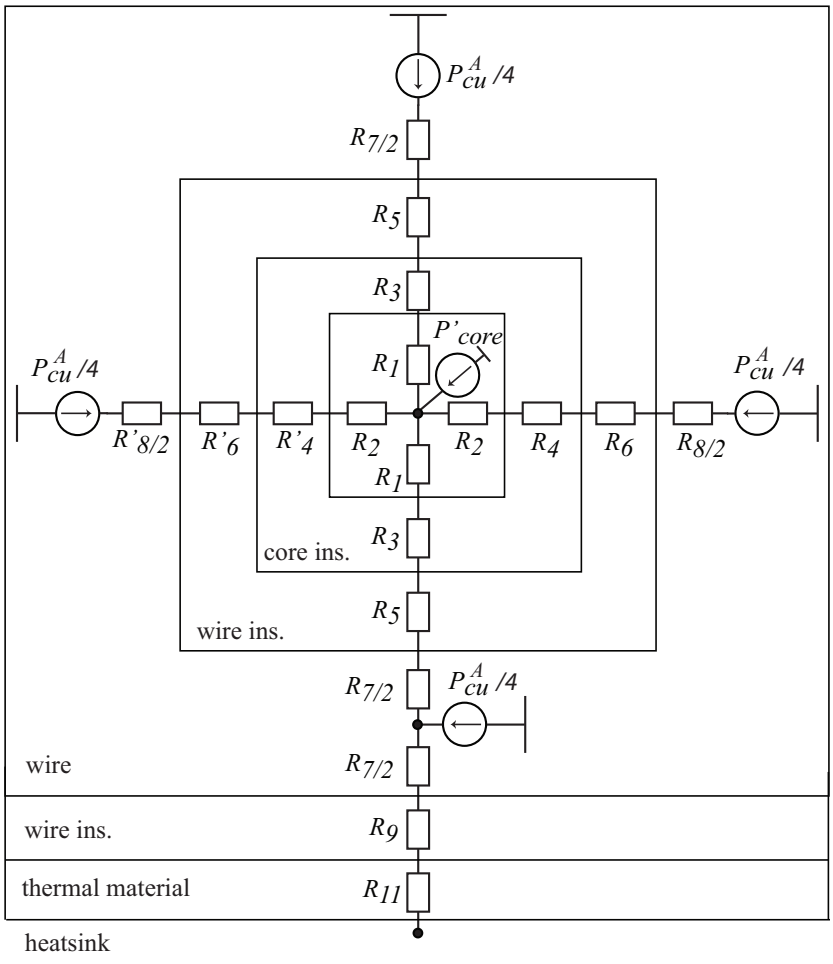


Figure B-3: Segment A 2D representation.

$$R_6 = \frac{d_{ins,cu}}{\lambda_{ins,cu} \cdot \pi \cdot r_{wire} \cdot H} \tag{B-34}$$

$$R_7 = \frac{1}{4 \cdot \pi \cdot \lambda_{cu} \cdot \pi \cdot (R_o - R_{in})} \tag{B-35}$$

$$R_{7/2} = 2 \cdot R_7 \tag{B-36}$$

$$R_8 = \frac{1}{4 \cdot \pi \cdot \lambda_{cu} \cdot \pi \cdot H} \tag{B-37}$$

$$R_{8/2} = 2 \cdot R_8 \tag{B-38}$$

$$R_9 = \frac{d_{ins,cu}}{\lambda_{ins,cu} \cdot \pi \cdot r_{wire} \cdot (R_o - R_{in})} \tag{B-39}$$

$$R_{11} = \frac{d_{paste}}{\lambda_{paste} \cdot A_2} \tag{B-40}$$

- Segment B

$$R_c = \frac{R_{mid} \cdot \theta_2}{\lambda_{core} \cdot H \cdot (R_o - R_{in})} \tag{B-41}$$

The system is simplified with equivalent resistor networks (series and parallel connection):

$$R_{17} = R_1 + R_3 + R_5 + R_{7/2} \tag{B-42}$$

$$R_{711} = R_{7/2} + R_9 + R_{11} \tag{B-43}$$

$$R_{28} = R_2 + R_4 + R_6 + R_{8/2} \tag{B-44}$$

$$R'_{28} = R'_2 + R'_4 + R_6 + R'_{8/2} \tag{B-45}$$

$$R_{28p} = R_{28} // R'_{28} \tag{B-46}$$

Copper losses distribution

$$P_{cu}^{A} = \frac{P_{cu,winding}}{N} \tag{B-47}$$

Core losses distribution

- Segment A

$$P_{core,winding} = \frac{P_{core}}{2}\frac{N \cdot \theta_1}{\pi} \tag{B-48a}$$

$$P_{core}^{A} = P_{core,winding} \cdot \frac{1}{N} \tag{B-48b}$$

- Segment B

$$P_{core}^{B} = \frac{P_{core}}{2}\frac{\theta_2}{\pi} \tag{B-49}$$

Capacitor modeling

The thermal models for the capacitor cooling are based on the empirical equations given in [68]. From these equations the difference between the surface temperature T_s and ambient temperature T_{air} is obtained. For component length L, width W and height H the heat transfer surfaces are defined as

$$A_{ver} = (W + L) \cdot 2 \cdot H \tag{B-50a}$$

$$A_{hor} = W \cdot L \tag{B-50b}$$

$$A_{rad} = A_{ver} + A_{hor} \tag{B-50c}$$

The characteristic $Rayleigh$ number Ra is defined as

$$Ra = Gr \cdot Pr \tag{B-51}$$

where Gr is the $Grashof$ number and Pr is the $Prandtl$ number for air at the specified ambient temperature.

- Free convection over the vertical surface

$$Gr = \frac{g \cdot l^3 \beta \cdot (T_s - T_{air})}{v^2} \tag{B-52}$$

$$\beta = 1/T_0 \tag{B-53}$$

$$Nu_{ver} = \{0.825 + 0.387 \cdot Ra^{1/6} \cdot f_1(Pr)\}^2 \tag{B-54}$$

$$f_1(Pr) = (1 + 0.671 \cdot Pr^{9/16})^{-8/27} \tag{B-55}$$

$$h_{c,ver} = \frac{Nu_{ver} \cdot \lambda_{air}}{H} \tag{B-56}$$

where β is the thermal expansion coefficient, $g = 9.81$ is the gravity coefficient and v is the kinematic viscosity of air at temperature T_{air}.

- Free convection over the top horizontal surface

$$Nu_{hor} = 0.766 \cdot (Ra \cdot f2)^{1/5} \tag{B-57}$$

$$h_{c,hor} = \frac{Nu_{hor} \cdot \lambda_{air}}{s} \tag{B-58}$$

$$s = \frac{W \cdot L}{2 \cdot (W + L)} \tag{B-59}$$

where s is the characteristic length.

- Radiation heat transfer

$$h_{rad} = \epsilon \cdot \sigma \cdot ((TK + T_s)^4 - (TK + T_{air})^4)/(T_s - T_{air}) \tag{B-60}$$

where $TK = 273^oC$, $\sigma = 5.67 \cdot 10^{-8}$ is the Stefan-Boltzmann constant and ϵ is the surface emissivity, considered $\epsilon = 0.8$ for the capacitor surface.

Appendix C

Component characteristics

Thermal domain components

Table C-1: Thermal-conducting materials

thickness [mm]	λ [W/m^{o}C]	Tmax [^{o}C]	Tmin [^{o}C]	ϵ_r
Sil-Pad-2000 [66]				
0.25	3.5	200	-60	4
Gap Pad A3000 [66]				
0.381	2.6	200	-60	7

Toroidal core

losses: $P = k \cdot f^{\alpha} \cdot B^{\beta}$, P in [mW/cm^3], f in [kHz], B in [kG]

Table C-2: Ferrite material 'J' core properties

Ferrite material 'J' core properties [75]				
Bsat [mT]	μ_r	Tcurie [^{o}C]	density [g/cm^3]	λ [W/m^{o}C]
430	5000	145	4.8 10^{-3}	2.9
Ferrite material 'J' loss parameters (@ 100^oC) [75]				
k	α	β		
0.245	1.39	2.5	at f<20 kHz	
0.00458	2.42	2.5	at f>=20 kHz	
Coating properties				
code	thickness [mm]	Tmax [^{o}C]	λ [W/m^{o}C]	
Z	1	200	1	

EMI load equivalent circuits

- Machine
  $R_s = 50\Omega$
  $L_s = 0.082$ mH
  $C_{wg} = 12$ nF
  $C_s = 1/10 \cdot C_g$

- Cable
  $R_c = 30\ \Omega/\text{m}$
  $L_c = 262 \cdot 10^{-9}$ H/m
  $C_{cg} = 278 \cdot 10^{-12}$ F/m

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