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High Time Resolution, Low-Noise, Power-Efficient, Charge-Sensitive Amplifier in 40 nm Technology

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Abstract – **Particle detection circuits are used for a wide range of applications from experimental physics to material testing and medical imaging. In the state-of-the-art systems, the trend is to design low-noise and low-power readout front-end electronics with a low detection error rate and small silicon area occupation. This paper presents the design of a high time resolution, low-noise, and power-efficient charge sensitive amplifier (CSA) in 40 nm CMOS technology. For every charge pulse of the detector, the CSA generates voltage signals with a peak amplitude of 30.6 mV, a rise time of 2.35 ns, and an equivalent noise charge (ENC) of 44e^- with 0.14 mW power consumption.**

Keywords – **charge sensitive amplifier (CSA); low-noise; power-efficient; high time resolution; readout front-end;**

I. Introduction

Modern imaging systems, such as scanning electron microscopes (SEMs), employ pixelated silicon PIN detectors to count the number of electrons backscattered from the specimen being bombarded by an electron beam [1]-[3]. The detector is coupled with multichannel front-end electronics to process the charge signals generated as a result of particle detection. High-resolution and high-speed scanning require the front-end electronics to process the weak detector charge signals in a very short time. Moreover, in the state-of-the-art systems, the trend is to design low-noise and low-power readout front-end electronics with a low detection error rate and low silicon area occupation.

To detect the weak and high event-rate charge signals, a high bandwidth low-noise preamplifier is often required, which is followed by a signal shaper and then a comparator to distinguish and count the signal pulses. The key, however, is to achieve a low detection error rate, which can be compromised by either noise or inter-symbol interference (ISI) [4]. The posterior refers to the pileup of the signals at the output of the preamplifier as a result of its limited bandwidth. As illustrated in Fig. 1, the aforementioned interplay results in an optimal bandwidth that balances the error rate between noise and ISI-induced errors [5].

In order to reach the required accuracy for event detection, the double-threshold technique was proposed in [4], [5]. It permits the analog components of the front-end electronics to be designed with reduced bandwidth, with the aim to reduce both power consumption and the integrated noise, while compensating for the induced pileup of the signals (ISI) due to the limited bandwidth at the output by adding the second threshold level to the discriminator; hence, a low error rate maintained. In addition, to reach a good time resolution for the landing event, a clock period of 2.5 ns is chosen, allowing an event rate up to 4×10^8 events/s [4].

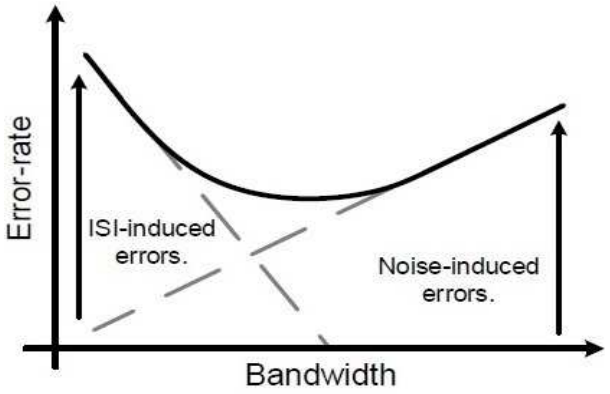

Fig. 1. Conceptual plot of the trade-off between bandwidth, noise, ISI, and the error rate.

In the reported solution, although the preamplifier, operating in transimpedance mode (TIA), was designed with a lower bandwidth, it was still the noisiest and most power-hungry block: the bottleneck of the readout front-end yet. Compatible with high event-rate charge signals, the TIA generates voltage signals with fast rising and falling edges; however, the stability and phase margin of the preamplifier must also be taken into account. Moreover, the TIA imposes second-order effects on the detection accuracy. This problem originates from the fact that the TIA voltage signal has a fast falling edge, and that the dynamic comparator might discriminate the TIA voltage signal at a lower amplitude point while the noise is constant; thus, as a result of discrimination with a lower SNR, the number of false counts increases [5].

Two solutions are proposed to address this issue and improve the performance of the double-threshold technique. The first is synchronizing the comparator clock signal with the peak of the TIA voltage signal; however, this solution is not practical as TIA voltage signals are generated randomly (following the random nature of the input charge signals) [5]. The other solution is redesigning the preamplifier to generate voltage signals with a slower falling edge, so that in every clock cycle, the dynamic comparator can discriminate them with a negligible drop of the SNR. For this purpose, the preamplifier should operate in charge-sensitive mode with a pole in low frequencies. By designing a lower bandwidth preamplifier, both the integrated noise and, consequently, the power consumption will shrink. However, the ISI-induced errors are more critical in this case as one signal may be counted multiple times.

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This paper presents the design of a high time resolution, low-noise, and power-efficient charge sensitive amplifier (CSA) in 40 nm CMOS technology. The shaping of the output signal of the CSA, required to eliminate the ISI-induced errors, will be discussed in a follow-up paper. In Section II we present the operation principle, noise model, and transfer function of generic front-end electronics. Section III reveals the most important aspects of the charge sensitive amplifier design. Section IV presents the post-layout simulation results. The paper ends with conclusions.

II. Front-end Electronics

A. Operation Principle

A simplified model of an analog readout front-end for semiconductor detectors, as shown in Fig. 2, has the following blocks: a preamplifier, a signal shaper amplifier, and a discriminator. The detector generates exponential decay current signals with an area equivalent to Q_{in} and a charge collection time τ_d as a result of particle detection. These current signals are collected and then converted into voltage signals by the preamplifier. Depending on the time constant of the feedback network ($\tau_F = R_F.C_F$), the preamplifier can operate either in charge sensitive ($\tau_F \gg t_p$) or transimpedance ($\tau_F \approx t_p$) modes, where t_p is the peaking time at the preamplifier output. The voltage signal after the preamplifier is then processed by a shaper amplifier which improves the signal-to-noise ratio (SNR) and shortens the time-width of the signal. Finally, the signal is converted from the analog to digital domain through a discriminator. The accuracy of the conversion depends on the SNR of the signal, the offset of the discriminator, and the accuracy of the threshold level.

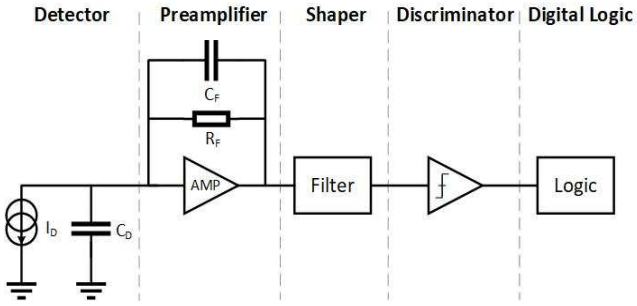

Fig. 2. Simplified block diagram of readout front-end electronics.

Regarding the low power consumption requirement, as noted in [4], the preamplifier can also take the role of the shaper. In other words, the poles in the preamplifier transfer function are used for shaping the preamplifier voltage signal in the time domain.

The low detection error rate requirement necessitates the preamplifier to operate with the maximum theoretical SNR, which can be attained by maximizing the voltage signal and minimizing the noise. Both are guaranteed once the preamplifier operates in charge sensitive mode ($\tau_F \gg t_p$) and has low bandwidth. Moreover, with respect to the detector charge collection time τ_d, to fully integrate the charge signal in the feedback capacitance, the preamplifier should have a time constant $\tau_F > \tau_d$ [6].

B. Noise

The major noise sources of front-end electronics can be modeled and categorized in two forms of series voltage contributions v_n and the parallel current contributions i_n, which can be expressed as [7]:

$$S_{V_n} = \frac{4KT\gamma_n}{g_m} + \frac{K_f}{C_{ox}WL} \cdot \frac{1}{f} = \alpha + \frac{A_f}{f} \quad (1)$$

$$S_{i_n} = \frac{4KT}{R_F} + 2qI_{leackage} = \beta \quad (2)$$

where K is the Boltzmann constant, T is the temperature in Kelvin, q is the electron charge, R_F is the feedback resistance, $I_{leackage}$ is the detector leakage current, K_f is the flicker noise coefficient, C_{ox} is the gate oxide capacitance per area, γ_n ranges from 1/2 (weak inversion) to 2/3 (strong inversion), and g_m, W and L are the transconductance and the dimensions of the preamplifier input transistor, respectively.

The noise power spectral density at the preamplifier output can be expressed as:

$$S_{V_{Preamp}} = \frac{\beta}{(2.\pi.f.C_F)^2} + \left(\alpha + \frac{A_f}{f}\right)\left(\frac{C_T + C_F}{C_F}\right)^2 \quad (3)$$

where $C_T = C_D + C_G$, C_D and C_G are the detector capacitance and gate capacitance of the preamplifier input transistor, respectively.

Assuming that the preamplifier is followed by a signal shaper with transfer function $H(s)$, the noise after the shaper block multiplies Eq. 3 by the square value of $H(s)$. By integrating the output noise in the frequency domain and dividing by the maximum value of $h(t)$, where $h(t) = L(H(s))^{-1}$, the noise of the front-end electronics, defined as the Equivalent Noise Charge (ENC), can be expressed as [7]:

$$ENC^2 = \frac{1}{C_F^2}\left(\beta \cdot t_s \cdot a_p + (C_D + C_G + C_F) \cdot \left(\frac{\alpha}{t_s} \cdot a_w + A_f \cdot a_f\right)\right) \quad (4)$$

where t_s is the shaper time constant, and a_p, a_w, and a_f are the noise coefficients related to the shaper transfer function $H(s)$.

It can be concluded from Eq. 4 that to improve the noise performance of the front-end electronics (i.e. to decrease the ENC), the shaper time constant t_s, the feedback resistance R_F, and the transconductance of the preamplifier input transistor g_m should be sufficiently increased for a given detector capacitance C_D and feedback capacitance C_F values.

C. Transfer Function

Figure 3 illustrates the transfer function of a preamplifier with two poles, which can be written as:

$$T_{CSA}(s) = \frac{R_F}{(1+s\tau_F)(1+s\tau_{CL})} \quad (5)$$

where $\tau_F = C_F R_F$ is the time constant of the first pole, which sets the discharge tail of the voltage signal in the time domain, and $\tau_{CL} = \frac{1}{GBW} \cdot \frac{C_F + C_D + C_G}{C_F}$ is the time constant of the

second pole, which sets the rise time of the voltage signal. The input charge Q_{in} induced by the moving charge carriers on the detector's electrodes appears as a voltage signal after the CSA. The shape of this voltage signal can be a function of the detector charge collection time τ_d. If τ_F is small compared with the duration of charge collection time in the detector (τ_d), then the voltage signal after the CSA has a shape nearly identical to that of the time dependence of the charge within the detector. If τ_F is much larger than the charge collection time τ_d, which is a more general case, the shape of the voltage signal after the CSA will mainly depend on the value of τ_F [7]. For an impulse input charge Q_{in}, the voltage signal after the CSA can be written in the time domain as:

$$V_{CSA}(t) = Q_{in} \cdot \frac{R_F}{\tau_F - \tau_{CL}} \left(e^{-\frac{t}{\tau_F}} - e^{-\frac{t}{\tau_{CL}}} \right) \quad (6)$$

which for $\tau_F \gg \tau_{CL}$ can be simplified as:

$$V_{CSA}(t) = Q_{in} \cdot \frac{1}{C_F} \left(e^{-\frac{t}{\tau_F}} \right) \quad (7)$$

In this regard, the CSA output voltage is inversely proportional to the feedback capacitance C_F. To achieve a sufficiently large voltage signal around 30 mV for a weak input charge signal of $Q_{in} = 1000\, e^-$, a feedback capacitance of $C_F = 5fF$ is chosen.

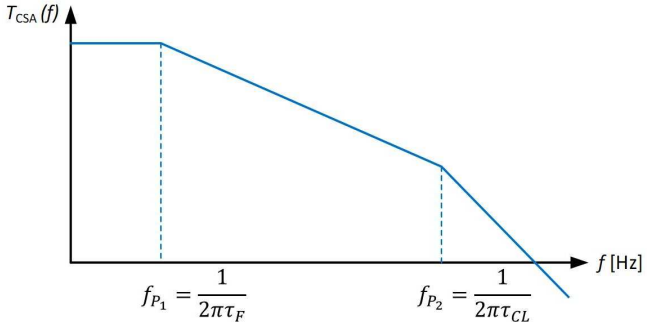

Fig. 3. Transfer function of a preamplifier with two poles.

The time constant of the second pole (τ_{CL}) is set according to the desired time resolution of the voltage signal. Compatible with the target discrimination clock period of 2.5 ns, the CSA voltage signal should have a peaking time of $t_p \leq 2.5\, ns$. This could be translated as a second pole beyond 400 MHz.

The time constant of the first pole (τ_F) is set according to the desired discharge tail of the analog voltage signal. To solve the issue of the second-order effects on the detection accuracy, the dynamic comparator must discriminate the CSA voltage signal with a negligible drop of the SNR in every clock cycle. While the noise is constant, the signal amplitude drops at the falling edge of the signal. In order to limit the signal drop to below 1%, the tail of the voltage signal must be 100 times larger than the discrimination period of 2.5 ns; hence, a discharge tail longer than 250 ns is needed which, in combination with a feedback capacitance C_F in the order of a few femtofarads, corresponds to a feedback resistance R_F in the order of a few megaohms.

There are several methods proposed for implementing a large feedback resistance R_F and a preamplifier in CSA mode. The Krummenacher network (Fig. 4) is widely used in photon counting front-end electronics [8], [9]. This network provides two feedback paths: a resistive path to implement an equivalent feedback resistance of $R_F \approx \frac{2}{g_{m1}}$ (assuming $g_{m1} = g_{m2}$) and then discharge the feedback capacitance C_F by a small constant current I_{Krum}, and an inductive path through M_3 and C_{Krum} to compensate the detector leakage current rather than it flowing into the feedback resistance R_F [8]. However, in applications in which the detector leakage current is negligible, the Krummenacher network might not be the best choice as its current noise contribution S_{i_n} is proportional to the bias current I_{Krum} while the shaping time is proportional to the $\frac{Q_{in}}{I_{Krum}}$. Hence, decreasing S_{i_n} results in a shaping time increment. Any variation in input charge Q_{in}, would directly change the shaping time as well [8], [9].

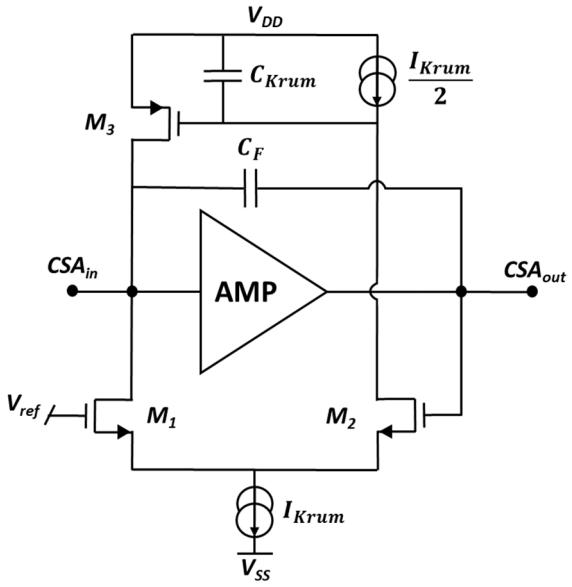

Fig. 4. Schematic of a CSA implemented by the Krummenacher network in the feedback.

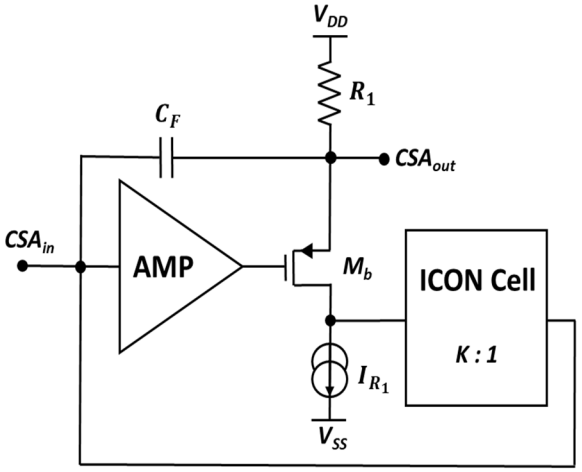

Fig. 5. Schematic of a CSA implemented by an ICON Cell in the feedback network.

To overcome the drawbacks of the Krummenacher network, the CSA can be implemented using a current conveyor, called an ICON Cell, in the feedback network as proposed in [10], [11] (Fig. 5). An ICON Cell provides a large resistance equivalent to $R_F = (K+1) \times R_1$ and a shaping time of $(K+1) \times R_1 \times C_F$ using a physical resistor of R_1, where K is the mirroring factor. In this network, the current noise contribution S_{i_n} is proportional to I_{out}, which is the bias current in the right branch of the current mirror inside the ICON cell (shown in Fig. 7). Hence, the shaping time is independent of the current noise contribution S_{i_n}. Details of the CSA with ICON Cell and simulation results are presented in the next sections.

III. Design of Charge Sensitive Amplifier

A. Core Amplifier

As a tradeoff between the low-noise on the one hand, and high gain and high input signal throughput on the other hand, a Folded Cascode architecture is used for the core amplifier (Fig. 6). Table 1 presents the transistors' dimensions and their drain currents.

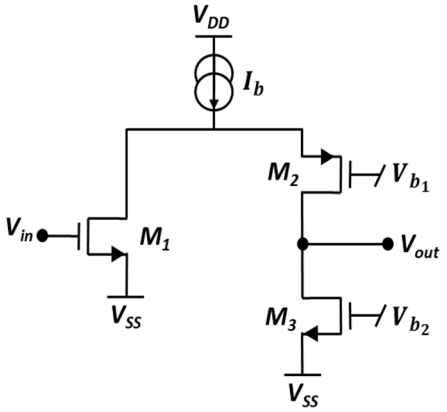

Fig. 6. Schematic of the Folded Cascode amplifier.

Table 1. Transistors' Dimensions and Their Drain Currents

	M_1	M_2	M_3
W [μm]	18	1.26	8.71
L [μm]	0.1	0.25	0.15
I_D [μA]	118	2	120

The DC gain of the core amplifier is calculated as:

$$G_{Amp} = g_{m1} \cdot R_{out} \tag{8}$$

where g_{m1} is the transconductance of the input transistor and R_{out} is the equivalent resistance seen from the output node. The DC gain can be increased by biasing the output branch with a small current ($I_{D2} = 2\ \mu A$) and the input device (a high threshold NMOS) in the subthreshold region with $I_{D1} = 118\ \mu A$. In this way, a transconductance of $g_{m1} = 1.5\ mS$ is achieved, which is mainly proportional to the drain current I_{D1} and shows a small dependence on the dimension of M_1.

To integrate the input charge in the feedback capacitance C_F (not shown in Fig. 6) with less than 10% charge loss, a $\frac{C_{in}}{C_D+C_G} > 10$ ratio must be guaranteed, where C_D is the detector capacitance, C_G is the gate capacitance of the preamplifier input transistor, and $C_{in} = C_F(1 + G_{Amp} \cdot \frac{C_F}{C_F+C_D+C_G})$ is the equivalent feedback capacitance seen from the input. Concerning the $C_F = 5fF$, $C_D = 50fF$, and $C_G = 9fF$, the DC gain of the amplifier should be $G_{Amp} > 40\ dB$. Moreover, concerning the aforementioned parameters, the requirement of setting the second pole of the CSA beyond $400\ MHz$ can be translated as a gain-bandwidth product (GBW) of larger than $4.8\ GHz$ for the core amplifier.

B. ICON Cell

A detailed schematic of the CSA with an ICON Cell is shown in Fig. 7. The resistor R_1 is implemented by biasing a transistor (M_5) in the triode region. In steady state, thanks to the feedback loop, since the current flowing into M_5 is equal to the current generated by the generator I_{R_1}, the current injected into the ICON Cell is zero, which makes the bias current of the ICON Cell independent of the resistor bias current I_{R_1}. Once the detector delivers charge into the input, the output voltage signal starts to rise. The output voltage is converted into current through the channel resistance of M_5, which then flows into the ICON Cell which is demagnified by the mirroring factor K. Finally, this demagnified current is forwarded back to the input node of the CSA and starts discharging the feedback capacitance C_F.

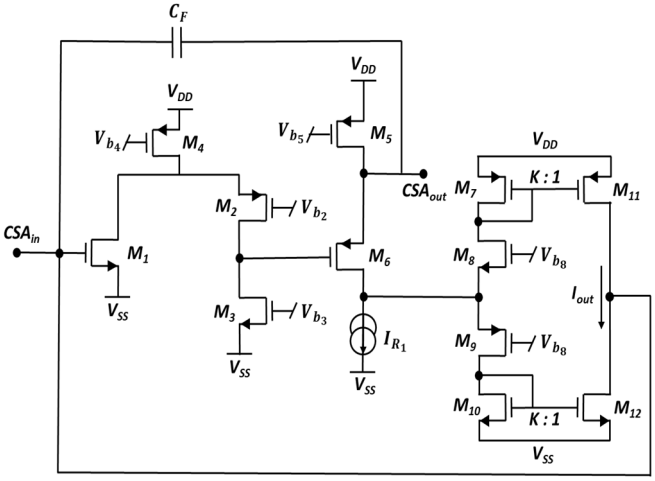

Fig. 7. Detailed schematic of the CSA with the ICON Cell.

A simple analysis of the circuit shown in Fig. 7 shows that V_{out} and I_{in} are related by the following equation:

$$\frac{V_{out}}{I_{in}} = \frac{KR_1}{(1+SC_FR_1(K+1))(1+s\tau_{CL})} \tag{9}$$

The dominant noise source in a CSA with an ICON Cell is the current noise contribution coming from the right branch of the mirror (I_{out}). In fact, thanks to the mirroring factor K, all the noise contributions present in the left branch of the mirror, generator I_{R_1}, and transistors M_5 and M_6 are nullified by a factor of K^2. Therefore, to keep the current

noise contribution small, the right branch of the ICON Cell is biased in the subthreshold region with an ultra-small current ($I_{out} = 230\ pA$). To achieve the required discharge tail for the voltage signal after the CSA and a sufficient demagnification factor for the noise sources, an ICON Cell with a mirror factor $K = 80$ is implemented.

IV. Simulation Results

The prototype of the CSA was designed in a TSMC 40 nm CMOS process. Figure 8 illustrates the layout mask view of the designed CSA, which occupies an area of 30 $\mu m \times$ 15 μm.

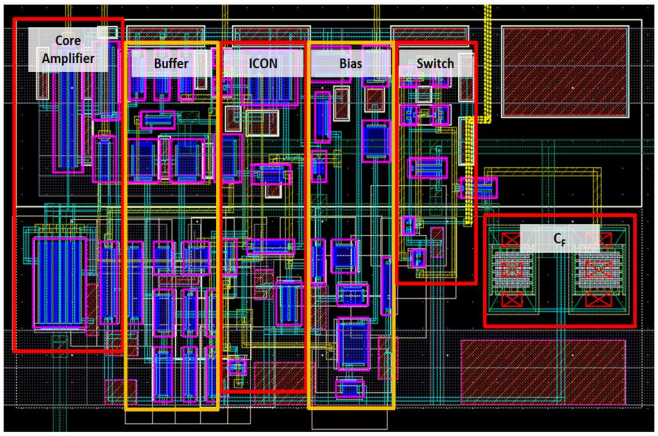

Fig. 8. Layout mask view of the designed CSA.

In the simulations and through this work, the PIN diode is modeled as a digitally controlled current source in parallel with a capacitance C_D. The current source should generate charge pulses with an area equivalent to $Q_{in} = 160\ aC$ ($1000\ e^-$) and a time width equal to the detector charge collection time $\tau_d = 1.8\ ns$. In this application, the τ_d is much smaller than the τ_F of the CSA; hence, as mentioned in Section II, the shape of the voltage signal after the CSA is irrelevant to the detector charge signal characteristics, but mainly depends on the value of τ_F. To observe the performance of the designed CSA under different conditions, two sets of test features are implemented in the CSA. By changing the feedback capacitance C_F value, the CSA can work in low gain ($C_F = 10\ fF$) or high gain ($C_F = 5\ fF$) mode, and by changing the equivalent feedback resistance R_F value, the CSA can work in slow ($R_1 = 133\ K\Omega$) or fast ($R_1 = 67\ K\Omega$) mode. Table 2 summarizes the post-layout simulation characteristics of the designed CSA for different values of feedback components and an ICON Cell with a mirroring factor of $K = 80$.

Table 2. Post-layout Simulation Characteristics of the CSA for Different Values of Feedback Components.

$C_F[fF]$	$R_1[K\Omega]$	t^*_{tail}[ns]	t_p[ns]	ENC[e^-]	SNR
5	67	133.8	2.1	43	23.2
	133	259.6	2.35	44	22.7
10	67	264.1	1.91	50	20.3
	133	579.6	1.94	52	19.2

**Discharge tail of the CSA voltage signal*

The optimum operating point of the CSA in terms of processing speed and SNR corresponds to $C_F = 5\ fF$ and $R_1 = 133\ K\Omega$, which in combination with $K = 80$ results in an equivalent feedback resistance of $R_F = 10.82\ M\Omega$, and a CSA with a bandwidth of 2.94 MHz. Figure 9 illustrates the simulated voltage signal after the CSA for the fast and slow modes with $C_F = 5\ fF$, while Fig. 10 illustrates the simulated voltage signal after the CSA for the low and high gain modes with $R_1 = 133\ K\Omega$.

Tables 3 and 4 contain the parameter spread for fast and slow operation modes with a feedback capacitance of $C_F = 5\ fF$ and $C_F = 10\ fF$ resulting from a Monte Carlo Analysis in 200 points, respectively. Table 5 summarizes the CSA performance characteristics designed in this work and compares them with other relevant works.

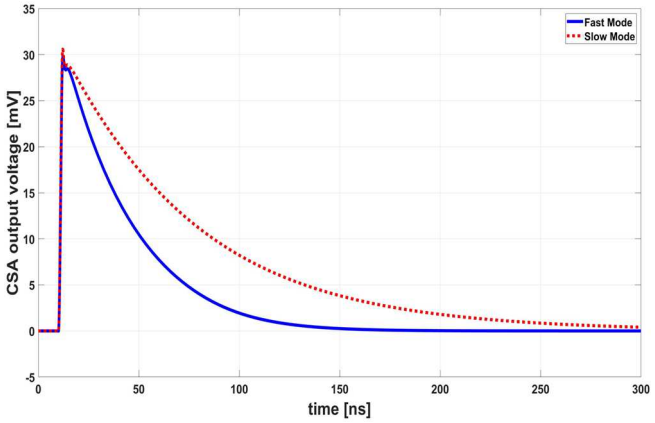

Fig. 9. Simulated CSA output voltage for the fast and slow modes with $C_F = 5\ fF$.

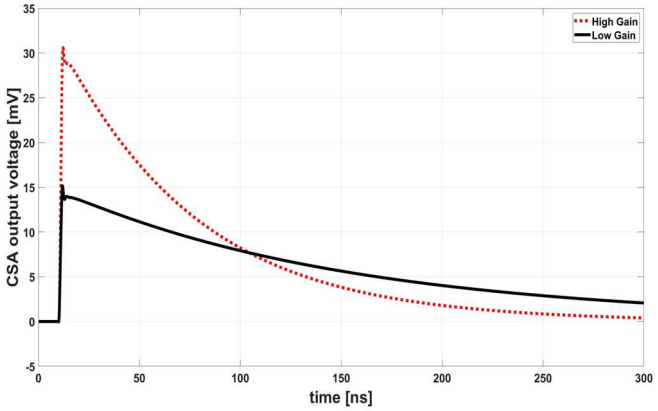

Fig. 10. Simulated CSA output voltage for the low and high gain modes with $R_1 = 133\ K\Omega$.

Table 3. Parameter Spread for Fast and Slow Operation Modes from a $C_F = 5\ fF$ - Monte Carlo Analysis

Parameters	Fast Mode		Slow Mode	
	μ	σ	μ	σ
$R_F\ [M\Omega]$	5.29	1.32	10.96	1.36
$t^*_{tail}\ [ns]$	135.6	32.3	261.6	44.6
$t_p\ [ns]$	2.24	0.31	2.43	0.29
$Signal_{max}\ [mV]$	29.5	0.5	30.8	0.7

**Discharge tail of the CSA voltage signal*

TABLE 4. PARAMETER SPREAD FOR FAST AND SLOW OPERATION MODES FROM A $C_F = 10\ fF$ - MONTE CARLO ANALYSIS

Parameters	Fast Mode		Slow Mode	
	μ	σ	μ	σ
$R_F\ [M\Omega]$	5.29	1.32	10.96	1.36
$t^*_{tail}\ [ns]$	268.8	31.6	584.2	43.8
$t_p\ [ns]$	2.08	0.3	2.15	0.27
$Signal_{max}\ [mV]$	14.86	0.52	15.07	0.66

**Discharge tail of the CSA voltage signal*

TABLE 5. COMPARING PERFORMANCE CHARACTERISTICS OF DESIGNED PREAMPLIFIER WITH OTHER RELEVANT WORKS

Preamplifier Mode	TIA [4]	CSA [6]	CSA [9]	CSA [This Work]
$IDR^*\ [Ke^-]$	3.1	7.3	-	6.5
$S_e^{**}[\mu V/e^-]$	14	43	11.4	30
$t_p\ [ns]$	4.3	3.4	100	2.35
$ENC\ [e^-]$	174	118	144	44
SNR	5.7	18.6	17.3	22.7
$Power\ [mW]$	1.34	0.021	0.016	0.14

**Input Dynamic Range*
***Sensitivity of output to a single electron*

Based on the aforementioned points, thanks to lower bandwidth, the CSA guarantees the charge-to-voltage conversion with a larger SNR, less power consumption, and a faster peaking time at the preamplifier output with respect to the TIA designed and qualified in [4], [5]. Although, due to the lower bandwidth, the ISI-induced errors would be more critical with the designed CSA, qualification tests in [5] indicate that optimizing the comparator threshold levels can help compensate the extra ISI-induced error. Moreover, a periodic discharge of feedback capacitance C_F concerning the input dynamic range of the CSA would be a backup solution, which will be studied and qualified in a follow-up publication.

V. CONCLUSION

This paper presented the design and post-layout simulation results of a high time resolution, low-noise, and power-efficient charge sensitive amplifier (CSA) in 40 nm CMOS technology. The operation principle, noise model, and transfer function of a generic readout front-end were reviewed. To attain a sufficiently low bandwidth, two popular methods for implementing a large time constant in the feedback network of a preamplifier were reviewed and compared. The method implemented employs an ICON Cell, with feedback components of $C_F = 5\ fF$ and $R_1 = 133\ K\Omega$. For every charge pulse of the detector of about $1000\ e^-$, the CSA generates voltage signals with a peak amplitude of $30.6\ mV$, a rise time of $2.35\ ns$, an ENC of $44e^-$, and an SNR of 22.7 with $0.14\ mW$ of power consumption and an area occupation of $30\ \mu m \times 15\ \mu m$.

The presented solution is intended for accurate detection of the impinging moment of charged particles on a detector surface. To accurately detect the arrival time of high rate charged particles, a follow-up work is in progress, focused on the additional functional blocks needed after the CSA, to eliminate the tail of the CSA output signal.

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