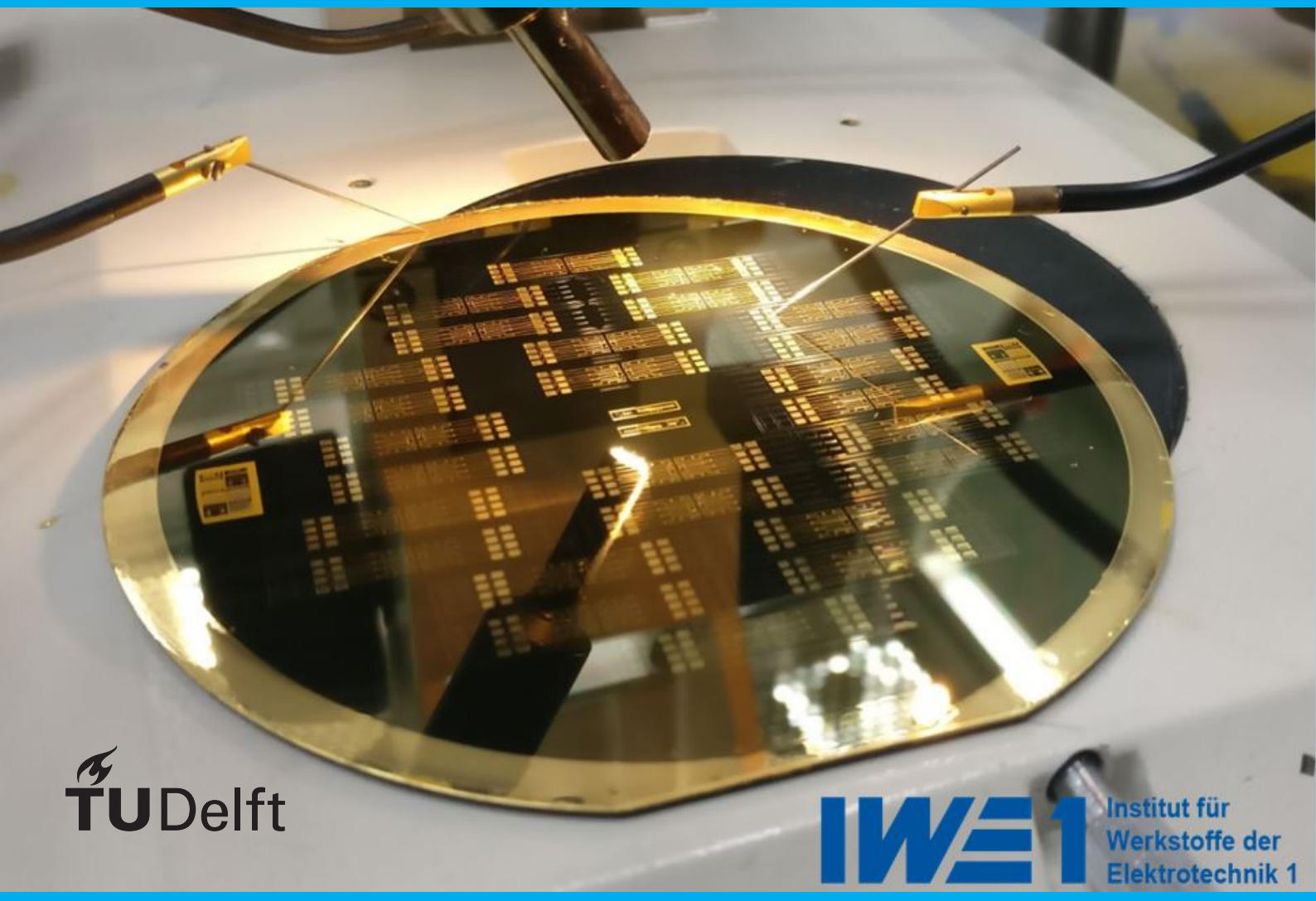
OPTOEPIRET

Development of a flexible epiretinal implant dummy with through-connections in the polyimide substrate

T.M. de Rijk



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OPTOEPIRET

Development of a flexible epiretinal implant dummy with through-connections in the polyimide substrate

by

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Abstract

Milions of people suffer from retinal diseases worlwide. Retinal diseases can either be cured or treated. Retinal implants try to do the latter and aim to restore, partially, the vision in visually impaired people. This research thesis introduces a flexible implant with through-connections and a corresponding thinned silicon dummy chip that, when bonded together, could function as a base for a retinal implant. The project, named OPTOEPIRET, manufactures such a two-part epiretinal implant, which will be completely implanted inside the human eye.

The silicon chip has to be thinned in order to meet the flexibility properties needed due to the eye curvature. Different methods are discussed in this thesis. Thinning the complete wafer to 40 μm and polishing the back surface before the chips are isolated yielded the best results.
Eleven different versions of the polyimide substrate were fabricated. Ensuring the correct adhesion agents are used for holding the gold pads into their corresponding polyimide holes was found to be critical. As well as ensuring a good connection between the gold pads and their corresponding paths.

The two parts are flip-chip bonded together and stress tested after the space between the two parts is filled with an underfill to spread the possible stress. The DC resistance was measured during bending of the dummy implant. Results showed the through-connections are able to withstand the bending stresses and forces during implantation into the human eye.

Preface

This thesis concludes the Master Graduation Project as a part of the Biomedical Engineering Master at the TU Delft. The project is part of the two year curriculum ME-BME and has to be successfully finished before on can finish the master program.

A proposal was done by prof.dr. P.J. French from the Technical University Delft in association with the university RWTH Aachen. This work consisted of manufacturing a flexible substrate with through-connections that could be implemented in retinal implants. This proposal was modified into a research project, part of the OPTOEPIRET project. Before this master thesis, a 6 month internship at the RWTH Uniklinik enabled for a useful insight in how retinal diseases are treated and newly investigated techniques. During the time of this master research project, a lot of technical experience was gained. Designing a multi-layer retinal dummy implant in AutoCAD, fabricating the implant in the cleanroom and testing the through-connections and flexibility properties all contributed to a successful thesis project with much gained valuable knowledge and skills.

I want to express my gratitude to Prof. Dr. rer. nat. W. Mokwa and Prof.dr. P.J. French for providing me the possibility to take part in this research project and being able to propose my research with an article and poster at 22th International Student Conference on Electrical Engineering in Prague on May 10. Furthermore, I would like to thank Dipl.-Phys. F. Waschkowski for the close supervision and day to day contact during this project. Special thanks goes out to D. Breuer for helping to manufacture the retinal dummy implants and assisting in solving multiple difficulties during this process. Another thanks goes to Dipl.-Ing. R. Fischer for all the help in the laboratory to explain and set up all the equipment needed to successfully bond the two-part implant together and test it. All persons, including the ones not specifically mentioned, gave insight and extra motivation to successfully complete this project.

T.M. de Rijk
Delft, May 2018

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1 Introduction

Retinal implants are able to restore part of the lost vision in blind people, with already achieving some great results. However, the stimulating area of the implants is most often very small, resulting in a narrow field of vision. The implants consist most often out of an intracellular and extracellular part, making the total device unnatural and impractical to wear. To improve on those two aspects, the OPTOEPIRET project aims to fabricate a retinal implant that is completely implanted into the human eye with no cables crossing the eye's wall. CMOS sensors will be located on the implant, hence no external camera is needed.

The research goal of this project is to fabricate a retinal implant dummy with through-connections in the polyimide substrate that is flexible enough for implantation in the human eye.
This project is part of the OPTOEPIRET project at IWE1 RWTH Aachen.

By integrating the flexible substrate with through-connections, the implant dimensions can be significantly reduced. The substrate layers can now be stacked on top of each other, instead of placed side by side and increasing the area of the chip. The implant will consist out of two parts: the dummy chip and the polyimide substrate substrate with gold through-connections. The dummy chip represents a basic version of the future chip that will be used for the implants logic, whereas the substrate's function is to guide the wires from the chip to the stimulating electrodes that are in contact with the retina. The necessary power will be transmitted via a wireless connection but will not be a part of this master thesis.
The process to manufacture polyimide substrates is already known at the RWTH IWE-1 Aachen, and the same procedure will be implemented for this project. However, the multiple complex layers of materials and the through-connections can become a challenging process. The thinning process of the silicon dummy chips to its final thickness, while ensuring a certain amount of mechanical flexibility, will be the second key part in this project. The total implant will have to be able to withstand the bending forces of implantation and the curvature of the human eye.

The silicon dummy chip will feature gold electrodes and paths, bonded to the polyimide substrate. The through-connections of the substrate enable the connection between the stimulating electrodes and chip connections. The first Chapters will describe the anatomy of the eyes and the already available implants. Chapter 3 discusses the advantages and disadvantages of the currently available implants. The next Chapter gives details in the design choices and the chosen layouts. The production of the chips (Chapter 5) and substrates (8) are executed in parallel. After both separate parts are finished, Chapter 10 continues with both parts and discusses the bonding process. After this bonding step, the implants connections are tested (via resistance measurements). The experimental setup and results are shown in Chapter 12. The thesis finishes with a conclusion and future recommendations in Chapters 13 and 14.

2

Background: Eye anatomy and diseases

2.1. Anatomy

The human eye is slightly asymmetrical and it grows gradually until it reaches a diameter of roughly 25 millimeters [18]. The anterior side consists out of the iris, cornea, pupil and the sclera. The incoming light will travel trough the pupil and is reflected by the lens and hits the retina. The space between the lens and the retina is occupied by a clear gel-like substance called vitreous humor [42]. A cross-section is given in Figure 2.1. This figure additionally displays a cross-section of a mouse eye. The difference in lens size can be noticed immediately, this is because the mouse eye needs a far greater refraction of light than in our eyes. The mouse eye is relevant for this research study because the eye is very similar as to humans and often used for eye research studies, as will be discussed more in the upcoming section.

The rods and cones are also displayed in the above mentioned figure. With retinal diseases, a degeneration in the photoreceptors (layers OS, IS, and ONL in Figure 2.1) occurs [20]. The retinal implants try to take over the function of these lost layers.

To further improve the authors knowledge of the human's eye physiology, he was granted access to the Operating Rooms in the Aachen University Hospital. I witnessed all kinds of eye surgeries. A few examples are: retinal detachments, cornea transplantation and cataract operations. I gained a great deal of useful practical knowledge (instead of only theoretical) during this month of how delicate the human eye is and how exactly all the layers work and what their function are.

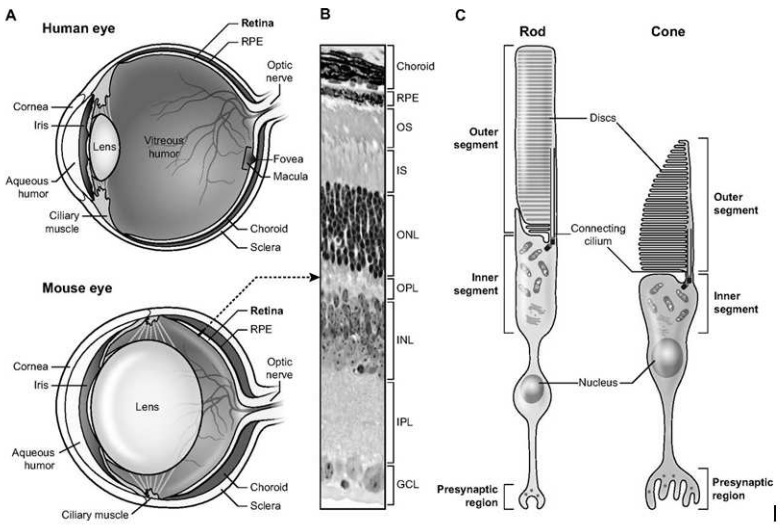


Figure 2.1: Cross-section of the human eye [45].

Mouse eye An implant is not the only aspect that is being researched in restoring vision in blind people. There are also numerous possibilities to counteract the effects on a molecular level, to investigate what genes cause retinal degeneration and try to counter effect these faults.
Mice eyes are physiologically very similar to human eyes. Therefore, mice are extensively used in retinal disease research groups. To try and understand what certain genes cause Retinal diseases like Retinitis Pigmentosa (RP), retinal cells of mice are isolated and investigated.
A mouse model for RP was created and named rd10 mouse [14]. During the lifetime of these mice they develop the same characteristic effects of RP in humans. The degeneration of photoreceptors slowly occurs during the mouse's development. Other research is still ongoing to create mice where the photoreceptor layer can be damaged by UV radiation, also mimicking the effects of RP. A possible advantage for this technique is that the need for expensive mice (and rabbits in next studies) becomes obsolete.

Rabbit eye The implants are often first implanted in rabbit eyes before into human eyes. Rabbits have larger eyes than mice, wherefore the surgeon can practice and familiarise himself with the implantation of a newly developed retinal implant. The surgeon can also rate the difficulty and feasibility of the surgery. This is useful for determining if implantation into human eyes could be possible. The VLARS structure [48] (from RWTH Aachen), which can be used to stimulate and detecting retina activity, was also implanted into rabbit eyes (in the Uniklinik, Aachen) and the surgery was rated complex but feasible.

2.2. Retinal diseases

The World Health Organization estimates that 285 million people were visually impaired around the world in 2010 [35]. Although the number of blindness cases has been dropping the last years, it is estimated that up to 80% of visual impairments are preventable or treatable (including cateract) [35].
Due to the diabetes incidence increase and ageing population, the two most frequent blindness causes are Diabetic retinopathy (DR) and Age-Related Macular degeneration (AMD). Another often cause is the already mentioned Retinitis Pigmentosa (RP).
The last retinal disease is discussed and relevant for this thesis work. RP disease is the loss of the photoreceptor layer, the layer that the retinal implant will take over. AMD is also briefly mentioned because of the studies performed at the RWTH Uniklinik in Aachen during my internship. These studies focus more on the cells behavior and finding a method to regenerate certain cells.

2.2.1. Retinitis Pigmentosa

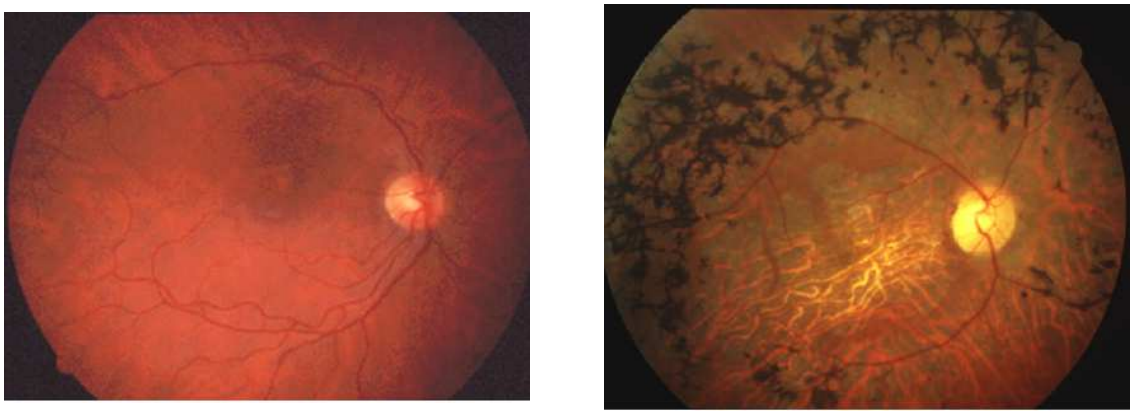
Retinitis Pigmentosa is a term given to a set of hereditary retinal disease that feature the degeneration of rod and cone photoreceptors. About 1 in 4000 persons are suffering from this genetic disease worldwide [17]. There are many known mutations and disease-causing genes [9]. The harmful changes can occur because more than 50 genes cannot produce the required protein for the photoreceptor cells, limiting the cell function [31]. Normally, the photoreceptor cells absorb the incoming light and convert it to electrical signals. After passing through several other layers this signal is transported from the optic nerve to the brain. The photoreceptor layer consists out of two layers: the rods and cones. The rods lie in the outer region of the retina and allow for seeing in dark or dim lighting. The cones are mostly located around the central part of the retina (macula), and allows us to perceive detail and color.

Symptoms The first symptom often is night-blindness. This is because the disease affects the rods earlier than the cones, which diminishes the ability to see in dark light. Eventually the cone degeneration follows, and the patients lose more of their visual field, ending in tunnel vision. Daily tasks become more and more difficult to perform. Even recognising faces becomes increasingly difficult [31]. Figure 2.2 shows how the degenerative disease looks like. The left figure shows a healthy eye. The right image shows the effects of the RP disease, the retina is completely disturbed and altered due to the retinal disease. The effects of RP are depicted in Figure 2.3

Inheritance RP can be inherited in one of three known ways [31] [38]:

1. Autosomal recessive Inheritance; it takes two copies of the mutant gene to give rise to the disorder.

2. Autosomal dominant Inheritance; it only takes one copy to bring the disorder. In this case, if one parent has a dominant gene, the child will have a 50% chance of inheriting the mutation.



(a) Healthy retina

(b) Degenerated retina

Figure 2.2: Effects of Retinitis Pigmentosa [46]

Figure 2.3: Effects of retinal degeneration. Left: Normal eye-sight. Middle: Central vision loss in macular degeneration. Right: Peripheral vision loss in Retinitis Pigmentosa [50].

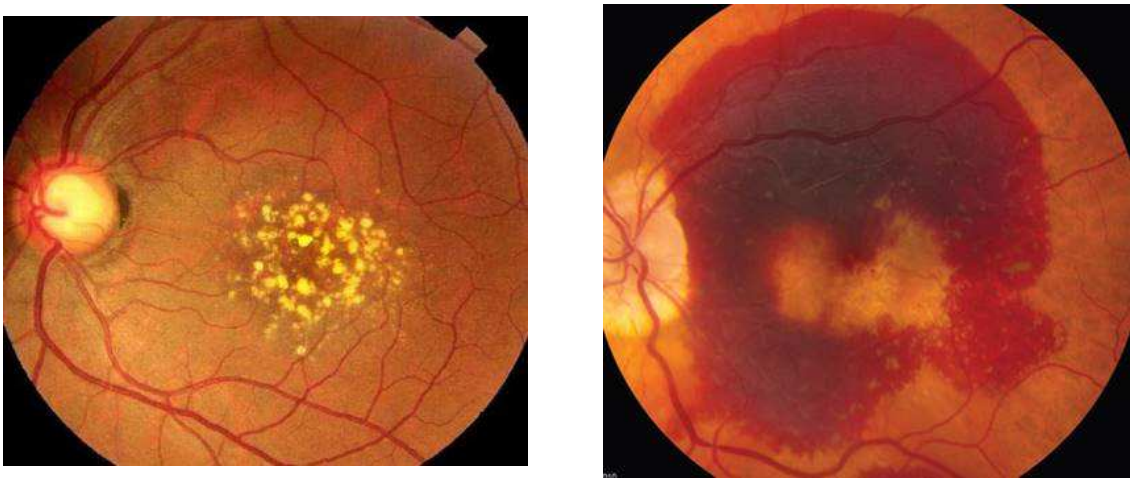
3. X-linked Inheritance; on one of the X chromosomes of the mother the mutated gene is carried and passed to their offspring. The chance that the offspring will have the disorder is 1 in 2.

Current treatments There is no known cure for RP. However there are a number of services and devices available to help people with vision loss. Such devices are, for example, text to speech software, portable lighting devices, and closed circuit televisions with a camera that can adjust the text size [31].
An NEI-sponsored clinical trial found that a daily dose of vitamin A palpitate could slow down the progression of the disorder [31]. However, other real treatments are yet to become available. A complete list of the NEI clinical trials can be found in reference [15]. Stem cell transplantation for RP patients, and gene identification of the RP disease are some of the latest completed trials.
Instead of only focusing on the genetics to find a treatment, research is also performed to investigate and improve retinal implants for visually impaired people. This prosthetic device takes over the function of the affected photoreceptors, and enables the patient to regain some of his/hers vision. Unfortunately, the devices are far from perfect and are only able to restore a small percentage of vision.

2.2.2. Age-related Macular Degeneration

Age-related macular degeneration is an eye condition that leads to vision loss. This mostly occurs among people around the age of 50 or older. AMD itself does not lead to complete blindness because the peripheral vision stays intact [32]. However, it will cause significant reductions in the quality of life. AMD causes damage to the macula that is located at the center of the eye. This small location is key for central vision (due to the high density of cones), and is important for seeing objects clearly. Abilities such as driving, reading a book or even recognising faces, will be affected by this disease [32].
AMD presents itself in two forms: non-neovascular (dry AMD) and neovascular (wet AMD) [34]. The dry form of AMD is most common to people, and is caused by aging and thinning of the tissues on the macula [6].
Dry AMD usually starts with so-called drusen that are formed under the retina. These yellowish pieces of fatty protein can cause the macula to stop working properly (See Figure 2.4).
As the usually harmless drusen grow further, more harmful atrophic areas could arise (wet AMD). When the

drusen's borders are sharp, it is termed to be a geographic atrophy (GA) [32]. In dry AMD, abnormal blood vessels grow beneath the retina. Swelling and damage of the macula can occur because these vessels can start leaking blood. This process is called *choroidal neovascularization (CNV)* [32]. When drusen form, the Retinal Pigment Epithelium (RPE) cells start dying. Next, an imbalance of angiogenic and anti-angiogenic factors cause an increase in vessel growth in the retina [4].



(a) Dry form AMD

(b) Wet form AMD

Figure 2.4: Effects of AMD. The yellowish drusen (left) can be clearly seen. The right figure shows the leaking blood vessels [33].

Current methods against AMD Currently there is no cure [16], but there are several treatments that can delay the progress of the disease. The most commonly used method is monthly injections of a so-called anti-VEGF [5]. During an injury or to bypass blocked blood vessels, normal VEGF creates new blood vessels. However, too much VEGF in the eye can cause the development of unwanted blood vessels. These additional blood vessels are more sensitive to breaking or bleeding, resulting in possible retina damage [16].
By injecting the patient regularly with anti-VEGF, the choroidal neovascularisation can be prevented or slowed down. Unfortunately, these injections mean that the patient has to travel to the hospital on a regular basis. In most cases this is impractical and takes a lot of time (for the patient, as well as for direct family members and friends).

TargetAMD, new approach for treating AMD TargetAMD [4] aims to improve current treatments. The project partners are developing a non-viral gene therapeutic approach for the treatment of executive AMD. This is done by transplanting genetically modified autologous pigment epithelial cells (IPE or RPE cells) that continuously secrete anti-angiogenic PEDF (pigment epithelium-derived factor) [5] [3]. PEDF is a natural antagonist of VEGF, that inhibits the growth of new blood vessels. The introduction of the modified pigment epithelial cells causes an over-expression of PEDF, resulting in a re-balance of the protein concentrations VEGF and PEDF [3]. Hence with TargetAMD, the patient does not need monthly injections into the eye, to keep the protein levels balanced.

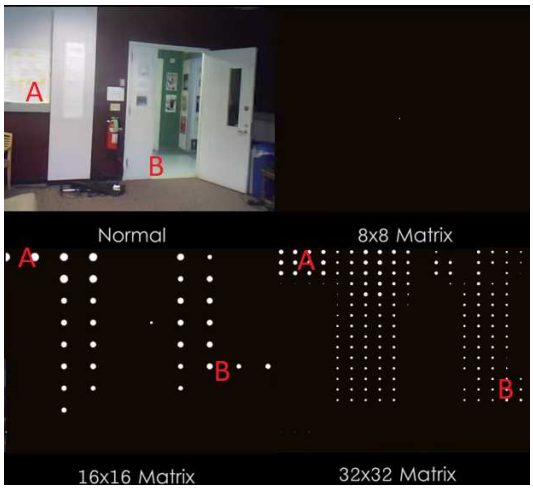
3

Background: Existing implants

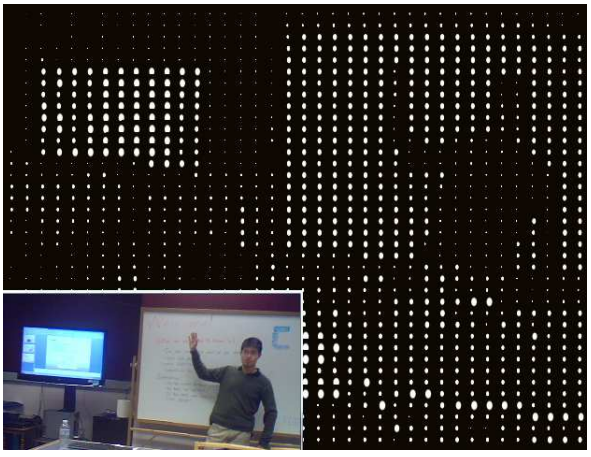
In the year 1968, the first electrode array was implanted into the retina of a human being. This study by G.S. Brindley and W.S. Lewin [7] implanted 80 passive extracranial radio receivers. By giving the appropriate radio signals, the patient could experience sensations of light in the left half of the visual field. Although this was a very small spot of white light, the first visual sensations of light by a retinal implant were a success.

Figure 3.1 give the reader a general idea of what it will look like for patients when wearing a retinal device. The small number of pixels that can be integrated is a limiting factor. Determining more complex shapes like a human or doorways are hard to detect with a low number electrodes. Larger stimulating areas with higher electrode numbers are necessary. However, very basic shapes from nearby with high intensity differences can still be detected.

There are multiple research teams and companies over the world trying the envoke visual sensations in visual impaired people by stimulating the retina. Two methods are researched intensively and already show promising results: subretinal and epiretinal implants. Figure 3.2 shows a schematic representation of the human eye with the two possible implant locations. The epiretinal implant lies on the retina, in contrast to the subretinal implant that is implanted deeper in the retinal layers. Appendix A shows a more detailed image of all the retinal layers and the exact locations of where the retinal implants would be implanted.



(a) Different amount of stimulating electrodes while looking at the same shape (a doorway). 8x8 matrix does not yield any information. The general shapes become visible in the larger matrices.



(b) With a high number of stimulating electrodes, more complex shapes like a person standing in front of a white background can be detected.

Figure 3.1: Showing the visual field with different amounts of pixels [49].

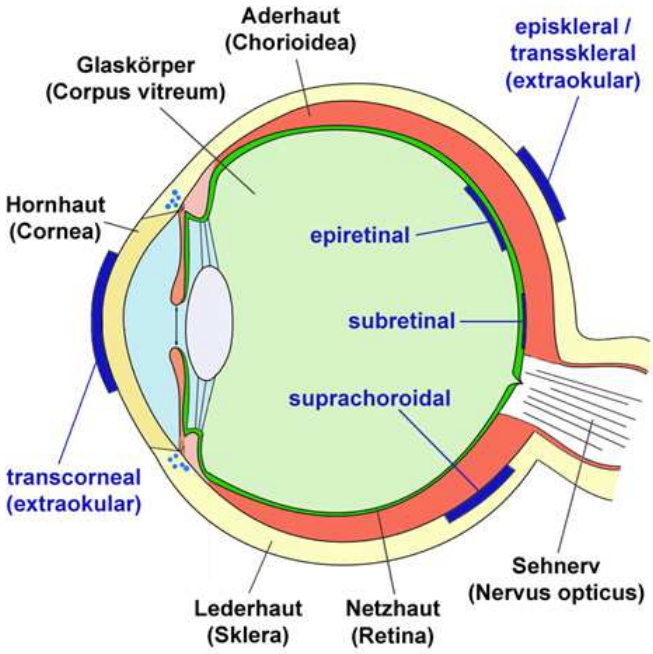


Figure 3.2: Sagittal view epiretinal and subretinal implant locations [46].

3.1. Subretinal implants

A subretinal device is implanted between the pigment epithelial layer and the outer layer of the retina [52]. Those layers contain the degenerated photoreceptors due to, for example, RP. In case a subretinal device is implanted, the light-sensitive microphotodiodes and microelectrodes are placed in this region to take over this function.

The light falls on the photodiodes and is transported to the electrodes, resulting in stimulation of retinal sensory neurons [52]. Figure 3.3 shows the layers of the human eye. The photoreceptor layer and the pigmented epithelium (most right) are clearly visible. The device is implanted between the two most right layers in Figure 3.3.

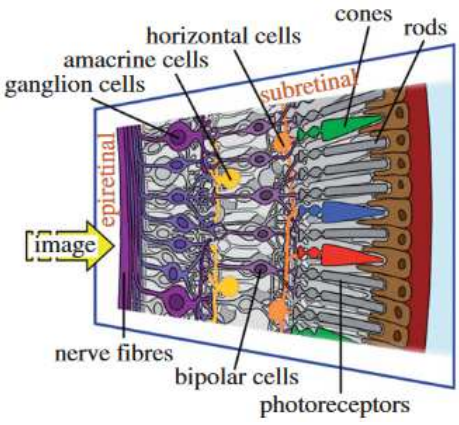


Figure 3.3: Cross-section of the retina layers [41].

Prosthesis integrated with photodiodes are also known as photovoltaic retinal prosthesis. The photodiodes photovoltaically convert the light pulses into bi-phasic currents that stimulates the nearby retinal neurons [47]. The light has to travel through the silicon implant. So the device has to be thick enough to absorb the incoming light, but still thin enough for subretinal implantation. A study from Wang, Lele, et al. in 2012 implemented a thickness of 30 µm. This thickness was chosen so that the implant can absorb roughly 70 %

of the incident light. A theory presented in the same study proposed that subretinal stimulation would result in more natural spiking patterns in response to pulsed stimulation than the direct activation of ganglion cells in the epiretinal approach [47].
The 1500 active microphotodiodes from ALpha IMS [47] [29] generates an array of 38 by 40 light-intensity-dependent pixels on the retina [41]. Although with a small stimulation area (visual angle 15° with 288 µm on the retina, Snellen visual acuity of 20/546 [41]), the subjects were still able to recognise and locate bright objects on a dark background (for example a fork and knife on a table) [29]. Figure 3.4 shows the Alpha IMS implanted into a patient. The subdermal coil and cable can be clearly seen. The right part of the figure shows the test results for visual acuity tests between the device turned on and off. A great improvement in the number of number of correctly identified objects is seen with the Alpha IMS system on (for both the standard geometric forms, top right, and the table setting forms, shown in the bottom right).

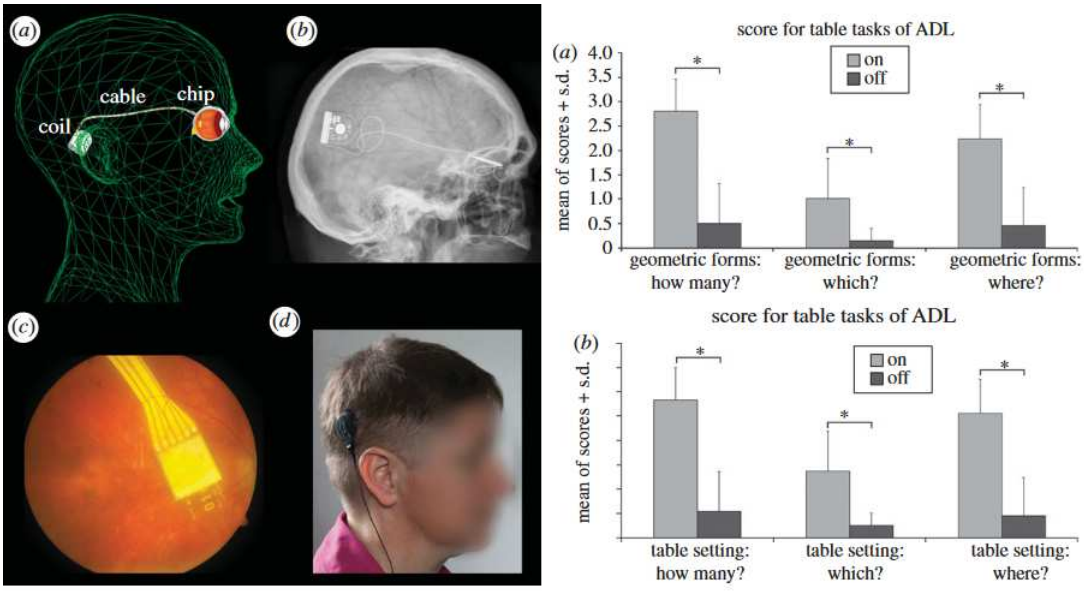


Figure 3.4: The alpha-IMS subretinal implant with the subdermal coil (a,b) [41].

3.2. Epiretinal implants

Currently epiretinal implants almost always consists of an extraocular and an intraoculur part [28]. A flexible structure with the stimulating electrodes is fixed onto the retina. This structure is most often anchored to the retina using a so-called retinal tack [1]. The main difference between an epiretinal and subretinal implant is that epiretinal implants lie on the retina, and are not implanted inside the retina layers.
The extraocular part captures the scene with a camera (CMOS sensor) often integrated in glasses, an artificial neural net that imitates the function of different ganglion layers of the retina (encoder), and a transmitter [28]. There are multiple epiretinal implants. A few (relevant) implants are discussed below.

3.2.1. EPI-RET-3 implant

The EPI-RET-3 was the first completely wireless retinal prosthesis implanted in humans [23] and was also manufactured in Aachen, Germany. No cable connection is crossing the eye's wall, minimising the risk of infection. Figure 3.5 shows a schematic representation of how the device will be implanted. In contrast to the Alpha IMS implant, no cable is crossing the eye's wall.
This prosthesis stimulates the retinal ganglion cells directly with 25 micro-electrodes. These electrodes are three-dimensional with a diameter of 100 µm and a height of 25 µm. The gold electrodes were coated with iridium oxide to achieve a large charge-delivery-capacitance up to $95 mC/cm^2$ (after electrochemical activation).
These structures enabled a close contact to the retinal ganglion cells, and permitted the sensitivity thresholds to be lower (on average $15 \mu C/cm^2$ [29]) than other found studies at that time ($73.2 mC/cm^2$ and $7.8 mC/cm^2$).
The entire system works as follows [29] [23] [22]:

- An external CMOS sensor takes an image of the environment.
- This image is processed by a digital signal processor (the so-called retina encoder).
- Data and energy are transferred via RF coupling to the implant inside the eye.
- Data and energy signals are separated by a receiver chip.
- The stimulation signals are send to the stimulation chip which generates the bipolar current pulses. These pulses stimulate the remaining intact ganglion cells of the retina.
- As mentioned earlier, because of the three-dimensional micro electrodes, the stimulation thresholds are lowered, hence a greater stimulation efficiency is reached.

The implant has to be biocompatible and still function after a period of 28 days (the length of the trial). Materials already known to be compatible are therefore used, and Parylene was used to encapsulate the implant to avoid infiltration of hazards materials that could damage the implant. The wireless power supply had to overcome a maximum distance of 25 mm.
Six subjects implanted with the device were legally blind for at least 2-5 years. All patients reported visual sensations to the applied stimulation's. Patients reported to see dots, lines, and arcs (depending on the stimulation). Figure 3.6 shows the implanted EPIRET-3 device seen from the outside and inside of the patients eye. The microcoil for the wireless energy is well shown.

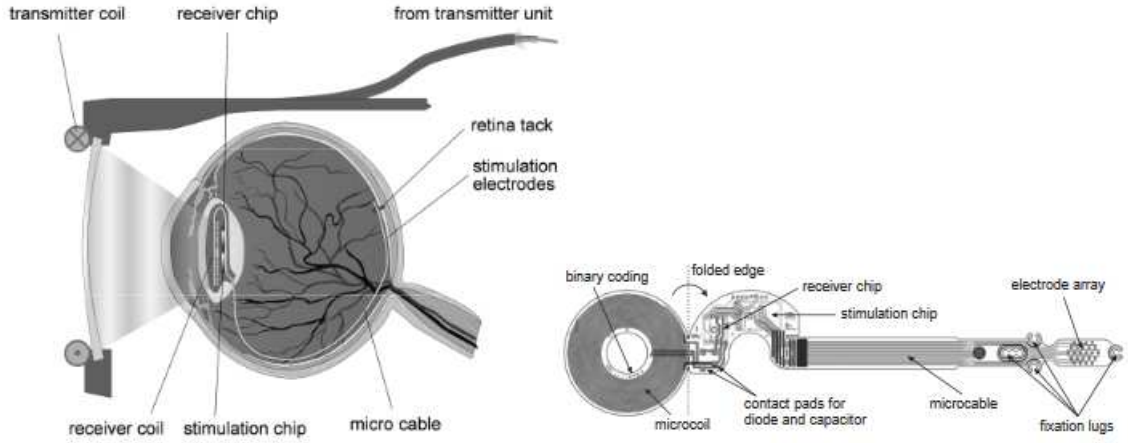
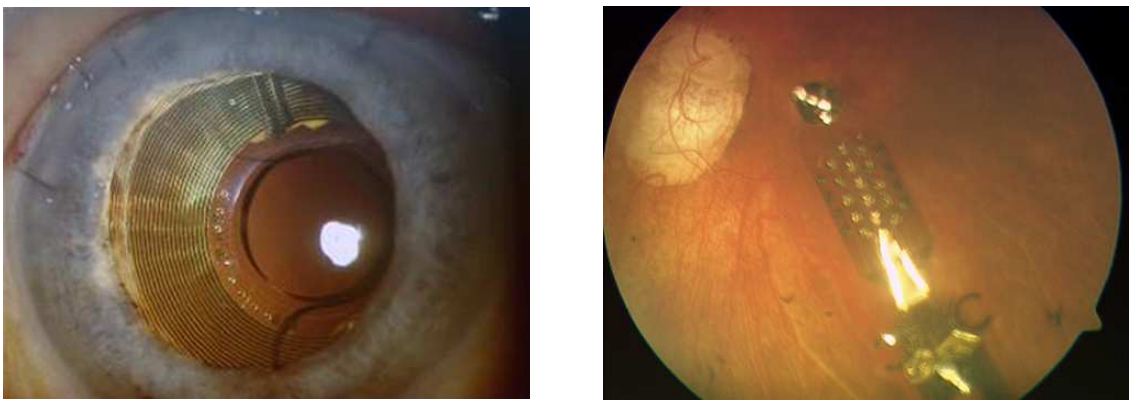


Figure 3.5: Schematic view of the EPIRET-3 system [30].



(a) Exterior view of EPIRET implant on the retina.

(b) View onto the retina.

Figure 3.6: Exterior and interior view of the implanted EPIRET-3 [46].

3.2.2. ARGUS I + II implant

The Argus II epiretinal prosthesis has been developed to provide partial restoration of vision to subjects blinded from outer retinal degenerative disease [1]. The Argus II has an approved regulatory CE mark from Europe and FDA approval [12]. The system consists of the following parts: 60 electrodes that can stimulate, an inductive coil link used to transmit the data and for power, a small external processing unit, and an external camera mounted on glasses. The electrode array is connected to the electronics case by a metalized polymer cable that penetrates the sclera [1] (Depicted in Figure 3.7). The damaged photoreceptors are bypassed and the inner nerve retinal ganglion layer is directly stimulated [12].

It is paramount that the electrode array is positioned as best as possible against the macula. Ahuja, A. K., et al. [1] showed a significant correlation between electrical threshold and electrode-retina distance. 90.3% of the electrodes that were in contact with the macula elicited percepts at charge densities below $1 mC/cm^2$. The average distance between the electrodes-retina was 179.6 ± 6.5 µm. The maximum achievable stimulated visual field with the Argus II device is 20°.

In 2013 a study from Da Cruz, Lyndon, et al. [8] performed a study where twenty-eight subjects with RP were given the Argus II system. The subjects had to identify certain letters, and several two-, three- and four-letter words. With the system turned on, the mean of the correctly identified letters was 72% (SD = 24.6%). In contrast to when the system was off (17.7% correct), a significant improvement.

Different groups of letters and small words were tested. The overall conclusion was that with the Argus II, the percentage of correct identified letters greatly improved. A subgroup of six subjects was able to consistently read letters of reduced size [2] [8] [21]. The minimum size was 0.9 cm from a distance of 30 cm. Table 3.1 summons several of the subjects tasks. With the Argus II system on, the subjects had a significant improvement in some daily tasks.

The average implantation time for this trial was 19.9 months [8]. Long-term studies with the Argus II implant showed that the device was well tolerated and functional over a 1-year follow-up period [47].

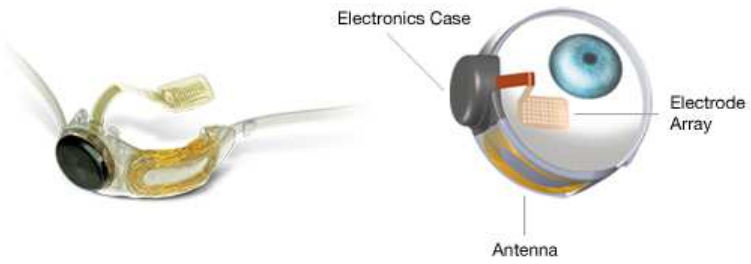


Figure 3.7: Argus II epiretinal prosthesis [40].

Table 3.1: Performance test of the Argus II system [46].

Tasks	System on	System off
Locate ordinary objects at various distances	75.0 %	20.8 %
Sort light from dark laundry	83.3 %	4.2 %
Travel within home independently	92.3 %	88.5 %
Identify ordinary objects at various distances	70.8 %	21.7 %
Independently cross residential streets	57.9 %	22.2 %
Avoid obstacles while walking	72.0 %	29.2 %

3.2.3. Intelligent Medical Implants IMI

Other promising research was performed at the company Intelligent Implants BmbH. They created an Intelligent Medical Implants (IMI) [19]. Twenty persons suffering from RP were selected for this acute human trial. The design is very similar to the Argus and EPI-RET implants. A digital camera takes images from the environment, processes the data, and sends it via a wireless transmission to the receiver implant. The microelectrodes stimulate the epiretinal side of the eye.
The implant consists out of three parts:

- The Retina Stimulator is the only part that is actually implanted into the eye.
- The Visual Interface consists out of several electronic components such as the camera, and the data and energy transmitters mounted in eyeglasses. The visual interface is connected via a cable to the pocket processor. Data is transmitted optically (IR) to the stimulator. Energy is transmitted using the electromagnetic approach.
- The Pocket Processor is responsible for image processing and power supply. The stimulator itself has no power supply. Images are translated into data signals for the retina stimulator. The information is send with IR LEDs from the front of the eye to the IR receivers on the stimulator. Because an optical link is used, eyelid closing causes the data stream to interrupt and no data will be transmitted, just as healthy eyes can't see when the eyelid is closed.

A trade-off decision must be made for the electrode size. Small electrodes have a low charge per unit area that can be run through without causing damage. Increasing the size of the electrodes can increase the charge but also decreases the selectivity. Instead of stimulating only a few cells with a small electrode, the stimulation area is larger. The conclusion was that a material and electrode size had to be found that was just large enough to stimulate the cells (the charge per unit area is above the stimulation threshold). With this in mind, the best selectivity is guaranteed while still being able to overcome the stimulation threshold of the retina cells. The paper of Robblee and Rose [39] investigates suitable materials for overcoming the stimulation threshold for human retinal stimulation.
For this trial, three different electrode sizes were tested: 50, 200 and 360 μm. The impedances were tested with a frequency range 1 to 100 kHz. The impedance was found to be 4 kΩ at a frequency of 1 kHz, which is comparable to the Argus II implant [51]. After the experiments a charge density of $1 mC/cm^2$ for 4 hours is safe and does not induce any tissue damage [39]. The mean stimulation threshold was found to be far lower than this maximum: 195 nC with a standard deviation of 189.7 nC [39]. Which is also in agreement with the results found in the Argus II studies [1] [51].

4

Design & specifications

The OPTOEPIRET implant will take over the function of the photoreceptors in the retina layer. As already mentioned in Chapter 2, visually impaired or blind people lose this layer and therefore their vision. However, studies showed that about 30% of the ganglion cells stay intact in RP patients after many years of blindness [22] [23] [28]. A retinal implant detects the incoming light and transforms it to electrical signals that can stimulate the different remaining ganglion layers of the retina [1].
Figure 4.1 shows the design of the retinal implant. The 9 mm diameter implant will feature multiple wings that interconnect in the middle like a flower. This thesis will focus on manufacturing and testing a single 'wing'. Due o the implants symmetry, the results from a single 'wing' can be used to design the final implant. The cable connects the part with the electrodes to the inductive coil for energy.
Light will fall on the CMOS sensors of the chip. This light will be processed and transferred through the polyimide substrate to the electrodes. The electrodes will thereafter stimulate the ganglion cells. The signals will be transported and interpreted by the human brain in the same way as a person with healthy eyes would. Figure 4.2 shows a side view of the retinal implant and its layers.

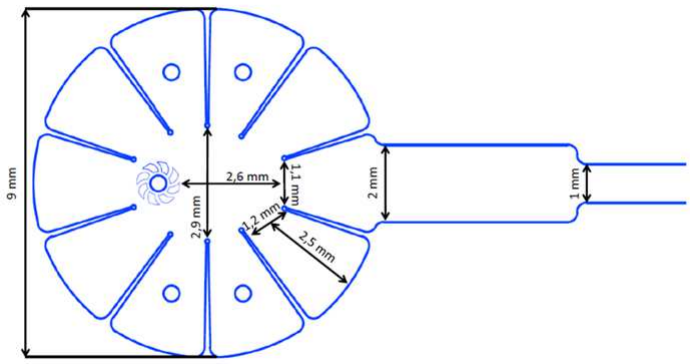


Figure 4.1: The OPTOEPIRET implant with the ten identical wings, based on the VLARS design.

The next thing to determine was to come up with a method to measure the through-connection from the chip to the electrodes. The chip and the polyimide substrate will be constructed separately but after they are glued together, it is not possible anymore to measure the contact points between the chip and the substrate. The measurements are needed in order to check whether the fabrication of the interconnects is valid and survive the stresses that occur during the bending motions. To solve this, additional wiring was created with gold paths and pads leading to the outside of the chip. This meant that the final size of the implant for testing would be increased. But this is only in the testing phase. After testing, the additional paths and pads for measurements will not be included in the design. A first impression of the design is given in Figure 4.3 (side view). The final implant will be the inner parts of the structure. The large measure pads are indicated with the letters A and B.

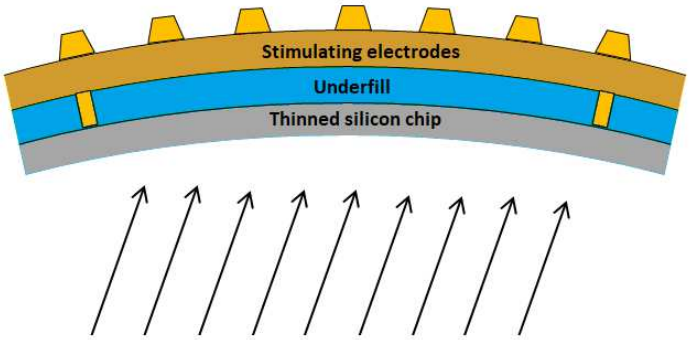


Figure 4.2: Schematic representation (not to scale) of the complete two-part dummy implant with through-connections.

4.1. Design criteria

At the end, the two parts will be bonded together via flip-chip bonding (Chapter 10). The retinal implant has to be flexible enough in order to survive the implantation into the eye and the curvature of the eye itself. The implant will be manufactured on a flat wafer, and after processing it has to have flexibility properties allowing it to bend to at least the curvature of the human eye (eye radius is roughly 12 mm). To try and achieve this goal, several design criteria and specifications were set up, and listed below:

- This thesis design focuses on a single 'wing' structure with maximum dimensions of 8 mm by 5 mm. These dimensions are chosen to resemble the final size of the retinal implant. The length is bound to the maximum incision the surgeon can safely make in the human eye.
- This dummy implant will not be implanted and serves only to develop a process that can later be implemented in the actual retinal implants.
- The contact pads for the chip should all be placed at the edges of the implant. The main reason for this decision is that when the flip-chip bonding method proves to be invalid, traditional ball-wedge bonding is still an option.
- There should be a connection from the implant through the polyimide substrate to the electrodes that will be in contact with the retina.
- The electrodes that are in contact with the retina have a size of 120 by 120 μm, corresponding with previous retinal implant designs manufactured in this institute.
- The base material of the substrate will be polyimide (PI-2611) with a layer thickness of 5 μm.
- The interconnect and electrodes will be gold.
- The through-connections will have a height of 5 μm. The electrical paths will be 2 μm height. These specifications are chosen conform the previous projects performed at the IWE RWTH Aachen University.
- The silicon chip has to be thinned to a point that it becomes flexible. This point lies beneath a thickness of 100 μm[47]. A thickness of 20 to 50 μm is aimed for.
- A process has to be developed to fabricate such thin, flexible and homogeneous silicon chips.
- The entire implant has to be mechanically flexible enough to be placed in the human eye and survive implantation. This means that the silicon, polyimide and gold connections have to stay intact when confronted to multiple bending motions. The dummy implant will be placed in a bend setup with a gap in the middle of 6 mm. With this gap, a minimum bending depth of 0.4 mm has to be achieved to resemble the curvature of the eye. The calculation is shown schematically in Figure 4.4. The letter 'd' represents the minimum distance the implant has to be bend to have the same curvature as the human eye. Due to the gap of 6 mm in the bend setup, the implant (although it is larger) is modeled to be 6 mm. It is assumed, that the rest of the implant follows the same curvature.

- To be able to measure whether the interconnect and the through-connections survive the shear and compression forces, additional measurement pads (with a size of 800 by 1000 μm) will be included. These pads will be at the left and right side of the implant, increasing the final size of the implant to 24 mm. The state of the through-connection can be determined by measuring the resistance between points A and B in Figure 4.3. This increase in size is only implemented to take measurements. The only relevant part of the implant (the inner 8 mm) will still be subjected to the bending motions conform the curvature of the eye.

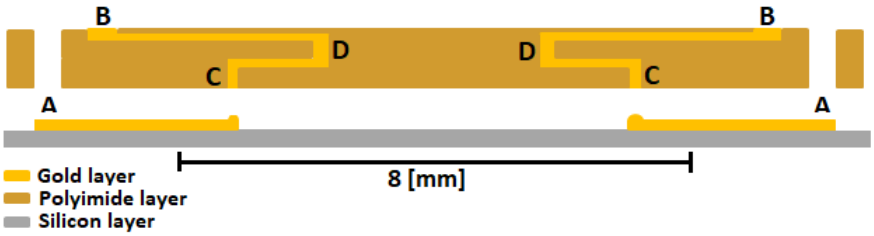


Figure 4.3: Schematic representation (side view, not to scale) of polyimide substrate and dummy chip.

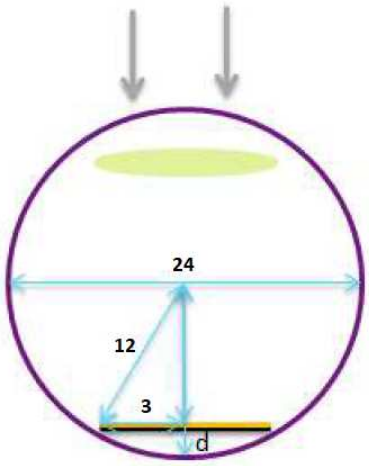


Figure 4.4: Schematic representation of the retinal implant (not to scale) and the curvature of the human eye.

4.2. Different designs

After the general specifications and dimensions of the implant were determined, several sketches were made before drawing the final design in AutoCAD 2017. The goal for these designs was to try and implement as many electrodes as possible. At the end, if this implant is really implanted into humans this way of thinking is very attractive because more pixels means in general a better field of vision. However, in the early stages it was found more useful to test the characteristics of the implant and materials, instead of focusing only on maximising the number of electrodes. The goal of this project is manufacturing and testing a part of the retinal implant and stress testing it by submitting it to bending forces.The chosen design features 16 electrodes with 8 connections to each side. This means a total of 32 measurement pads are located on both sides (16 on the chip and 16 on the substrate. An autoCAD design (top view) of the polyimide substrate design is shown in Figure 4.5.

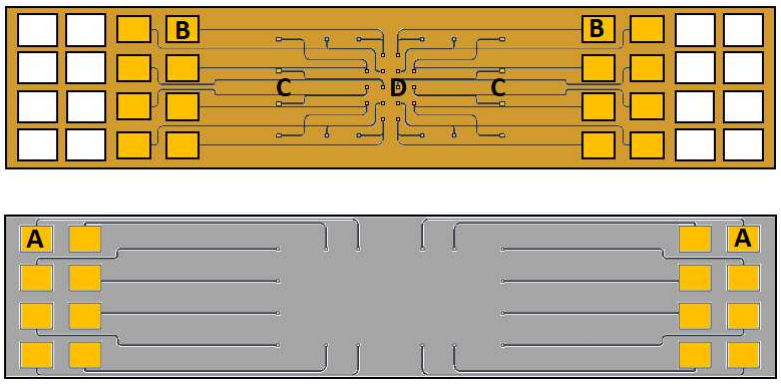


Figure 4.5: Top view of the test structure implant. Top part is the polyimide substrate, bottom part the silicon dummy chip (design 1).

Table 4.1: Overview of different substrate and chip versions.

	Polyimide substrate	Silicon dummy chip
Design 1	Size: 24 by 5 mm Electroplating, PI and gold pads equal size	Size: 24 by 5 mm
Design 2	Size: 24 by 5 mm Electroplating, PI and gold pads equal size	Size: 10 by 4 mm
Design 3	Size: 24 by 5 mm Electroplating, smaller PI holes	Size: 10 by 4 mm
Design 4	Size: 24 by 5 mm Gold sputtering , smaller PI holes	Size: 10 by 4 mm

4.2.1. Implant design 1

Figure 4.5 illustrates the first design of the chip and the polyimide substrate. The measure pads (A and B) are visibly larger than the electrodes (D) in the middle. This is done to enable easy measurements and handling to determine whether the through-connections stay intact during the stress and bend tests.
Nine substrate masks were needed to fabricate this test implant, three polyimide layers and four galvanic layers. The last two masks are for the dummy chip, consisting of a silicon base material with gold interconnect on top of it. Chrome masks feature the possibility for highly detailed structures. However, all objects in the AutoCAD designs for this project are larger than 20 µm, making a substrate mask more than suitable (and cheaper) for this project. Appendix B depicts the seven masks.
Multiple structures are placed on a single wafer, as can be shown in Appendix C. No structures are placed near the edges due to in-homogeneity effects at the outer edges. A total of 26 chips or polyimide substrates can be manufactured from one wafer with this design.

To align all the masks with the wafer before exposing, additional markings have to be placed for position localisation. The markings are alignment structures and are shown in Figure C.2. The left side of this figures shows the actual crosses that are used for localisation. On the wafer, the outer edges of the crosses are already visible through the microscope (for example, the outer crosses are gold on the silicon). To align the next mask perfectly in order to have all layers exactly on top of each other, the inner cross has to fit as good as possible in the outer cross. Once the mask is aligned with the wafer, the exposing step can begin. The right side of Figure C.2 shows a structure that is used for additional test structures and for process control. Each layer must have a specific thickness. To be able to test this easily, this structure is also included on the wafer. During every step a piece of the horizontal line is also exposed and structured (from left to right). This is done in a staircase manner, always leaving the original layer intact so someone can measure the thickness differences between the current layer and the previous layer.
Figure B.1 shows actually two different designs. On the same wafer, there are two kinds of interconnect: round edges and sharp edges. Layer GL-2 and GL-4 show this in Appendix Figure B.1. This is chosen to investigate whether the design with the smooth/round edges withstands higher bending stresses. The stress build-up is always higher at corners. Eliminating or minimising these corners could give the implants a higher stress resistance. However, it is expected that the difference between the two is minimal because the gold interconnect layer is very thin and relatively flexible.

4.2.2. Implant design 2

In the first implant design, both the chip and the substrate share the same dimensions. This was chosen in order to be able to measure the through-connections of the total implant. However, after several months it was thought of to make the chip smaller in size, getting rid of the large measuring pads at the side, and still be able to measure the connections. This should, in theory, make it easier to release the chips from the wax layer after thinning, and improve the overall handling of the thin chips. As an additional advantage, more chips could be manufactured on a single wafer.
Figure 4.6 shows this new dummy chips design. The chip can be placed on the polyimide substrate the same way as in design one: via the chip connection points located in a rectangular fashion (See the previous Figure 4.5). The chip connection points are now all connected (in a so-called Daisy-chain). The measuring pads for the substrates are still intact, as can be seen in Figure 4.3. If the through-connections of the two top left measuring pads want to be measured, this is still possible. The electrical path runs now from the first pad through the implant to the dummy chip, where it runs through the next chip connection pad (because they are now all connected), and back through the implant to the large measuring pad on the substrate. The daisy-chain enables the possibility to measure every through-connection (only pair wise).

Another difference in this design is that the wafer can be divided into four identical pieces. This gives the possibility to decrease the possible surface tension on the wafer as its getting thinned. The surface tension problems of the wafers are discussed in more detail in Chapter 6.

4.2.3. Implant design 3

Polyimide substrate design 3 features larger gold pads. The size of the pads was increased from 120 µm (same as the PI-layer) to 150 µm. This addition was chosen after the previous two versions were tested thoroughly. The rest of the substrate was kept identical.

4.2.4. Implant design 4

Manufacturing the substrates is very time consuming. The four galvanic steps and their corresponding masks take a lot of time to manufacture. The four steps are needed because first the pads are grown and then the connecting paths (twice). To save time and other troubles that occurred during the fabrication of the substrates (discussed in Chapter 8), this last version is manufactured using a gold sputtering method. Now the gold pads and paths are applied in a single step.

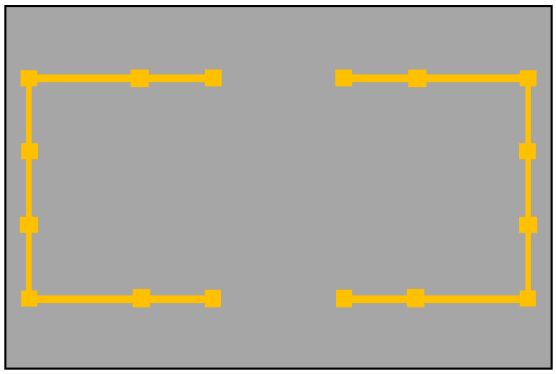


Figure 4.6: A more detailed close-up of the second dummy chips design and its daisy chain.

5

Dummy chip: Overview

The dummy chips are made from a basic four inch silicon wafer that is structured with gold electrodes and paths. In this research project, two different processes were implemented to fabricate such chips. This Chapter will elaborate on the two processes used to manufacture such dummy chips. However, these are the standard steps and after multiple versions, different findings resulted in altering the steps slightly. Those experimental findings and results and their differences are discussed in more detail in Chapter 6.
A 500 µm silicon oxide wafer is used for the fabrication of the chips. When the electroplating step is performed (for galvanic gold pads) without oxidised wafers (backside only), the gold also forms on the entire backside of the wafer. The oxide layer forms a passivisation layer, making sure the gold only forms on the areas of interest. The oxide layer is only a few 100 nm thick, which is enough for the passivization. For the first dummy chip fabrications (Version #1 - #5) some did not have any gold electrodes and paths on the wafer. In these cases, no oxidised wafers were needed and normal silicon wafer could be used. In this report the wafers used to fabricate the dummy chips are monocrystaline P/Boron silicon and in the 100 plane.

- The general idea at the beginning was to first structure the silicon wafers with gold electrode and etch the trenches (from now on called: **trenches-first**). The trenches are to isolate the chips from each other on the wafer. Only after these steps, the wafers are thinned from the backside until the trenches are almost free. With an-isotropic plasma etching the last few micrometers are removed until the trenches are completely free and the chips can be separated from the wafer. (Isotropic etching would also cause the removal of the sides of the trenches). A detailed table of the processing steps is shown in 6.1 in Chapter 6. This table shows the different processing steps for each dummy chip version. The full list can be found in Appendix D.
- From Version #6 the process sequence was altered. Some additional cleaning steps (step ●8 in Table 6.2) were included and the trenches were etched as a final step instead of before mechanical thinning (from now on called: **thinning-first**). Another difference is that the use of a protective photoresist layer (step ●6 in Table 6.2) on the active side before gluing the wafer on the carrier is left out in Versions #6 and further. The reason for this is discussed in Appendix H.4. The corresponding process list, discussing the different versions and their variations, is displayed in Table 6.2. Once again, a more detailed process list with all the steps can be found in Appendix E.

Figure 5.1 schematically displays the fabrication steps for thinning silicon wafers. The silicon wafer (1) is structured with gold interconnect via electroplating (2). The wafer is glued with the active side to the glass carrier with wax (3). The glass carrier enables for easier handling in thinning the silicon wafer from the backside (4). After the wafer is thinned, the trenches are etched free (5). The wafer is placed in a hot Isopropanol bath overnight to be released from the glass carrier.

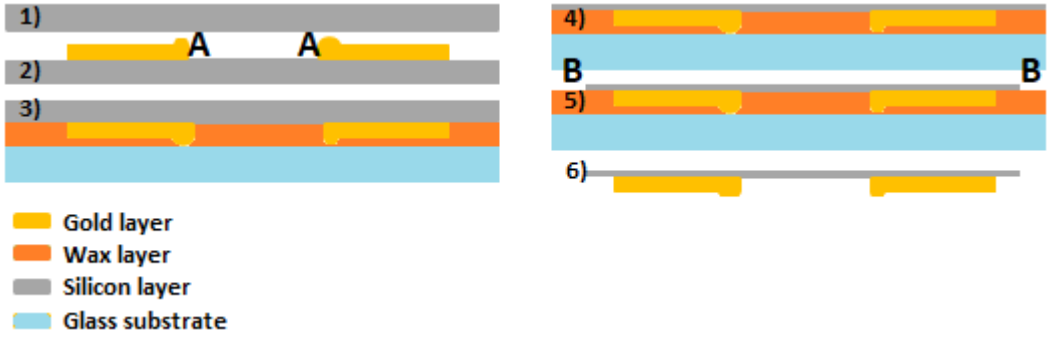


Figure 5.1: Side view: schematic representation (not to scale) of silicon chip layers. (1) Silicon wafer. (2) Gold pads (A) to connect to the carrier, and paths deposited via electroplating. (3) Placing wafer with active side on glass carrier with a wax layer. (4) Thinning wafer. (5) Dry etching the trenches (B) to isolate the chips on the wafer. (6) de-bonding procedure.

6

Dummy chip: Process experiences

A total of 9 different versions of dummy chips were manufactured. A table of all versions and their major changes can be found below in Tables 6.1 and 6.2. As already mentioned in Chapter 5, two main methods were used for manufacturing the thinned chips (trenches-first and thinning-first). The crosses and/or checkmarks indicate whether this step was performed in this version or not. Every version consisted out of four to eight wafers. An overview of every single wafer and its production timeline is given in Appendix I.

Table 6.1: Total table **Version overview Trenches-first**

#	Version			
Process step	#1-2	#3	#4	#5
Step ●1 Wafer type	non-ox	ox	non-ox	ox
Step ●2 Plating-base	✗	✓	✗	✓
Step ●3a Photoresist	AZ5214			AZ9260
Step ●3b Exposing & Developing	Front side			
Step ●4 Gold Galvanic	✗	✓	✗	✓
Step ●7a Trench etching	25- 60 µm, in-homogeneous			
Step ●7b Etching plating-base	✗	✓	✗	✓
Step ●8 Protective layer	✗	✓		
Step ●9a Pre-grinding substrate	20 minutes			
Step ●9b Gluing wafer to substrate	110 °C heat/ vacuum off directly			
Step ●9c Thinning 15 µm grain	in-homogeneous			
Step ●9d Thinning 9 µm grain	in-homogeneous			
Step ●9e CMP	✗	✗\✓	✗	✗✓
Step ●9f Cleaning step	✗			
Step ●10 Plasma etching	In-homogeneous			
Step ●11a De-bonding	2 hour 80 °C Isoprop.			Overnight Isoprop 80 °C
Step ●11b Cleaning	✗			✓

6.1. Mechanical thinning

The thinning procedure is done with the Logitech LP50 machine [43] shown in Appendix Figure H.5. The images shows the grinding plate with slits (later the plate without slits was used. This will explained more below). The Läppkopf is the grinding head where the wafer and substrate are placed, and held in place with a vacuum. The white rotating canister, contains the abrasive grinding liquid. There are two variants used:

- To start thinning the wafer from its initial thickness to a thickness of 60 µm, the more coarse 15 µm grain size is used. The coarse grain size enables for a faster thinning. However, stopping now would result in large surface cracks over the wafer. That is why the next steps are highly recommended.

Table 6.2: Total table **Version overview Thinning-first**

#	Version			
Process step	#6	#7	#8	#9
Step ●1 Wafer type	oxidised			ox, New design
Step ●2 Plating-base	✓			
Step ●3a Photoresist	AZ9260			
Step ●3b Exposing & Developing	Front side			
Step ●4 Gold Galvanic	✓			
Step ●5 Etching Plating-base	✓			
Step ●6 Protective layer	✓		✗	✗ Sawing in 4 pieces
Step ●7a Pre-grinding substrate	20 minutes		90 minutes	
Step ●7b Gluing wafer to substrate	110 °C, directly off	Slowly turn off heat	20 min on, cool overnight	
Step ●7c Thinning 15 µm grain	in-homogeneous	✗\✓	✓	
Step ●7d Thinning 9 µm grain	in-homogeneous	✗\✓	✓	
Step ●7e CMP	✗✓		✓	
Step ●8 Cleaning step	✗		✓	
Step ●9a Adhesion agent	HMDS	Ti Prime		
Step ●9b Photoresist	AZ9260			
Step ●9c Exposing & Developing	Back side			
Step ●10 Through trench etching	Cracked, poor wax adhesion		✓	
Step ●11 De-bonding	Overnight Isoprop 80 °C			
Step ●12 Cleaning	✓			

- The more fine 9 µm grain size is used to smoothen the surface even more and thin another 20 µm. The final thickness of the wafer should now be (in theory) 40 µm. The surface cracks are minimised to a maximum depth of 9 µm.

All abrasive liquids are in a suspension of 90% DI-water and 10% Aluminium-oxide (Al2O3). The removal rate can be slightly determined by several factors:

- The pressure from the grinding head to the plate. This pressure can be changed by turning a wheel at the center of the head, by which a spring is pressed together or extended. This spring regulates the wafer pressure on the grinding plate. The more pressure, the faster the removal rate. As an addition to this, it is possible to place a 2.5kg weight on the grinding head, once again increasing the pressure and removal rate. This is a very favorable technique for thinning the first few hundred micrometers. But, when the wafer becomes thinner, the chances are higher that the increased pressure is too much and the wafer cracks. Hence, this technique is only used until a wafer thickness of roughly 100 µm.
- The second method to slightly regulate the removal rate is the abrasive flow rate. If too much abrasive is used, aquaplaning occurs. The wafer 'floats' over the grinding plate and the removal rate drops dramatically. If not enough abrasive is used, the plate dries and aluminum-oxide grains form, which could scratch the plate and wafer. So a delicate combination has to be found.
- It was found during this project that the rotation speed also influences the removal rate and homogeneity. In the manual of the LP50, a speed of 50 to 70 RPM is recommended. However, the removal rate was far more steady (homogeneous) and faster with lower rotational speeds. Hence, after Charge #6 speeds around 30-35 RPM were set, which improved the homogeneity dramatically.

6.2. Chemical-Mechanical planarization

There are still small surface cracks in the silicon after mechanical grinding with a grain size of 9 µm. To further smoothen the backside surface, which improves the mechanical stability and flexibility, a chemical-mechanical polishing step is performed. The wafer is once again placed on the grinding head and polished. Two different polish plates were used in this project:

- A polyurethane polish plate. This polish plate was the default choice to polish the final micrometers of the already thinned layers. The plates polish rate was, however, very in-homogeneous. The outer edges were polished almost immediately, but the inner circle was never polished to a shiny surface. This resulted in very long polish sessions and very in-homogeneous thicknesses throughout the wafer (inner parts very thick, edges very thin). Because the wafers were not homogeneous in thickness from the start in the first 7 versions, this resulted in multiple damaged or broken wafers.

- After the thinning process was improved and more homogeneous (new grinding plate), a new polish plate was chosen. This polish plate is made from a synthetic fabric and can be glued on the grinding base. This plates removal rate was homogeneous and the wafers were polished over the whole surface.

The name of the process step already mentions it is a chemical and mechanical step. The chemical part of this process is a SF1 solution. This is a alkaline solution (pH of 10.5) that consists out of Si02 particles with a grain size of 30 nm. This basic solution, also called 'Syton', is mainly responsible for the removal rate [13].

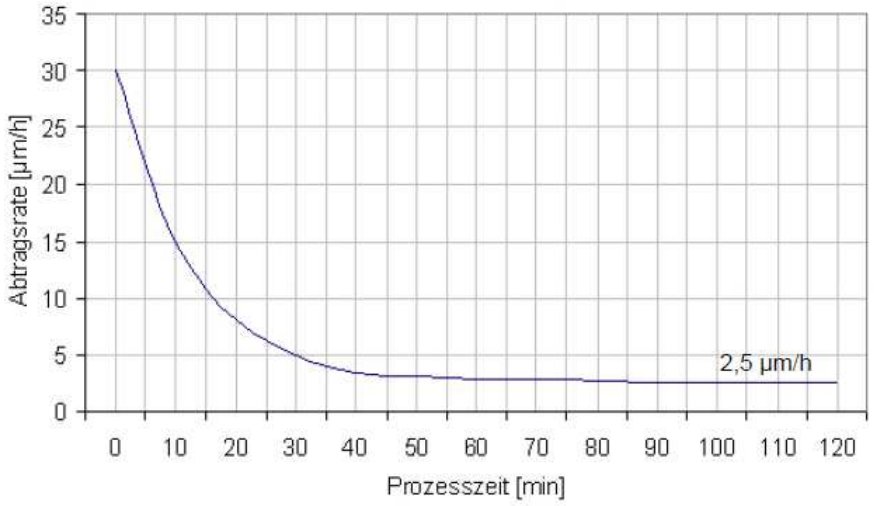


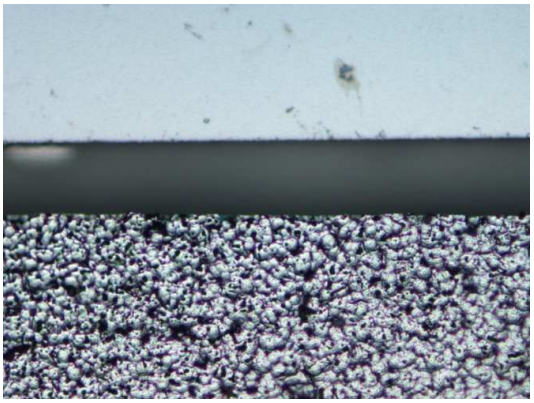
Figure 6.1: Chemical-Mechanical Polishing removal rate versus polish time [13].

After mechanical thinning the surface is rough and has many surface cracks. Hence, the first minutes polishing have a high removal rate. The rough surface has a lower contact area to the polish plate, realising a higher removal rate. The smoother the surface becomes, the larger the contact area between the surface and the plate, and the lower the removal rate.

Another aspect influencing the removal rate is the homogeneity after mechanical thinning. An in-homogeneous wafer (for example due to a convex thinning plate), has a higher removal rate because of the smaller contact area. The PhD thesis of F. Fuders from the IWE-1 institute in Aachen showed these relations in Figure 6.1. This data shows that a polish time of at least an hour should be taken to ensure the wafer is completely smooth. Figure 6.2 shows two different microscopic images of the backside of polished silicon dummy chips. The effects of polishing are easily noticed and the importance of this step is very clear. Figure 6.2b shows how a small scratch looks like on the dummy chip. Probably a large particle came between the wafer and the polish plate and scratched the wafer. These small cracks could later cause problems because they influence the mechanical flexibility.

6.3. Chip versions #1 - 9

Chapter 5 discussed the individual steps of the dummy chip fabrication. The upcoming sections will go further into the design choices that were made during all the different versions. Also the most important changes and challenges that occurred during the fabrication will be mentioned. Some details specific to the process are left out in this Chapter and can be found in Appendix H. The reader is invited to read these additional sections when more in-depth information about certain process steps is wished for.



(a) Silicon dummy backside. Difference between a rough and polished surface.

(b) Extremely polished surface with a single scratch, a larger particle damaged the backside silicon.

Figure 6.2: Microscopic images of the backside of silicon oxide dummy chips.

Chip Version #1

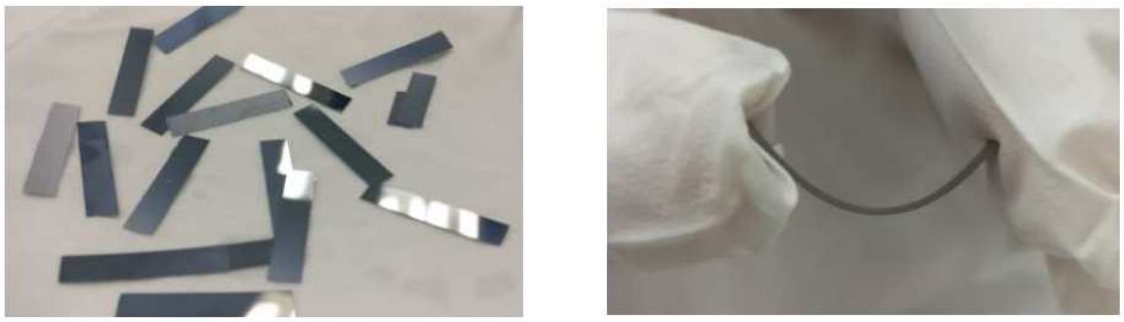
The first version was produced to get familiarised with all the process steps and find the possible weakspots and complications of the fabrication process. After the mask was applied, the gold paths and pads were grown on the silicon wafer using galvanic deposition. Then, the outside trenches were dry etched using a Tegal 901 (with CH4 to remove the oxide layer and SF6 to etch the trenches). This etching process was very in-homogeneous. The removal rate at the top-half part was faster than the bottom half part (see Figure G.2a in Appendix G). This problem could be partly remedied by rotating the wafer every ten minutes. However, the trench depths varied widely between 30 - 50 μm.
Two different grain sizes (15 and 9 μm) were used for mechanical thinning. The grinding plate showed to be highly convex, for which the grinding machine wasn't able to compensate for. This caused a further in-homogeneous removal rate and a very thin wafer on one side (already showing the free trenches), and a thicker wafer on the other side. This meant the wafers could not be polished, leaving the back surface rough. The few chips that survived were detached from the glass carrier. However, the chips were not homogeneous in thickness and do not feature the mechanical stability and flexibility.

Chip Version #2-4

For these different versions, a protective layer of photoresist AZ9260 was applied to protect the active side of the chip when gluing it to the glass carrier. However, in these versions the gold paths were left out to first try and determine a suitable thinning method first. From Version 1, it was noticed that while looking through the microscope, the top surface (not the surface that was mechanically thinned), was full of scratches. The protective photoresist layer could help to prevent this. The thought was also that when implementing this protective layer, the chips could more easily be removed during the lift-off step.
Dry etching with the Tegal 901 was still very in-homogeneous. To minimise these problems, the wafers were inspected every 10 minutes and the already freed trenches were covered with photoresist (manually with a brush). These parts were then protected, while the other trenches could still be opened without damaging the already finished chips.
To determine the in-homogeneity of the mechanical grinding, in two wafers the trenches were sawed mechanically to save time and then thinned using the steps also mentioned before. At the end of the thinning steps it was concluded that the grinding plate and head were very convex and the cable monitoring the homogeneity of the plate was faulty. It can be assumed that this was the main reason for the large thickness differences of the chips throughout the wafer. However, some chips succeeded and were relatively flexible. This is the first version that did not have completely fragile dummy chips (no gold paths and pads were included in this version). Figure 6.3 shows the successful Version 4 chips.

Chip Version #5

The thinning process is still not homogeneous enough. Mechanical thinning is done with the Logitech LP50 grinding machine [43]. The machine monitors the condition of the plate and can move the head slightly to try and minimise the in-homogeneity. Apparently the cable was broken, letting the machine think the



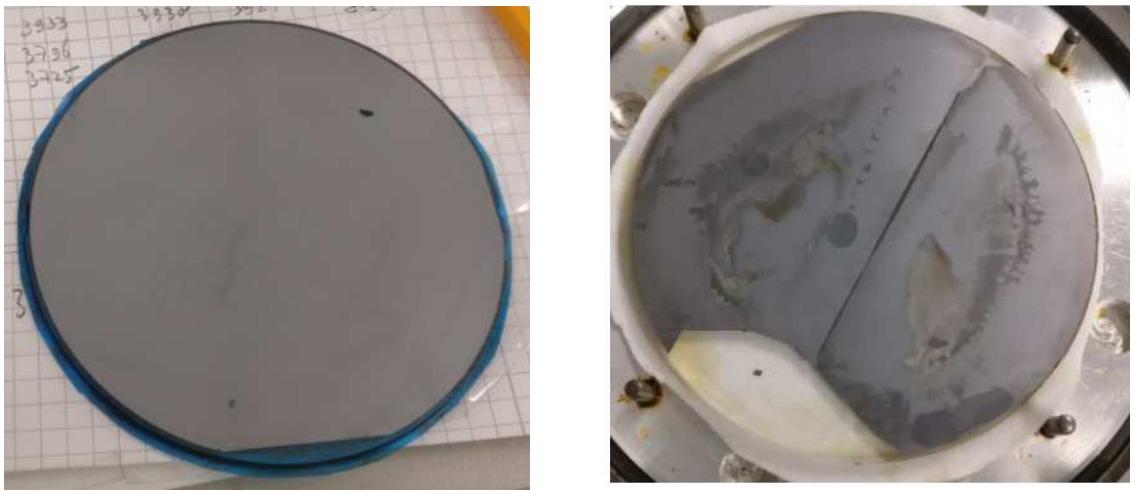
(a) First successful flexible dummy chips with no gold.

(b) First bend test with Version 4 chips.

Figure 6.3: Version 4 chips: First batch of flexible chips.

plate was very convex (which it was not at the beginning). The machine tried to overcompensate for that, making the plate more and more concave. From this point it was decided that a different plate had to be used. Unfortunately there was only one available with slits in it. The slits function is to minimise the effect of aquaplaning. This problem was counteracted by using a small piece of stone that grinds to the side of the plate, removing the build-up fluids at the etches. Now a grinding plate could be used without slits.

Another aspect that was changed in this version was the glass carrier. The carriers are used more than once, and after every time they are used they get thinner. It was perceived that when the total thickness of the wafer and glass carrier was below 3300 µm, the grinding rate reduced drastically. Normally a rate between 1 and 2 µm per minute could be achieved. But, when the thickness dropped under roughly 3300 µm the rate dropped to below 0.2 µm per minute. New glass carriers were ordered with a thickness of 5 mm so that the next Versions could be glued on the thicker carriers, in which it was hoped that this would improve the grinding rate. Another advantage of the new carriers was that the edges of the glass were still smooth. With the old carriers it sometimes occurred that a small piece of glass broke off from the side, damaging the grinding plate. To smoothen the plate once again, hours and hours of polishing was needed, throwing away valuable time. Figure 6.4 depicts two images were the damage is clearly visible. The small hole in Figure 6.4a eventually became larger and the crack spread over the complete wafer. Another possible advantage is that the new glass carriers did not need an adhesive foil layer on the backside to ensure a good vacuum connection during grinding. With the old carriers the vacuum did not always hold, and such foils were needed.



(a) Small hole in wafer (top right) due to broken piece of glass that damaged wafer.

(b) Piece of glass broke off from the carrier, cracking the wafer in three pieces.

Figure 6.4: Version 1-5: Glass carrier damages wafer sometimes. Left: The blue adhesion foil can be seen that is used to ensure a good vacuum connection.

The fabrication of dummy chips is still not optimised. The main problem is the homogeneity of the chips. Plasma etching and mechanical grinding do not have a steady and homogeneous etching/grinding rate. As already mentioned, the grinding plate and cable are renewed during Version #5, which helped with the homogeneity. After also using a new grinding head, the grinding was even more smooth. The LP50 shows that the plate deviation is less than 2 µm (before was over 10 µm). Also the trenches will not be etched at the beginning but at the end. The wafer will first be thinned to the final thickness of 25-40 µm, after which the trenches are etched. An advantage for this procedure is that the in-homogeneity of etching is overcome because now there is no need for etching a precise amount of depth in the silicon (before, the trenches were only a small distance in the thick wafer, now the trenches go through the entire thin wafer). The chips are protected with a photoresist and the trenches are etched until all are free.
With this method a new problem came to light. The wafer with the gold paths and pads were glued to the glass carrier. Normally during the lithography step the mask for the trenches was applied via normal front-side lighting. However, now the wafers need a backside backside alignment step. This meant that the glass carrier had to be clear, because in order to still see the markings on the wafer, you'd have to see through the carrier. Hence, polishing the glass carriers before gluing them on the wafer was now an important step. Normally the carrier was only polished from the one side where the wafer was glued onto.

Chip Version #6

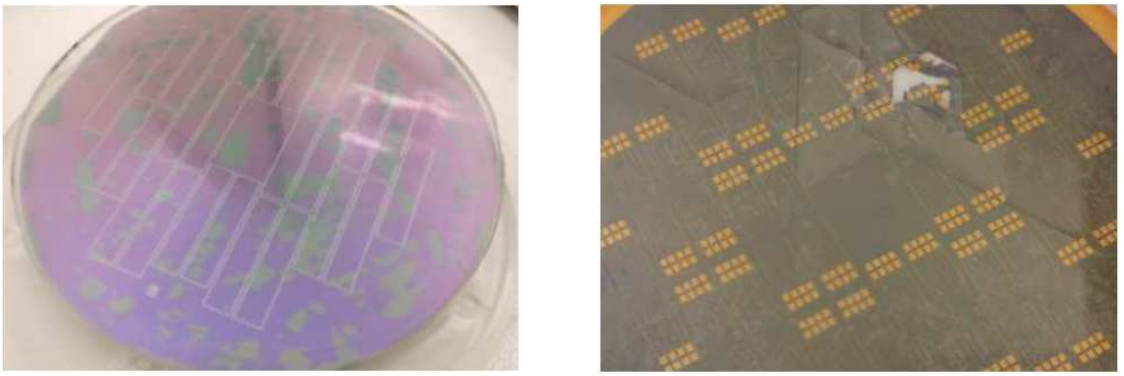
This is the first Version with this new process. The galvanic step and gluing the wafer on the glass carrier is a relatively simple step and runs smoothly. This version is to test all the further steps and practice with the backside lithography and identify problems or steps that need improvement or alteration. As mentioned in Section , the grinding head can be used to change the pressure on the wafer and thereby the thinning rate. However, the mechanics inside were completely stuck and the pressure could not be regulated. The grinding head was interchanged with another one, while the other was send to be repaired. Unfortunately the very thin wafers cracked during the HMDS [26] step. This step requires a vacuum, which the wafers could not handle. HMDS is an adhesion agent used at the final step when applying the photoresist to the backside of the silicon (for the trenches). HMDS enables a good connection between the silicon oxide and the photoresist.

Figure 6.5: Version 6 chips: Cracked wafers due to HMDS adhesion agent.

Chip Version #7

The new grinding plate and head enabled for a very homogeneous removal rate. But, the main focus on this Version is the final polishing step. After carefully looking under the microscope, it was observed that the surface was not always smooth everywhere. When there are still some surface irregularities due to the grinding grain, these can cause the chip to break or become mechanically unstable. In Version #6 the polish (CMP) step was performed when the chip was around 25-35 µm. The problem was the in-homogeneity of this polishing step. The polish head was slightly spherical. The outer edges were polished more than the inside. This meant that to completely polish the wafer, the outer edges became thinner and thinner. Consequently, the polishing step was only brief and not the entire wafer was polished. For Version #7 the polish step will

start earlier, around 35-40 μm, so that the entire wafer could (in theory) be polished such that the surface is smooth.
For backside lithography the photoresist has to be applied on the backside of the silicon. The photoresist does not hold on the silicon oxide layer. A new adhesion agent (TI Prime, see Appendix H H.6) was ordered to ensure the photoresist stayed attached to the backside of the wafer.
Once again all wafers cracked during the last polishing step or during etching (when the wafers were extremely thin). Some chips were still salvageable, but many were lost. The suspicion is that the wafers often crack because of their surface tension or the pressure changes (with the previously used HMDS adhesion agent). When the silicon wafer becomes thinner and thinner, the imperfections on the wafer or glass carrier or in the wax become more and more dangerous. One small fault, air, or polish solution can get between the wafer and carrier and after a while the wafer cracks.
Another aspect was the imperfect wax distribution. When the wafer gets thinner, more and more air bubbles grow between the two surfaces.. After a while the middle of the wafer releases from the wax and the edges are still firmly glued. This also results in a crack throughout the wafer. To solve the problem of this surface tension new masks were designed that will be sawed into four equal square pieces. In this way the silicon area is smaller, which should lessen the surface tension. Also the new masks feature a design with a smaller chip-size as discussed in Chapter 4.
The air bubbles could also occur because the protection layer applied on the active side of the silicon oxide does not hold very well. In Version #7 this was confirmed because all four wafers have air bubbles and the wax layer detaches from the wafer. Thus, for the next Version the protective layer was not used. This meant that the active side had no protection and could scratch easily. Additional awareness during lift-off was necessary. When the chips detaches from the wax, the chips had to be fully submerged in order that they could slowly sink to the bottom and not scratch. Scratching happened, as observed, when during lift-off the isopropanol was completely vaporised and the chips still hang partly on the glass carrier.



(a) Air bubbles compromising the adhesion.

(b) Cracked wafer due to poor wax adhesion.

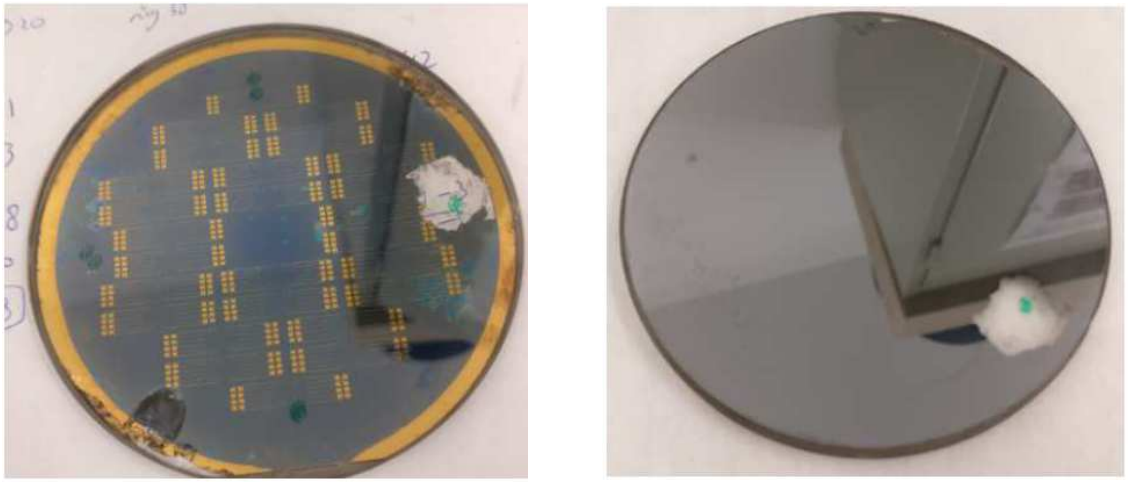
Figure 6.6: Version 7 chips: Air bubbles between wax layer and wafer.

The dummy chips that were successfully detached from the glass carrier and placed into a petri dish were still not flexible enough. As suspected, the surface was still not entirely polished and smooth. Thus for the next Version #8, the wafers will be polished with a new plate (even finer) and even longer. The last 15-20 μm will be polished in the expectation that this will be enough (and homogeneous enough) to fully smoothen the surface, enabling a flexible silicon chip.

Chip Version #8

In this version, the glass carriers were pre-grinded for a longer period of time. It was told from other project partners that grinding the carriers longer improves the homogeneity drastically. Normally this was done between 15 and 30 minutes, now this was increased to around 90 minutes. Table H.1 in Appendix H clearly shows that after around 60 minutes the removal rate gets very homogeneous. In this version, the glass carriers were pre-grinded for a longer period of time. It was told from other project partners that grinding the carriers longer improves the homogeneity drastically. Normally this was done between 15 and 30 minutes, now this was increased to around 90 minutes. Table H.1 in Appendix H clearly shows that after around 60 minutes the removal rate gets very homogeneous.

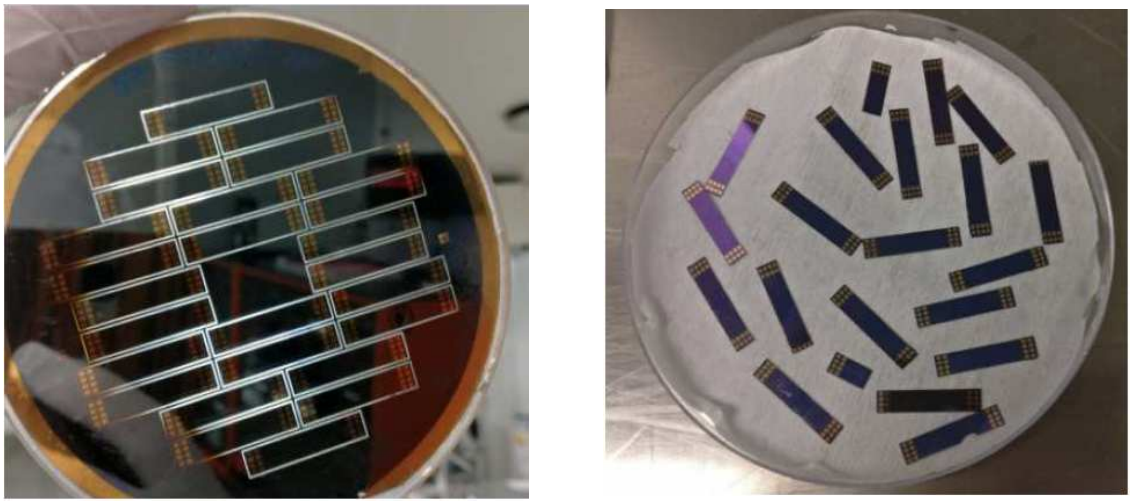
From now on the wafers are glued on the glass carrier and cooled overnight (without the protective photoresist layer). The other parameters in this step from Version #7 were left unchanged (See Table 6.2). The adhesion agent HMDS is not used anymore because of the suspicion the pressure differences crack the wafers. Ti Prime is now used as an adhesion agent for the photoresist mask during the backside lithography. A possible disadvantage in the future is that Ti Prime contains titanium elements, which could form a problem when using real chips (with logic) and not dummy chips. However, for this project now, the Ti Prime works very well and no wafers cracked in this Version. This meant that the photoresist layer that was always added as an protection caused indeed the air bubbles and cracked wafer due to the poor adhesion. The implant will be encapsulated with the biocompatible material Parylene C, hence TiPrime can still be implemented then.
The grinding head and plate are now in alignment and the thinning method proceeds without further difficulties. The wafers are thinned and after the back-side lithography step, the trenches are etched free. The first batch (#8 w4) of chips are flexible and have a uniform thickness of around 52 µm(slightly too thick according to the original plan). The chips are highly polished and have a smooth surface (See Figure 6.7b). A remarkable note can be added that all 26 chips on the wafer were successfully de-bonded from the glass carrier and appeared to be in a good condition.



(a) Hole in wafer during thinning.

(b) Even with the hole, the wafer is polished perfectly.

Figure 6.7: Version 8 chips: Highly polished wafer with small hole due to in-homogeneity.



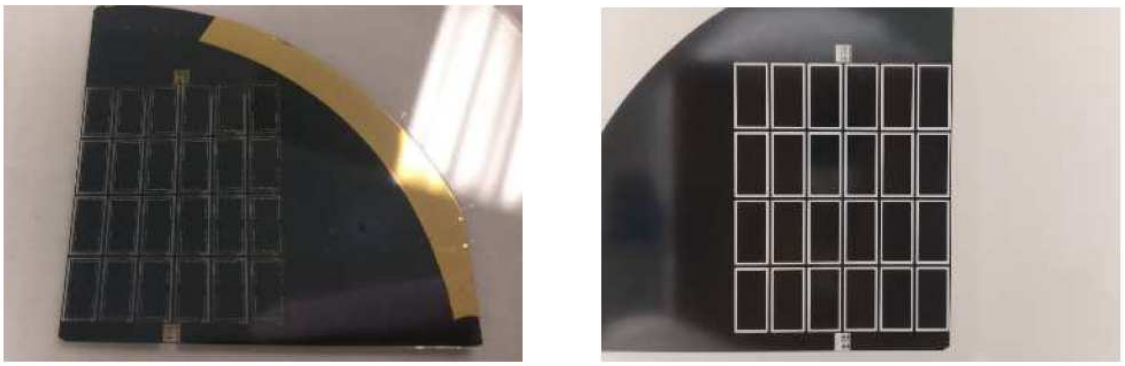
(a) Chips isolated using dry etching.

(b) First sucessful batch of chips.

Figure 6.8: Version 8 chips: First batch (yield 100%) of flexible chips with a thickness of 52 µm.

Chip Version #9

The newly designed chips were fabricated and the wafer was sawed into four pieces to simplify handling and relief possible surface stresses that occur when gluing the large thin wafer to the glass carrier. The quarter wafers underwent the same steps as mentioned in the previous versions. Thinning and polishing occured with a very high homogeneity. The smaller surface area ensured a higher and more homogeneous removal rate. After etching the trenches free, the individual chips were placed in a petridish. The complete manufacture of this version went without any problems. The only minor difficulty was making sure the sawed piece of wafer was placed in the middle of the glass carrier. This was needed due to the fact that the lithography microscope has a limited range of motion. When the wafer was not properly centered, it was possible that the allignment structures could not be seen due to the microscope. Images of the sawed wafer (front side) and the etched wafer are shown in Figure 6.9.



(a) Front side wafer with visible freed trenches.

(b) Backside wafer after etching trenches free.

Figure 6.9: Version 9 chips: new smaller design chips.

7

Polyimide substrate: Overview

The previous Chapter discussed the fabrication of the silicon (dummy) chip and the two different implemented processes. This Chapter will continue forth on the second part of the retinal implant: the polyimide substrate. The polyimide substrate is a support substrate that features the interconnect. The actual stimulating electrodes that come into contact with the retina are connected to the chip connection points at the other side of the substrate substrate. This so-called through-connection ensures the connection between the contact pads and the stimulating electrodes. The large horizontal gold paths are only included in the testing designs. The eventual implant will not have these, and the stimulating electrodes will be free and be pressed against the retina. Figure 7.2 shows a sketch of the implant design without the testing pads and connections. The stimulating electrodes are free and clearly visible on top.
As Chapter 4 mentioned, the implant size will be 5 by 24 mm. Figure 7.1 depicts a schematic representation of the different layers. The implant consists out of several polyimide layers of 8 μm thick and a total of four galvanic steps to grow all the gold interconnect. A more detailed list of the process steps can be found in Appendix F. It can be seen that the process of making the polyimide substrate is far more complicated and has more intricate steps then the dummy chips, hence the fabrication time is also longer. The dummy chips are fabricated generally within several weeks, in contrast to the several months of the polyimide substrate production times.

The support substrate with the gold interconnect will be fabricated on 4-inch silicon wafers with a titanium-aluminum-titanium sacrificial layer on it. The polyimide substrate will be constructed on this sacrificial aluminum layer (the titanium functions as an adhesion agent), and after the substrates are finished this layer is removed via wet etching and the substrates are released from the wafers. After the first polyimide layer is spin-coated, exposed and developed, the polyimide has to be hardened. The high temperatures with a maximum of 400 degrees Celsius ensures the hardening of the polyimide.
Before every process the wafers are cleaned and treated in a oxygen plasma oven. The oxygen flow rate has to be lowered accordingly if the wafers already feature a polyimide layer, as this plasma can also slowly etch into the polyimide. After the first polyimide layer, two different galvanic steps are next. The first step grows the gold connection pads to a height of 5 μm. The second galvanic layer is placed directly on top, creating the horizontal gold paths (2 μm) leading from connection pads to the outer measure pads. After a new polyimide layer is in place to ensure the different gold layers are isolated from each-other, the next two galvanic steps are performed. Once again, first the electrodes are grown with a height of 5 μm. After which the horizontal paths leading from the electrodes to the outer measuring pads are created. To shield the gold paths a last polyimide layer is coated on the top part of the substrate, with holes around the gold measuring pads. Table 7.1 shows this overview. On the right side of the table, a list of the main processing steps of version #9 substrates is listed. In this version, the electroplating method is changed to a sputter deposition to manufacture the gold interconnect in the substrate.
A more detailed and complete description of the processing steps and material properties can be found in Appendix F.

Table 7.1: Polyimide substrate fabrication modules (simplified)

Method:	Electroplating (version 1-8,10,11)	Sputter deposition (version 9)
Module 1	Wafer selection	Wafer selection
Module 2	Standard Polyimide PI2611	Standard Polyimide PI2611
Module 3	Galvanic 5 µm	Sputter deposition
Module 4	Galvanic 2 µm	nLOF 2070 7 µm
Module 5	Standard Polyimide PI2611	Standard Polyimide PI2611
Module 6	Galvanic 5 µm	Sputter deposition
Module 7	Galvanic 2 µm	nLOF 2070 7 µm
Module 8	Standard Polyimide PI2611	Standard Polyimide PI2611
Module 9	Lift-off	Lift-off

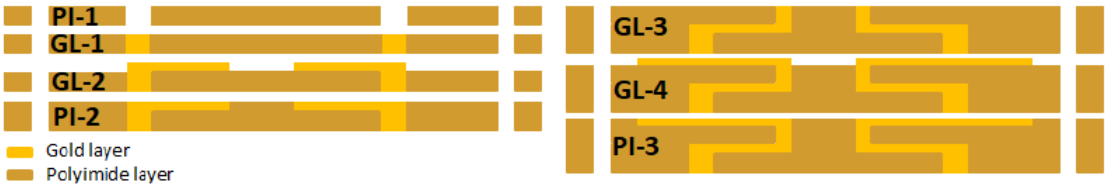


Figure 7.1: Side view: schematic representation (not to scale) of polyimide substrate layers.

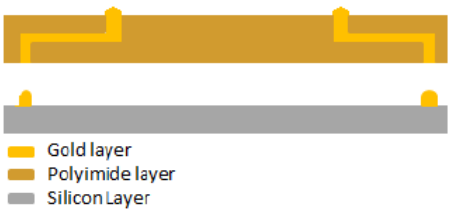


Figure 7.2: Side view: sketch (not to scale) of how the polyimide substrate would look like when not in testing phase.

8

Polyimide substrate: Process experiences

Chapter 7 discussed the standard processing steps for manufacturing the polyimide substrates. In this project, nine different versions were made of the polyimide substrate. A more detailed explanation of every version and its changes will be discussed in this Chapter. A brief overview of the versions and their major differences are shown in Table 8.1

Table 8.1: Polyimide version overview

Versions:	Differences
Version 1 - 4	Standard process as showed in Figure 7.1
Version 5 - 6	Missing gold pads due to TI plating base. Switching to chrome
Version 7	Double exposure after 2nd and 4th Galvanic to remove all mask
Version 8	New Galvanic masks. No more trenches between PI and gold pad
Version 9	Replacing galvanic with gold sputter deposition
Version 10 - 11	Same procedure and design as Version 8

Substrate Version #1 -2

This version was already manufactured before this master thesis work began. The purpose of this version was to find out whether it was possible to manufacture the through-connections in the polyimide substrates. The substrate design consisted out of several electrodes at one long end of the substrate, with a connection through the film and long gold paths to the other side of the substrate. The results showed that it is indeed possible to manufacture (these simplified) through-connections.

Substrate Version #3

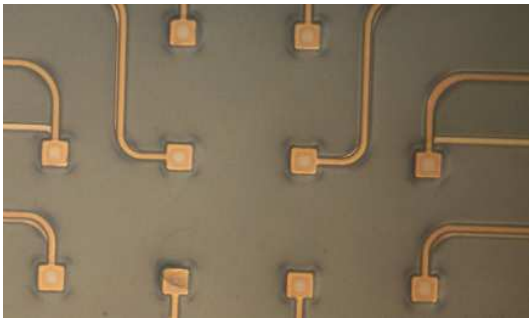
As already mentioned, the complete process list of manufacturing substrate implants can be found in Appendix F. This process list is for Version 5. The only difference with Version 5 and Version 3 & 4 is the use of chrome adhesion agent instead of titanium. The process of polyimide substrates was already well known at the IWE-1 institute for several years. Hence, it was expected not to have many difficulties manufacturing the polyimide substrates.

Substrate Version #4

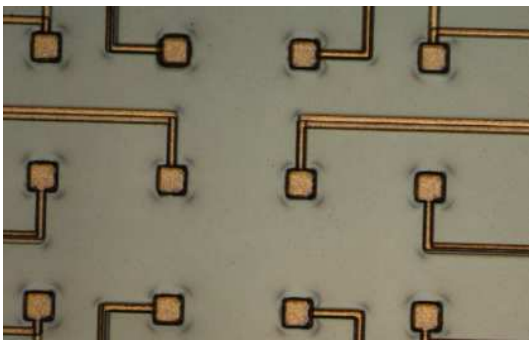
The same process list was run through again. But now yhe author was responsible for every production step and decisions. Once again, no troubles occurred during the manufacturing of the substrates. It happened sometimes that small artifacts were found on the substrates (air bubbles or dirt particles), however, the yield of the substrates was always over 95%.

Unfortunately, it was found that a crucial step in the fabrication process caused gold pads of the substrate-chip interconnect to fall out of the implant. This was only seen under the microscope after the version 4

substrates were completed. The gold pads are grown in the polyimide holes using electroplating. As an adhesion agent (as can be seen in Appendix F), a thin titanium layer was used. At the end of the process, the sacrificial layer (consisting out of Titanium- Aluminium- Titanium) was etched as a standard procedure. This caused the unwanted effect of etching the adhesion layer to the gold pads. The etch solution probably also reached to the sides of the pads, removing the thin titanium layer holding the gold. After each fabrication step, the state of the wafer and its layers is thoroughly checked. The gold pads were still intact before the lift off procedure. The substrates were detached from the wafer and it was assumed the pads were still all present. It could be clearly seen, through the microscope, that the electrodes fell out during the last step. Small gold rests were still visible in the holes were the pads were supposed to be. The future versions will feature a chrome adhesion agent. This ensured that the gold electrodes would not be affected during the removal of the sacrificial layer in the final step. Figures 8.1 show the inner gold through-connections of the polyimide substrates. Those connections are shielded from the etching step and are therefore still intact. Some surface tension of the polyimide substrate was visible around the pads. This was because of the height differences of the polyimide layer. This effect was expected and should not give any problems. Sub-figure 8.1a has round edges, in contrast to sharp edge sub-figure 8.1b. The next figure (8.2) shows two gold pads were only the holes are visible. The gold is (almost) completely detached.

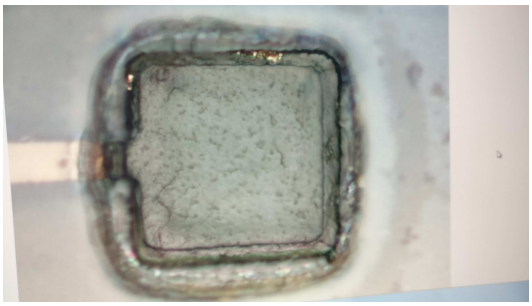


(a) Version 3: Intact gold through-connections.

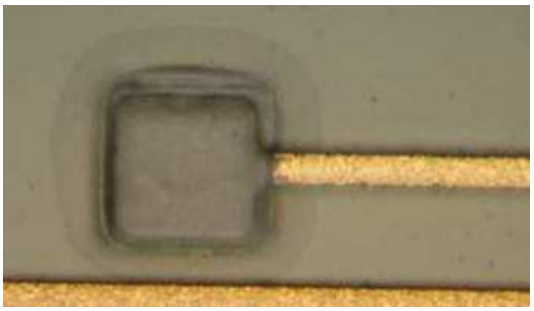


(b) Version 3: Tension around through-connections.

Figure 8.1: Version 3 substrate: Inner gold through-connections.



(a) Version 4: Small gold pieces in gold pad.



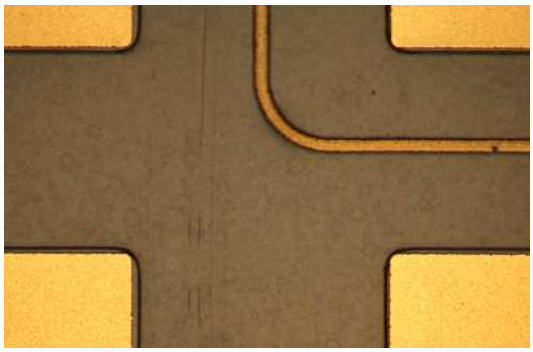
(b) Version 4: Missing gold pads.

Figure 8.2: Version 4 substrate: Missing gold pads due to etch step.

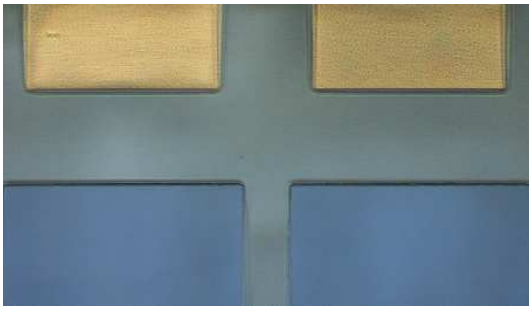
Substrate Version #5

Version 5 was immediately started after the crucial fault in the previous process list was found. The entire process was run again for 8 wafers with the only exception that a chrome adhesion agent was used instead of titanium. The process proceeded smoothly without any difficulties. After examination under the microscope it could be stated that the missing gold pads in Version 3 and 4 were indeed the cause of the titanium adhesion agent. In this version, all gold pads were present. The polyimide substrates are, as were other version, extremely flexible and did not break under the applied stresses. The large electrode pads and the corresponding holes were the dummy chip pads will come, are shown in sub-figure 8.3b. Sub-figure 8.3a that sharp edges with polyimide is not possible. The mask for the polyimide layer has very sharp edges. But the polyimide has

the property to slightly round all edges, as can be seen in the sub-figure. Around the sharp gold corners, a more round black line (the polyimide) can be noticed.



(a) Version 5: Measure pads.



(b) Version 5: Measure pads (top) and holes (bottom) for chip pad.

Figure 8.3: Version 5 substrate: Large gold pads on polyimide substrate.

Now, all the pads stayed in place, the next step of testing the substrates could begin. Until now, the substrates connections were tested only briefly because of the understanding that the polyimide substrate process was already well established. However, when testing all the individual connections, it was noticed that multiple electrode-pad connections were not intact. Resistance measurements were performed for every connection and the results showed that a great deal of the interconnect was faulty. Either a very large resistance was measured (ranging from 100 to 900 Ohm's), or no resistance was measured at all (open circuit). The ideal resistance would be around the 6 Ohm (calculated using gold resistance meter). Hence it was chosen that any connection with a resistance above 30 Ohm's would be defined as faulty. The long thin gold paths determine the actual gold resistance. The large and thick measure pads do not really contribute to the total resistance. Thus, the to calculate this resistance, only the path lengths are implemented. To give the reader an general idea of the values: the resistance of the large measure pads are 0.006 Ohm, quite some degree smaller than the 4 Ohm path resistance from the measure pads to the electrodes.

Substrate Version #6

Version 6 was already began before the faulty connections were found in the previous version. The goal for this version was to have enough substrates for the testing phase where the substrates were going to be bonded to the dummy chips. However, now this version purpose was to further evaluate and determine why the gold through-connections were sometimes not intact. Two wafers were taken out the clean-room into the laboratory and used for intensive testing. The wafers had just seen the 4th Galvanic step, meaning the top gold paths from the electrodes to the measurement pads outside were already present. Because the substrates were still on the wafer with the bottom plating base, the state of all the through-connections could be easily measured. One electrode is placed on the outer gold ring of the wafer (the entire gold layer is connected to the gold plating-base under the entire wafer and in connection to the gold electrodes formed during the first Galvanic step), and the other electrode is placed on every measure pad of the substrate (the large outside pads, eight on each side). Figure 8.4 shows the measurement setup. It can be seen that one electrode (left) is placed on the outer gold ring and the other electrode on the separate gold pads.
Version 6 showed two probable causes for the faulty connections:

- When the wafers are prepared for the galvanic step, there is still some residual photoresist in the sides of the holes where the galvanic has to grow. In previous projects this was sometimes the case. When implementing very deep small trenches, it seemed that sometimes not all the photoresist was removed after the lithography steps. Where the photoresist is still present, no gold will grow there, meaning the gold will not grow against the sides of the holes for the pads. Figure 8.8 shows a schematic representation of this situation, clearly showing that the presence of photoresist could cause a bad (or faulty) connection between the pad and the paths. Because the expsosing and developing step are done conform a 8 μm thick photoresist layer (and the layer is much thicker in the trenches) not all photoresist is removed.
- It was noticed that the polyimide hole, where the gold should grow inside, was some degree larger than

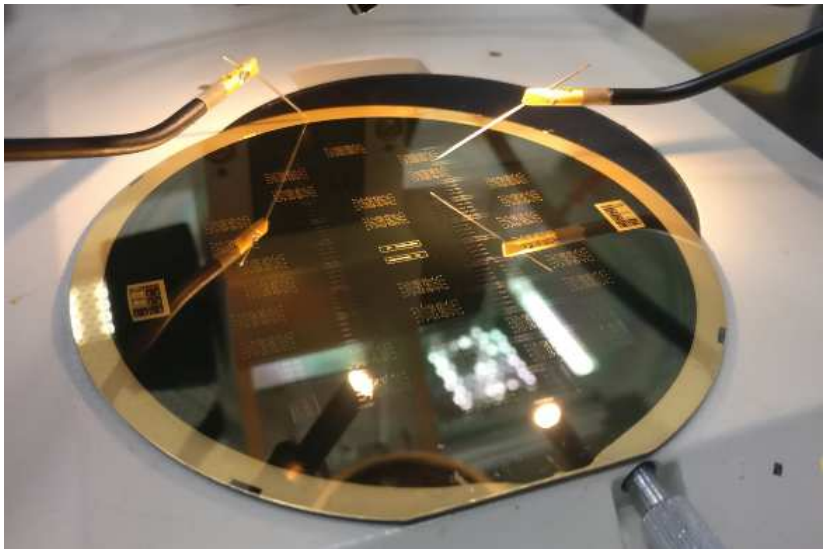
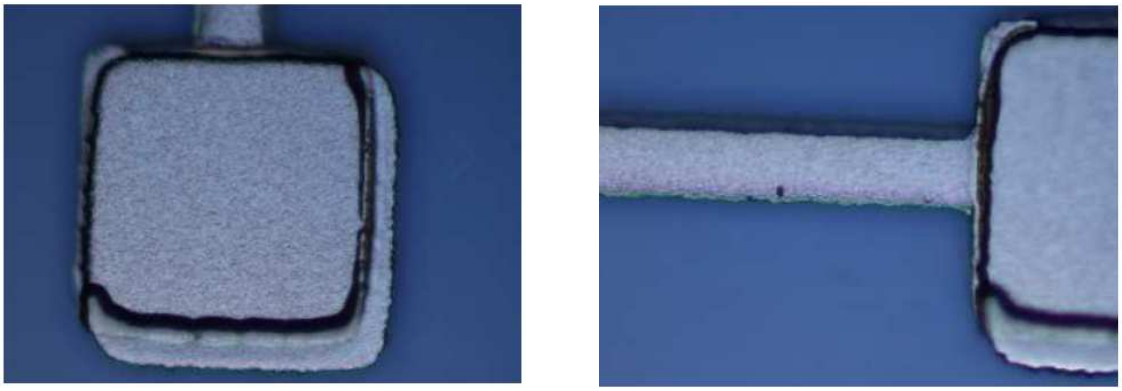


Figure 8.4: Measuring the through-connections of Version #6 Wafers.

the gold paths. This meant that the gold interconnect could break because it has to 'jump' over the edge leading from the pad to the path. To find out whether this was indeed the case, a new Version 7 will be manufactured and stopped directly after the second galvanic step. At this stage, only the first polyimide layer with the first gold interconnect is present on the wafer.

Figure 8.5 shows two microscopic images of the Version 6 electrodes. It can be seen that there is no perfect connection between the inner pad and the corresponding path. The next version should shed more light on the situation, showing which of the above mentioned causes are indeed true.



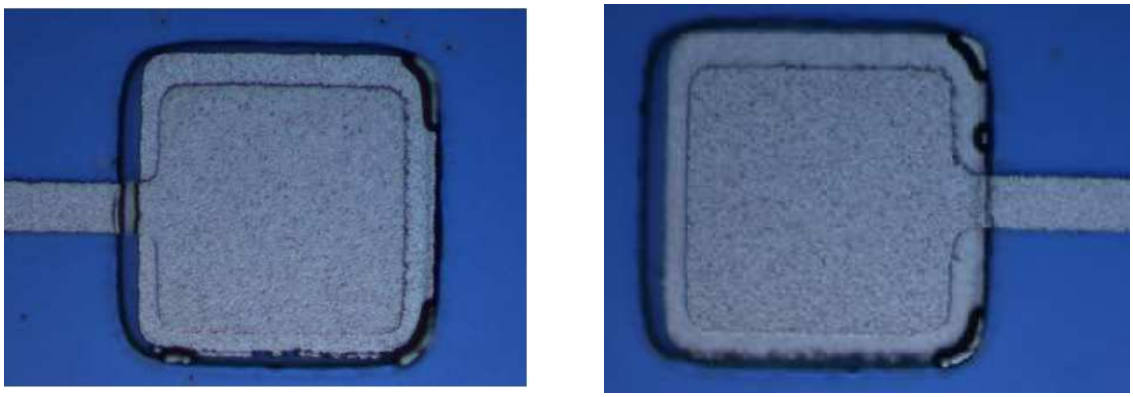
(a) microscope view. (b) Microscope view.

Figure 8.5: Version 6 substrate: view of an electrode pad after fourth galvanic layer.

Substrate Version #7

The possibility of leftover photoresist residue on the wafer was limited by performing the lithography step twice (two exposures). After the second galvanic step, the wafers were taken up to the lab for testing. It was found that the polyimide hole was indeed much greater and it seems that the paths either do not grow over the gap or they break/bend. Figure 8.6 clearly shows the large difference between the polyimide and gold hole. The images are much clearer than the previous microscopic images of Version 6 because they are taken before the second polyimide layer, which covers the possible trenches of the first polyimide layer.
Sub-figure 8.6a shows that the second galvanic layer (the path and the top pad) are positioned slightly too much to the right, causing a larger cap at the path side. On the right side of the pad, the gold has grown completely to the border of the polyimide hole. Sub-figure 8.6b is from the same wafer but shows another

pad with the path leading to the right. This connection, in contrast to the other pad, was in good condition. The reason seems pretty clear: because of the second galvanic step that is aligned more to the right side, the gold had no large trench to overcome and the connection between the pad and path was made. However, this was not always the case. most often, the connections were still not fully intact. The reader is invited to take a look at more figures of this version and the corresponding faulty and working connections in Appendix K. After examining multiple wafers and many chips it was concluded that there is no correlation between the location of the chips on the wafer or their specific locations inside the chip. Whether the connection was proper seems to be a large part random and a part depended on the alignment of the galvanic on the previous layer. Although the galvanic step was oriented more to one side, as shown in Figure 8.6, it was not always the case that there was a good connection. Sometimes the gap was just to large or the connection failed after the fourth galvanic step were the connection from the electrodes to the outer measure pads are created.



(a) View of dimension difference between PI and gold layer.

(b) Pad with other orientation and possible photoresist residue on the right side.

Figure 8.6: Version 7 substrate: Large gap between the pad and paths.

The size difference of the polyimide hole and the gold pad was measured to find out ascertain the numbers how much the polyimide pad was to large. The next version will feature larger gold pads, to overcome this problem with the galvanic steps (only galvanic layers 2 and 4 see this problem because they feature the connection between the pads and the paths). A graph of the measurement is displayed in Figure 8.7, clearly showing the gap on the right side. It was found that the average gap was around 15 µm. Version 8 substrates will feature pads with a size of 150 by 150 µm (instead of the 120 by 120 µm in the first galvanic layer).

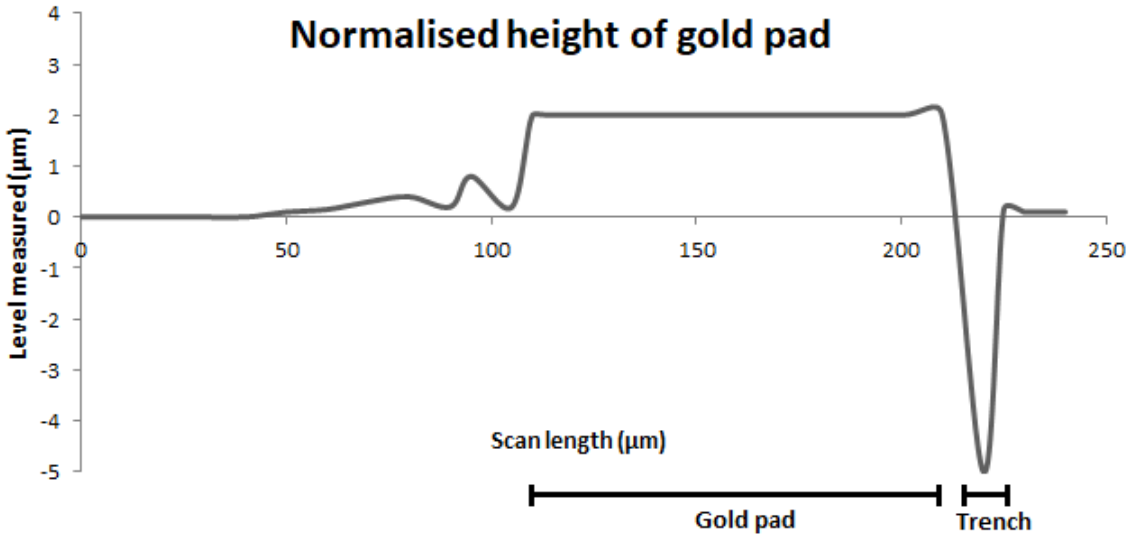


Figure 8.7: Version 7 substrate: measurement of the trench between the gold pad and the polyimide layer.

Substrate Version #8

Figure 8.8 shows a schematic overview of the two earlier discussed problems: left-over photoresist and the trench between the hole pads. When only exposing the photomask once, the intensity is not high enough to reach all the way in the gap between the gold and the polyimide (during the second galvanic step). Also if the exposing step is repeated, and all the mask is developed correctly, the gap is still too wide for the gold to overlap the trench between the first galvanic and the polyimide. Because the trench is around 15 µm and the second galvanic step only grows an additional 2 µm of gold the gold grows on either sides of the trench but will not connect (thus for example, the gold grows on the left side of the gold pad to the left, the gold grows on the left side of the polyimide hole to the right, but the distance is too great for a connection). Sometimes a connection is there, but after the removal of the plating base it probably happens often that the very thin connection between the pad and the path is etched away. This is because in the very thin and deep trench the gold will grow less fast during the galvanic step due to the low possible particle exchange.
This version implemented the new masks with the larger galvanic pads to ensure there is no trench between the gold pad and the polyimide hole. The exposing step is step is still performed twice, to guarantee the removal of all photoresist. Unfortunately, this version was stopped prematurely due to a contamination on the wafer after the plating base was vaporised on the wafers. Versions 10 and 11 will start this process again.

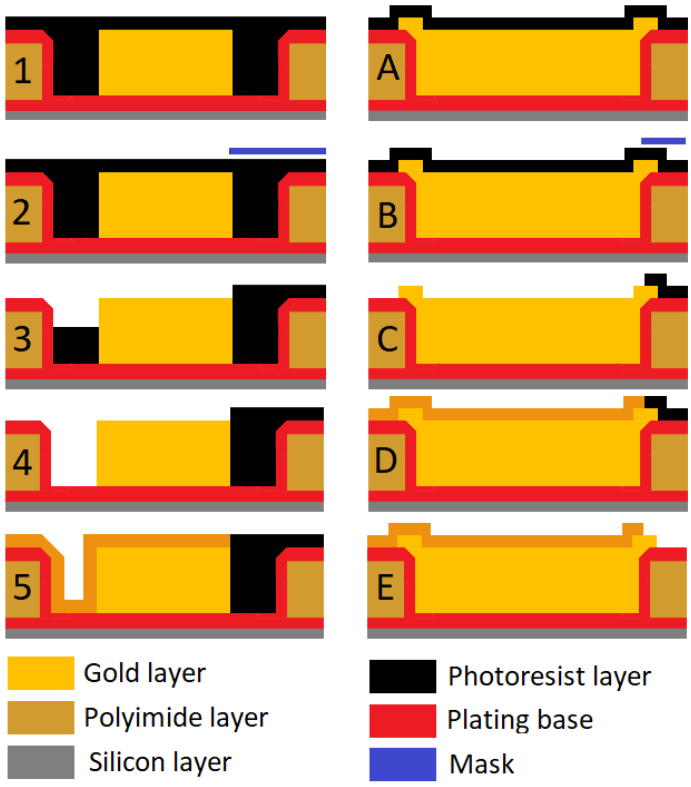


Figure 8.8: Schematic representation to show the need for double exposure when implementing two sequential galvanic steps (not to scale).

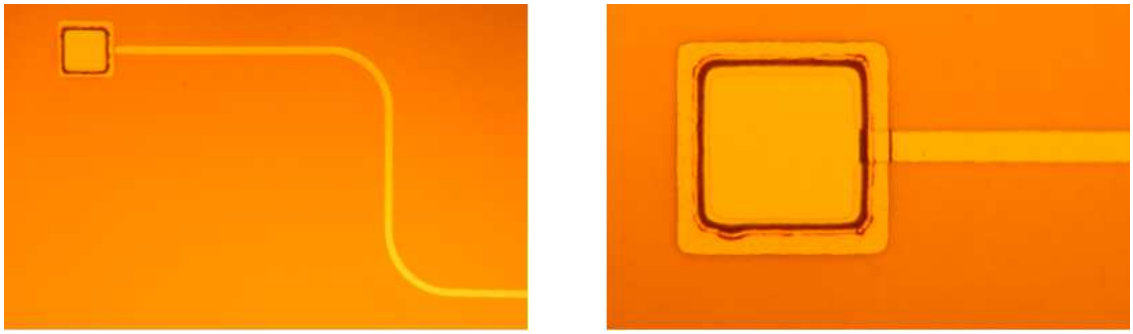
Substrate Version #9

This version features the new galvanic masks with the larger gold pads and a new gold deposition technique. The main problem in the fabrication of the polyimide substrate was the connection between the pads and paths. In this version, gold is applied on the wafer using sputter deposition. The gold deposition occurs with the Nordiko NS2550 Berlin machine. Both masks (GL-1 and GL-2) are used to expose the photoresist. This layer is not the standard photoresist as used in previous versions. For gold sputtering, AZ nLOF 2070 is used and exposed in 17.9 seconds with an intensity of 14 mW /cm2. Now the pads and paths can be constructed in the same step. An additional advantage is the shorter manufacturing time for the polyimide substrates. Unfortunately, not all gold interconnect stayed on the polyimide layer. The adhesion between the sputtered gold and the polyimide was not optimal in all places. The cause was presumed to be due to the missing

pretreatment steps for the polyimide. Normally before electroplating, the wafers go in the plasma oven and see a short pre-bake to ensure all the moisture is out of the material. This step was not implemented in this version, probably causing bad adhesion in some places on the wafer.

Substrate Version #10 - 11

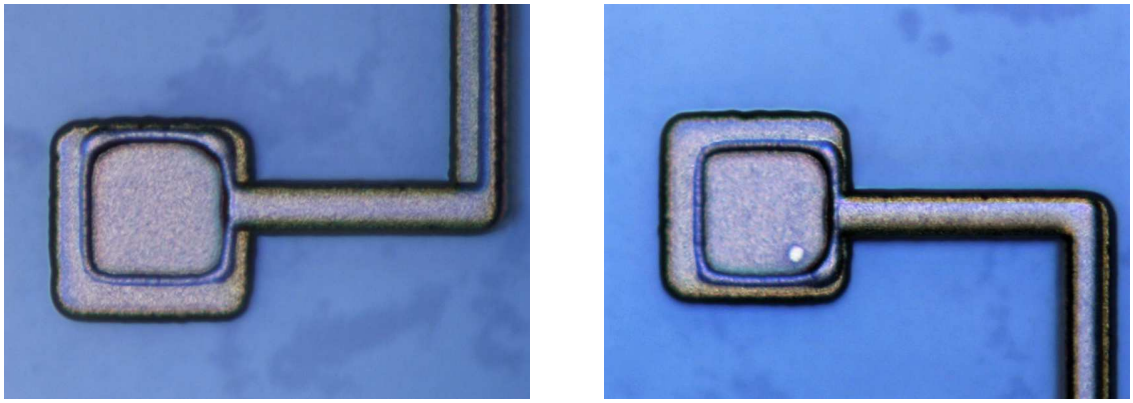
Version 10 and 11 feature the same steps as the version 8 wafers. Due to the fact that version 8 wafers were not finished, these two version were started to manufacture the polyimide substrates with the new masks. After the second galvanic step, the wafers were taken into the lab. The through-connections were now in a good condition, no trenches were visible between the gold pads and their corresponding polyimide opening (See Figure 8.9). The double exposing step and the new masks enable for a good connection between the pads and paths. The second galvanic pad is clearly smaller, as can be seen in Figure 8.9 by the bulged inner square. Figure 8.9 displays the results after the 2nd galvanic step, Figure 8.10 shows the results after completion of the substrate. The connection between the pad and path is clearly intact, with no trench between the two parts.



(a) Gold pad and path.

(b) Close-up view of gold pad.

Figure 8.9: Version 11 substrate: New masks with larger gold pads, no trenches between gold and polyimide. Good connection between pad and path after 2nd galvanic step.



(a) Microscope image of gold pad.

(b) Microscope image of gold pad.

Figure 8.10: Version 11 substrate: No trenches between gold and polyimide after completion.

9

Chosen processing steps for the implant

This chapter is included to give the reader a clear overview of the final chosen version and their processing steps of the dummy chip and the polyimide substrate. A combined of 20 different versions were fabricated during this thesis project, with numerous different changes per version.

9.1. Final dummy chip version

The dummy chip is manufactured on a oxidised wafer and structured with gold interconnect from the new masks (the small chips). The wafers are glued to the glass carrier (without the protection layer) under vacuum conditions for at least 2 hours and after this, cooled overnight. To minimise the possible surface tensions and for faster mechanical thinning, the wafers are sawed into four parts. Thinning occurs with the new grinding settings and plate/head. To smoothen the surface, the polishing step is prolonged to at least one hour, to ensure a completely smooth surface. A thin layer of Ti Prime (adhesion agent) is spincoated on the wafer before backside lithography. The chips are isolated using the dry etching step. The still remaining in-homogeneous removal rate does not form any problems when implementing this step after the wafer has been thinned to its final thickness. Table 9.1 shows the steps once more in a clear overview.

9.2. Final polyimide substrate version

The substrate substrate is manufactured with a chrome adhesion agent between the gold and polyimide. The gold pads of galvanic layer 1 and 3 are increased to minimise the possibility of a trench between the pads and the polyimide holes. To ensure all the photoresist is exposed (also in the possible deep trenches), and the gold can grow a good connection between the pads and paths, the lithography step is repeated. During the steps in galvanic 2 and 4, the photoresist is exposed twice. Table 9.2 shows a clear overview of the layer and its important fabrication parameters.

Table 9.1: Chosen final dummy chip version

Process step	Chip version #9
Step ●1 Wafer type	oxidised wafer
Step ●2 Plating-base	Gold- chrome layer
Step ●3a Photoresist	AZ9260 Positive photoresist
Step ●3b Exposing & Developing	Front side lithography
Step ●4 Gold Galvanic	Electroplating method
Step ●5 Etching Plating-base	✓
Step ●6 Protective layer	✗ causes bad adhesion
Step ●7a Pre-grinding substrate	90 minutes
Step ●7b Gluing wafer to substrate	20 min on 100 °C, 2 hours with vacuum on, cool overnight
Step ●7c Thinning 15 µm grain	Till a thickness of 60 µm
Step ●7d Thinning 9 µm grain	Till a thickness of 35 µm
Step ●7e CMP	Till a thickness 25 µm
Step ●8 Cleaning step	In Acetone and Isopropanol
Step ●9a Adhesion agent	Ti Prime
Step ●9b Photoresist	AZ9260
Step ●9c Exposing & Developing	Backside lithography
Step ●10 Through trench etching	Tegal 901 Dry etching
Step ●11 Lift-off	Overnight Isoprop 80 °C bath
Step ●12 Cleaning	In Acetone and Isopropanol

Table 9.2: Chosen final substrate version

Process step	Substrate version #11
Step ●1 Wafer type	TiALTi oxide wafer
Step ●2 Polyimide layer 1	With photoresist AZ5214
Step ●3 Galvanic 1	Electroplating with large gold pads with Cr adhesion agent
Step ●4 Galvanic 2	Double exposing, electroplating with large gold pads
Step ●5 Polyimide layer 2	With photoresist AZ9260
Step ●6 Galvanic 3	Electroplating with large gold pads
Step ●7 Galvanic 4	Double exposing, electroplating with large gold pads
Step ●8 Polyimide layer 3	With photoresist AZ9260
Step ●9 Lift-off	Remove TiAlTi sacrificial layer with wet etching

10

Bonding the two-part implant

The two parts of the retinal implant has to be stacked on top of eachother using either the flip-chip bond method or via ball-wedge bonding. The first method is implemented first and will be discussed in this Chapter. For this project a Finetech bonder [10] is used. The implant will be bonded together in several steps:

- The polyimide substrate is placed on the bonding table and is picked up and rotated upward 90 degrees.
- The silicon dummy chip with the bonding glue (anisotropic or isotropic) already on it and aligned exactly to the substrate.
- When aligned, the arm swings slowly back down and presses with a predetermined force on the complete implant.
- After a certain amount of time the heating phase begins. The implant is heated with a maximum of 4 Kelvin per second to a given maximum temperature.
- The implant is kept at a constant temperature for a set time, in which also the pressure remains constant.
- After this the temperature is slowly lowered with a maximum of 3 Kelvin per second to the set base temperature.
- After the implant has reached this set temperature the arms swings slowly back up, releasing the pressure and the implant is bonded together.

Two different bonding glues are used in this project: the anisotropic Panacol Elecolit 3061 [36] or the isotropic Panacol Elecolit 414 [37]. The key difference lies in the conducting properties (anisotropic versus isotropic). Both glues can be placed on the gold pads with a dispenser. However, the isotropic glue is very thick and can also be placed manually on the chips gold pads using a small copper wire. The wire is dipped in the glue and then carefully pressed on the gold pads, leaving a small drop of glue behind on the pad. Other properties of the glues are compared and listed in Table 10.1.

Table 10.1: Comparing properties of Elecolit 3061 and 414 [36] [37]

	Elecolit 3061	Elecolit 414
Type	Anisotropic	Isotropic
Viscosity	35 000 - 45 000	20 000 - 25 000
Temperature Resistance	-40 to +180 °C	-50 to +200 °C
Curing time	10 seconds with 150 °C	300 seconds with 150 °C

Bonding

The implants were bonded using different procedures to try and evaluate the best method for bonding the silicon dummy chip to the polyimide substrate. The steps are summarized and explained below. Results of both Design 1 and Design 4 dummy implants, after flip-chip bonding, are shown in Figures 10.1 and 10.2.

- First, the anisotropic glue was utilised because of its attractive anisotropic feature. This meant no underfill was needed between the pads and the glue could be spread evenly between the substrates. Due to the force and heat of the bonding procedure, the few conducting particles should orient themselves and make a conducting pathway between the two opposing pads. However, it was found that after bonding there were hardly any working connections. It was, falsely, assumed that the glue did not work properly with the chosen settings and that there were not enough conducting particles to form a proper connection. The fact that some connections were really imperfect (in the order of several hundreds of Ohm's), this reasoning was even more confirmed. But, as was confirmed later, the through-connections of the polyimide substrate were faulty. Hence, the bonding procedure was probably working as advertised.

- Because of this reasoning that the anisotropic glue did not work, the isotropic counterpart was implemented. The glue needed less force but longer heat to bond. According to other projects, a bonding force of 0.5 to 1 Newton should be already sufficient to bond the implants together. However, after the low force and 5 minutes of curing time, the two-part implant did not bond properly and did not connect properly.

- It was thought that the higher surface area of this implant caused the bad connections. The other projects had far smaller implants that had to be bonded, hence a force of maximum 1 Newton was not enough. The force was increased between 5 and 10 N and the curing time also increased to 360 seconds. This resulted in chips that were bonded correctly to the polyimide substrate. The two parts could not be separated from eachother (without breaking either one).

- However, still not all connections were bonded firmly together. After looking under the microscope it was found that multiple substrate pads could be moved slightly up and down, while the bottom chip gold pads remained unmoved. Either the force was still not large enough to firmly press all pads together, or the varying amount of glue on the pads caused an inhomogeneity of force over the bonding places, or the bonding head (which presses on the implant) is not homogeneous. The latter was assumed to be also the case because it was noticed that most often the pads on one area were connected firmly, in contrast to the opposing area.

- To try and counter effect the proposed problems, several changes were made in the bonding procedure. Normally the force was released immediately after the implant was cooled to the room temperature. To make sure the implant is fully cooled before the arm is released, the cooling phase with force is increased by several minutes. Also the force is increased to 10 - 12 Newtons and the constant heating phase is increased to be more than 360 seconds. The two parts were now firmly bonded to the eachother.

Underfill

To relieve the possible bending stresses on the bonds, an underfill is used. This underfill is placed between the two implants to, ideally, form a uniform connection between the substrate and the chip (instead of only between the 16 bonding places). The employed underfill is EPOTEK 301 and consists out of two components that have to be mixed in a 4 to 1 ratio. After this, the mixture can hold op to two hours before hardening. This gives for plenty of time to prepare the substrates and implement the underfill. The underfill hardens easily in an oven within 1.5 hours on 85 degrees Celsius.
The first eight chip versions consisted out of the same large dummy chip with the exact same size as the substrate. The underfill could be placed between the two parts from either sides, however the substance did not reach all the way to the pads in the middle. The capillary effect of the very viscous fluid was apparently not strong enough. Slightly smaller chips or chips with a hole in the middle could deliver teh underfill more effective and evenly across the surface. If the substrate is smaller, the underfill could be administered on the edge, while still being over the chip. If that is tried now with this large design, the underfill will glue the implant to the glass substrate. The only option remains, if this problem is not overcome, to switch back to the

anisotropic glue and to cover the complete area with it. This option seems valid because it was later proven that the bad connection problems were not the fault of the anisotropic glue.
The Version 9 dummy chips are smaller and also less wide than the substrates, enabling for a more easy and efficient underfill process. The underfill can be administered via the four sides and the fluid is able to cover almost all the space between the implant (only the very middle area is not reached by the underfill). This is not ideal but this should give at least a good stress relieve when the implant is subjected to bending forces.

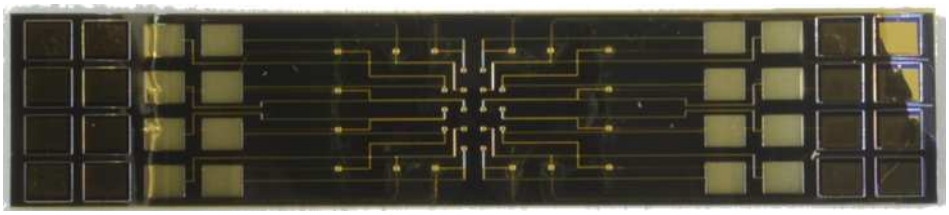


Figure 10.1: Design 1 result after flip-chip bonding.

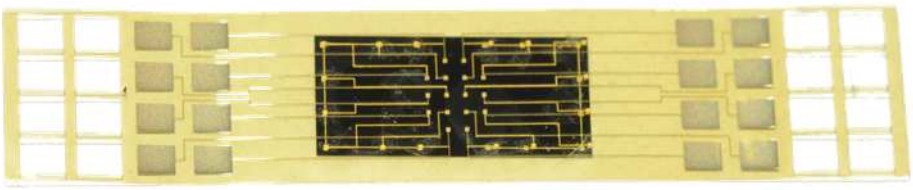


Figure 10.2: Design 4 result after flip-chip bonding.

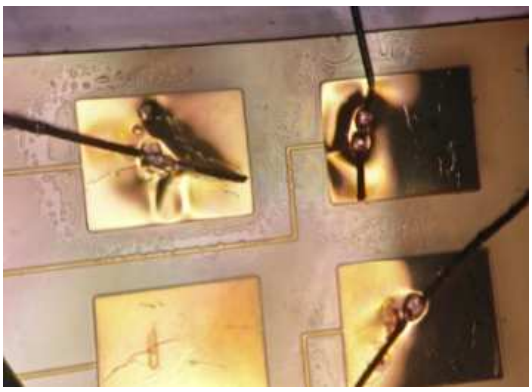
11

Mechanical stability and flexibility test setup

The two parts are successfully bonded together. The underfill ensures the stresses are distributed over the complete surface, in stead of localized on the 16 bonding pads. The condition of the through-connections during bending is tested with a four point bend test. To be able to measure the DC resistance in real-time during bending, cables have to be attached to the measure pads.

A 150 μm (isolated) copper cable is welded to the gold pads using a DC resistance welding system from Unitek Equipment [44]. The machine is equipped with three different modes: Current-driven, voltage-driven, and power-driven. Previous projects working with polyimide substrates already determined the most suitable mode to be voltage driven. The cable is placed on the pads and two small electrodes are pressed on the cable. A large current will flow through the electrodes (with the determined voltage of 0.400 V), welding the cable to the pad. Both materials are heated to such a point that the materials bond together. A force of 5 N is used to press the cable to the pad. A higher force caused damage to the implant. Figure 11.1 displays a microscopic view of some cables welded to the gold pads.

(a) Cable connecting to gold pad.



(b) Cables connecting to gold pads.

Figure 11.1: DC resistance welding cable to implant gold pads.

The implant is placed on a 3D printed structure with a opening in the middle. Figure 11.4a depicts the setup. The part is indicated by the letter A. The opening is 6 mm wide, where the implant will be bend and pushed down. The top part that pushes on the implant (letter B in Figure 11.4a), has a 2 mm slit in the middle. This slit enables for a more circular curvature of the implant. When pushing down on a single point in the middle of the implant, the implant would not bend in a curvature fashion but in a rectangular shape. The test starts by placing the implant on the structure (as shown in Figure 11.4a), and the top part is slowly moved down until a difference in force is measured. This will be the starting position. Now the top part is moved down in small incremental steps and the force is measured and automatically saved in an excel sheet. The iteration stops

when the maximum vertical distance has been achieved. An abrupt change in force indicates the implant is broken. The DC resistance is measured during bending to monitor the condition of the through-connections. Figure 11.2 shows an example a single measurement. The vertical axis shows the force that is pressed down on the implant. The force increases steadily, as the implant keeps bending downwards. At a certain point, the force is too great and the silicon dummy chip breaks. The remaining force is due to the fact that the broken chip is attached to the polyimide substrate, which is still absorbing part of the force.

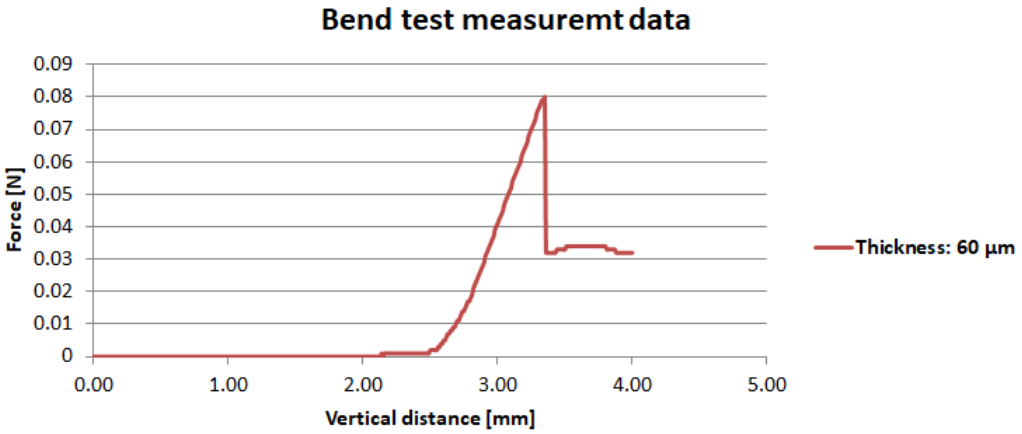


Figure 11.2: Example of a bend measurement.

The setup is run with Labview 2016 and all the different modules that make up the program for the bend test are given below. The different modules were written by Johanna Schiller at the IWE-1 institute Aachen and provided an excellent basis for testing the flexibility and mechanical properties of the implant. Figure 11.3 displays the program used for the bend testing. The program is divided into three sections (labeled 1, 2, and 3 in Figure 11.3.

- Before the program is ran, several parameters have to be entered. On the bottom left side of Figure 11.3, three parameters are given: 'Festklemmen' has to be set to true when the motor should first run slowly until the implant is pinched between the top and bottom part. From this moment, the measurement can begin. Without this module, the vertical distance includes the distance from the starting position until the top part reaches the implant (This means when bending the implant downwards 1 mm, the actual vertical distance will be less, due to this extra space). 'Biegerichtung' determines whether the chip is bend downwards or upwards. In this case, it is set to be true: downwards. The Comport number is needed to ensure a connection between the motor and the computer.
- The first part, drives the top part slowly downwards until a force difference is measured. This difference indicates the top part is now into contact with the implant. The measurement will start from this position.
- The second part is the actual bending of the chip. The motor slowly drives the top part down, the force is measured and the data (force and distance) is saved to an excel sheet. This procedure is positioned in a while loop and goes on as long as the maximum distance has not been achieved.
- After the measurement is complete, the motor position is reset to the original position (labeled 3 in Figure 11.3.

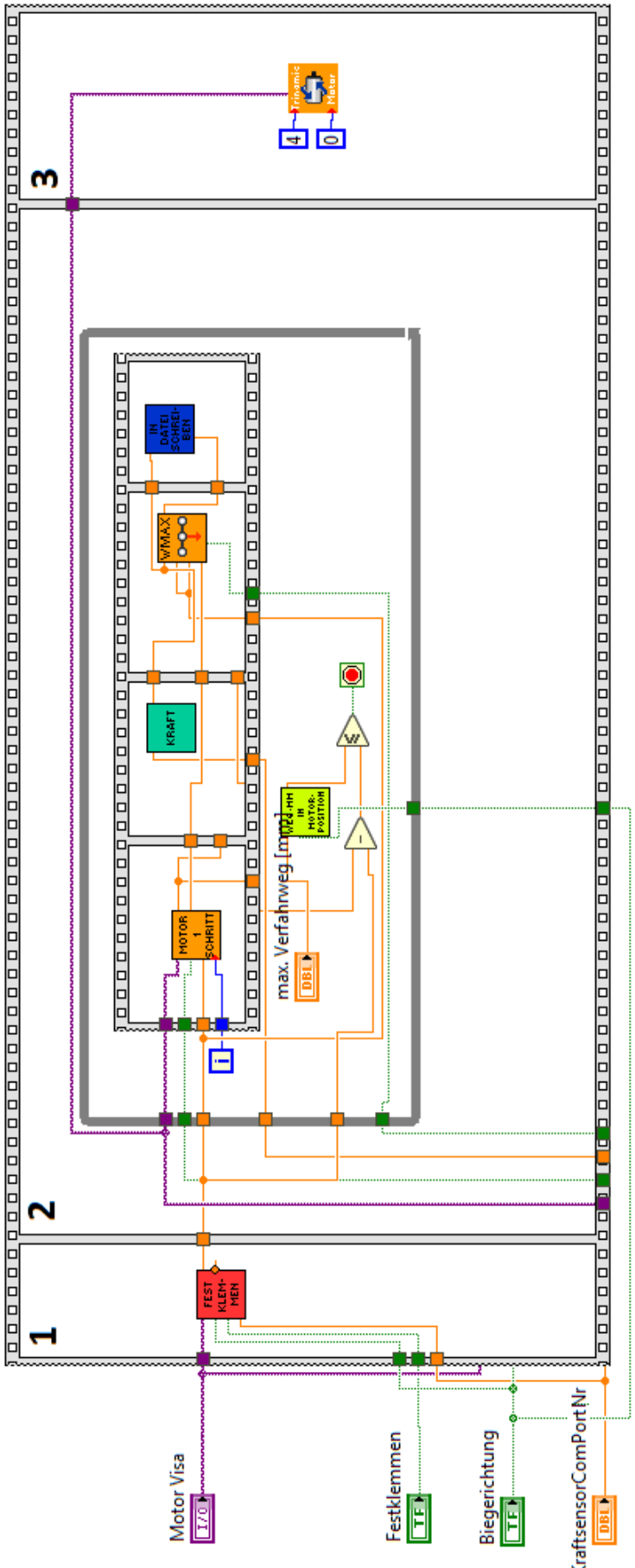
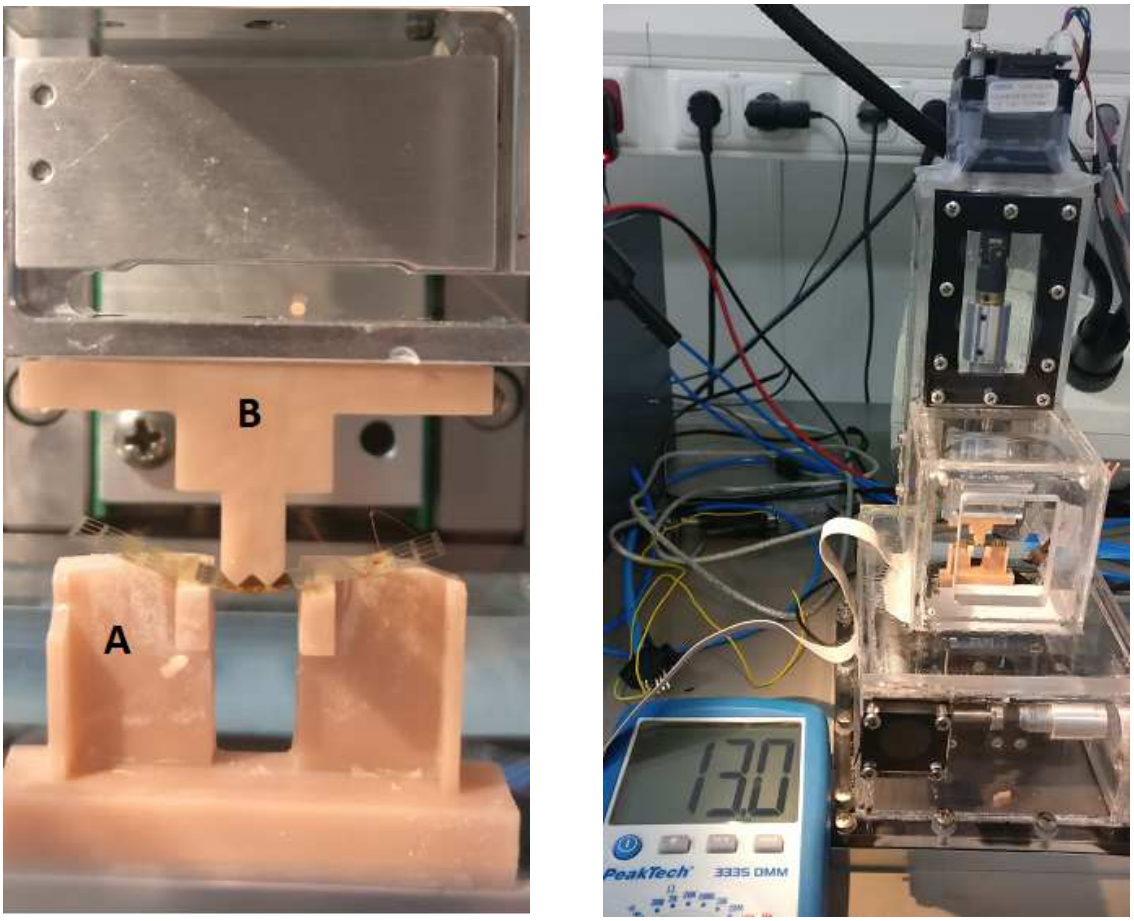


Figure 11.3: Labview overview.

The force on the implant will steadily increase until the chip cracks and the force suddenly drops down. During the entire measurement, the DC resistance of the through-connections is measured with a multimeter to determine the state of the connections. This setup is shown in Figure 11.4b. The resistance measured is, in this case, 13 Ohm. The chip is bend several times and the state of the connection is monitored.



(a) Detailed look of the bend test setup.

(b) Bend test setup with DC resistance measurement.

Figure 11.4: Bend test setup.

11.1. Linear beam theory

The implant is pressed down with two small electrodes. Due to the fact that the middle part of the implant is pressed even more downwards, the measured vertical distance is not the actual total distance. This property is displayed in Figure 11.5. To be able to retrieve the actual distance, this point is calculated using linear beam equations. The PhD proposal of R. Fischer implemented these equations and found the formula to calculate the maximum bend distance (taking the sliding of the implant along the outer contact points into account). In the equation, E is the E modulus, z is the measured vertical distance of the electrodes, b the width of the chip, F the applied maximum force, l the distance between the electrodes and h the total height of the implant. This maximum w_{max} is used and compared to the minimum bending distance of 0.4 mm mentioned in the design specifications.

$$w_{max} = z + \frac{3}{64}\frac{Fl^3}{Ebh^3} \tag{11.1}$$

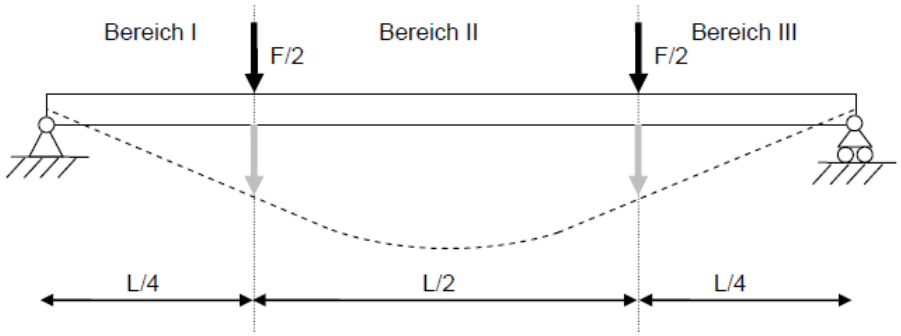


Figure 11.5: Schematic view of the bend setup [11].

12

Experimental results

Four different implant designs are fabricated. Wherein, Design 1 the only design with a large 24 by 5 mm dummy chip. Design 3 and 4 feature the new masks with larger gold pads, with the latter design implementing the gold sputtering technique. Two large determining factors showed that the most promising designs for this retinal implant dummy are Design 3 and 4. The smaller chip, in comparison to the polyimide substrate, helps the diffusion of the underfill after the bonding. Additionally, the larger gold pads enable for a higher number of valid through-connections. As already mentioned in the previous chapter, the chips will be bend until either the chips breaks or the DC resistance measurement a failed through-connection. The point where the chips breaks can be measured by looking at the distance-force output. If the chip breaks, a sudden drop of force on the implant is measured. This point of failure is also visually (and audibly) confirmed.

All measured through-connections, working before the measurements, survived the bend test multiple times. The DC resistance did not change over time, indicating the gold interconnect withstand the compression and shear forces occurring during bending. Due to the fact that 100% of the working through-connections stayed intact, this is not further graphically shown in this thesis. The other main aspect of the bend setup was determining the flexibility of complete retinal implant dummy. Measurements with the Design 3 and 4 implants were performed with each in several chip thicknesses (35 to 60 μm). The sample group of each design with its specific thickness was between 5 and 10. The results are averaged and displayed in Figure 12.1. Another distinction was made between the use of an underfill between the chip and the substrate and without underfill. Two linear lines can be seen in the figure, with the expected result that thinner silicon chips are more flexible and bend further downwards. The blue dotted line clearly shows the chips with the underfill, are able to handle a higher bending distances, confirming the theory that the underfill divides the pressure more evenly across the entire implant dummy.

Figure 12.2 shows the importance of the underfill once more. As already stated before, applying the underfill evenly between the large chip and substrate (Design 1) was not possible. The underfill did not reach to middle part of the dummy. In Design 4, with the smaller chips, this was not the problem and the underfill could be dispersed completely. This difference was clearly noticed during the bend results, as depicted in Figure 12.2. The large chips, with no underfill in the middle of the chips, show no noticable difference between the measurements with and without underfill. However, with the small chips, the applied underfill made a large differences by improving the mechanical flexibility of the total structure by almost 25%.

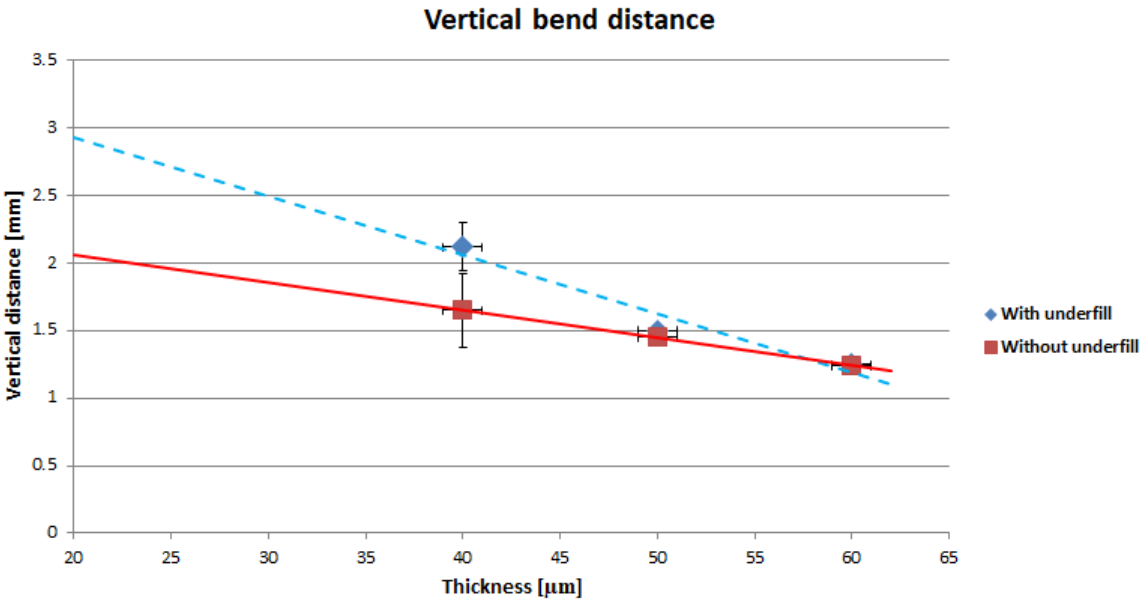


Figure 12.1: Average maximum vertical bend distance of implants with different chip thicknesses.

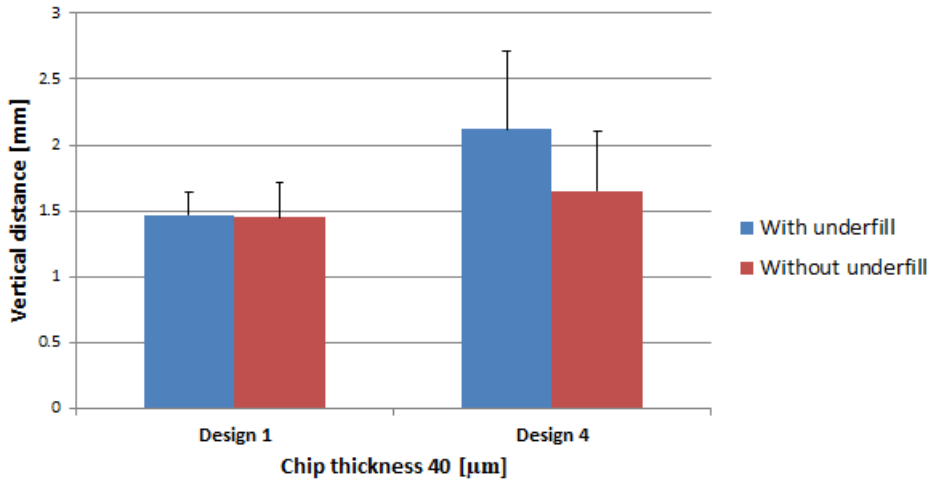


Figure 12.2: Design 1 (large dummy chip) and Design 4 (small dummy chip) results.

13

Conclusion

This project was part of the research project named OPTOEPIRET at the RWTH Aachen. The main goal was to fabricate a flexible substrate with through-connections and a corresponding thinned chip that can be bonded together. The total implants flexibility properties and the state of the through-connections were tested with a bend test setup that measured the bend radius, applied force and DC resistance of the gold interconnect.
The fabrication of this dummy retinal implant can be divided into four groups, that will be listed separately below.

The dummy chip consisted of a silicon base material with gold interconnect on top. The main difficulty in manufacturing the thinned chips was the homogeneity problems. Placing the wafer on the glass substrate without a protective layer ensured a good adhesion between the both, and the wafers did not crack anymore when they were thinned. Thinning and polishing with a high precision and homogeneity resulted flexible chips which did not break instantly when some force was applied to them. Etching the trenches, to isolate the chips, after the thinning step was found to be the ideal situation. With the sometime in-homogeneous dry etching, the trenches could now be freed without the need to constantly check the precise depth.

The fabrication of the polyimide substrate was more complex than presumed. The use of the correct adhesion agent to ensure the gold pads don't fall out when the substrate is released from the wafer via wet etching is crucial. However, the most important discovery in manufacturing the polyimide substrates was the connection between the pads and paths. When the masks of the polyimide holes and the corresponding golds pads are of equal size, the actual polyimide hole will be larger and leaving a trench between the two materials. This trench, in combination with possible left-over photoresist during the lithography step, often resulted in faulty through-connections in the substrate. The problem could be solved by increasing the size of the gold pads and double exposing the photoresist to ensure all the photoresist was exposed and could be developed properly. Switching from electroplating to gold sputter deposition to create the gold interconnect solved the difficulties between the gold pads and paths. Unfortunately, the adhesion of the gold to the polyimide was not optimal in this version, causing some gold interconnect 'flowing away'. In the future, this method should work when ensuring a good adhesion by following the same pretreatment steps as with the regular electroplating method.

Bonding the two parts together resulted finally in a proper connection between the silicon chip and the polyimide substrate. Dispensing small isotropic glue (Elecolit 414) on the silicon pads and bonding it to the substrate at a temperature of 150 degrees Celsius for more than 360 seconds resulted in a solid bond between both parts. The underfill ensured the stresses during bending were evenly spread across the complete surface and not only on the 16 bonding points, minimising the risk of implant fracture.
Normally the implant will be encapsulated in the bio-compatible material Parylene C. Because this implant was only for testing purposes, this was not done here. Wires were welded to the implant measure pads and the DC resistance and distance to break were measured with the bend test setup. Results showed the through-connections stayed intact, even far beyond the breaking point of the silicon chip. The DC resistance measured before, during and after the bend tests did not show any variation, indicating the gold interconnect is not affected during the test. The complete implant should be able to withstand bending downwards to at least 0.7

mm, conform the curvature of the human eye. This means the middle of the 8 mm implant has to be pressed down at least this distance. A certain margin is wished for, due to the possible bending during implantation. Hence, the measured distances of 1.5 to 2.0 mm are very promising. This showed that it is indeed possible, with the equipment at the IWE1 institute, to fabricate flexible thin silicon chips. The use of an underfill, as shown in the previous chapter, is highly recommended as it increases the overall flexibility of the implant dummy.

To conclude, this project was able to develop a process, and fabricate an epiretinal dummy implant with through-connections in the polyimide substrate that featured high enough flexibility properties needed for eye implantation. This research will be continued and implemented in the development of the OPTOEPIRET implant with the actual chip and layout and hopefully, someday, be implanted in humans to restore their field of vision.

14

Discussion

This thesis project ended in May 2018. The project continues and several versions are still being fabricated, as well as the real implant designs of the final OPTOEPIRET implant (the flower-like design). Although all the goals were achieved in this project, there are still some future recommendations for this project.

The first recommendation is to have each implant labeled on the wafer. This is extremely useful in case it is needed to know the specific location of the substrate on the wafer. During this project it was often noticed that certain through-connections were faulty. However, some substrates on the wafer (with a total of 26 substrates per wafer) had a high percentage of viable connections, which now had to be marked by hand. After lift-off, all substrates look the same otherwise and the orientation is unknown due to the axial symmetry. The substrates were now marked with small isotropic drops in a 5-bit sequence to mark the orientation and number of the substrate. An imprinted labeling system on the substrate would therefore be a large improvement, and as of the real OPTOEPIRET designs, this recommendation is already been included into the designs. Additionally, a larger contact area between the pads and paths is advised. Now the 120 μm pad connects to the 20 μm wide gold path. This small contact area was often faulty. Newer designs should feature, for example, a more diagonally transition between the pad and path, increasing the contact area.

Dry etching in the Tegal 901 and mechanical thinning with the Logitech LP50 was not homogenous enough for a project that needs such thin chips. A deviation of a few micrometers, when a total thickness of 25 μm is wished for, is not wished for. Solving the problems by changing grinding heads, plates, materials and speed, solved some of the thinning problems but a deviation of several micrometers was always present. A system that would allow for a more homogeneous mechanical grinding without the need to constantly check the removal rate and homogeneity would be an advantage. Also, the anisotropic dry etching of the wafer to open all the trenches should be able to be more homogenous. At the end, it did not result in large problems with the chips, but it increased the fabrication time (and number of wafers) considerably. In the cleanroom, another dry etching device is available (Rie 80). This machine has, apparently, a slower removal rate but could be worth investigating whether it has a more favorable homogeneity. Either way, it can be of a great addition to investigate a method to achieve a homogeneous removal rate with dry etching.

Another improvement would be to have either a hole in the polyimide substrate or have smaller substrate dimension as the dimensions of the chip. In this case it is possible to insert the underfill liquid more effective between the two parts of the implant. The fluid has a high capillary effect but it did not reach all the way to the middle in the first designs (with the same chip and substrate size). This resulted in having the underfill everywhere, except at the places around the bonding connections, where the fluid is most needed. The version with the smaller, and slightly less wide chips, were favored due to the fact that the underfill could be easily dispensed via the sides of the implant. The distance the underfill had to travel was smaller. Hence, it was able to reach the complete surface.

Due to the fabrication problems of the polyimide substrates and the time restraints, the two different path versions on the chips were not tested thoroughly. One version featured round edges in the paths on the substrate and chip, as the other had sharp 90 degree edges. Although no apparent difference was noticed and both connections were able to withstand the stresses, the difference in the two has not yet been investigated. It is presumed that the sharp corners find higher stresses and will be more likely to break. At the other hand, gold is relatively flexible and the thin gold layer should not form any problems when it is exposed to the bending forces (as was shown in this project). The limiting factor, in terms of flexibility, will always be the relatively stiff silicon chip. Especially if the chip is not extremely thin, as was in this project (around 40 - 50 μm). The substrates were able to withstand any kind of stress (even twisting and rolling the device in a circle, far more than 360 degrees), as for the chips, they would only withstand bending them several millimeters at most. For future projects, a method for thinning the chips (homogeneously) even further to the desired 25 μm is needed. Due to the in-homogeneity problems, this was now utmost difficult and therefore the chips were slightly thicker.

This research in the fabrication of a retinal implant dummy with through-connections was used to write a 5 page abstract paper for the 22th International Student Conference on Electrical Engineering "Poster 2018", which will be held on 10th of May. The poster and paper is included in Appendix L

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A

Retinal implant positions in retina

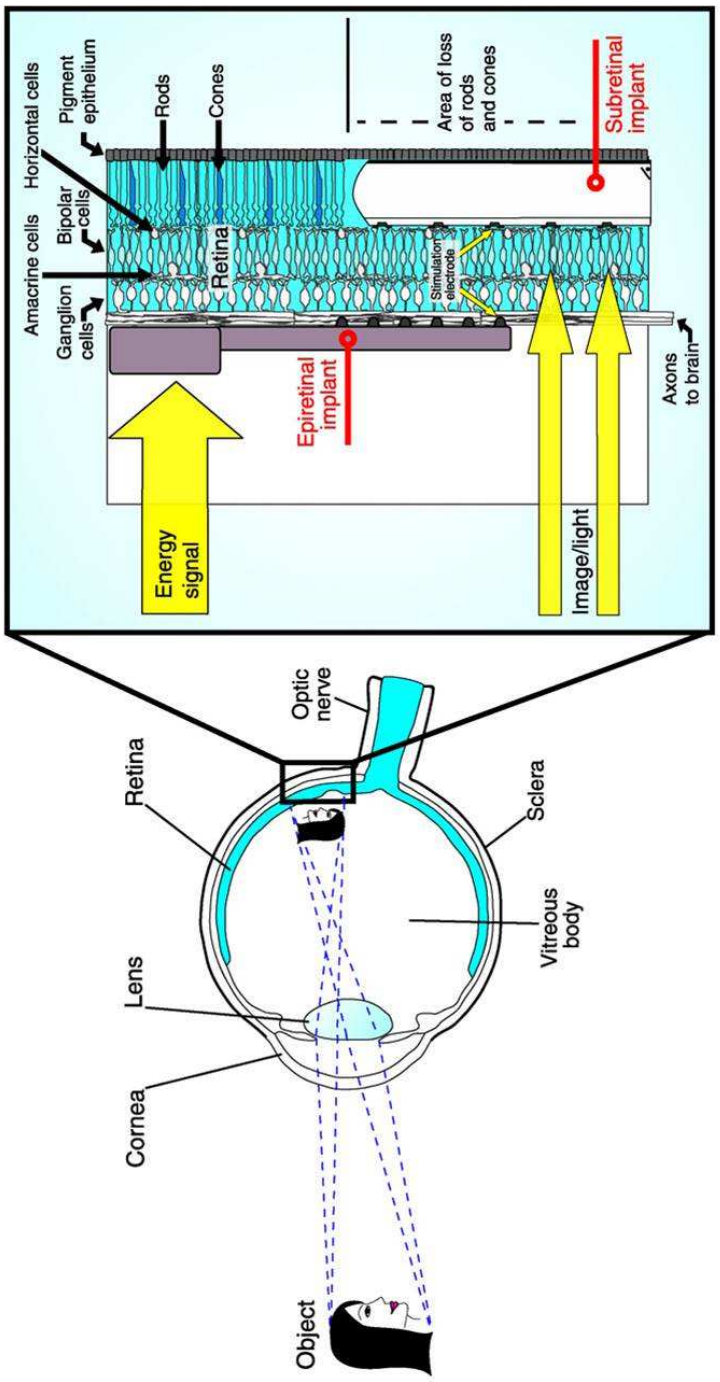


Figure A.1: Epiretinal and subretinal implant location in the retina layers [46].

B

Masks for the polyimide substrate

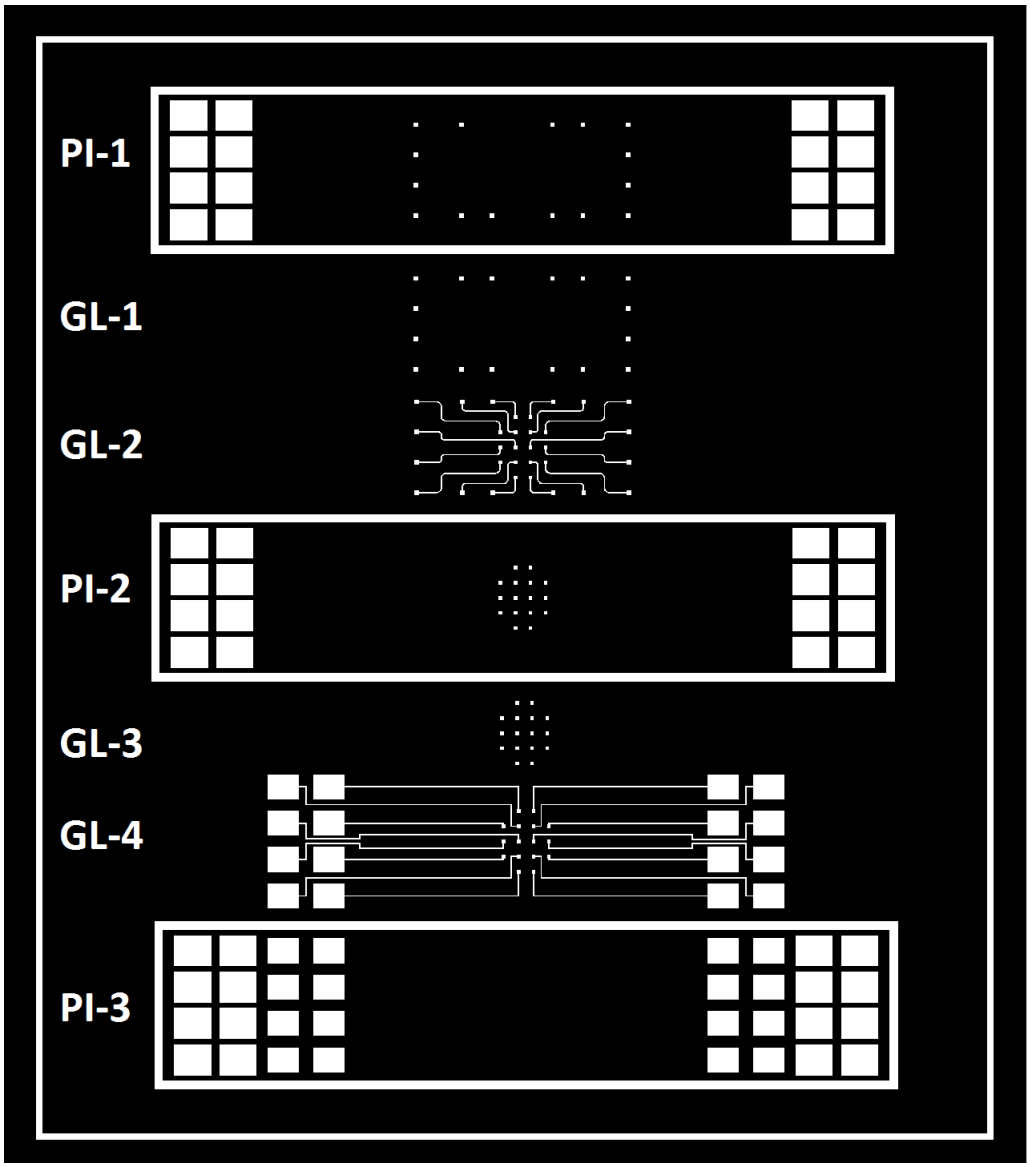


Figure B.1: The seven masks for the different substrate layers

C

Wafer overview in AutoCAD

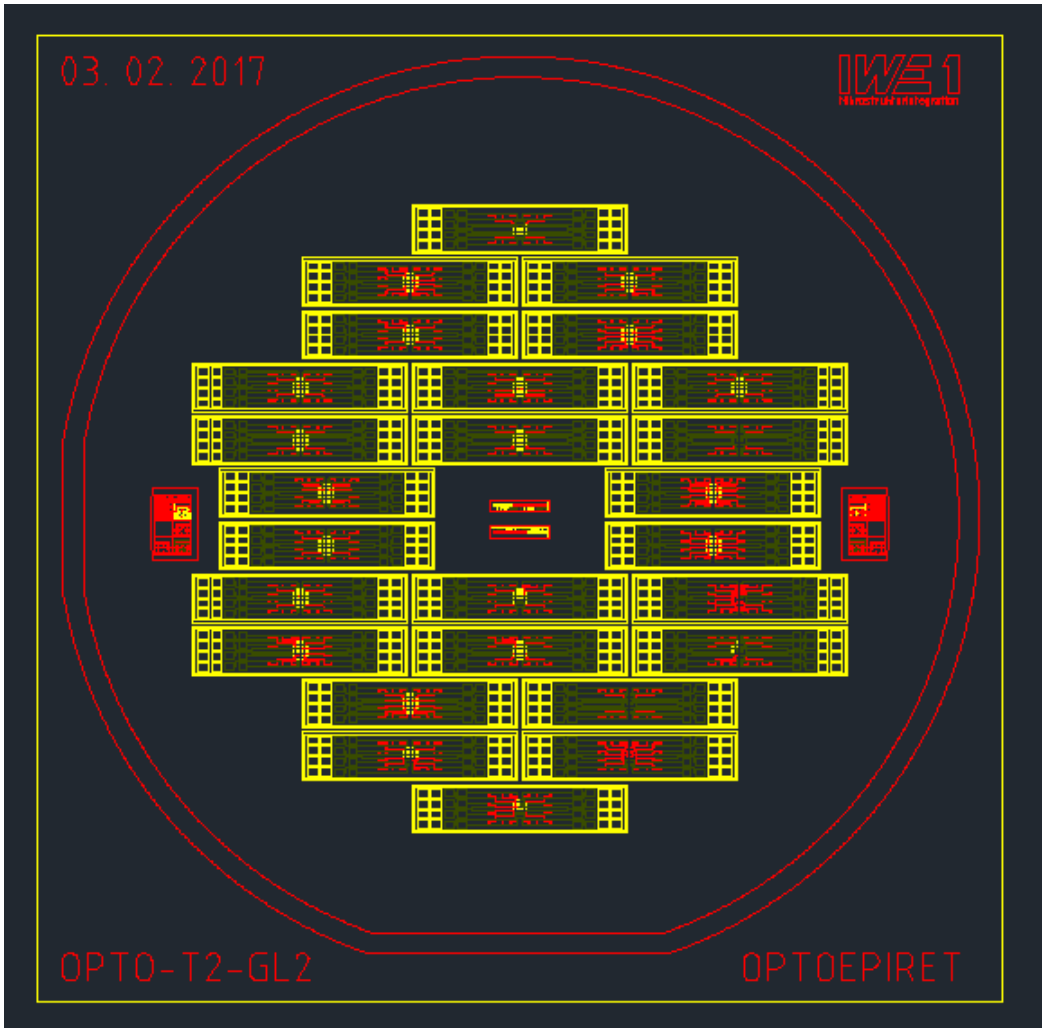


Figure C.1: Complete overview of the AutoCAD wafer layout.

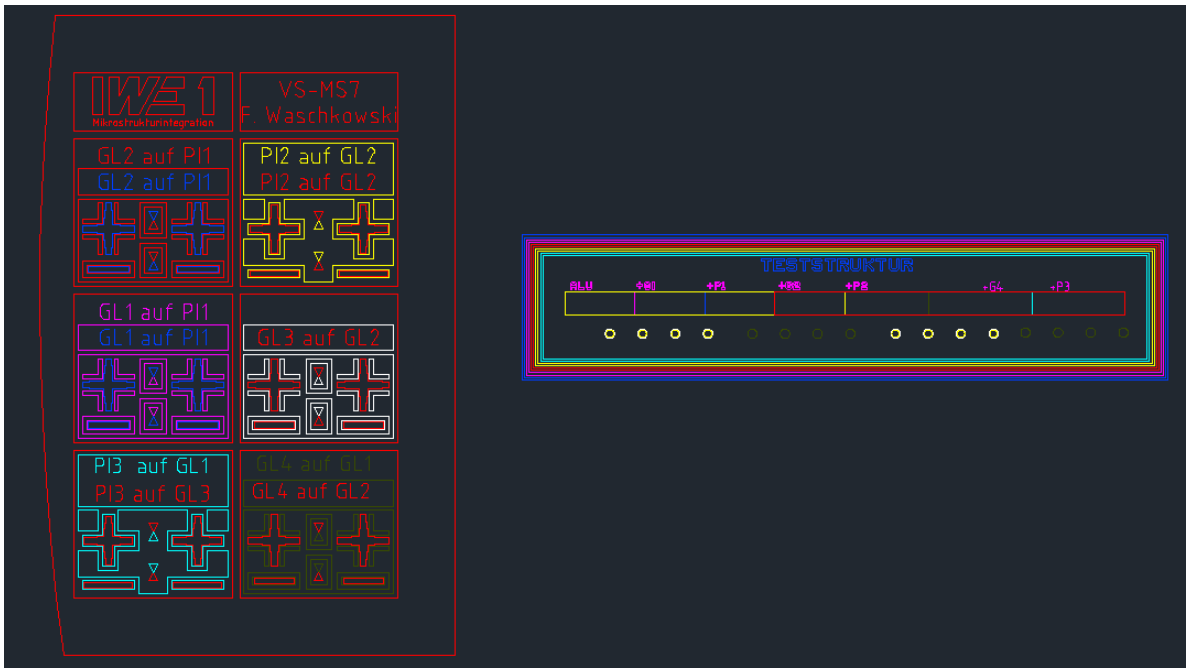


Figure C.2: Alignment structures to align the wafer and the current mask perfectly during the lithography.

D

Dummy chip fabrication steps: Trenches first

Table D.1: Version #2 - 5 of the Dummy chips. The trenches were etched **before** thinning.

#	Process step
	Modul 1: Select wafer type (4 or 8 wafers)
Nr. ●1	Wafer selection: oxidised silicon 4-inch wafer
	Modul 2: Standard Fotolack AZ5214 or AZ9260
Nr. ●2	Vorbehandlung Plasmastripper
Nr. ●3	Vorbehandlung Hotplate
Nr. ●4	Beschichtung Fotolack
Nr. ●5	Prebake Fotolack
Nr. ●6	Randenentlackung
Nr. ●7	Prebake Randentlackung
Nr. ●8	Belichtung Fotolack
Nr. ●9	Entwicklung Fotolack
Nr. ●10	Kontrolle Strukturierung Fotolack
	Modul 3: Standard Goldgalvanik
Nr. ●11	02-FLash
Nr. ●12	Gold-Galvanik
Nr. ●13	Kontrolle Gold-Galvanik
Nr. ●14	Entfernung Fotolack
Nr. ●15	Messung Golddicke und Rauhighkeit
	Modul 4: Entfernung Plating-Base
Nr. ●16	Vorbehandlung Plasmastripper
Nr. ●17	Nassätzen Gold-Plating-Base
Nr. ●18	Kontrolle Nassätzen Gold-Plating-Base
Nr. ●19	Nassätzen Chrom-Haftvermittler
Nr. ●20	Kontrolle Nassätzen Haftvermittler
	Modul 5: Standard Fotolack AZ5214 or AZ9260
Nr. ●21	Vorbehandlung Plasmastripper
Nr. ●22	Vorbehandlung Hotplate
Nr. ●23	Beschichtung Fotolack
Nr. ●24	Prebake Fotolack
Nr. ●25	Belichtung Fotolack
Nr. ●26	Entwicklung Fotolack
Nr. ●27	Kontrolle Strukturierung Fotolack
	Modul 6: SI02 öffnen
Nr. ●28	HF schritt
Nr. ●29	Wafer spülen
Nr. ●30	Entfernung Fotolack
Nr. ●31	Plasmareinigung
Nr. ●32	HF-Dip
	Modul 7: Standard Si anisotrop ätzen Tegal
Nr. ●33	Si anisotrop Tegal (gräbentiefe 25-50 µm)
	Modul 8: Entfernung Fotolack
Nr. ●34	Reinigung
	Modul 9: Sägeschutzlack AZ9260
Nr. ●35	Beschichtung mit Fotolack
	Modul 10: Dünnschleifen
Nr. ●36	Glassubstrat einseitig einschleifen
Nr. ●37	Waferdicke messen
Nr. ●38	Wafer auf Trägersubstrat aufbringen und Sandwichdicke messen
Nr. ●39	Läppen (15 µm)
Nr. ●40	Läppen (9 µm)
Nr. ●41	CMP
	Modul 9: Standard Si anisotrop ätzen Tegal
Nr. ●42	Si anisotrop Tegal (bis chips frei)

E

Dummy chip fabrication steps: Thinning first

Table E.1: Version #6 - 9 of the Dummy chips. The trenches were etched **after** thinning.

#	Process step
	Modul 1: Select wafer type (4 or 8 wafers)
1	Wafer selection: oxidised silicon 4-inch wafer
	Modul 2: Standard Fotolack AZ5214 or AZ9260
2	Vorbehandlung Plasmastripper
3	Vorbehandlung Hotplate
4	Beschichtung Fotolack
5	Prebake Fotolack
6	Randenentlackung
7	Prebake Randentlackung
8	Belichtung Fotolack
9	Entwicklung Fotolack
10	Kontrolle Strukturierung Fotolack
	Modul 3: Standard Goldgalvanik
11	02-FLash
12	Gold-Galvanik
13	Kontrolle Gold-Galvanik
14	Entfernung Fotolack
15	Messung Golddicke und Rauhighkeit
	Modul 4: Entfernung Plating-Base
16	Vorbehandlung Plasmastripper
17	Nassätzen Gold-Plating-Base
18	Kontrolle Nassätzen Gold-Plating-Base
19	Nassätzen Chrom-Haftvermittler
20	Kontrolle Nassätzen Haftvermittler
	Modul 8: Dünnschleifen
21	Glassubstrat einseitig einschleifen
22	Waferdicke messen
23	Wafer auf Trägersubstrat aufbringen und Sandwichdicke messen
24	Läppen (15 µm)
25	Läppen (9 µm)
26	CMP
27	Reinigung
	Modul 5: Standard Fotolack AZ5214 or AZ9260 (**backside**)
28	Vorbehandlung Hotplate
29	Beschichtung Fotolack
30	Prebake Fotolack
31	Belichtung Fotolack
32	Entwicklung Fotolack
33	Kontrolle Strukturierung Fotolack
	Modul 6: Gräben öffnen
34	Trockenätzen Tegal bis gräben frei
	Modul 9: Dünne Chips ablösen
35	Ablösen der Chips vom Glasssubstrat
	Modul 9: Entfernung Fotolack
36	Reinigung

F

Polyimide substrate fabrication steps

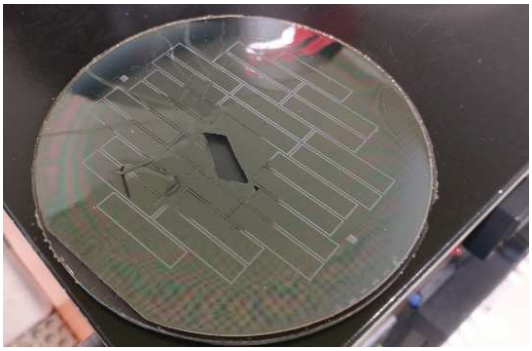
Table F.1: List of Polyimide substrate fabrication steps.

Step	Process step	Thickness	Additional information
	Wafer type		
Step 1	TiAlTi Silicon oxide wafer	500 µm	Base layer to build substrate on
	Polyimide 1		
Step 2	Standard Polyimide	5 µm	**First layer**
Step 3	Photoresist layer AZ5214	8 µm	Mask for structuring substrate
Step 4	Exposing & developing photoresist		AZ726 solution
Step 5	Hard bake Polyimide		400 degrees Celsius
	Galvanic 1		
Step 6	Vapor deposition: gold	100 nm	Electrical contact for galvanic step
Step 7	Adhesion agent: chrome	30 nm	Adhesion silicon oxide to gold galvanic
Step 8	Photoresist layer AZ9260	8 µm	Mask for galvanic
Step 9	Exposing & developing photoresist		AZ400K:H20 solution
Step 10	Standard Gold-galvanic	2 µm	Electroplating pads
	Galvanic 2		
Step 11	Photoresist layer AZ9260	8 µm	Mask for galvanic
Step 12	Exposing & developing photoresist		AZ400K:H20 solution
Step 13	Standard Gold-galvanic	5 µm	Electroplating paths
Step 14	Wet etching Gold-Plating-Base		HNO3:HCL = 1:3
Step 15	Wet etching Chrome adhesion agent		15g KOH + 15g Kaliumhexacyanoferrat III + DI Water
	Polyimide 2		
Step 16	Standard Polyimide	5 µm	**Second layer**
Step 17	Photoresist layer AZ9260	8 µm	Mask structuring substrate
Step 18	Exposing & developing photoresist		AZ400K:H20 solution
Step 19	Hard bake Polyimide		400 degrees Celsius
	Galvanic 3		
Step 20	Vapor deposition: gold	100 nm	Electrical contact for galvanic step
Step 21	Adhesion agent: chrome	30 nm	Adhesion silicon oxide to gold galvanic
Step 22	Photoresist layer AZ9260	8 µm	Mask for galvanic
Step 23	Exposing & developing photoresist		AZ400K:H20 solution
Step 24	Standard Gold-galvanic	5 µm	Electroplating pads
	Galvanic 4		
Step 25	Photoresist layer AZ9260	8 µm	Mask for galvanic
Step 26	Exposing & developing photoresist		AZ400K:H20 solution
Step 27	Standard Gold-galvanic	5 µm	Electroplating paths
Step 28	Wet etching Gold-Plating-Base		HNO3:HCL = 1:3
Step 29	Wet etching Chrome adhesion agent		15g KOH + 15g Kaliumhexacyanoferrat III + DI Water
	Polyimide 3		
Step 30	Standard Polyimide	5 µm	**Third layer**
Step 31	Photoresist layer AZ9260	8 µm	Mask structuring substrate
Step 32	Exposing & developing photoresist		AZ400K:H20 solution
Step 33	Hard bake Polyimide		400 degrees Celsius
Step 34	Remove TiAlTi sacrificial layer		Ti and Al wet etching

G

Tegal 901 plasma etching

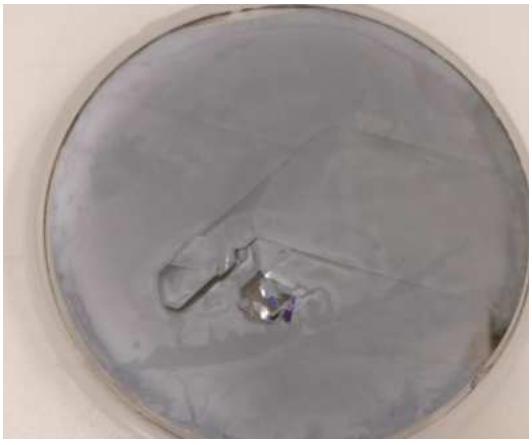
(a) The thin wafer cracks under the pressure differences.



(b) The in-homogeneity of the Tegal 901.

Figure G.1: Cracked wafers during plasma etching.

(a) Trenches manually masked with photoresist for protection during further etching.



(b) The extremely thin wafers with poor adhesion to the substrate crack due to the large surface tension.

Figure G.2: Tegal 901 results of extremely thin wafers. Homogeneity and tension problems.

H

Dummy chip step detailed process

H.1. Plating-base on oxidised silicon wafer

A silicon oxide layer has to be used when depositing galvanic layers on the wafer. To insure the gold deposition holds to this silicon oxide, an adhesion agent is used (30 nm Chrome is coated on the wafer). The material is thin and a good conductor (not as good as gold but still well within this projects targets), this layer will not be removed under the gold-plated areas. The rest is removed via a wet-etching process. This process uses a basic pH solution of 15g KOH + 15g Kaliumhexacyanoferrat III + 300ml DI-water. After roughly 120 seconds, the wafer color changes from silver to gray, giving a clear moment when the chrome layer is removed and the etching step is complete.
The gold electrodes grow during the galvanic deposition process on predetermined areas. To manage this, a very thin gold layer is deposited on the complete surface (the plating base). After the mask has been applied, gold grows from the gold surfaces connected to the anode. The process of galvanic deposition is further explained in Appendix H.3.

H.2. Applying and exposing photoresist layer

To fabricate multiple chips and objects on a wafer, a mask is needed that covers parts of the wafer during the exposing step. There are two photoresists used in this project:

- Photoresist AZ5214 [24]: The AZ5214 is a photoresist used in the cleanroom at the IWE-1 institute when very fine details are not necessary (less than 10 μm). The properties and results for relative large structures are almost identical as for the AZ9260 resist.

- Photoresist AZ9260 [25]: is a positive photoresist that is suitable for thicknesses between the 5 and 20 μm. It is sensitive in the 310 - 410 nmUV spectrum. The advantage in comparison to the AZ5214 is that it has a lower optical absorpion, which simplifies exposure of thick resists. At the IWE-1 institute in Aachen this resist is most commonly used because of the ability for higher detail. This photoresist is able to develop more finer details than the above mentioned.

The photoresist is spincoated on the wafers with the so-called 'Lackschleuder RC 8'. A pre-set program can be selected that enables for a resist thickness of 8μm+- 1.5 μm. As the structures in the OPTOEPIRET designs do not have finer details than 10 μm, both resists can be used. However, AZ5214 is the current standard for the first masks, due to the absence of structures on the wafer. After the first polyimide layer, AZ9260 is used.
After the photoresist is coated on the wafer, the wafers are loaded in the Karl Suss MA6/BA 6. This device exposes the wafer to UV light. The device used in the IWE-1 cleanroom has a intensity of 12 mW/cm2. The total dose of normal structured wafers is 480 mJ/cm2, which results in a total time of 40 seconds. Figure H.1 shows how the wafer is aligned to the mask. The dark black outlines (alignment structures) on the figure are the mask. To perfectly align the wafer, the inner cross should be as good as possible positioned inside the black outlines. Because the dummy chips (and polyimide substrates) consist out of various layers, multiple alignment structures are placed on the wafer such that always one structure is visible. Figure C.2 in Appendix C depicts this. For every layer there is a description. This image is for the fabrication of polyimide substrates,

hence there are so many alignment structures (due to the high number of layers). It can be seen that Figure H.1 shows the second galvanic layer (top of figure).
The aligning is done manually at the RWTH IWE-1 cleanroom. The more precise the alignment step is executed, the better the mask will be on the wafer and the sharper (and more precise) the edges and borders of the structures will be. Hence, it can take some time to manually align every wafer. To further improve the manual aligning, multiple alignment structures are on the wafer, as can be seen, once again, in Figure C.2 in Appendix C.

Figure H.1: Aligning the wafer to the mask before exposing.

After aligning and exposing, the wafers are placed in a so-called developing solution to remove the exposed photoresist. After this step, the wafer is ready to receive the next layer (Galvanic or polyimide for example).

H.3. Galvanic deposition

The gold interconnect and electrodes are grown on the wafer via the electroplating technique. This technique uses a gold saturated bath where the wafer is placed in. The anode is connected to the wafer, attracting the positive gold ions. The current between the anode and cathode determines the rate at which the gold grows on the wafer. A typical current for the wafers used in this project is 9 mA. Figure H.2 shows that a seed layer (plating base) is needed. The gold only grows on the areas where there is already a conducting surface (connected to the anode). This seed layer in combination with the mask assures the gold only grows at predetermined areas.

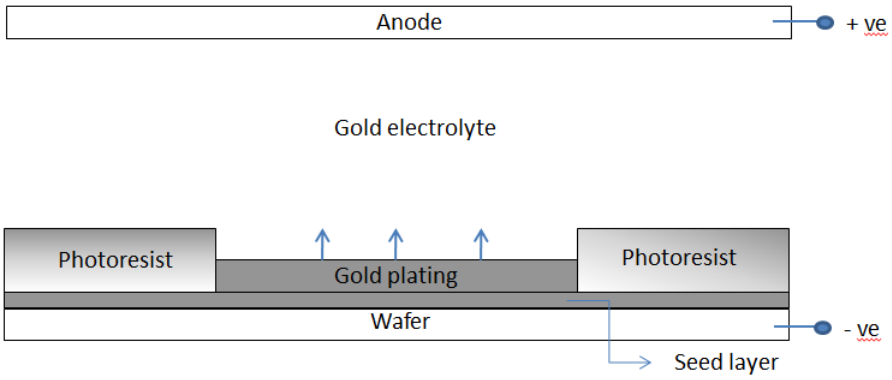
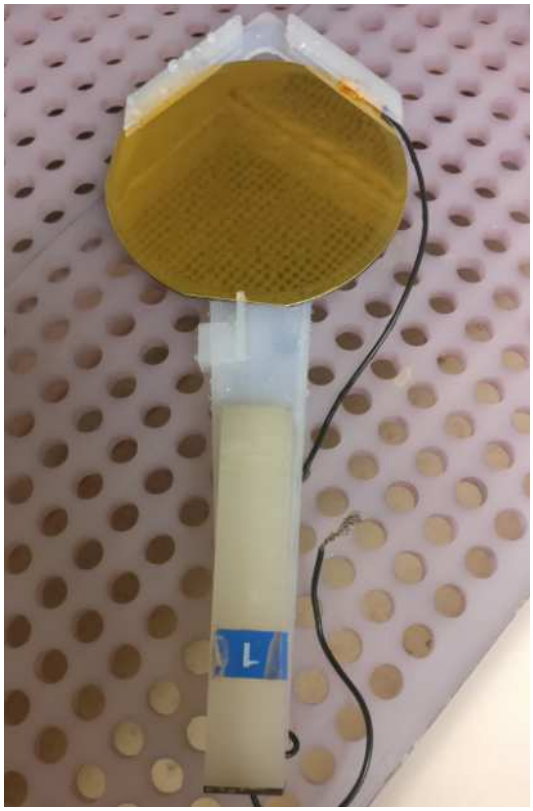


Figure H.2: Electroplating procedure.



(a) The anode is squeezed on the wafer. At this place the photoresist is removed to ensure a connection to the gold plating base.

(b) The galvanic setup. The wafer is placed in the bath. Once the cathode and anode are connected, the gold deposition is beginning. The wafer is moved up and down in the bath to ensure an even gold growth over the wafer.

Figure H.3: The galvanic setup.

H.4. Glass carrier

Thinning the wafers until a final thickness of 25 µm is difficult because the silicon changes properties below a 100 µm thickness. To improve handling, the wafers are glued on a glass substrate. This substrate is between 3 and 5 mm thick, making the entire package easier to handle and less fragile. However, every thinning head and thinning plate has it's own shape (convex or concave). This means that if a perfect homogeneous glass substrate is used, the first thinning is not homogeneous throughout the wafer. The thinning head grinds with a certain angle on the plate, thinning at different speeds throughout the wafer (See Figure H.5 for the LP50 thinning machine, and H.6 for what happens if the glass substrate is not first matched to the grinding plate). To make sure the thinning is homogeneous, the glass carrier is ingrained first to match the thinning plate. This procedure takes about 30 to 90 minutes with AL2O3 15 µm grain size. This method is clarified with an image, shown in Figure H.4. The wafer and glass substrate are also marked on the side, to be sure they are always placed in the same orientation on the grinding head.

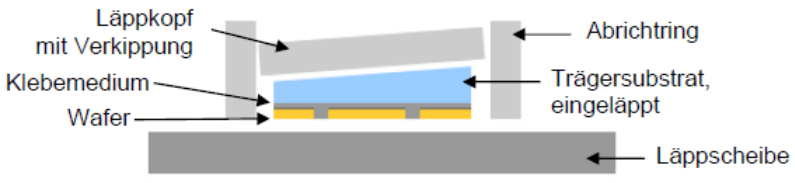


Figure H.4: Matching the inclination of the grinding plate [13].

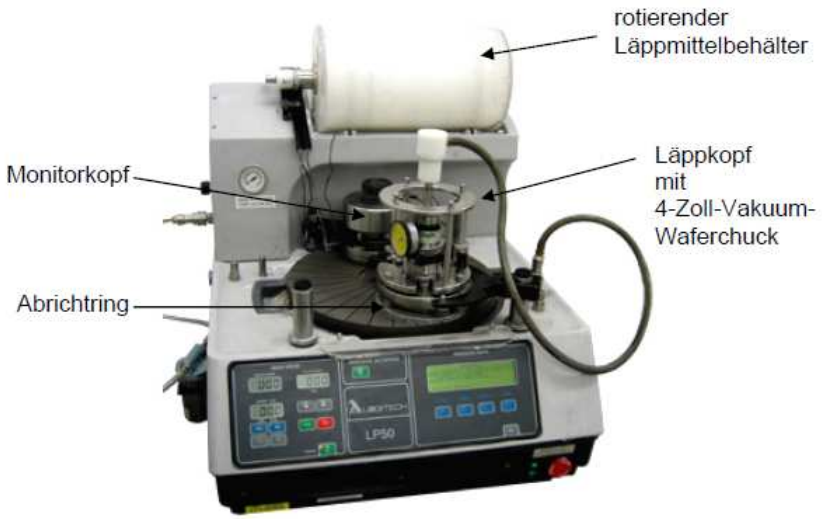


Figure H.5: The Logitech LP50 mechanical thinning device [43] [13].

Figure H.6: Grinding results if the glass carrier is not pre-grinded.

Before gluing the wafer on the glass carrier, both the wafer and carrier thickness are measured. This is important to know before thinning step, so it is known how much material can be removed with mechanical grinding. After this, the glass carrier is heated to around 110 degrees Celsius and the Quartz wax is spread out over the carrier. When the wax has melted and evenly spread across the carrier, the wafer is placed on the wax (with the active side on the wax). The whole setup is cooled slowly and placed under vacuum to ensure the best adhesion possible (Figure H.7). Further information and different processes tested in this project are listed below in the summation. In some cases, an extra protective photoresist was added on the active side to protect it from the wax. More on this subject can be found in Chapter 6.
Different steps were used to glue the wafer to the glass carrier. Figure H.10 shows a overview of the four different steps. A brief explanation of every step will be given below:

- The glass carrier has to match the inclination of the grinding plate. At first, this was done by thinning

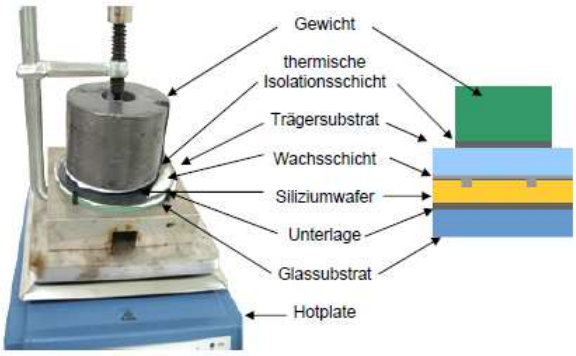


Figure H.7: Gluing the wafer with the active side to the glass carrier [13].

the wafer for 15 - 20 minutes. The removal rate seemed homogeneous after this. But because of the ongoing homogeneity problems, it was once tried to thin the wafers even further (roughly 90 minutes). It was found, as well as in other research groups at IWE-1 institute, that the removal rate was far more homogeneous when pre-grinding the carrier for over an hour. An example of the removal rate measurements is shown in Table H.1. It can be clearly seen that after a time of 60 minutes, the removal rate becomes very constant throughout the wafer.

- To protect the active side of the chips (gold electrodes and paths), a protection layer of photoresist was added. However, the adhesion of the photoresist to the wax layer was not optimal. This resulted in that the thinner the wafer became, the more air bubbles grew under the wafer, resulting in high surface tension and eventually breakage. It was thought that the protection layer was needed to ensure that the active side did not scratch when it was placed on the wax or released from it. Because at the first versions, some wafers did not receive a protective layer and they were scratch on the top surface (Figure H.8). The versions with the protection layer did not have such scratch (or significantly less scratches). But, because the adhesion was not good enough, it was chosen not to further implement this protection layer and gluing the wafer immediately to the glass carrier. From now on, the adhesion was perfect and no growing air bubbles were visible during the entire process. Extra care has to be given now when placing the wafer on the carrier and removing it, not damaging the active side of the chips.

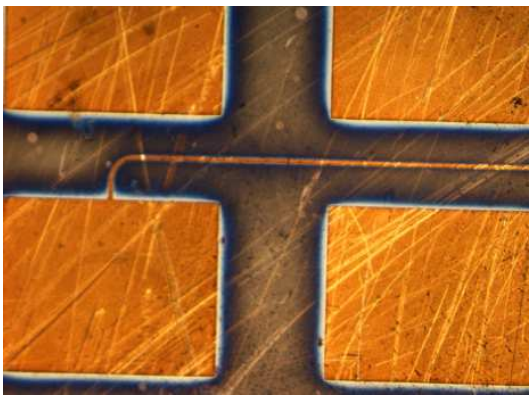
- The Quartz wax melts around a temperature of 80 degrees Celsius. To ensure the wax is completely liquid and spread out as homogeneous as possible, the temperature is held steady at 100-110 degrees Celsius. As already mentioned in Figure H.10, several techniques were used during this project. The first default method was placing the wafer on the liquid wax and letting it cool down under vacuum conditions. However, the vacuum was turned off immediately after the wafer was placed on the wax. The seals were not completely air tight, meaning the air pressure increased over time. The combination of the protective photoresist layer and the short time the wafer is heated on the wax resulted in a poor adhesion. Therefore, other combinations were tried with a perfect solution at the end: when the wafer is placed on the wax surface, the temperature is kept at 100 degrees for another 20 minutes. The vacuum is kept for at least 2 hours to ensure all the air is removed from the chamber and the wax layer during hardening of the wax. After this, the temperature is gradually decreased to room temperature and kept overnight. This technique yielded perfect adhesion of the wafer to the carrier.

H.5. Mechanical thinning

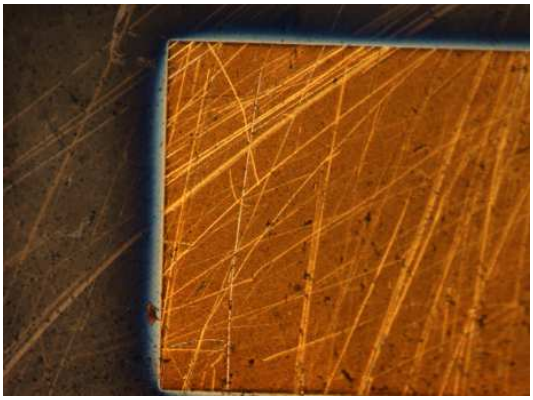
The LP50 machine itself is able to measure the condition of the plate. With an additional grinding head ('Monitorkopf' in Figure H.5), the machine detects whether the plate is convex or concave, and tries to correct for that by moving both grinding heads slightly to the middle or outside of the plate. Unfortunately the cable that is used for monitoring the condition of the plate was broken (this wasn't noticed at the beginning), causing the machine to overcompensate and making the plate even more concave. This made the grinding plate with slits useless, and a new grinding plate had to be used from then on out.
Aquaplaning effects are minimised by using the grinding plate with slits. Unfortunately the plate with slits was very concave and the removal rate was far from homogeneous (differences over 20 μm). Therefore, a new

Table H.1: Thinning rate of pre-grinding glass carrier

Wafer removal rate					
Time [min]	Top [µm]	Right [µm]	Bottom [µm]	Left [µm]	Differences [µm]
T = 0	-100	-109	-93	-85	24
T = 15	-20	-29	-31	-21	11
T = 25	-26	+1	-20	-51	52
T = 35	-31	-57	-34	-10	47
T = 45	-35	-34	-31	-30	5
T = 55	-16	+7	-16	-40	47
T = 65	-14	-16	-17	-14	3
T = 75	-16	-15	-15	-16	2
T = 85	-18	-20	-19	-20	2
T = 95	-9	-8	-8	-7	2
T = 110	-3	-2	-3	-5	3
T = 125	-2	-2	-2	-1	1



(a) Dummy chip.



(b) Dummy chip with higher magnification.

Figure H.8: Damaged chips when not carefully detached from glass carrier.

grinding plate was used for the next Charges. This plate did not have slits and the risk of aquaplaning was increased. After carefully regulating the abrasive flow, rotation speed and pressure, the removal rate was once again the same and very homogeneous. A good indicator is the black stripes on the grinding plate. The black color comes from the removed silicon particles. If the grinding plate only shows a white liquid, the user can see that there is no silicon removed from the wafer. A preview of this is shown in Figure H.9.

Figure H.10 depicts an overview of the different processing steps during the thinning procedures. The problems at the beginning were homogeneity. The wafers were not the same thickness everywhere, which resulted in the in-ability to completely polish the wafer, resulting in an imperfect surface and fragile chips. This in combination with the detaching wax layer resulted in many lost wafers. After a procedure was found that resulted in a homogeneous removal rate and the wafers stayed attached on the glass carriers, the process went smoothly. The final process can be found in the upper right column of Figure H.10.

H.6. Adhesion agents

Some materials do not hold onto certain materials. This means when, for example, gold is deposited on silicon oxide, the gold will not stay/bond with the silicon oxide and will fall off with relative ease. To improve the bonding between those two materials (and other material combinations), certain adhesion agents are used.

The first adhesion layer is already applied before the first layers of the chip or polyimide substrate are con-

Figure H.9: Mechanical grinding: black stripes indicate removed silicon.

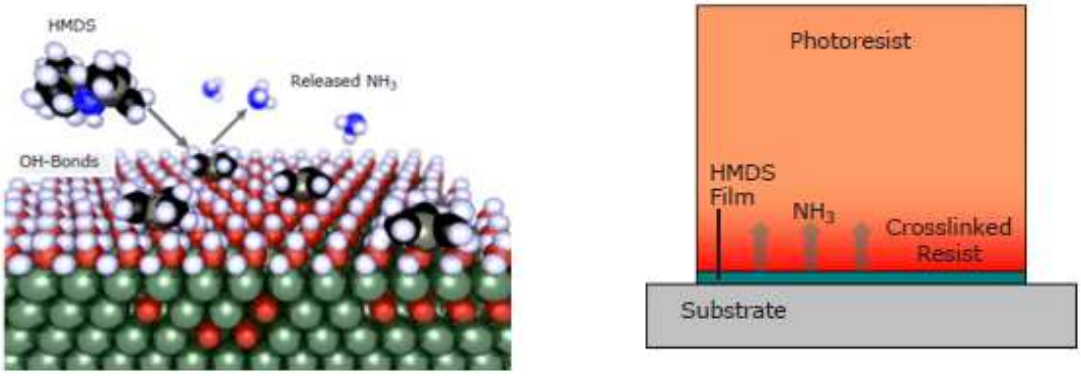
Wafer type	500 µm silicon oxide wafer with gold galvanic			
Pre-grinding glass substrate	20 minutes	20 minutes	20 minutes	90 minutes
Protective photoresist layer on active side	AZ9260 photoresist	AZ9260 photoresist	No. Wax does not hold good on photoresist	No
Applying wafer on glass substrate	Heating wax to 100 °C. Turning off heat and vacuum and wait 1.5 - 2 hours	Heating wax to 100 °C and cooling to70 °C. Turn off heat and vacuum and wait 1.5-2 hours	Heating wax to 100 °C. Place wafer and wait 20 min. Gradually turn off heating and wait 2 hours. Turn off vacuum and wait overnight	Heating wax to 100 °C. Place wafer and wait 20 min. Gradually turn off heating and wait 2 hours. Turn off vacuum and wait overnight
Grinding 15 µm grain size	Thickness between 50-70 µm. Very in-homogenous grinding plate	Wafer detached from glass substrate. Wax did not hold. Many air bubbles in wax	Thickness 60-70 µm	Thickness 70 µm
Grinding 9 µm grain size	Thickness between 25-50 µm. Large thickness differences		Thickness 30-40 µm	Thickness 40 µm
Polish step (CMD)	Wafer too thin/ in-homogenous to polish entire wafer		Polishing still very in-homogenous	New polish plate. Homogeneous
Result	Only few chips succeeded. Fragile chips with large thickness differences		20% of chips succeeded but not flexible	

Figure H.10: Lapping diagram

structed. Appendix H.1 already discussed the thin chrome layer for bonding the gold to the oxide layer. Without this chrome layer, the gold will easily detach and fall off. The importance of the chrome layer could be seen during the fabrication of the polyimide substrate Version #4, where the electrodes fell out of their 'sockets'. This is further explained in Chapter 6.

The second adhesion agent is often used to enable a good connection between the silicon (oxide) layer and the photoresist. As well as the photoresist AZ5214 as AZ9260 both profit from an adhesion agent. The most commonly used agent for this at the RWTH IWE-1 is HMDS. It chemically bonds its Si atom to the oxygen of

oxidised surfaces, accompanied by the release of ammonia (NH3). A hydrophobic surface is formed (by the methyl groups of the HMDS fragments), improving the resist wetting and adhesion [26]. Figures H.11a and H.11b show this property.
HMDS is applied on the oxide layer in a vacuum oven at 110 degrees Celsius. The adhesion agent is vaporised and released in the chamber, forming a thin layer on the wafer.



(a) Schematic overview of the HMDS adhesion layer.

(b) The HMDS adhesion agent bonds to the oxidised surface, releasing ammonia.

Figure H.11:]
HMDS adhesion agent. Atom colours: C = black, N= blue, O = red, Si = grey, H =white [26]

The disadvantage of the adhesion agent HMDS is the need for a vacuum. When the wafers with the dummy chips are extremely thin (for example, less than 40 μm) and HMDS has to be applied for a lithography step, the wafers crack under the sudden change in atmospheric pressure. That is why a new adhesion agent, Ti Prime, was ordered and used for certain processing steps with extremely small thicknesses.
TI prime [27] is sold from the same company MicroChemicals and promotes the adhesion on Si and glass carriers. This adhesion agent is applied via spin-coating and does not need a vacuum chamber. This should solve the cracking of the wafers.
Another option would be to spin-coat the photoresist immediately on the wafer and then expose it. This step could work, however, it was noticed that some parts of the resist do not hold, making those parts of the wafer useless because undesired areas are also exposed by the UV light.

H.7. Plasma etching

Plasma etching is also used to thin the backside of silicon wafers or etch trenches in the wafer to isolate the individual chips. The Tegal 901 plasma etcher transports the wafer to the Reaction Chamber where a gas mixture is introduced. This gas mixture becomes reactive by the application of radio frequency electromagnetic radiation. This reactive mixture etches away the material. This process is, in theory, very homogeneous. A protective photoresist mask can be used to protect certain surfaces from the plasma. For example, etching trenches in the wafer. The masks covers the entire wafer except the trenches. After a certain time, the trenches are etched free and the rest of the silicon is left untouched.
The gas mixture is called SF6, which is used to an-isotropic etch the silicon. This mixture has difficulties to remove the build-up oxide layer on the wafer. Therefore, the etch process always starts with 15 minutes of CF4 gas mixture to remove this possible oxide layer.
Some problems with homogeneity also occurred with the Tegal 901. The removal rate was not completely homogeneous as expected, but was more like two moon-shaped areas. The top part removed the silicon faster, resulting in large thickness differences throughout the wafer. More information and possible fixes to this problem are introduced in Chapter 6. Another problem occurred while placing the already thinned wafers in the vacuum chamber. The first Charges already had some adhesion problems between the glass carrier and the wafer. This meant that there already were some air bubbles or other irregularities between the two surfaces. When placed in the vacuum chamber, very often the wafers cracked under the sudden pressure differences. Later, with the newer Charges where the wafers had a good adhesion to the carrier and were very homogeneous, these problems were not to be found again. Some images that show the ramification of those

adhesion and in-homogeneous problems are shown in Appendix G.

As mentioned earlier, two different dummy chips production methods were used **trenches-first** and **thinning-first**. Difficulties with the first process were that the trenches were first etched in the silicon until a depth of 30 µm was reached. But, because of the in-homogeneity problems this gave a lot of problems and the trenches were not all evenly deep. To circumnavigate this problem, the chips were first thinned to 25 - 30 µm, before the trenches were etched. Now the wafers could be in the plasma chamber as long as needed to clear all the trenches. The adhesion and tension problems were also solved by skipping the protective mask on the active side and/ or sawing the wafer in smaller pieces for stress relieve.
The trench depths are checked regularly. Figure H.12 shows the program that is used to determine the trench depths and widths. Two small measuring needles are slowly moved down and sideways over the wafer to measure the surface. On the bottom left, the depth of the current trench can be seen.

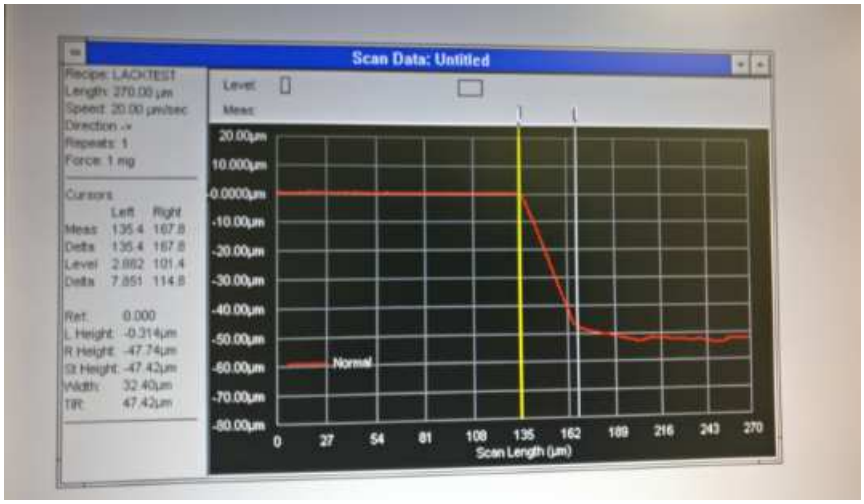


Figure H.12: Measuring trench depths after every plasma etch step.

The figure shows an additional possible problem of long plasma etching. The etch rate is not only vertically, but also horizontally. The trenches become more and more wide, the longer the wafers are etched. If very thin and high structures have to be etched, sometimes the etching step is repeated with a nice mask to protect all the structures. This protects the thin structures and ensures a sharp edge as possible.

Individual wafer production timeline

Table I.1: Timline table of all fabricated wafers

Version										
	Galvanic	Trench etch	Protective layer	wax + substrate	Thinning	Polish	Etch trench free	Lift-off	Thickness	Info
#3 w1	✓	✓	✓	✓	✓					polished to thin
#3 w2	✓	✓	✓	✓						Thinned to much
#3 w3	✓	✓		✓	✓		✓	✓	50 µm	Fragile
#3 w4	✓	✓		✓	✓	✓	✓	✓	50 µm	Fragile, not clean
#3 w5		✓	✓	✓	✓					Polished to thin
#3 w6	✗	✓		✓	✓	✓	✓	✓	40 µm	
#3 w7	✗	✓								Broken during sawing
#3 w8	✗	✓								
#4 w1	✓	✓	✗	✓						Wax to cold (70 °)
#4 w2	✓	✓	✓	✓						Discontinued
#4 w3	✗	✓	✗	✓	✓	✗	✓	✓	25 µm	Flexible
#4 w4	✗		✗	✓	✓	✓	✓	✓	25 µm	Flexible
#4 w5		✓								Gold-Chrome mask
#4 w6	✓	✓	✓	✓	✓	✓	✓	✓	50 µm	Gold-Chrome still on chips
#5 w1	✓	✓	✗	✓	✓					Broken during thinning
#5 w2		✓	✗	✓	✓					Thin rate too slow
#5 w3		✓	✗	✓	✓					Broken during thinning
#5 w4	✗	✓								Resist adhesive problems

Table I.2: Timline table of all fabricated wafers

Version										
	Galvanic	Trench etch	Protective layer	wax + substrate	Thinning	Polish	Etch trench free	Lift-off	Thickness	Info
#6 w1	✓	✓	✓	✓						Damaged substrate
#6 w2	✓	✓	✓	✓						Poor wax adhesion
#6 w3	✓	✓	✓	✓						Cracked during thinning
#6 w4	✓	✓	✓	✓						Poor wax adhesion
#7 w1	✓	✓	✓	✓						Wafer fell during thinning
#7 w2	✓	✓	✓	✓	✓✗	✓	Ti Prime	✓	50 µm	Few chips, little flexible
#7 w3	✓	✓	✓	✓	✓✗					Poor wax adhesion
#7 w4	✓	✓	✓	✓	✓✗	✓	Ti Prime	✓	50 µm	Few chips, little flexible
#8 w1	✓	✗								
#8 w2	✓	✗	✓	✓						Cracked during thinning
#8 w3	✓	✗	✓	✓	✓					
#8 w4	✓	✗	✓	✓	✓	✓	✓	Ti Prime	52 µm	Flexible thin chips
#9 w1p1	✓	✗	✓	✓	✓	✓	✓	Ti Prime	30 µm	Flexible thin chips
#9 w1p2	✓	✗	✓	✓	✓	✓	✓	Ti Prime	30 µm	Flexible thin chips
#9 w2p1	✓	✗	✓	✓	✓	✓	✓	Ti Prime	50 µm	Flexible thin chips
#9 w2p2	✓	✗	✓	✓	✓	✓	✓	Ti Prime	50 µm	Flexible thin chips

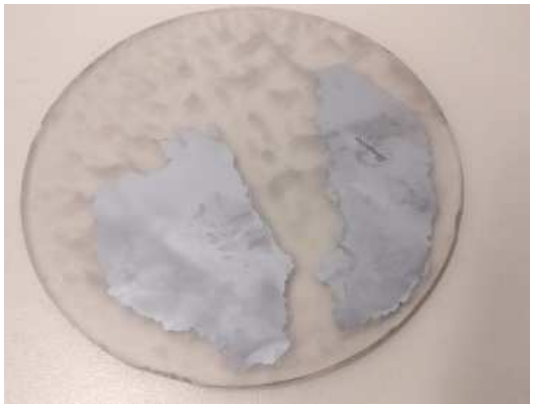
J

Polishing wafers

(a) In-homogeneous polish rate. The outer edges are polished faster (bottom of figure).

(b) Version #8 polish. Perfect homogeneity.

Figure J.1: Differences between homogeneous polish (right) and in-homogeneous polishing (left).



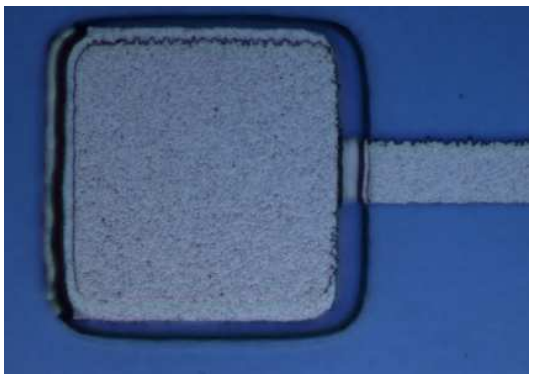
(a) Over polished.

(b) Over polished.

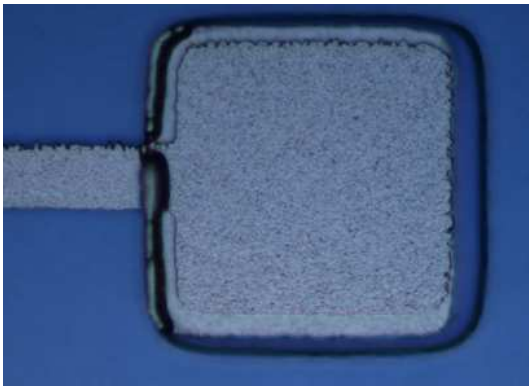
Figure J.2: During the earlier Versions the polishing rate was not very constant.

K

substrate version #7

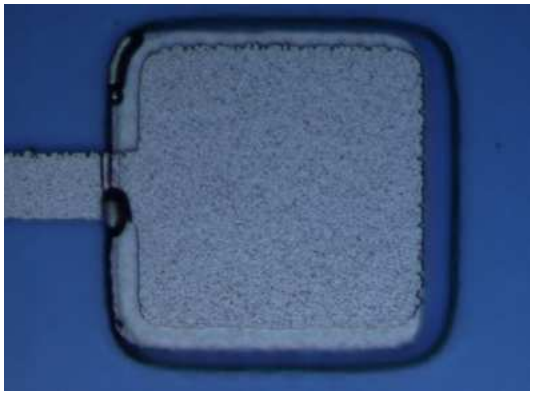


(a) Faulty interconnect

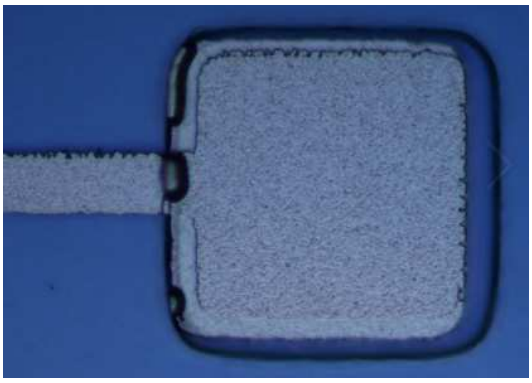


(b) Bad connection between pad and path.

Figure K.1: Version 7 substrate: Bad or no connection between pad and path due to large gap in polyimide substrate.



(a) Almost proper connection between pad and path.



(b) Still not a perfect connection.

Figure K.2: Version 7 substrate: High impedance connections between pad and path.

Publication article for "Poster 2018" in Prague

Development of a flexible polyimide substrate with through-connections

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Abstract. *The interest of flexible substrates and chips is increasing over the last years. Flexible substrates can, for example, be used in retinal implants to invoke visual sensations in visually impaired people. Through-connections in flexible substrates enable the possibility for new methods for packaging electronics in small spaces. Instead of placing all the electronics side by side, the through-connections facilitate smaller sizes by stacking the layers on top of each-other. The flexible foils are manufactured from polyimide and the condition of the through-connections can be tested using a fabricated thinned silicon chip. To ensure good through-connections, a proper adhesion agent should be chosen, as well as correct gold pad sizes, corresponding to the polyimide openings in which they are grown. The foil and chip are flip-chip bonded together using either an anisotropic or isotropic glue, respectively Elecolit 3061 and Elecolit 414.*

Keywords

Flexible substrate, Flip-chip bonding, Polyimide, Thinned silicon, Through-connections.

1. Introduction

Human skin and/or tissue is in a constant state of motion. When implementing stiff electronics onto the bodies surface, the experienced stresses are most often too high. Therefore, medical devices have to be flexible and able to handle body movements. The market for flexible wearable technology increases fast. It is estimated, according to IDTechEx, that the total market value can reach up to 70 billion US dollar by the year 2025, with the largest parties to be in the medical and fitness field. A few possible applications are retinal and cochlear implants, small heartbeat monitors, artificial electronic skins, physiological health monitoring and assessment, and therapeutic and drug delivery.

Flexible substrates for retinal devices carry the stimulating impulses through the substrate to the electrodes placed against the retina. This paper will discuss the development of such a flexible substrate. The process of manufacturing through-connections and a testing method to determine the condition of these connections will be mentioned below. Light will fall on the CMOS sensors located on a flexible thinned silicon chip. The light is converted into electrical impulses and send through a polyimide substrate foil to the stimulating electrodes located against the inner retina. The current pulses stimulate the ganglion cells, invoking light sensations in the patient.

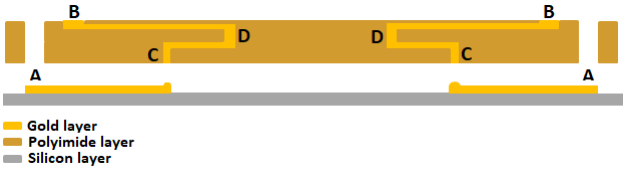


Figure 1: Side view: schematic representation (not to scale) of polyimide foil with the Galvanic steps.

2. Design

The structure is symmetrical over the short axis and features 16 through-connections. The outer dimensions are 5 by 24 mm with 100 by 100 $\mu\mathrm{m}$ gold pads and 20 $\mu\mathrm{m}$ wide interconnect paths.

These dimensions are chosen due to their high correspondence to Micro Electrode Arrays (MEA). A top view of the substrate is given in Figure 2. The flexible substrate will have polyimide PI-2611 as a base material. The polyimide layers will be 5 $\mu\mathrm{m}$ thick. The through-connections are pure gold and will be deposited with a galvanic electroplating method: the pads will be grown to a thickness of 5 $\mu\mathrm{m}$, the paths to 2 $\mu\mathrm{m}$. Figure 1 depicts a side view of the flexible foil and the silicon chip (bottom part). The silicon chip can be used to test the state of the through-connections by measuring the impedance between point A and B.

3. Fabrication

Polyimide PI-2611 from HD MicroSystems is already highly flexible and ideal for manufacturing flexible substrates. The foils are produced on a standard 4 inch silicon wafer with a

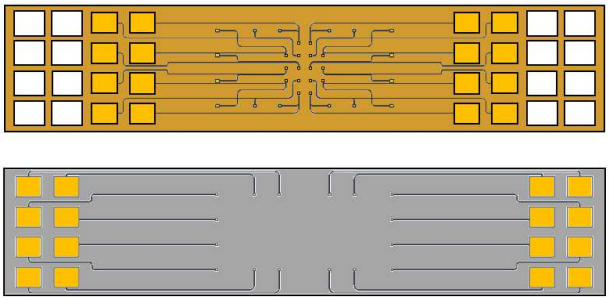


Figure 2: Top view: schematic representation of the polyimide foil (top) and silicon chip (bottom).

Titanium-Aluminum-Titanium sacrificial layer in between. After completion of the foils, the sacrificial layer is removed via wet etching and the foils are isolated from the silicon wafer. A connection between the bottom gold pads and the pads at the topside is created, as shown in Figure 3. The base layer of the foil is the polyimide layer with holes in it (PI-1) wherein (GL-1) the gold pads grow (indicated with a C in Figure 1. These pads will later be bonded to the chip. The second galvanic step (GL-2) deposits gold paths from the previous gold pads to the inner pads (indicated with a D in Figure 1). These pads (GL-3) are grown after a second layer of polyimide (PI-2) is placed to isolate the bottom gold pads and paths. The top paths are deposited during the final galvanic step (GL-4). Once again, all the connections are shielded and isolated (Except the pads at B) with a third polyimide layer (PI-3). As Figure 3 shows, the state through-connection can now be easily determined by measuring the DC resistance between A and B.

To be able to test the substrate and its through-connections, a dummy chip is placed on the foil and connected via gold pads. Normally, silicon does not allow itself to be bend. The material has to be thinned to a thickness well below 100 μm in order to become more flexible [1]. The chips are made from standard four inch silicon wafers with a single galvanic step to place the gold interconnect. For easier handling during mechanical grinding, the wafers are glued (with wax) to a glass substrate and thinned to its final thickness of 25 - 40 μm. Grinding occurs with a abrasive liquid solution formed from distilled water and Aluminum-oxide (Al2O3). To promote flexibility properties, chemical polishing (CMP) and cleaning steps are highly recommended for a smooth silicon surface. Trenches are etched around the chips with CH4 and SF6 gas mixtures to isolate the chips. To provide a mask for this etching step, backside lithography is necessary because the trenches are etched from the backside of the wafer.

The polyimide foil is bonded to the chip (the orientation is the same as shown in Figure 1) with the flip-chip bonding method. The substrate is placed on the bonding plate, lifted upward, and rotated away from the plate by a rotating arm. The chip is placed on the bonding plate and aligned as perfect as possible to match the foil pads. Before this step, the chip pads are covered in a bonding glue (anisotropic or isotropic). After alignment is complete, the arm swings slowly back down and presses with a predetermined force on the complete structure. After a certain amount of time the heating phase begins (with a 4 Kelvin per second increase) and the structure is heated until the bonding glue has hardened and the connection is final. After the structure is cooled (with a 3 Kelvin per second decrease), the arm is slowly rotated away, releasing the pressure and ending the cycle.

Two different bonding glues are used in this project: the anisotropic Panacol Elecolit 3061 [2] or the isotropic Panacol Elecolit 414 [3]. The key difference is the conducting property: anisotropic versus isotropic. Both glues can be placed on the gold pads with a dispenser. However, the isotropic glue is very thick and can also be placed manually on the chips gold pads using a small copper wire. The wire is dipped in the glue and then carefully pressed on the gold pads, leaving a small drop of residue behind on the pad. Other properties of the glues are compared and listed in Table 1.

Table 1: Comparing properties of Elecolit 3061 and 414 [2] [3]

	Elecolit 3061	Elecolit 414
Type	Anisotropic	Isotropic
Viscosity	35 000 - 45 000	20 000 - 25 000
Temperature Resistance	-40 to +180 °C	-50 to +200 °C
Curing time	10s on 150 °C	300s on 150 °C

4. Results

During the manufacturing process of the foils and the chips, a few process steps were found to be key for a successful through-connection in the substrate and the associated chip for measuring the condition of those connections.

4.1. Polyimide substrate foils

An adhesion agent is used to enhance the connection between the gold and the polyimide. But, because the complete polyimide foils are manufactured on a silicon wafer with a Ti-Al-Ti sacrificial layer, the choice for an adhesion agent should be carefully considered. When, in this case, the same adhesion agent (Titanium) is chosen as the sacrificial layer, problems could arise during the final steps when wet etching the sacrificial layer. Even though the etching step is brief, it is possible that the etchend creeps along the sides of the gold pad and slightly dissolves the adhesion layer. This results in loss of the gold pads in the polyimide foils. Choosing a different adhesion agent than the sacrificial layer solves this problem.

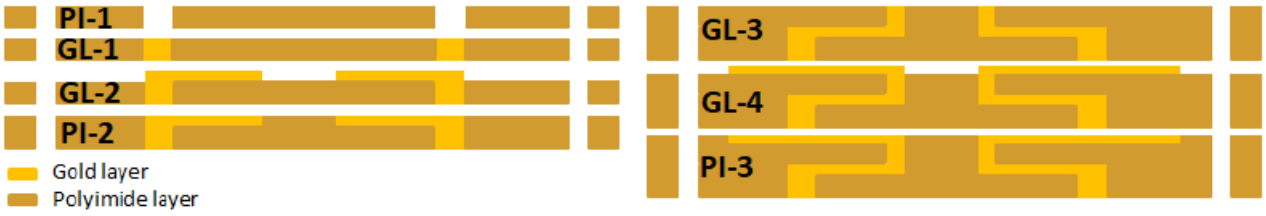


Figure 3: Side view: schematic representation (not to scale) of polyimide foil layers.

Another aspect is to ensure the gold pads have the same size as the polyimide foil openings in which the pads are located. Polyimide can not have sharp edges. It always slightly expands, and has round corners. When fabricating masks, this property of polyimide has to be taken into account. Ideally both parts should be of equal size, but it is favored to have slightly larger gold pads, even when the gold deposits little over the edge, instead of a trench between the polyimide and the gold. This trench can cause problems during the following galvanic steps. When the trench is large enough, a gold connection between the gold pads and their corresponding paths is not possible. Figure 4 shows a measurement of a substrate surface. From left to right: the polyimide layer and the higher gold pad are measured. After this, the trench is clearly visible as a large down facing peak. The depth of the peak and the top of the pad corresponds exactly to the 5 µm first galvanic layer and the second 2 µm from the second galvanic step. The gold pad is slightly aligned to the left. On the right side there is no gap, only a little additional gold bump on the foil. The average size difference between the polyimide hole and the gold pad was 13 µm. When the galvanic layer deposits only 2 µm the gold cannot connect to each other from either side (Figure 6a). Other electrodes from another wafer, and thus a different alignment of the galvanic step in relation to the polyimide layer, show a good connection to the paths, as shown in Figure 6b.

The final but maybe most important processing step is to include a second exposing step after the second and fourth galvanic step. With the first galvanic, the pads grow in the designated areas in the polyimide holes. When there still is a trench between the foil and the pad, the photoresist used for the second galvanic will completely fill this trench. When exposing this mask for, let's say a 8 µm photoresist mask, the intensity will not be enough to completely expose all the photoresist in the trench (the total thickness of the mask and the trench is far over the 8 µm). This results in possible unexposed photoresist residues in the trenches, disabling the gold to grow a connection between the pad and the path. A schematic representation of this property is shown in in the left side of Figure 5. The right side shows displays the procedure with a pad size corresponding to polyimide hole. The gold grows slightly outside of the pad, but a connection between the path and pad is guaranteed.

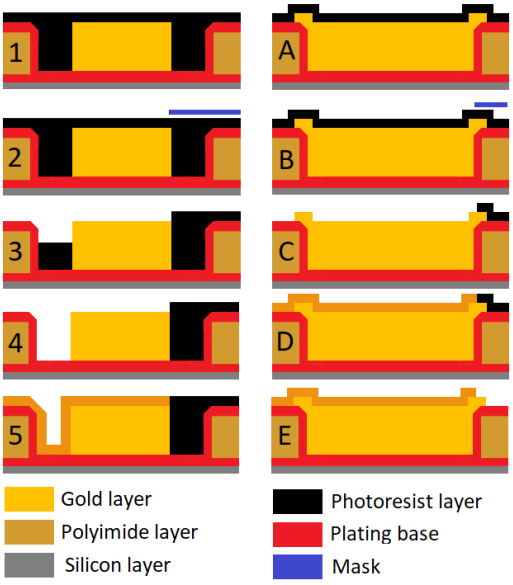


Figure 5: Schematic representation (not to scale) displaying the double exposure when implementing two sequential galvanic steps.

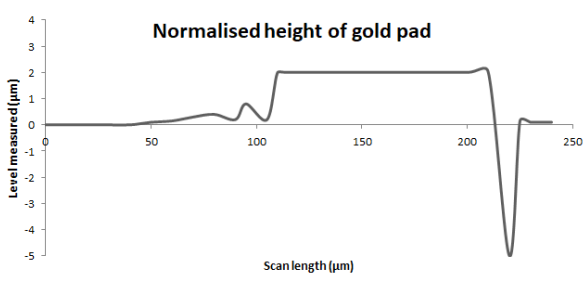
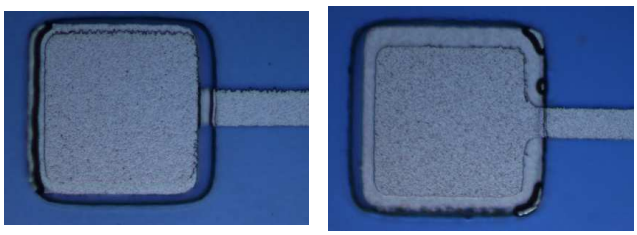


Figure 4: Measurement of surface level over a gold pad.

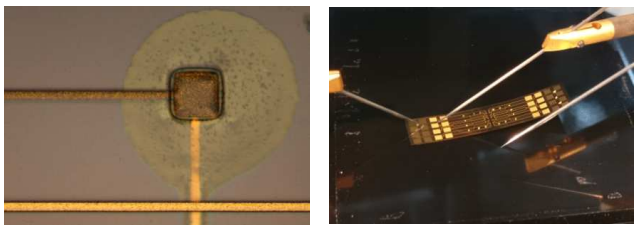
4.2. Thinning silicon chips

Multiple different chip versions were manufactured. It was noticed that dry etching the trenches before thinning gave rise to a set of problems. The main disadvantage of this method was the in-homogeneous removal rate of the dry etching. The trench depth was determined to be 25 µm. However, it was extremely difficult to achieve this depth homogeneously throughout the entire wafer. Rotating the wafer every few minutes during dry etching was able to partly remedy this problem however the trench depths var-



(a) (b)

Figure 6: (a): After the 2nd galvanic step, the trench is clearly visible. (b): Other wafer with different alignment with a good connection.



(a) (b)

Figure 7: (a): Bonding with anisotropic Elecolit 3061. Some conducting particles can be seen in the clear liquid. (b): Measure setup for testing the through-connections.

ied widely between 25 to even 50 μm. Due to this fact, it is highly recommended to thin the wafers first. When implementing this method, the trenches are etched after the chip already has its final thickness and the trenches can be freed with relative ease. Figure 8 demonstrates the flexibility properties of a thinned silicon dummy chip.

For achieving thin, flexible, and homogeneous silicon chips it was extremely important to have a good mechanical thinning process setup. To ensure this, the wafers were chemically polished until the wafers had a highly polished view and had a reflecting mirror-like surface.

A protective layer on between the active side of the chip and the glass substrate can be integrated to protect the chip against scratching and to ease the lift-off procedure. However, it was found when doing this, the wafers did not have a a good surface adhesion to the wax-layer that is used to glue the wafer to the glass substrate. The photoresist used as a protection layer did not hold good to the oxide layer of the chip. For the lithography process this did not yield to any problems but when mechanical stresses were applied to the wafer and glass substrate, air bubbles formed and eventually the wafer cracked under the stress.

Additionally in the backside lithography step it is recommended not using HMDS [5] as an adhesion agent for the photoresist layer. The very thin but wide wafer features relative high surface tensions. The HMDS adhesion agent is applied in vacuum conditions and high temperatures, which in this projects case, always resulted in cracked wafers. A different adhesion agent, like Ti Prime [6], can be used that is spin-coated on the wafer.

4.3. Assembly

As discussed in the previous chapter, two different glues were used to bond the chip and the substrate together. Both glues are able to connect the two parts together, however a slight preference was given to the less viscous isotropic glue. Small drops could be dispensed on the bonding pads and, when there is enough space and not too much pads, this process was relatively simple. The concern was that the anisotropic glue did not always yield in a proper bonding connection, due to its low number of conducting particles. See Figure 7 showing bonding with anisotropic glue and test setup for measuring the through-connections.

When bonding to parts together, it should be noticed that the pressure on the implant should be kept steady until both parts completely cooled and the glue is properly hardened. When the pressure is released, thus the pressure arm swings back up, there is a possibility that two parts shift relative to each other.

To lessen the stresses on the bonding pads during bending of the implant, an underfill can be used. This underfill will flow between the two parts and hardens. However, the capillary effects of the underfill used (Epotek 301 [4]) is not able to overcome extremely large distances (more than a centimeter). In the current designs of the dummy chips of this project it was only possible to dispense the underfill from either sides. The distance to the center was too small, hence the area around the bond pads could not be reached. A smaller and less wide chip than the polyimide foil is recommended to ensure a proper dispersion of the underfill (See bottom part of Figure 8). Another possibility would be to create a small hole in the middle of the polyimide foil, where the underfill could be dispensed. Daisy-chains were used in the smaller design in order that the outer measure pads were not needed anymore. The through-connections could now be easily measured between any two large substrate pads.

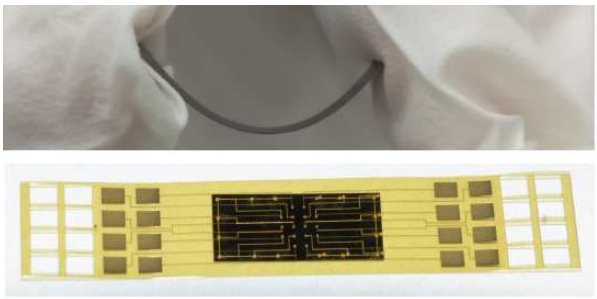


Figure 8: Polymide substrate bonded to small thinned silicon chip for testing.

5. Conclusion

This paper proposed a method for fabricating through-connections in a flexible substrate. Polyimide PI-2611 is used in these setup with 16 trough-connections. Different sharp edge or round edge connections were implemented but no differences were noticed during bending of the thin flexible substrate. Two main aspects are recommended for the manufacturing of through-connections: Minimise the dimension difference between the pad and its corresponding polyimide hole so that there is no gap between them. And to reduce the possibility of left-over photoresist in the possible trenches between the gold pads and its corresponding polyimide opening, a second exposure step is recommended. For testing purposes, a thinned silicon chip can be used that is bonded afterward to the substrate. Flexibility is increased by relieving the surface tensions by polishing and cleaning the thinned chips.

A flexible substrate with through-connections could be implemented for retinal implants. The flexible foil can be placed on the retina with stimulating electrodes on the ganglion cell layer. The thinned silicon chip can direct the current through the connections to the electrodes, stimulating the retinal cells and invoking visual sensations in the patient.

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[3] PANACOL, *Panacol Elecolit 414*, (2018).

[4] EPOTEK, *Epotek 301*, (2018).

[5] MICROCHEMICALS, *Hmds adhesion promoter*, (2017).

[6] MICROCHEMICALS, *Ti Prime adhesion promoter*, (2017).

About Authors...

Tim DE RIJK was born in Haarlem, The Netherlands on the 9th of April, 1993. After receiving his Bachelors degree in Electrical Engineering at the Technical University of Delft in 2015 with BSc project title 'Heart beat measurement in a wireless headphone', he started the master Biomedical Engineering in the year 2015. With the specialisation track 'bioelectronics', a close contact is kept to electrical engineering. The research presented in this paper is part of the master thesis project.

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Publication poster for "Poster 2018" in Prague

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Development of a flexible polyimide substrate with through-connections

Introduction

Human skin and/or tissue is in a constant state of motion. When implementing stiff electronics onto the bodies surface, the experienced stresses are most often too high. Therefore, many medical devices have to be flexible and able to handle body movements. The market for flexible wearable technology increases fast. According to IDTechEx, it is estimated that the total market value can reach up to 70 billion US dollar by the year 2025, with the largest parties to be in the medical and fitness field. A few possible applications are retinal and cochlear implants, small heartbeat monitors, artificial electronic skins, physiological health monitoring and assessment, and therapeutic and drug delivery.

Research goal

Flexible substrates for retinal devices carry the stimulating impulses through the substrate to the electrodes placed against the retina. Through-connections allow for smaller implants, because the structures are stacked and not placed side to side. The challenge is to fabricate such through-connections in a flexible substrate. The process of manufacturing through-connections and a testing method to determine the condition of these connections will be mentioned here.

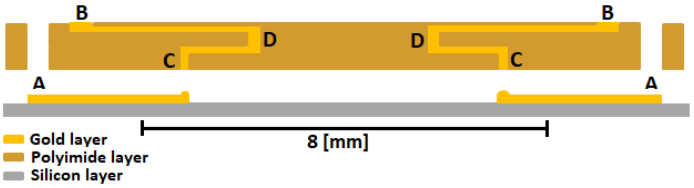

Figure 1: Side view: schematic representation (not to scale) of polyimide foil with: A,B the gold measure pad, C the polyimide bond pad to the chip, and D the electrodes.

Fabrication

The substrate (top part of Figure 1 & 2) features 16 through-connections. The inner 8 mm contains the through-connections, the additional length is only for testing purposes. The substrate starts with a Polyimide (PI) base with holes in which the bond pads are grown with electroplating (C in Figure 1). The next galvanic layer is grown on top of this layer (C to D) and this interconnect is isolated with another PI layer, and the process is repeated. For testing purposes, the substrate is flip-chip bonded to a thinned silicon dummy chip (bottom part of Figure 1 & 2) where the through-connections can now be measured between points A and B.

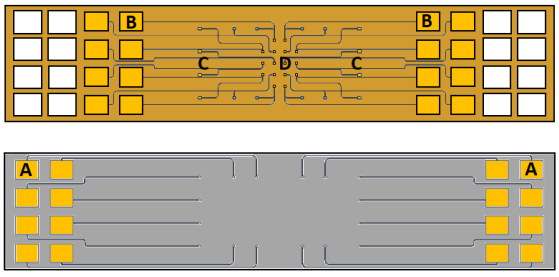

Figure 2: Top view of retinal dummy implant. The state of the through-connections can be measured between (A and B). (C) indicates the bond connections to the dummy chip, (D) the electrodes.

The substrate is flip-chip bonded to the dummy chip with isotropic glue Elecolit 414. An underfill (Epotek 301) is dispensed between the structures to promote higher flexibility properties.

Results

A second exposing step is needed when two consecutive galvanic steps are planned. There can be un-exposed photoresist between the polyimide holes and pads, as shown in Figure 4 (left).

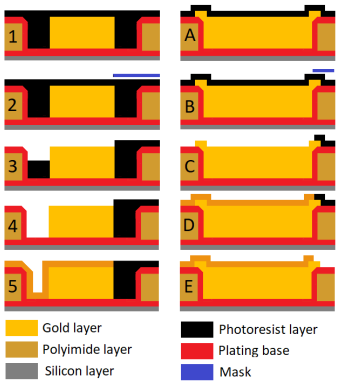

Figure 4: Schematic representation (not to scale) of remaining photoresist in trenches (left) and the importance of double exposing, and (right) the solution by increasing the gold pad size.

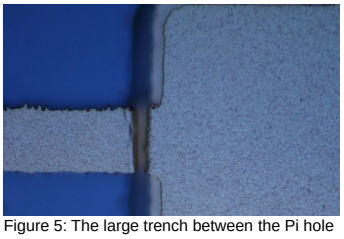

Figure 5: The large trench between the Pi hole and gold pad caused faulty connections.

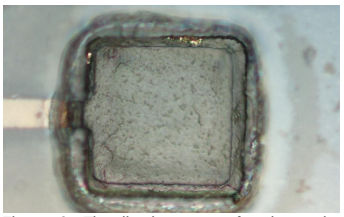

Figure 6: Ti adhesion agent for the pads, caused pads to fall out during de-bonding. Wet etching the Ti sacrificial layer affected also the adhesion agent. Changing to chrome adhesion agent with Ti-Al-Ti sacrificial layer gave good adhesion.

Polyimide (PI) has the property to enlarge slightly. To minimize the risk of trenches between the PI hole and gold pad, the pad size can be increased (Figure 4, right side). Figure 6 shows the effects of this trench: a faulty connection due to the large gap between the pad and path. Additionally, the importance of choosing the correct adhesion agent for the gold interconnect is depicted in Figure 6. When featuring the same adhesion agent as the sacrificial layer, the wet etching solvent could affect the adhesion agent, causing pads to fall out the substrate. Figure 7 shows a viable connection, which was manufactured by implementing the above mentioned process steps.

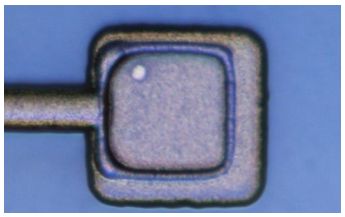

Figure 7: Low DC resistance through-connection and proper pad to path attachment. Little bulge around smaller top pad and path is noticeable, as expected due to the larger gold pad than PI hole.

Conclusion

This research proposed a method for fabricating through-connections in a flexible substrate. As shown, multiple aspects are of great importance to ensure viable and low resistance through-connections. A flexible substrate with through-connections could be implemented for retinal implants. The flexible foil can be placed on the retina with stimulating electrodes on the ganglion cell layer.

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