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ORIGINAL RESEARCH

PECVD silicon carbide surface micromachining technology and selected MEMS applications

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Abstract Attractive material properties of plasma enhanced chemical vapour deposited (PECVD) silicon carbide (SiC) when combined with CMOS-compatible low thermal budget processing provides an ideal technology platform for developing various microelectromechanical systems (MEMS) devices and merging them with integrated circuits. In this paper we present a generic surface micromachining technology developed using a stress-optimised PECVD SiC as the structural and encapsulation material for MEMS. An overview of selected MEMS applications realised, at DIMES Technology Center (DTC) of TU Delft, using the PECVD SiC surface micromachining technology is provided. Presented MEMS examples include—a pressure sensor, wafer-level thin-film packaging, RF switch and accelerometers. Potential applications for the presented technology include automotive, industrial and medical systems, where devices are often subjected to harsh environments.

Keywords Silicon carbide (SiC) · Microelectromechanical systems (MEMS) · Micromachining · Pressure sensor · Accelerometer · RF switch · Wafer-level packaging (WLP) · Thin film encapsulation (TFE)

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1 Introduction

Since the 1990's, silicon carbide (SiC) has gained considerable research and development attention, as an attractive alternative micromachining material to silicon, for realising various microelectromechanical systems (MEMS) sensors and actuators suitable for operation in harsh environments [1–7]. Thanks to its highly desired material properties such as high physicochemical stability, high hardness, good thermal conductivity, high-temperature operability, wear resistance and chemical inertness. During these years, majority of research efforts focussed on the technology development of SiC for establishing robust and reliable manufacturable processes. In this light, the material properties, in the form of plasma enhanced chemical vapour deposited (PECVD) SiC, when combined with CMOS-compatible low thermal budget post-processing shall provide an attractive surface micromachining technology platform for merging SiC MEMS with integrated circuits (ICs). By using high resistivity PECVD SiC thin films, as dielectric and structural material, and aluminium (Al) as electrical conductor, MEMS can be post-IC processed on top of the IC [5–7].

In this paper, a generic surface micromachining technology that exploits a stress-optimised PECVD SiC layer as the structural and encapsulation material for MEMS is described. An overview of selected MEMS applications realised in this technology at the DIMES Technology Center (DTC) of TU Delft is provided. Presented MEMS examples include—an absolute pressure sensor [8], wafer-

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level thin-film packaging [9, 10], RF switch [9, 11] and accelerometers [12]. Key features of the proposed technology are its ability to withstand certain harsh environments, versatility in fabricating a wide range of MEMS, reliable and cost-effective batch manufacturability, CMOS compatibility, smaller footprint and chip thickness than bulk micromachined counterparts [13, 14] as well as reduced process complexity.

2 Generic PECVD SiC MEMS technology

For microfabrication, a 65 MPa low tensile stress PECVD SiC layer devoid of pin-holes was developed in a Novellus concept one plasma deposition system using a mixture of SiH_4 and CH_4 gases at 400°C. The dry plasma etching of PECVD SiC was performed in an Alcatel GIR300 plasma etch system using a combination of CF_4, SF_6 and O_2 gases. Proper etch selectivity was achieved against inorganic and organic sacrificial materials used in standard semiconductor technology like PECVD oxides and polyimide, aluminium and silicon using different etch chemistries. The deposition and etching parameters of low-stress PECVD SiC are enlisted in Table 1.

The PECVD SiC surface micromachining process was designed to add (MEMS) functionality to a fully processed IC wafer typically consisting of an insulating scratch protection layer with open metal bondpads, formed from top metal layer of IC process. This top metal layer can already be used as a starting point for PECVD SiC MEMS fabrication in the form of MEMS bottom electrode. However for simplicity, the authors will henceforth describe the SiC surface micromachining process using a dummy silicon wafer as the starting substrate and aim to present example MEMS applications realised thereof. The fabrication process illustrated in Fig. 1 was developed on 100 mm wafers at TU Delft's DIMES Technology Center. Here, PECVD SiC is utilised as the structural and encapsulating layer for MEMS.

Table 1 Process parameters for low-stress PECVD SiC [9]

Parameter	Deposition	Etching
System	Novellus concept one	Alcatel GIR 300
Gas flow		
SiH_4 (sccm)	250	–
CH_4 (sccm)	3000	–
CF_4 (sccm)	–	70
SF_6 (sccm)	–	10
O_2 (sccm)	–	10
Temperature (°C)	400	–
Pressure (Torr)	2	37.5
HF power (W)	450	60
LF power (W)	150	–

The MEMS fabrication procedure begins with sputtering and RIE patterning of a 100 nm Al layer, that will serve as the first or bottom electrode. Next, a 1.5 µm sacrificial PECVD oxide layer is deposited on top of the Al layer and RIE patterned, see Fig. 1a. This step is followed by the deposition and RIE patterning of a 2 µm thick PECVD SiC to create the first layer of the mechanical structure as shown in Fig. 1b. On top of this layer, a 100 nm thick Al layer is sputtered and RIE patterned to form the second set of electrode, seen in Fig. 1c. Over this electrode, a second layer of PECVD SiC is then deposited and RIE patterned, refer Fig. 1d. In the next step, horizontal etch-holes placed across the periphery of the device are opened in order to access the underlying sacrificial oxide layer, refer Fig. 1e. The sacrificial PECVD oxide layer is then etched in 73% HF with addition of 2-propanol that is immediately followed by a freeze-drying process with cyclohexane to prevent stiction. It is worth mentioning that sacrificial oxide etching is performed using 73% HF due to its compatibility with existing aluminium metallisation.

Now another 2 µm of PECVD SiC layer is deposited over the previous PECVD SiC layer in order to seal the etch-holes, as shown in Fig. 1f, and finally the contact openings are created in the device to access a part of the second set of electrodes that serve as bond pads.

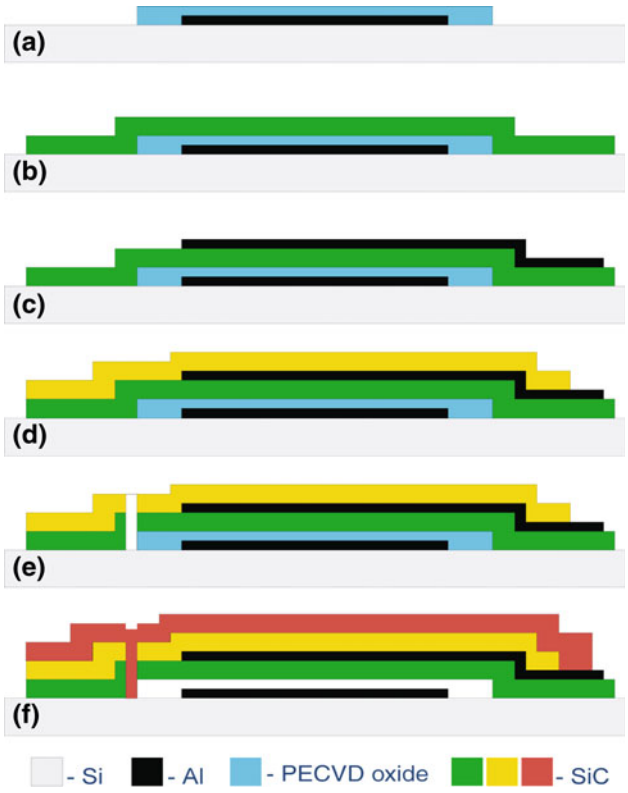

Fig. 1 PECVD SiC surface micromachining process flow

By introducing necessary variations to the abovementioned microfabrication process, a wide range of surface-micromachined devices employing capacitive detection and electrostatic actuation, such as pressure sensors, vertical and lateral accelerometers, and RF-switches can be fabricated. Furthermore, the presented process also enables the fabrication of encapsulated and sealed microstructures. Hence microstructures requiring wafer-level thin-film packaging can also benefit from the reported PECVD SiC technology. Besides, this packaging approach enables a smaller footprint and chip thickness compared to other wafer-level packaging (WLP) techniques employing wafer bonding [14, 15]. Also this encapsulation process can impart functionality by integrating additional *z*-axis electrodes [9, 11] for devices requiring vertical detection or actuation, implemented in our electrostatic RF MEMS switch described in Sect. 3.3.

3 PECVD SiC MEMS applications

A wide variety of MEMS can be fabricated using the above process. The structure and design of some selected MEMS devices employing capacitive detection and electrostatic actuation, namely, pressure sensor [8], accelerometers [12] and RF switch [11] together with wafer-level thin-film packaging [9, 10], are presented below.

3.1 Absolute pressure sensors

Figure 2 presents the schematic structure of a capacitive absolute pressure sensor and the resultant cross-section after device fabrication. In this device, explained in detail in [8], the capacitance changes accordingly with changes in pressure. The pressure sensor consists of an array of 100 circular sensing membranes, connected in parallel. This configuration resulted in a rest capacitance of 13.6 pF, when the device is under rest. Circular shape was chosen for the sensor design to minimise the stress concentration along the membrane edges and release-holes were placed along the device periphery. The sensor was designed to measure absolute pressures ranging from 10 mbar to 5 bar resulting in a relative capacitance change variation of 3% per bar of applied pressure. The full scale pressure range of the sensor can be tuned based on the thickness of the sensing membrane.

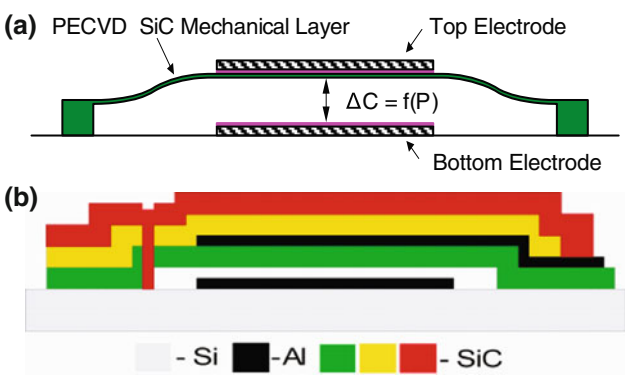

Fig. 2 Schematic of the capacitive absolute pressure sensor structure (**a**) and the fabricated cross-section (**b**)

3.2 Wafer-level thin-film packaging

The schematic shown in Fig. 3 illustrates the concept of wafer-level thin-film encapsulation using PECVD SiC for MEMS, instead of conventional zero-level packaging using wafer bonding. Benefits of applying PECVD SiC for wafer-level encapsulation includes robustness, CMOS compatibility, ability to withstand harsh environments, smaller footprint, and reduced chip thickness and process complexity. The possibility of adding functionality to device package by integrating an additional top electrode for devices requiring a vertical detection or actuation [11] is also illustrated. Thus the function of PECVD SiC layer is two-fold. Firstly, it holds the top electrode and secondly, it encapsulates and seals the microcavity defining the zero-level packaged environment for device operation. This type of WLP is suitable for small-area microstructures such as cantilevers, resonators, bridges, switches, etc. Moreover, this approach enables a smaller footprint and chip thickness compared to other WLP techniques employing wafer bonding [14, 15]. Here, only the feasibility of obtaining such an encapsulation using the generic process is discussed and a more detailed treatment is reported elsewhere [9, 10]. As an example, the RF switch discussed in the following section has been designed using the packaging concept described here.

3.3 Electrostatic RF switch

The RF switch structure [11] presented in Fig. 4a consists of three electrodes—top (supplementary) and bottom electrodes made of Al and a free-standing bar-shaped Al armature that is used for switching. The switch operates in

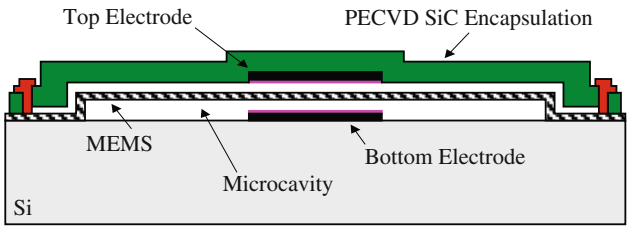

Fig. 3 Schematic of a wafer-level thin-film packaged MEMS with integrated vertical (*top*) electrode

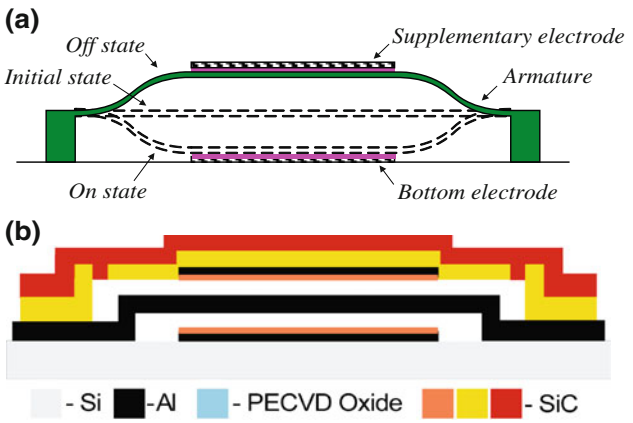

Fig. 4 Schematic of the electrostatic RF switch structure (**a**) and the fabricated cross-section (**b**)

three different states. In the initial state, the armature is at rest position. Here, the armature is electrostatically brought to its mechanical resonance by applying a 5 V AC voltage between the armature and the supplementary electrode. Now as the armature reaches its maximum displacement amplitude after a finite time period, a 5 V DC voltage is applied in order to capture the armature at the top electrode. This situation corresponds to the off-state of the switch. Now there is mechanical energy stored in the stressed armature which behaves as a spring system. In the on-state, the armature is released from the top electrode and is allowed to travel to the bottom electrode, where it is re-captured. The pre-stored mechanical energy drives the armature towards the bottom electrode resulting in a lower capturing voltage. In the presented case, a 5 V DC voltage was used for capturing purpose. For comparison, the same switch design using a conventional single-electrode configuration requires a pull-in voltage of at least 38 V for capturing the armature than the current design. Thus the reported RF switch design requires a lower operating voltage than a conventional single-electrode design.

The resultant device cross-section upon fabrication is illustrated in Fig. 4b that required some modifications to the generic process. Here, after sputtering and RIE patterning the Al bottom electrode, a thin PECVD SiC isolation layer is deposited and RIE patterned followed by the deposition and RIE patterning of the sacrificial layer. Then a 2.5 μm Al layer is sputtered and RIE patterned for the armature. Now a second layer of sacrificial material is added on top of the Al armature above which a second PECVD SiC isolation layer is deposited and RIE patterned. This step is followed by sputtering of Al supplementary electrode on the top over which a further 2 μm SiC encapsulation layer is deposited and RIE patterned. Release holes are then etched around the device periphery for removing the sacrificial PECVD oxide. After sacrificial etching, the release holes are sealed again with an additional layer of 2 μm PECVD SiC is applied for sealing purpose.

3.4 Vertical and lateral accelerometers

Figure 5a presents the structure of the designed vertical and lateral capacitive accelerometers. It is also possible to obtain a tri-axial accelerometer [12], as the lateral and vertical accelerometers could be fabricated simultaneously in the same process. The accelerometers have a triple-layered (PECVD SiC–Al–PECVD SiC) proof-mass suspended on four double-layered (PECVD SiC–Al) springs. In the vertical accelerometer, an applied inertial force along the z-axis is converted into the vertical movement of the proof-mass against fixed electrodes, due to which a capacitance change proportional to the inertial force is detected. The bottom electrode of the vertical accelerometer is divided into four parts such that the device is also able to sense the tilt and not just vertical displacements. The design of the lateral accelerometer uses planar electrodes that are embedded into the proof-mass, instead of using a typical area-consuming comb electrode. In this configuration, an applied inertial force causes lateral displacement of the proof-mass that is sensed as a capacitance change due to varying overlapping area. Hence, the footprint of the accelerometer can be significantly reduced.

Figure 5b shows the cross-sectional schematic of the vertical and lateral accelerometers upon fabrication. During device fabrication, the second PECVD SiC layer is

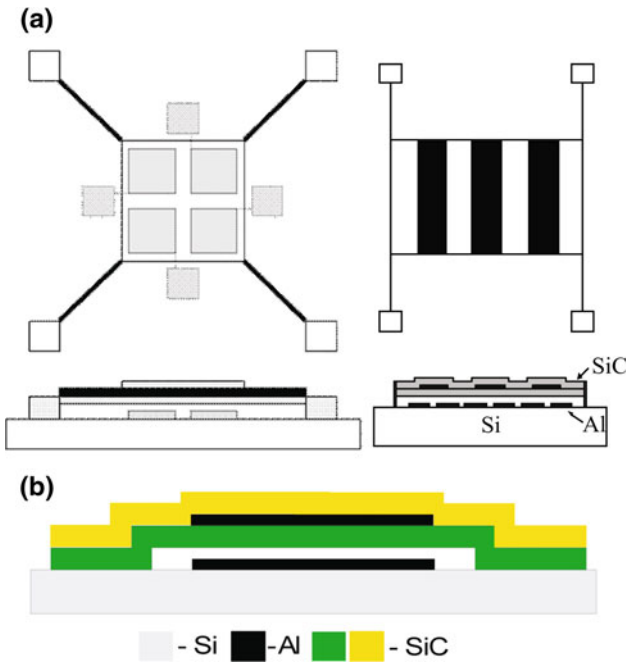

Fig. 5 Schematic of the vertical and lateral accelerometer structures (**a**) and the fabricated cross-section (**b**)

Table 2 Summary of design parameters of PECVD SiC accelerometers [12]

	Beam		Proof-mass	
	Length × Width	Thickness	Length × Width	Thickness
Vertical AXL	200 μm × 2.5 μm	1.8 μm SiC + 1.4 μm Al	500 μm × 500 μm	1.8 μm SiC + 1.4 μm Al + 1.8 μm SiC
Lateral AXL	300 μm × 2.5 μm		800 μm × 400 μm	

made free-standing that is suspended by the springs and thus is not sealed as with the other MEMS applications discussed in this paper. The accelerometers were designed to operate in a 5G range and a summary of design parameters are given in Table 2.

4 Results

Figure 6 shows a pressure sensing cell belonging to an absolute pressure sensor which consisted of an array of 100 such circular membranes of 80 μm diameter, resulting in a rest capacitance of 14.9 pF. The measured output device characteristic is presented in Fig. 7. The device was measured at various pressures ranging between 10 mbar and 5 bar that indicates a measured sensitivity of 2.6%/bar against a calculated sensitivity of 3%/bar. The change in capacitance with pressure from 10 mbar to 1 bar and from 1 to 5 bar was 0.4 and 3 pF, respectively. Simple vacuum sealing tests conducted with the above absolute pressure sensor indicated, no hysteresis and no change in the sensor output over a 3 year period. This test hence proves the reliability and long-term stability of the hermetic SiC encapsulation and also suggests no leakage condition.

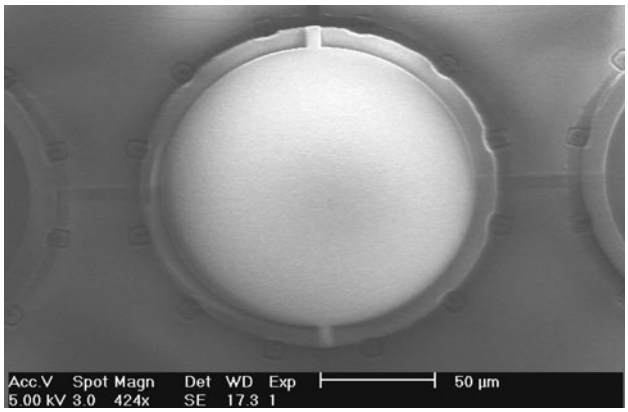

Fig. 6 SEM image of a pressure cell of a 5 bar absolute pressure sensor [8]

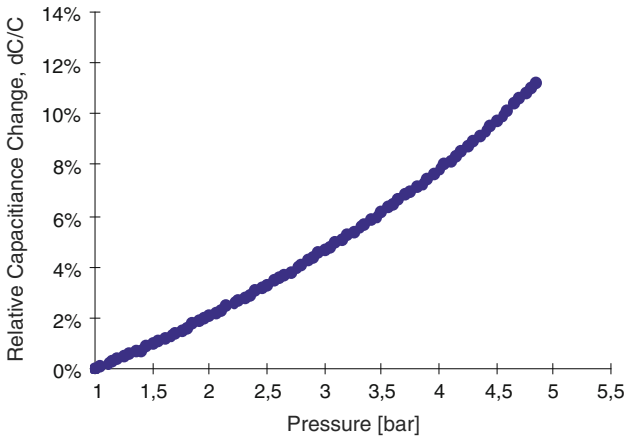

Fig. 7 Output characteristic of the microfabricated PECVD SiC pressure sensor [8]

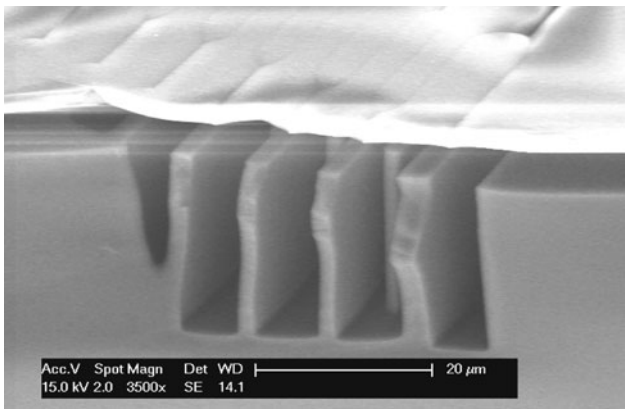

Fig. 8 Cross-sectional view of a wafer-level thin-film packaged high aspect ratio microstructure

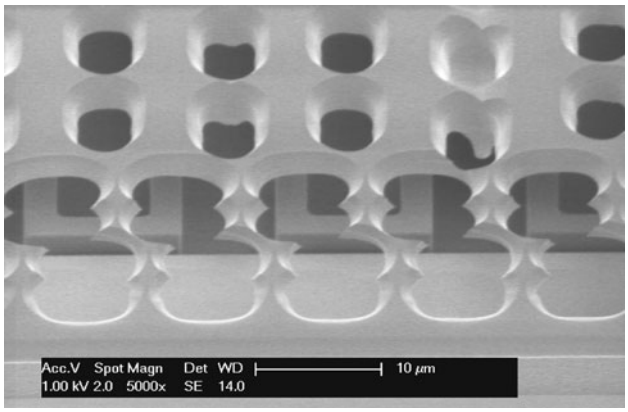

Fig. 9 Detailed view of an encapsulated meander-shaped microstructure. Here, the PECVD SiC encapsulation has been over etched to expose the underlying microstructure

The cross-sectional view of a wafer-level PECVD SiC encapsulation of a high aspect ratio microstructure is shown in Fig. 8 and a close-up view of a deliberately over-etched PECVD encapsulation is presented in Figure 9 to reveal the underlying meander-shaped microstructure. Such an encapsulation is suitable for packaging small-area microstructures such as cantilevers, resonators, bridges and high aspect ratio MEMS such as inertial sensors on a wafer-level. The vacuum level in the cavity was determined during the deposition conditions of PECVD SiC sealing layer.

A surface micromachined electrostatic RF switch is shown in Fig. 10. Device measurements performed at 5 V indicated a resonance frequency of 204 kHz, a Q-factor of 687.5, pull-in and pull-off voltages of 38 and 1 V, and capacitances of 14.7 fF (top electrode) and 2.66 pF (bottom electrode) with respect to the middle electrode at rest position, that are summarised in Table 3. In the vertical accelerometer, shown in Fig. 11, the 500 × 500 μm^2 triple-layered proof-mass is suspended over four bottom electrodes to sense the z-axis acceleration as well as the tilt. Measurements, refer Table 4, indicate a rest capacitance of 0.42 pF and a resonance frequency of 2.79 kHz. The

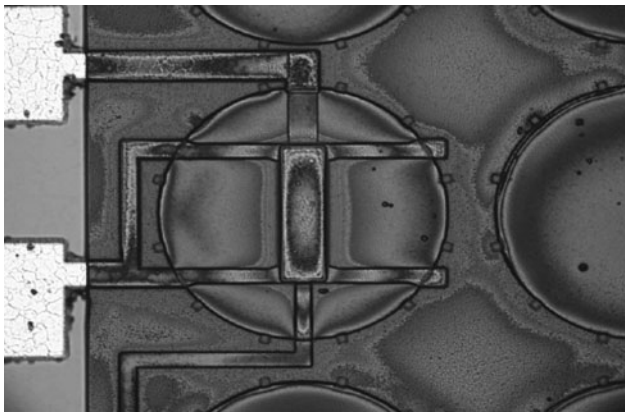

Fig. 10 Top view of the fabricated RF electrostatic switch [9, 11]

Table 3 Measured parameters of the RF switch [9, 11]

Device parameter	Values
Resonant frequency (kHz)	204
Quality factor	687.5
Pull-in voltage (V)	38
Pull-off voltage (V)	1
Capacitance (down, pF/up, fF)	2.66/14.7
Operating voltage (V)	5

Table 4 Measured parameters of the PECVD SiC accelerometers [12]

Device parameter	Vertical AXL	Lateral AXL
Resonant frequency (kHz)	5.6	6.3
Rest capacitance, C_o (pF)	0.58	0.23
Sensitivity, ΔC/g (fF/g)	1.84	3.16
Pull-in voltage, V_P (V)	3.1	4.5
Thermal noise ($\mu g/\sqrt{Hz}$)	4.7	5.4

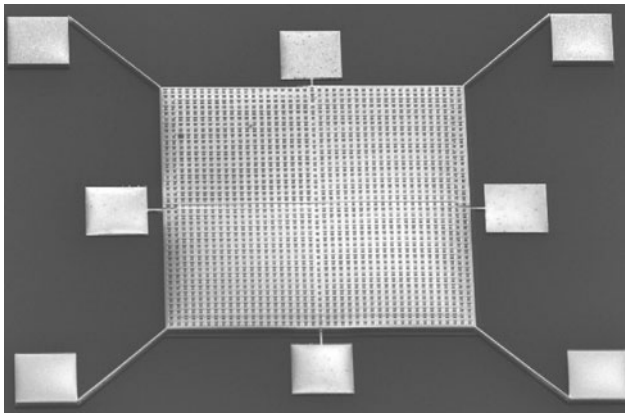

Fig. 11 A free-standing vertical accelerometer [12]

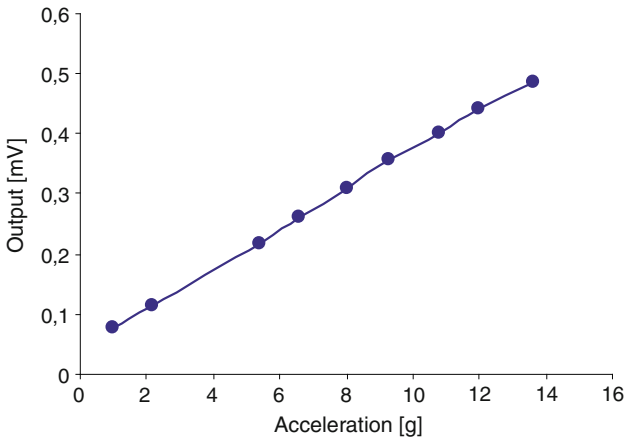

Fig. 12 Output characteristics of the vertical accelerometer [12]

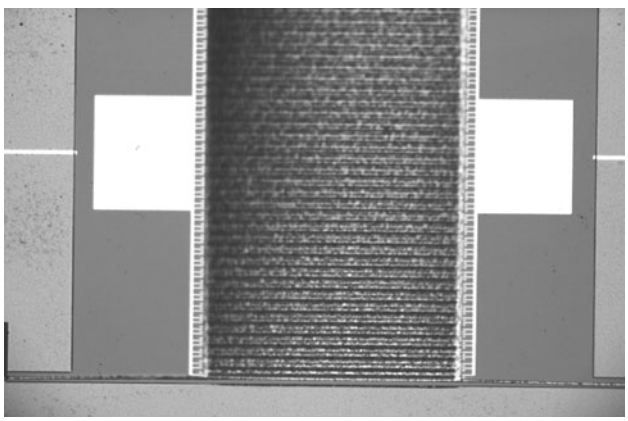

Fig. 13 Top view of a released lateral accelerometer [12]

measured output characteristics of the PECVD SiC vertical accelerometer is presented in Fig. 12. The lateral accelerometer presented in Fig. 13 was fabricated in the same process and features a $400 \times 800\ \mu m^2$ triple-layered proof-mass with embedded electrodes with a measured rest capacitance of 0.23 pF.

5 Conclusions

A generic surface micromachining technology utilising a stress-optimised PECVD SiC as the structural and encapsulation material was discussed. To showcase the versatility of the post-CMOS microfabrication technology, relevant MEMS applications developed using the above technology, namely, an absolute pressure sensor, wafer-level thin-film encapsulation, an electrostatic RF switch and vertical and lateral accelerometers, were presented along with device characterisation results. Presented MEMS applications and results indicate the suitability of the PECVD SiC MEMS technology for applications requiring CMOS compatibility, robustness, small footprint and low device integration costs. Hence, primary applications for this technology are envisaged in automotive, industrial and medical systems, where devices are often subjected to harsh environments.

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