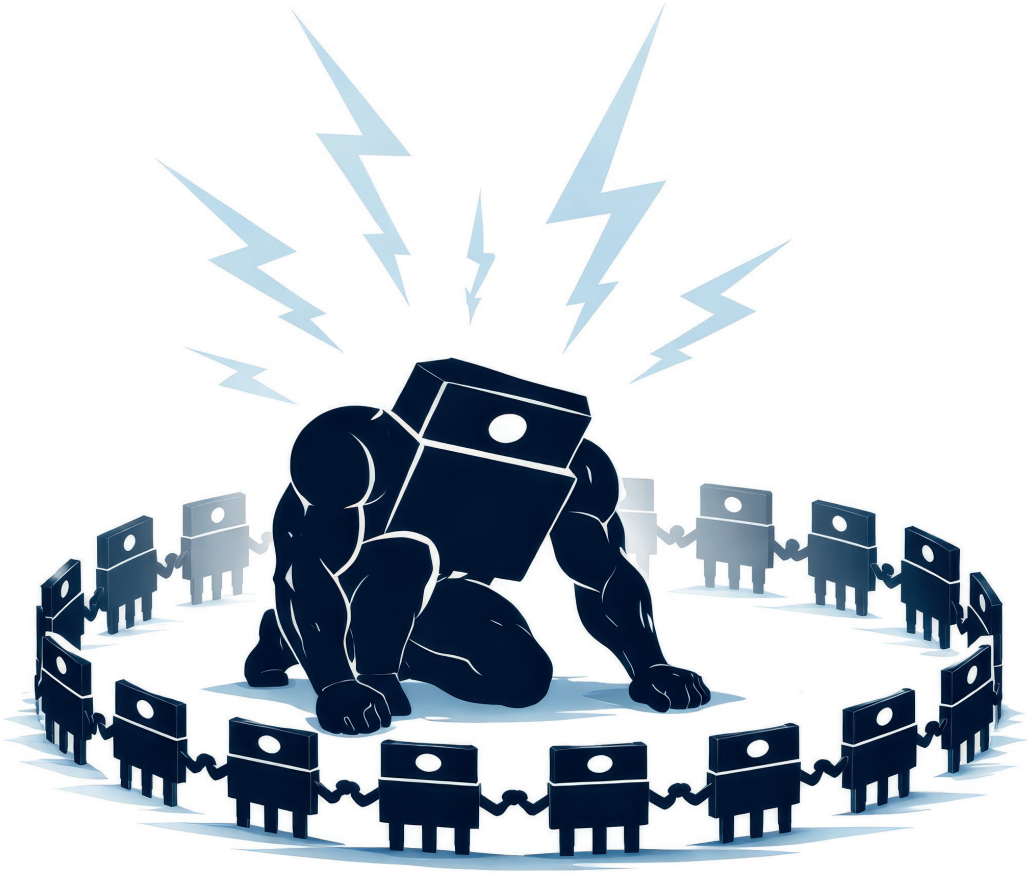
Development of a High Voltage Switch Using Series Connected Low Voltage Devices for Development of Power Electronics Based Arbitrary Waveform Generator



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Development of a High Voltage Switch Using Series Connected Low Voltage Devices for Development of Power Electronics Based Arbitrary Waveform Generator

Dissertation

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By

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The greatest use of a life is to spend it
on something that will outlast it.

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Summary

The global transition toward sustainable and electrified energy systems is fundamentally transforming electrical power grids. Increasing penetration of renewable energy sources, electrification of transport and heating, and widespread deployment of power-electronics-based interfaces are driving the evolution of today's AC grids toward future hybrid AC/DC architectures. While this transformation enhances flexibility and controllability, it also introduces fast switching transients, non-sinusoidal waveforms, and steep voltage gradients that impose novel electrical stresses on existing grid assets. Conventional high-voltage test equipment, designed for sinusoidal AC, DC, and impulse testing, is no longer sufficient to realistically replicate these in-service conditions. This creates a clear need for compact, flexible, and high-voltage Arbitrary Waveform Generator (AWG) capable of emulating future grid stresses. Power-electronics-based AWGs using modular multilevel converter (MMC) architecture offer a promising solution due to its scalability and waveform flexibility. However, practical implementation of MMC-based high-voltage test sources is often limited by excessive system complexity, large numbers of low-voltage submodules, more points of failure, and high cost. Increasing the voltage capability of a single MMC submodule therefore emerges as a key enabler for reducing system complexity, footprint, and cost while maintaining high performance.

Within this context, this PhD thesis addresses the fundamental challenge of realizing high-voltage and high-speed switching, using commercially available low-voltage wide-bandgap semiconductor devices. The work investigates series connection of SiC MOSFETs and GaN HEMTs as a cost-effective and scalable approach to enhance voltage-blocking capability.

The thesis establishes a comprehensive understanding of voltage imbalance mechanisms in series-connected devices, identifying gate-drive signal mismatch as the dominant contributor to dynamic voltage imbalance, while also revealing the critical and often overlooked influence of measurement-probe-induced parasitics on voltage distribution across series connected devices. Based on these insights, a transformer-coupled, gate-current-synchronized driving approach is identified as the most effective voltage-balancing technique. To overcome the inherent frequency and duty-cycle limitations of conventional transformer-based drivers, a novel programmable dual-transformer gate-driving architecture is developed. This approach decouples switching control from transformer constraints, enabling flexible, microcontroller-compatible arbitrary waveform generation while maintaining nearly uniform voltage sharing across series-connected SiC MOSFETs. Experimental validation demonstrates stable operation at kilovolt levels with nearly even voltage balance.

The work further extends and modifies the proposed new series-connection and gate-current synchronization concepts to ultrafast GaN HEMTs, addressing the challenges posed by nanosecond-scale switching. The developed open-loop, dual transformer gate driving strategy is shown to be well suited for GaN devices, and systematic optimization of transformer and excitation-stage parameters enables balanced voltage sharing at kilovolt levels while preserving the intrinsic speed advantages of GaN technology, confirmed by experimental validation on a hardware prototype under high-voltage, high-dv/dt switching conditions..

Overall, this thesis provides a simple, scalable, and experimentally proven high-voltage switching solution that enables low-voltage wide-bandgap devices to be used in medium-voltage systems. The proposed high-voltage switch has the potential to significantly reduce the complexity of MMC-based arbitrary waveform generator, enabling compact, cost-effective high voltage testing system capable of emulating realistic electrical stresses of renewables-rich hybrid power grid.

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Acronyms

2DEG	Two-Dimensional Electron Gas
AC	Alternating Current
AC/DC	Alternating Current / Direct Current
AlGaN	Aluminum Gallium Nitride
ANSYS	Analysis System (Commercial FEM Simulation Software)
AWG	Arbitrary Waveform Generator
C_{ds}	Drain–Source Capacitance
CEM	Common-Mode Electromagnetic
C_{gd}	Gate–Drain Capacitance
C_{gs}	Gate–Source Capacitance
CHB	Cascaded H-Bridge
C_{iss}	Input Capacitance
COTS	Commercial Off-The-Shelf
C_{oss}	Output Capacitance
C_{rss}	Reverse Transfer Capacitance
DC	Direct Current
DC–DC	Direct Current to Direct Current Converter
di/dt	Rate of Change of Current
dV/dt	Rate of Change of Voltage
E-Class	Class-E Resonant Switching Topology
EMI	Electromagnetic Interference
EMT	Electromagnetic Transient
EV	Electric Vehicle
FEM	Finite Element Method
FET	Field-Effect Transistor
GaN	Gallium Nitride
GND	Ground
H-Bridge	Full-Bridge Power Converter
HEMT	High Electron Mobility Transistor
HV	High Voltage
HVDC	High-Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
kHz	Kilohertz
kV	Kilovolt
KCL	Kirchhoff’s Current Law

KVL	Kirchhoff's Voltage Law
LC	Inductor–Capacitor
LCLC	Inductor–Capacitor–Inductor–Capacitor Resonant Network
LCR	Inductance–Capacitance–Resistance
L_3C_2	Resonant Inductor–Capacitor Compensation Network
LV	Low Voltage
MATLAB	Matrix Laboratory
MHz	Megahertz
MMC	Modular Multilevel Converter
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MV	Medium Voltage
O.C.	Open Circuit
PCB	Printed Circuit Board
PE	Power Electronics
pF	Picofarad
PhD	Doctor of Philosophy
PTFE	Polytetrafluoroethylene
PWM	Pulse Width Modulation
RC	Resistor–Capacitor
$R_{ds(on)}$	Drain–Source On-State Resistance
RE	Renewable Energy
R_g	Gate Resistance
S.C.	Short Circuit
Si	Silicon
SiC	Silicon Carbide
SNR	Signal-to-Noise Ratio
TA	Test Accessory
TVS	Transient Voltage Suppression (Diode)
V_{ds}	Drain–Source Voltage
V_{gs}	Gate–Source Voltage
V_{th}	Threshold Voltage
WBG	Wide Bandgap
XLPE	Cross-Linked Polyethylene

1

"If at first the idea is not absurd, then there is no hope for it."

— Albert Einstein

1. Introduction

The global transition towards sustainable and electrified energy systems is driving a fundamental transformation of electrical power grids, characterized by high penetration of renewable energy sources and an increasing reliance on power-electronics-based conversion technologies. This shift introduces new electrical stresses and operational challenges for existing grid assets, creating a growing need for advanced high-voltage testing solutions capable of emulating realistic in-service conditions. Within this context, this thesis investigates power-electronics-based high-voltage arbitrary waveform generation, focusing on modular converter architectures and series-connected wide-bandgap semiconductor devices as a scalable and cost-effective pathway toward compact, high-performance testing platforms.

1.1. Background and motivation

The economic growth around the world has raised serious concerns regarding the availability of natural resources and the environment, which are becoming key bottlenecks for sustainable development. Due to climate change, a major challenge of our time is to establish a sustainable and resilient energy system. Consequently, a massive global transition is underway, shifting traditional fossil-based energy production toward renewable sources such as wind, solar, and battery storage. At the same time, electricity consumption continues to grow rapidly due to the electrification of transport (EVs), heat pumps, and electrification of industrial processes. As a result, the demand for greener, more affordable, and more accessible electrical energy is increasing at an unprecedented pace. Experts agree that the importance of electricity as "the fuel of choice" will more than double over the next few decades, firmly establishing the electrical power grid as the backbone of future energy systems [1] [2]. Figure 1.1.1 shows an artistic illustration of future renewables rich smart electric power grid.

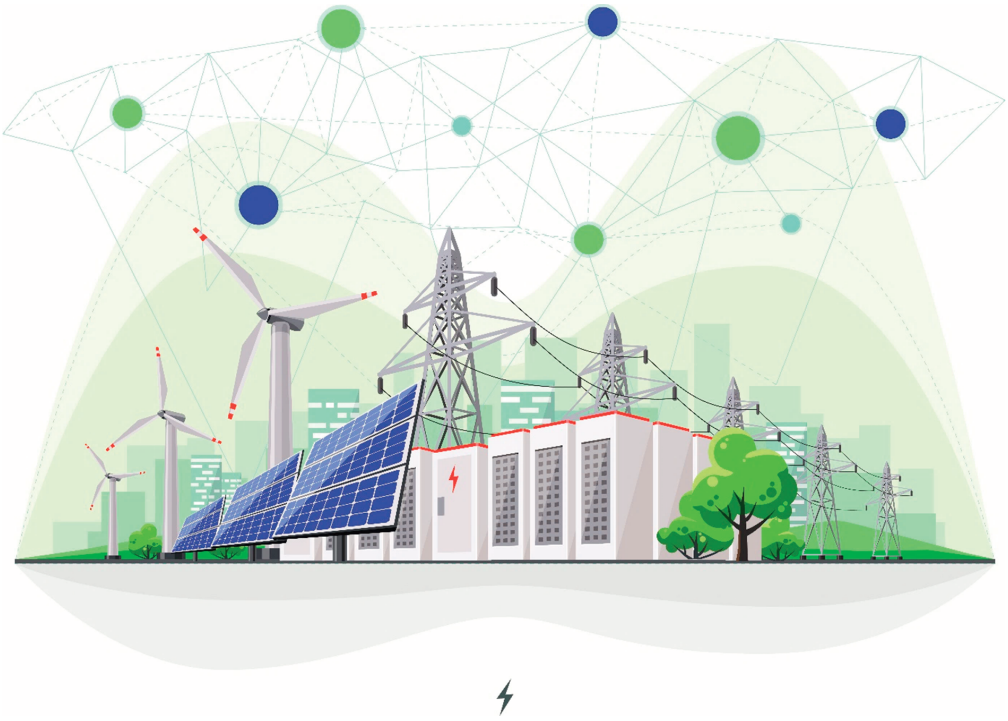


Figure 1.1.1. An artistic impression of renewable energy smart grid with solar, wind and battery storage. Image licensed from iStock [3].

In this context, the present grid is undergoing a profound transformation driven not only by renewable generation but also by the widespread deployment of advanced power electronics for energy conversion, control, and protection as illustrated in Figure 1.1.2. These power electronic converters, capable of fast switching, precise control, and seamless interfacing, are now central to integrating variable renewable sources, enabling flexible AC/DC conversion, and supporting the growing introduction of DC at low-voltage, medium-voltage, and (ultra) high-voltage levels. Rather than a simple transition from an AC power system to a fully DC power system, experts envision a gradual evolution toward a hybridized grid, in which AC and DC technologies coexist and complement one another. This future structure resembles a "sandwich architecture": DC technology dominates the upper and lower layers of the energy system through HVDC transmission and DC-based distributed energy resources, while AC continues to govern the intermediate layer in its conventional form [4] [5].

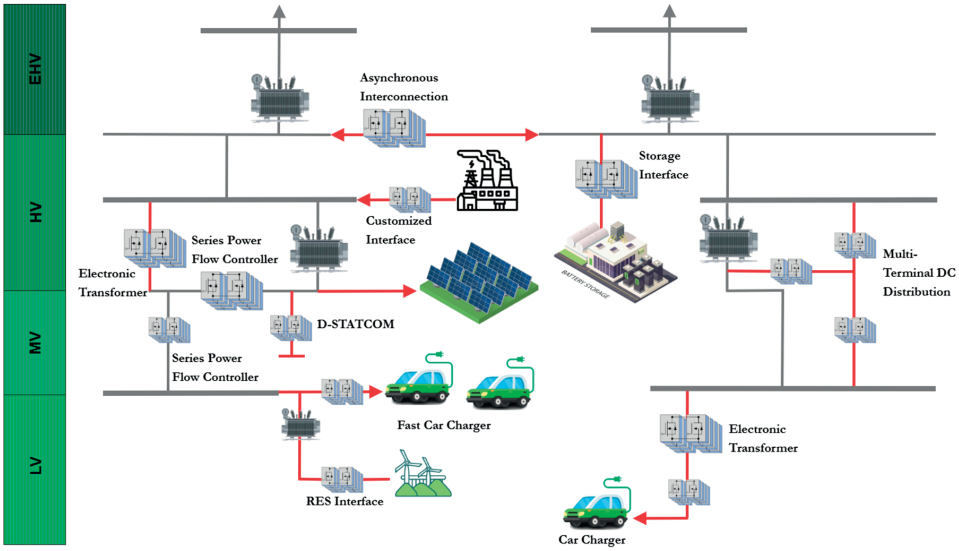


Figure 1.1.2: Widespread deployment of power electronics in the electrical power grid.

However, this hybridized and power-electronics-dominated grid, despite its superior flexibility and controllability, will also become far more complex to operate. The increasing reliance on converter-interfaced generation introduces new and unfamiliar electrical stresses into the network. Unlike conventional sinusoidal AC signals produced by rotating machines, renewable energy sources interfaced through power electronics generate staircase-shaped and PWM-modulated waveforms as shown in Figure 1.1.3 (a) and 1.1.3 (b), often superimposed with steep voltage gradients and fast transients as shown in Figure 1.1.3 (c). Such signals can impose significantly higher electrical stress on traditional grid assets, potentially affecting their dielectric strength and long-term reliability. As the share of converter-interfaced devices grows, the grid will exhibit new dynamic behaviors and interactions that existing equipment was neither designed for or tested to handle [6].

The traditional power system's components are tested with traditional high voltage test sources like transformers, impulse generators, and rectifier circuits that generate 50 Hz/60 Hz AC, lightning/switching impulse, and DC. However, the inclusion of renewable sources has created a need for testing of installed power infrastructure components with un-conventional HV signals.

Medium Voltage equipment (36 kV) is tested at a maximum voltage of 70 kV for power frequency but anticipating future requirements, a maximum voltage magnitude of 100 kV for power frequency signal is considered appropriate [7]. Some of high voltage test signals like sinusoidal and lightning/switching impulse etc. can be generated with a function generator in combination with a high voltage amplifier. However, this improvised arrangement is complicated and bulky to set up and has the available commercial high voltage amplifier has limitation of generating high voltage signals up to 60 kV in amplitude and a few kHz in the frequency bandwidth.

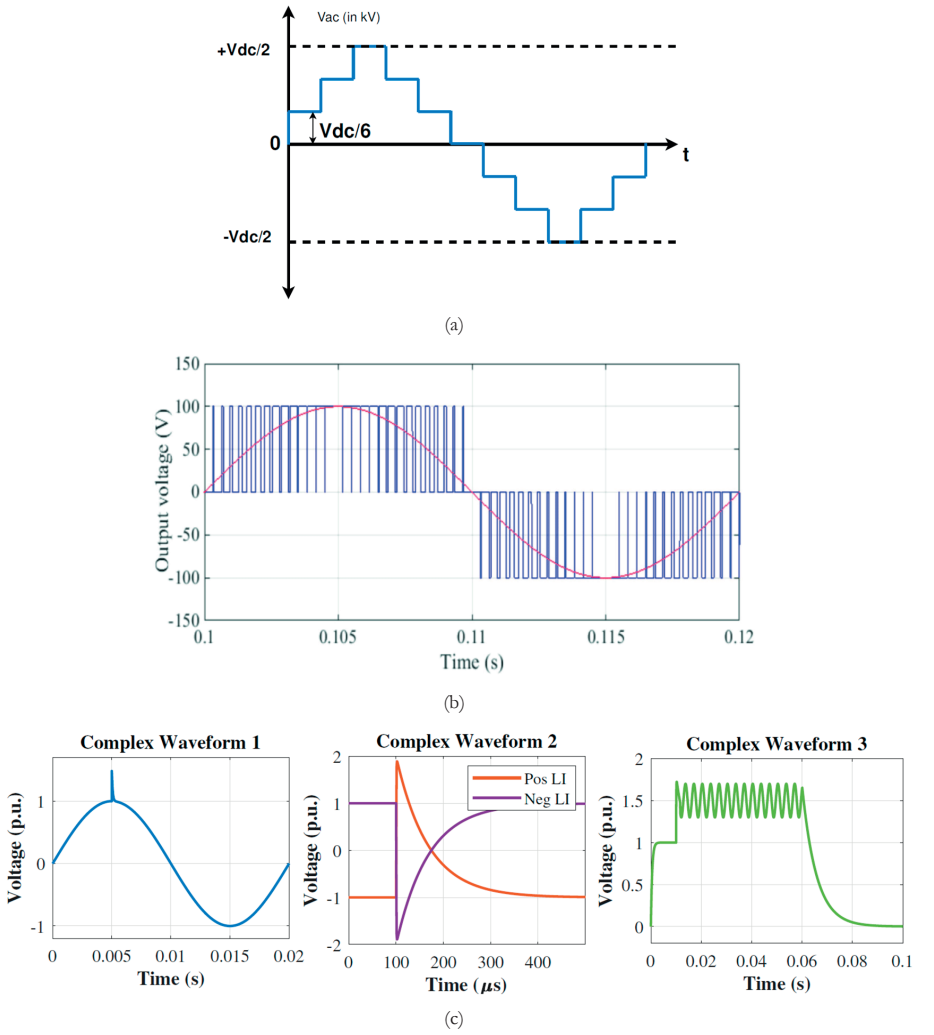


Figure 1.1.3: (a). Staircase shaped electric power signals. (b). PWM electric power signals. (c) Typical complex waveforms required for the dielectric tests of grid assets [6] [8] [9].

Therefore to replicate actual in-service electrical stresses with larger signal bandwidth and higher voltage level, there is a radically innovative idea of developing a high-voltage Arbitrary Waveforms Generator (AWG) using power electronics. To realize this, modular multilevel conversion topologies like Modular Multi-level Converters (MMC) and Cascaded H-Bridge (CHB) provide promising solutions in which multiple similar low-voltage modules can be stacked on top of each other to increase the voltage level of the converter to the desired high voltage level.

1.2. Modular Converters – Modular Multi-level Converters (MMCs) v/s Cascaded H-Bridge (CHB) Topologies

CHB and MMC are among the most popular topologies in high voltage conversion applications. It is essential to first and foremost choose the suitable topology for AWG application. Their simplified circuit diagrams are illustrated in Figure 1.2.1 where the capacitor C_{DUT} represents the equivalent capacitance of the insulation of Device Under Test (DUT). The most prominent point of the comparison is the DC source input to the converter. For MMC only 2 high voltage DC voltage sources will be required. However, CHB requires a large N number of DC sources for N Stages. Therefore, based on the reduced requirement for high-voltage DC sources, the MMC topology is identified as the more suitable choice for AWG applications [10].

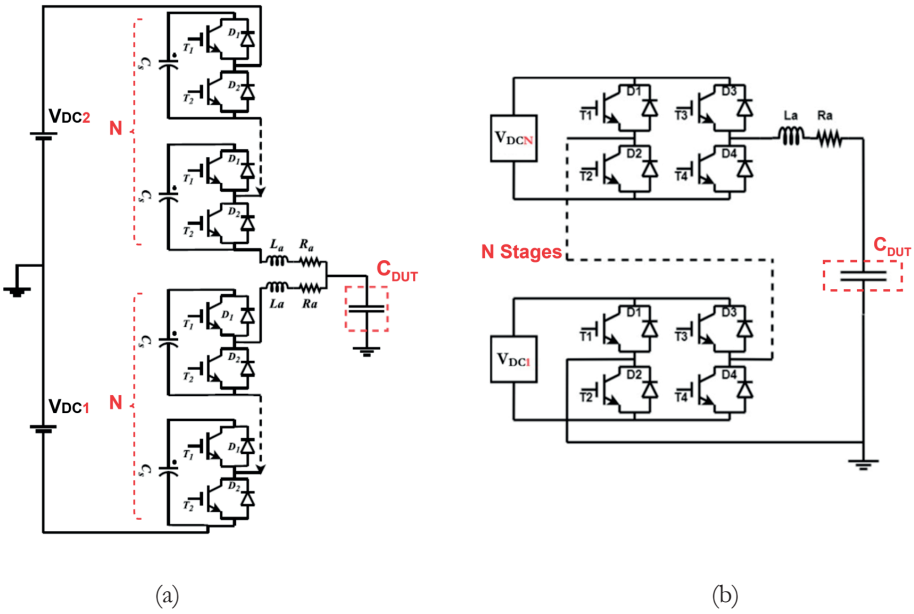


Figure 1.2.1: Simplified circuit diagrams of (a) MMC (b) CHB

1.3. Series-Connected Devices and Modular Multi-level Converters (MMCs)

Even with the promising features offered by the MMC, there is a catch. If the individual basic cell which is the building block of the MMC is able to handle around 1 kV, such configuration will result in stacking up many of these modules in order to achieve higher voltage handling capability. Along with the associated control and protection circuitry for each individual cell, such topology would make the device very complicated and hard to operate. Moreover, more components introduce more failure points in the device reducing the reliability of the device. Study in [6] established the number of submodules required as per their individual voltage blocking capability for a 200 kV DC link MMC in table 1.1.

Table 1.1. Number of submodules and voltage rating per submodule for a 200kV DC link MMC.

Sr #	Number of Submodules	Voltage rating of individual submodule (kV)
1.	12	16.7
2.	33	6
3.	50	4
4.	67	3
5.	100	2
6.	200	1

A very prominent desired feature of the AWGs is to achieve high voltage while reducing the complexity. Additionally, the goal is to make the AWGs compact without the need of setting up big equipment to avoid complexity and save time and space. One of the most promising techniques to achieve this is by increasing the blocking voltage of the devices. Although commercially available high-voltage Si MOSFETs driven by commercial gate drivers can withstand voltages up to 4.5 kV, however these devices offer limited current capability, often around 1 A continuous or 3 A peak. Devices with higher current ratings do exist, but they are significantly more expensive. There are custom-made switches that go even higher from several kV to 10s of kV. But these are application specific switches that cannot be driven by commercially available gate drivers [11]. They come with custom made driving and control circuitry. Moreover, the cost of these switches is exorbitant which would make the MMC arbitrary waveform generator not only expensive but difficult to maintain in case of failure of even a single switch.

The most appropriate approach for achieving a higher voltage level using low voltage devices are series-connected devices. A study in [12] demonstrated that series connected devices provide better on-resistance and higher current density compared to a single equivalent higher voltage device. Therefore, a cost-effective and efficient solution to increase the blocking voltage of the single submodule is to employ commercially available low voltage, low cost SiC MOSFETs and put them in series to increase the voltage handling capability beyond the commercial 1.7 kV rating to higher voltage levels as illustrated in Figure 1.3.1.

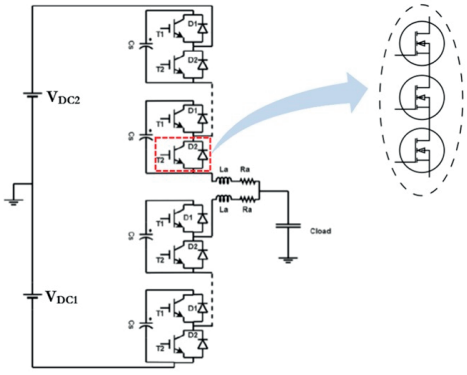


Figure 1.3.1: MMC submodule with series connected MOSFETs

1.4. Research Motivation and Objectives

Based upon the energy transition background, its foreseeable impact on power systems and technological advantages offered by MMCs, a power electronics-based compact Arbitrary Waveform Generator (AWG) offers a compact and flexible solution for testing grid assets [10]. However, since the MMC is a complicated and difficult to control topology, there is also a need to bring the complexity of the MMC AWG down. Therefore, a comprehensive study regarding the series connection of low voltage switching devices and novel solutions to achieve voltage balancing across them has been carried out in this PhD in order to achieve high voltage blocking capability of the single switch employed in MMC. This research has investigated a novel gate driving technique capable of synchronous switching and voltage balancing across multiple series connected SiC MOSFETs and GaN HEMTs. The high voltage switch will be the key building block that allows price reduction and accelerating the learning curve of the power electronics-based HV devices for dielectric testing of power electronics dominated grids.

1.5. Scientific Challenge, PhD Objective and Research Questions

The development of compact, high-voltage arbitrary waveform generators for medium-voltage grid asset testing requires scalable and reliable high-voltage switching building blocks. Series connection of wide-bandgap devices such as SiC MOSFETs and GaN HEMTs is a promising approach, but achieving uniform static and dynamic voltage sharing during fast and arbitrary switching remains a fundamental challenge. Voltage imbalance caused by gate-drive mismatches, parasitics, and measurement-induced effects can lead to device overstress, failure and limit system reliability.

The scientific challenge lies in understanding the mechanisms governing voltage imbalance in series-connected devices and in developing a simple, open loop gate-driving technique that ensures nearly uniform voltage sharing for high-voltage applications that is programmable, cost-effective, and scalable to medium-voltage levels. Addressing these challenges enables the realization of modular, low-complexity high-voltage switches as key building blocks for MMC-based arbitrary waveform generators and advances the broader field of high-frequency, high-voltage power electronics.

The PhD goal is to develop and build a high voltage switch using series connected SiC MOSFETs as a basic building block for an MMC prototype of a high-voltage Arbitrary Waveform Generator (AWG) for testing of grid assets of Medium Voltage Class (36 kV). To address the objective, the following research questions are formulated:

1. What methods exist to achieve voltage balancing in series-connected switching devices for MMC-based arbitrary waveform generation, and which factors govern uniform static and dynamic voltage distribution among these devices?

2. Which gate-driving technique provides nearly even voltage balancing across series-connected SiC MOSFETs while being simple to implement, cost-effective, and compatible with control using a basic microcontroller in a high-voltage AWG application?

3. Which technique can be applied to extend the voltage-blocking capability of ultrafast lateral series-connected GaN devices for future high-frequency high-voltage AWG applications?

1.6. Scientific Contributions

The principal scientific contributions of this PhD thesis are as follows:

Comprehensive classification and experimental validation of voltage-balancing techniques for series-connected switching devices

This thesis presents a systematic literature review and critical evaluation of methods used to enhance the voltage-blocking capability of individual switching devices through series connection, with specific focus on MMC-based arbitrary waveform generator applications. Voltage-balancing approaches are classified into voltage clamping, passive balancing, active gate control, and gate-current synchronization techniques. Through analysis and experimentation, the work identifies gate-drive signal mismatch as the dominant cause of dynamic voltage imbalance during fast switching and demonstrates, for the first time, the significant influence of measurement-probe-induced parasitics on both static and dynamic voltage distribution. It establishes accurate experimental methodologies, highlighting the necessity of probe compensation and high-bandwidth instrumentation, addressing an important gap in literature.

Development of a new programmable transformer-coupled gate-driving architecture for series-connected SiC MOSFETs

The thesis demonstrates that transformer-coupled gate-current synchronization is an inherently scalable, high-voltage-isolated, and dynamically robust gate-driving technique for series-connected SiC MOSFETs. While conventional implementations are fundamentally constrained by transformer operating frequency, limiting their suitability for arbitrary waveform generation, this work introduces a novel dual, complementary transformer configuration that overcomes this limitation. The proposed architecture decouples device switching from transformer frequency, enabling user-defined turn-on and turn-off control, independent adjustment of switching frequency and duty cycle, and compatibility with low-complexity microcontroller-based control which was validated experimentally through hardware implementation. It enables the realization of simple, cost-effective, and reliable high-voltage switches using low-cost commercial off-the-shelf components, while maintaining nearly uniform voltage sharing across series-connected devices.

Extension and modification of series-connection and gate-current synchronization concepts to ultrafast GaN HEMTs for kilovolt-level operation

This thesis extends voltage-blocking techniques to ultrafast lateral GaN HEMTs, addressing the fundamental challenges associated with their nanosecond-scale

switching speeds. It is shown that closed-loop voltage-balancing techniques become impractical for GaN devices due to the extreme demands on sensing, control latency, and bandwidth. Instead, an open-loop, transformer-coupled gate-current synchronization approach is demonstrated to be ideally suited for such applications. The work further contributes by employing simple GaN-based full-bridge excitation circuits, rather than complex E-class oscillators, and by systematically identifying and optimizing critical transformer parameters such as leakage inductance, coupling coefficient, and compensation capacitances that govern ultrafast gate-current transfer. This integrated excitation-stage and transformer-level optimization successfully enhances the switching speed of series-connected GaN devices, achieving nearly uniform dynamic voltage distribution at kilovolt levels, confirmed through experimental validation on a hardware prototype under high-voltage, ultra-fast switching conditions.

Overall Impact

By combining practical voltage balancing techniques, programmable transformer-coupled gate-driving architectures, and rigorously validated measurement methodologies, this thesis provides a scalable, low-complexity, and cost-effective foundation for high-voltage switching systems. These contributions directly enable the development of compact and reliable high-voltage switching modules as key building blocks for power-electronics-based arbitrary waveform generators used in medium-voltage grid asset testing, while also offering broader applicability to future high-frequency and high-voltage power-electronics systems.

1.7. Thesis Layout

The thesis follows a structured and systematic approach, progressing logically from foundational concepts to practical implementation.

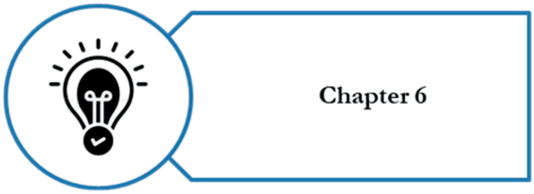
Chapter 1 introduces the background of the energy transition and the novel electric stresses occurring in future power grids, followed by the motivation, research goals, and the formulation of research questions and challenges.

Chapter 2 provides a concise review of series-connected MOSFETs topology, including a classification of gate-driving and voltage-balancing techniques, the requirements for cost-effective isolated gate drivers for high-voltage arbitrary waveform generation, and the selection of a simple, open-loop transformer-coupled technique.

Building on this, Chapter 3 describes the design of a high-voltage switch based on series-connected SiC MOSFETs with programmable switching frequency and duty cycle, which is experimentally validated using a laboratory prototype. It discusses the advantages and challenges of transformer-coupled gate driving, introduces a method to decouple switch duty cycle from transformer frequency to enable complex voltage waveform generation, and analyzes the associated resonance circuits through modeling, simulation, and optimization of the driver's operational frequencies and key components.

Chapter 4 establishes the influence of measurement probes on the voltage distribution across series-connected devices, validated through experimental measurements. Subsequently,

Chapter 5 extends the developed technique to GaN FET–based ultra-fast gate drivers for driving series-connected GaN devices to realize high-voltage, high-frequency switches validated through experimental results.



Finally, Chapter 6 concludes the thesis by summarizing the key findings, answering the research questions, and providing recommendations for future work.

2

"The future is already here, it's just not evenly distributed."

— William Gibson

2. Series Connected MOSFETs

Before developing a high voltage switch using series connected MOSFETs, it is necessary to understand this topology and challenges associated with it. Series-connected MOSFETs introduce significant challenges, including unequal voltage sharing, variations in device dynamic behaviour, synchronization of gate signals, and the risk of overvoltage during switching transients. This chapter therefore reviews the fundamentals of series connection topology, its limitations and surveys the state-of-the-art techniques for voltage balancing across them laying the foundation for the high-voltage switch topology developed in this work.

2.1. Series Connected MOSFETs

To enhance the voltage handling capability of a switch, the series connection of switching devices is a cost-effective method that preserves many advantages of mature low-voltage devices [13]. Higher efficiency and power density can be achieved by increasing the voltage-blocking capability of switching devices of a power converter [14]. Although there are custom-made SiC Devices under test in research laboratories that go as high as 10 kV and 15 kV, however, the commercially available SiC MOSFETs can handle voltages up to 1.7 kV [15], [16]. Apart from the scarce availability, the excessive cost of these experimental high-voltage devices makes commissioning and maintenance in medium-voltage conversion applications quite challenging. More importantly, the gate driving circuitry required to control these 10 / 15 kV SiC MOSFETs needs to be custom-made as Commercial-Off-The-Shelf (COTS) gate driving solutions fail to comply with the required high-voltage isolation requirement [16]. Additionally, the study in [17] shows that the specific on-resistance of power semiconductor switches increases exponentially as $R_{ds\text{-}on} \propto V_B^{2.3\sim2.5}$, where V_B is the device breakdown voltage. As a result, the current handling capability of high-voltage SiC MOSFETs decreases quickly, which could make them unsuitable for medium-voltage applications.

With the ability to connect commercially available and mature but lower breakdown-voltage switches in series, medium-voltage converters can be built with a significant cost reduction. Even though commercially available IGBTs offer breakdown voltages up to 6.5 kV, their switching speed is limited. The chip area of SiC MOSFET is smaller in comparison to IGBT, it results in smaller parasitic capacitances and higher intrinsic switching speeds of SiC MOSFET [18]. That is why SiC MOSFETs excel in providing not only fast switching performance but also a significantly small form factor, which results in compacting the size of the converters.

2.2. Factors Affecting Voltage Sharing Between Series-Connected SiC MOSFETs

In an ideal scenario, when synchronous gate signals are applied to the series-connected SiC MOSFETs, the voltage across the SiC MOSFETs should be equal at all times, as shown in Figure 2.2.1. However, in reality, the voltage sharing is not equal across the individual switches in both static and dynamic phases. Stressing the semiconductor device over its rated breakdown voltage might result in permanent damage to the switch. Static phase imbalance can be easily resolved by placing a static resistor of mega-Ohm values across drain-source terminals of the individual SiC MOSFETs [19]. Dynamic phase imbalance is, however, complicated with many variables involved. Dynamic voltage imbalance requires complex techniques for nearly equal voltage distribution among the series-connected MOSFETs [20].

There is a significant relation between gate driving signal and dynamic voltage imbalance across drain-source terminals of series-connected SiC MOSFETs [14]. In general, there are two categories of asynchronous gating signals. The first category consists of the time delay between gate control signals for series-connected SiC MOSFETs, as depicted in Figure 2.2.2. The gating signal of the top SiC MOSFET (in blue) turns off the switch M_2 quicker, resulting in an unequal voltage sharing between V_{ds2} (in blue) and V_{ds1} (in red). The dV_{ds}/dt slope defines the dynamic phase of the voltage sharing while ΔV defines the difference in the static phase of the voltage sharing. Typically, a mismatch of a few nanoseconds (time delay) between gate signals for series-connected SiC MOSFETs can result in a difference of a few kV across the individual device [21]. The next category of the asynchronous gating signals is distinguished in terms of the dVgs/dt slope, as visualized in Figure 2.2.3. Even if the control signals arrive at the respective gate terminal simultaneously, the time it takes to raise the gate voltage above the miller plateau voltage varies the V_{ds} response. This slope difference results in unequal voltage sharing in both static and dynamic phases [14]. These asynchronous gating signals are a significant contributor to the dynamic voltage imbalance problem, as only a 4 ns delay can result up to 40% voltage imbalance [14]. A few other factors also affect the voltage distribution. Figure 2.2.4 shows the capacitive network that influences the balanced voltage distribution. The physical structure of a SiC MOSFET exhibits intrinsic parasitic capacitances namely C_{gs} (gate-source), C_{gd} (gate-drain), and C_{ds} (drain-source).

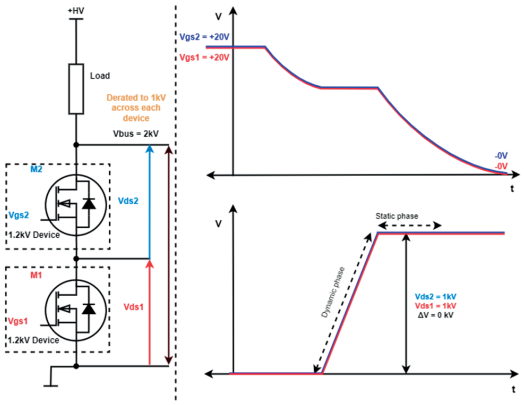


Figure 2.2.1. An ideal case of synchronous switching between series-connected SiC MOSFETs.

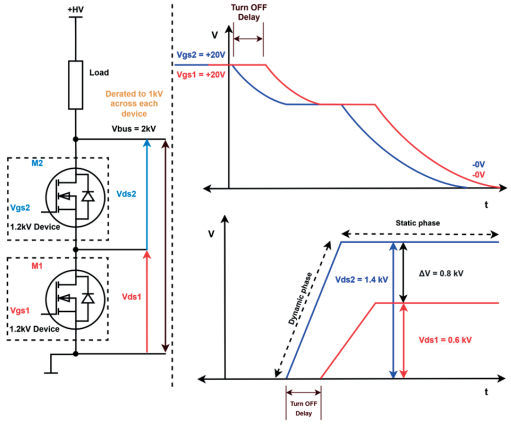


Figure 2.2.2. Asynchronous switching between series-connected SiC MOSFETs due to turn-off delay.

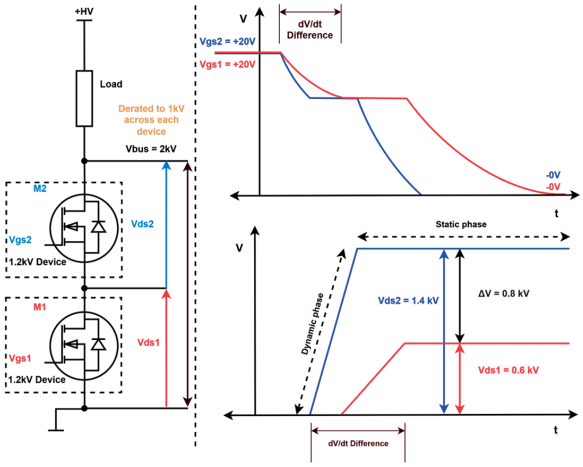


Figure 2.2.3. Asynchronous switching between series-connected SiC MOSFETs due to different in dV_{gs}/dt slope.

Typically, in the datasheet of a MOSFET, the capacitance curves of above mentioned capacitances are not explicitly given but are described as a graph of the following [22]:

1) Input Capacitance $C_{iss} = C_{gs} + C_{gd}$
2) Reverse Transfer Capacitance $C_{rss} = C_{gd}$
3) Output Capacitance $C_{oss} = C_{gd} + C_{ds}$

In addition to the intrinsic capacitive network, there are a few extrinsic capacitive couplings that influence equal voltage sharing across synchronously driven series connected SiC MOSFETs [14]. The use of multiple DC-DC converters to drive high-side SiC MOSFETs is inevitable. The isolation transformers for the DC-DC converters exhibit a dielectric coupling C_{ps1}, C_{ps2} referred to common ground [23]. As can be seen in Figure 2.2.4, both the control grounds (GND_1, GND_2) and power grounds are shorted on the input side of the DC-DC converters. Moreover, to enhance heat conduction from junction to the ambient, it is a common practice to mount devices on a heatsink which is grounded. Although SiC MOSFETs are electrically isolated from the heatsinks, the dielectric capacitance C_{pac1}, C_{pac2} is created, which offers an alternative path for conduction current flowing through SiC MOSFETs [20]. The turn-on and turn-off process of a SiC MOSFET is mainly the charging and discharging of these parasitic capacitances and the process variation or manufacturing defects define the deviation in the capacitance values for individual SiC MOSFETs [24], [25].

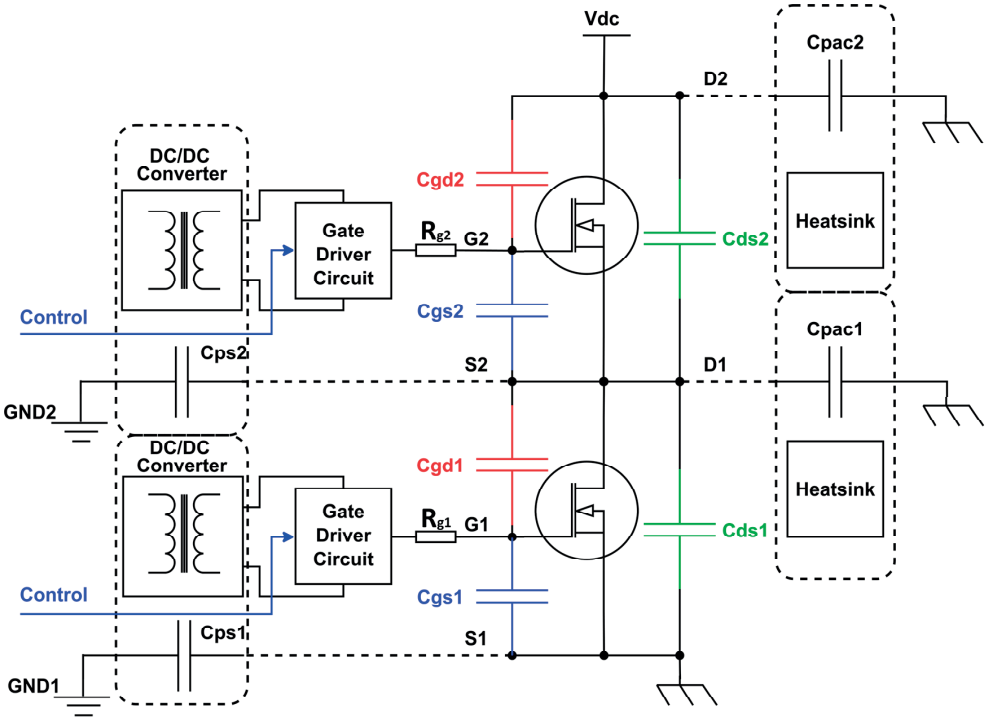


Figure 2.2.4. Potential parasitic capacitive contributors to unequal voltage sharing.

To test the effect of the process variation on voltage sharing a MATLAB simulation shown in Figure 2.2.5 is performed where C_{gs}, C_{gd} and C_{ds} intrinsic capacitances undergo ± 10% parametric sweep as an extreme mismatch case without any difference in gating signals. It is pertinent to mention that these intrinsic capacitances are non-linear, and their values with voltage variation are simulated as per graphs given in SiC MOSFET's datasheet [22]. Furthermore, to study the effect of the extrinsic capacitances, 10 pF and 20 pF capacitors are introduced across the drain-source terminal of each series-connected SiC MOSFETs. The results for the parametric sweep simulation are presented in Figure 2.2.6, which clearly show that the 10% variation in both static and dynamic phases of the V_{ds} voltage is nearly 10% which is comparatively less significant compared to the 40% imbalance created by the 4 ns gating signal mismatch shown in study [14].

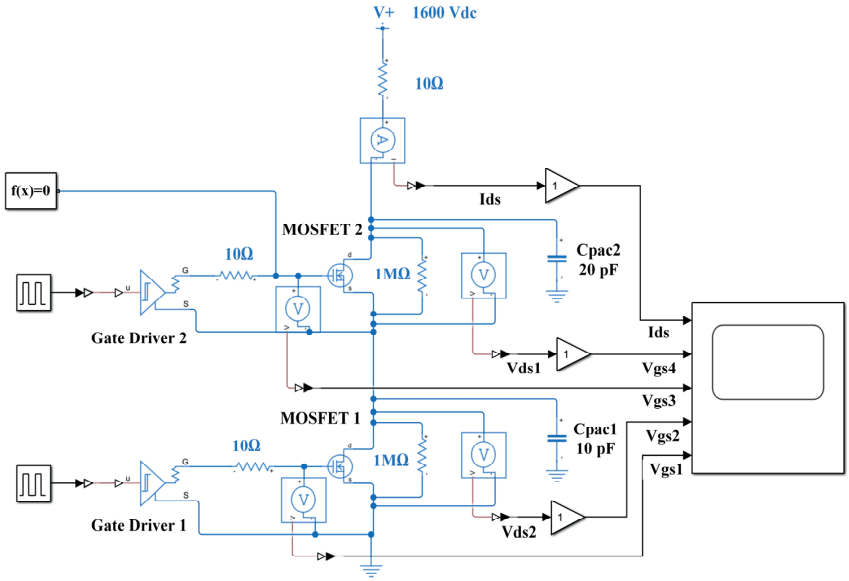
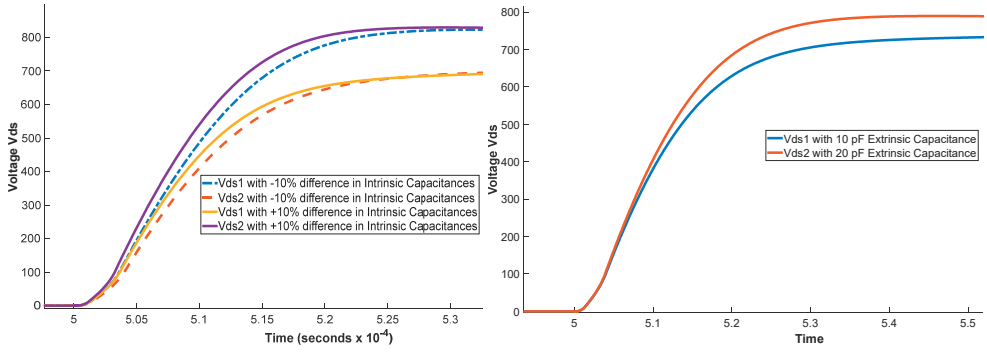


Figure 2.2.5. MATLAB Simulation to evaluate the effect of intrinsic and extrinsic capacitance on voltage sharing.



(a) (b)

Figure 2.2.6. (a) The V_{ds} voltage distribution on two series-connected switches during turn-off due to a mismatch of 10% intrinsic capacitance. (b) The V_{ds} voltage distribution on two series-connected switches during turn-off due to the presence of different extrinsic capacitances.

To conclude, the overall significant factors influencing voltage balancing across series-connected SiC MOSFETs are summarized as follows:

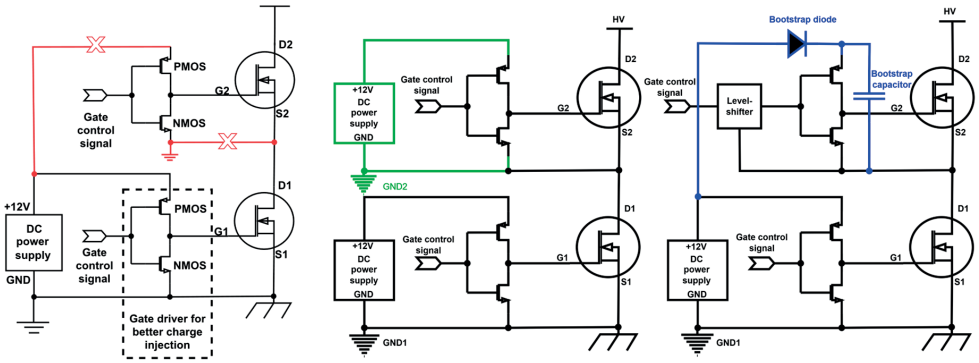
1) Gate signals difference introduced by the gate driver circuit and associated power supply.
2) Process variation in intrinsic parasitic capacitances (C_{gs}, C_{gd}, C_{ds}).
3) External capacitance to ground introduced by the heatsink or DC-DC converters (C_{ps}, C_{pac}).
4) Difference in gate resistances (R_g).
5) Parasitic inductance introduced by the interconnects between series-connected devices.

With the findings from the preliminary simulations and study [20], the gate signal mismatch is one of the most significant causes of the voltage imbalance. The extrinsic capacitances can be minimized using the multi-step packaging approach presented in [20]. The intrinsic tolerances of the above-mentioned variables can be minimized by sorting and careful selection of components from a single production batch where the process variations would be minimal [26] [27].

2.3. Challenges of High-Voltage Isolation and Gate Driving in Series-Connected MOSFETs

In a series connection, all stacked devices are considered as high-side MOSFETs apart from the bottommost MOSFET, as their respective source terminals are floating on the drain of the lower-adjacent MOSFET. The bottommost MOSFET is referred to as low-side MOSFET, as its source terminal is referred to both control and power grounds. Figure 2.3.1(a) depicts a simple push-pull pair gate driving circuit supplied with a 12 V_{dc} power supply and a gate control signal is provided externally. Pay attention to the control and power grounds shorted for the low-side MOSFET. The same power supply cannot be connected to the push-pull pair of high-side MOSFET as the gate (*G2*) must be raised to 12 V with respect to floating source (*S2*) i.e. V_{gs2} = (V_{ds1} +12) V. One commonly employed solution is creating a floating power supply using an isolated DC-DC converter as demonstrated in Figure 2.3.1 (b). However, this technique has a limitation as to cascade multiple high-side devices, multiple DC-DC converters and external gate control signals must be used. These additional components bring various propagation delays which again create the mismatch in the gate signals limiting the ability to switch the series-connected SiC MOSFETs simultaneously.

An alternate non-isolated gate driving integrated solution is shown in Figure 2.3.1 (c) where the floating power supply for the high-side MOSFET is generated by bootstrapping a charged capacitor which floats on the source (S_2). However, this technique also has limitations as the level shifter mechanism introduces a propagation delay, and high-voltage transients can easily reach the blocking capacity of the bootstrap diode and permanently damage the control circuitry and its peripherals.



(a) (b) (c)

Figure 2.3.1. (a) The problem of driving high-side MOSFETs, (b) Isolated gate driving solution, (c) Non-isolated gate driving solution.

2.4. VOLTAGE BALANCING TECHNIQUES FOR SERIES CONNECTED DEVICES

A detailed review of the literature on voltage-balancing strategies [20] – [28] indicates that optimization techniques for both static and dynamic balancing can generally be classified into four major groups: voltage clamping, passive balancing, active gate control, and gate current synchronization.

Figure 2.4.1 attempts to consolidate the voltage balancing techniques and draws the reader's attention to the magnetically coupled gate-driving technique proposed in [29] pursued in this thesis for being simple, open loop and capable to deliver nearly matching gate signals.

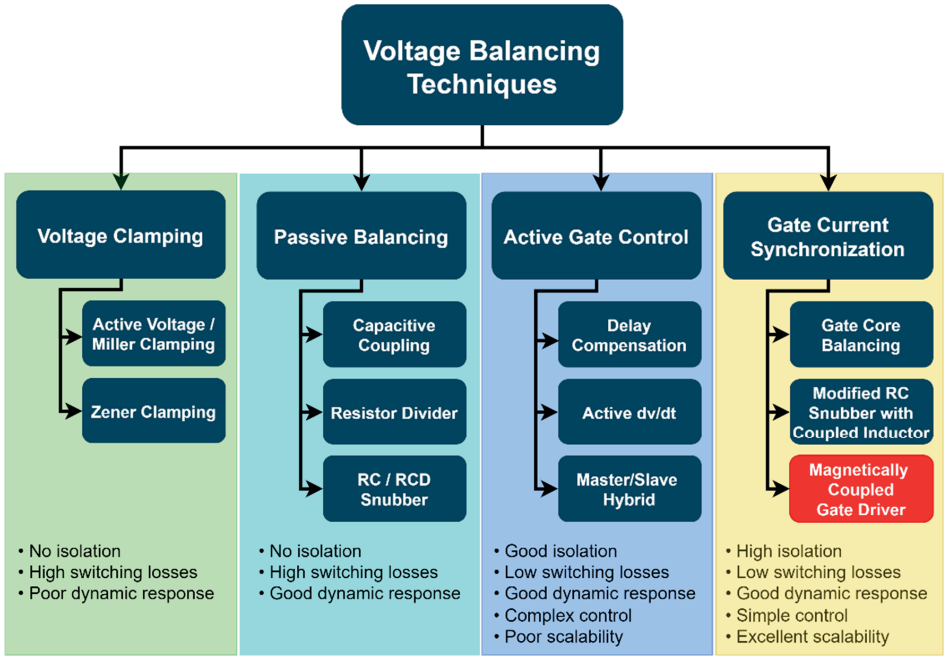


Figure 2.4.1. An overview of voltage balancing techniques.

2.4.1 Voltage Clamping Methods

Voltage clamping methods [30] [31] [32] [33] employ auxiliary components such as clamping diodes, varistors, or snubber circuits to restrict the voltage stress across individual devices. These methods are relatively simple to implement and cost-effective since they require no additional isolation circuitry. However, they suffer from inherently high switching losses because the clamping elements repeatedly absorb excess energy. Moreover, their response time to fast transients is limited, making them less effective in applications requiring precise dynamic voltage balancing.

2.4.2 Passive Balancing Methods

Passive balancing methods [20] [34] typically rely on resistors or RC snubber networks to equalize voltage sharing among series devices. Similar to clamping methods, these techniques do not provide galvanic isolation and therefore have limited flexibility in high-voltage applications. They also introduce additional static and dynamic power losses, which reduce system efficiency. On the other hand, passive balancing offers a relatively good transient response, making it useful in certain medium-voltage, moderate-speed switching applications.

2.4.3 Active Gate Control Methods

Active gate control methods [35] [36] [37] [38] [39] [40] [33] [30] improve upon the limitations of passive techniques by dynamically adjusting the gate signals of the series-connected devices. This approach provides good isolation, low switching losses, and excellent dynamic balancing performance. Nevertheless, the control strategy is significantly more complex, requiring high-speed feedback loops, advanced driver circuitry, and precise coordination of multiple gate signals. Furthermore, as the number of series devices increases, the complexity and cost of the system grow disproportionately, making scalability a key drawback.

2.4.4 Gate Current Synchronization Methods

Gate current synchronization methods [29] [41] [19] represent a promising solution for series-connected wide-bandgap devices. By magnetically or capacitively coupling the gate drive currents, these methods inherently synchronize the switching transitions of all devices in the stack. They offer good isolation, very low switching losses, and excellent dynamic response. Additionally, the control strategy is comparatively simple, and the method scales efficiently to a large number of devices, making it attractive for ultra-high-voltage applications. The primary challenges lie in designing high-quality coupling elements and ensuring insulation reliability at extreme voltage levels, but overall, this approach combines the benefits of efficiency, scalability, and robustness better than the other groups.

A brief comparison chart of these techniques is shown in Table 2.1. Comparison chart of Voltage Balancing Methods for Series-Connected MOSFETs.. From the comparative evaluation, it is evident that voltage clamping and passive balancing methods are attractive for their simplicity and low cost, but their lack of isolation and inherently high switching losses limit their use to relatively low or medium voltage applications. Active gate control, while capable of delivering precise dynamic balancing with reduced switching losses, introduces significant control complexity

and poor scalability, restricting its practicality to systems with only a few devices operating at high frequency.

In contrast, open loop gate current synchronization techniques offer the most balanced trade-off combining high isolation, low losses, simple control, and excellent scalability making them a very prominent candidate for driving SiC MOSFETs connected in series. A comparative analysis of different gate-driver topologies presented by the authors in study [24] demonstrates that magnetically isolated drivers offer a cost-effective and straightforward option for high-frequency operation (2.5–50 kHz) at voltages above 8 kV, especially in cases involving a large number of series-connected devices.

Table 2.1. Comparison chart of Voltage Balancing Methods for Series-Connected MOSFETs.

	Voltage Clamping	Passive Balancing	Active Gate Control	Gate Current Synchronization
Principle	Limits voltage stress using energy-absorbing components	Equalizes voltage via passive networks	Dynamically adjusts gate signals for each device	Synchronizes gate drive currents to align switching transitions
Typical Components	Clamping diodes, varistors, snubber circuits	Resistors, RC snubbers	Active gate driver with feedback, variable gate voltage or impedance	Magnetic or capacitive coupling between gate drives
Isolation	None	None	Yes	Yes
Switching Losses	High (Energy dissipation in clamping elements)	High (Static & Dynamic losses)	Low	Very low
Dynamic Response	Moderate	Moderate to Good	Excellent	Excellent
Control Complexity	Low	Low	High (Requires coordination and feedback loops)	Low
Scalability	Moderate	Moderate	Limited (Grows complex with device count)	High
Key advantages	Low cost and easy to implement	Simple, stable, decent transient behavior	Precise control, efficient, good isolation	High efficiency, strong isolation, easy scalability
Main Limitations	Poor transient response, energy losses, limited to moderate voltage	Inefficient at high frequency, limited voltage scalability	High cost, complexity, synchronization required	Design of coupling components and insulation reliability is critical
Best suited applications	Low voltage & low frequency systems where cost is main concern	Medium voltage and moderate speed converters	High frequency converters with small number of devices	High voltage multi kV systems

2.5. Chapter Conclusions

In this chapter the fundamental principles of the series-connected MOSFETs topology are presented and its key advantages are highlighted over single high-voltage semiconductor devices. By employing multiple commercially available low-voltage SiC MOSFETs in series, the topology enables higher voltage ratings while benefiting from lower cost, higher switching speed, improved efficiency, and greater power density compared to single high-voltage devices.

The mechanisms governing voltage sharing in series-connected MOSFETs were examined and the primary factors responsible for voltage imbalance under both static and dynamic operating conditions were identified. Particular emphasis was placed on dynamic voltage imbalance, where mismatches in gate drive timing, gate voltage slew rates, intrinsic device parameter variations, and extrinsic parasitic elements can lead to severe overvoltage stress on individual devices. In addition, the challenges associated with high-voltage isolation and high-side gate driving were discussed, demonstrating how conventional isolated and non-isolated driving approaches introduce propagation delays, insulation constraints, and reliability concerns that limit synchronous switching in series connected device configurations.

Finally, a structured overview of voltage-balancing techniques for series-connected devices was provided, classifying them into voltage clamping, passive balancing, active gate control, and gate current synchronization methods. A comparative analysis of these approaches highlighted their respective advantages and limitations in terms of isolation capability, switching losses, control complexity, and scalability. This overview finally directed the focus on transformer coupled gate drivers and advanced gate-current synchronization technique discussed in subsequent chapters.

3

"Harmony makes small things grow; lack of it makes great things decay."

— Sallust

3. Transformer Coupled Gate Current Synchronization Technique With Programmable Frequency and Duty Cycle

The previous chapter explained the series connected MOSFETs topology, the associated challenges and an overview of the different techniques to achieve a voltage balance across series connected devices. This chapter introduces a novel gate driving technique to overcome challenges like low voltage side isolation, matching gate signals and detachment of switching frequency from transformer frequency to achieve user defined programmable switching frequency.

3.1. Transformer Coupled Gate Drivers

A High-Voltage Arbitrary Waveform Generator (AWG) requires a scalable, cost-effective, and simple open-loop voltage balancing gate driver with good galvanic isolation that can provide a user-defined on / off function since feedback networks increase the complexity in terms of design layout and isolation. The simplicity and cost effectiveness of the high-voltage switch will bring a fast price reduction in the learning curve of AWG technologies [42]. The ability to independently control on and off duration is essential for synthesizing complex high-voltage waveforms, which are needed to test grid assets insulation in future power-electronics-dominated energy grids [7]. Transformer-coupled gate driving techniques can satisfy the requirements of scalability, simplicity, open-loop voltage balancing, and high galvanic isolation; however, their operation is inherently constrained by the transformer switching frequency, which prevents the series-connected switches from being maintained in a on or off state as per custom defined frequency and duty cycle.

3.2. Transformer Coupled Gate Current Synchronization Technique With Programmable Duty Cycle

To overcome the limitations imposed by transformer-frequency-dependent gate driving, a novel gate-current-synchronizing driver with programmable frequency and duty cycle is proposed in this thesis for series-connected SiC MOSFETs, enabling user-defined on/off control while retaining synchronous switching and high galvanic isolation through a transformer-coupled architecture. The concept diagram is shown in Figure 3.2.1. Figure 3.2.2 shows the block diagram of the proposed gate driver design, broadly divided into primary and secondary-side drivers.

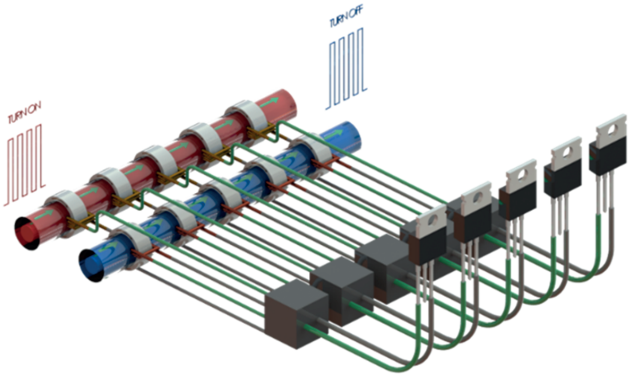


Figure 3.2.1. Concept diagram - Pulse transformers arrangement with high voltage insulated cable passing through toroidal cores.

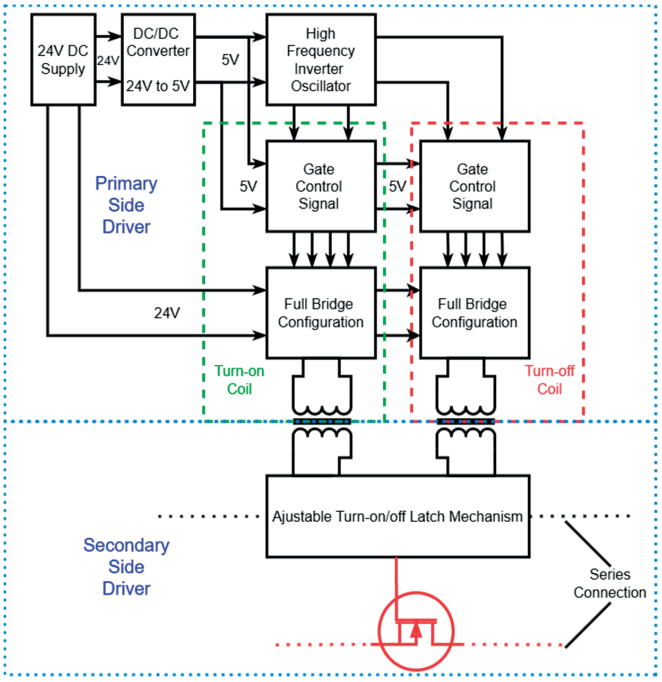


Figure 3.2.2. Block diagram for the proposed gate driver.

On the primary side, there are two single-turn high-voltage insulated turn on / off loops driven with ± 24 V bipolar pulses using full-bridge converters. The turn-on and turn-off coils are driven complimentary to each other. The secondary side driver includes an adjustable turn-on / off latch mechanism for arbitrary switching functions for the SiC MOSFETs connected in series. Each series-connected SiC MOSFET will have its own 2 secondary coils, one for turn-on and the other for turn-off and latch mechanisms. The power required for the gate control is fed externally from a 24 V_{dc} power supply. An onboard non-isolated DC-DC converter generates a 5 V logic power supply to power up the respective digital control circuitry.

The detailed circuit is elaborated in Figure 3.2.3. The circuit operation starts from the primary side of the circuit with the oscillator. Figure 3.2.4 shows the corresponding timing diagram illustrating the modulation process to generate respective gate control pulses for the full-bridge pulse generator. The user defined digital turn on and turn off signals are modulated and converted into two streams of mutually exclusive pulses. These streams work together on the primary side to drive the full bridge converter, generating ± 24 V bipolar voltage pulses across the single turn high voltage turn on loop during the entire period of the on signal. The turn-off coil remains inactive during this time. The turn-off digital signal is converted to drive the full bridge in similar way across the single turn high voltage turn off loop and the other coil remains inactive during this period. On the secondary side driver section, a small signal MOSFET latch facilitates controlling the switching frequency and duty cycle of the series-connected SiC MOSFETs, irrespective of the frequency at which the pulse transformer is driven. The turn-on / off latch mechanism consists of two secondary windings wound on two toroidal cores and two low-voltage signal MOSFETs M_1 and M_2, for each series-connected SiC MOSFET. During turn on, a half-wave rectifier is constructed with Schottky diode D_3 and C_{iss} capacitance of SiC MOSFETs, which is clamped at 15 V with Zener diode Z_3 as recommended in [22] to drive the SiC MOSFET with a recommended voltage of +15 V for optimum switching performance. A small signal MOSFET used for M_2 is driven directly with the transformer's bipolar voltage. When the turn-on coil is energized, the drain of the M_2 transistor ensures that the capacitor C_1 is discharged and transistor M_1 cannot turn on. Similarly, when the turn-off coil is energized, the gate of the SiC MOSFET is pulled to negative potential to avoid false turn-on of SiC MOSFETs in series.

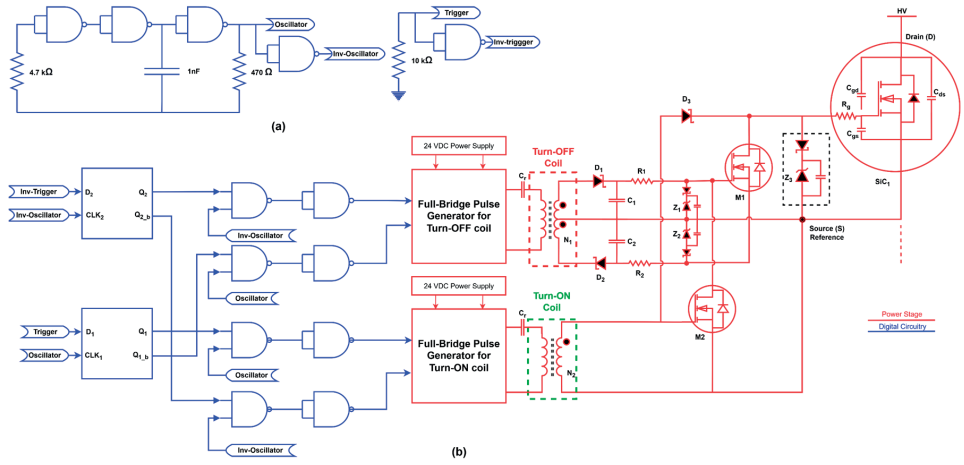


Figure 3.2.3. (a) Oscillator circuit (b) Gate current synchronization driving circuit with programmable frequency and duty cycle.

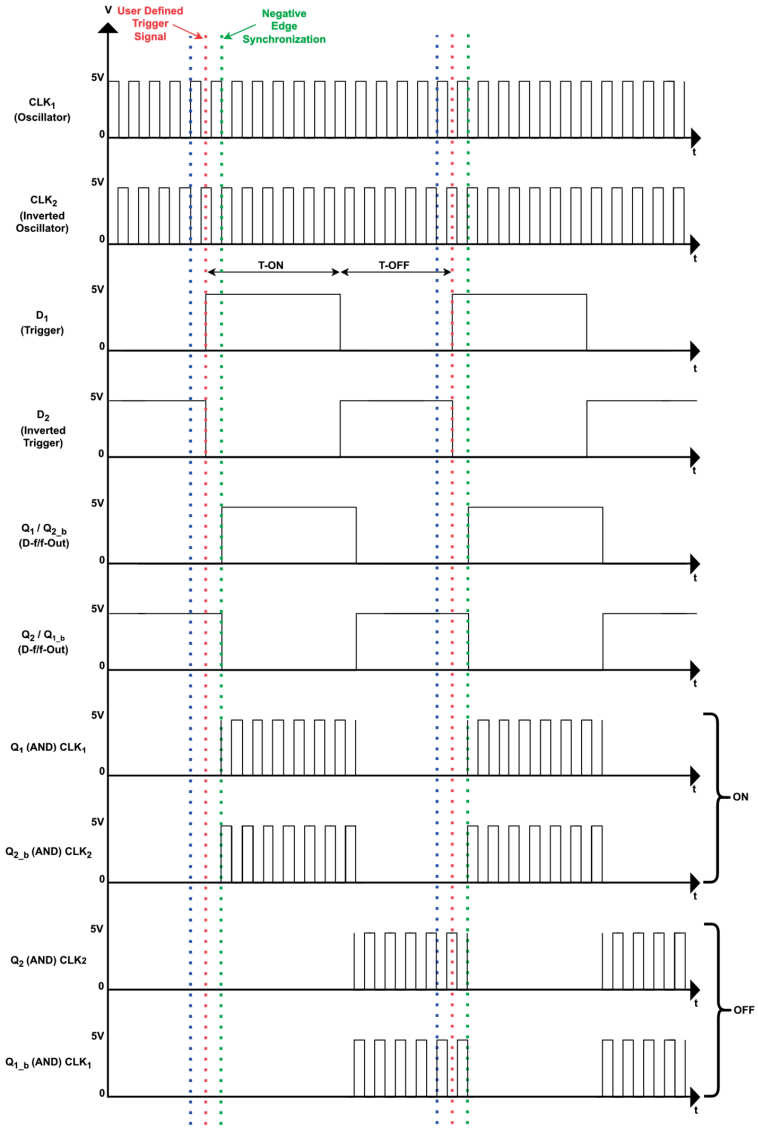


Figure 3.2.4. Detailed timing diagram for circuit presented in Figure 3.2.3 where user defined on and off trigger signals are modulated over 167 kHz complementary digital signals to drive the coil between the full bridge circuits.

The turn-off coil is designed as a center-tapped secondary to generate a dual polarity supply. During the turn-off, two half-wave rectifiers are constructed with the help of Schottky Diodes connected with a center-tapped transformer. The center tap of the transformer is connected to the mid-point of the split capacitor arrangement. Zener diode Z_1 is selected with a reverse breakdown potential of 12 V connected to the gate of M_1, whereas Zener diode Z_2 has a 4.7 V reverse breakdown voltage connected to the source of M_1. This configuration subjects the gate of the SiC MOSFET during turn off to negative voltage instead of ground to better extract charges from gate capacitance C_{iss}. The turn-on and turn-off coils are energized in a mutually exclusive way, and the latch mechanism is achieved.

Zener diodes are typically used in reverse bias for voltage clamping, with their P-N junction acting as a capacitance that decreases with increasing reverse voltage until the Zener breakdown point, where it stabilizes [43]. At high frequencies (around 100 kHz) with fast switching speeds (10 µs), this capacitance can distort the diode's behaviour. To improve clamping, a Schottky diode and a shunt capacitance are added, allowing efficient clamping without the charging/discharging of the Zener diode's capacitance, as highlighted in the black box in Figure 3.2.3 (b) [43]. The Schottky diode, characterized by its negligible reverse-recovery charge and low junction capacitance, provides a fast and low-impedance clamping path during transient events. The added shunt capacitance serves as the primary charge-buffering element, effectively absorbing high-frequency voltage spikes and controlling dv/dt. As a result, the Zener diode is relieved from repeatedly charging and discharging its intrinsic junction capacitance, thereby minimizing waveform distortion and improving clamping stability. This arrangement ensures more predictable voltage limiting behavior under fast switching conditions and enhances overall high-frequency performance.

3.2.1 Operational Modes

Figure 3.2.5 describes the turn-on mode of the switch and highlights the components responsible for turning on the series-connected SiC MOSFETs. The blue measurement probes direct the reader to follow the timing diagram shown in Figure 3.2.7. The positive half pulse propagates through diode D_3 and clamped by Zener Diode Z_3 at +15V, charges the gate capacitance C_{iss} of the main series connected SiC MOSFET SiC_1 to gate voltage V_{gs3} as shown in Figure 3.2.5(a). As soon as the input voltage becomes equal to or less than the gate voltage V_{gs3}, the diode D_3 becomes reverse-biased and stops the flow of charge across the gate-source terminal from draining. The diode remains in reverse-biased mode during the negative half cycle and becomes forward-biased as soon as the input voltage becomes greater than the gate voltage V_{gs3} of the SiC_1 MOSFET, as shown in Figure 3.2.5 (b). The SiC_1 MOSFET during this whole period remains on. At the same time, this positive half cycle of the transformer pulse turns on the small signal MOSFET M_2 which drains the gate charge of M_1 to keep it off. It is pertinent to mention that once the gate capacitance is fully charged, the main SiC MOSFET is fully turned on, and the gate capacitance behaves like an open circuit. However, since a very small leakage current still flows through the gate-source terminal, the next positive pulse replenishes this tiny loss, and a very little current flows through the circuit during the subsequent positive pulses.

Similarly, Figure 3.2.6 depicts the active components of the secondary side driver circuit during the turn-off phase of the series connected SiC MOSFETs. The positive half cycle across the turn off secondary propagates through diode D_1 and clamped by Zener Diode Z_1 at +12V, charges the gate capacitance C_{iss} of the small signal MOSFET M_1 to gate voltage V_{g1} as shown in Figure 3.2.6 (a). The only difference with the turn-on coil during turn-off is that a center tap transformer configuration is used that allows the negative half of the secondary voltage to propagate through diode D_2 clamped by Zener Z_2 at -5 V and establish a negative voltage across the source terminal of the small signal MOSFET M_1 during the negative half cycle. This topology generates a dual polarity supply from the turn-off coil across capacitors C_1 and C_2 switching the small signal MOSFET M_1 to on state. The drain-source path of this MOSFET discharges the stored gate charge across the main SiC MOSFET SiC_1. The negative polarity at the Source terminal of M_1 is generated to pull down and better extract the stored charge switching the main SiC MOSFET SiC_1 to off state.

This whole cycle is synchronously executed across all series connected SiC MOSFETs, providing them with matching gate voltages and switching them at the same time ensuring nearly even voltage distribution among them all.

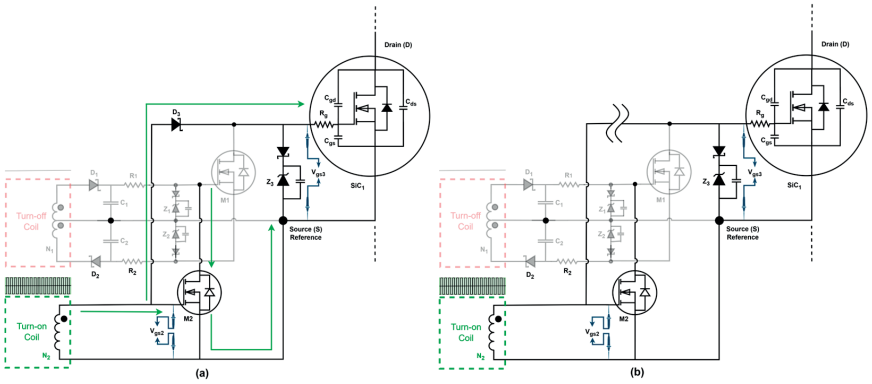


Figure 3.2.5. Illustration of the turn-on mechanism for series-connected SiC MOSFETs, highlighting M2's role in synchronizing with SiC1 and controlling M1, with D3 charging Ciss to switch SiC1 ON, and timing diagram correlation with Figure 3.2.4. (a) Circuit during positive half voltage pulse. (b) Circuit during negative half voltage cycle.

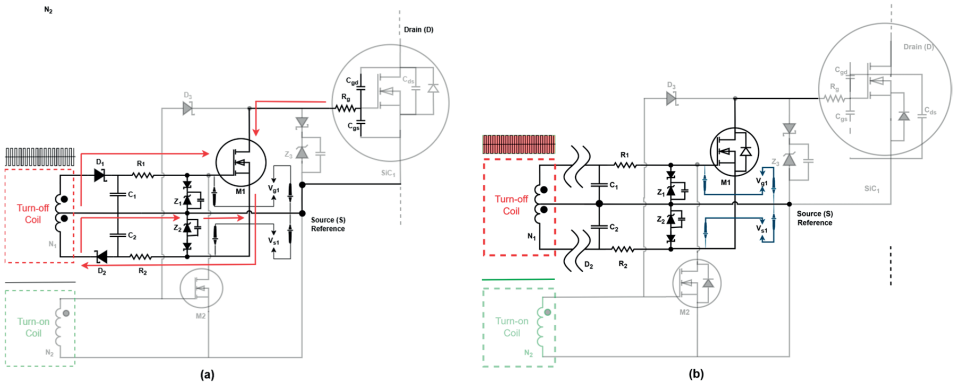


Figure 3.2.6. Active components in the secondary driver circuit during turn-off phase, illustrating dual polarity supply generation and timing diagram correlation with Figure 3.2.4. (a) Circuit during positive half voltage pulse. (b) Circuit during negative half voltage cycle.

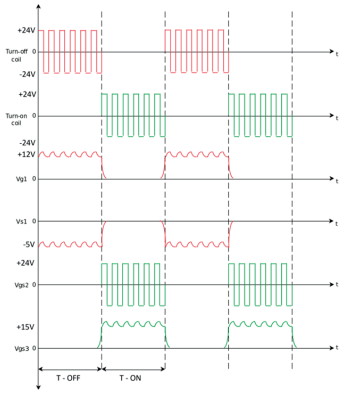


Figure 3.2.7. Voltage waveforms for the functional schematic presented in Figures 3.2.5 and 3.2.6.

3.2.2 Modulator Circuit Design

The transformer coupling with the primary compensation capacitor is driven by a full-bridge circuit. The gate pulses for the full-bridge square wave generator are integrated into the primary side driver, as depicted in Figure 3.2.3. A 5 V trigger input is taken externally specifies the user-defined frequency and duty cycle for the series-connected SiC MOSFETs. An internal inverter-based oscillator is implemented using Schmitt-triggered two-input NAND gates to generate a stable high-frequency excitation signal. By configuring one NAND gate as an inverting amplifier with a feedback network consisting of a resistor and capacitor, a relaxation-type oscillator is formed. The oscillation frequency is primarily determined by the RC time constant and the Schmitt-trigger threshold levels, enabling predictable and stable frequency generation suitable for driving the subsequent excitation stage. The oscillating frequency is tuned using equation 1 [44] and the full-bridge circuit drives the pulse transformers at the tuned frequency. The thresholds V_{T+} and V_{T-} are described in the datasheet of the NAND Gate IC [45].

$$f_A = \frac{1}{2\,RC\,ln\left(\frac{V_{T+}}{V_{T-}}\right)} \qquad (1)$$

Where f_A is the frequency of the digital oscillator.

3.2.3 Transformer Design

The transformer consists of primary and secondary windings, each incorporating specific reactive components. The primary winding has a self-inductance L_1 in series with a compensation capacitor C_r, forming a resonant LC network. The secondary winding has a self-inductance L_2 in series with a rectifier diode and a capacitive load C_{load}, which corresponds to the MOSFET input capacitance C_{iss}.

The selection of the toroidal core is primarily governed by magnetic saturation constraints and inductance requirements. The core area A is determined using equation:

$$A = \frac{E}{k\,f\,B_m N_p} (2)$$

To ensure that the magnetic flux density does not exceed the allowable maximum B_m, following equations were used to verify that the required inductance could be achieved without exceeding the permissible flux density under peak current conditions

$$B = \frac{LI}{NA} \qquad (3)$$

$$L = \frac{BNA}{I} \qquad (4)$$

Since minimizing leakage inductance is critical for ultrafast gate-current transfer, the number of primary turns was intentionally limited to one ($N_p = 1$). However, reducing the number of turns increases the flux density for a given applied voltage, making adequate core cross-sectional area essential to prevent saturation. To ensure safe operation, the maximum flux density was evaluated under worst-case conditions. For a 24 V nearly square-wave excitation at 167 kHz with a single primary turn, the peak flux density is approximated by:

$$B_{max} = \frac{V}{4fNA_e} (5)$$

For the selected TX13/7.9/6.4-3C90 toroidal core (outer diameter 13 mm, inner diameter 7.9 mm, height 6.4 mm), the radial thickness is 2.55 mm, resulting in an effective cross-sectional area

$$A_e \approx 2.55 \times 6.4 = 16.32 \text{ mm}^2 = 16.32 \times 10^{-6} \text{ m}^2.$$

Substituting into the flux equation yields

$$B_{max} = \frac{24}{4 \times 167000 \times 1 \times 16.32 \times 10^{-6}} \approx 0.22 \text{ T}.$$

This value is well below the typical saturation flux density of 3C90 ferrite (approximately 0.35–0.4 T), confirming that the selected core operates safely below saturation [46]. Furthermore, 3C90 is a well-established MnZn ferrite material characterized by low core losses in the 20–200 kHz frequency range, making it suitable for the intended operating frequency. The single-turn primary design simultaneously minimizes leakage inductance while maintaining safe magnetic operation and high-speed switching performance.

To evaluate the coupling coefficient between a high-voltage insulated loop and secondary windings on toroidal cores, inductance measurements were carried out using secondary side open-circuit (O.C.) and short-circuit (S.C.) tests using a Keysight U1733C LCR meter. Table 3.1 demonstrates the results for performed O.C. / S.C. tests, and the coupling coefficient is computed as follows [47], [48].

$$\boldsymbol{k = \sqrt{1 - \frac{L_1(S.C.L_2)}{L_1(O.C.L_2)}} = \frac{M}{\sqrt{L_1 L_2}}} \quad (6)$$

Where L_1, L_2 are self-inductances, L_1 *(S.C* L_2*)* is primary side inductance with secondary side winding short circuited and L_1 *(O.C* L_2*)* is primary side inductance with secondary side open circuited.

Table 3.1. LCR meter measurements for computing coupling coefficient

N_1	N_2	L_1(µH)	L_2(µH)	$L_1(O.C.L_2)$	$L_1(S.C.L_2)$	M(µH)	k
	1		9.04	10.09	8.27	0.7	0.425
	2		20.7	10.55	8.38	1.13	0.454
1	3	0.3	30.8	10.3	8.45	1.28	0.423
	4		55	10.5	8.5	1.77	0.436
	5		76	10.4	8.45	2.07	0.433

The number of turns of the secondary coils must also be minimal to reduce the leakage inductance. With calculated coupling coefficients, the minimum number of turns that can produce a voltage above the gate threshold (V_{th} 4.5 V and $V_{GS\text{-}ON}$ +15 V for SiC MOSFETs) is 2. Therefore, turns for the secondary side are selected to be 2. Since the turn-off coils have small signal MOSFETs, which can be switched at 12 V, the turn-off coil is also given 2 turns with a center tap. This configuration creates a symmetric circuit.

3.2.4 Resonant Circuit Design

To mitigate transformer parasitics, a resonant compensation network is used [49] - [50]. The primary side of transformer consists of a self-inductance L_1 in series with a capacitor C_r, while the secondary includes L_2, a rectifier diode, and the gate capacitance C_{iss} acting as the load. Together these elements form an L_3C_2 circuit with distinct resonant frequencies on both sides of the transformer. Figure 3.2.8 shows the simplified compensation network. To analyze its behavior, a MATLAB simulation was designed using a mutual inductance model with one primary and four secondary windings. The study examined the resonant characteristics over a frequency range from a few kHz up to several MHz, with the diode modelled as a short circuit during conduction.

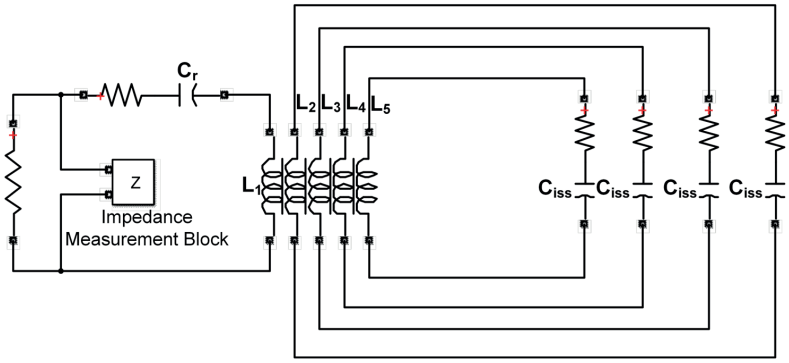


Figure 3.2.8. MATLAB Simulink model illustrating the primary-side impedance characteristics of a resonant transformer circuit.

The transformer's mutual and self-inductances are represented in the inductance matrix L, initialized as follows:

$$L = \begin{bmatrix} L_1 & M_{12} & M_{13} & M_{14} & M_{15} \\ M_{21} & L_2 & M_{23} & M_{24} & M_{25} \\ M_{31} & M_{32} & L_3 & M_{34} & M_{35} \\ M_{41} & M_{42} & M_{43} & L_4 & M_{44} \\ M_{51} & M_{52} & M_{53} & M_{54} & L_5 \end{bmatrix} \quad (7)$$

Here, L_1 denotes the self-inductance of the primary loop measured with the secondary side open, while L_2, L_3, L_4, and L_5 represent the self-inductances of the secondary windings, measured with the primary side open. Since the secondary toroidal cores are physically isolated and exert identical influence on the primary while having negligible coupling among themselves, the inductance matrix of the transformer can be simplified as follows:

$$L = \begin{bmatrix} L_1 & M_{12} & M_{13} & M_{14} & M_{15} \\ M_{12} & L_2 & 0 & 0 & 0 \\ M_{13} & 0 & L_3 & 0 & 0 \\ M_{14} & 0 & 0 & L_4 & 0 \\ M_{15} & 0 & 0 & 0 & L_5 \end{bmatrix} \quad (8)$$

The equivalent impedance of the network, as derived in [51], can be expressed as:

$$Z_{eq}(j\omega) = j\omega L_1 + \frac{1-L_2C_r\omega^2}{j\omega C_r(1-\omega^2 L_2 C_{iss})} \quad (9)$$

This representation highlights the dual-resonant nature of the circuit, where the primary and secondary sides resonate at different frequencies, producing a wide impedance plateau favorable for stable operation. The impedance response observed from the primary side, as shown in Figure 3.2.9, reveals two distinct resonant frequencies. The primary resonance frequency is governed by the compensation capacitor C_r and the primary self-inductance L_1, and can be expressed as [51]:

$$f_p = \frac{1}{2\pi\sqrt{L_1 C_r}} \quad (10)$$

Where f_p is the primary side resonance frequency, and L_1 denotes the self-inductance of the primary side.

On the secondary side, the circuit is connected to a capacitive load C_{load}, which represents the SiC MOSFET's gate capacitance C_{iss}. Simulation results indicate that the secondary-side resonance frequency is governed by the interaction between the secondary leakage inductance L_{s-lk} and the load capacitance C_{load}, and is expressed as:

$$f_s = \frac{1}{2\pi\sqrt{L_{s-lk}\, C_{load}}} \quad (11)$$

Due to the small gate capacitance C_{iss}, the secondary side exhibits a relatively high resonance frequency. The network shown in Figure 3.2.10 (a) can be simplified into the reduced L_2C_2 model illustrated in Figure 3.2.10 (b). For the case of a single secondary winding, the leakage inductance can be expressed as:

$$L_{s-lk-1} = L_2 - \frac{M^2}{L_1} \quad (12)$$

where L_{s-lk-1} is the effective secondary leakage inductance with just one secondary winding, L_2 is the secondary side self-inductance, M is the mutual inductance between primary and secondary, and L_1 is the self-inductance of the primary side.

Adding each secondary winding changes the effective leakage inductance of the secondary according to the following relationship:

$$L_{s-lk-n} = L_2 - n\,\frac{M^2}{L_1} \quad (13)$$

where n is the number of secondary windings.

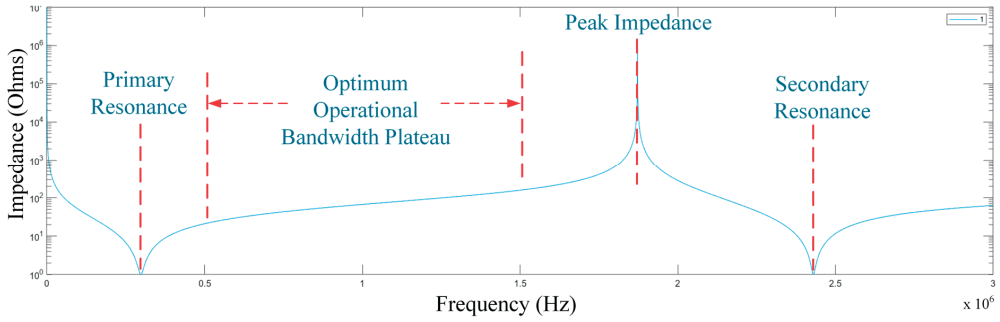


Figure 3.2.9. Simulated impedance response of the L_3C_2 circuit, exhibiting dual resonance peaks and indicating the optimal operating bandwidth.

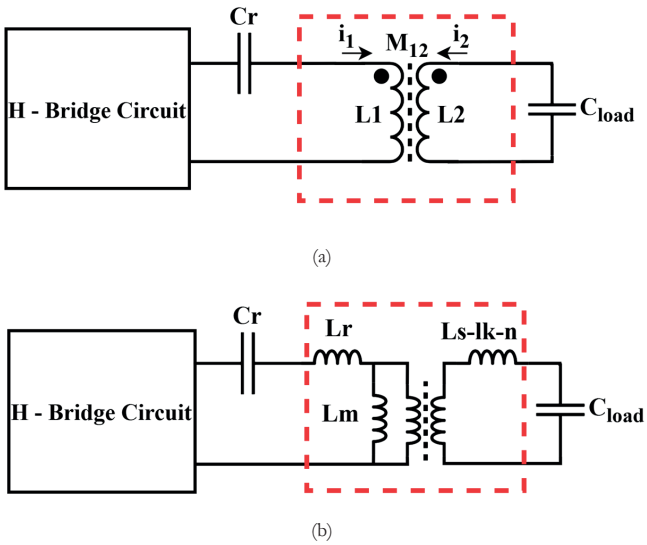


Figure 3.2.10. Simplified equivalent model of the resonant transformer circuit for analysis [50] [51]**. (a) Resonant transformer showing self/mutual inductances, compensation, and load capacitors. (b) Equivalent circuit illustrating leakage and magnetizing inductances with associated capacitors.**

Equations (5) and (6) indicate that adding each secondary winding shifts the resonance frequency of the secondary side higher. They also reveal that the effective leakage inductance of the secondary which defines the resonance point of the secondary *LC* circuit is influenced not only by the mutual inductance but also by the self-inductance of the primary side.

The quality factor, which characterizes the sharpness of the resonance, is given by:

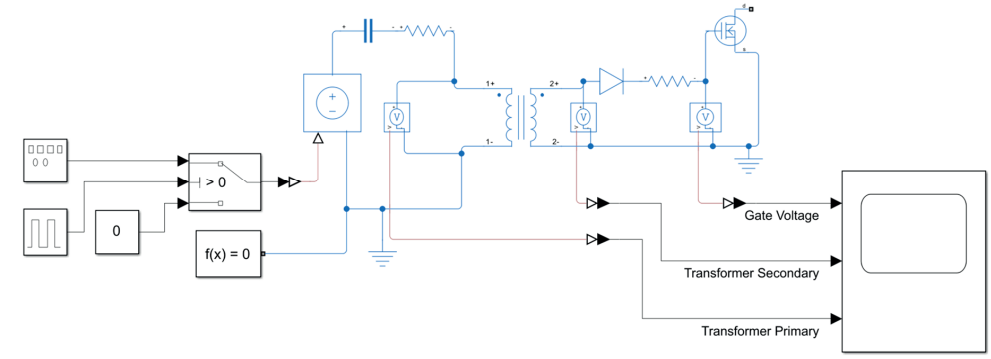
$$Q = \frac{1}{R_{eq}} \sqrt{\frac{L_1 + L_2}{C_r + C_{iss}}} \quad (14)$$

A high Q-factor indicates stronger resonance and reduced damping, enhancing voltage amplification but potentially introducing peaking effects if not properly tuned. Therefore, careful

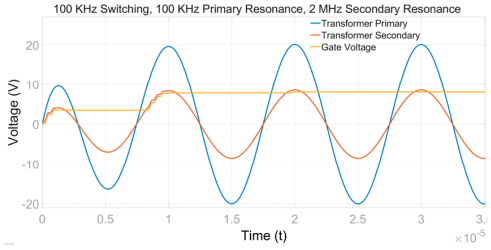
selection of C_r and transformer inductances ensures operation within the impedance plateau, avoiding excessive resonance while maintaining high dV/dt performance [52].

The primary resonance frequency can be tuned by choosing a suitable primary compensation capacitor C_r, enabling adaptation to the desired switching speed and other system requirements. Since the main purpose of the circuit is to charge the gate capacitance of the series-connected SiC MOSFETs during the first pulse, using separate windings for turn-ON and turn-OFF, it does not require operation at a fixed resonance frequency. This tuning can be achieved by selecting an appropriate resonant frequency along with the corresponding primary compensation capacitor. The critical factor is the dV/dt of the rising edge of the driving pulse, rather than the entire waveform. The impedance characteristics shown in Figure 3.2.9 indicate that the impedance reaches its minimum near the primary resonance frequency. Operating close to this point results in increased current flow, which, due to transformer parasitics and source resistance, impedes voltage rise. Conversely, beyond the impedance plateau, the impedance magnitude increases, adversely affecting circuit performance. Beyond the secondary resonance, the system behaves as a second-order resonant converter, an operationally viable mode but one that introduces high-frequency challenges such as EMI and the need for extremely small passive components. Hence, the optimal operating region is within the impedance plateau between the primary and secondary resonance frequencies, as illustrated in Figure 3.2.9. The primary resonance frequency can be adjusted to meet the desired high-voltage dV/dt requirements by appropriately selecting the compensation capacitor C_r.

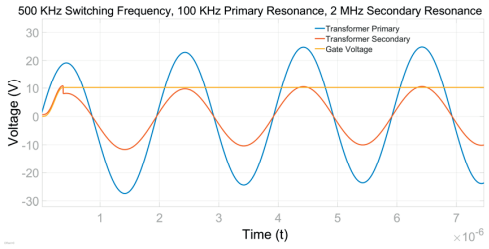
A MATLAB simulation, shown in Figure 3.2.11 (a) was conducted to study the effect of different switching frequencies on the primary and secondary resonant frequencies. The primary resonance is determined by the compensation capacitor and primary inductance, while the secondary resonance depends on the secondary inductance and the gate capacitance of SiC MOSFET. With the primary resonance set at 100 kHz and the secondary at 2 MHz, results for a 100 kHz switching frequency in Figure 3.2.11 (b) show that the gate voltage does not build up during the first pulse. Since the circuit's goal is to charge the gate in the initial pulse, operating at the primary resonance frequency is unsuitable. Figure 3.2.11 (c) shows that a 500 kHz switching frequency allows the peak gate voltage to develop within the first pulse. Similar behavior is observed at 1.5 MHz and 2 MHz switching frequencies (Figure 3.2.11 (d) and (e). However, at 6 MHz (Figure 3.2.11 (f)), the gate voltage fails to reach its peak during the first pulse and requires multiple pulses to fully charge the gate capacitor. Figure 3.2.11 (g) presents results for a 2.5 MHz switching frequency, with the primary resonance set at 3 MHz and the secondary at 2 MHz.



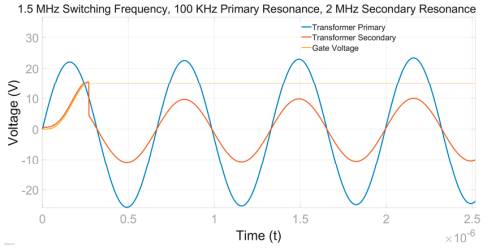
(a)



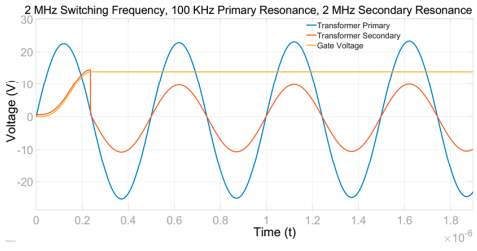
(b)



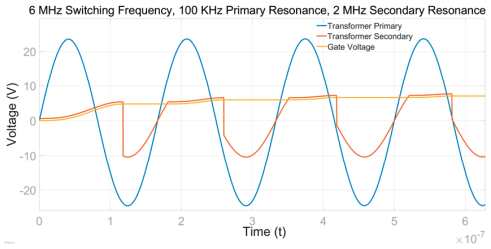
(c)



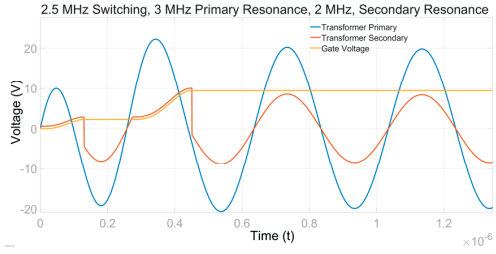
(d)



(e)



(f)



(g)

Figure 3.2.11. Simulink model and voltage waveforms of the resonant transformer showing effects of switching and resonant frequency variations. (a) Model. (b–f) Waveforms at 100 kHz–6 MHz. (g) 2.5 MHz case with higher primary resonance.

The simulation demonstrates that when the primary resonance exceeds the secondary resonance, the peak gate voltage cannot be achieved in the first pulse. Therefore, the primary resonance should always be equal to or lower than the secondary resonance.

Since, the primary objective of the proposed circuit is to charge the gate capacitance of the series-connected MOSFETs during the first driving pulse, rather than to operate at a specific resonant frequency. Owing to the use of separate transformer windings for turn-on and turn-off, resonance-based operation is not required. The LCLC compensation network enables flexible operation over a wide linear frequency range between the primary-side resonance frequency f_{primary} and the secondary-side resonance frequency $f_{\text{secondary}}$, as illustrated in Figure 3.2.9. The operating frequency can be freely selected by appropriately choosing the primary-side compensation capacitor C_r, allowing adaptation to different switching-speed and system requirements. Consequently, the critical design parameter is the dv/dt of the rising edge of the gate-driving pulse, which determines effective gate charging and may be positioned anywhere within the dv/dt range bounded by the primary- and secondary-side resonance frequencies, as shown in Figure 3.2.9. Frequencies between 100 kHz and 500 kHz offer an optimal trade-off, avoiding large components and excessive losses, and in this work, a 167 kHz operating frequency was chosen to balance efficient power transfer, manageable component size, and minimized losses. This frequency was chosen as it is easy to program gate signals using general Arduino Microcontroller with different frequency and duty cycles. While higher frequencies are feasible and potentially can improve performance significantly, they may introduce challenges such as more electromagnetic interference (EMI) and thermal management issues.

3.2.5 Temporal Analysis

The timing diagram of the voltage waveforms is shown in Figure 3.2.12. The circuit has two dynamic phases and two steady-state conditions during turn ON and OFF. Positive waveforms shown in Figure 3.2.12 (a) are both similar for turn ON and turn OFF coils. However, the negative waveform shown in Figure 3.2.12 (b) is only for turn OFF coil which has a center tapped transformer configuration. Moreover, for turn OFF coil, the voltage waveforms and corresponding timing sequences (t0 to t7) in Figure 3.2.12 (a) and (t8 to t12) in Figure 3.2.12 (b) are occurring at the same time.

1) **0 to t_0**

From 0 to t_0, the voltage rises on the secondary side of the transformer to the miller plateau. The gate starts charging at this instant and the MOSFET turns on after crossing the threshold voltage V_{th}.

2) **t_0 to t_1**

From t_0 to t_1, the secondary voltage increases and is clamped by the Zener Diode. The gate capacitance C_{iss} is charged, and the gate voltage V_{gs} reaches the clamped secondary voltage. The diode allows charges to flow in the forward direction only during this time period.

3) **t_1 to t_2**

The circuit enters the steady state and during this time period very little charge flows since the gate capacitance is fully charged. The gate voltage V_{gs} is maintained at a steady level by Zener Diode.

4) **t_2 to t_3**

When the secondary voltage drops below the gate voltage, the top diode enters reverse bias, halting charge flow in the opposite direction and maintaining the gate voltage. This sudden diode turn-off stops the current flow, creating a negative EMF that causes a sharp voltage drop and oscillations due to the inductance of the turn-on transformer and the circuit's capacitances. The circuit in this state behaves like an open circuit. Although the gate-source resistance is in the megaohms range, a very little gate leakage current is still able to flow during this short duration, but this current is too small to result in any significant loss of gate voltage.

5) **t_3 to t_4**

When the next positive pulse reaches above the gate voltage, the diode is forward biased again to allow very little charge to flow again to replete the charge lost during the second phase of the cycle. As a result a small ripple appears on top of the gate voltage in line with secondary voltage signal. This ripple can be minimized by increasing the transformer switching frequency to ensure fast replenishment of the gate charge and minimize the discharge.

6) **t_4 to t_5**

The circuit enters the steady state.

7) **t_5 to t_6**

The circuit enters the dynamic state of turning off from t_5. At this instant, the MOSFET M_1 turns on and provides path to extract charges from the gate of main SiC MOSFET. It reaches to threshold voltage V_{th} and the main SiC MOSFET turns off below this voltage.

8) **t_6 to t_7**

From t_6 to t_7, the gate charge continues to drop and the gate voltage comes down to zero.

9) **t_7 to t_8**

The voltage on the lower half of the center-tapped secondary side rises and is clamped at -5 volts by the Zener diode across the source terminal of the turn-off MOSFET M_1 with respect to the ground.

10) **t_8 to t_9**

The circuit enters the steady state, and this negative voltage ensures better charge extraction from the gate of the main SiC MOSFET that is connected to the drain of turn-off MOSFET M1 during the off cycle.

11) **t_9 to t_{10}**

The charge is replenished again during this phase, and a small negative ripple appears.

12) **t_{11} to t_{12}**

The turn-off coil stops getting the transformer pulses, and the negative voltage goes down to the ground during this phase.

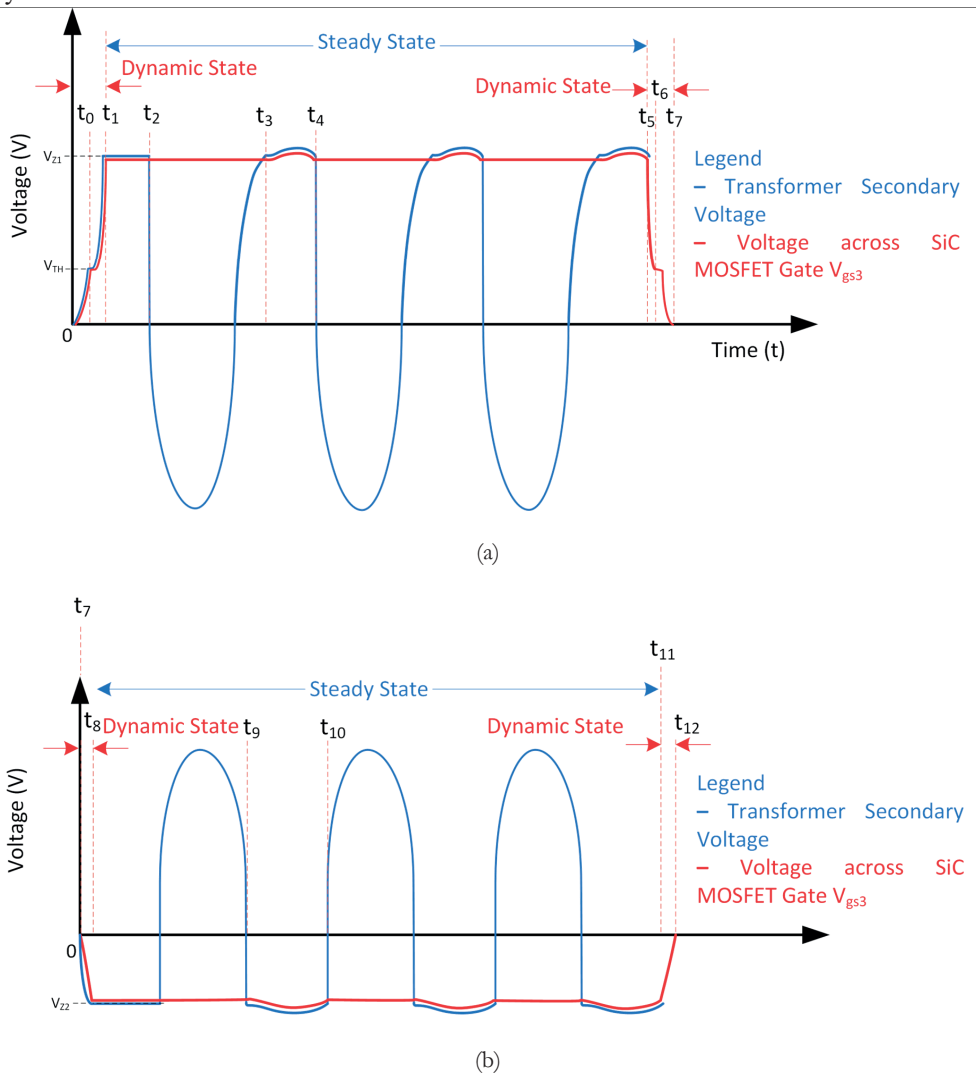


Figure 3.2.12. Voltage waveform profiles across secondary and across SiC MOSFET gate. (a) The voltage waveforms across the gates of MOSFETs connected on secondaries. (b) The voltage waveforms across the lower half of the turn off secondary coil.

3.2.6 Experimental Results

The prototype board with 5 IMW120R220M1H Infineon CoolSiC 1.2 kV SiC MOSFETs connected in series is shown in Figure 3.2.13. After verifying the prototype operation, the V_{ds} voltage of 3.2 kV is applied from a DC test source, and various waveforms are captured. It is important to mention that although the prototype being built to accommodate 5 SiC MOSFETs in series, the experimentation was performed with V_{ds} applied across 4 SiC MOSFETs, and waveforms captured are for only 4 MOSFETs since a 4-channel oscilloscope was used to perform the measurements. The switching frequency of the pulse transformer is set at approximately 167 kHz.

The high-voltage DC test setup block diagram for the developed module is shown in Figure 3.2.14. Figure 3.2.15(a) shows the control and monitoring station established outside the protective high-voltage Faraday's Cage. The setup includes a 4-channel oscilloscope, a laptop for user-defined frequency / duty cycle input, a DC lab supply for powering up the PCB board, a protective interlock system, and a high-voltage Heinzinger HV-DC 6 kV / 30 mA DC power supply. A high-voltage capacitor bank is charged from the high-voltage power supply, and then the voltage developed across the capacitor is switched to prevent the power supply from tripping due to a high current surge.

Figure 3.2.15 (b) shows the high-voltage test setup established inside the protective Faraday's Cage. High-voltage PCB is fed through the capacitor bank connected to the Heinzinger HV power supply. The high voltage differential probes are attached to the drain-source terminals of 4 series connected SiC MOSFETs. A current sensor is placed across the drain-source cable to measure the current flowing through the circuit. The variable frequency and duty cycle programming is configured through Arduino as shown. The switching frequency of the complete series connected SiC MOSFETs is set higher, and after every few cycles, the switching module is kept open for a short duration to allow the capacitors to recover the depleted voltage.

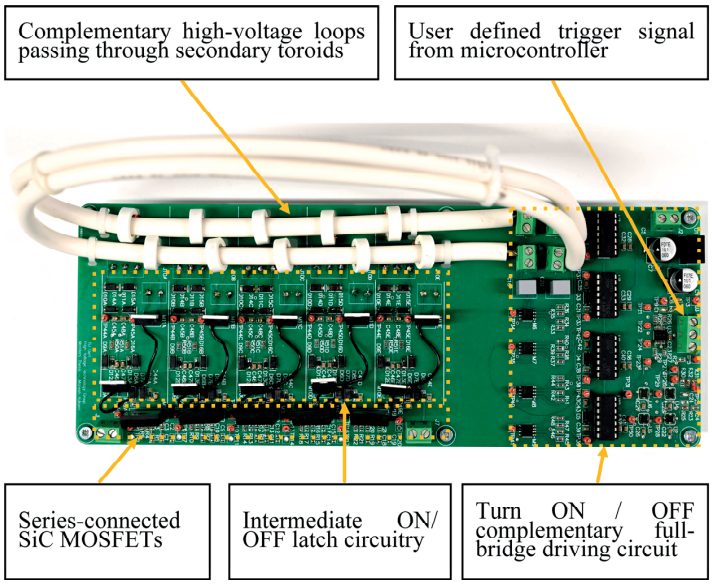


Figure 3.2.13. Prototype Board with HV turn on / off single turn loops passing through toroid cores coupled to the 5 series connected SiC MOSFETs through intermediate circuitry.

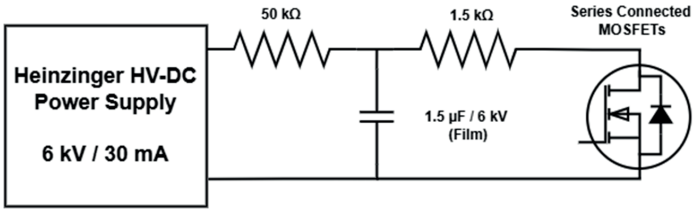


Figure 3.2.14. Block diagram of test setup for high voltage DC test on the developed series connected switches module.

One approach to verify voltage balancing between series connected switches is to capture the gate to source V_{gs} voltages across each switch. Active differential probes TA057 with an attenuation ratio of 20:1 are employed across the gate-source terminal of each series connected SiC MOSFET to measure gate voltage. Matching 15V peak V_{gs} signal waveforms with turn-on and turn-off instances across 4 series connected SiC MOSFETs can be observed in Figure 3.2.16. The charging profile of the input capacitance C_{iss} for each SiC MOSFET appears to be similar. The ripple observed in the waveform results from the pulse transformer switching at 167 kHz. The series-connected MOSFETs stack will turn completely on when it crosses the Miller Plateau Voltage of 4.5 V.

Subsequently, active high voltage differential probes TA044 were placed across drain-source terminals of each series connected SiC MOSFET to measure the V_{ds} voltage. Figure 3.2.17 illustrates the prototype PCB measurement diagram with V_{ds} waveforms measured across each series connected MOSFET using high-voltage differential probes. A nearly even distribution of a total of 3.2 kV switching at 50 kHz with 50% duty cycle across 4 switches can be observed in the Figure 3.2.17 (c). The same are tabulated below:

Table 3.2. V_{ds} Measurement across each series connected SiC MOSFET

S No.	Drain-Source Voltage	Value Observed	Percentage deviation
1.	V_{ds1} (Bottom most MOSFET)	800.1 V	~ 0%
2.	V_{ds2}	803.5 V	~ 0.4375%
3.	V_{ds3}	790.0 V	~ 1.25%
4.	V_{ds4}	794.5 V	~ 0.8125%

Figure 3.2.17 (d) shows the V_{ds} voltage rise time of 97 ns and fall time of 128 ns under specific conditions (oscillator speed 167 kHz, series connected MOSFETs switching speed 50 kHz, load resistance 1.5 kΩ). A current sensor N2780B by Keysight Technologies is employed to measure current across the entire series of connected switches. The datasheet of the sensor shows the voltage of 0.1V represents current of 1A [53]. The green waveform in Figure 3.2.17 (d) shows the current I_{ds} flowing across the series connected switches. A maximum current of 8 A (shown as 800 mV) can be observed under specific conditions. It is important to mention that the load for most of high-voltage testing applications is capacitive and resistive which requires a maximum current nearly 0.2 A [7]. Hence, for high-voltage testing applications, the switch's current handling capability is satisfactory. Since, the load in majority of tests are capacitive, the inductive load has not been included in this study.

Subsequently, similar measurements were carried out across each series connected MOSFETs stack for different frequencies and duty cycles to ascertain gate driver's performance. Figure 3.2.18(a), (b), (c) and (d) show the series connected SiC MOSFETs switching around 3.2 kV at 10, 25, 50 and 83.5 kHz frequency respectively. A nearly equal voltage distribution across all switches can be observed. The entire switch can switch at a maximum of half the switching frequency of the transformer. The maximum switching frequency can therefore be:

$$f_{switch\_max} = f_{transformer}/2 \quad (15)$$

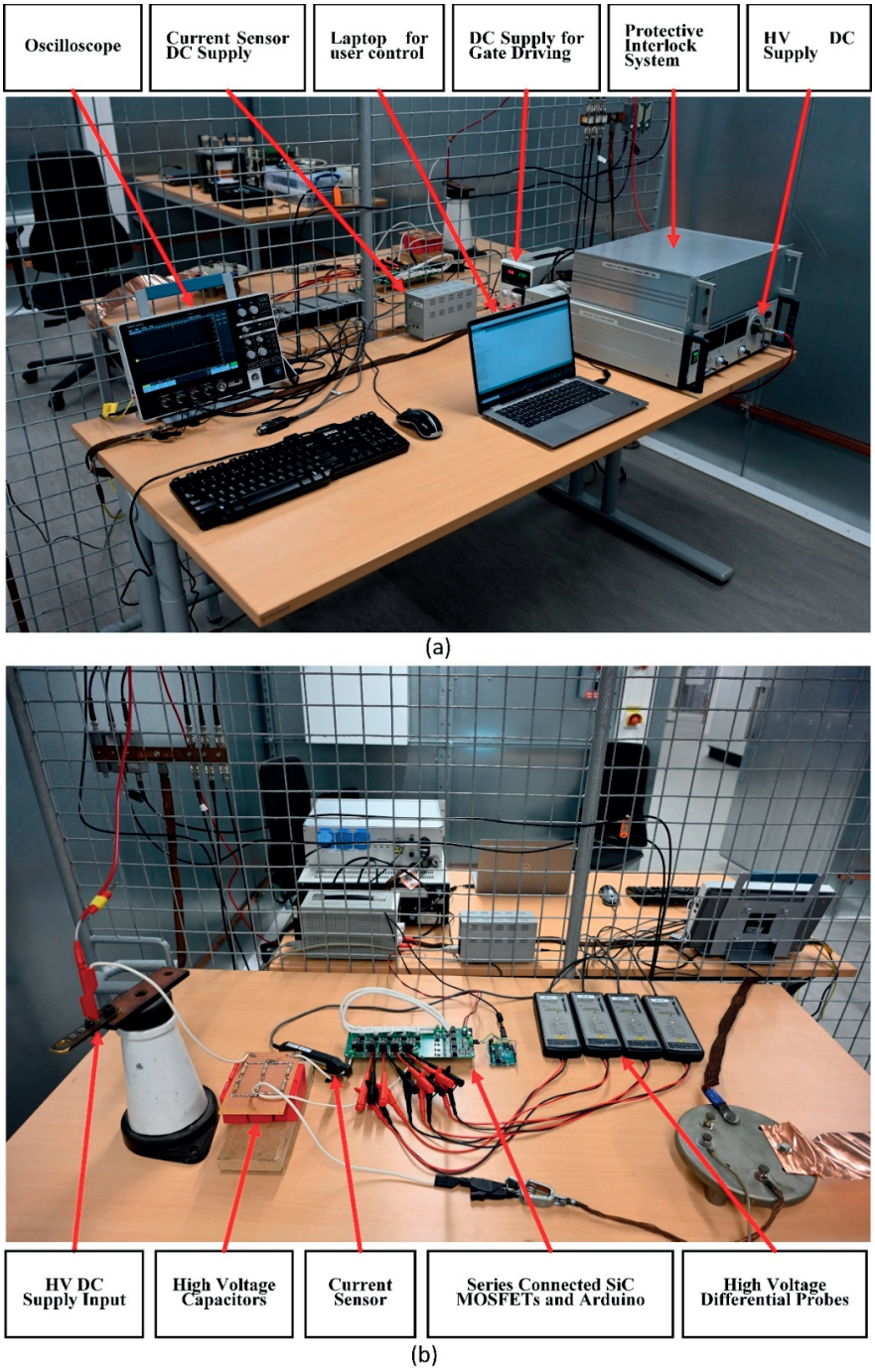


Figure 3.2.15. (a) Control and monitoring setup installed outside the Faraday's cage with 24V DC supply, Heinzinger HV DC Supply, Oscilloscope and a PC to input user-defined signal to Arduino. (b) High voltage test setup inside protective Faraday's cage with high voltage capacitors, current sensor, series connected MOSFETs prototype PCB, Arduino and 4 high voltage active differential probes attached to the source drain terminals of 4 series connected SiC MOSFETs.

Figure 3.2.16. Gate to source (Vgs) voltage across 4 SiC MOSFETs in series during turn-on and turn off.

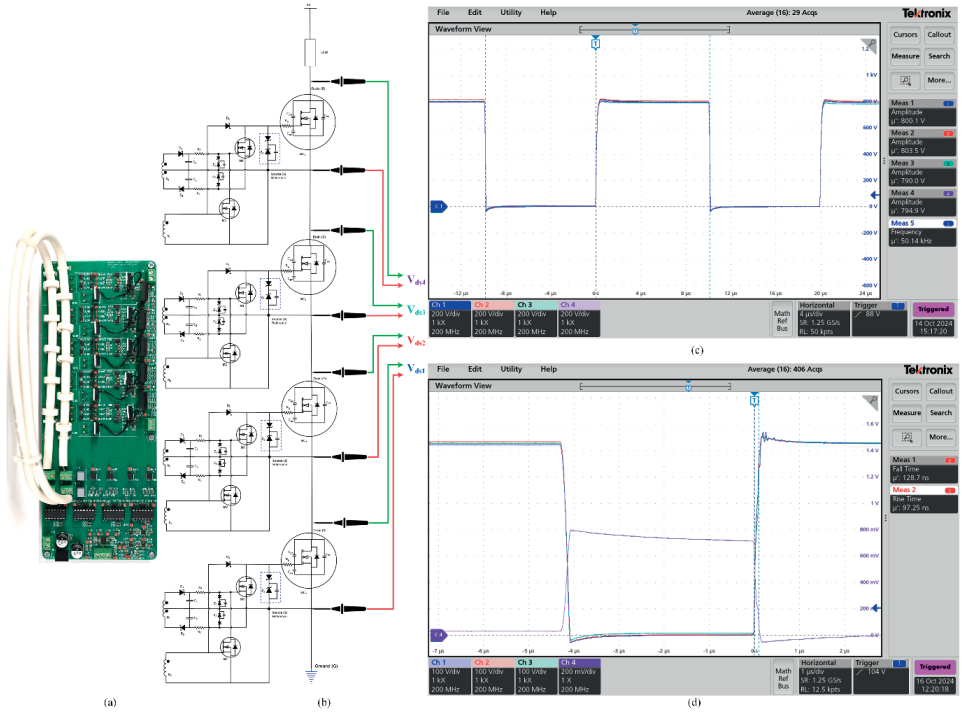


Figure 3.2.17. (a) Prototype PCB (b) High voltage side circuit V_{ds} measurement diagram (c) V_{ds} across each series connected SiC MOSFET with nearly even voltage distribution (d) Rise & fall time of voltage V_{ds} and current I_{ds} (middle waveform) through series connected SiC MOSFETs.

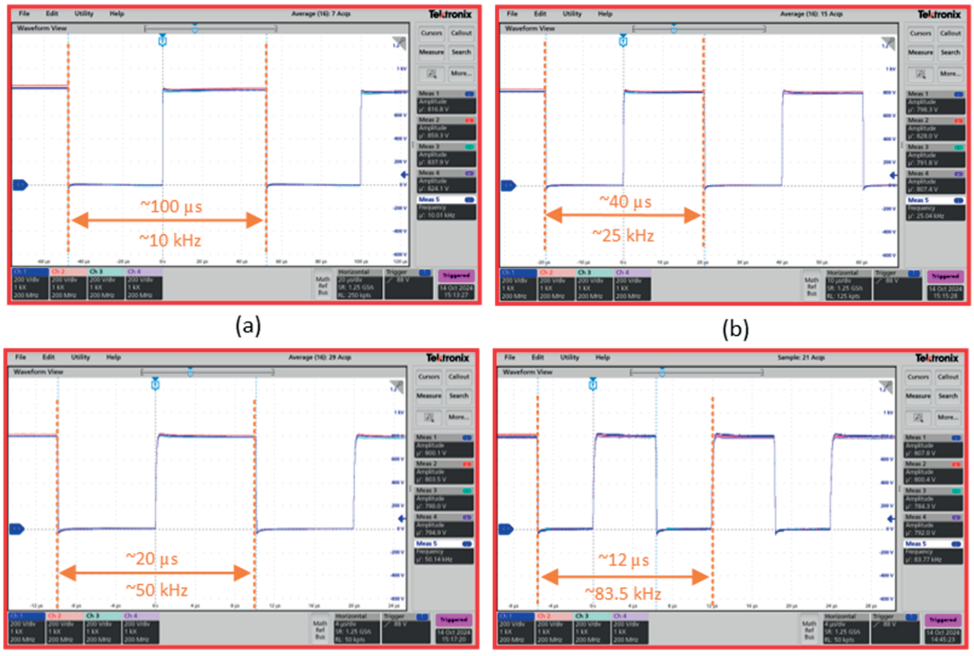


Figure 3.2.18. Vds voltage across 4 SiC MOSFETs in series switching at (a) 10 kHz (b) 25 kHz (c) 50 kHz (d) 83.5 kHz with 3.2 kV applied voltage.

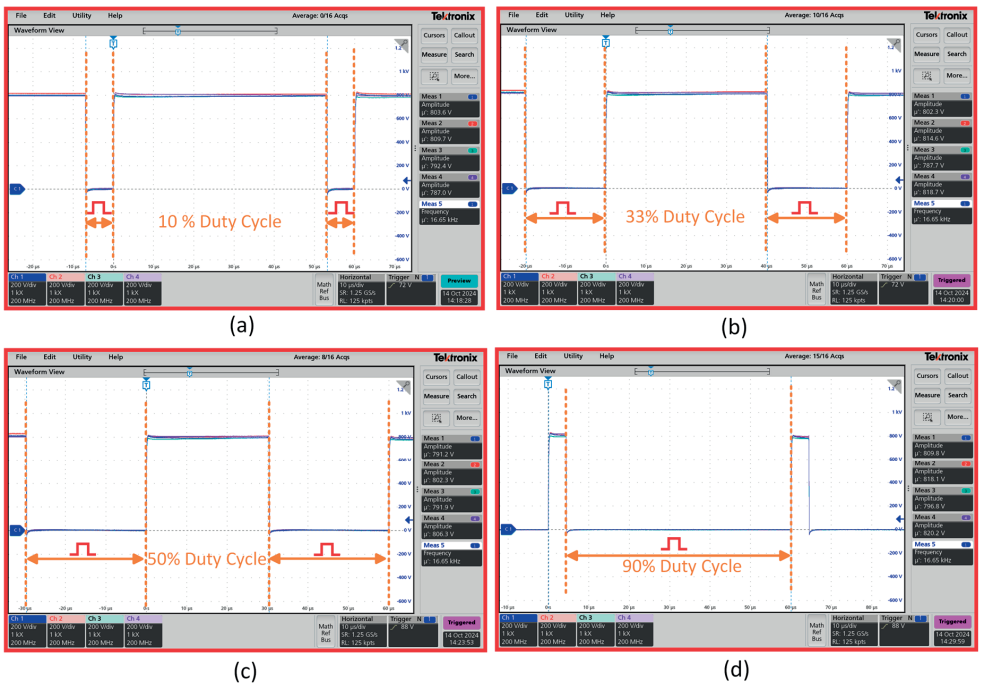


Figure 3.2.19. Vds voltage across 4 SiC MOSFETs in series switching at 16.7 kHz with (a) 10% duty cycle (b) 33% duty cycle (c) 50% duty cycle (d) 90% duty cycle.

3.3. Chapter Conclusion

Future power systems with high penetration of renewable energy sources and extensive use of power electronic interfaces will require testing under complex high-voltage waveforms. High-voltage switching modules are a key requirement for medium-voltage DC grid testing applications and can be realized by series connection of mature low-voltage semiconductor devices. The primary challenges associated with such series-connected configurations are the provision of reliable high-voltage–isolated gate driving and the achievement of uniform dynamic voltage sharing among individual switches. Conventional transformer-coupled gate driving approaches are excellent in achieving nearly even voltage distribution and high-voltage isolation but are inherently constrained to transformer pulse-frequency operation, which limits their applicability to generate arbitrary high-voltage waveforms with programmable frequency and duty cycle.

This chapter has identified and summarized the mechanisms leading to dynamic voltage imbalance in series-connected SiC MOSFETs and critically reviewed the limitations of previously reported gate driving techniques in enabling flexible switching control. To address these limitations, a programmable gate driving approach has been presented that decouples the turn-on and turn-off control of the series-connected MOSFETs from the constraints imposed by high-frequency transformer coupling. The proposed technique enables independent control of switching frequency and duty cycle while maintaining near-uniform voltage distribution within approximately 1% across the devices. Experimental validation with four series-connected SiC MOSFETs demonstrates stable operation at voltages up to 3.2 kV over a wide range of switching frequencies and duty cycles. The scalability of the proposed approach is primarily limited by the insulation capability of the primary-side single loop passing through the secondary toroidal windings. Provided that sufficient insulation is employed for example, insulation rated on the order of 100 kV, the architecture can be scaled to a correspondingly large number of series-connected switches.

Overall, the proposed gate driver architecture enables a simple and cost-effective high-voltage switching solution based on series-connected SiC MOSFETs. It represents a versatile building block for medium-voltage DC testing applications, particularly for the generation of complex voltage waveforms required to test future power electronics–dominated grid assets.

4

"Every measurement we make disturbs the system we are trying to measure."

— Max Planck

4. Measurement Probe Influence

The previous chapter explained the novel transformer coupled gate driving technique with programmable frequency and duty cycle for series connected SiC MOSFETs to generate high-voltage arbitrary waveforms. This chapter introduces the phenomenon of measurement probes parasitic impedance influence on voltage distribution across series connected MOSFETs. To the best of the author's knowledge, this phenomenon has not been reported in prior literature and constitutes a key and highly significant finding of this thesis for series-connected device topologies.

4.1. Measurement Probe Influence on Voltage Distribution Across Series-Connected MOSFETs

The evaluation of equal voltage distribution among series-connected SiC MOSFETs is performed by monitoring the drain-to-source voltage (V_{ds}) across each device. When a MOSFET switches off, its V_{ds} rises from zero to the applied voltage, and the intrinsic capacitances, C_{oss} and C_{iss}, discharge, forcing the device to transition from conduction to the voltage-blocking state. Figure 4.1.1 (a) shows the placement of isolated differential probes used to measure V_{ds} for each SiC MOSFET relative to its own source terminal. According to the differential probe user manual [54], the probe introduces approximately 4 MΩ of resistance to ground. As noted in [26], an off-state MOSFET exhibits drain-to-source resistance on the order of several hundred MΩ; therefore, the additional 4 MΩ path from the probe can create a low-resistance path to ground, potentially causing uneven voltage distribution during the static phase. Figure 4.1.1 (b) illustrates these probe resistances in red and the compensation resistors in blue, which are implemented to mitigate voltage imbalance [26]. To counteract the effect of this resistive loading, compensation resistors in the range of several hundred kΩ are connected to provide a preferred path for leakage currents to ground. The methodology for calculating these resistor values using KVL and KCL is detailed in

[26]. Typically, the compensation resistor values decrease from the bottom MOSFET to the top, with the exact values depending on the total number of series-connected devices [26].

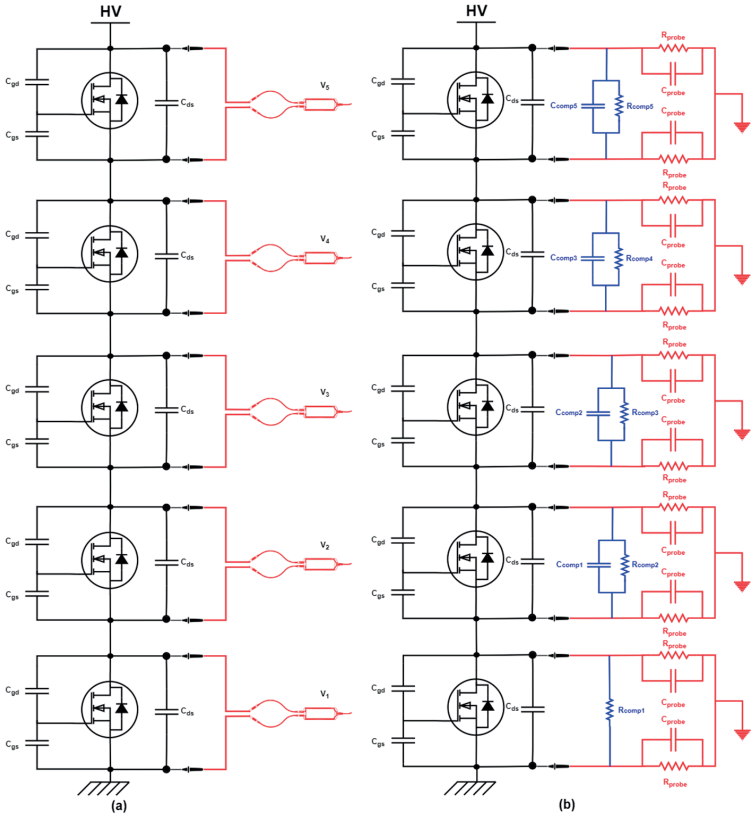


Figure 4.1.1. (a) Circuit Diagram for 4 SiC MOSFETs in series with differential probe placement, (b) Circuit Diagram for 4 SiC MOSFETs in series with probe introduced impedances and RC compensation.

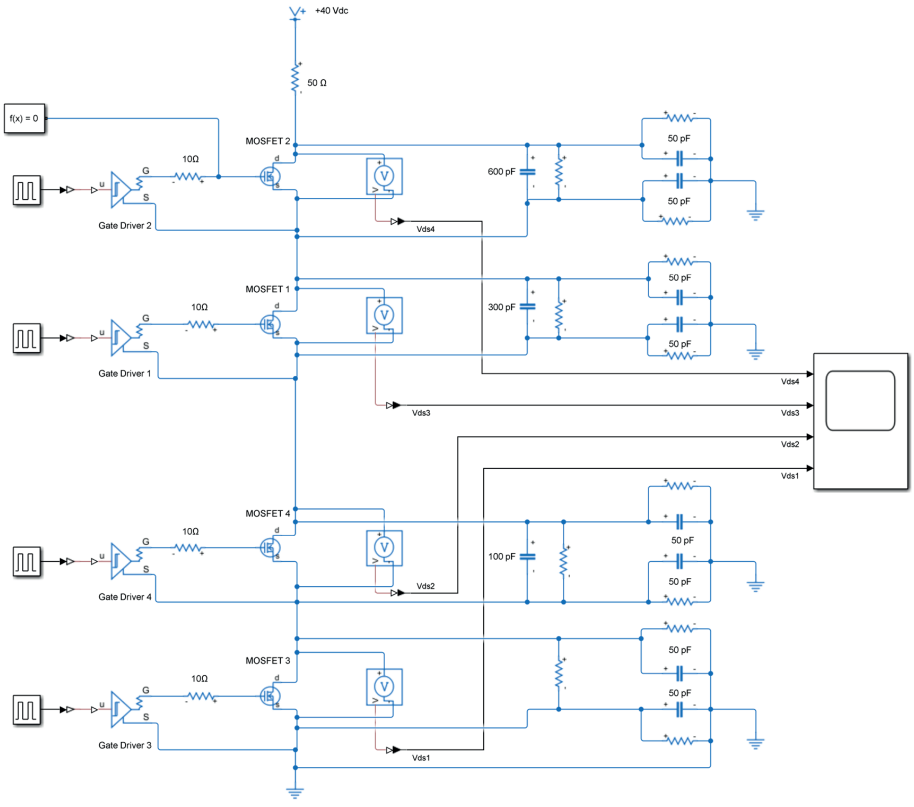
Similarly, the differential probe user manual indicates that these probes introduce a parallel capacitance of approximately 5.5 pF alongside the 4 MΩ resistor, as highlighted in red in Figure 4.1.1 (b) [50]. This additional capacitive element causes a V_{ds} imbalance during the dynamic switching phase, with the effect increasing from the bottom to the top MOSFET, as illustrated in Figure 4.1.3 (a), where a 40 V voltage is applied across four series-connected SiC MOSFETs. The intrinsic capacitances, C_{iss} and C_{oss}, of each MOSFET must discharge to ground through the gate terminal; however, the probe capacitance alters the charging and discharging behavior of these intrinsic capacitances. Consequently, the probe-induced capacitance has a significant impact on voltage distribution among the series-connected devices. To correct for voltage imbalance during dynamic turn-off events, this additional capacitance must be compensated. Similar to resistive compensation, the values for capacitive compensation are determined using KVL and KCL, but in contrast to resistors, the compensation capacitance increases from the bottom MOSFET to the top. The capacitive compensation network, shown in blue in Figure 4.1.1(b), is calculated using the following equation:

$$C_{compi} = \frac{n\,(n+1)}{2} \times C_p \qquad (16)$$

Where C_{compi} is the i^{th} compensation capacitor starting from the bottom with n = 1, and C_p = C_{probe} / 2.

Figure 4.1.3 (b) illustrates the V_{ds} waveforms after capacitive and resistive compensation, showing a nearly balanced voltage distribution. However, the inclusion of these additional compensation capacitors in parallel slightly slows the turn-off transition by a few nanoseconds. Therefore, the compensation capacitance must be carefully optimized to maintain an acceptable dV_{ds}/dt slope. It is important to note that these compensating resistors and capacitors are only required when differential probes are connected for V_{ds} measurements. During normal operation, when no probes are attached to the series-connected MOSFETs, such compensation is not necessary.

A MATLAB Simulation shown in Figure 4.1.2 (a) is performed to verify the impact of additional capacitance introduced across drain-source terminals of series connected MOSFETs by differential probes. Figure 4.1.2 (b) shows the imbalance created by probe capacitances and Figure 4.1.2 (c) shows the voltage balance achieved across series connected MOSFETs after introducing capacitor compensation as per equation 15. The resistive influence and its compensation calculation is detailed in study [26].



(a)

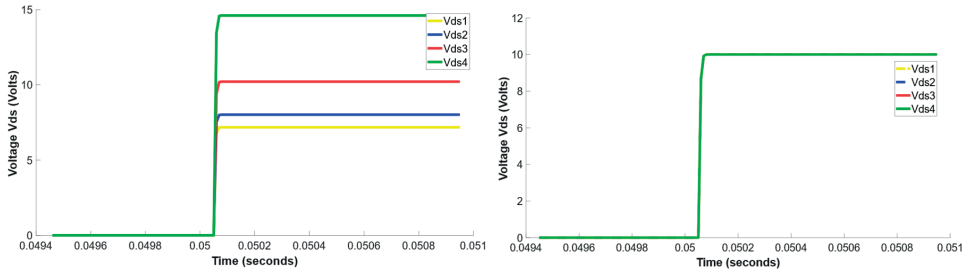


Figure 4.1.2. (a) MATLAB Simulation driving 4 series connected MOSFETs with probe impedances attached on drain-source terminals. (b) Drain to source (Vds) voltage across 4 SiC MOSFETs in series during turn-off with no probe compensation. (c) Drain to source (Vds) voltage across 4 SiC MOSFETs in series during turn-off with probe compensation as per equation 12.

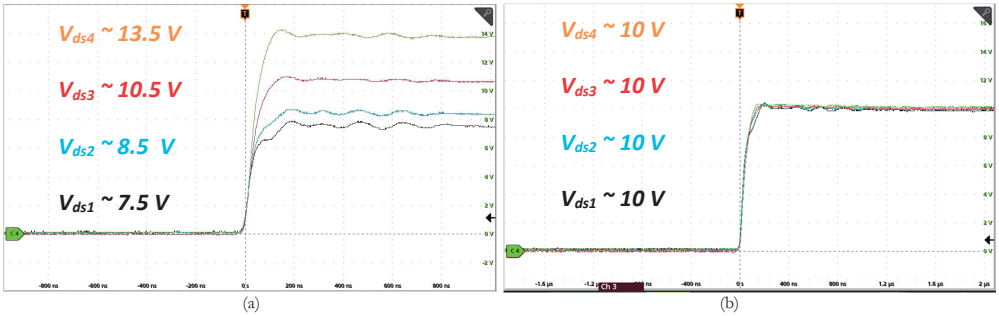


Figure 4.1.3. (a) Drain to source (Vds) voltage across 4 SiC MOSFETs in series during turn-off with no probe compensation. (b) Drain to source (Vds) voltage across 4 SiC MOSFETs in series during turn-off with probe compensation.

4.2. Chapter Conclusions

This chapter highlights the significant influence of measurement probes on the voltage distribution across series-connected MOSFETs. It has been shown that the presence of differential probes during V_{ds} measurements introduces additional resistive and capacitive paths, which can lead to noticeable voltage imbalance across the individual switches. To obtain accurate measurements, compensation resistors and capacitors must be carefully implemented across each MOSFET, ensuring that the measured voltage distribution reflects the true behavior of the devices under test. Importantly, these passive compensation components are only required during measurement and are removed during normal operation when no probes are present. This phenomenon underscores a critical consideration often overlooked in previous studies: snubber component values reported without accounting for probe-induced effects may not provide proper voltage balance once the probes are removed. Therefore, the impact of measurement probes must be carefully considered, particularly when selecting snubber capacitors, as inappropriate values could result in dynamic voltage imbalances during normal operation. Overall, understanding and mitigating probe-induced disturbances is essential for both accurate characterization and reliable operation of series-connected MOSFETs.

5

"New technologies come from ideas that seem unnecessary at the time."

— Freeman Dyson

5. Series Connection of GaN HEMTs

The previous chapters presented a novel transformer-coupled gate-driving technique with programmable frequency and duty cycle, and analyzed the influence of measurement probes on voltage distribution across series-connected SiC MOSFETs. Building on this foundation, the present chapter introduces a modified dual transformer-coupled architecture in which an ultra-fast GaN full-bridge drives the transformer primary, enabling effective and nearly balanced voltage sharing among series-connected GaN devices and extending their operation into the kilovolt regime. This development is motivated by the fact that modern power-electronics-dominated grids are already subjected to nanosecond-scale electrical stress. Standardized immunity tests, including Electrical Fast Transient / Burst EFT/B (IEC 61000-4-4) and Electrostatic Discharge ESD (IEC 61000-4-2), specify nanosecond-scale voltage rise times, underscoring the increasing need for ultra-fast high-voltage switch.

5.1 High-Frequency Switch Design using GaN HEMTs

Solid-state switches such as IGBTs and MOSFETs are extensively employed in high-voltage pulse generators because they offer advantages over conventional spark-gap switches, including longer operational lifetime, lower losses, compact size, higher repetition rates, and improved controllability [55]. Nevertheless, their relatively slow voltage rise times limit their ability to produce ultrafast high-voltage nanosecond pulses. In contrast, wide-bandgap (WBG) devices are gaining attention in power electronics due to their superior electrical and thermal properties, lower conduction and switching losses, and enhanced overall efficiency [55]. Among these, GaN High Electron Mobility Transistors (HEMTs) are particularly promising. Their lateral device architecture provides significantly lower gate charge, approximately six times smaller than SiC

devices and nearly fifty times smaller than conventional silicon devices [56] [57] [58] enabling the generation of high-voltage arbitrary waveforms with ultrafast rise times.

GaN HEMTs present a practical alternative to Si and SiC MOSFETs in applications requiring high power density, allowing MHz-range switching, reduced device footprint, higher power density, and improved efficiency through lower switching energy and minimized reverse recovery losses. These advantages are particularly important for test generators, which must deliver fast, high-voltage waveforms continuously and reliably without excessive losses or bulky cooling requirements. While GaN HEMTs share the same terminal nomenclature as conventional MOSFETs Gate, Source, and Drain they differ in several fundamental aspects. Notably, GaN transistors lack an inherent body diode, necessitating reverse conduction through the channel, which must be actively managed by the gate driver. Additionally, the gate characteristics of GaN devices differ significantly from those of Si and SiC MOSFETs. GaN HEMTs typically exhibit low threshold voltages in the range of approximately 1–2 V and maximum recommended gate voltages of about 6–7 V, whereas SiC MOSFETs generally have threshold voltages around 2–4 V and are commonly driven at 15–18 V. This narrower gate-voltage margin in GaN devices necessitates highly precise gate control to avoid gate overstress and ensure reliable operation. Furthermore, their extremely low input capacitance and high dv/dt capability demand gate drivers with minimal propagation delay to ensure reliable high-speed operation, making gate driving design more critical than for conventional Si or SiC devices [59] [60].

Structurally, Si and SiC MOSFETs use a vertical architecture, with current flowing through the bulk, whereas GaN FETs typically employ a lateral structure, with conduction occurring in a two-dimensional electron gas (2DEG) channel formed at the AlGaN/GaN interface [59] [60] [61]. Figure 5.1.1 shows a typical lateral GaN HEMT, consisting of a silicon substrate, GaN buffer layer, AlGaN barrier, and the three terminals (source, gate, drain), along with a passivation dielectric and a source-connected field plate. The passivation layer reduces surface electron traps between gate and drain, while the field plate enhances breakdown voltage and suppresses trapping effects. The AlGaN/GaN heterojunction creates a high-density, high-mobility 2DEG channel, which conducts current differently from the depletion-region conduction in Si MOSFETs [59] [60] [61]. However, due to their lateral design, commercially available GaN HEMTs are typically limited to voltage ratings of around 650 V [62] [63]. Attempts to increase the voltage rating of GaN HEMTs beyond 650 V have been investigated, but these strategies typically involve trade-offs that can reduce the inherent advantages of GaN technology. For example, incorporating field plates or other structural modifications to enhance breakdown voltage often adds parasitic capacitance and increases switching losses, thereby compromising the fast-switching performance that makes GaN attractive [64].

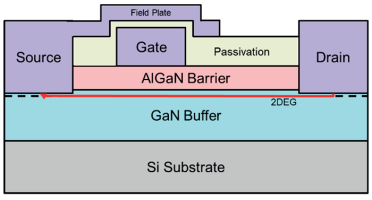


Figure 5.1.1. Basic Lateral Structure of a GaN FET [60].

While higher-voltage GaN devices may be achievable in the future, they may not fully retain the key benefits of GaN, such as rapid switching and low on-resistance. Consequently, the lateral device structure that provides GaN HEMTs with their superior performance inherently limits their voltage-blocking capability, restricting their ability to generate ultrafast nanosecond-scale arbitrary high-voltage pulses in the kilovolt range.

5.2 Series-Connected GaN Devices: Opportunities And Voltage Balancing Challenges

This trade-off between ultrafast switching and higher voltage capability motivates alternative approaches, such as series-connecting multiple GaN devices, to fully exploit their potential for high-voltage, nanosecond-scale pulse generation. Using mature, commercially available low-voltage GaN devices in series offers a cost-effective and practical solution [13]. However, series-connection topologies present their own challenges, most notably ensuring equal voltage distribution across all devices. Unequal voltage sharing can lead to inefficient operation or even failure of overloaded devices, making careful design and compensation strategies essential for reliable performance.

As discussed in Chapter 3, unequal voltage distribution among series-connected devices arises from several factors, including small variations in intrinsic parasitic elements within the devices, differing external capacitive couplings, and discrepancies in the applied gate signals [14]. Among these, mismatched gate signals are identified as the most critical factor, with studies showing that even a minor delay of 4 ns can result in up to 40% voltage imbalance across the switches [20]. Further investigation is needed for GaN devices, where voltage imbalance tends to be more pronounced due to their extremely low intrinsic capacitances (C_{iss}, C_{rss}, and C_{oss}) and exceptionally fast turn-on and turn-off characteristics [59]. In the case of GaN HEMTs, the impact of mismatched gate signals is particularly severe because of these small parasitic capacitances, lower gate voltage levels, and ultrafast switching speeds exceeding 50 V/ns. Even a gate signal mismatch on the order of a few nanoseconds can produce substantial voltage imbalance across series-connected devices.

5.3 Limitations Of Conventional Gate Driving Methods For Series-Connected GaN Switches

Recent progress in dynamic voltage balancing for GaN devices has been reported in [65] [66] [67] and [68] primarily based on closed-loop active gate current control techniques. These methods show promise in enhancing dynamic performance; however, they remain iterative and cannot ensure instantaneous voltage balance across series-connected devices. As a result, if the temporal or current resolution is insufficient, control failures may occur, leading to uneven stress distribution and potential failure of one or more devices. Additionally, these studies have not thoroughly addressed the issue of voltage overshoot, which is particularly critical in high-speed GaN switching due to the devices' low intrinsic capacitances and extremely fast transient response. Therefore, while these approaches mark important progress, several challenges must still be resolved before they can serve as a robust reliable solutions for high-voltage switches based on series-connected GaN devices.

In contrast, open loop gate current synchronization technique as described in previous chapters offers a balanced trade-off combining high isolation, simple control, and excellent scalability making them a very prominent candidate for driving GaN devices connected in series.

In comparison to closed-loop feedback oriented techniques, open-loop gate current synchronization techniques provide a well-balanced solution, combining high isolation, low losses, straightforward control, and excellent scalability, making them a highly attractive approach for driving series-connected GaN devices. In this chapter a scalable gate-driver architecture is examined based on transformer-coupled magnetic isolation, which was initially proposed in [29]. In this approach, gate current synchronization across series-connected SiC MOSFETs is achieved using a current transformer. Comparable high-voltage gate-driver designs for series-connected MOSFETs have been reported in [19], [69], [70], [71] and [72] where pulse transformers were employed to drive multiple SiC MOSFETs simultaneously, and capacitive snubbers were incorporated to provide additional passive voltage balancing.

As detailed in Chapter 3, the transformer-coupled gate-driving approach is highly scalable, allowing many GaN devices to be connected in series with minimal changes to the gate-driver structure. Scalability is primarily enabled by the isolation provided by the transformers, which separates the floating sources of high-side devices from the low-voltage primary circuit, eliminating complex level-shifting circuits. The main limitation arises from insulation requirements: for example, stacking 11 GaN devices rated at 650 V each results in nearly 6.5 kV at the top device source, necessitating robust insulation and appropriately sized transformer cores. Advanced dielectric materials, such as polyimide, PTFE, and XLPE, provide high breakdown strength in thin layers, supporting compact high-voltage isolation.

While transformer-based drivers offer synchronized gate signals, high isolation, and scalability, they inherently operate at a fixed frequency, limiting user-defined control of switching frequency and duty cycle [19]. This can restrict applications requiring precise pulse width, rise time, amplitude, and shape, such as plasma generation and high-voltage dielectric testing [56], [7]. To overcome this limitation, the dual-transformer scheme introduced in [73] and detailed in Chapter 3 is employed, allowing programmable control of switching frequency and duty cycle while maintaining safe, reliable transitions across series-connected GaN HEMTs.

5.4 Optimization Of Transformer-Coupled Gate Driver For High-Speed Operation

Transformer-coupled gate drivers, although highly scalable and effective for isolation, are inherently limited in switching speed [74]. Both prior studies and the work presented in this thesis have shown that the achievable rise time is primarily determined by several factors, including the switching frequency of the primary-side H-bridge, the self-inductance of the primary and secondary windings, the transformer's coupling coefficient, the value of the primary-side compensation capacitor, and the secondary-side load capacitance [75] [76]. To achieve a rapid voltage rise across the secondary windings that drive the gates, both the primary side switching stage and the transformer design must be optimized to handle fast transients. On the secondary side, the effective capacitance is dominated by the intrinsic gate capacitance of the GaN HEMTs, which is extremely

small and fixed [77] [78]. Consequently, optimization efforts focus on adjustable parameters, the primary switching frequency, transformer design, and compensation network to achieve the fast-rise secondary voltage necessary for high-speed GaN gate driving.

Previous approaches for MHz-level gate driving often relied on complex E-class oscillators [70], which are challenging to implement. In contrast, this work employs a simple GaN-based full-bridge (H-bridge) circuit on the primary side as the excitation stage, generating ultrafast, nearly square voltage pulses. The configuration shown in Figure 5.7.1, drives the primary winding efficiently, enabling rapid gate voltage transitions across series-connected GaN devices without the complexity of resonant circuits. To transfer the fast voltage rise effectively to the secondary side, key design parameters are carefully considered. The primary-side compensation capacitor is selected to shape the pulse and limit overshoot, while the transformer core, winding self-inductances, and coupling coefficient are optimized to preserve the sharp rise time and minimize distortion. These measures ensure that the secondary gate voltage transitions rapidly, delivering synchronized fast gate signals required for balanced voltage distribution among the series-connected devices.

The high-frequency design also maintains the necessary charge on the gate capacitance (Ciss) while allowing the transformer to be smaller, resulting in a more compact and efficient switching solution. Overall, transformer-coupled gate drivers with GaN-based ultrafast excitation enable high-voltage switching applications while retaining the speed, efficiency, and compactness characteristic of low-voltage GaN devices.

Transformer-coupled gate drivers using GaN-based ultrafast excitation transformers hold significant promise for realizing high-voltage switching applications, combining the efficiency, rapid switching, and compact form factor of commercially available low-voltage GaN devices. This approach opens new opportunities for next-generation power electronics, enabling ultrafast, high-voltage systems that were previously unattainable with conventional devices.

5.5 Measurement Probes Impact On Voltage Distribution And Measurement Accuracy

The authors in studies [79] and [26] have shown that measurement probes can substantially distort voltage sharing in series-connected MOSFETs, making it essential to account for and compensate probe effects during experiments. In GaN devices, with their extremely low gate capacitance and ultrafast dv/dt and di/dt, probe impedance and parasitic capacitance can significantly alter both static and dynamic V_{ds} distribution, and may even induce high-frequency resonances at the gate terminals, distorting gate voltage signals and the resulting output voltage, as illustrated in Figure 5.5.1 and Figure 5.5.2. These effects are particularly critical when characterizing nanosecond-scale switching edges, where probes with excessive capacitance, long ground leads, or limited bandwidth can slow edges, introduce ringing, or mask true device performance. Accurate measurement therefore requires high-bandwidth, low-capacitance differential probes, minimized ground connections, matched impedance, and properly rated oscilloscopes [80]. Proper probe compensation ensures reproducible experimental results and prevents misinterpretation of device behaviour, guaranteeing that observed limitations reflect the device and gate-drive performance rather than characteristics of the measurement setup.

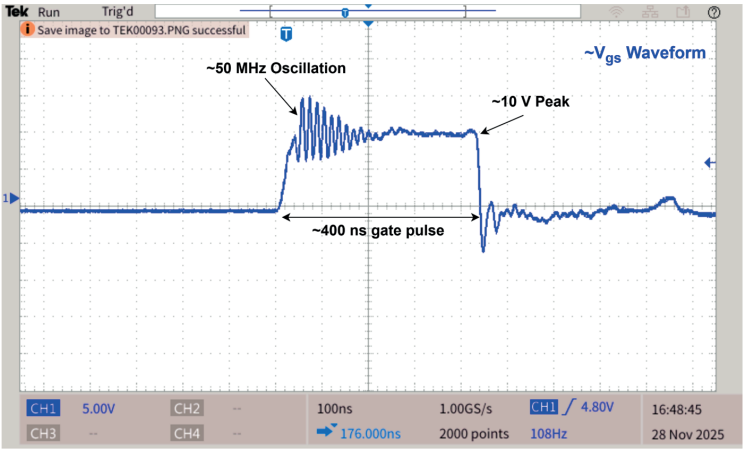


Figure 5.5.1. Gate voltage distortion due to probe parasitic influence.

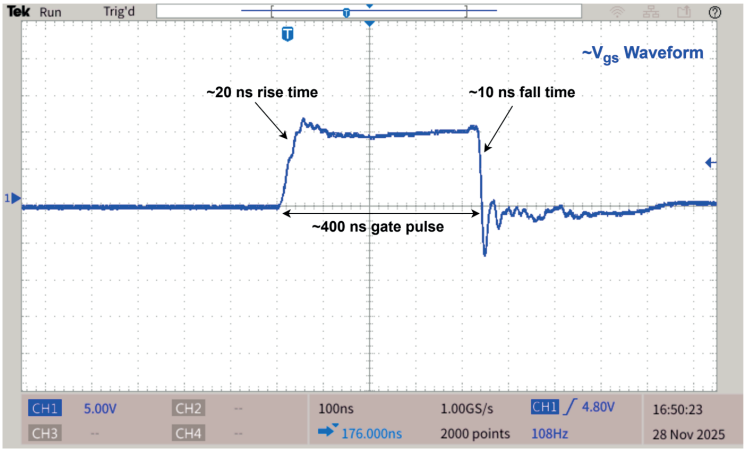


Figure 5.5.2. Gate voltage after probe parasitic compensation.

5.6 Transformer-Coupled Gate Driving for Series-Connected GaN Devices

Unlike conventional Si or SiC devices, GaN HEMTs feature a lateral structure that enables ultrafast switching and high efficiency but inherently limits voltage-blocking capability. To overcome this constraint while preserving GaN's high-speed advantages, a scalable, magnetically isolated gate-driving scheme designed to synchronize gate currents across series-connected GaN devices is developed. A simple open-loop transformer-coupled gate driver architecture employed previously for SiC MOSFETs is modified for GaN HEMTs and presented, achieving nearly equal voltage distribution across a series connection of low-voltage GaN HEMTs for high-voltage, fast pulse generation. More importantly, instead of relying on complex high-frequency oscillators like E-Class oscillators, the proposed approach uses a GaN-based full-bridge excitation circuit with an optimized L_3C_2 resonant compensation network, providing minimal propagation delay and precise gate charge control. Practical design guidelines are established to ensure operation within the linear impedance plateau, allowing the gate capacitance of series-connected GaN HEMTs to be fully

charged within the first pulse. The work also addresses the challenge of switch overshoot, which is prominent at ultrahigh switching speeds, by minimizing loop inductance using non-inductive, thick-film resistors [81].

Experimental validation confirms nearly uniform voltage sharing among two series-connected GaN devices up to 1 kV, demonstrating the effectiveness of the open-loop transformer-coupled gate driver. The results highlight a practical pathway for extending GaN's high-speed, high-efficiency performance into the kilovolt regime, enabling simple, compact, and cost-effective solid-state switches for future pulsed power systems, dielectric testing, and advanced power electronic applications. The subsequent paragraphs provide a detailed description of the gate-driver design and its implementation.

5.7 GaN-Based Transformer-Coupled High-Frequency Excitation Technique For Gate Current Synchronization In Series-Connected GaN Devices

5.7.1 Circuit Description

To address the limitations of existing voltage balancing techniques across series connected GaN HEMTs, the programmable open loop gate current synchronizing driver presented in Chapter 3 is modified to achieve matching gate signals and high-voltage isolation. The updated architecture, shown in Figure 5.7.1, retains the fundamental transformer-coupled concept of Chapter 3 but incorporates several key enhancements to support ultrafast GaN switching and improved gate protection. On the primary side, an ultrafast GaN-based full-bridge excitation circuit is employed to drive the transformer, replacing conventional excitation methods. This full bridge generates ±24 V bipolar pulses with sub-nanosecond transition capability, ensuring sharp excitation of the transformer windings. Two single-turn, high-voltage–insulated primary loops are used for turn-on and turn-off operations and are driven in a complementary manner to guarantee reliable switching. A highly permeable transformer core is selected to maximize the coupling coefficient, which is critical for achieving fast rise times and minimal distortion on the secondary-side gate signals. On the secondary side, the gate-driving circuitry is adapted to support nanosecond-scale voltage clamping by replacing Zener diodes with transient voltage suppressor (TVS) diodes. This modification provides faster and more robust gate-voltage protection suitable for high-speed GaN operation. Each GaN device in the series stack is driven by two dedicated secondary windings one for turn-on and one for turn-off along with corresponding gate charging and discharging paths, preserving precise timing symmetry across devices. The GaN full-bridge excitation circuit is powered by a 12 V DC supply for control circuitry, while a 24 V DC bus provides the primary excitation voltage for the transformer. These modifications collectively extend the Chapter 3 concept toward high-speed, high-voltage operation while maintaining the core objective of synchronized gate driving for effective voltage balancing across series-connected GaN devices.

5.7.2 Circuit Operation And Timing Sequence

The circuit operation starts with the user signal of turn on/off which is turned into streams of mutually exclusive digital gate pulses for turn on and turn off signal by the microcontroller. These streams of digital pulses then subsequently drive the high frequency GaN H-Bridge to generate 24V

nearly square high frequency bipolar pulses on the primary side of the transformer. This produces around ±24 V bipolar pulses across either the turn-on or turn-off single-turn loops, with only one coil active at a time. On the secondary side, a gate charging and discharging circuit is built with small-signal MOSFETs controlling the switching frequency and duty cycle of the series-connected GaN HEMTs, independent of the transformer's operating frequency. The detailed schematic is shown in Figure 5.7.2 and its corresponding timing diagram is shown in Figure 5.7.3.

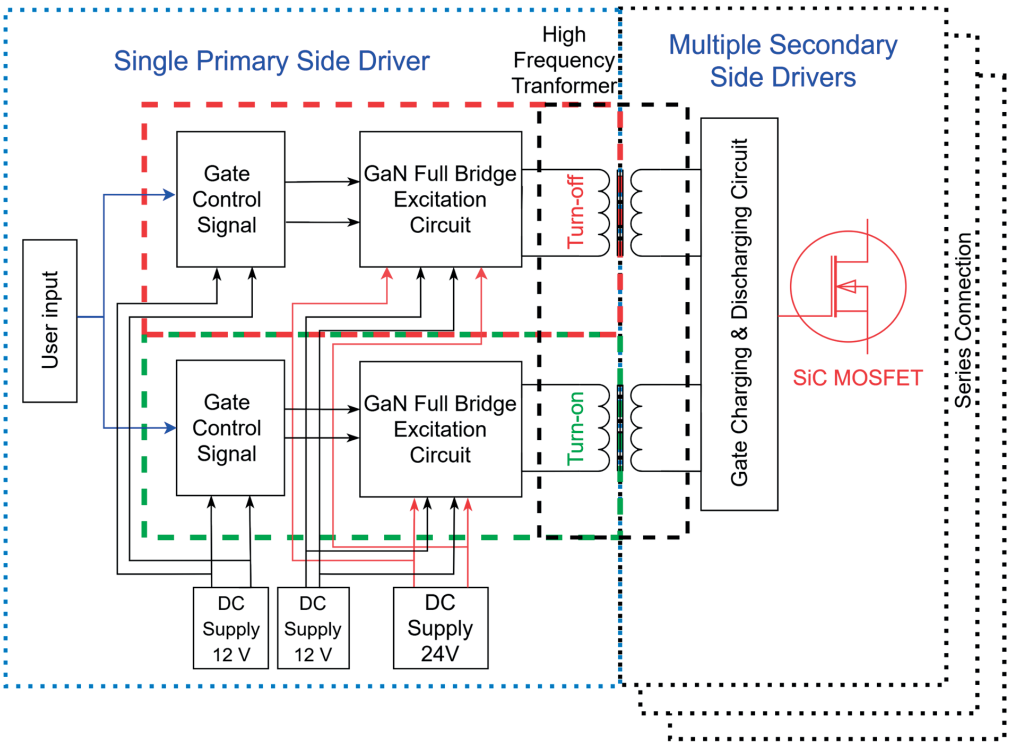


Figure 5.7.1. Block diagram for the proposed scheme.

During turn-on, the first rising voltage pulse charges the GaN's gate capacitance C_{iss} through Schottky diode D_3 to turn it on. The gate voltage is clamped by a TVS diode for switch protection, which has fast response of nanosecond scale compared to Zener. At the same time, the same pulse charges the small signal MOSFET M_2 which discharges the gate of MOSFET M_1 to turn it off. The turn off coil remains inactive during the turn on operation.

For turn-off cycle, the turn off transformer is excited with fast bipolar pulses from GaN H Bridge, which in turn generates a fast voltage pulse on the secondary side turning the small signal MOSFET M_2 on, immediately discharging the GaN gate capacitance C_{iss}, turning it effectively off. The turn on coil remains stalled during the turn off operation cycle.

In this way the secondary windings ensure rapid charge and discharge of relevant switch gates ensuring triggering of the series-connected GaN devices as per user defined digital input and preventing any false turn on/off.

5.7.3 Gate Charging & Discharging Mechanism For Series-Connected GaN Devices

Figure 5.7.4 illustrates the turn-on operation of the switch, emphasizing the components responsible for activating the series-connected GaN HEMTs. The blue measurement probes correspond to the timing sequence presented in Figure 5.7.3. During the positive half cycle, the signal passes through diode D_3 and is clamped by TVS Z_3 at +10 V, thereby charging the input capacitance C_{iss} of the GaN Switch (GaN_1) to the gate voltage V_{gs3}, as shown in Figure 5.7.4 (a). When the input voltage falls below V_{gs3}, the diode D_3 becomes reverse-biased, halting current flow through the gate–source path as depicted in Figure 5.7.4 (b). The diode remains reverse-biased throughout the negative half cycle and resumes conduction once the input voltage exceeds V_{gs3} again. Throughout this interval, GaN switch remains in the on state.

Simultaneously, the positive pulse from the transformer activates the small-signal MOSFET M_2, which discharges the gate of M_1 to maintain it in the off state. Once the gate capacitance of GaN switch is fully charged, the device is completely turned on, and the capacitance behaves as an open circuit. However, a small leakage current continues to flow through the gate–source junction, which is replenished by subsequent positive pulses, resulting in minimal current circulation during operation.

Figure 5.7.5 presents the components active during the turn-off phase of the series-connected GaN HEMTs. In this mode, the positive half cycle of the secondary is clamped by TVS Z_1 at +10 V, charging the gate capacitance C_{iss} of the small-signal MOSFET M_1 to gate voltage V_{gs1}, as illustrated in Figure 5.7.3. The drain–source path of M_1 then discharges the gate charge of the GaN Switch (GaN_1), ensuring its rapid turn-off.

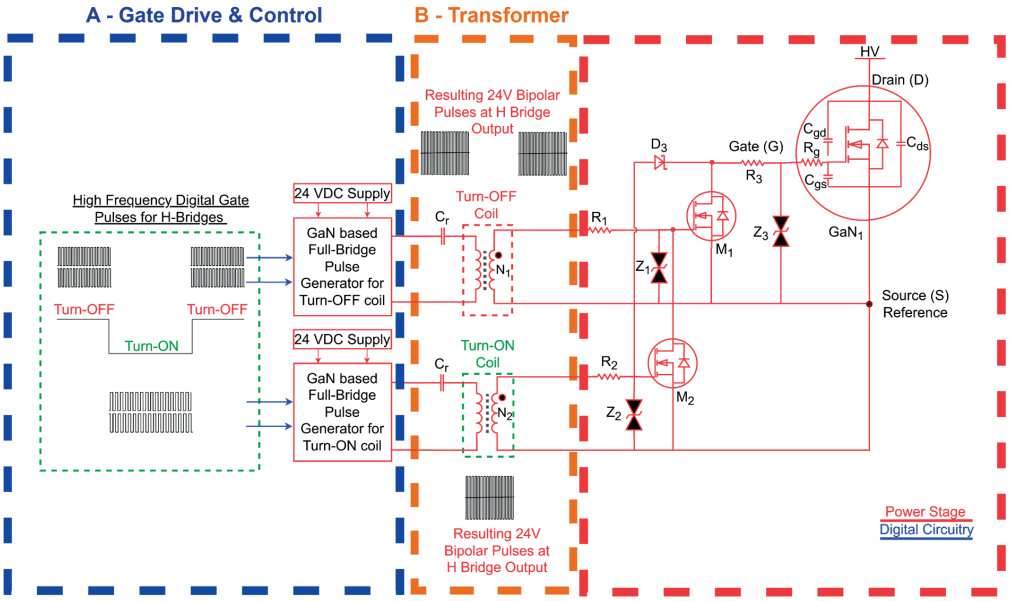


Figure 5.7.2. GaN based high frequency excitation gate current synchronization driving circuit with programmable frequency and duty cycle.

This process occurs synchronously across all series-connected GaN Switches, ensuring uniform gate voltages and simultaneous switching, which results in an even voltage distribution among all devices.

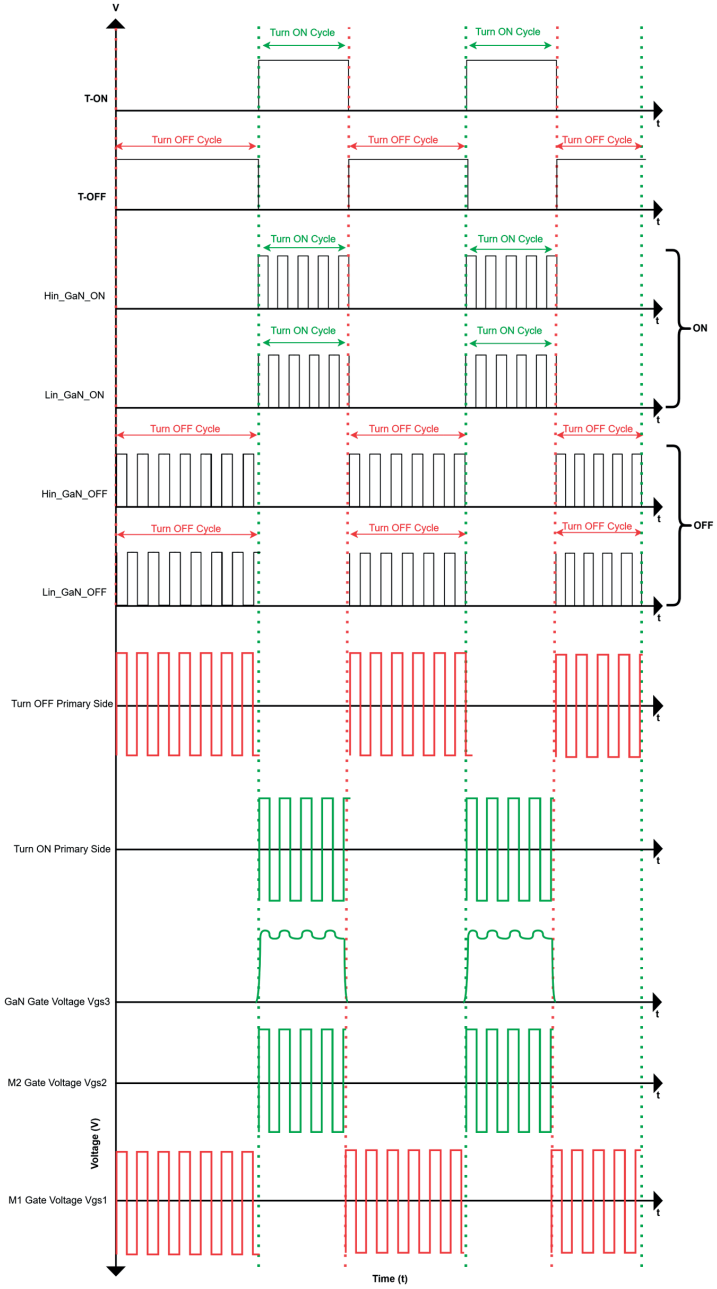


Figure 5.7.3. Detailed timing diagram for circuit presented in Figure 5.8.2 where user defined on and off trigger signals are modulated into high frequency complementary digital signals to drive the coil between the full bridge circuits.

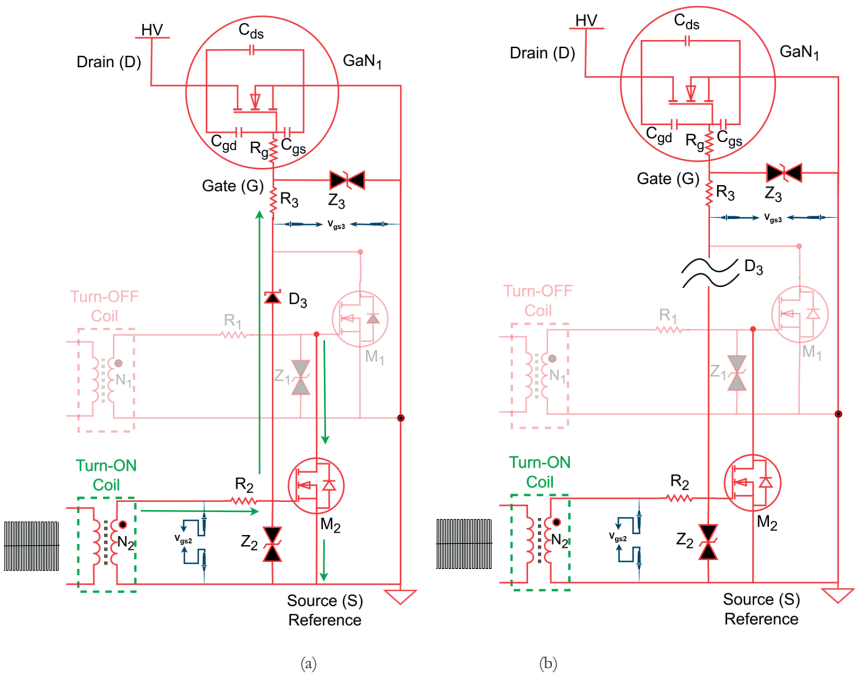


Figure 5.7.4. Turn-on operation of series-connected GaN HEMTs showing M2's synchronization with GaN1 and control of M1, with D3 charging Ciss to turn GaN1 ON (see timing diagram in Figure 5.7.3). (a) Circuit during positive half voltage pulse. (b) Circuit during negative half voltage cycle.

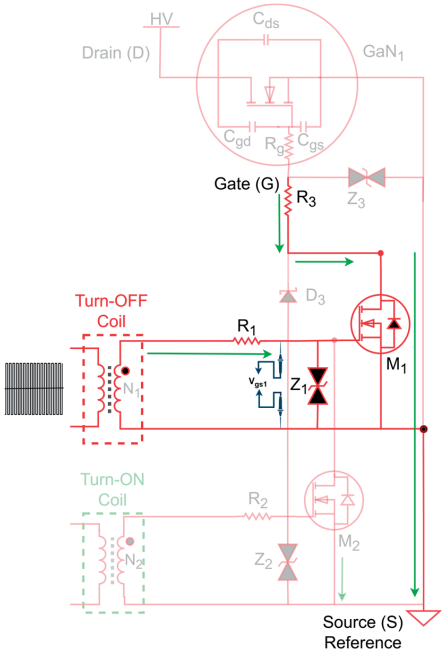
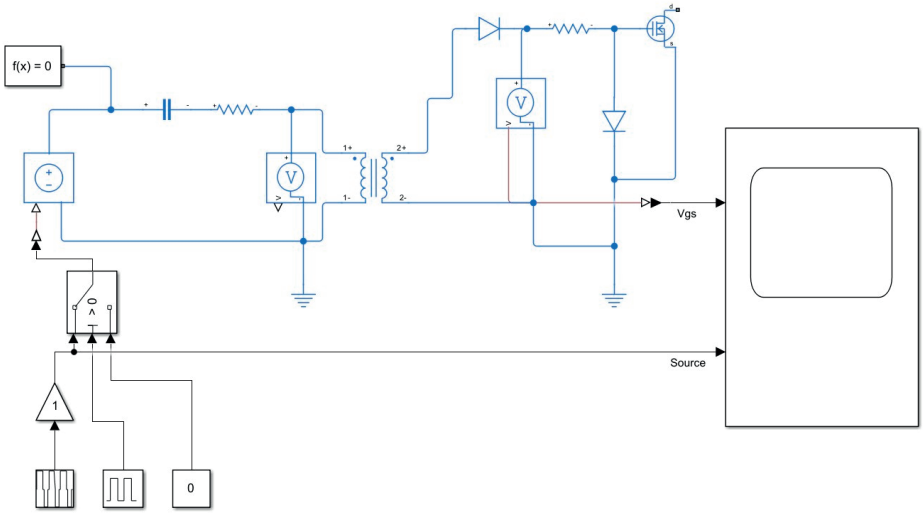


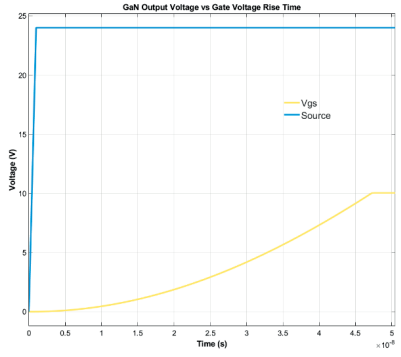
Figure 5.7.5. Active components in the secondary driver circuit during turn-OFF phase, illustrating operation as per timing diagram shown in Figure 5.7.3.

5.7.4 GaN Half Bridge Rise Time Simulation

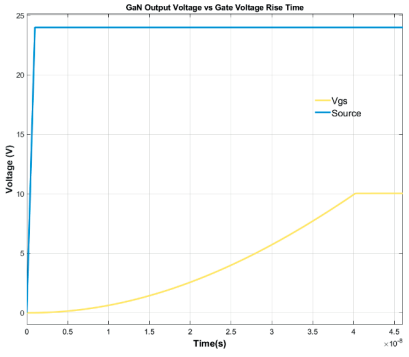
A MATLAB Simulation was designed to establish the GaN Half bridge output voltage waveform translation into secondary side transformer output voltage rise time as shown in Figure 5.7.6 (a). With primary side inductance of 12 uH, secondary side inductance of 26 uH the measured rise time strongly depended on the transformer coupling coefficient. As shown in Figure 5.7.6 a rise time of approximately 47 ns was observed at a coupling coefficient of 0.8 (b), which slightly improved to about 45 ns at 0.85 (c). A more noticeable reduction to roughly 33 ns was achieved at 0.9 (d), while the best performance of approximately 20 ns was obtained at a coupling coefficient of 0.96 (e). The simulation shows that in order to achieve fast rise time, the coupling coefficient plays the most crucial role. The higher the coupling the faster is the transformer secondary side gate voltage rise time. The results can be verified in Figure 5.8.2 of the actual gate voltage where rise time around 20 ns can be observed.



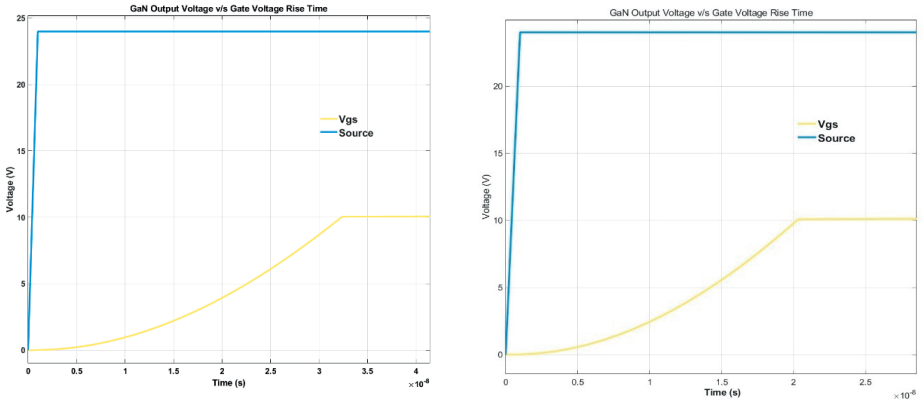
(a)



(b)



(c)



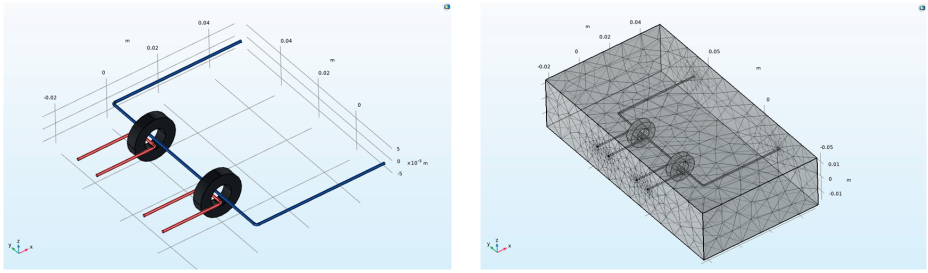
(d) (e)

Figure 5.7.6. (a) MATLAB Simulink model to establish rise time of the voltage across transformer secondary. (b) ~47 ns rise time with 0.8 coupling coefficient. (c) ~45 ns rise time with 0.85 coupling coefficient. (d) ~33 ns rise time with 0.9 coupling coefficient. (e) ~20 ns rise time with 0.96 coupling coefficient.

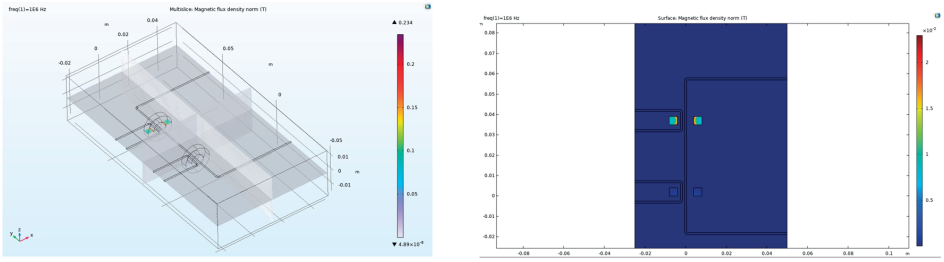
5.7.5 Transformer Core Cross Coupling Analysis

To verify the magnetic behavior and coupling assumptions of the proposed transformer structure, a finite-element method (FEM) simulation was conducted in COMSOL as shown in Figure 5.7.7. The simulated model comprises a single-turn primary conductor passing through two toroidal magnetic cores, each incorporating a single-turn secondary winding driven at a switching frequency of 1 MHz. The cores have dimensions of 8 × 4 × 4 mm and are characterized by an inductance factor AL of 5500 nH. The resulting magnetic flux density distribution indicates that, due to the high permeability of the core material, the magnetic flux is strongly confined within each toroidal core and follows the flux path established by the primary excitation.

Flux leakage into the surrounding space is negligible, and no appreciable magnetic interaction is observed between adjacent cores. These results confirm that cross-coupling between secondary windings is effectively suppressed in the proposed configuration. Consequently, the mutual coupling among secondary windings can be considered negligible, and the corresponding mutual inductances may be safely assumed to be zero in the circuit-level resonance analysis.



(a) (b)



(c) (d)

Figure 5.7.7. Magnetic flux density (T) distribution at 1 MHz obtained from COMSOL FEM simulation, illustrating flux confinement within the high-permeability toroidal cores and negligible magnetic interaction between adjacent secondary cores. (a) COMSOL Simulation. (b) Meshed Simulation. (c) Isometric Plot showing magnetic flux density B (T). (d) Cut Plot showing magnetic flux density B (T).

5.8 Experimental Results

The prototype board with 2 GaN HEMTs GAN111-650WSB in TO-247 package by NEXPERIA connected in series and driven by SGT120R65AL e-mode GaN HEMT by STM Electronics based full bridge inverter circuits is shown in Figure 5.8.1. After verifying the prototype operation, the Vds voltage of 1.0 kV is applied from a DC test source. Vds and Ids waveforms are captured using 70 MHz High Voltage Differential Probes TA044 by Pico Technology, Current Probe N2780B by Keysight Technologies on a 250 MHz Tektronix TBS2000B Oscilloscope. The technical items utilized are summarized in the Table 5.1.

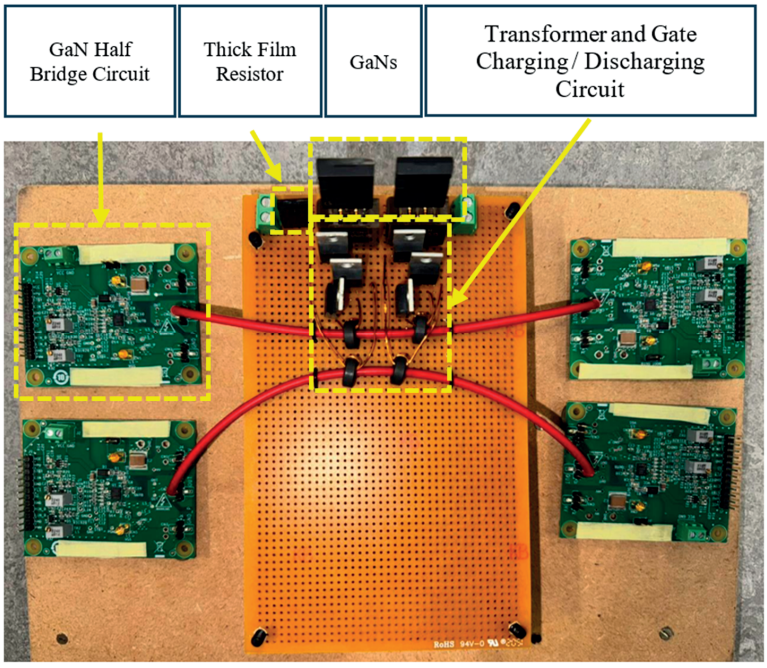


Figure 5.8.1. Prototype board showing HV turn-on/off single-turn loops through toroidal cores, coupled to two series-connected GaN HEMTs via intermediate circuitry.

Table 5.1. Various components used in the experimental setup.

S No.	Part Number	Description
1.	GAN111-650WSB	Through Hole GaN Switch, 650 V
2.	SGT120R65AL	GaN Switch, 650 V
3.	STDRIVEG610	GaN Half Bridge Gate Driver
4.	IRFZ14	Small Signal MOSFET
5.	AP851 390/100/25R F 50PPM	Ohmite Thick Film Non Inductive Resistor
6.	B64290P0751X038	High Permeability Toroidal Core
7.	N2780B	Current Probe by Keysight
8.	TBS2000B	250 MHz Tektronix Oscilloscope
9.	CT4072	100 MHz, High Voltage Differential Probe by CAL Test Electronics
10.	Heinzinger PNC 6000 - 30	6 kV / 30 mA HV-DC power source
11.	MKP1W041007K00KSSD	1 µF 3000V Film Capacitor

5.8.1 Mitigation Of Parasitic Inductance Induced Voltage Overshoot In Fast GaN Switching

When a power switch turns off very rapidly, the abrupt interruption of current interacting with circuit parasitics especially the stray inductance, produces a voltage overshoot according to $v = L\,\mathrm{d}i/\mathrm{d}t$. As the turn-off speed increases, the rate of change of current becomes extremely high, causing correspondingly large overshoot and ringing on the switching node. This problem becomes significantly more severe with GaN HEMTs, which exhibit much faster switching transitions and higher di/dt compared to Si and SiC MOSFETs. Their ultrafast turn-off capability amplifies the effect of even small parasitic inductances, leading to substantial overshoot which can potentially overstress the device and lead to its failure.

To reliably evaluate the series-connected GaN devices, the test setup was carefully engineered to minimize parasitic inductances. Straight copper bars were used for the high-voltage DC bus connections to reduce loop inductance and maintain a low-impedance current path. It is worth while to mention that conventional wire-wound or spiral-track resistors inherently exhibit parasitic inductance, which can introduce significant voltage overshoot when subjected to the extremely high di/dt produced by GaN devices. Therefore, non-wirewound thick-film resistors [81] specifically designed with nearly zero inductance were selected as the resistive load. These Ohmite thick-film elements help suppress overshoot and ringing by minimizing the inductive component of the load, enabling accurate characterization of the GaN device's switching behavior.

5.8.2 Voltage Balancing At High Voltage

The block diagram of the developed high-voltage DC test setup is presented in Figure 5.8.1.

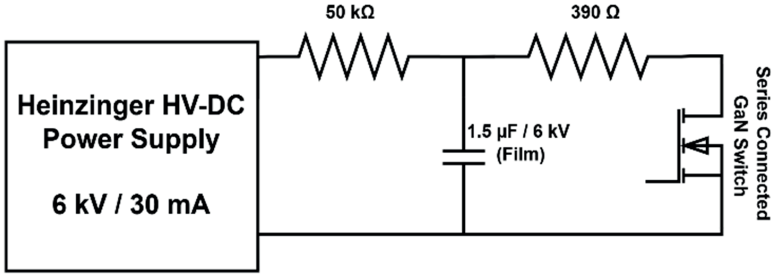


Figure 5.8.1. Block diagram of the test setup for high-voltage DC testing of the developed series-connected switch module.

The control and monitoring station, placed outside the protective high-voltage Faraday cage, consists of a high frequency 4-channel oscilloscope (Model TBS2000B), a laptop for defining switching time, DC laboratory power supplies for energizing the PCBs, a protective interlock system, and a Heinzinger 6 kV / 30 mA HV-DC power source. Since the power supply is unable to deliver high current at high voltage, a capacitor bank is charged using the high-voltage supply, after which the stored energy is switched across the load to avoid tripping the supply due to high inrush current surges. The GaN-based high voltage switch module is energized through a capacitor bank charged by a Heinzinger HV-DC power supply. High frequency high voltage differential probes (Model CT4072 by Cal Test Electronics) were connected across the drain of each individual switch and its source terminal, while the current probe is placed in the drain path to monitor circuit current. The switching gate signals were programmed via an Arduino interface.

To confirm proper gate drive synchronization and voltage sharing, the gate-to-source voltages Vgs of all devices were captured. High frequency probes (CT4072, 200:1 attenuation) were placed across the gate source terminals of each GaN HEMT. Identical Vgs waveforms with matched turn-on and turn-off instants can be observed across both devices, reaching ~10 V peak as shown in Figure 5.8.2 (a). The similarity in charging profiles of the input capacitance C_{iss} confirms uniform gate excitation. The GaN HEMT stack is fully turned on once the threshold voltage is exceeded.

Subsequently, high frequency probes (model CT4072) were connected across the drain-source terminals of each GaN HEMT to measure V_{ds}. Figure 5.8.2 (c)-(d) present the double-pulse test results obtained with three non-inductive resistive loads of 150 Ω, 250 Ω, and 400 Ω, corresponding to peak drain currents of 6.4 A, 4.00 A, and 2.512 A, respectively. With an approximately 1 kV DC-link voltage, the two GaN devices exhibit nearly even static and dynamic voltage sharing during both turn-on and turn-off transients, confirming effective voltage balancing under all load conditions. The oscilloscope captured transition characteristics further show a clear dependence of rise time on load resistance. For the 400 Ω load, a rise time of approximately 67 ns and a fall time of approximately 26 ns were measured. With the load resistance reduced to 250 Ω, the rise and fall times decreased to approximately 44 ns and 19 ns, respectively. For the 150 Ω load, a much faster rise time of approximately 14 ns and a fall time of approximately 13 ns were observed, corresponding to the higher current level. These results demonstrate that faster voltage transitions are achievable at the expense of increased current stress. Despite the variation in load and current, the transformer-coupled gate driver consistently maintains nearly balanced Vds sharing across the series-connected GaN devices, validating the robustness and effectiveness of the proposed gate-driving approach.

It is important to note that the measured rise and fall times are subject to the bandwidth limitations of the measurement setup. A 100 MHz differential voltage probe (CT4072) was used in conjunction with a 250 MHz oscilloscope. Based on standard bandwidth considerations ($t_r \approx 0.35/\mathrm{BW}$), the corresponding rise-time limits of the probe and oscilloscope are approximately 3.5 ns and 1.4 ns, respectively. The combined system rise-time limitation, estimated using a root-sum-square approach, is therefore approximately 3.8 – 4 ns. Since the experimentally observed rise and fall times are significantly larger than this limit, the reported measurements capture the switching dynamics within the constraints of the probing arrangement. This clarification is

provided to ensure transparency and reproducibility of the experimental results under high-dv/dt operating conditions.

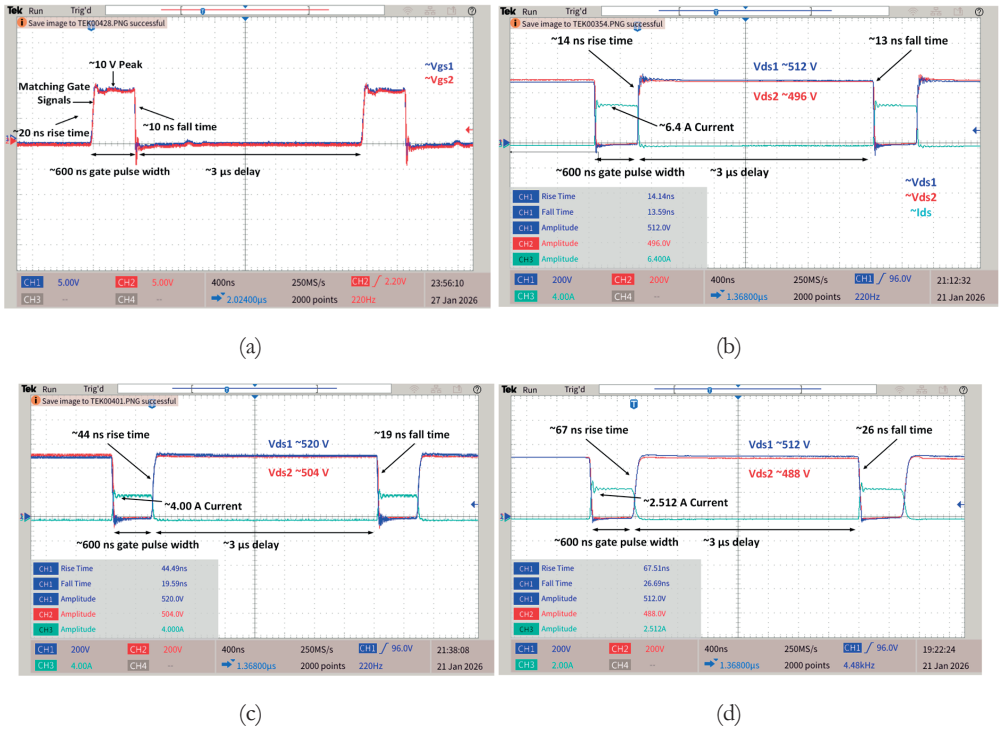


Figure 5.8.2. (a) Gate to source (V_{gs}) voltage across 2 GaN HEMTs in series during turn-on and turn off. (b) V_{ds} voltage across 2 GaN HEMTs in series switching at 1 kV with 150 Ω Load. (c) V_{ds} voltage across 2 GaN HEMTs in series switching at 1 kV with 250 Ω Load. (d) V_{ds} voltage across 2 GaN HEMTs in series switching at 1 kV with 400 Ω Load.

5.9 Chapter Conclusion

GaN devices, owing to their lateral device structure contrary to conventional vertical structure, exhibit excellent characteristics such as low gate charge, fast switching, and high dv/dt capability, making them superior to conventional IGBTs and SiC MOSFETs for ultrafast operation. However, the same lateral structure inherently limits their voltage blocking capability to about 650 V, restricting their direct use in kilovolt-level applications. Series-connecting GaN devices therefore emerges as the most viable solution to harness the advantages of GaN technology at higher voltages.

Efforts have been made quite recently to achieve voltage balance across series connected GaN devices using closed loop techniques. This work however demonstrates a scalable open-loop transformer-coupled gate driver that achieves nearly equal voltage sharing across series-connected GaN HEMTs. Using a simple GaN-based full-bridge driver, an optimized L_3C_2 resonant network, and a straightforward gate-charging/discharging circuit, the method delivers minimal signal mismatch and precise gate-current synchronization across series connected devices.

Detailed analysis of the transformer design parameters, supported by an L_3C_2 equivalent-circuit framework and comprehensive MATLAB/Simulink/FEM simulations with one primary

and multiple secondary windings, identifies the resonance conditions and operational bandwidth plateau needed to ensure complete gate-capacitance charging within the first excitation pulse, an essential requirement for dynamic voltage balancing. The study also emphasizes the significant influence of measurement probe parasitics on gate and output voltage waveforms, demonstrating that proper probe compensation and high-bandwidth instrumentation are critical for accurate characterization of MHz-range switching transitions.

Additionally, the work addresses the challenge of voltage overshoot commonly encountered with ultrafast GaN switching, showing effective mitigation through loop-inductance minimization with the use of non-inductive thick-film resistors.

Experimental results confirm nearly balanced voltage sharing up to 1 kV using two series-connected GaN HEMTs under different load and current conditions, validating the effectiveness of the proposed open-loop transformer-coupled gate-driving approach. These results demonstrate that transformer-coupled gate driving is an effective means of extending GaN performance benefits into the kilovolt regime. Importantly, the proposed technique is inherently scalable, with the maximum number of series-connected devices primarily limited by the insulation capability of the primary excitation conductor passing through the toroidal cores coupled to high-voltage secondary windings. As a result, additional switches can be stacked in series as permitted by the achievable insulation strength across the secondary-side circuitry. This approach enables the realization of compact, cost-effective, high-frequency, high-voltage solid-state switches and supports scalable, programmable systems capable of generating complex ultrafast arbitrary waveforms for advanced high-voltage testing of grid assets.

Although the advancements in wide-bandgap semiconductor technology have the potential to offer high voltage switches up to 30 kV in the near future to implement medium-voltage converters without series-connection and multi-level topologies [20]. However, the knowledge base of the series-connected switches will certainly open up new possibilities with the new generation of semiconductor switches beyond 30 kV in high-voltage applications [20].

6

"The present is theirs; the future, for which I really worked, is mine."
— Nicolas Tesla

6. Conclusions and Future Work Recommendations

Future hybrid AC/DC power grids will experience fast switching, non-sinusoidal waveforms, and steep voltage transients that exceed the capabilities of conventional high-voltage testing, creating a need for compact and flexible high-voltage arbitrary waveform generation to realistically emulate in-service stresses. Modular multilevel converter (MMC) architectures offer a promising route toward scalable high-voltage systems, yet their practical deployment is often hindered by excessive system complexity, large component counts, and reduced reliability when many low-voltage submodules are stacked. Increasing the voltage capability of an individual MMC cell therefore emerges as a crucial step toward reducing system complexity, footprint, and cost. Within this context, this PhD thesis has addressed a key technological challenge: enabling high-voltage, high-speed switching using commercially available low-voltage semiconductor devices, with the ultimate objective of simplifying and advancing power-electronics-based high-voltage arbitrary waveform generators.

This thesis addressed the challenge of realizing compact, flexible, and high-voltage switching solutions capable of generating arbitrary waveforms representative of stresses in future power-electronics-dominated AC/DC grids. Using series connection of commercially available mature low-voltage wide-bandgap devices like SiC MOSFETs and GaN HEMTs the work demonstrated a scalable path to kilovolt-level switching while preserving their benefits like reliability, low $R_{ds\text{-}on}$ and better thermal performance. Two principal contributions underpin these results. First, a dual transformer-coupled gate-driving architecture was developed that overcomes the intrinsic frequency and duty-cycle limitations of conventional transformer-based gate drivers, enabling fully programmable switching control while maintaining nearly even static and dynamic voltage sharing across series-connected devices. Second, the thesis identified and demonstrated that voltage

measurement probes are not passive observers but active elements that can substantially distort both static and dynamic voltage distributions in series-connected switches leading to potentially misleading conclusions if not properly compensated.

By combining a series-connected wide-bandgap switch architecture with transformer-coupled, programmable gate driving and probe-compensated measurement methodology, this thesis establishes a reliable and scalable high-voltage switching building block for the development of power-electronics-based arbitrary waveform generators for advanced high-voltage testing of future hybrid grids.

6.1 Conclusions

The thesis first established a comprehensive theoretical foundation for series-connected MOSFET operation by analyzing the mechanisms responsible for voltage imbalance under both steady-state and transient conditions. It shows that dynamic voltage imbalance, is dominated by gate-signal timing mismatch, while device parameter spread and parasitic inductances and capacitances have a comparatively secondary influence. A systematic comparison of voltage-balancing techniques confirmed that transformer-coupled gate-current synchronization provides the most effective means of achieving closely matched gate signals, offering an optimal combination of scalability, high-voltage isolation, and implementation simplicity. This finding directly prompted the design of the advanced gate-driving architectures developed in this thesis.

Building on this foundation, the thesis introduces and experimentally validated a programmable gate-driving approach for series-connected SiC MOSFETs that overcomes the intrinsic frequency and duty-cycle limitations of conventional transformer-based drivers. By decoupling gate control flexibility from transformer pulse constraints, the proposed architecture enables arbitrary switching patterns while maintaining near-uniform voltage sharing across devices. Experimental results demonstrated stable operation up to 3.2 kV with four SiC devices connected in series, over a switching frequency range of 10 to 83.5 kHz and a duty-cycle range of 10% to 90%, confirming the suitability of this approach for arbitrary waveform generation.

Recognizing that accurate experimental validation is crucial for high-speed, high-voltage research, this thesis also addresses a critical yet often overlooked issue: the impact of measurement probes on voltage sharing in series-connected devices. The study demonstrated that probe-induced parasitic impedances can significantly distort both static and dynamic voltage distributions, potentially leading to erroneous conclusions about circuit performance. By systematically analyzing and compensating for these effects, this work provides essential guidance for reliable measurement practices. These findings underscore the necessity of proper probe compensation for accurate device characterization, an aspect that has been insufficiently addressed in prior literature highlighting the importance of distinguishing true device behaviour from probe-induced artifacts.

The final technical contribution extended the series-connection concept to GaN HEMTs, whose exceptional switching speed and low gate charge make them highly attractive for ultrafast applications but whose lateral structure limits their voltage rating. The transformer-coupled gate-

driving scheme was modified and optimized to synchronize gate currents across series-connected GaN devices. Through careful transformer design, resonant compensation, and excitation-stage optimization, the proposed approach successfully transferred the ultrafast switching capability of GaN devices to the kilovolt range. Experimental validation confirmed balanced voltage sharing up to 1 kV as a proof of concept, while also demonstrating effective mitigation of voltage overshoot and emphasizing the critical role of probe bandwidth and loading in nanosecond-scale measurements.

Collectively, the results of this thesis establish series-connected wide-bandgap devices, driven by appropriately designed transformer-coupled and programmable gate drivers, as a viable and scalable building block for next-generation high-voltage switching systems. The proposed solutions significantly reduce the complexity traditionally associated with high-voltage converters, enabling compact, cost-effective, and high-performance switching modules suitable for power-electronics-based arbitrary waveform generators. Beyond testing applications, the findings of this work have broader implications for medium- and high-voltage DC converters, pulsed power systems, and other applications in emerging power-electronics-dominated grids.

In conclusion, this thesis combines both fundamental insight and practical design methodologies that bridges the gap between low-voltage wide-bandgap device capabilities and high-voltage system requirements. By enabling flexible, and scalable high-voltage switching using mature commercial devices, this work supports the development of advanced testing infrastructure and power conversion technologies essential for the sustainable, resilient, and electrified energy systems of the future.

6.2 Research Questions

This section gives an overview of the research questions posed in Chapter 1 and answers them.

Research Question 1: What methods exist to achieve voltage balancing in series-connected switching devices to develop a high voltage switch for MMC-based arbitrary waveform generator, and which factors govern uniform static and dynamic voltage distribution among these devices?

Reliable operation of series-connected devices depends critically on effective voltage-balancing strategies. The main methods can be classified as:

1. **Voltage clamping techniques** – using auxiliary components to limit overvoltage on individual devices.
2. **Passive balancing networks** – employing resistive and/or capacitive elements for static and dynamic voltage sharing.
3. **Active gate control methods** – dynamically regulating individual gate signals to balance voltages.
4. **Gate-current synchronization approaches** – typically implemented using transformer-coupled architectures to ensure simultaneous switching.

Uniform static and dynamic voltage distribution is influenced by several factors, including:

- **Intrinsic device parameters** – threshold voltage variations, parasitic capacitances, and on-resistance differences.
- **Extrinsic parasitics** – stray capacitances and inductances in layout and packaging.
- **Gate-drive signal characteristics** – timing, slew rate, and synchronization, which are the most critical contributors to voltage imbalance during fast switching. Conventional approaches can experience up to 40% imbalance due to these mismatches.
- **Measurement setup effects** – probe-induced parasitic capacitance, impedance, and bandwidth limitations, which can significantly distort voltage sharing, particularly in ultrafast GaN-based systems.

Overall, gate-signal mismatch and measurement probes parasitic elements are the most dominant factor affecting voltage balancing in series-connected devices. Gate-current synchronization techniques implemented using transformer-coupled gate drivers are most effective for achieving well-matched gate signals and uniform dynamic voltage sharing, while appropriate probe-parasitic compensation mitigates measurement-induced distortions.

Research Question 2: Which gate-driving technique provides nearly even voltage balancing across series-connected SiC MOSFETs in a high-voltage AWG application while being open loop, straightforward to implement with minimal additional circuitry, cost-effective, and compatible with control using a standard microcontroller for programmable switching?

The literature review and experimental investigations conducted in this thesis confirm that transformer-coupled gate-current synchronization is an exceptionally effective gate-driving technique for series-connected SiC MOSFETs, offering excellent scalability, very good high-voltage isolation, and superior dynamic voltage balancing through the delivery of closely matched gate signals. By ensuring simultaneous switching across devices, this approach inherently promotes nearly uniform static and dynamic voltage sharing, making it particularly attractive for high-voltage AWG applications. However, the principal limitation or Achilles' heel of the conventional transformer-coupled gate drivers is their strict dependence on the transformer switching frequency, which prevents direct turn-on and turn-off control based on user-defined input signals and significantly limits switching flexibility critically needed for arbitrary waveform generation. This PhD thesis introduces a novel and experimentally validated gate-driving technique based on a dual complementary transformer configuration, which preserves the inherent advantages of transformer-coupled synchronization while decoupling device switching from the transformer operating frequency. The proposed technique is open-loop, straightforward to implement, requires minimal additional circuitry, and is cost-effective, while remaining fully compatible with standard microcontroller-based control for programmable switching. The architecture enables programmable turn-on and turn-off control, independent adjustment of switching frequency and duty cycle, thereby extending transformer-coupled gate drivers to flexible, cost-effective, and high-performance MMC-based high-voltage arbitrary waveform generation.

Research Question 3: Which technique can be applied to extend the voltage-blocking capability of ultrafast lateral GaN devices for future high-frequency high-voltage AWG applications?

The voltage-blocking capability of ultrafast lateral GaN HEMTs can be effectively extended by series-connecting multiple devices and driving them using a modified open-loop, transformer-coupled gate-current synchronization technique as is developed for SiC MOSFETs and is experimentally validated through prototype of two series connected GaN devices. Transformer-coupled gate drivers offer a fundamentally simpler and more robust solution, providing inherent synchronization, strong isolation, and dynamic voltage balancing without reliance on real-time feedback. However, to fully exploit the intrinsic speed of GaN devices in series and extend their operation into the kilovolt regime, the transformer excitation stage and associated magnetic components must themselves exhibit exceptionally fast transient performance. This PhD thesis addresses this requirement by employing simple GaN-based full-bridge excitation circuits, rather than the complex E-class oscillators used in other researchers work, and by systematically identifying and optimizing key transformer parameters such as leakage inductance, coupling coefficient, and compensation capacitances that govern high-speed gate-current transfer. The proposed technique is experimentally validated. The combined optimization of the excitation stage and transformer design, with emphasis on achieving strong magnetic coupling, enables efficient ultrafast gate-current transfer. As a result, the intrinsic high-speed switching capability of GaN devices is successfully preserved in transformer coupled series-connected configurations. As a result, nearly uniform dynamic voltage distribution is achieved while retaining the speed, efficiency, and scalability required for future high-frequency, high-voltage AWG applications.

6.3 Recommendations for Future Work

Based on the conclusions and answers to the research questions of this thesis, the following recommendations for future work can be given:

1. **Enhancement and adoption of series-connected wide-bandgap switches**

   For medium and high-voltage arbitrary waveform generator applications requiring fast switching and compact implementation, series-connected SiC MOSFETs and GaN HEMTs are recommended as a practical and scalable alternative to single high-voltage devices. Further work should focus on advancing the proposed novel open-loop voltage-balancing technique into a compact, plug-and-play switching module PCB, including high-voltage potting and insulation, to demonstrate robustness, ease of integration, and suitability for deployment in practical high-voltage AWG systems.

2. **Use of transformer-coupled, gate-current-synchronized drivers**

   For series-connected devices, gate-driving architectures that combine transformer-coupled isolation with synchronized gate-current delivery and programmable control are recommended. Such drivers provide robust voltage sharing, high isolation strength, scalability, and implementation simplicity, while also decoupling switching frequency and duty cycle from transformer constraints. This enables flexible arbitrary waveform generation without sacrificing voltage balance. Future work should investigate the possible

configurations of an integrated half-bridge / full-bridge switching module by modifying the proposed multi-transformer coupling.

3. **Careful consideration of measurement practices**

   Measurement probe effects must be explicitly accounted for in both experimental validation and system design. Proper probe compensation, high-bandwidth instrumentation, and minimized probe loading are essential to avoid misinterpretation of voltage sharing and switching performance. For future work involving series-connected switching devices, probe compensation should be incorporated as a prerequisite for all voltage measurements. Further investigation of measurement-related and other parasitic influences affecting voltage balancing across series connected devices is recommended to improve accuracy of experimental characterization.

4. **Extension to ultrafast GaN-based systems**

   For high-frequency and nanosecond-scale applications, series-connected GaN HEMTs driven by optimized transformer-coupled gate drivers are recommended. Future work should focus on enhancing their capability to reliably drive inductive loads, while rigorously addressing overshoot mitigation, loop inductance minimization, and measurement bandwidth.

5. **System-level integration and Scalability**

   Future research should focus on integrating the high-voltage switches developed in this thesis into half-bridge or full-bridge modules, which can serve as modular building blocks for constructing full-fledged MMC-based arbitrary waveform generators. Additionally, further studies should investigate the scalability of series connected switching modules to higher voltage levels and evaluate their performance with next-generation wide-bandgap devices that exceed current voltage limits.

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List of Publications

Publications Related to the Thesis

Journals

- S. Ghafoor, M. Kulkarni, R. Mirzadarani, P. Vaessen and M. G. Niasar, "A Scalable Isolated Gate Driver With Programmable Frequency and Duty Cycle for Series-Connected SiC MOSFETs," IEEE Open Journal of the Industrial Electronics Society, vol. 6, pp. 95-114, 2024.
- S. Ghafoor, R. Mirzadarani, H. Dialani, P. Vaessen and M. G. Niasar, "Voltage Balancing in Series-Connected GaN Devices using Scalable Transformer-Coupled Gate Driver," IEEE Open Journal of the Industrial Electronics Society, 2026.
- W. Zhao, S. Ghafoor, G. W. Lagerweij, G. Rietveld, P. Vaessen and M. G. Niasar, "Comprehensive Investigation of Promising Techniques to Enhance the Voltage Sharing among SiC MOSFET Strings, Supported by Experimental and Simulation Validations," Electronics, vol. 13, no. 8, 2024.

Conferences

- S. Ghafoor, R. Mirzadarani, P. Vaessen and M. G. Niasar, "Resonance Frequency Optimization in Transformer Gate Drivers of Series-Connected SiC MOSFETs with Programmable Switching Characteristics for High-Voltage Testing" in ISH 2025, The 24th International Symposium on High Voltage Engineering, Karuizawa, Japan.
- S. Ghafoor, R. Mirzadarani, P. Vaessen and M. G. Niasar, "Design of a High-Voltage, High-Frequency Solid-State Switch Using Series-Connected SiC MOSFETs and a GaN HEMT-Based Transformer-Coupled Gate Driver for Dielectric Insulation Testing of a Renewables-Rich Future Energy Grid" in International Conference on Dielectrics ICD 2026, UK.

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Thank you Prof. Peter Vaessen for giving me so much of your time at TU Delft. From my PhD agreement to my thesis, you went so thoroughly from every document I sent for review that your feedback felt like a reward. I felt like a million dollars knowing that you really went into what I wrote. In my entire PhD period, I have never seen you in anger or a bad temper. You'd always be in a charming mood. I am really inspired by your management style. In every meeting, you'd be engaging people to give out their own opinion instead of imposing yours. You'd propose an idea with such enthusiasm but if not supported by majority, you'd just let it go. In our very last workshop, you gave an example of top management asking you for a solution but you always offered to initiate the process of finding solutions instead of solution. I have seen you doing that in our HVT meetings. You have shown practically shown me a very democratic way of running an organization despite being an expert of your field and having a position of power.

Thank you Mohamad for interviewing and accepting me. People talk about how great it is to listen to Michael Jackson and I tell them it's even great to work with him. You are the Michael Jackson of Electrical Engineering. I have seen legendary people working with you like Geis, Reza, Mahesh, Suraj and so many more. They were all very inspired by you. You have some unexplainable energy and aura that just captures people around you. I feel rewarded by the divine that despite being very non-technical and average student, I was able to secure a spot with you. You never lost your cool and composure in every meeting that we had where I would put up very idiotic questions

and you would answer each one of them from the very basics. You'd ask again and again if I understood or should you explain again. That kind of patience is way bigger than that of a mother for a child. I would ask you to stay late in lab for the experiments and you never refused even a single time. You helped me even solder boards. I properly re-did my whole electrical engineering with you. Scientific studies say the biggest regret people have is their education and career. But everyone who has worked with you believes that you were born to be an electrical engineer and a teacher. I have been attacked with depression and panic attacks a lot in past four years because of the weather, work and a lot of things, but I managed it all without taking any anti-depressant because every weekly meeting with you was an anti-depressant itself. I would enter the meeting disappointed and leave reborn with hope. Your energy throughout the PhD has been beyond inspiration.

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I would like to express my sincere gratitude to Prof. Marjan Popov for demonstrating that elegance and grace can thrive even within the highly technical and often abstract world of electrical engineering. In a field frequently perceived as dry and complex, you brought a distinctive human dimension through your presence, your clarity of speech, and the confidence with which you carried yourself. Your personal style, your way of engaging with students, and even the small details how you entered a room, how you wore your coat or muffler left a lasting impression. I have witnessed master's students subtly copy not only your academic rigor but also your composure and professionalism. That quiet influence speaks volumes about your impact as an educator. Beyond your technical expertise, you showed us that how we present ideas, how we communicate, and how we embody our profession matters just as much as the knowledge itself. Just as universities teach entrepreneurship, engineering ethics, and engineering economics, I genuinely believe there should be a mandatory course on "engineering grace" as well.

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tradition, they have been a welcome pause, a moment to reconnect, reflect, and recharge. Especially during the long and often dark winter months, those Fridays felt like a light at the end of the tunnel, bringing warmth, laughter, and a sense of community that carried us through the challenges of research life.

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And now to the most special person in my entire life, my sheikh, Reza. I could write books about you and even they won't do justice. After your interview, Mohamad told me that a guy will be coming in July 2022, and you will learn a lot from him. And boy was he right about it or what. Its not just technical stuff that I learned from you, you know a lot about everything. I feel like you already have lived many lives on this planet and are resurrected. I thought I knew the concept of mentor-mentee, but you showed me what it really is. You've actually broke every concept that I had about everything, about electrical engineering, politics, economics, and about life in general. You'd offer company to a tour to some place and I would just immediately grab that opportunity without looking at my calendar thinking that the rest of the activities will be managed but not the time spent with you. There was a famous quote that the real travel happens inside, everywhere I went with you, there was a traveling happening inside me constantly.

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Thank you Marieke for prioritizing my task and immediately drop whatever you were working on every time I asked you for something. Thank you for showing me the most amazing spots to view Rotterdam skyline that I could never have discovered.

Thank you Imke. My house has lights because of you and every time I switch them when I enter or leave my house, I think of you. Shifting to a completely empty apartment with no lights was a very shocking experience for me and I thank you for helping me out during that very rough

period. Thank you for completely transforming my experiments into super fancy test setups. There is no way I could have had successfully conducted my high voltage tests if it wasn't for you. You have a beautiful gift of putting out simple solutions to complex problems in a very witty way like energy congestion. You made working in high voltage lab a very enthusiastic experience and I feel very passionate about Electrical Engineering because of you.

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even in the technical field. We'd bring up any topic from movies to politics to multi-nationals to housing crisis and you would enlighten us all on it in a very artistic way. Your technical jargons are almost poetic. Thank you for letting me being around you which was a privilege.

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Thank you Jianning for lending me your legendary cameras for so many occasions. I could not have made such great memories without your gadgets. I would discuss with you some unbelievably impossible technical scenarios that even Hollywood directors would say are too impractical, yet you would entertain those ideas. You'd go into technical details like how much power or material or time would it take in solid terms and bring it out of impossibility. Billionaire entrepreneurs can make a fortune if they have you because you can make all of their ideas possible.

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There are many more people I wish I could thank, but memory and energy have their limits. **The truth is, very little in us is entirely our own.** We are shaped by the generosity, ideas, and character of those around us. **None of us becomes who we are without the influence of others.** We are all, in some way, a mosaic of borrowed strengths, fragments of mentors, friends, colleagues, and family. **What we fail to learn, the good qualities we choose not to adopt, may be our only true omissions. The better parts of us are rarely self-made; they are gifts we were fortunate enough to receive and wise enough to keep. In this sense, humility is not optional, but a necessary recognition of reality.**

Curriculum Vitae

Sohrab Ghafoor

11-01-1987 Born in Mirpur, Azad Kashmir, Pakistan.

Education

2005-2009 BSc in Electrical Engineering
AJK University, Pakistan.

2010-2013 MSc in Engineering Management
National University of Science and Technology, Islamabad.

2022-2026 Ph.D. in Electrical Engineering
Delft University of Technology, Delft, Netherlands.

Thesis: Development Of A High Voltage Switch Using Series Connected Low Voltage Devices For Development Of Power Electronics Based Arbitrary Waveform Generator
Promotor: Prof. Ir. Peter Vaessen

Work Experience

2009-2010 BSS Engineer, North Region Kashmir
HUAWEI Technologies.

2010 – till date Electrical Engineer
National Engineering and Scientific Commission, Islamabad, Pakistan.

Awards

2010 National University of Science and Technology MSc Scholarship Award
2021 National Engineering and Scientific Commission PhD Scholarship Award

The future renewable-rich power grid is introducing unconventional electrical stresses and demands new technlogies to reproduce them. This thesis transforms mature low-voltage switching devices into scalable high-voltage high frequency switching systems, enabling compact advanced high-voltage testing solutions for future electrical grids.

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