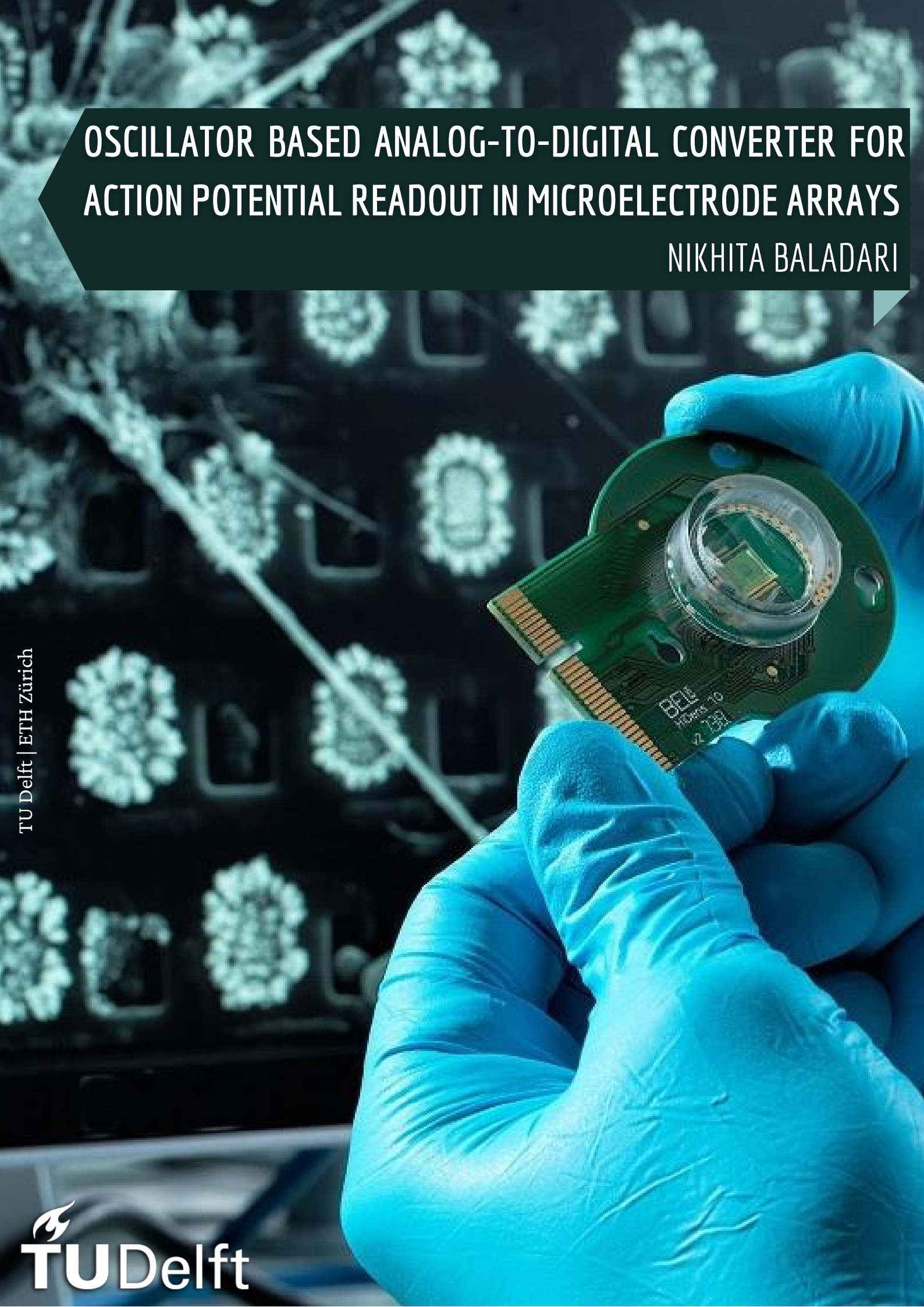
OSCILLATOR BASED ANALOG-TO-DIGITAL CONVERTER FOR ACTION POTENTIAL READOUT IN MICROELECTRODE ARRAYS

NIKHITA BALADARI



TU Delft | ETH Zürich

TUDelft

Oscillator based ADC for Action Potential Readout in Microelectrode Arrays

by

Nikhita Baladari

at the Bio Engineering Lab, ETH Zürich under the supervision of
Dr. Fernando Cardes and Prof. Andreas Hierlemann,

to obtain the degree of Master of Science in Biomedical Engineering
at the Delft University of Technology,
to be defended publicly on August 28, 2020.

Student number:	4815882	
Project duration:	August 1, 2019 – January 31, 2020	
Thesis committee:	Dr. Virgilio Valente,	TU Delft, supervisor
	Prof. Dr. Ir. Wouter Serdijn,	TU Delft
	Prof. Dr. Ir. Ronald Dekker,	TU Delft

TU Delft

Acknowledgments

This thesis would not have been possible without the invaluable guidance of Dr. Fernando Cardes, my thesis supervisor, who has been my constant pillar of confidence throughout the project. His brilliance in this field never ceases to inspire me. Thanks for acknowledging and building my passion for bioelectronic design. I want to express my sincere gratitude to Prof. Andreas Hierlemann for providing me this opportunity to work at Bio Engineering Laboratory, ETH Zürich. He is the coolest professor I have met so far. I enjoyed working in this multi-disciplinary environment and have had the opportunity to learn something new every day from my teammates.

I want to thank Dr. Virgilio Valente, my advisor at TU Delft, whose constant feedback has always helped me and pushed me towards betterment. Thanks for the valuable suggestions and for helping me shape my thesis. I would like to thank Prof. Wouter Serdijn, who has always been supportive and encouraging during the decisions I had to take during my Masters.

As it goes without saying, my family has always been there for me throughout this journey. I should thank my mom, who never knew how to not believe in me, my dad, who always supported me in turning my dreams to reality, and my brother, who still thinks he has the coolest sister in the world (which he should). Thanks for always being there for me and never giving up on me.

I don't know if I should continue in the previous paragraph as I mention Srikanth Nallanthighal and Suryateja Sharma, who are more like family to me. My heartfelt thanks to Srikanth, who has constantly been babysitting me throughout my Masters. The Netherlands is home to me because of him. I want to thank Suryateja, who was the first person that inspired me to pursue a career in biomedical engineering. It is the greatest decision I have made, and he deserves all the credit for that. I want to thank all my friends who have been a part of this journey with me. Thanks to Akhil and Ganesh, who stuck by my side, despite my tantrums. Thanks to my 'Master gang' at ETH, Giulia, Ashlyn, Bram, Patricia, Philip, and Jeanne, who made my exchange semester smooth and memorable.

Abstract

The functioning of the brain depends on the interplay between a large number of neurons. To understand the information processing in neuronal networks, we need tools to record the electrical activity of cells at high resolution. Microelectrode arrays (MEAs) are predominantly used to measure neuronal activity at high spatial and temporal resolution. With the advent of complementary metal-oxide-semiconductor (CMOS) based MEAs, it has been possible to design high-density MEAs with electrode sizes comparable to that of the individual neurons, allowing sub-cellular resolution. CMOS technology has also facilitated the on-chip signal conditioning needed to record the low-amplitude bio-signals with superior signal quality. In this thesis, a readout architecture for in-vitro MEAs has been proposed for a low-noise extracellular action potential (AP) readout.

One of the challenges in MEA implementation is the design of thousands of low-noise readout channels for simultaneously recording the signals. There is a need to design low-noise ADCs with optimal power and area consumption. In this thesis, a unique low-noise oscillator based sigma-delta ($\Sigma\Delta$) ADC has been designed for MEA applications. With the advantages of oversampling and time-encoding techniques, the in-band noise has been optimized, without increased hardware complexity. The simple implementation of this proposed ADC makes it efficient in terms of area and power consumption.

The integrated circuit for this oscillator based $\Sigma\Delta$ ADC has been implemented in 0.18 μm CMOS technology to demonstrate the feasibility of high-order oscillator-based ADCs for low-noise extracellular AP readout. It was possible to obtain a noise below 5 μV_{RMS} (simulations) and power consumption under 3 μW using this ADC, which approximately occupies an area of 0.002 mm^2. The action potential readout system implemented with this ADC has been taped-out for further analysis through measurements.

Contents

List of Figures

List of Tables

List of Abbreviations

AAF ..... Anti-aliasing filter

AC ..... Alternating current

ADC ..... Analog-to-digital converter

AFE ..... Analog front-end

AP ..... Action potential

APS ..... Active pixel sensor

CMOS ..... Complementary metal-oxide-semiconductor

CT ..... Continuous time

DAC ..... Digital-to-analog converter

DC ..... Direct current

DFF ..... D-flip flop

DPS ..... Digital pixel sensor

DRC ..... Design rule check

DSP ..... Digital signal processing

DT ..... Discrete time

EAP ..... Extracellular action potential

EEG ..... Electroencephalography

ENOB ..... Effective number of bits

F2D ..... Frequency-to-digital converter

FFT ..... Fast Fourier transform

FPGA ..... Field programmable gate array

HD ..... High-density

HPF ..... High pass filter

iPSC ..... Induced pluripotent stem cells

IRN ..... Input referred noise

IS ..... Input stage

LFP ..... Local field potential

LPF ..... Low pass filter

LSB ..... Least significant bit

LVDS ..... Low-voltage differential signaling

LVS ..... Layout versus schematic

MEA ..... Microelectrode array

MOSFET ..... Metal-oxide-semiconductor field-effect transistor

MPW ..... Multi-project wafer

MRI ..... Magnetic resonance imaging

MSB ..... Most significant bit

OSR ..... Oversampling ratio

PET ..... Positron emission tomography

PPS ..... Passive pixel sensor

PSD ..... Power spectral density

PSS ..... Periodic steady-state analysis

QE ..... Quantization error

RMS ..... Root mean square

SAR ..... Successive-approximation register

ΣΔ ..... Sigma-delta

SM ..... Switch matrix

SNR ..... Signal-to-noise ratio

SQNR ..... Signal-to-quantization noise ratio

VCO ..... Voltage-controlled-oscillator

VLSI ..... Very-large-scale integration

1 Introduction

The brain is the most complex organ in our body, and understanding it has always been a challenge. It is made up of billions of neurons massively interconnected at hundreds of trillions of junctions and thousands of kilometer-long wiring, forming the world's most complex network [1, 2]. The electrochemical reactions between neurons are the core of the brain's operation, some of which include memory, cognition, and sensory functions. Any abnormality in these interconnections and electrochemical reactions translates into neurological disorders such as epilepsy, Alzheimer's, Parkinson's, dementia, etc. Studying the neurons and neural networks is crucial to understand the functioning of the brain, the origin of neurological disorders, and potential treatments. Many techniques have been developed to study this neurophysiology. Figure 1.1 shows the spatial and temporal resolution of some of these techniques used for neurophysiology studies. Spatial resolution is defined as the ability to discriminate two different points in space, while the temporal resolution is the time-scale precision of the recording.

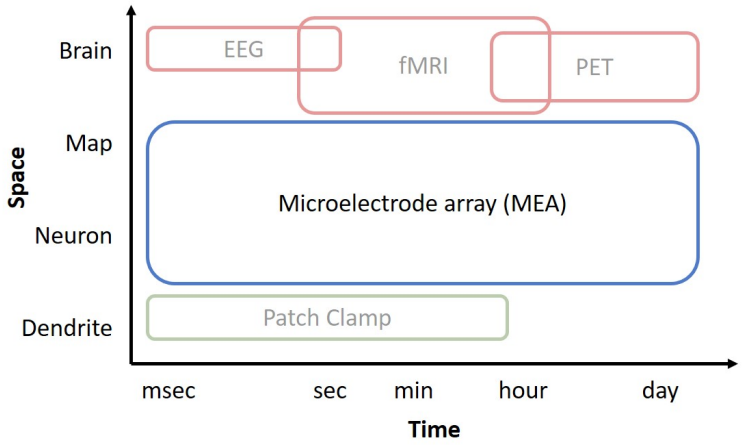


Figure 1.1: Spatial and temporal resolution of neuronal sensing techniques

At the macro-level, there are techniques such as electroencephalography (EEG), functional magnetic resonance imaging (fMRI), positron emission tomography (PET) scans, etc. which are non-invasive brain imaging methods (figure 1.2c). However, these techniques are capable of sensing the electrical changes of thousands of neurons that are signaling at the same time rather than detecting the electrical activity of a single neuron, resulting in low spatial resolution. There are patch-clamp techniques at the micro-level that can detect the electrical activity in single cells, 'patch'-es of the cell membrane, or even single ion channels for studying electrophysiology at a single-cell level. However,

patch-clamp is invasive, where the cell membrane is punctured to record the intracellular signals (figure 1.2a). It is also limited by the number of cells that can be probed at the same time, and cell viability.

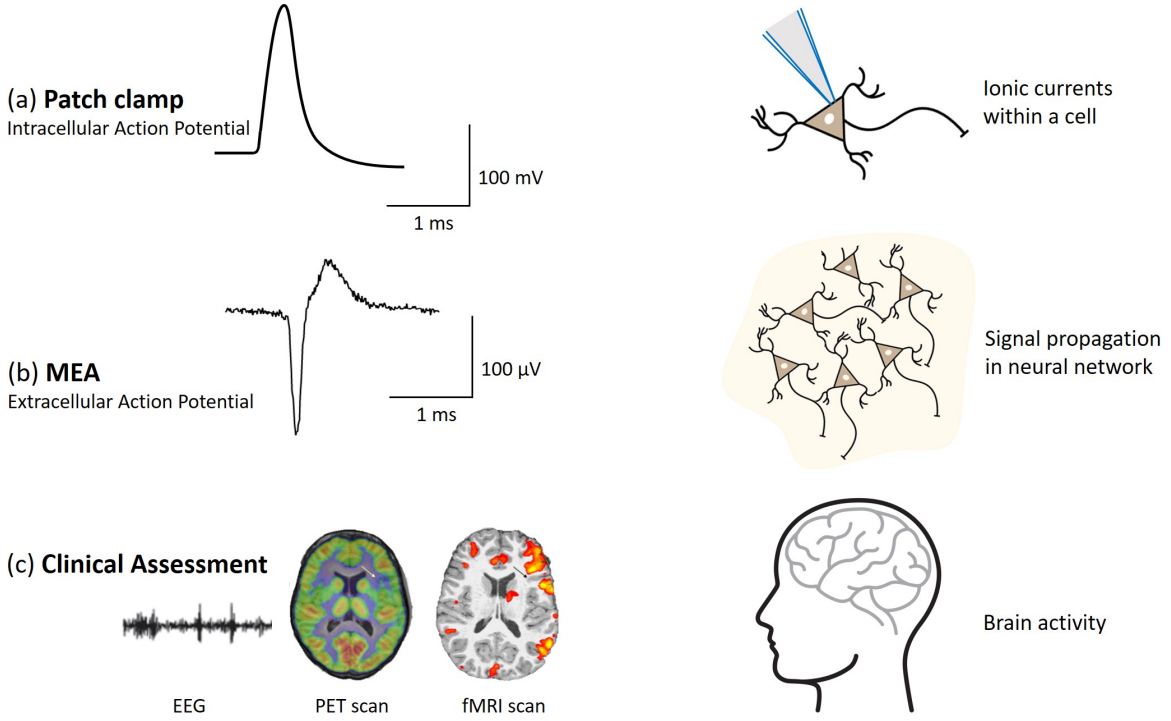


Figure 1.2: Neuronal sensing techniques and their application

High spatial- and temporal- resolution techniques are essential to record the electrical activity of cells to monitor the electrophysiology at both single-cell and cellular network levels. Microelectrode arrays (MEAs) can measure the extracellular signals, such as local field potentials (LFPs) and extracellular action potentials (EAPs) (figure 1.2b), via electrodes to study the electrical activity of cells. MEAs enable carrying out long-term measurements as they are non-invasive, while providing the necessary spatial resolution required to quantify the electrical activity of neuronal networks or even single-cell activity.

MEAs can be used in-vivo to study the brain using implantable probes (having electrodes) and, in-vitro to study the neuronal activity in cell-cultures, brain slices, etc. Although in-vivo MEAs can be used for the study of a fully functional brain giving a realistic understanding, they are invasive and thereby can create tissue damage. In-vitro MEAs are used for fundamental research to investigate the signal propagation, neuroplasticity, and drug screening and toxicological screening [3]. The focus of this thesis is on in-vitro MEAs that are predominantly used to study individual neurons and small networks in detail, detecting the small and fast action potentials.

1.1 CMOS based in-vitro MEAs

MEAs should be able to detect the low-amplitude extracellular signals, typically in hundreds [4, 5] or sometimes even tens [6] of μV range, with high signal quality. Also, since the signals being recorded originate from the cells in close proximity to the electrodes, the MEA should be able to separate the individual signal sources [7]. A low electrode pitch (figure 1.3) is required to resolve sub-cellular details from single neurons. Complementary metal-oxide-semiconductor (CMOS) technology can provide the possibility of integrating a large number of microelectrodes on a small chip. Using CMOS technology, on-chip signal conditioning such as amplification and filtering can be performed to record the low amplitude bio-signals with maximum precision [4]. Also, the analog-to-digital converters (ADC) can be integrated in the silicon closer to the electrodes to reduce the parasitics and interferences [8]. CMOS MEAs offer electrodes with sizes comparable to that of a single cell, and minimally spaced as shown in the figure 1.3b thereby providing access to the activity of individual cells at sub-cellular resolution.

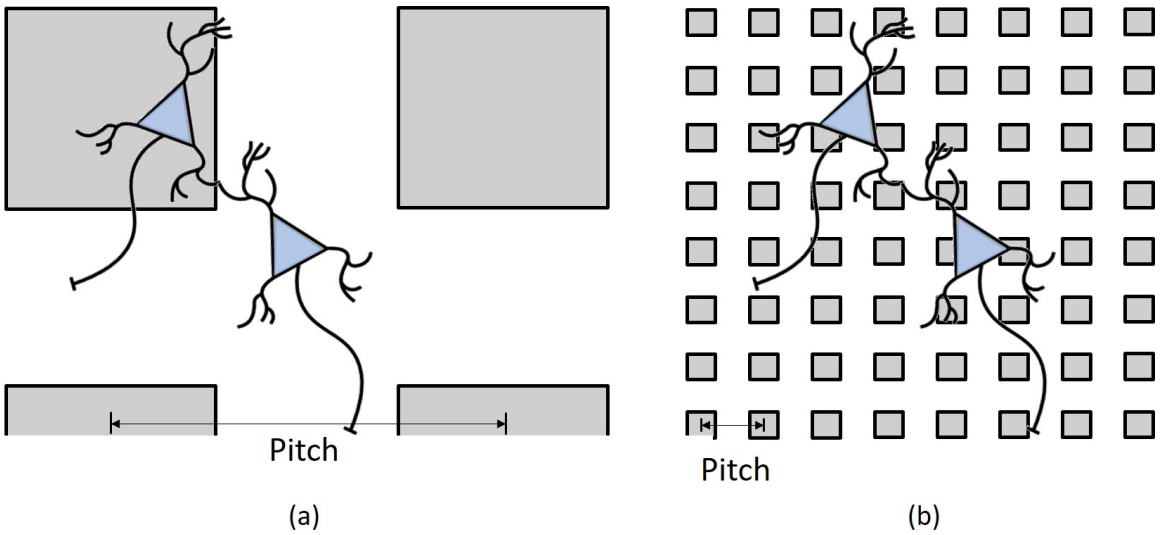


Figure 1.3: Illustration of neurons on top of MEAs. a) In MEAs with large pitch, signals from different neurons are captured by the same electrode. b) In CMOS based MEAs with small pitch, each neuron can be measured by several electrodes.

1.2 In-vitro MEA applications

In-vitro MEAs can be used to carry out experiments on different biological preparations such as primary neurons, brain slices, retina, cardiomyocytes, etc. MEA experiments with retina target the understanding behind how the eye perceives visual information. MEAs are also being used to study the synchronous neuronal activity using brain slices [9] to decipher the pathology of the brain [10]. MEA experiments

with acute brain slices, which mimick the in-vivo environment, are being used to understand and model neurological disorders such as epilepsy [11].

Induced pluripotent stem cell (iPSC) derived neuron cultures are human-derived stem cells that have been found to generate spontaneous neuronal activity under the influence of different physiological, toxicological, and pharmacological conditions [12]. However, the amplitude of extracellular AP in iPSCs is as low as tens of μVolts, which is relatively lesser than the extracellular AP in primary cells [6, 13]. Ultra-low noise MEAs [8, 14] are now emphasizing on accurately detecting these low-amplitude iPSC signals [6], which could allow MEAs to replace the in-vivo animal testing for drug- and toxicology-screening, that is under ethical debate.

In contrast to the intracellular recording, which invasively picks up the signal (patch clamp), in MEAs, the electrodes record the extracellular signals of all neurons in the vicinity. This makes it difficult to assign each extracellular action potential (spike) to the individual neuron. High-density MEAs that provide high-spatial resolution can efficiently separate individual neurons, and spike sorting algorithms can be used to classify the spikes and identify which neuron is generating each spike [5]. Using the combination of high-density MEA and patch-clamp techniques, it has been possible to understand how the multiple input signals integrate and interact within a single-cell [15].

1.3 Challenges in MEA readout design

A typical CMOS MEA system with on-chip signal-conditioning circuitry is shown in figure 1.4. The signals recorded by the electrode array are filtered, amplified, and digitized by the 'readout blocks' shown in figure 1.4b. Two of the widely used readout architectures in MEAs are the switch matrix (SM) and active pixel sensor (APS). In SM MEAs, a flexible routing scheme is used to record only from a subset of electrodes simultaneously. In this architecture, the readout circuitry is entirely placed outside the array area, leaving sufficient area to implement large low-noise analog front-end amplifiers, resulting in a high signal-to-noise ratio (SNR). SM MEAs can detect very low-amplitude signals, such as iPSC AP (tens of μVolts) [6], owing to their high SNR. However, typically only 10% of the total available electrodes are used during simultaneous readout, resulting in complexity during experiments. APS MEAs, on the other hand, can record from all the electrode simultaneously, which is referred to as 'full-frame readout'. In these MEAs, the front-end amplifiers are integrated beneath the electrode in the pixel. Due to the limitations in the available area to implement the active circuitry, APS-based MEAs have relatively higher noise. APS MEAs are hence more suitable for recording large-amplitude signals, such as action potentials (APs) of primary neurons and local field potentials (LFPs) [16].

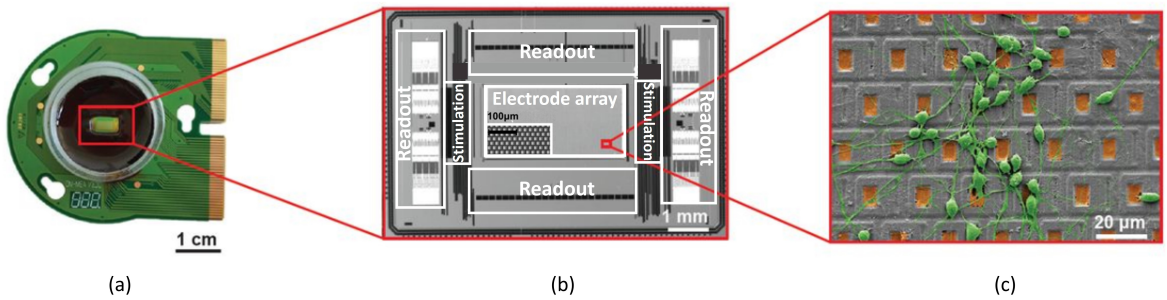


Figure 1.4: Typical CMOS MEA system showing the (a) packaged device used for experiments, (b) chip micrograph showing the electrode array, readout and stimulation blocks, and (c) micrograph of primary neurons cultured atop the MEA [16].

This thesis aims to overcome the limitations of the existing SM and APS MEAs, by designing a low-noise readout architecture for APS MEAs, targeting simultaneous readout from thousands of electrodes, without compromising the spatial resolution of the MEA. The target MEA implemented with this readout channel should have the combined benefits offered by the SM and MEA topologies, as shown in table 1.1.

	SM MEA	APS MEA	Target APS MEA
Parallel readout channels	<10%	100%	100%
Noise per readout channel	<5 uV	>10uV	<5 uV
Most useful application	Single-cell studies	Cell-network studies	Both

Table 1.1: Desired specifications for the target APS MEA in comparison to the existing SM and APS MEAs.

The two key features that should be preserved while implementing APS MEAs are spatial resolution and signal quality. To achieve the target spatial resolution, simple AFE architecture should be used, and for superior signal quality, the noise from the readout circuitry should be minimized. However, the typical readout blocks in MEAs include multi-stage AFEs and SAR ADCs, both of which use complex hardware that is undesirable for the target MEA. To overcome these limitations, a simple in-pixel AFE architecture should be implemented, and compact ADCs should be implemented outside the array with optimized noise and area.

Sigma-delta ($\Sigma\Delta$) data converters are known for their efficient analog-to-digital conversion for low-bandwidth applications making them a suitable choice for MEAs. Time encoding based $\Sigma\Delta$ ADCs have been reported to have improved SNR and potential advantages in terms of area and power consumption [17, 18], making them the significant design choice in this thesis.

1.4 Time encoding based ADCs

The task of implementing MEAs in deep-submicron process environment comes with its challenges. Although CMOS technology scaling is seen as efficient in terms of area and power consumption, which favors the MEA applications, analog circuitry design gets intensively complex. This is because analog circuits are driven by process parameters such as voltage supply, transistor gains, voltage thresholds, etc. These parameters significantly vary with each technology node [19]. On the other hand, an upside to shifting towards smaller technology nodes is the fast switching of the MOSFETs offering excellent accuracy in timing at high frequencies. So, as an alternative to amplitude quantization in data converters, time encoding can be used due to its feasibility of implementation in low-voltage CMOS technology nodes [18–21]. The advantage of time-encoding systems is that most of the design can be implemented using digital circuitry, which benefits from CMOS scaling.

One example of this time-encoding approach is a voltage controlled oscillator (VCO), in which the input voltage is encoded into the frequency of the oscillator (frequency encoding). There are two possible ways [22] of integrating the VCO in the MEA readout circuitry, which are shown in figure 1.5. In both cases, the filtered and amplified (by AFE) electrode voltage variations modulate the frequency of the VCO, whose output is digitized using a frequency-to-digital modulator. In the first architecture (figure 1.5a), the VCO is integrated in the pixel area itself along with the AFE circuitry. However, realizing this architecture is complicated, given the size restriction on the pixel area. In the second architecture (figure 1.5b), the VCO is integrated outside the pixel and designed as a VCO based ΣΔ modulator. In this thesis, the second architecture, 'VCO based ΣΔ ADC,' is considered for implementing the MEA readout, and the AFE is integrated as an input stage in the ADC while designing the readout channel (figure 1.5b).

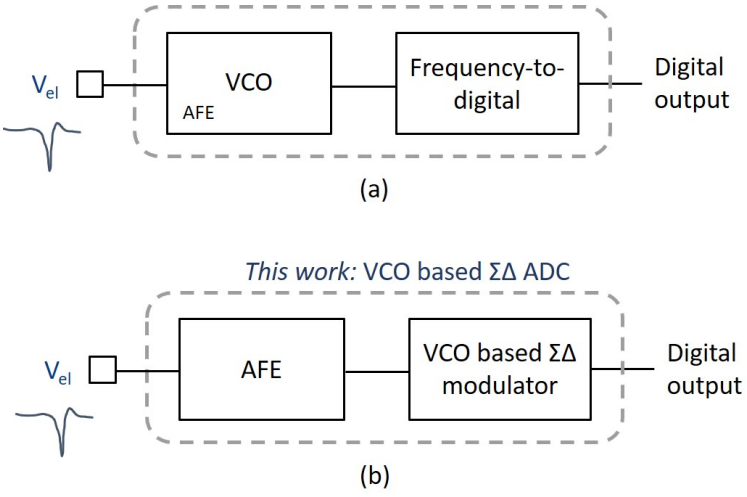


Figure 1.5: Possible VCO based readout architectures. (a) The VCO is integrated in the AFE and the off-pixel area is used for frequency to digital modulation (b) The VCO is integrated in a classical ΣΔ modulator outside the pixel area.

1.5 Thesis objectives

This thesis aims to bridge the gap between SM and APS MEA architectures, which are known for their high electrode density with low-noise, and full-frame readout, respectively. A low-noise oscillator based ΣΔ ADC for APS MEAs has been proposed in this thesis to read out the signals from all the electrodes simultaneously. The MEA implemented using this architecture should offer low-noise readout sufficient to detect signals as low as tens of μVolts, with high spatial resolution.

The thesis goals are further broken down as follows:

- Review the existing MEA readout architectures and design trade-offs to understand the specifications for different applications of MEAs.
- Design a compact low-noise oscillator based ADC for APS MEAs. The aim is to optimize the readout channel noise to 5 μV_{RMS} in the 300 Hz - 7 kHz AP band using second-order noise shaping.
- Implement the proposed system in a test chip in 0.18 μm technology node, including all the necessary auxiliary circuits for testing and debugging the ADC.

1.6 Structure of the thesis

Chapter 2 introduces the terminology and signal flow in MEAs, followed by a discussion on the different readout architectures that can be used for implementing the MEAs. The two predominantly used MEA topologies, SM and APS, have been explained with a focus on the challenges, drawbacks, and design trade-offs faced by them. Taking support from this background knowledge, the problem statement of the thesis has been introduced, which is to 'design a compact low-noise ADC for APS MEA readout.' The MEA that can be implemented using this ADC has been benchmarked against state-of-the-art SM and APS MEAs to show the value of our design. The chapter ends with some findings on ΣΔ ADCs that have been deemed to be the right fit to achieve low-noise MEA readout requirements.

Chapter 3 starts with a brief introduction to the analog-to-digital conversion and the parameters that define the performance of the ADC, such as SNR and quantization noise. The chapter focuses on the theory and advantage behind oversampling, noise shaping, and time encoding, the conceptual pillars that support the design choice of an oscillator based ADC for APS MEAs. Chapter 4 focuses on the system-level design and implementation of the oscillator based ΣΔ ADC, which can be used for MEA readout. The train of thought behind the design of the VCO based ΣΔ ADC has been given in this section.

The circuit-level implementation of this readout architecture and the results obtained in the simulations are discussed in chapter 5. The design choices, layout design, and post-layout simulations are also reported here. Chapter 6 overviews and critically describes the entire process of the thesis and design implementation. The final results have been reiterated here and compared with the state-of-the-art bio-potential readout architectures. Some of the possible limitations of the design have been pointed out, and the dissertation finally ends with the conclusions and prospective work for the readout architecture that has been implemented in this thesis.

2 In-vitro Microelectrode arrays

To understand complex biological systems like the brain, we need to understand the connectivity and coordinated cell activity of electrogenic cells such as neurons. Microelectrode arrays are used to study the electrophysiology of cells, such as neurons, heart cells, and retina cells at a sub-cellular spatial resolution and a sub-millisecond time scale. Since they detect the extracellular signal generated by the cell population at interest, they can provide long-term measurements owing to their non-invasive nature. The electrodes are tightly packed to achieve sub-cellular spatial resolution, reducing the area allotted for wiring the electrodes to readout circuitry. Thanks to the CMOS technology, it is possible to integrate thousands of electrodes in a small area. It has also made the integration of on-chip amplification and digitization circuitry feasible, improving the signal quality.

The critical trade-off to make while implementing MEAs is between the spatial resolution and signal-to-noise ratio (SNR) that can be attained. High-spatial resolution requires small electrodes, increasing the electrode impedance, resulting in high thermal noise. The size of the transistors used for amplification and filtering should also be small, which again results in high flicker noise. For optimum performance of an MEA, these design trade-offs should be considered during the MEA design. The MEA signal flow and the different architectures used for realizing MEAs are discussed in this chapter to provide a rationale behind the objective of this thesis.

2.1 Signal flow in MEA system

Any electrical activity in a cell results in the flow of ions via ion channels. This, in turn, causes a change in the electric field in the extracellular space, acting as a volume conductor [4]. This change in the electric field is detected by the electrodes in the microelectrode array (figure 2.1). These signals are then filtered and amplified by the analog-front-end (AFE) circuitry and transduced to a digital readout by the analog-to-digital converter. Owing to the advances in the CMOS technology, it has been possible to integrate the AFE and ADC on the MEA chip itself. Having the AFE and ADC close to the sensing area results in reduced parasitics and interferences, thereby resulting in better SNR.

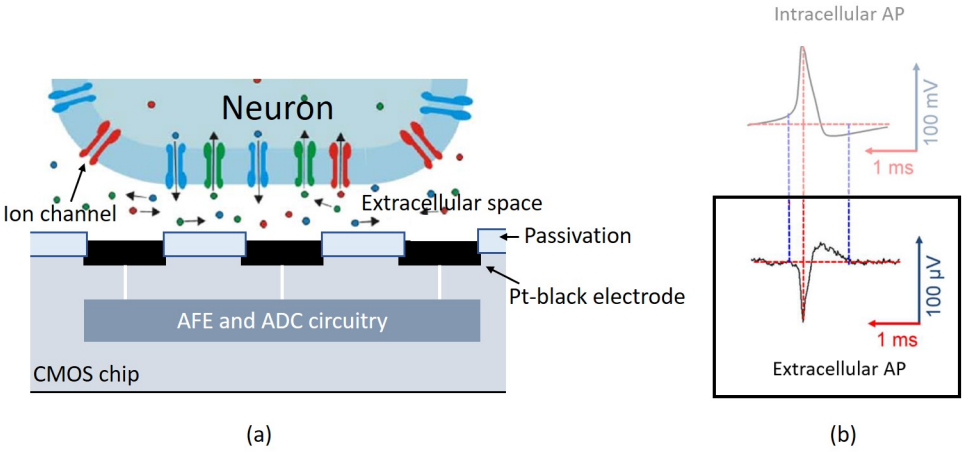


Figure 2.1: (a) Cell-MEA interface and (b) magnitude of extracellular action potential (AP) in comparison with the intracellular AP, modified from [4].

There can be interference from different noise sources, which can alter the SNR of the recorded signal. These noise sources include the thermal noise at the electrode-electrolyte interface, due to the size and hence the impedance of the electrode, and the noise from the hardware (AFE and ADC blocks) [5]. The noise from these sources must be minimized by optimizing the electrode size and reducing the intrinsic hardware noise for efficient MEAs. Also, the typical amplitude of the extracellular signal is in tens [6] and hundreds of μVolts range (figure 2.1b) [4], which manifests the criticality of designing low-noise circuitry with intrinsic noise much lesser than the amplitude of the recorded signal itself. The signal flow of the readout process in an MEA is shown in figure 2.2. In this thesis, the AFE and ADC blocks of the readout architecture are designed for optimum noise performance. The parameters that determine the fate of these readout blocks are the gain, bandwidth, and noise for the AFE, and the resolution and sampling rate for the ADC.

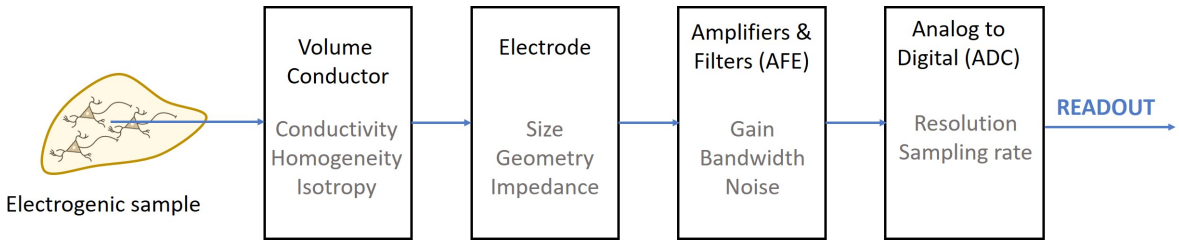


Figure 2.2: The readout process flow in an MEA and different parameters that effect the readout signal [5].

The standard CMOS fabrication process only allows the production of electrodes of certain materials, usually Aluminium alloy, which is unstable in contact with physiological solutions that are used during the experiments. Due to the toxicity and poor bio-compatibility of the contact material and to protect the CMOS circuitry from corrosion, a post-processing protocol is mandatory to seal the

CMOS part from the biological samples [23]. During this post-processing step, the CMOS chip is coated with a passivation layer (SiO_2/Si_3N_4)[23] and a suitable electrode material such as platinum [24], gold [23] or chloridized silver [25] is deposited on top of the contact material through the openings in the passivation layer (figure 2.1a) to ensure compatibility as well as decrease of the electrode impedance for better SNR [23–26]. Pt-black is often used as a coating on top of the electrodes [4] (figure 2.1a) for increasing the surface area, thereby further reducing the electrode impedance. The post-processed chip is mounted and wire-bonded, followed by encapsulation using epoxy resin [25, 27]. A glass ring that surrounds the MEA is mounted for culturing the biological samples after which, the MEA can be used for the experiments.

Different readout design strategies have been used over the past years in the attempt to realize high-density, low-noise, or full-frame readout MEAs. Some of these readout architectures will be described here to show their advantages, limitations, and potential improvement.

2.2 MEA readout architectures

Before starting the discussion on MEA topologies, some of the commonly used MEA terminologies are introduced here. 'Pixel' is the sensor element that picks up the signal, such as the extracellular potential, in MEAs. These MEA pixels can be passive, active, or digital based on the inclusion of the active elements beneath the electrode area, which picks up the signal. Passive pixel usually comprises just an electrode, and maybe some switches used to address and select the electrodes. On the other hand, the active pixel has an electrode and some active elements underneath the electrode area to buffer or amplify the detected signal. Recent advances in CMOS imagers show the possibility of using digital pixel, which consists of the electrode and an in-pixel ADC and memory, integrated beneath the sensing area. The digital pixels are grouped under the active pixel category here (figure 2.3), due to their in-pixel active elements.

MEAs can be implemented using different topologies based on the placement of signal conditioning circuitry with respect to the electrodes. The simplest way to design an MEA is to connect the electrodes to signal pads through fixed wiring, as shown in figure 2.3a with the signal conditioning circuitry implemented off-chip. This is a classic example of passive pixel topology. However, this results in long metal lines needed for routing the electrodes with the signal conditional blocks increasing the parasitic capacitance [28]. Also, due to the lack of active circuitry or multiplexing in the electrode array, the number of electrodes is limited by the number of signal pads that can be implemented. Figure 2.3b shows another approach with a passive pixel sensor (PPS) where the limitations of parasitic capacitance and number of pads have been handled by including active circuitry, for amplification and multiplexing, on-chip. However, since there is a one-on-one routing of the electrode and AFE, this approach still does not allow achieving high-density implementation of the microelectrodes due to the limitations on

interconnections within the array and inefficient usage of electrode array area [5].

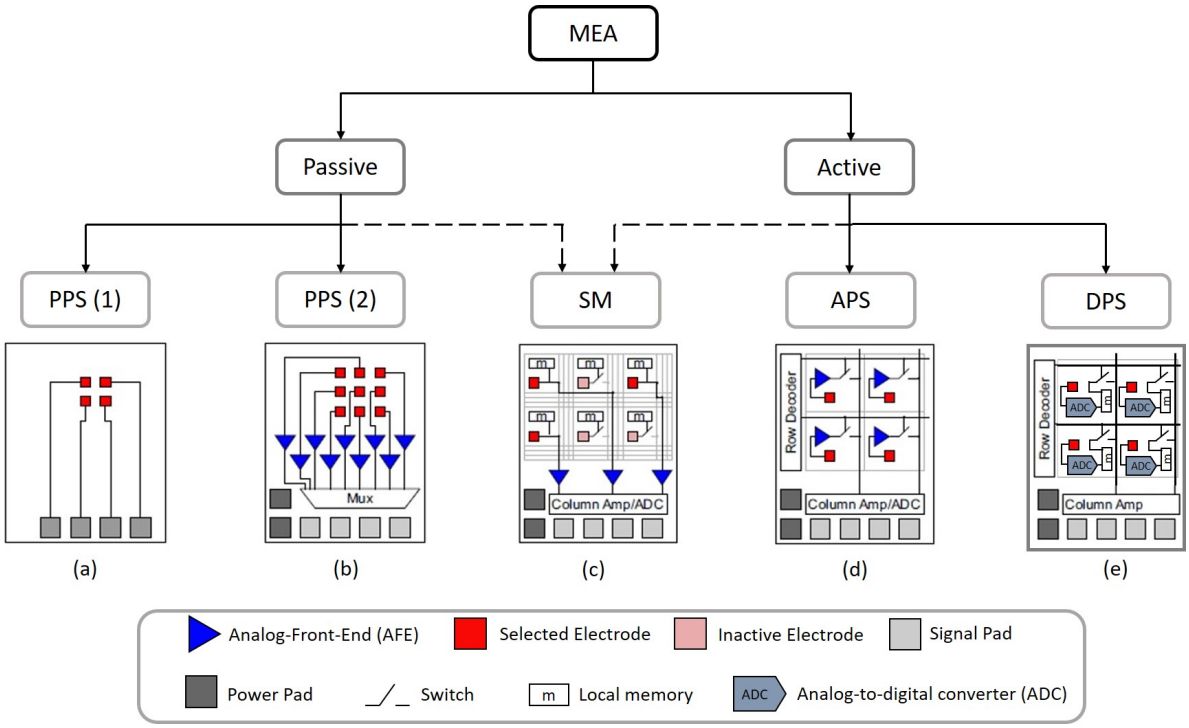


Figure 2.3: Classification of MEAs based on the type of pixel and placement of signal conditioning blocks (a) fixed wiring scheme with off-chip circuitry, (b) fixed wiring scheme with on-chip circuitry, (c) switch-matrix (SM) that allows flexible selection of electrodes, (d) active pixel sensor (APS) with in-pixel analog front-end, and (e) digital pixel sensor (DPS) with in-pixel ADC. Inspired from [5].

The MEA readout architecture, which is popularly known as 'switch matrix' (SM), is shown in figure 2.3c. In this topology, the electrode array is decoupled from the readout channels, and a subset of 'interesting' electrodes (selected electrode in figure 2.3c) can be flexibly chosen for readout [29]. The routing pathways are implemented such that the selected subset of electrodes is rewired flexibly to the available readout channels, outside the actual electrode array. An in-pixel local memory is used to set the state of the control signals needed for switching the respective electrodes. The main advantage of this topology is that, since the number of channels implemented for signal readout can be reduced depending on the designer's choice, the available area to implement the circuitry is high, allowing low-noise CMOS circuitry. However, it requires complex experimental protocols to identify the interesting electrodes, since not all electrodes can be chosen to detect the biological sample activity. MEAs implemented with this topology are often used for low-noise signal acquisition and when there is no need to record signals from all electrodes. Their low-noise operation also makes them advantageous in low-amplitude spike detection applications.

Another prevalent architecture used for the MEA implementation is the 'active pixel sensor' (APS) (figure 2.3d), which is similar to the image sensors in CMOS cameras. In this topology, the pixel

consists of an electrode along with a dedicated AFE block. Every pixel is sampled once within each frame resulting in a full-frame readout. The challenge lies in designing a low-noise AFE since the size requirements are quite restrictive for implementing high-density pixel array. Also, since the electrodes and biological medium themselves give out wide-band noise [5], a low-pass filter should be included inside the pixel to make sure this noise is not aliased into the signal band during sampling, further constraining the pixel area.

The digital pixel sensor (DPS) topology is shown in figure 2.3e with an in-pixel ADC, which can result in higher signal quality. However, the implementation of in-pixel ADC further increases the pixel area resulting in lower spatial resolution. This is why although they have not been prevalent in the consumer electronics market, they are used for image sensors [30]. However, there is a scope for implementing DPS based MEAs in the future, given the advances in the development of low-area and low-noise ADCs. In this section, an overview of the frequently used topologies for implementing MEAs, SM and APS, is given.

2.2.1 Switch matrix architecture

The most desirable features in high-density MEAs are low-noise readout and high-spatial resolution. It is not feasible to have ultra-low-noise readout circuits designed for each of the thousands of electrodes, given the area constraints. Sometimes, it is not essential to record from every single electrode because only a few electrodes provide most of the relevant information. So, less number of ultra-low noise readout channels can be implemented in the area outside the electrode array, and the space below the electrode array can be used for implementing the switches needed for the interconnection of the selected electrode with the readout channel, as shown in the figure 2.4 and local memory that can set the state of the electrode.

In this SM architecture, the number of electrodes can be much higher than the number of channels as only a set of electrodes are chosen for readout, which allows the implementation of MEAs with high spatial resolution. The electrodes are initially scanned in successive recordings to identify the electrodes that will be used for continuous readout during the experiment protocol. The area available to implement the amplifiers is large since they are placed outside the electrode array, allowing the implementation of low-noise large amplifiers. The reduced flicker noise due to the large transistors used in the realization of amplifiers results in increased SNR. Several MEAs that have been implemented using the SM architecture over the last decade are summarized in table 2.1.

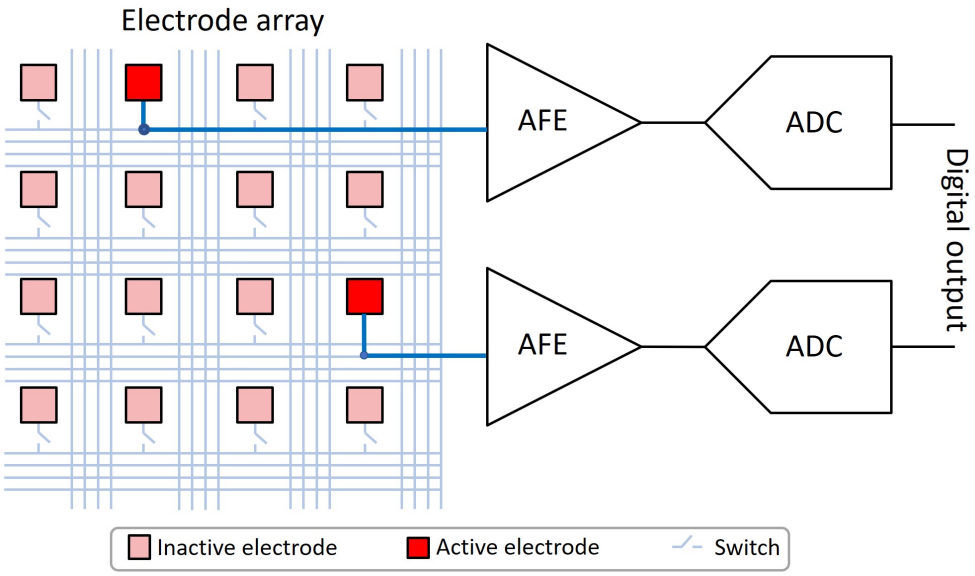


Figure 2.4: Switch matrix block diagram showing the reduced and interesting subset of the array (red = electrodes of interest, pink = inactive electrodes). Two out of the sixteen electrodes picking up the neural signals are connected through a matrix of switches and wires to two readout channels by closing the respective switches.

Technology	No. of electrodes	No. of channels (AP)	Electrode pitch	Noise/ channel	Power/ channel	Year	Ref.
0.18 μm	455	52	35 μm	3.08 μV_{RMS}	-	2014	[31]
0.6 μm	752	32	40 μm	-	57.5 μW	2011	[32]
0.13 μm	966	276	20 μm	6.36 μV_{RMS}	49.06 μW	2017	[33]
0.6 μm	11011	126	18 μm	7 - 9 μV_{RMS}	160 μW	2010	[14]
0.13 μm	16384	1024	15 μm	7.5 μV_{RMS}	19.8 μW	2018	[34]
0.18 μm	19584	246	18 μm	3.1 μV_{RMS}	39.1 μW	2018	[35]
0.35 μm	26400	1024	17.5 μm	2.4 μV_{RMS}	45 μW	2014	[8]
0.18 μm	59760	2048	13.5 μm	2.4 μV_{RMS}	16 μW	2017	[36]

Table 2.1: Different MEAs implemented with SM architecture

Table 2.1 shows that MEAs with noise as low as 2.4 μV_{RMS} can be implemented using SM architecture [8, 14]. The noise band chosen for the 'Noise/channel' values in the table 2.1, for AP readout, is slightly different in each citation. Since the power consumption due to the readout blocks with complex hardware (AFE and ADC) is high, the power budget should be kept in mind while designing these MEAs.

2.2.2 Active pixel architecture

The APS architecture is used to obtain a full-frame readout for recording signals from all the electrodes. In the APS architecture, the AFE is included inside the pixel along with the electrode as shown in figure 2.5. The output from AFE is individually routed to the ADC in the ADC array. The limitation on the size of the pixel and power consumption results in designing front-end circuitry with small transistors. Since small transistors generate higher flicker noise, a trade-off with noise is made here for full-frame readout.

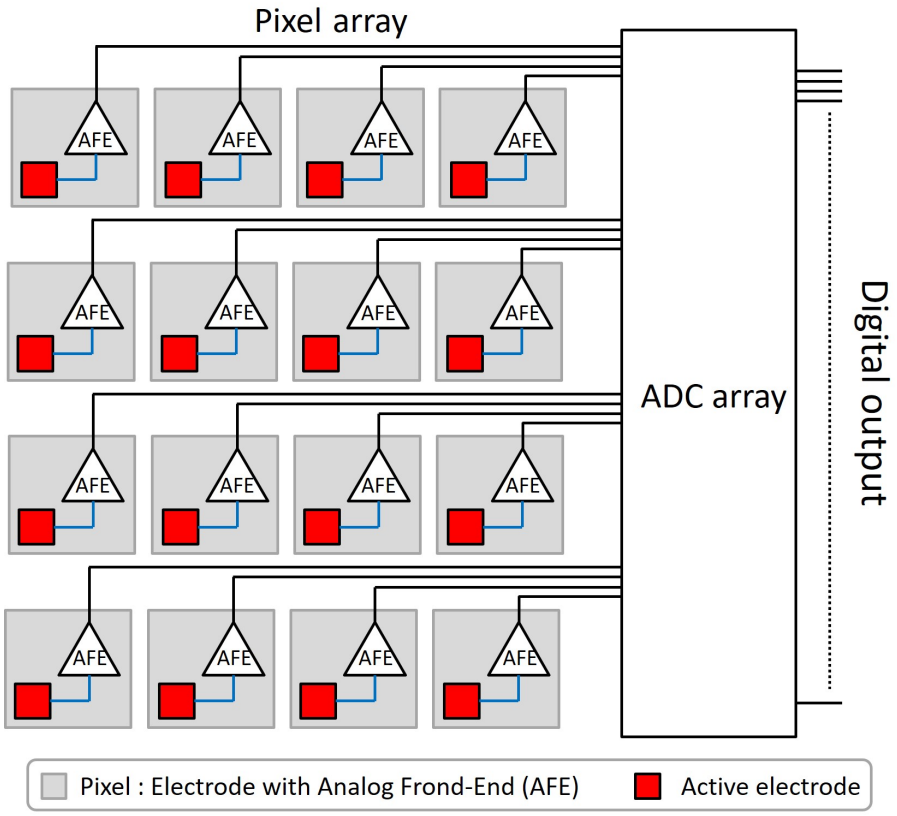


Figure 2.5: The block diagram of an APS based MEA with each pixel, including an electrode along with the AFE. The output from the AFE is routed to the ADCs depicted here as an ADC array.

Routing of the pixel to its corresponding ADC would get more complex as the number of electrodes increases. So, it is crucial to optimize the noise and the number of electrodes and channels while using APS architecture. Since the transistors used in implementing the front-end in APS MEAs are small in size, power consumption per channel is mainly dependent on ADC complexity. Some of the APS architecture based MEAs developed over the last years are shown in the table [2.2]. It can be seen that the noise obtained per channel for action potential band is higher compared to the SM MEAs, which were shown in the previous section.

Technology	No. of electrodes	Pixel pitch	Noise/ channel	Power/ channel	Year	Ref.
0.6 μm	128	250 μm	11.7 μV_{RMS}	-	2006	[37]
0.35 μm	128	200 μm	6.08 μV_{RMS}	15.5 μW	2010	[38]
0.35 μm	256	200 μm	7 μV_{RMS}	15 μW	2009	[39]
0.13 μm	384	20 μm	6.36 μV_{RMS}	49.06 μW	2017	[33]
0.18 μm	512	25 μm	20.6 μV_{RMS}	2.7 μW	2018	[40]
0.18 μm	1120	50 μm	-	12.6 μW	2013	[41]
0.35 μm	4096	42 μm	26 μV_{RMS}	-	2008	[42]
0.35 μm	4096	60 μm	21.2 μV_{RMS}	-	2013	[43]
0.18 μm	4225	16 μm	>44 μV_{RMS}	-	2014	[44]
0.5 μm	16384	17.5 μm	-	-	2011	[45]
0.18 μm	19584	18 μm	10.9 μV_{RMS}	5.9 μW	2018	[35]
0.14 μm	27684	24 μm	15.3 μV_{RMS}	-	2017	[46]
0.18 μm	65536	25.5 μm	10.02 μV_{RMS}	-	2017	[47]

Table 2.2: Different MEA designs implemented with APS architecture

2.2.3 Switch Matrix vs Active Pixel Sensor

Using SM topology, it is possible to implement MEAs with high electrode density and with high spatial resolution owing to the absence of amplification or buffering elements included in the pixel along with the electrode. For experiments needing full-frame readout and high-density recordings, APS implementation of MEAs is used. To further compare these traits, the noise and the number of readout channels in the listed architectures (2.1 and 2.2), are plotted in figure 2.6. The low-noise of the SM architecture (blue in figure 2.6) makes it perfect for spike-sorting, as it is easy to effectively detect the spike when the background noise is less than 10 μV_{RMS} [29]. This can be comprehended from the three blocks showing the amplitude of noise with respect to the spike on the left side of the graph. On the other hand, using APS MEAs can offer a higher number of parallel readout channels, providing simultaneous readout from a higher number of electrodes compared to SM MEAs.

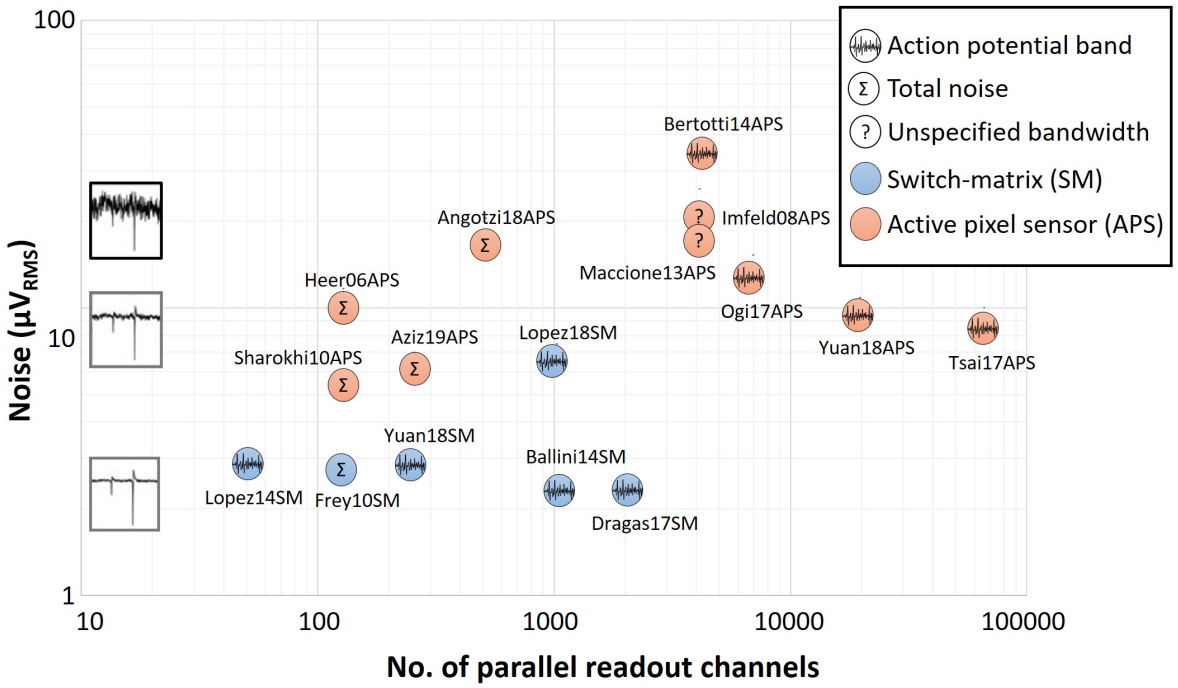


Figure 2.6: The comparison of output noise of MEAs with respect to the number of parallel readout channels. However, the noise reported for these MEAs has a slightly different choice of noise bandwidth, making this graph a rough comparison. The last name of the first author, type of readout topology and year are given next to the listed MEA. Inspired from [5].

2.3 Improvement of readout architecture for APS MEAs

For APS MEAs, the number of readout channels is relatively high, and the noise due to in-pixel circuitry deteriorates the signal quality. This calls for the need for low-noise readout strategies, which can reduce the noise caused by the readout circuitry without compromising the spatial resolution and high-density recordings (full-frame readout). In this thesis, a low-noise readout architecture designed using compact ADC will be proposed and evaluated. The designed ADC has an input stage that will be integrated into the pixel of the target MEA, making it the AFE. This readout architecture targets to bridge the gap between SM and APS readout topologies that have been discussed so far, by providing a low-noise, full-frame readout.

2.3.1 Target MEA specifications

The mentioned target specifications of MEA with respect to existing state-of-the-art SM and APS architectures (with on-chip ADCs) are shown in the table 2.3. Since thousands of electrodes are adequate for most MEA experiments, the specification for the number of parallel readout channels in target MEA has been set to approximately ten thousand. To achieve sub-cellular resolution, the pitch specification

is chosen to be nearly 17 μ m, which allows capturing the signal from the same neuron from different electrodes. For precisely capturing signals with amplitudes as low as tens of μV (iPSC neurons [6, 13]), the noise specification per channel in the AP band has been set to $< 5\ \mu V_{RMS}$. A compact low-noise ADC for APS MEAs is designed in this thesis to achieve these specifications.

	SM [36]	Target MEA	APS [35]
Technology	0.18 μm	0.18 μm	0.18 μm
Readout channels	2048	~10000	19584
Noise/channel	2.4 μV_{RMS}	$< 5\ \mu V_{RMS}$	10.9 μV_{RMS}
Pitch	13.5 μm	17 μm	18 μm
Signal bandwidth	1 Hz - 10 kHz	300 Hz - 7 kHz	300 Hz - 5 kHz
Power	16 μW	5 μW	5.9 μW
Output data rate	40.96 Mbps	~10 Gbps	2.4 Gbps

Table 2.3: Target MEA specification in comparison with the existing state-of-the-art SM [36] and APS [35] MEAs

Most reported MEAs typically use the AFE implemented using multiple gain stages to provide high amplification before digitizing the signal. The amplified signal is then digitized, typically using SAR ADCs with good resolution. This might not be a problem for SM MEAs where the AFE and ADC are entirely outside the sensing area, and given the reduced number of readout channels, it is practical to implement these readout blocks with low-noise performance. However, due to the size constraints in APS MEAs, the amplifiers and filters are implemented using small transistors, increasing the noise in the readout channel. Moreover, it is not practical to implement thousands of SAR ADCs (which are typically being used for MEAs) outside the pixel array, forcing the designer towards multiplexing options, which again requires additional circuitry in the pixel. Although SAR ADCs are primarily being used for MEAs [31, 33, 35, 36], the design of low-noise SAR ADC demands complicated circuit blocks increasing the area consumption.

Due to these limitations, in this thesis, an oscillator based sigma-delta ($\Sigma\Delta$) ADC has been used for the action potential readout in MEAs. $\Sigma\Delta$ ADC trades-off bandwidth for low-noise, which makes it an excellent choice for low-bandwidth applications. The signal-bandwidth of the neuronal signals such as extracellular AP is below 7 kHz [8]. This makes $\Sigma\Delta$ ADCs have an edge over SAR ADCs for digitizing low-frequency signals. $\Sigma\Delta$ ADCs can provide high precision resulting in low quantization noise in the signal band because of their oversampling and noise shaping properties. To further corroborate the choice of $\Sigma\Delta$ ADCs for MEAs, similar applications that benefited from this ADC are discussed here to show the performance attributes in terms of area and power for low-bandwidth applications. A new approach that has been chosen for implementing a compact low-noise $\Sigma\Delta$ ADC will then be introduced

and explained in detail in the next chapters.

2.3.2 ΣΔ ADCs for MEAs

ΣΔ modulators have gained popularity in the implementation of biomedical electronics such as wearable and implantable devices and bio-acquisition systems. Several ultra-low-power ΣΔ based ADCs with high accuracy and large dynamic range have been implemented in [48–52]. This ultra-low-power (μW range) operation of the ADCs ensures the long battery life in the case of implantable and portable devices, and this could be especially beneficial in MEA applications targetting a large number of readout channels. The operational amplifiers, usually used to implement the integrator block in the ΣΔ modulators, are the most power-consuming blocks in the ADC. To optimize the power consumption to a range of nanowatts, large scale neural recording implants have implemented ADCs with passive integrators to integrate the error signal [53]. These are only some of the many design variants and choices made in ΣΔ ADCs based on the specific bio-acquisition application.

ΣΔ ADCs are being widely used in active neural probes which are in-vivo MEAs used for deep brain recordings [54, 55]. Active neural probes imply including the signal conditioning circuitry on the probe shaft to reduce parasitics due to routing from the electrode to readout electronics, and increase the signal quality. Hence, the design of high-density active neural probes is highly limited by the available area on the probe shaft for the electronic integration. Low noise and low power ΣΔ ADCs that can be integrated along the neural shaft to avoid routing of sensitive input bio-signal, would improve the readout quality of the signal. Neural probe with a pitch of 60 μm accommodating in-pixel digitization using ΣΔ ADC has been reported [55] showing the promising future of ΣΔ ADCs for MEA applications.

Another interesting application of the ΣΔ ADCs is in CMOS image sensors. Pixel-level data conversion [56–59] where the ΣΔ ADC is in-built in the pixel itself shows the scope of using in-pixel ΣΔ modulators in DPS based MEAs which are functionally similar to these CMOS based image sensors. However, this would be a trade-off with achieving a high spatial resolution that the designer has to make, which again depends on the type of experiments and biological signal that is at the interest of acquiring.

The quantization noise in ΣΔ ADCs decreases with higher-order noise shaping, which will be explained in chapter 3. However, the hardware complexity of the ΣΔ ADCs increases with the order of noise shaping. Since a compact ADC with minimum hardware complexity is ideal for implementing thousands of readout channels, a time-encoding approach has been chosen to implement the proposed ADC. The theory behind oversampling, noise-shaping, and time-encoding will be discussed in the next chapter to explain and support the design choice made for the readout architecture for target APS MEAs.

2.4 Conclusion

In this chapter, the different MEA terminologies and the signal flow in an MEA system have been introduced. The different readout architectures used to implement the in-vitro MEAs have been stated, focusing on the widely used SM and APS architectures. Their advantages, limitations, and trade-offs have been compared after which, the goal of the thesis has been introduced. The thesis targets to design a low-noise readout for APS MEAs. The candidature of ΣΔ ADCs for MEAs has been spotlighted and its promising application has been validated by different examples which benefited from ΣΔ ADCs. The theory behind the ΣΔ ADCs and the time-encoding approach chosen to optimize the quantization noise in the ΣΔ ADCs will be explained in the next chapter.

3 Time encoding ΣΔ ADCs

3.1 Introduction

Most electronic devices deal with both analog and digital signals. Although the real-world signals are analog, analog signals are neither robust to noise nor efficient and versatile for signal processing. Digital signals, on the other hand, are very resilient to noise and easily understandable and manipulable by the microprocessors and the signal processing circuitry. So, the analog-to-digital conversion is very crucial in data acquisition systems. The analog-to-digital conversion takes place in two steps: 'sampling' and 'quantization.' The discretization of the analog signal in the time domain is called sampling, and the discretization of the amplitude range is called quantization. During sampling, the continuous-time signal is converted to a discrete-time signal. Quantization is the process where the analog signal is discretized into a finite set of values. Figure 3.1 illustrates the concepts of sampling and quantization steps. The two factors that determine the accuracy of the analog-to-digital conversion, resolution, and sampling rate, will be briefed.

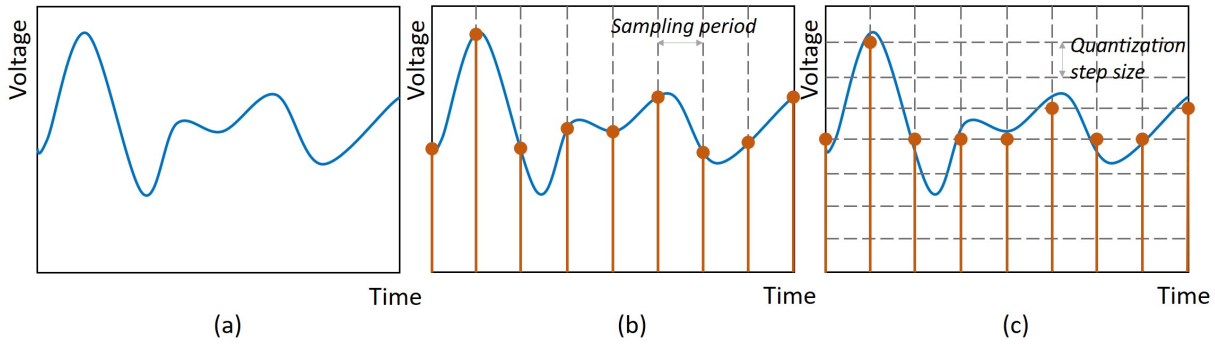


Figure 3.1: Illustration of sampling and quantization steps during analog to digital conversion of signal (a) Input signal (b) Sampling and (c) Quantization

3.1.1 Sampling

The sampling rate is given by how fast the analog signal is sampled by the rising or falling edge of the clock. The Nyquist-Shannon theorem gives the sampling condition for the accurate reconstruction of the digitized signal without an error.

3.1.1.1 Nyquist-Shannon sampling theorem

The Nyquist-Shannon theorem states that the signal should be sampled at a rate of at least twice the highest frequency component of the signal for its accurate reconstruction (figure 3.2b,c). If f_0 is the highest frequency value in the input signal which is also the signal bandwidth, then the sampling rate should be, $f_s > 2f_0$. During sampling, the signal band spectrum can be overlapped by its periodic mirrored replicas (alias) when the signal is sampled at a frequency less than $2f_0$, as shown in the figure 3.2d, resulting in artifacts (aliasing). An anti-aliasing filter (AAF) that is a low-pass filter is used to restrict the signal bandwidth before sampling, to satisfy the Nyquist criterion.

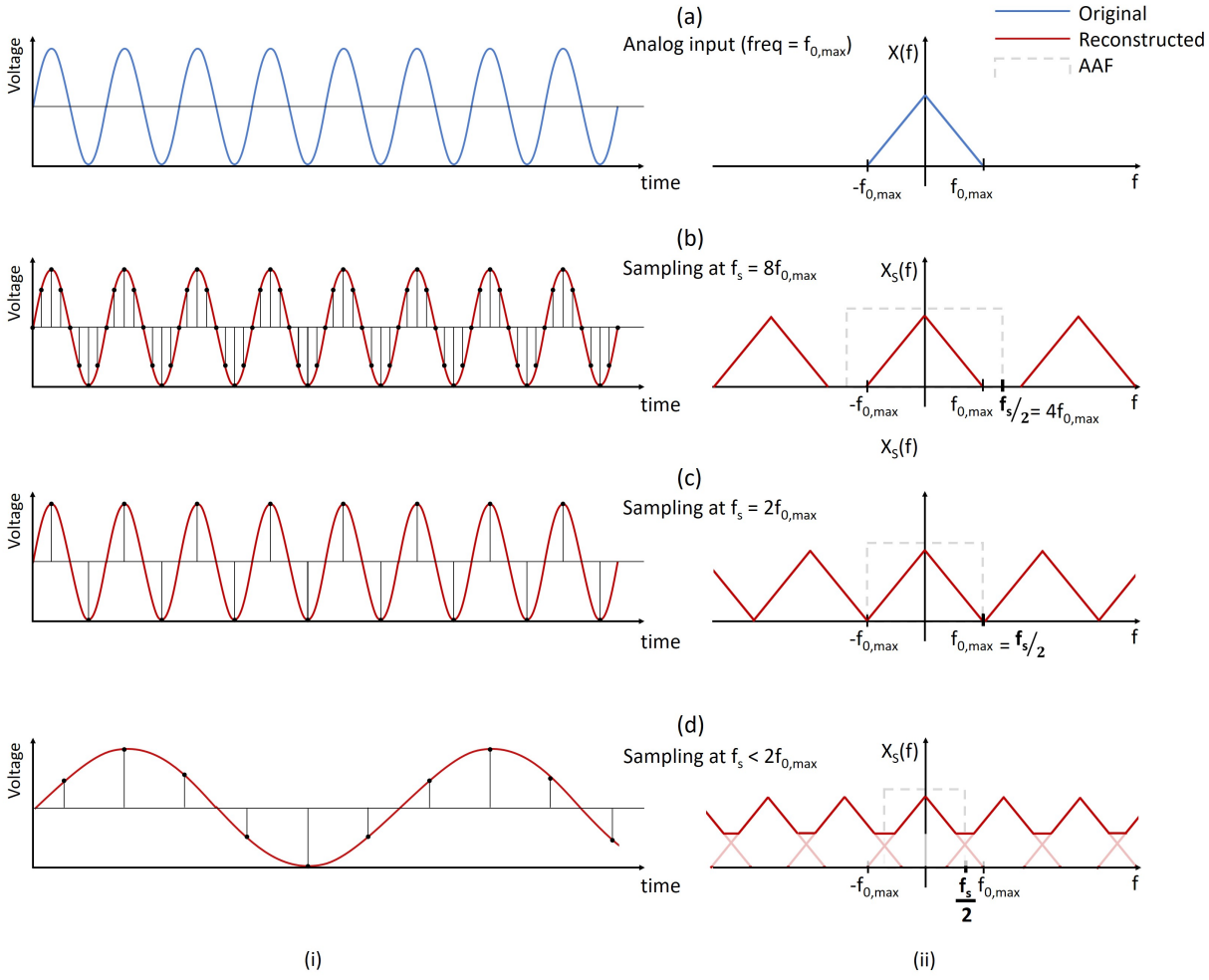


Figure 3.2: Example for Nyquist theorem showing reconstruction of sampled signal at f_s in (i) time-domain and (ii) frequency domain (double-sided spectrum). (a) Input signal with frequency $f_{o,max}$, where $f_{o,max}$ is the signal bandwidth. (b) Signal sampled at a frequency ($f_s = 8f_{o,max}$ showing relaxed anti-aliasing filter requirements (dotted lines). (c) Signal sampled at Nyquist frequency with AAF designed to remove out-of-band spectra. (d) Signal sampled at frequency less than Nyquist resulting in inaccurate reconstruction due to 'aliasing'.

Designing an AAF is quite challenging as it trades-off between the bandwidth and aliasing,

meaning that either some aliasing is still present or some frequencies in the bandwidth close to the Nyquist limit are attenuated. One of the advantages of sampling at very high frequencies (oversampling) is that the design requirements for AAF are rather relaxed since the replicas are far away from the signal band.

3.1.2 Quantization

The sampled signal can be reconstructed under suitable conditions, as previously discussed. However, quantization replaces each analog value with a value from the set of discrete values, making it irreversible with loss of information (quantization error). The value of this quantization error depends on the number of discrete quantization levels and can be modeled as an additive random signal called quantization noise because of its stochastic behavior. When the quantizer uses a higher number of quantization levels, the quantization noise reduces, resulting in better resolution. This is demonstrated in figure 3.3, where the analog signal is quantized by a 2- and 3-bit quantizer. It can be seen that the 3-bit resolution offers a closer resemblance of the digitized signal with the analog signal compared to the 2-bit resolution.

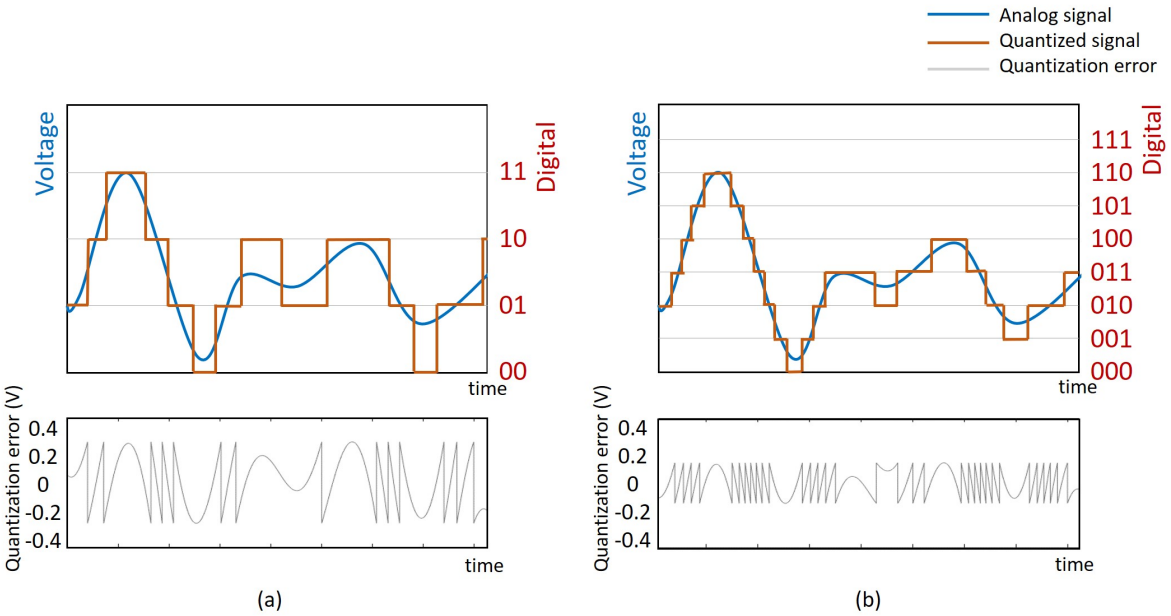


Figure 3.3: (a) Quantization with 2-bit and (b) 3-bit resolutions

The performance of an ADC is characterized by the signal-to-quantization noise ratio (SQNR) and the bandwidth. The SQNR of the ADC is affected by the quantization error while the sampling rate characterizes the bandwidth. For a Nyquist data converter, the maximum SQNR (at "full-scale") obtained for the sine input (see Appendix section A.1) is given by,

$$SQNR_{\max} = 6.02N + 1.76dB$$

where N is the resolution of the ADC, given by the number of quantizer bits. One way to improve the SQNR is by increasing the number of resolution bits, which increases the hardware complexity of the design. For the target APS MEA, we want to keep the hardware complexity minimum, to have thousands of parallel readout channels. To improve the SQNR of the ADC for the same number of quantizer bits, oversampling and noise shaping techniques can be used, which will be discussed next.

3.2 Oversampling data converters

Oversampling data converters are mainly used for implementing applications where high resolution is needed. The sampling frequency in oversampling data converters (f_S) is much higher compared to the traditional Nyquist data converters ($f_N = 2f_0$). The quantization noise is spread over a wide frequency range, as shown in figure 3.4, and out-of-band noise is filtered using a digital filter during post-processing. Oversampling converters relax the complexity of analog circuitry while adding extra bits of resolution, at the cost of increased digital circuit complexity. It is easier to implement complex digital circuitry in less area in deep sub-micron CMOS technology nodes compared to high-resolution analog circuitry, which is limited by low voltage supply and short-channel effects. The SQNR of an oversampled data converter for a sine input (see Appendix section A.2) is given by,

$$SQNR_{\max} = 6.02N + 1.76 + 10log_{10}(OSR)$$

where OSR is the oversampling ratio given by f_S/f_N.

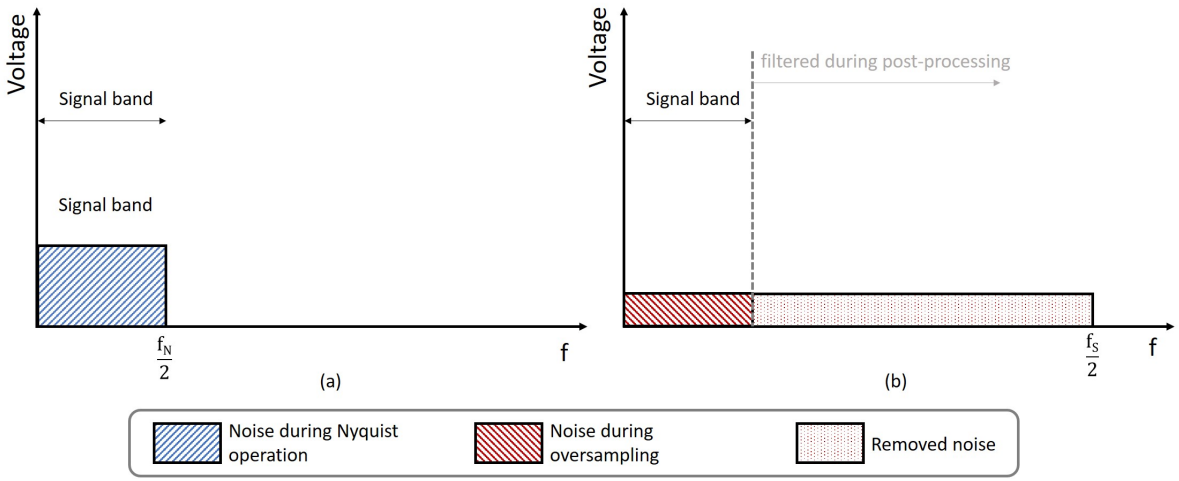


Figure 3.4: Comparison of the quantization noise present in a (a) nyquist data converter and a (b) oversampled data converter

Comparing the SQNR with and without oversampling, it can be seen that there is an improvement in SQNR by a value of $10\log_{10}(\text{OSR})$ when a signal is oversampled at OSR times the Nyquist rate. This enhancement also takes place for other types of noise like the thermal noise in circuits, improving the overall SNR by $10\log_{10}(\text{OSR})$ [60].

3.2.1 Sigma-delta data converters

Although oversampling increases the SQNR, the linearity is not improved [60]. Since a 1-bit DAC has only two output values, which can be defined by a straight line, it is inherently linear [60]. Using the 1-bit DAC to provide negative feedback, we can further improve the SQNR by spectral shaping the quantization noise (noise shaping). The noise shaping applied to oversampled signals is also referred to as sigma-delta modulation.

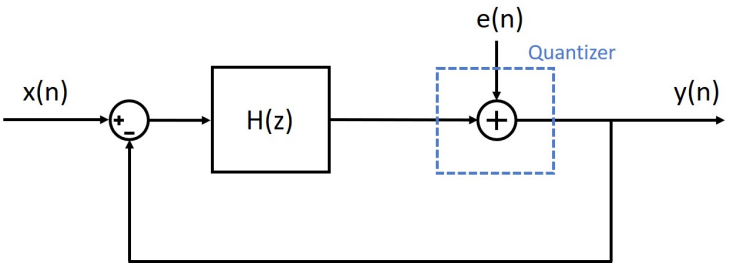


Figure 3.5: Linear model of ΣΔ data converter

Figure 3.5 shows the linear model of the block diagram of a simple ΣΔ where H(z) is the transfer function of the loop-filter. The input (x(n)) and error signals (e(n)) are assumed to be independent from each other while calculating the the transfer function of the output which can be expressed as,

$$Y(z) = S(z)X(z) + N(z)E(z)$$

where S(z) and N(z) are the signal and noise transfer functions respectively, which in this case are,

$$S(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \qquad N(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}$$

It can be seen from the above equations that the poles of H(z) are the same as the zeroes of N(z), meaning that N(z) approaches zero when H(z) approaches infinity. When H(z) is chosen such that its magnitude is large in the band of interest, the signal transfer function approaches unity while the noise transfer function will be minimized [60]. This is how the noise is shaped by being pushed

towards higher frequencies, thereby reducing quantization noise in the signal band. The high-frequency quantization noise outside the signal band is filtered during post-processing using a digital filter.

3.2.1.1 First order ΣΔ modulator

We want to high-pass filter the quantization noise for which N(z) should be zero when H(z) reaches infinity since the poles of H(z) are the same as the zeros of N(z). For a first-order function having a pole at say z = 1, H(z) will be 1/(z-1), making the loop filter an integrator.

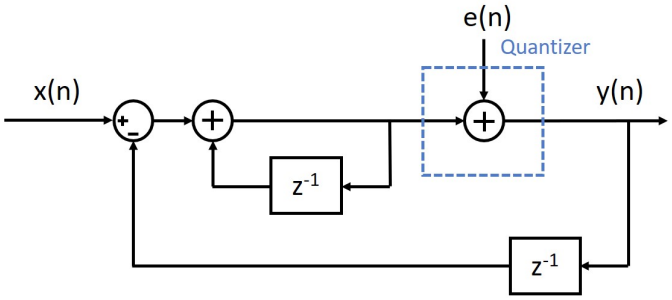


Figure 3.6: Linear model of a first order ΣΔ data converter

The block diagram of the first-order ΣΔ modulator is shown in the figure 3.6 from which the output transfer function can be calculated as,

$$Y(z) = E(z) + (X(z) - z^{-1}Y(z))\left(\frac{1}{1 - z^{-1}}\right)$$

$$Y(z) = X(z) + E(z)(1 - z^{-1})$$

showing N(z) as a high-pass filter. The $SQNR_{max}$ of a first order ΣΔ modulator (see section A.3) can be calculated to be,

$$SQNR_{\max} = 6.02N + 1.76 - 5.17 + 30log_{10}(OSR)$$

which shows that the SQNR of a first-order ΣΔ modulator is much higher than the SQNR of Nyquist and oversampled (without noise shaping) ADCs. The SQNR value can be further increased by increasing the order of the ΣΔ converter.

3.2.1.2 Second order ΣΔ modulator

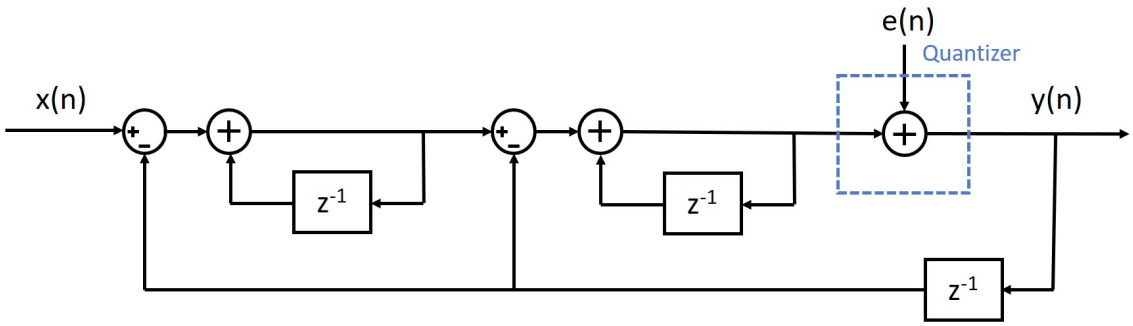


Figure 3.7: Linear model of a second order ΣΔ data converter

The block diagram of a second order ΣΔ modulator obtained by replacing the quantizer in first order ΣΔ modulator by the modulator itself, is shown in the figure A.5. The transfer function for this system can be calculated as,

$$Y(z) = E(z) + \left((X(z) - z^{-1}Y(z))\left(\frac{1}{1-z^{-1}}\right) - z^{-1}Y(z)\right)\left(\frac{1}{1-z^{-1}}\right)$$

$$(1-z^{-1})^2 Y(z) = (1-z^{-1})^2 E(z) + (X(z) - z^{-1}Y(z)) - (1-z^{-1})z^{-1}Y(z)$$

$$Y(z) = (1-z^{-1})^2 E(z) + X(z)$$

showing that while the system transfer remains the same, the noise transfer shows a second-order high-pass filtering. Calculating the $SQNR_{max}$ for a second-order ΣΔ modulator (see section A.4) we get,

$$SQNR_{\max} = 6.02N + 1.76 - 12.9 + 50log_{10}(OSR)$$

showing the improvement in SQNR due to the increase in the order of the ΣΔ modulation. Table 3.1 summarizes the $SQNR_{max}$ comparison among the different types of ADCs that have been explained so far.

Type of ADC	$SQNR_{max}$ (in dB)
Nyquist	6.02N+1.76
Oversampled	6.02N+1.76+10log$_{10}$(OSR)
1st order ΣΔ	6.02N+1.76-5.17+30log$_{10}$(OSR)
2nd order ΣΔ	6.02N+1.76-12.9+50log$_{10}$(OSR)

Table 3.1: Calculated $SQNR_{max}$ of different ADCs

The noise transfer functions for oversampled ADCs without noise shaping and with first and second-order noise shaping are compared in the figure 3.8. It can be seen that the magnitude of noise in signal-band (0 to f_0) decreases with higher-order ΣΔ modulators. The slope of the noise shaping is 20 dB/decade for a first-order ΣΔ modulator and 40 dB/decade for a second-order ΣΔ modulator. Higher-order ΣΔ modulators (m > 2) increase the SQNR further. Although these are possible to construct using different feedback and feed-forward connections, they cannot be made by just adding further stages, as shown in the case of the second-order modulator because of the system instability caused due to phase turn by more than two integrators [60].

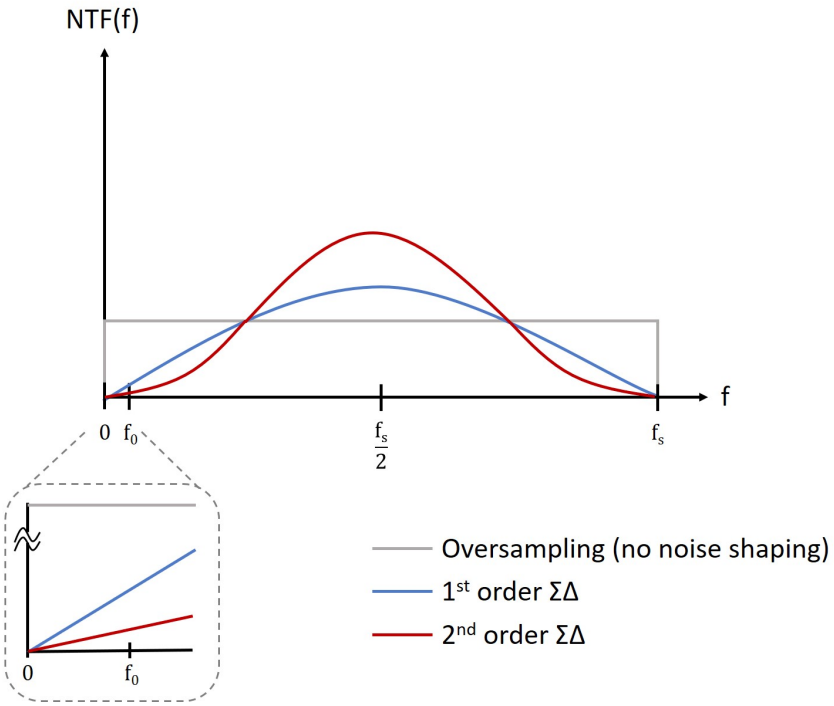


Figure 3.8: Noise shaping in oversampled ADCs

ΣΔ modulators can either be implemented using discrete time(DT) [48, 49] approach or continuous time(CT) [50–52] approach which are illustrated in figure 3.9. DTΣΔ converters are typically implemented using switched capacitors and require operational amplifiers increasing the power consumption of the system [61]. The lack of switching elements in CTΣΔ modulators reduces the power consumption but there could be problems increased sensitivity to clock jitter [18, 62]. This however is not a problem in MEA applications, since MEA is a lab instrument and stable off-chip clock generators can be used. Also, unlike in the DTΣΔ converters, the sampling is done after the loop filter (H(z)) in CTΣΔ converters which eliminates the need to include a dedicated anti-aliasing filter in the system as the filter acts as one [63].

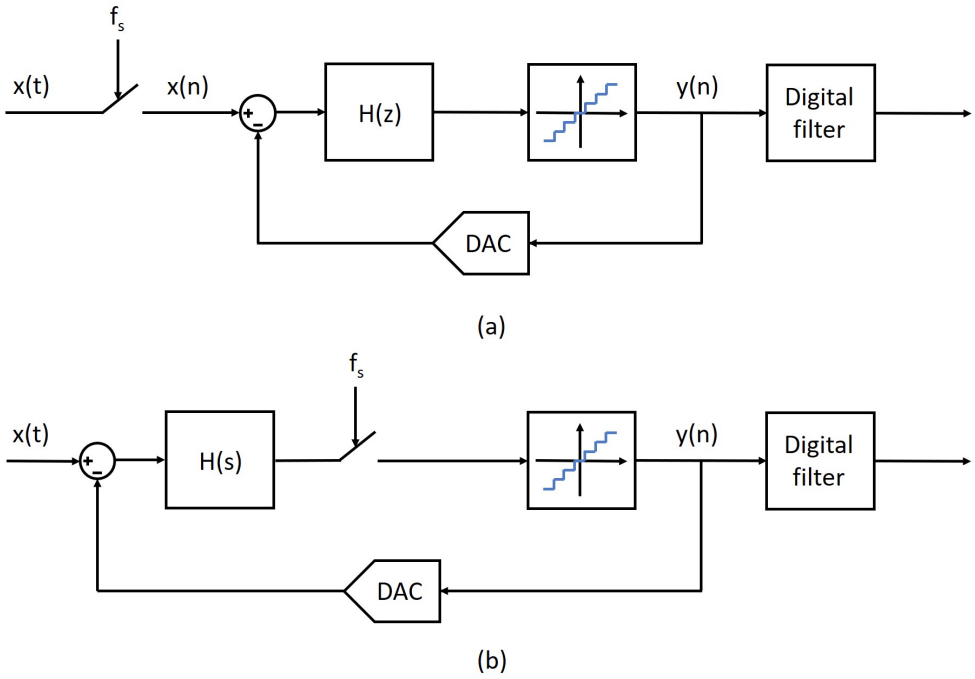


Figure 3.9: Block diagram of (a) discrete-time and (b) continuous-time ΣΔ

However, relatively fewer higher order CTΣΔ modulators have been reported so far compared to the higher-order DTΣΔ modulators that are implemented for bio-acquisition due to the increased complexity in designing the loop filter and digital filter in CTΣΔ ADCs [51]. Time encoding of the signals can be used for implementing higher order CTΣΔ to overcome these limitations [17–19, 21].

3.3 Time encoding ADCs

CMOS process scaling reduces the performance of analog circuitry as the transistor gains and available voltage headroom are reduced, and several non-idealities such as short channel effect, gate leakage, and dopant fluctuation kick-in. Digital circuits, on the other hand, greatly benefit from technology scaling, and the fast switching of the small transistors offers excellent temporal accuracy. Taking advantage of this, we can encode the analog signals into time-domain signals such as frequency, delay, or duty cycle and handle this temporal signal using digital circuitry [17–19, 21]. The time-encoding data converter, which encodes the input signal into the frequency of a carrier signal to implement a compact low-noise ADC, is the focus of this thesis.

The block diagram of a frequency encoding based data converter is shown in figure 3.10a. The frequency encoder generates an oscillation whose frequency depends on the input signal, for example, voltage or current. Considering a voltage input, a voltage-controlled oscillator (VCO) oscillates with a frequency dependent on the voltage, acting as a frequency encoder. The frequency output is converted

into a digital signal (Y in figure 3.10) by using a frequency to digital converter (F2D) that can be implemented using a counter, sampler, and a first difference. The VCO block converts the voltage to frequency, and the counter value increases by a single unit for each rising edge of the oscillation. The digital signal will have the total number of 1's that are counted by the counter in a clock period set by the sampler (figure 3.10c). The first difference resets the value of the counter after each clock period. The VCO frequency should be designed such that it remains less than half the sampling frequency (clk) [17] to make sure all the rising edges are detected.

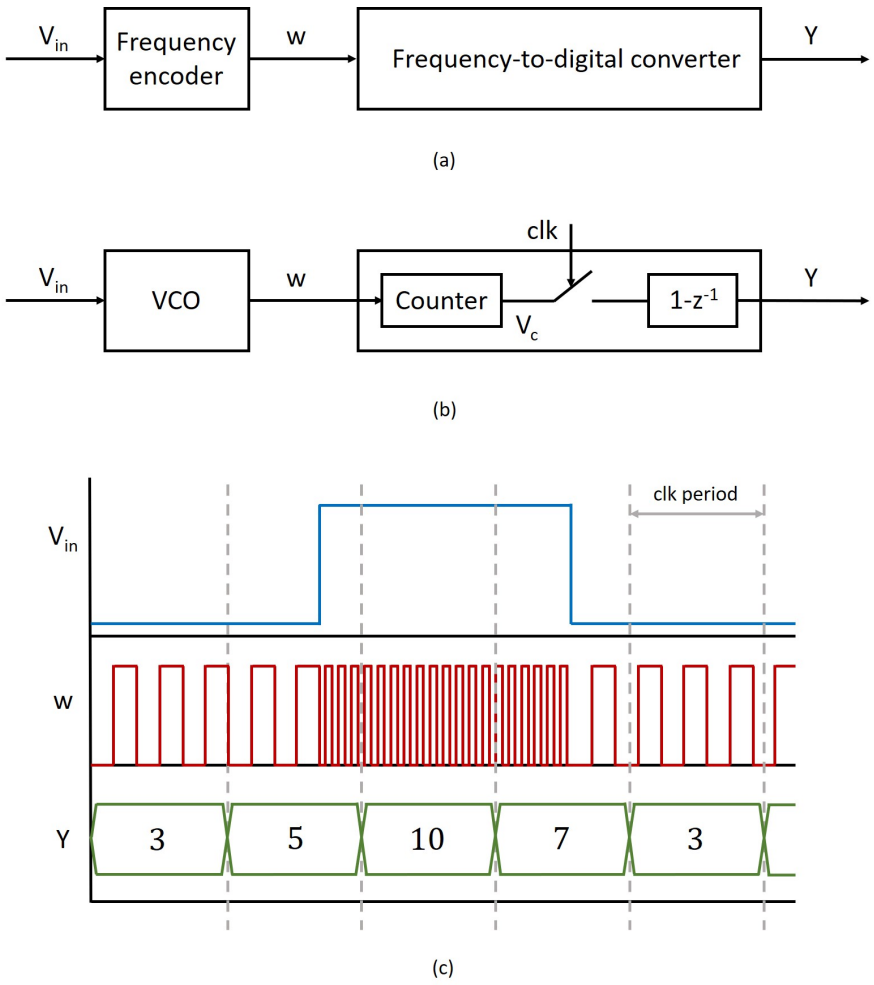


Figure 3.10: (a) Block diagram of an ADC based on frequency encoding (b) Simplified block diagram of a VCO based ADC (c) Illustration of the frequency encoding process

The VCO can be seen as a phase integrator with a gain of K_{VCO} with an oscillation frequency depending on the input voltage ($f(t) = K_{VCO} \times V_{in}(t)$). The simplified linear model of the VCO quantizer [17] takes into consideration two non-idealities: VCO phase noise and quantization noise. The VCO phase noise occurs due to the fluctuations in the phase (or frequency) caused by electronic perturbations such as flicker and thermal noise. For the linear model, the phase noise is considered to

have -20 dB/decade, which in reality is steeper for frequencies where flicker noise dominates, and for very high frequencies where there is noise floor (0 dB/decade) [64, 65] (see Appendix B).

The quantization noise occurs due to the finite sampling frequency, limiting the time resolution of the F2D [17, 18]. This quantization noise is modeled as white noise in this case, similar to the quantization noise considered in the previous ADC models. The errors due to phase noise and quantization noise are high pass filtered by the first-order difference, which shapes the quantization noise to high frequencies providing first-order noise shaping [17]. This shows that the VCO itself acts as a first-order ΣΔ modulator without a feedback loop [66].

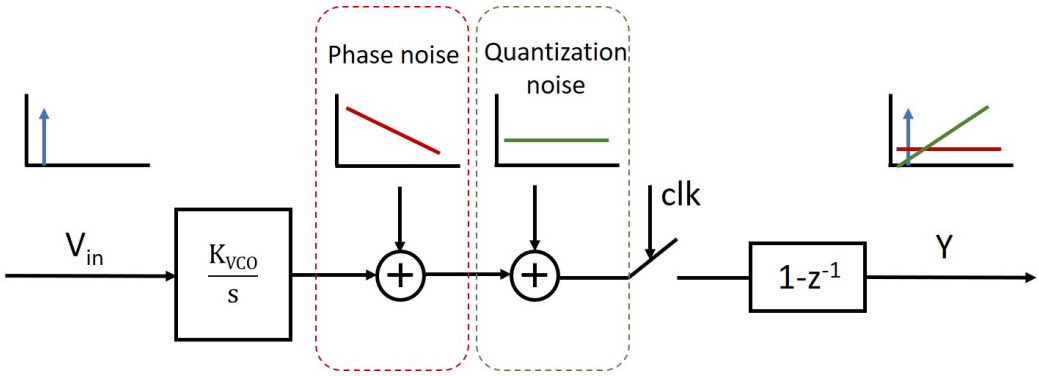


Figure 3.11: Linear model of VCO based ADC [17]

The VCO based quantizer model, shown in figure 3.10b, has been implemented in Simulink for a quick evaluation of its behavior. The center frequency and sensitivity of the VCO are set to 100 kHz and 10 MHz/V, respectively. The PSD obtained for a sinusoidal input with 0.1 V amplitude and 1 kHz frequency, and a clock frequency of 1 MHz shows a noise shaping with a slope of 20 dB/decade, explaining the first-order noise shaping in a VCO quantizer model.

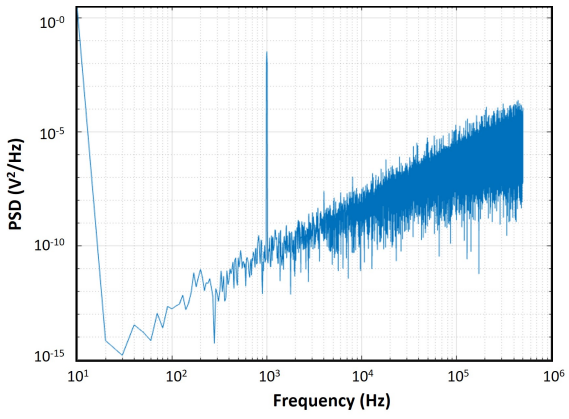


Figure 3.12: PSD obtained from the VCO quantizer model

The $SQNR_{max}$ of the first order oscillator based ΣΔ ADC ADC, where $V_{in,FS}$ is the input

magnitude at full-scale, can be approximately estimated [22] to be,

$$SQNR_{\max} = 20log\left(\frac{2K_{\mathrm{VCO}}V_{\mathrm{in,FS}}}{f_{\mathrm{s}}}\right) + 1.76 - 5.17 + 30log_{10}(OSR)$$

showing that the VCO quantizer can improve the SQNR of the ADC [18]. VCO based quantizer can be used within a continuous-time sigma-delta ADC to provide higher-order noise shaping instead of increased feedback loops [17, 67]. Figure 3.13 shows the VCO based ΣΔ ADC where the first-order noise shaping of the quantizer is added to the noise shaping achieved from the closed-loop filtering, which will be designed in the next chapter.

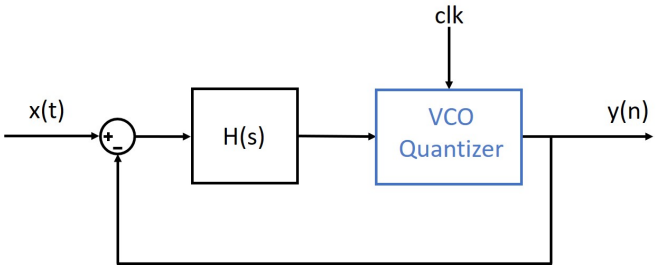


Figure 3.13: Block diagram of VCO based ΣΔ ADC

3.4 Conclusion

In this chapter, analog-to-digital conversion and the theory behind the performance of over-sampled data converters have been discussed. The contribution of oversampling and noise-shaping for reduced noise in the signal bandwidth has been explained. To further improve the performance of the ΣΔ ADCs without exerting hardware complexity, a time-encoding approach has been introduced and explained. The next chapter focuses on translating this theory into a system-level implementation of a VCO based ΣΔ ADC, which is targeted to provide second-order noise-shaping for optimum quantization noise.

4 System-level design of VCO based ΣΔ ADC

4.1 Introduction

The VCO based ADC designed in this thesis is a proof of concept to show the low-noise readout, that in future can be implemented for an MEA with target specifications shown in table 2.3. So, the designed ADC is implemented in a test chip and taped-out to evaluate the performance of the readout system that could be used in an APS MEA. The specifications for the ADC implemented for MEA readout are given in table 4.1. A reasonable range for the input signal has been chosen between ± 2 mV, which covers the signals in most of the experiments [4]. The frequency bandwidth of the neuronal action potential is chosen as 300 Hz to 7 kHz [8] while reporting the noise performance.

The maximum total noise is targeted at 5 μV_{RMS} to allow the readout of signals with tens of μVolts. The specification for the quantization noise has been set to 1.5 μV_{RMS} to leave enough noise margin for thermal and flicker noises, which will arise from the circuit implementation of the readout channel. The specifications for the SQNR and ENOB of the ADC have been evaluated from the full-scale and quantization noise specifications. The specification for maximum power consumption per channel is set to 5 μW [68], to ensure the safety of the biological sample during experiments.

Parameter	Specification
Input signal range	±2 mV
Signal band	300 Hz - 7 kHz
Total noise	5 μV_{RMS}
Quantization noise	1.5 μV_{RMS}
$SQNR_{max}$	60 dB
ENOB	10-bit
Supply	1.8 V
Power	5 μW

Table 4.1: Target readout channel specifications

4.2 Implementation of ADC

4.2.1 First order ΣΔ ADC

To see how far the noise obtained from first-order noise shaping is, with respect to the quantization noise specification, a first-order ΣΔ ADC has been designed as the first step. The block diagram of the implemented first order ΣΔ ADC with 1-bit quantizer is shown in figure 4.1. The DAC gain is chosen as 2 mV (full-scale), and the integrator gain as 10^6. Dithering has been used, by adding a random noise source before the quantizer, to randomize and spread the quantization error, modeling the quantization noise as white noise [69]. The clock frequency is chosen to be 1 MHz for achieving a high SNR due to the oversampling ratio.

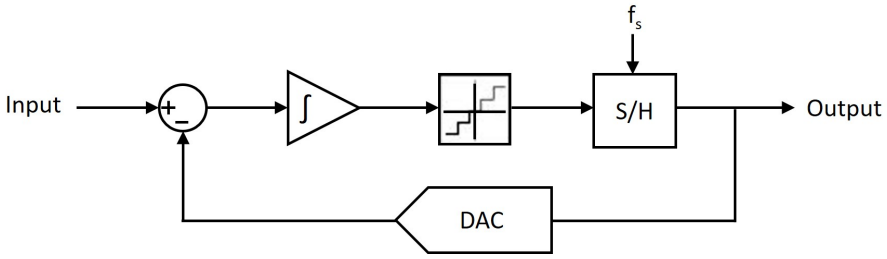


Figure 4.1: Block diagram of first order ΣΔ modulator

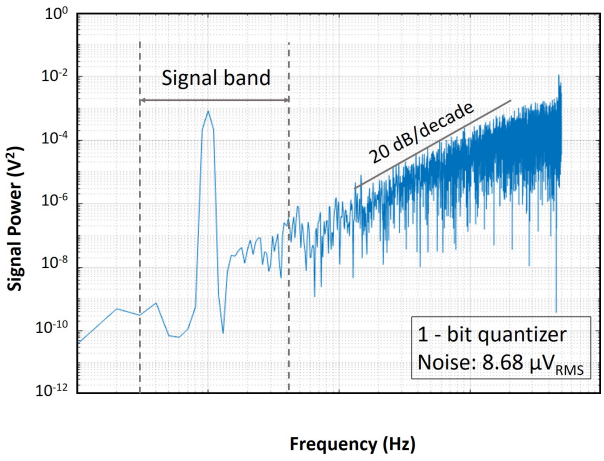


Figure 4.2: PSD of first order ΣΔ ADC yielding an SQNR_{max} of 47 dB.

The PSD obtained for a sinusoidal input with 100 μV amplitude and 1 kHz frequency is given in the figure 4.2, showing 20 dB/decade noise shaping. A noise of 8.68 μV_{RMS} was obtained with a first-order ΣΔ ADC using a 1-bit quantizer. This first-order noise shaping yields an SQNR_{max} of 47 dB, which would only meet the SQNR_{max} requirement for a 3-bit quantizer (6.02 dB increment for each additional bit). To implement multi-bit quantizers would mean increased circuit complexity, which we

want to avoid by using a VCO quantizer instead.

4.2.2 Oscillator based ΣΔ ADC

To reduce the ADC noise, the quantizer in the first order ΣΔ ADC has been replaced with a VCO based quantizer to achieve second-order noise shaping. The block diagram of this design is illustrated in figure 4.3, which has been realized using an integrator, a VCO based quantizer, and a 1-bit DAC.

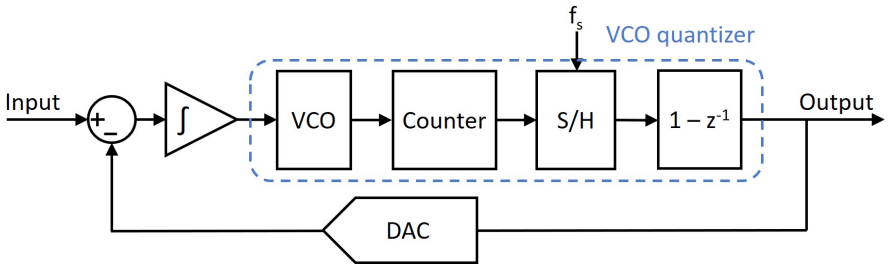


Figure 4.3: Block diagram of VCO based ΣΔ modulator

An input stage has been added after the input signal (figure 4.4), representing the AFE in the APS MEAs. The input stage can be implemented by a transconductor that injects the sum of DC current ($I_{b,IS}$) and current due to input voltage (G_{IS}*Input) as shown in figure 4.4. The feedback DAC gives two different currents, greater or lesser than the input stage current, depending on the ADC output, which is 1 or 0.

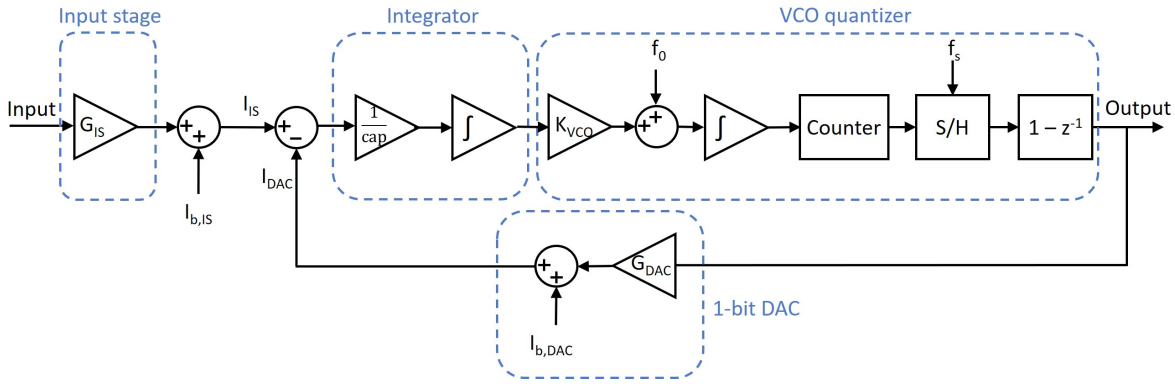


Figure 4.4: System-level implementation of the ADC

For the readout channel in the test chip, we want to test the ADC behavior for four different bias currents, since we have a power budget of 5 μ W. To test low-power operation, 200 nA and 400 nA bias currents have been chosen. However, lower currents could result in higher thermal noise. To find the optimum noise performance of the ADC, bias currents 800 nA and 1.2 μA have been chosen. In the system-level design, all the explanation is done for a nominal case of 200 nA, but table 4.2 demonstrates

the different values for different bias currents for which the given explanation and results hold true.

The value of G_{IS} has been chosen based on the g_m/I_d factor [70]. Since we want to design a low-power transconductor, a g_m/I_d of 20 has been chosen as a reasonable maximum limit for weak-inversion operation, resulting in a G_{IS} of 4 $\mu\Omega^{-1}$. This decision has been corroborated by the simultaneous circuit-level implementation of the input stage. The full-scale of the ADC is limited by the relation between the feedback current and transconductor current. The ADC will be saturated if the feedback current cannot compensate the current from the input stage. If the readout channel input approaches its maximum limits (±2 mV), the ADC system may not be stable because of non-idealities [71, 72], increasing the in-band quantization noise. To reduce this, the full-scale of the DAC has been designed to be ±5 mV after iterative simulations. For a full-scale input of ±2mV, the I_{IS} will be varying between ±8 nA. I_{DAC} should be increased by ±20 (8*5/2), giving a value of 40 nA for G_{DAC} and 180 nA for $I_{b,DAC}$.

The value of G_{IS}*K_{VCO}/cap plays a critical role while optimizing the quantization noise because of its direct relation to the signal transfer. The values of capacitor and K_{VCO} are chosen such that the quantization noise obtained for G_{IS}*K_{VCO}/cap product is minimum. Figure 4.5 shows the variation of the quantization noise with respect to G_{IS}*K_{VCO}/cap for a signal amplitude of 100 μV. The plot shows that the quantization noise is minimum for the G_{IS}*K_{VCO}/cap ratio of 5.37 x 10^{13}. The value of K_{VCO} is fixed for all bias currents, as it is the gain of the VCO. So, to maintain the G_{IS}*K_{VCO}/cap ratio such that the quantization error stays minimum for all bias currents, the capacitor has been made programmable.

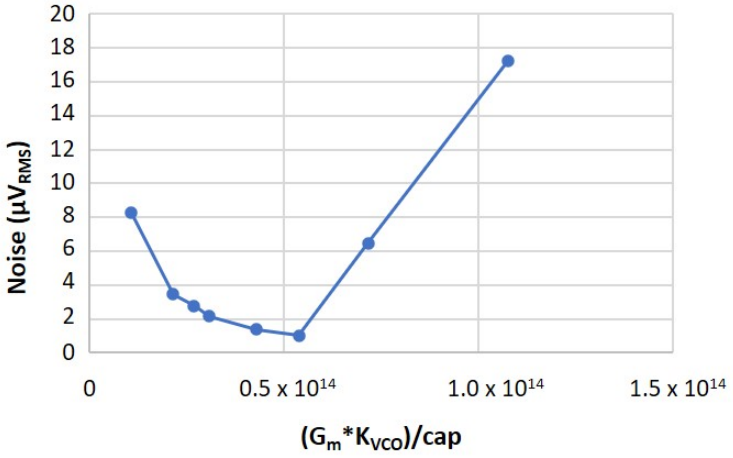


Figure 4.5: Variation of SNR with respect to the K_{VCO}/cap ratio

The center frequency of the VCO, f_0 has been chosen to be half the clock frequency (f_s) to ensure a stable oscillation. After a preliminary circuit design of the VCO with a center frequency of f_0, a feasible value of 1.875 MHz/V has been chosen for K_{VCO}, and the value of the capacitor is calculated

to be 140 fF for minimum noise. The counter counts the number of rising edges in the oscillation for each clock period ($1/f_s$). All the parameter choices discussed so far are tabulated in table 4.2.

Parameter	Value			
$I_{b,IS}$	200 nA	400 nA	800 nA	1.2 μA
G_{IS}	4 $\mu\Omega^{-1}$	8 $\mu\Omega^{-1}$	16 $\mu\Omega^{-1}$	24 $\mu\Omega^{-1}$
$I_{b,DAC}$	180 nA	360 nA	720 nA	1.08 μA
G_{DAC}	40 nA	80 nA	160 nA	240 nA
cap	140 fF	280 fF	560 fF	840 fF
K_{VCO}	1.875 MHz/V			
f_0	500 kHz			
f_s	1 MHz			

Table 4.2: Parameters of the VCO based ADC for different bias current conditions

With these parameters, an optimized quantization noise of 1.02 μV_{RMS} has been attained. This noise meets the set specification for the quantization noise, leaving enough margin to the main noise contributors, thermal and flicker, which are still not taken into account. The PSD obtained for the VCO based ΣΔ ADC for a sinusoidal input with 100 μV amplitude and 1 kHz frequency is shown in the figure 4.6, confirming the 40 dB/decade slope. The $SQNR_{max}$ obtained for the ADC is 62.8 dB, and the ENOB as calculated from (SQNR - 1.76)/6.02 is 10.1, qualifying the ADC specifications. The variation of the ADC SQNR with respect to the different input voltages is plotted and shown in figure 4.7, which confirms the calculated $SQNR_{max}$ to be close to 63 dB at a full-scale of 2mV.

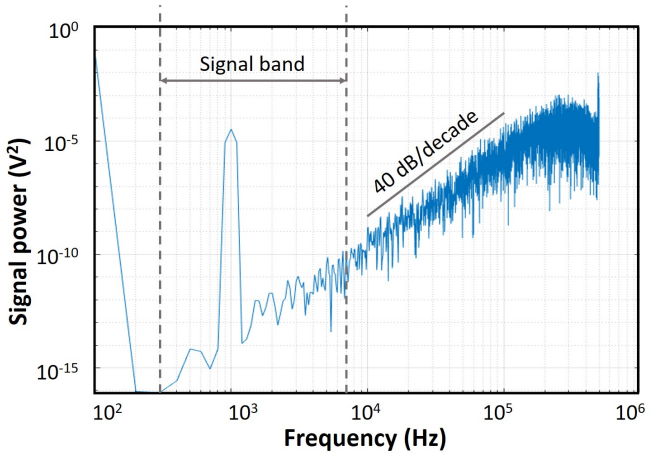


Figure 4.6: PSD of VCO based ΣΔ modulator yielding an $SQNR_{max}$ of 62.8 dB

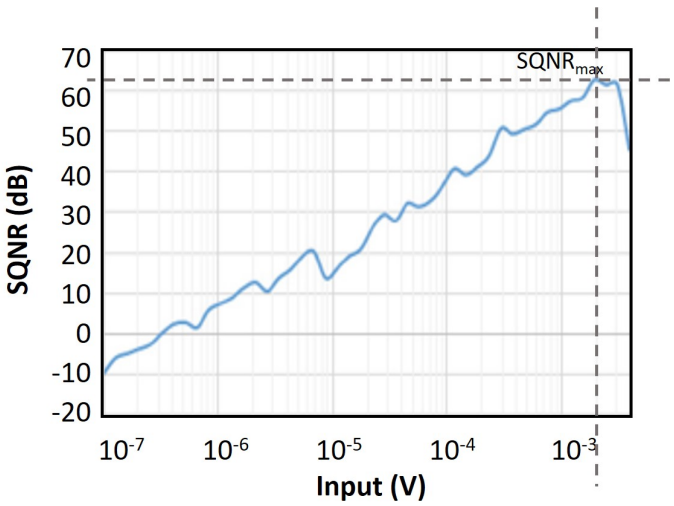


Figure 4.7: SQNR vs input voltage of the readout channel

4.3 VCO based ΣΔ ADC for MEA

The working principle of the VCO based ΣΔ ADC designed in this thesis, is shown in figure 4.8. The input stage comprises a high-pass filter (HPF) that removes the low-frequency voltage drift, and a transconductor that converts the extracellular AP voltage into the current. In the APS MEA implementation, this input stage is the AFE that will be integrated in the pixel. The difference in the currents of the input stage and feedback DAC is integrated by the capacitor, modulating the frequency of the VCO, which is converted to digital readout by the frequency-to-digital converter (F2D). The output current of the feedback DAC is set based on the F2D output, making the whole system a classic negative-feedback system.

For instance, when the feedback DAC current is higher than the input stage current, the voltage across the capacitor decreases, thereby reducing the frequency of the output signal from the VCO. This results in a decrease in the average F2D output, which decreases the output current of the feedback DAC to be less than the input stage current. The system operates such that the voltage at node X1 is ensured to be oscillating stably around the DC point. The value of the center frequency of the VCO depends on the average output of F2D that would make the DAC compensate the current from the input stage. The digital output of the F2D, which is sampled at a clock frequency of 1 MHz, is then sent off-chip where it is post-processed.

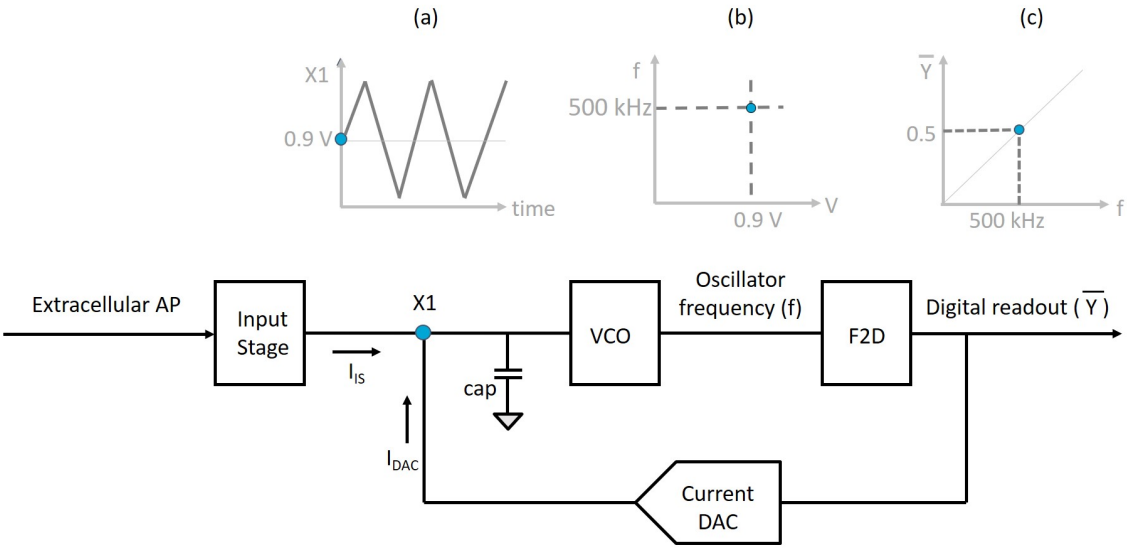


Figure 4.8: System level block diagram of the VCO based **ΣΔ** ADC showing the DC point operation at each node

The input stage current, DAC currents, and VCO properties will be designed to keep the average voltage of X1 around 0.9V, leaving enough voltage headroom for both the input stage and DAC. The triangular waveform at the node of the capacitor (figure 4.8a) shows the integration of difference in the input stage and feedback DAC currents. The VCO is designed such that the center frequency is 500 kHz when X1 voltage is 0.9 V (figure 4.8b). This also sets the average value of the F2D output at 0.5 at the center frequency (figure 4.8c). The individual circuit level implementation of each ADC block will be explained in detail in chapter 5.

4.4 Circuit impairments

Non-idealities can degrade the performance of the proposed ADC, which may appear in the different building blocks. However, since the MEA is a laboratory system, most of these non-idealities can be calibrated before the experiments, and necessary correction can be applied. During calibration, we can inject a known sinusoidal input and measure the output. Since the distortion and offset obtained during calibration are constantly there, they are always deterministic and compensated during post-processing. For this ADC readout channel, we neglect the analysis of DC errors such as gain and offset errors, because ideally, these should be filtered by the digital band-pass filter during post-processing. Also, since this is a sigma-delta ADC, it is inherently monotonic, avoiding any problems due to monotonic instability. Some of the important non-idealities that can appear during the circuit design of the ADC blocks are listed here.

4.4.1 Transconductor

The transconductor implemented in the input stage is one of the most sensitive blocks of the system because it is the first stage without any amplification before. Any noise and distortion present in the transconductor can directly affect the signal quality. During the system-level implementation, the input stage (and hence, the transconductor) has been modeled as a block with linear gain. However, in reality, no circuit implementation is linear, making the distortion inevitable. Techniques such as source degeneration could be used for a wide linear input stage. However, there is very less available space for designing a transconductor with such implementations. Fortunately, since the input signals we want to readout are typically below 1 mV amplitude, the distortion for this narrow signal range should not be a problem. In any case, the distortion can also be calibrated by applying a known input signal while measuring the output. The shape of the distortion can be estimated this way, assuming it is repetitive. This correction can be applied to the readout signal in the post-processing stage.

There can also be non-idealities arising due to the process, voltage, and temperature variations. The variations due to temperature are not very important in the MEA application, because all the experiments are carried out in a temperature-controlled environment, an incubator, to maintain the biological sample. The voltage variations are also not critical because a regulated voltage supply is used with an option to trim the supply if necessary. The effect of process variations will be present, which will be simulated using corner analysis in the next chapter.

The current ($I_{b,IS}$) used to bias the transconductor can vary if the transconductor is placed far from the reference generators. This could cause an offset error, which can be high-pass filtered using the digital filter during post-processing. It is, however, advantageous to have an option to trim the bias current so that we can compensate this offset error is needed.

4.4.2 Current DAC

The DAC used in this readout channel is a 1-bit DAC making it inherently linear. So, it usually does not require any calibration or trimming [60]. The possible non-idealities in the DAC could be caused due to the variations in bias currents that affect the output and gain of the DAC, and trimming could be a possible solution. The variations due to the process variations have been simulated and analyzed in the next chapter using corner analysis.

4.4.3 Capacitor

Although the capacitors fabricated are very accurate, there would be additional parasitic capacitance that could change the effective value of the integrator capacitance. However, small changes in the

value of capacitance should not increase the quantization noise a lot, given the ±10% tolerance of the capacitance value (shown in figure 4.5). Nevertheless, it would be better to have trimming options for the final MEA with one small capacitor that can be used for trimming.

4.4.4 VCO based quantizer

The two main non-idealities in the VCO are the phase noise and non-linear relationship between the input voltage and output frequency (K_{VCO} non-linearity). Ideally, the oscillation frequency would be a deterministic value which only depends on circuit parameters and the input voltage. In reality, there is a stochastic component due to circuit noise that randomly shifts the instantaneous oscillation frequency, which is the phase noise (see Appendix B) [17, 64]. A non-linear VCO can degrade the system's performance, and it is not possible to apply a digital correction to overcome this. However, the VCO placed inside the feedback loop reduces the effect of the non-idealities from K_{VCO} non-linearity and VCO phase noise as it is filtered out by the loop [17]. The VCO design with a rather linear K_{VCO} will be explained in chapter 5. The variation in K_{VCO} value can affect the quantization noise of the ADC (figure 4.5) which can be compensated if needed, by the trimming capacitor that has been mentioned in subsection 4.4.3.

The F2D in the VCO quantizer should be designed to cover the full range of the oscillation frequencies and provides a monotonically increasing average output, to avoid problems due to instability. The architecture used to design the F2D with these features will be explained in the next chapter.

4.4.5 Clock jitter and metastability

Continuous-time ΣΔ modulators are more sensitive to random variations in the sampling period which is the clock jitter. The errors introduced by clock jitter are visible on the output spectrum and may limit the degrade the performance of the ADC. This would be a problem in other applications, where the clocks are generated on-chip and are not very stable, such as consumer electronics. However, for an MEA, very stable off-chip clock generators are implemented since the MEA is a lab instrument. Due to non-synchronization between the oscillators and the sampling clock, there can be inevitable problems due to metastability in digital circuitry. However, simulations can show if this error is frequent enough to degrade the system's performance.

4.5 Conclusion

The implementation of the system-level design of VCO based ΣΔ ADC has been demonstrated here, focusing on the design choices made in building the ADC system. A noise optimum of 1.02 μV_{RMS} has

been obtained from the system-level (ideal) implementation giving an $SQNR_{max}$ of 62.8 dB. The circuit impairments that should be taken care of while translating this system-level design to its transistor-level counterpart are introduced in this chapter. In the next chapter, this design is translated into transistor-level and then the layout-level design, which would mark the completion of the VCO based ΣΔ ADC design flow will be shown.

5 Implementation of VCO based ΣΔ ADC

The ADC proposed in the chapter 4 has been implemented in 0.18 μm CMOS technology node for the test chip, to test the different design variants of the blocks in the ADC. To have a possibility to characterize the ADC blocks, bidirectional probing has been used. In the MEA system, the noise common to all the channels can be filtered during post-processing. This is a potential disadvantage of implementing a single readout channel in the test chip. A pseudo-differential implementation of this readout system has been chosen for this test chip to account for this. The chapter starts by explaining the design choices made to implement each block in the ADC system, arriving at the ADC integration in the test chip, and the results obtained.

5.1 Circuit design of VCO based ΣΔ ADC

5.1.1 Input stage

5.1.1.1 Architecture

The input stage has the components that are part of the pixel in an APS MEA, as shown in figure 5.1. A high-pass filter (HPF), as mentioned, is designed to filter the low-frequency voltage drifts. So, the voltage V_X in figure 5.1 is the summation of the bias voltage and fast electrode voltage. The cut-off frequency of the HPF should be designed to be less than at least 10 Hz to make sure this HPF does not filter the signals in action potential band. A PMOS transconductor that converts the filtered electrode voltage into the current is designed along with a cascode stage to increase the output impedance, thereby making the current independent from the output node. PMOS transistors have been chosen for the input stage design due to the low flicker noise in PMOS compared to the NMOS transistor with the same size. This is due to the lesser value of hole mobility resulting in lesser collisions due to Brownian motion. Due to the size constraints of the pixel, the size of the transistors in the transconductor block (M_1, M_2), capacitor (C_{HPF}), and the HPF resistor have been minimized for optimum area. For the low cut-off frequency (f_{3dB}) needed to implement the HPF, a pseudoresistor has been designed to provide TΩ without consuming much of the pixel area.

An optimum noise from the input stage components is desired as this is the first stage, and the noise in this stage would deteriorate the system performance. The three transistors in the input stage

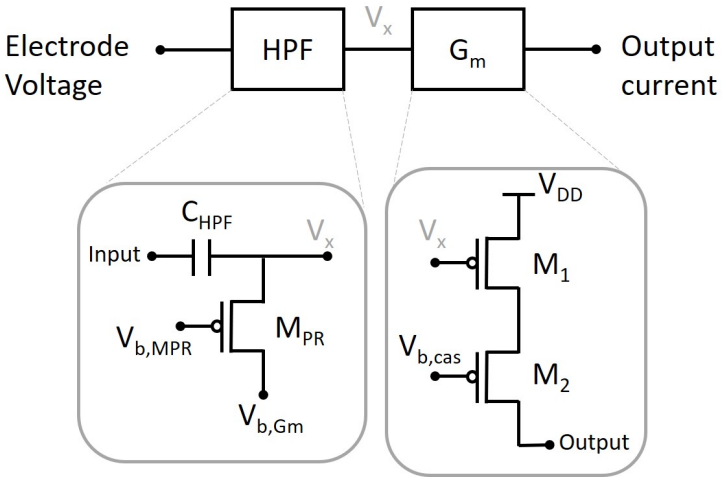


Figure 5.1: Input stage of the readout channel

mainly contribute to this noise as the capacitor does not generate noise (see Appendix B). The gain of the input stage (G_{IS}) is given by the product of the magnitude of the HPF transfer function (H(s)) and the value of transconductance of the transconductor stage (G_m). G_{IS} (= |H(S)| . G_m) should be maximum for amplifying the signal while having minimal noise for better signal quality. This gain depends on the choice of model parameters such as capacitance of the HPF (C_{HPF}), the resistance of the pseudoresistor (given by $W_{M_{PR}}$, $L_{M_{PR}}$, V_{PR}), and G_m. The gain of the HPF at 1 kHz ($|H(S)|_{G1k}$), as shown in figure 5.2 should be designed such that any attenuation due to the filter should be minimum.

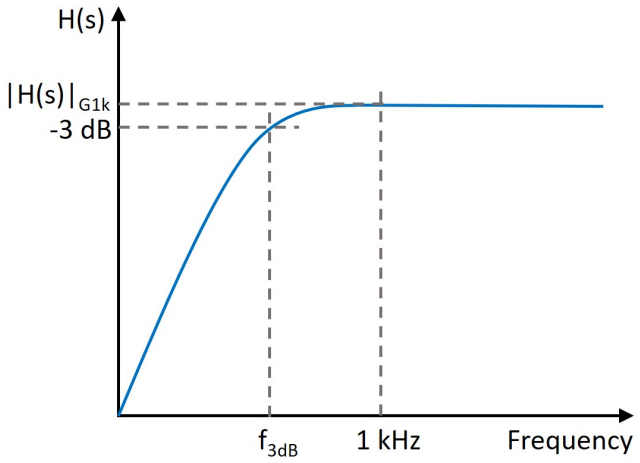


Figure 5.2: Transfer function of HPF

In the HPF, the main noise component would be given by the kT/C noise, which is dependent on the value of capacitance only. However, this noise is generated by the pseudoresistor and not the capacitance itself (see Appendix B). The noise generated by the pseudoresistor should be low-pass filtered to keep this noise out of the signal band. This will be done by the capacitor (C_{HPF}) seen from $V_{b,Gm}$ node of the pseudoresistor (figure 5.3a) when the noise (V_n) is referred to the input. Figure 5.3b

explains this concept, from which it can be seen that when a cut-off frequency of 10 Hz is chosen, some on the pseudoresistor noise (V_n) can be present in the signal band. This behavior has been observed and confirmed during simulations. With very low cut-off frequency, we can make sure that the noise from the pseudoresistor does not disturb the signal band. After choosing the optimum value for capacitance, depending on the pixel size restriction, the cut-off frequency depends only on the pseudoresistor. To achieve a very low cut-off frequency, a pseudoresistor has been implemented with the parameters and biasing, as shown in table 5.1 to get a cut-off frequency of 1.6 Hz, to minimize the pseudoresistor noise in the signal band (figure 5.3b). The total noise (given by the area under the curve) remains the same, while the cut-off frequency controls the amount of in-band (300 - 7 kHz) noise. Figure 5.4 shows the HPF behavior obtained through AC analysis. The attenuation caused by the HPF has been minimized to avoid the steep decrease in overall input stage gain. The results obtained for the designed HPF are shown the table 5.2.

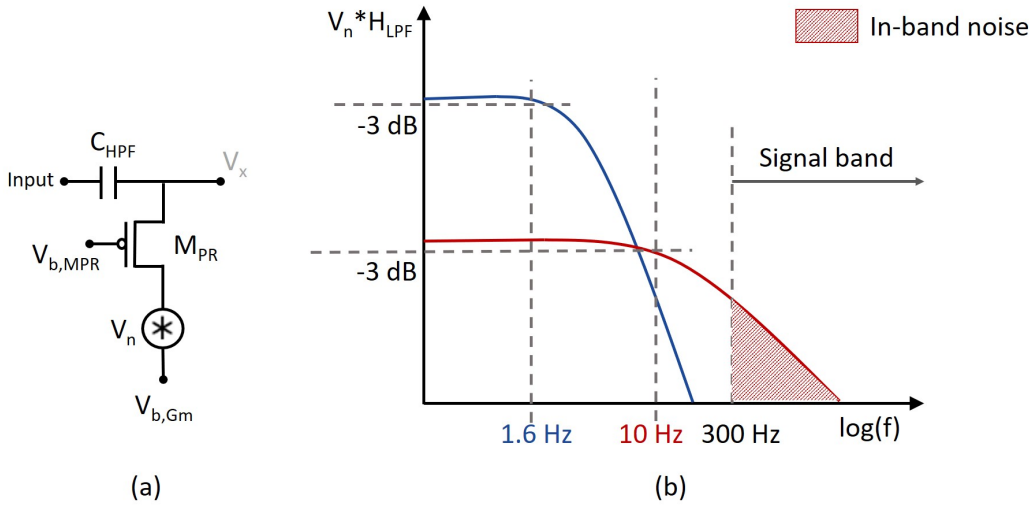


Figure 5.3: (a) LPF seen from the node of pseudoresistor, filters the noise from pseudoresistor when being referred to the input, (b) Pseudoresistor noise after being low pass filtered (V_n*H_{LPF}) by LPF with cut-off frequencies 10 Hz (initial) and 1.6 Hz (optimized).

Parameter	Value
C_{HPF}	300 fF
$W_{M_{PR}}$	1 μm
$L_{M_{PR}}$	400 nm
$V_{b,M_{PR}}$	1.8 V
$V_{b,Gm}$	1.492 V

Table 5.1: Parameters of input stage HPF

HPF results	
Parameter	Value
-3dB frequency (f_{3dB})	1.6 Hz
Gain at 1kHz	-1.8 dB
HPF attenuation	-1.8 dB

Table 5.2: Results obtained for input stage HPF

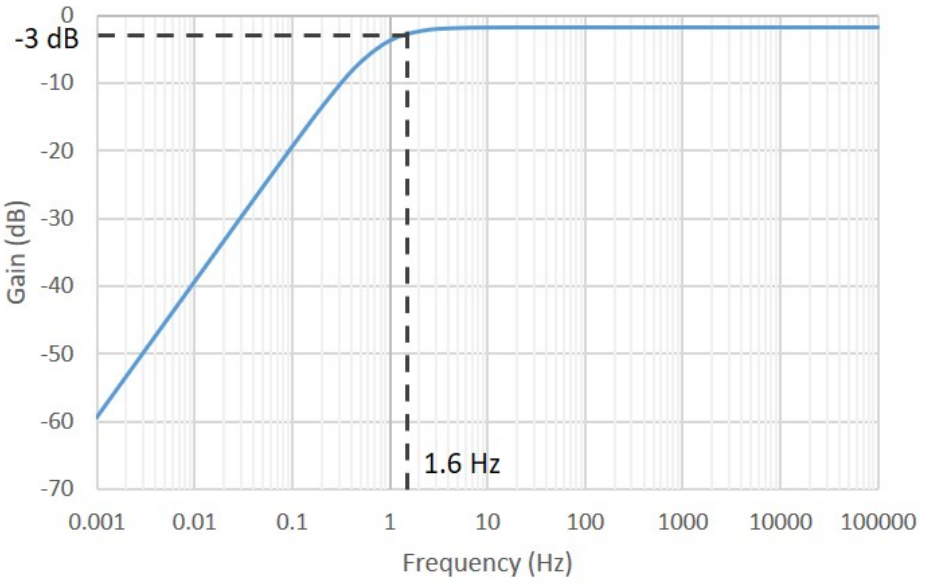


Figure 5.4: Frequency response of HPF obtained from AC analysis

The gain, G_m can be approximated to the transconductance of the M_1 transistor, since the cascode transistor (M_2) does not contribute much to the gain of the transconductor [73]. So the parameters, that define the value of G_m are W_{M_1} and L_{M_1}. The M_1 transistor is the main contributor to the noise in G_m stage as the noise generated by the cascode transistor is comparatively negligible due to degeneration [73]. The transistors M_1 and M_2 in the transconductor stage are modeled with the model parameter values, as shown in table 5.3 to achieve optimum noise and area consumption while keeping in mind the trade-off between transistor sizes and flicker noise (small transistors result in high flicker noise). The gain obtained for different bias currents by the transconductor stage, and the input stage is given in table 5.4, which also shows the slight attenuation due to the HPF.

Parameter	Value (μm)
W_{M_1}	30
L_{M_1}	1.2
W_{M_2}	10
L_{M_2}	1.2

Table 5.3: Parameters in G_m stage

Current (I_{bias})	200 nA	400 nA	800 nA	1.2 μA
G_m (Ω^{-1})	5.177μ	9.647μ	18.07μ	25.84μ
G_{IS} (Ω^{-1})	4.139μ	7.712μ	14.27μ	20.4μ

Table 5.4: Gain of the transconductor (G_m) and input stage (G_{IS})

The output noise power of the input stage has been plotted and shown in figure 5.5. The input-referred noise (IRN) of the input stage, calculated for different bias currents, has been summarised in the table 5.5. It can be seen that the total noise and thermal noise decreases with higher bias currents.

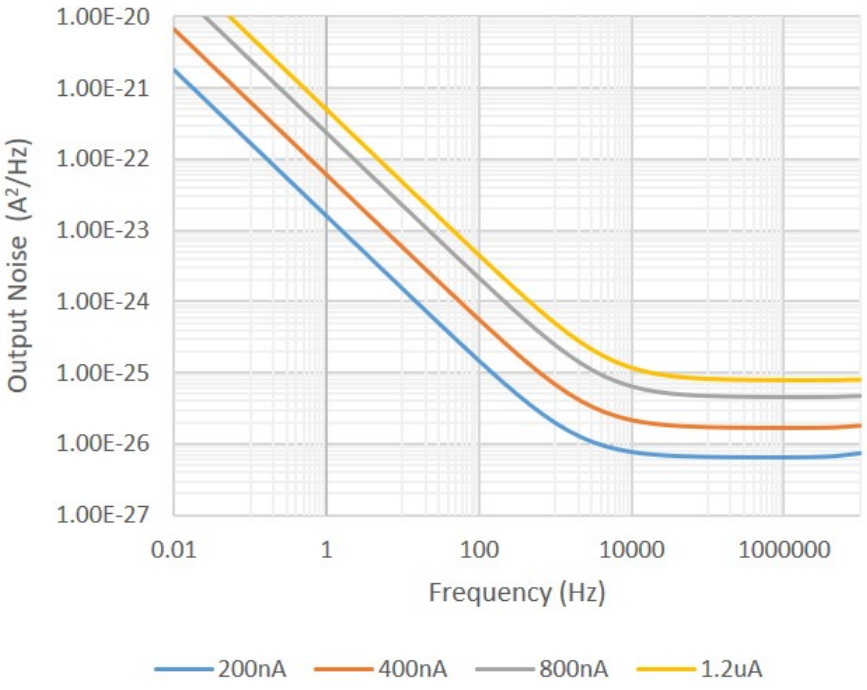


Figure 5.5: Output noise (in A^2/Hz) of input stage for different bias currents

Bias current	200nA	400nA	800nA	1.2 μA
Total Noise (μV_{RMS})	1.836	1.769	1.74	1.732
Flicker Noise (μV_{RMS})	1.318	1.388	1.45	1.481
Thermal Noise (μV_{RMS})	1.279	1.098	0.962	0.897

Table 5.5: Results obtained for total (input referred), flicker and thermal noise for different bias currents

5.1.1.2 Corners and Monte Carlo analysis

The circuit performance under extreme variations in the manufacturing process can be measured through the corner analysis in Cadence. The extreme variations in the process, temperature, and voltage parameters are considered in this analysis. However, the temperature and supply variations are not very critical in this case since the temperature will be maintained at 37^0C as all the experiments will be carried out when MEA is placed in the incubator, and the power supply can be regulated at 1.8 V through voltage trimming. The corner analysis simulates extreme cases that typically never exist during real fabrication, guaranteeing that the circuit will work under any circumstance.

The worst cases are 'ws' which is the worst speed, 'wp' which is the worst power, 'wo' which is the worst one when NMOS is very fast compared to the PMOS, and 'wz' which is the worst zero where PMOS is very fast compared to the NMOS. The table 5.6 shows the results obtained for the corner analysis of the input stage for a bias current of 400 nA. The variation of the parameters obtained is within a $\pm$10% tolerance.

	wp	ws	wo	wz
G_m	9.918μ	9.370μ	9.463μ	9.817μ
G_{IS}	7.821μ	7.366μ	7.442μ	7.741μ

Table 5.6: Corner analysis summary for input stage (I_{bias} = 400 nA)

The Monte Carlo analysis has been performed in Cadence to statistically analyze the VLSI circuit under the effects of process variation and device mismatch in a single chip or wafer. It calculates the randomness of the parameter according to a statistical distribution model during each simulation run. With this analysis, the most frequent region at which the circuit operates can be observed. The histogram obtained from the Monte Carlo analysis for the gain of the input stage performed in Cadence, for a bias current of 400 nA, is shown in figure 5.6. It can be seen that the variation of the gain of the input stage at 1 kHz is minimum, ensuring the robustness of the design.

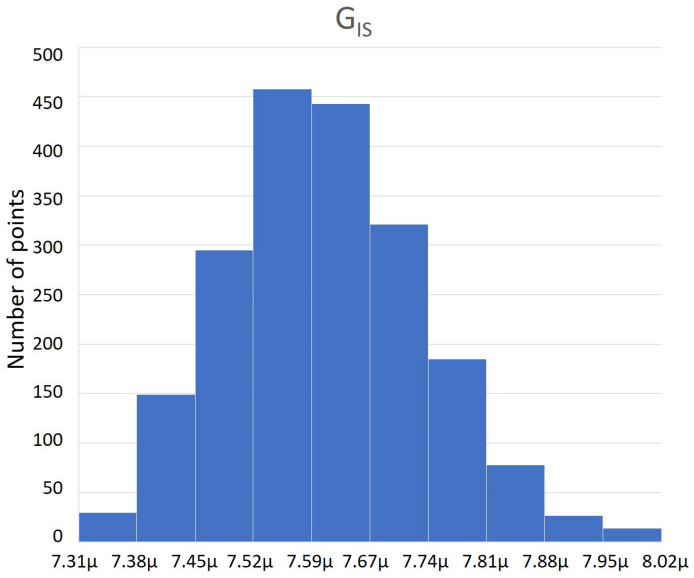


Figure 5.6: Monte Carlo analysis for the input stage (I_{bias} = 400 nA)

5.1.2 Feedback DAC

5.1.2.1 Architecture

A 1-bit current DAC has been implemented for the ADC as shown in figure 5.7. As explained in chapter chapter 4, based on the output of the frequency-to-digital converter, the current DAC gives a current of $I_{bias} \pm \Delta I$. The value of ΔI is modelled such that $\Delta I = (0.1{*}I_{bias})$. The current mirror generates a current of $(0.9{*}I_{bias})$ and $(0.2{*}I_{bias})$ in each of the two branches. The ADC output switches the transmission gate in the $(0.2{*}I_{bias})$ branch ON or OFF deciding the total current that is generated by the DAC. This can be related to the DAC behavioral model shown in figure 4.4 where G_{DAC} is given by $(0.2{*}I_{bias})$. To keep the transistors M_5 and M_6 biased all the time, a dummy transmission gate implemented using $M_{dummy,P}$, and $M_{dummy,N}$ is used. The value of V_{dummy} is set to 0.9 V, the DC operation point as shown in the figure 4.8.

The transistors' width and length have been chosen such that the thermal and flicker noise generated by the DAC transistors is minimum (table 5.7). The value of the switching transmission gate transistors is chosen to be as small as possible to achieve fast switching. The noise generated by the transistors in the DAC varies with the biasing current. For biasing currents as low as 200 nA, it has been observed that the parameters of the transistors in the DAC are slightly different, which is why two design variants of the DAC were implemented for the test chip, whose parameters are given in the table 5.7. The DAC1 can be used for small bias currents which are less than 200 nA, while the DAC2 is used for bias currents greater than 200 nA for optimum noise performance.

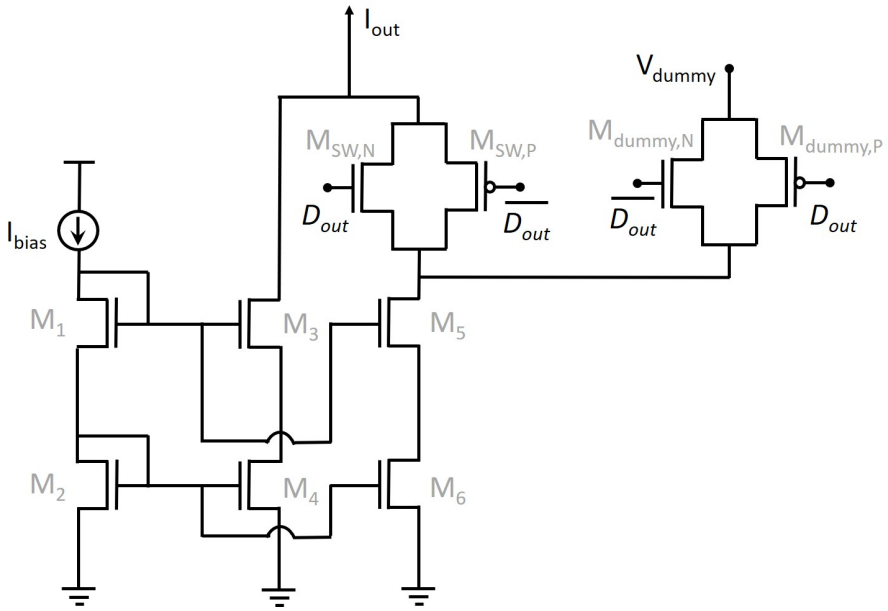


Figure 5.7: Current DAC for feedback in the ADC

Parameters	DAC1		DAC2	
	W	L	W	L
M_1, M_2	10 * 1 μm	5 μm	10 * 0.7 μm	10 μm
M_3, M_4	9 * 1 μm	5 μm	9 * 0.7 μm	10 μm
M_5, M_6	2 * 1 μm	5 μm	2 * 0.7 μm	10 μm
$M_{SW,P}$, $M_{dummy,P}$	0.42 μm	0.18 μm	0.42 μm	0.18 μm
$M_{SW,N}$, $M_{dummy,N}$	0.29 μm	0.18 μm	0.29 μm	0.18 μm
V_{dummy}	0.9 V		0.9 V	

Table 5.7: Parameters of transistors in DAC1 (I_{bias} = 200 nA) and DAC2 (I_{bias} = 400 nA, 800 nA and 1.2 μA) for optimized noise. (m * k μm) represents that m number of fingers each with a width of k μm has been used.

The output noise power of the DAC for different bias currents is plotted in figure 5.8.Most of the noise is contributed by the transistors M_4 and M_6, and the cascode transistors almost generate relatively negligible noise. This can be observed in the noise analysis performed for each bias current as tabulated in table 5.8, which shows the major noise sources in the circuit and the type and percentage of total noise it generates. The total DAC noise referred to the input of the IS stage, is also shown in the table for respective bias currents.

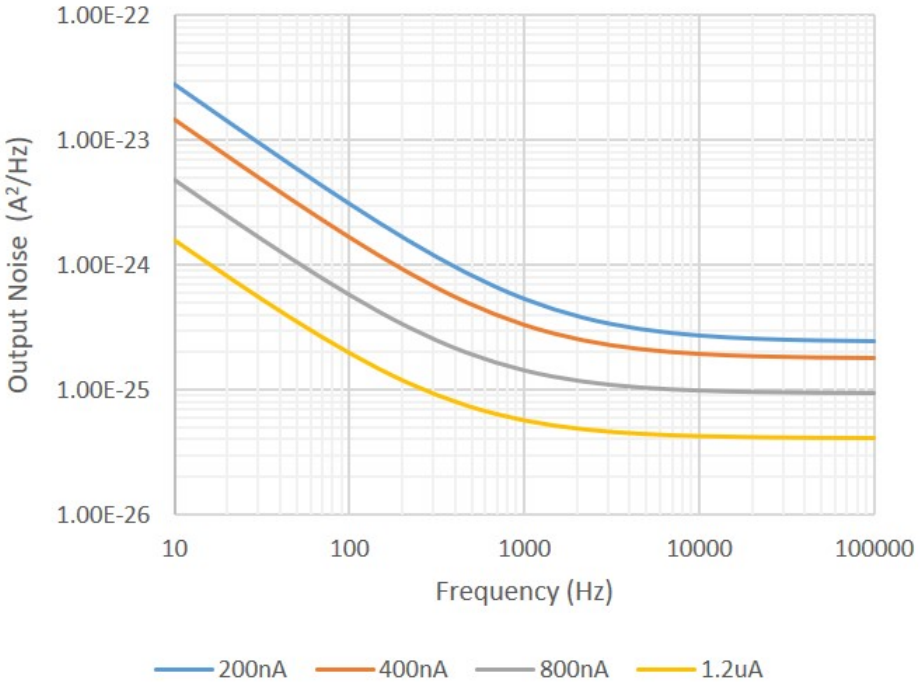


Figure 5.8: Output noise (in A^2/Hz) of the current DACs for different I_{bias}. Parameters for DAC2 have been chosen to simulate the noise for I_{bias} = 400 nA, 800 nA and 1.2 μA. DAC1 parameters have been used to simulate the noise when I_{bias} = 200 nA

		Bias current			
Device	Noise type	200 nA	400 nA	800 nA	1.2 μA
M4	flicker	13.74%	17.68%	25.33%	31.7%
M4	thermal	68.08%	64.14%	56.49%	50.12%
M6	flicker	3.05%	3.93%	5.63%	7.04%
M6	thermal	15.13%	14.25%	12.55%	11.14%
Total Noise (μV_{RMS})		4.445	3.735	2.951	2.585

Table 5.8: The percentage contribution of noise (flicker and thermal) from each device. The total noise given by the DAC is referred to the input.

5.1.2.2 Corners and Monte Carlo analysis

The results obtained from the corner analysis are shown in the table 5.9 for an I_{bias} of 200 nA and D_{out} set to 1. The effect of process variations and device mismatch during semiconductor manufacturing on the output current of the DAC and the input-referred noise (IRN) is shown in the histograms in figure 5.9. It can be seen that the most values of I_{bias} and IRN are close to nominal values showing the robustness of the DAC designed. As long as the variations in the currents are small enough, the ADC gain and the average output value will not be substantially affected.

	wp	ws	wo	wz
Iout (nA)	220	220	220	220
IRN (μV_{RMS})	3.372	3.566	3.433	3.513

Table 5.9: Corner analysis for current DAC2

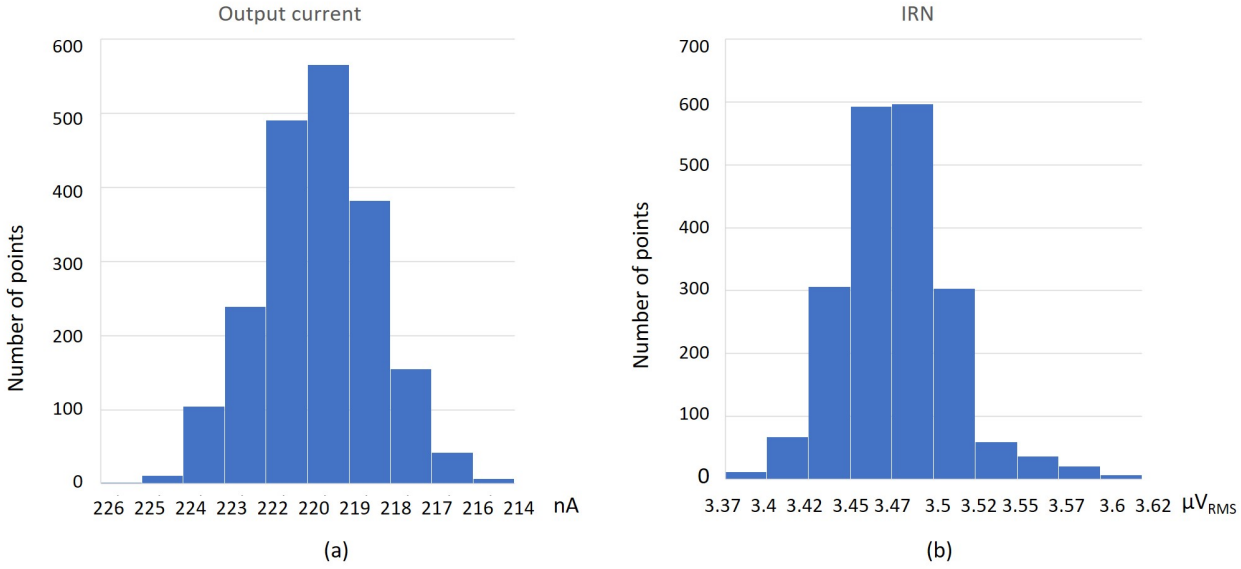


Figure 5.9: Monte Carlo analysis for DAC2 (I_{bias} = 200 nA)

5.1.3 Integrator

A capacitive integrator has been designed, considering the current output from the input stage and feedback DAC. The value of the capacitor, which integrates the difference in transconductor and DAC currents, depends on the bias current. Since the bias current changes the gain of the input stage and ADC, the capacitor has to be modulated accordingly to keep the G_{IS}*K_{VCO}/cap value constant (figure 4.5) as discussed in chapter 4. A programmable capacitor (figure 5.10) to accommodate the different choice of bias currents has been designed, and the values of the capacitance for different bias currents and the control bits to get the respective effective capacitance from the integrator are shown in the table 5.10. These values of the capacitors are the nominal values needed for each biasing. However, there is a flexibility to trim these values depending on parasitics.

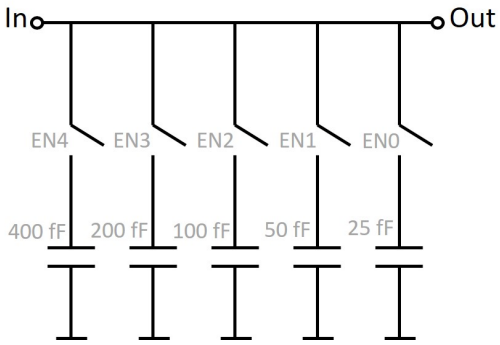


Figure 5.10: Programmable capacitor

Ibias	Capacitance	EN4	EN3	EN2	EN1	EN0
200 nA	125 fF	0	0	1	0	1
400 nA	250 fF	0	1	0	1	0
800 nA	500 fF	1	0	1	0	0
1.2 μA	750 fF	1	1	1	1	0

Table 5.10: Parameters of programmable integrator for different bias currents

5.1.4 Voltage controlled oscillator

5.1.4.1 Architecture

The key building block of the frequency-based encoding is the oscillator that can be controlled by the magnitude of the input parameter, such as voltage, current, capacitance, or resistance. In this ADC design, a voltage-controlled oscillator (VCO) has been designed, which converts the input voltage to frequency. The VCO is sensitive to process and temperature variations, introducing distortion in the system for large input voltages. A 3-stage ring oscillator based VCO design has been implemented for this ADC, with source follower and level shifter (figure 5.11). The source follower has been used to alter the DC point of the VCO from 0.9 V to a value needed to set the center frequency to 500 kHz.

The VCO has been characterized to achieve a linear relationship ('Optimized VCO') between voltage and frequency. Table 5.11 gives the parameters of the two design cases, while figure 5.12 shows the corresponding voltage to frequency transfer characteristic of the VCOs, for evaluating the non-linearity. This transfer characteristic has been obtained by performing periodic steady-state (PSS) analysis by sweeping the voltage between ±200 mV and plotting the corresponding frequency.

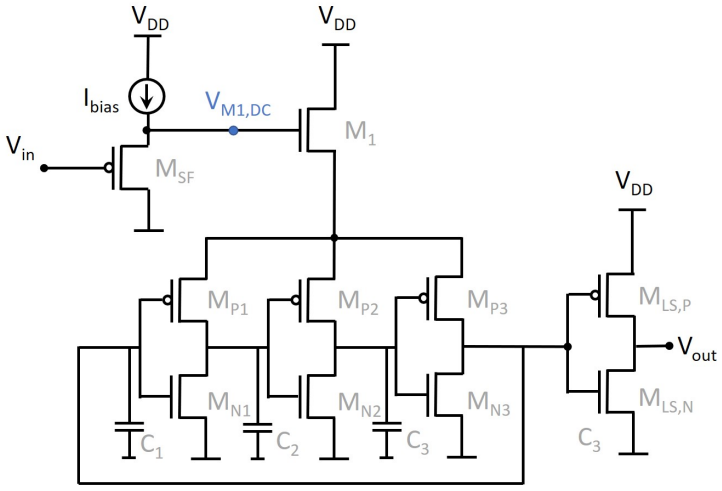


Figure 5.11: Schematic of the VCO along with the source follower and level-shifter

Parameters	Initial VCO		Optimized VCO	
	W	L	W	L
M_1	600 nm	4 μm	400 nm	20 μm
M_{P1}, M_{P2}, M_{P3}	5 μm	6 μm	5 μm	6 μm
M_{N1}, M_{N2}, M_{N3}	2 μm	6 μm	2 μm	6 μm
M_{SF}	4 μm	600 nm	400 nm	2 μm
$M_{LS,P}$	400 nm	2 μm	400 nm	2 μm
$M_{LS,N}$	4 μm	400 nm	4 μm	400 nm
C_1, C_2, C_3	70 fF		70 fF	
I_{bias}	20 nA		20 nA	
$V_{M1,DC}$	1.2 V		1.392 V	

Table 5.11: Design parameters of the VCO before (Initial VCO) and after (Optimized VCO) compensating the non-linearity

The voltage to frequency transfer obtained for the initial and optimized VCOs are,

$$f(V_{\text{in}})_{\text{initial}} = (-3.06(V_{\text{in}} - 0.9)^3 + 3.873(V_{\text{in}} - 0.9)^2 + 2.573(V_{\text{in}} - 0.9) + 0.509) * 10^6$$
$$f(V_{\text{in}})_{\text{optimized}} = (-0.985(V_{\text{in}} - 0.9)^3 + 0.88(V_{\text{in}} - 0.9)^2 + 1.576(V_{\text{in}} - 0.9) + 0.523) * 10^6$$

The coefficients of the second- and third-order terms have been reduced in the optimized VCO to reduce non-linearity. The distortion due K_{VCO} non-linearity has been quantified by the ratio of the second-order term to the first-order term in the equations, which is 1.497 before, and 0.558 after optimizing the VCO. The VCO output is connected to a level-shifter, which translates the output

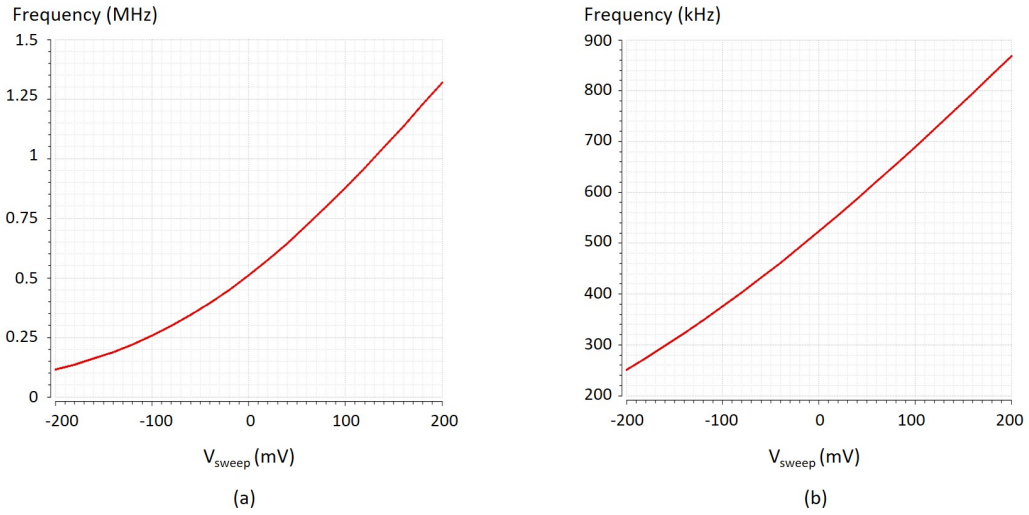


Figure 5.12: VCO transfer: (a) before (Initial VCO) and (b) after (Optimized VCO) minimizing the non-linearity of the VCO

frequency signal to a square signal varying between 1.8 V and 0 V, to feed into the F2D converter. The full schematic of this VCO, including the source follower and level-shifter, is shown in figure 5.11b. The transistors' parameters in level-shifter have been chosen to have a transition (high-to-low and low-to-high) at half the maximum output peak of the VCO. The designed VCO has a K_{VCO} gain of 1.576 MHz/V and a center frequency of 523.3 kHz. The difference in the value of K_{VCO} from the system level implementation (1.875 MHz/V) is due to the adaptation of the parameters for minimizing the non-linearity (section 4.4).

5.1.5 Frequency to digital converter

The frequency-to-digital converter (F2D) block converts the frequency output from the VCO to digital output by detecting the rising or falling edges of the VCO. Three different F2Ds have been designed and evaluated to check their feasibility to implement in the readout channel, which are listed here.

5.1.5.1 Architecture

The first F2D design is a AND-gate based rising-edge detector which is illustrated in the figure 5.13a. The operation of this circuit at $f_0 = f_s/4$, where f_0 is the frequency of the oscillator and f_s is the sampling frequency, is shown in figure 5.13b. The output Y[n] is 1 only when a rising edge of the VCO is detected when $Q_1[n] = Q_2'[n]$ (NOT $Q_2[n]$) = 1. The average output value, $\overline{Y}$ with respect to the ratio of oscillator(f_0) and sampling(f_s) frequencies is plotted in figures 5.13.

Figure 5.13c shows that, when $f_0 = fs/2$, the average output value reaches the maximum value of 0.5. When $f_0 > f_s/2$, the average value decreases making this design valid only in 0 to 0.5 range ($\overline{Y}$

range). However, 0.5 is the middle point for $\overline{Y}$, in the proposed ADC system (figure 4.8), and we need an F2D that can operate between 0 to 1 range. The second problem with this F2D is that there is more than one frequency that would generate the same $\overline{Y}$ output, since the function is not monotonically increasing, causing stability problems [74].

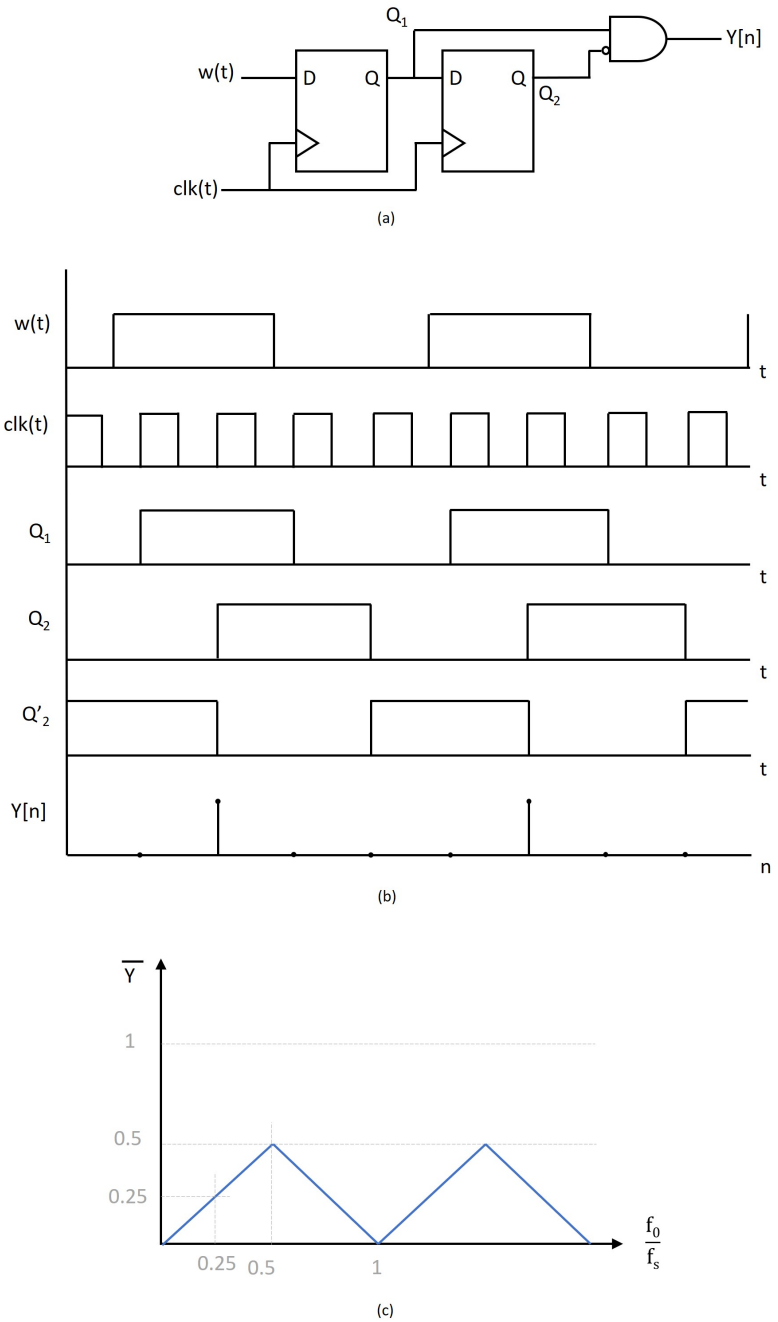


Figure 5.13: AND gate based F2D (a) Block diagram (b) Operation at $f_0 = f_s/4$ (c) Average output vs $\frac{f_0}{f_s}$

The second design of the F2D comprises a XOR-based modulator that detects both rising and falling edges of the oscillation. This allows accurate capturing of all the edges in the signals for

frequencies up to $f_s/2$. Figure 5.14 shows the working of the F2D for $f_0 = f_s/4$. The average output value, $\overline{Y}$ plotted against f_0/f_s can be seen the figure 5.14c. Although the signals are sampled properly for frequencies up to $f_s/2$, at oscillation frequencies beyond $f_s/2$ the F2D has the same problem as the previous design. So, although this F2D design solves the range problem (range of $\overline{Y}$ is 0 to 1), the modulator function is still not monotonically increasing, which may cause stability problems as f_0 approaches half the f_s.

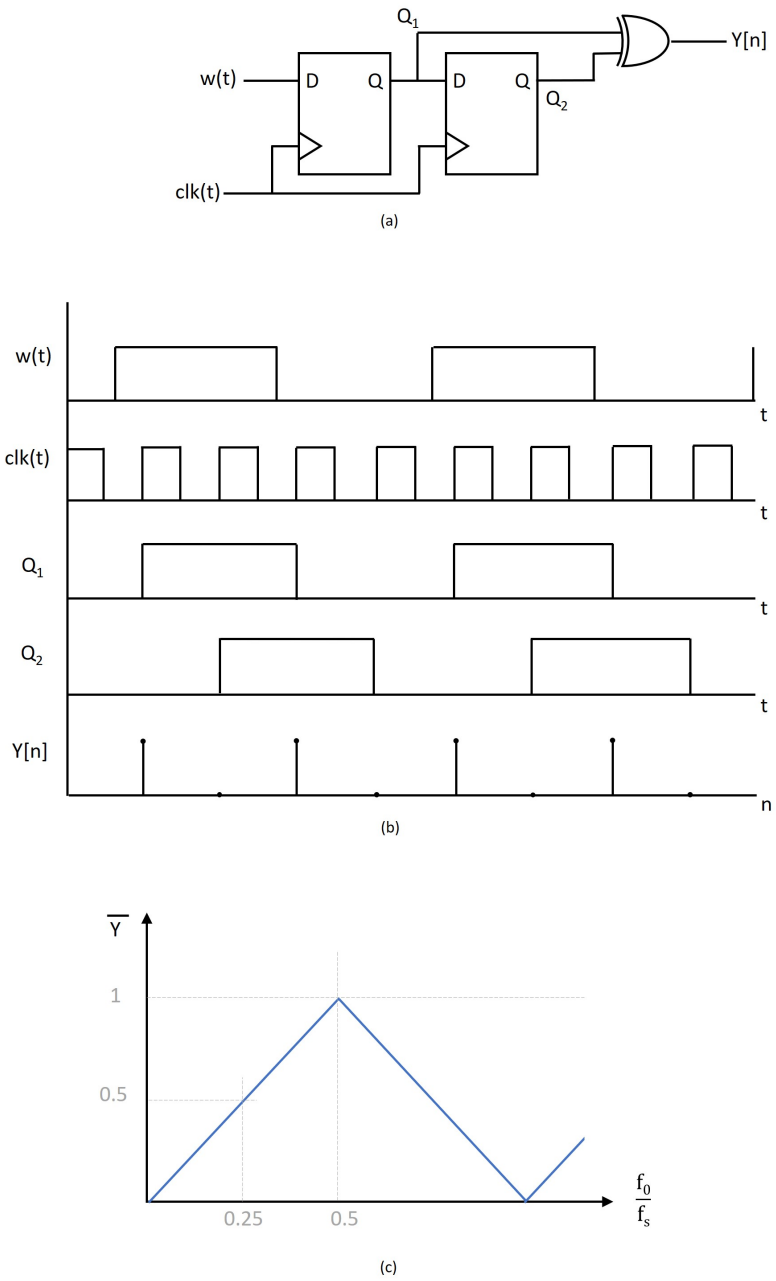


Figure 5.14: XOR gate based F2D (a) Block diagram (b) Operation at $f_0 = f_s/4$ (c) Average output vs $\frac{f_0}{f_s}$

To overcome the aforementioned limitations, a 3 flip-flop XOR-based DFF (figure 5.15) was

implemented in the ADC as a frequency to digital converter. This F2D uses a frequency divider to slow down the oscillation by $f_0/2$ and then samples the signal. Figure 5.15b shows the working of the F2D for $f_0 = f_s/4$. The average value of the output, Y[n], is maintained at 1 for frequencies above f_s, as seen in figure 5.15c saturating the upper limit of $\overline{Y}$ in case the signal oscillates faster than the f_s. This design solves both the range and non-monotonicity problems making it the best choice for this readout channel. This F2D consumes a current of approximately 100 nA for a supply voltage of 1.8 V.

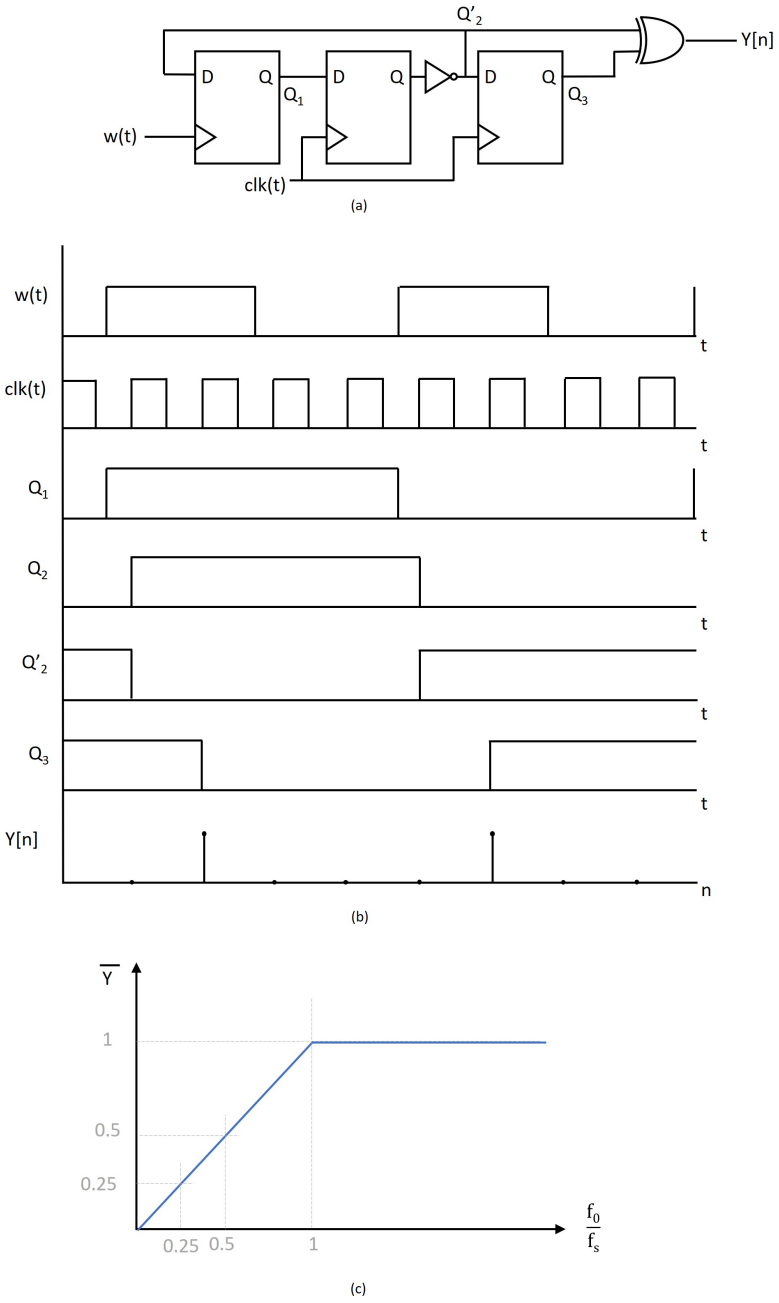


Figure 5.15: 3 flip-flop XOR based F2D (a) Block diagram (b) Operation of the F2D (c) Average output vs $\frac{f_0}{f_s}$

5.1.6 Schematic simulations

The results obtained from the circuit-level implementation of the VCO based ΣΔ ADC in Cadence are discussed in this section. The power spectral density plots obtained at different bias currents for an input voltage of 100 μV and frequency of 5 kHz are shown in figure 5.16, which confirm the second-order noise shaping of the ADC. The noise obtained in the AP band (300 Hz - 7 kHz) for different bias currents are reported in the table 5.12. The noise obtained from the schematic simulations, for the chosen bias currents lies between 3 - 7 μV_{RMS}. The noise is less than 4.2 μV_{RMS} for bias currents higher than 800 nA, satisfying the set specifications. The power consumed by each sub-circuit of the designed ADC and the total power consumed by the readout channel, for different bias currents, is shown in the table 5.13. It can be observed from tables 5.12 and 5.13 that the main trade-off to make is between the noise and power consumption of the ADC. However, since the power specifications are well within the set specifications, bias currents above 800 nA can be used for the final MEA since the noise per channel is lesser.

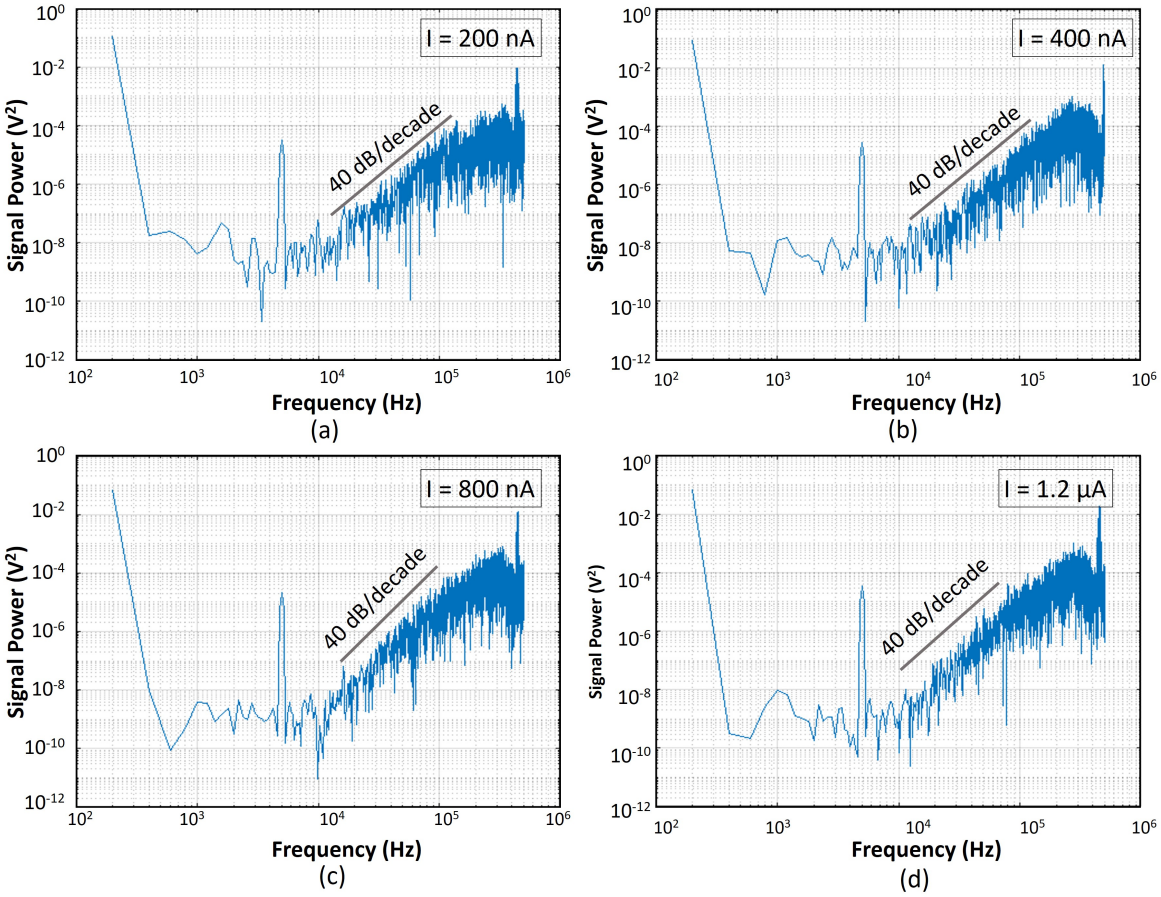


Figure 5.16: PSD obtained from schematic simulations when the bias current is (a) 200 nA (b) 400 nA (c) 800 nA and (d) 1.2 μA

Bias current	Noise (μV_{RMS})
200 nA	6.64
400 nA	5.3
800 nA	4.22
1.2 μA	3.17

Table 5.12: Noise obtained from schematic simulations for different bias currents

	Power consumption (μW)				
Bias current	Input stage	DAC	VCO	F2D	Full readout channel
200 nA	0.18	0.2	0.45	0.18	1.01
400 nA	0.36	0.4	0.45	0.18	1.39
800 nA	0.72	0.8	0.45	0.18	2.15
1.2 μA	1.08	1.2	0.45	0.18	2.91

Table 5.13: Power consumed by different blocks in the ADC for different bias currents

5.2 Integration in the test chip

5.2.1 Complete ADC system

A test chip has been designed to evaluate the functionality and performance of the proposed VCO based ΣΔ ADC. The goal of the test chip is to be able to debug and characterize the sub-circuits and ADC. Thus, the ADC was implemented with different design variants for each functional sub-circuit, to make sure there could be a selection between these variants. The blue blocks in the figure 5.17 are the nominal blocks designed for the MEA that have been discussed so far. The red blocks in the 5.17 have been designed with a similar specification but without any size restrictions. For example, 'G_m 2' and 'HPF 2' are too large to integrate in the pixel as it would deteriorate the spatial resolution. However, we want to have these alternatives to see the extent of noise we can attenuate with larger AFE. This could provide design insights about the performance of an SM MEA implemented using such readout architecture.

A digital interface based on a shift register has been designed to control hundreds of digital lines needed to enable and select these sub-circuit variants in the test chip. The relevant voltages and currents needed for biasing can be trimmed using the current and voltage DACs in the biasing block. The current trimming can be done with an accuracy of ±20%. Three bidirectional test-points, to measure most of the relevant voltages and currents and characterize main sub-circuits, have been

used.

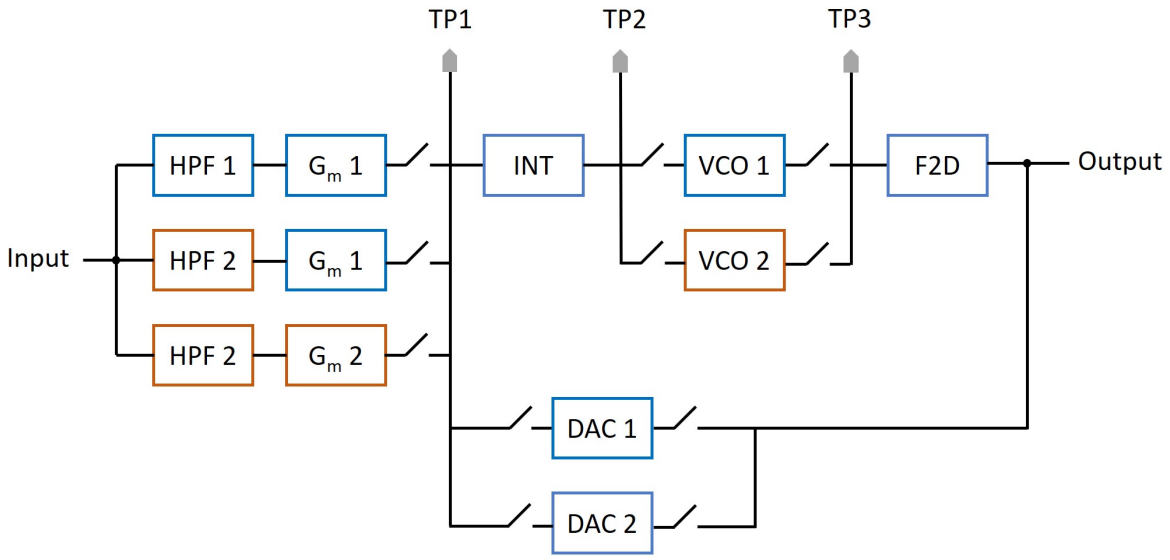


Figure 5.17: Implemented ADC system including alternative designs for the key sub-circuits and several test-points for characterization and debugging.

5.2.2 Pseudo-differential system

The proposed readout architecture has been optimized, area- and noise-wise, to be integrated as a part of the MEA. However, we are not designing an MEA due to the limitations in the modules offered by the foundry, in this run and time, for this test chip. Implementing a single readout channel in the test chip has a potential disadvantage compared to the MEA configuration. For example, the input stage will be very sensitive to power supply noise, since the current generated by the transconductor depends on the V_{SG}, which is V_{DD}-V_{in}. In the MEA array, this noise would be common to all the input stages, which can be compensated in the post-processing step. In the single readout channel, this noise is indistinguishable from the intrinsic noise. Hence, to make sure the intrinsic noise of the readout channel can be distinguished from the supply noise or other interferences, two identical ADC channels have been included in the test chip, which can work independently or in a pseudo-differential configuration. With the possibility to record both the readout channels simultaneously, the single-channel measurements can be compared with the pseudo-differential measurement to evaluate the influence on common noise.

Figure 5.18 shows the pseudo-differential operation of the readout channels which pick-up the noise from the common supply (VDD). The off-ship digital signal processor (DSP) post-processes and reconstructs the digital output (Y_p and Y_{ref}). The single-channel signals after reconstruction (R_p and R_{ref}) have the noise from VDD, while the difference (R_{diff}) eliminates this common noise as shown in figure 5.18.

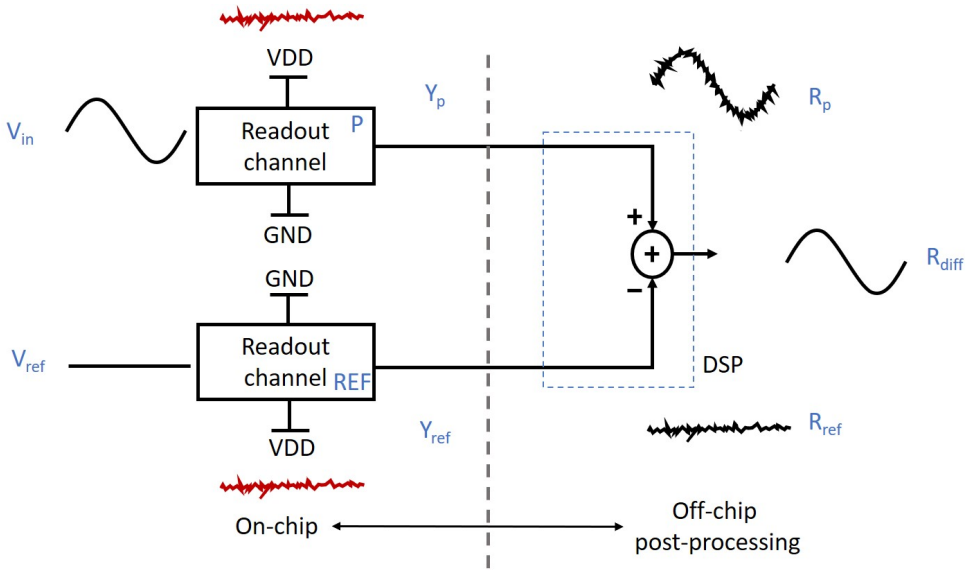


Figure 5.18: Pseudo-differential implementation of the readout channel in test chip showing the noise picked-up from VDD (spikes), the post-processed signals for single-ended channels (R_p, R_{ref}) and signal after common noise compensation (R_{diff}).

5.3 Layout

The layout of the individual ADC sub-blocks has been implemented abiding the design rule check (DRC) and layout vs. schematic (LVS) check. The most sensitive blocks, such as VCO, have been simulated in post-layout, and parasitic capacitances, have been compensated in layout. Since the foundry offered a maximum of 6 metal layer stack for the implementation of this test chip on a multi-project wafer (MPW), the highest (topmost) metal used to design the sub-blocks was limited to metal-2 or metal-3 in case of complex layouts. To avoid the complexity in integrating the layout of these sub-blocks in the full ADC layout and test chip, the even metals (metal-2, metal-4) have been routed horizontally while the odd metals (metal-3) have been routed vertically. The highest metal layer in the MPW, M6, was not used till the last step of the ADC layout, which is to route the final local supplies (VDD) and local ground(s) (GND) with the thick metal-6 metal. This metal is especially thick and has very low resistance, making it perfect for supplies and inefficient for signal routing as it causes congestion.

Since this is a mixed-signal design with analog and digital sub-circuits, the layout should be carefully designed to ensure the sensitive blocks are protected from the noisy ones. The analog blocks are sensitive, while the digital blocks are noisy due to the constant switching of the transistors. Guard rings have been used for all the sub-blocks in the design to prevent undesirable interaction between the blocks. To further avoid the coupling between the analog and digital counterparts in the design, the power supplies and ground signals have been separated for the analog (VDDA, GNDA) and digital blocks (VDDD, GNDD). The analog blocks here which shared VDDA and GNDA are the input stage,

integrator, VCO (because it is a sensitive block), and the decoupling capacitors used in and near these sub-circuits. The digital blocks, F2D and DAC, shared the digital supplies VDDD and GNDD. Decoupling capacitors have been placed before the most sensitive and noisy circuits.

The layout of the implemented VCO based ADC system is shown in figure 5.19. The 'T-shaped' part is the biasing block, and the two readout channels (exact copies) have been placed symmetrically on either side of the biasing block. The individual blocks of the 'Readout channel P' are labeled in the figure. The digital inputs for the ADC system have been all routed, and the metal contacts are brought to the left part to make connections to the output of the shift register easier. The metal contacts for all the supply and ground signals (VDDA, VDDD, GNDA, GNDD) are routed to have contacts on the top-side of the layout.

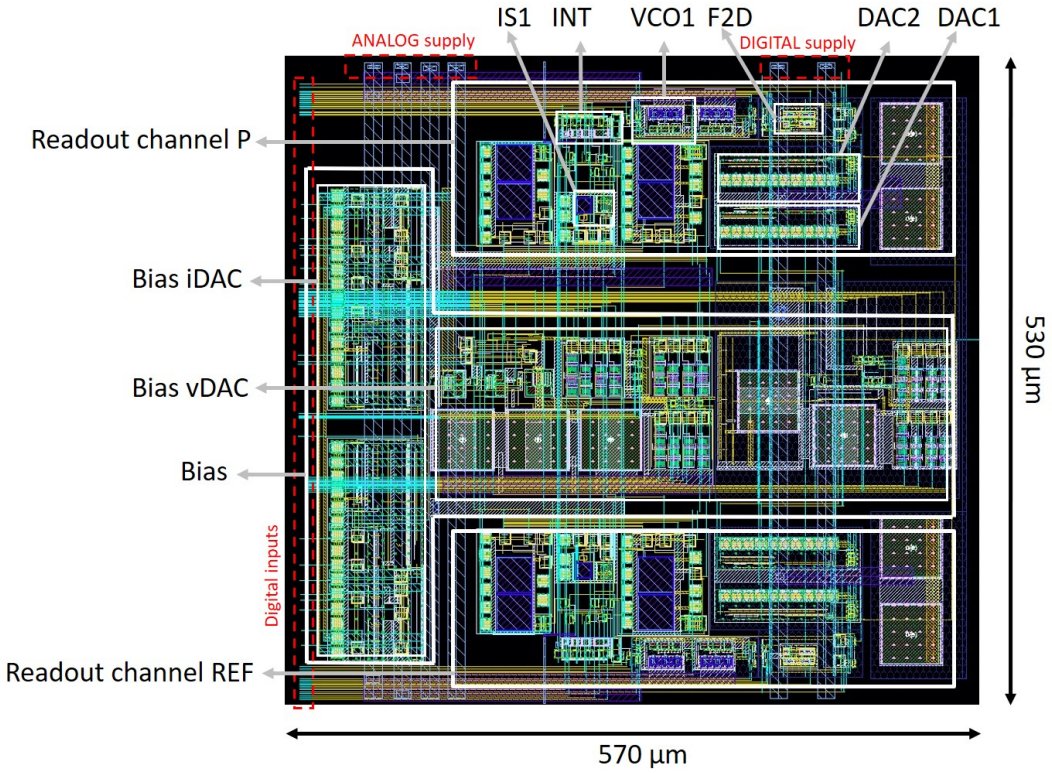


Figure 5.19: Layout of the pseudo-differential readout channels. The ADC blocks that have been optimized for MEA implementation are marked, along with the current (iDAC) and voltage DACs (vDAC) used for biasing.

The total area of this pseudo-differential readout system implemented in the test chip is 530 x 570 μm^2, including the biasing blocks, two readout channels, and the many switches and variants implemented in the ADCs. The pixel dimensions are estimated to be 17 x 17 μm^2 based on the layout, ensuring the possibility of implementing this ADC for a high-density MEA with sub-cellular spatial resolution. The full ADC area, including the input stage, could be potentially shrunk down to 45 x 45 μm^2.

5.3.1 Post-layout simulations

Post-layout simulations have been performed to ensure that the parasitic resistances and capacitances present after designing the layout do not affect the functionality and performance of the actual design. Simulations with the analog extracted view with the parasitic resistances and capacitances for a bias current of 800 nA have been done. To observe the functionality of pseudo-differential implementation, the REF-channel input is set to 0 V, while a sinusoidal input with a voltage of 100 μV and a frequency of 5 kHz has been given to P-channel. The PSD plots obtained for a post-layout are shown in figure 5.20. The noise obtained during these simulations is tabulated in table 5.14. However, the value of differential noise obtained from post-layout simulations is pessimistic because the number of points in the FFT (figure 5.20) for low frequencies is not sufficient, especially at the beginning of the signal band, to evaluate the exact noise even after week-long simulations.

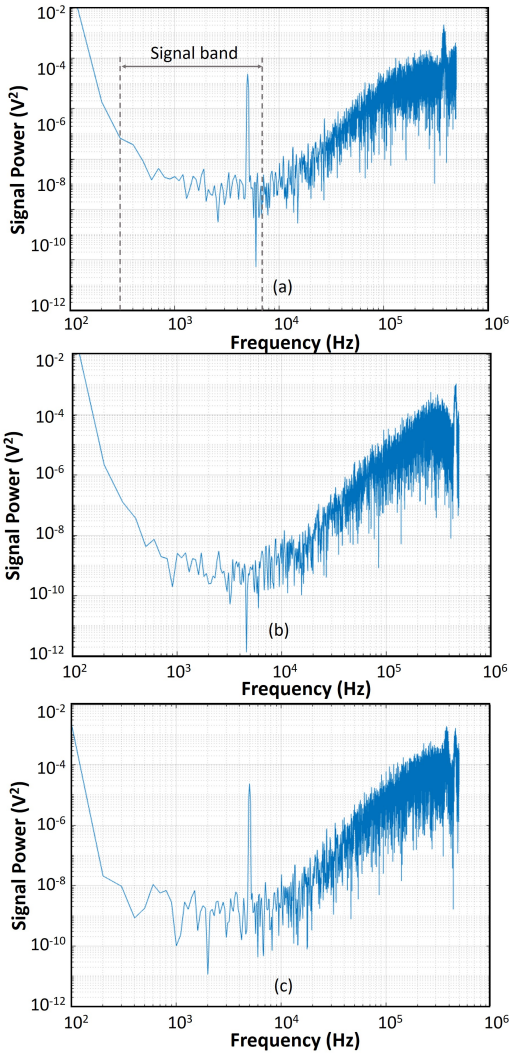


Figure 5.20: PSD obtained from one of the post-layout simulation for a bias current of 800 nA showing (a) the output of P-channel, (b) output of reference channel, and (c) differential noise (post-processed)

	Noise (μV_{RMS})	
	Simulation 1	Simulation 2
P channel	5.85	4.67
REF channel	5.58	5.37
Differntial	4.86	4.4

Table 5.14: Noise obtained from post-layout simulations

Nevertheless, the post-layout simulations show hopeful results and ensure that the functionality and performance of the designed readout channel are not degraded after the implementation (layout) phase. Short post-layout simulations were also run for sensitive sub-blocks such as VCO and input stage, to ensure their performance.

5.4 Conclusion

In this chapter, the block-by-block circuit-level implementation of the VCO based ADC had been discussed. The design concepts, considerations, and flow during the implementation were explained. Each block implementation started off with the design and optimization in Cadence, followed by the evaluation and analysis of results and then validating the robustness of the blocks through corners and Monte Carlo analysis (where necessary). After all the blocks have been designed to meet the specific requirements and functionality, they have been integrated into the full ADC system, according to the system level implementation presented in the previous chapter. The results obtained for the implemented ADC schematic was evaluated for different bias currents.

To characterize, debug, and test the validity of the designed ADC for MEA applications, design variants, and test-points have been incorporated. The ADC has been implemented as a pseudo-differential system (2 readout channels, P and REF) in this test chip, considering that when implemented in an MEA, there will never be a single channel, but instead, there will be several channels making it possible to remove the common noise picked up by the channels. After the schematic design, the layout level implementation of each block has been done abiding by the DRC and LVS. The design rules adhered to while implementing this mixed-signal design layout has been discussed. Post-layout simulations have been performed to validate the functionality and performance of the layout-level implementation.

The second-order noise shaping that has been aimed for has been observed in both the schematic and post-layout simulations. The noise obtained from each channel in the pseudo-differential system and the noise after compensating the common noise component has been presented. The performance of this ADC (single channel) is being gauged by the noise since the idea was to develop a low-noise ADC for APS MEAs. A noise in the range of 3 to 7 μV_{RMS} has been obtained per channel

depending on the choice of bias current during schematic-level simulations. For bias currents above 800 nA, the noise obtained is less than 4.2 μV_{RMS}. The post-layout simulation for a bias current of 800 nA revealed that the performance of the readout channel is preserved. The power consumption of the readout channel is in the range of 1 to 3 μW. The estimated pixel dimensions for an MEA implemented with these channels are under 17 x 17 μm^2, showing the scope of high-resolution high-density MEA implementation. The area of the readout channel is under 0.003 mm^2 (45 x 45 μm^2), showing the possibility of having thousands of parallel readout channels which can provide a full-frame readout.

6 Discussion

In this chapter, the research question and goal of this thesis is reiterated to center the discussion on the results obtained, challenges faced, and future recommendations around this. The thesis aims to design a low-noise readout system which can be used to implement full-frame APS MEAs with high spatial resolution. The constraint on the pixel dimension forces the implementation of AFE using small transistors. The problem with small transistors is that the flicker noise will be high, deteriorating the signal quality of the recorded signal. The integration of AFE with large transistors deteriorates the spatial resolution of the MEA. These design trade-offs are shown in figure 6.1. For this reason, most of the APS MEAs implemented so far have a 'dual-mode operation' where low-noise readout is achieved for selected electrodes due to the additional AFE stage in the readout channels implemented with the large transistors.

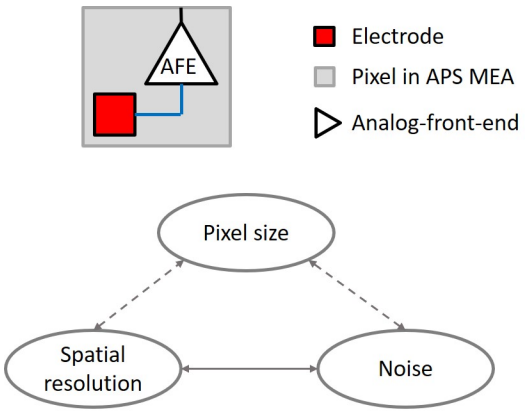


Figure 6.1: Trade-offs in APS full-frame readout MEA

Most state-of-the-art APS MEAs use SAR ADC architecture because of their high accuracy and low power consumption, making them perfect for data acquisition applications. However, the high accuracy in SAR ADCs comes from the hardware complexity, which is undesirable for implementing thousands of parallel readout channels. Time multiplexing approaches have been used to overcome the limitation of the reduced number of ADCs, which in turn requires additional circuitry such as anti-aliasing filters to be integrated in the pixel area [35]. The other candidate in the race is sigma-delta ADC, which trades-off bandwidth for low quantization noise. The oversampling nature of these ADCs resulting in 'noise-shaping,' which reduces the quantization noise in the signal bandwidth, which in our case is less (300 Hz - 7 kHz), making the bandwidth-noise trade-off feasible. Another advantage of

ΣΔ ADCs over SAR ADCs is that they do not need complicated anti-aliasing filters because of their oversampling nature. Given these advantages, ΣΔ has been chosen to be the design choice in this thesis.

For higher-order noise shaping, higher-order implementation of the ΣΔ ADCs is required. However, the traditional way of increasing the order of the ΣΔ would mean complex hardware (circuitry) implementation, which again increases power and area consumption. To bypass this issue, a time-encoding approach has been chosen in this thesis for increasing the order of noise shaping with minimum circuit complexity. The proposed readout system is shown in figure 6.3. Instead of having a multi-stage AFE, a compact HPF and a simple PMOS transconductor have been designed with optimum noise and area performance. The filtered electrode voltage is converted into current (I_{out}) by this transconductor, which is sent to the VCO based ΣΔ modulator, which would be outside the array in the target MEA. The VCO based quantizer used in the ΣΔ modulator improves the SQNR of the ADC by enhancing the order of noise-shaping, thereby shifting the noise outside the signal band. This VCO quantizer has been implemented using a 3-stage ring oscillator that modulates the voltage at the integrator to frequency oscillation (w_{osc}). The frequency-to-digital block converts this oscillation into a digital signal (Y_{out}). The 1-bit current DAC implemented for the negative feedback in the ΣΔ modulator is inherently linear and rather compact. The system realized using these simple blocks has been designed and simulated to evaluate its performance and application for APS MEAs.

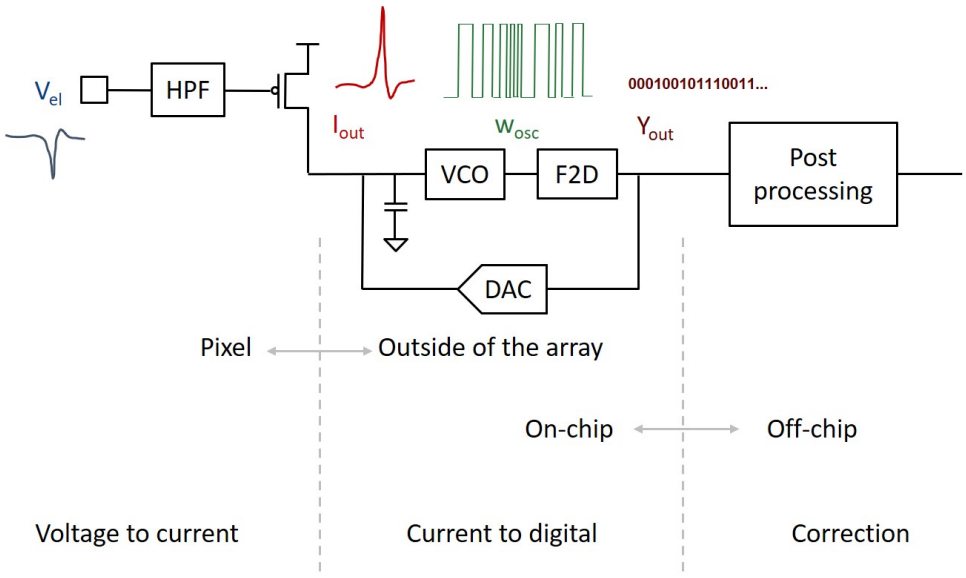


Figure 6.2: Oscillator based ΣΔ ADC

This oscillator based ΣΔ ADC has been designed in three steps: the system-level implementation using Simulink, the circuit-level implementation in Cadence, and finally, the layout level implementation. The noise performance of these implementations has been analyzed using post-processing done in MATLAB. The system-level simulations show that VCO based ΣΔ ADC provides a higher-order noise

shaping, resulting in an SQNR of 63 dB using simple blocks such as 1-bit DAC and a VCO quantizer instead of complex multi-bit DACs and quantizers, saving area and power consumption. A quantization noise of 1.02 μV_{RMS} was attained with system-level optimization leaving enough margin for the thermal and flicker noises that would appear during circuit-level implementation. Given the power budget of the ADC, four different bias current variants (200 nA, 400 nA, 800 nA, 1.2 μA) have been chosen for the ADC implementation in the test chip. The next design step would be to translate this system-level design into transistor-level, which has been explained in chapter chapter 5. A noise in the range of 3 μV_{RMS} to 7 μV_{RMS} has been obtained from the readout channel, in the AP band depending on the bias currents chosen. Using bias currents above 800 nA for the final MEA implementation could result in a noise that is less than 4.2 μV_{RMS} in the AP band. The power consumed by the readout channel is in the range of 1 to 3 μW.

The designed readout channel has been integrated on the test chip using different design variants, bidirectional test-points, and a digital block to handle the bits, to have an option to debug and characterize each sub-circuit of the readout channel. A pseudo-differential implementation of this readout channel has been designed in this test chip to eliminate the common noise, which will not be an issue during the multi-channel implementation in the actual MEA. Mixed-signal layout design for this readout channel system for test chip has been designed, and post-layout simulations have been carried out to confirm the validity of this low-noise ADC performance. These results ensure the functionality and performance of the designed ADC. The comparison of this readout architecture, with the state-of-the-art readout technologies used for bio-signal recordings, is shown in table 6.1. The schematic simulation results obtained for 800 nA and 1.2 μA have been used for this comparison.

	[75]	[33]	[47]	[76]	[35]	[36]	This work	
Year	2019	2017	2017	2017	2018	2017		
Technology (nm)	130	130	180	65	180	180	180	
Input signal	EAP, LFP	EAP, LFP	EAP	EAP	EAP, LFP	EAP, LFP	EAP	
Pixel size (μm^2)	16 x 16	12 x 12	25.5 x 25.5	-	18 x 18	13.5 x 13.5	17 x 17	
Type of ADC	SAR	SAR	off-chip	ΣΔ	SAR	SAR	ΣΔ	
Channel size (mm^2)	*0.025	*0.09	-	0.006	*0.002	*0.026	0.0021	
Noise (μV_{RMS})	3.7	6.36	10.02	3.8	10.9	2.4	4.22[1]	3.17[2]
Noise band (Hz)	401 - 2.3k	300 - 10k	300 - 3k	11k	300 - 5k	300 - 10k	300 - 7k	
Power (uW)	-	49.06	-	1.2	5.9	16	2.15[1]	2.91[2]

Table 6.1: Comparison with the state-of-the-art bio-signal readout channels.

*The readout channel size is a calculated estimation from the citation (Area occupied by readout channels on die / No.of channels).
1: Bias current - 800 nA; 2: Bias current - 1.2 μA

The performance of the ADC designed, with the advantages inherited from oversampling and time-encoding techniques, is within the desired requirements. However, the design constraints associated with the implementation of this ADC in MEAs should be examined while designing the MEA system. Since only two ADC channels are implemented in this test chip, the data rate can be handled without complications for a sampling frequency of 1 MHz that has been chosen. However, in MEAs with thousands of channels, the data rate would be very high, making it difficult to handle this data. However, using high-speed FPGAs and techniques such as LVDS, these problems can be resolved [77, 78]. Another challenge in implementing this system for HD-MEA would be the complications in routing a large number of pixels to the large number of ADCs. Having thousands of channels would require thousands of metal lines running parallel to each other, which may result in a complex routing scheme, crosstalk, and increased parasitics.

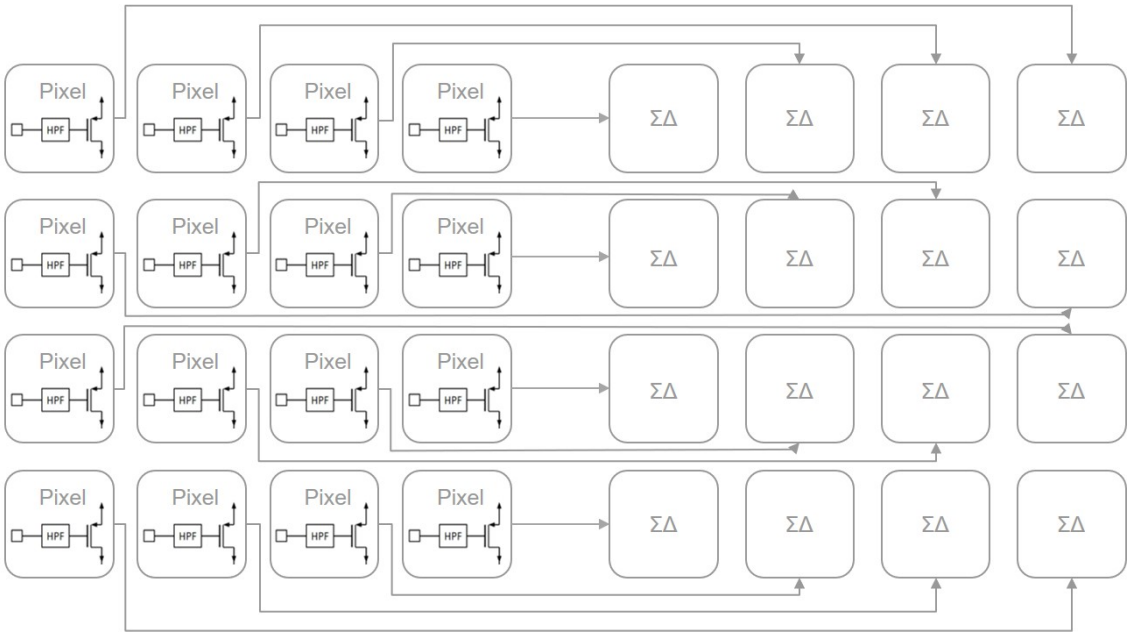


Figure 6.3: Illustration of one-on-one routing of pixel with oscillator based **ΣΔ** ADC for a 4 x 4 MEA. The target MEA aims to scale up the number of channels to approximately ten thousand.

7 Conclusion and future work

7.1 Conclusion

A VCO based ΣΔ ADC has been designed as a proof-of-concept to implement low-noise MEAs with full-readout. To achieve a high-signal quality of the readout signal, we need the analog front-end circuitry closer to the electrodes to amplify and filter the signal. Depending on the size of the AFE, the pixel size increases, thereby reducing the spatial resolution of the system. In this thesis, we propose a simple readout system that can offer low-noise performance, which does not require a large area to implement. The input stage of the readout channel, integrated into the pixel, consists of a PMOS transistor which converts the electrode voltage to current. The choice of the PMOS transistor has bee made owing to its lower flicker noise. The HPF implemented by a pseudoresistor and capacitor with a reasonable size is used in the input stage to remove the low-frequency voltage drift. Together, these components made up the pixel within 17 x 17 μm^2 area, ensuring the possibility of implementing an MEA with high-spatial resolution.

In order to implement a low-noise ADC in a small area, time-encoding based ΣΔ ADC has been designed. The VCO based ΣΔ ADC has been implemented using simple blocks such as VCO, F2D, and a 1-bit current DAC. A second-order noise-shaping has been obtained using the proposed ADC without having to use complex circuitry that is typically used for higher-order ΣΔ ADCs. For integration in test chip, a system where different designs variants of the sub-circuits and bidirectional probes, to characterize some of the important blocks, has been implemented. To be able to remove the common noise during post-processing similar to the MEA implementation scenario, a pseudo-differential readout channel system has been implemented in the test chip. The noise obtained through simulations shows promising results where a noise as low as 5 μV_{RMS} can be obtained (depending on the choice of bias current).

7.2 Future work

With the simulated performances obtained for VCO based ΣΔ ADC, the following recommendations can be made for future work.

- The circuit impairments have taken into account the possible non-idealities from each sub-block, which can be individually characterized using test-point in the test chip to measure these non-idealities and improve the design of these blocks accordingly.

- The different design variants will be tested to find and evaluate the best possible design parameters needed to implement this ADC in the MEA. The post-layout results did not provide enough points on FFT to accurately analyze the exact noise even after very long simulations. So, the best bias current need for optimum noise performance can be evaluated through measurements on the chip, which yield results in less than a minute.

- The output data rate obtained from the calculated number of channels would probably be in Gbps for a high-channel count (for example, ten thousand). An LVDS block which can allow handing these high data rates should be designed. The data rate can be reduced if necessary, by reducing the sampling frequency to an extent where the desired noise specifications are still met.

A SQNR of ADCs

For an N-bit ADC with V_{in} and V_{ref} as the analog and reference signals respectively, the analog to digital equivalence can be given by,

$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + ... + b_N 2^{-N}) = V_{in}$$

where b_1 is the most significant bit (MSB) and b_N is the least significant bit (LSB) [60]. N is the resolution of the ADC, given by the number of bits used to discretize the analog signal. An N-bit resolution means that the data converter can resolve 2^N analog values distinctly. However, it is not an indicator of the accuracy of the converter but rather a value that defines the number of output bits. The value of the coefficients b_1, b_2,...., b_N is either 0 or 1 (binary). V_{LSB} is defined as the change in voltage when the lowest significant bit is changed.

$$V_{LSB} = \frac{V_{ref}}{2^N}$$

The performance of an ADC is characterized by the signal-to-quantization noise ratio (SQNR) and the bandwidth. The SQNR of the ADC is affected by the quantization error while the sampling rate characterizes the bandwidth.

A.1 Nyquist converters

To calculate the SQNR of Nyquist ADC, we first assume that the quantization noise is stochastic, and the input signal is varying such that this noise is uniformly distributed between $-V_{LSB}/2$ and $+V_{LSB}/2$ [60]. The probability density function of the quantization error signal ($f_{QE}(x)$) after this assumption, is shown in the figure A.1.

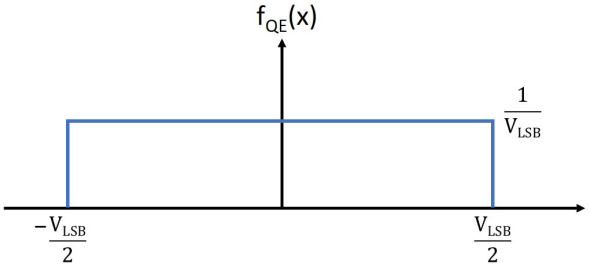


Figure A.1: Probability density function of quantization error

Since the total probability should be equal to 1, the height of the probability density function between $\pm$ $V_{LSB}/2$ will be equal to $1/V_{LSB}$. This makes the RMS value of the quantization error,

$$V_{\mathrm{QE,RMS}} = \sqrt{\int_{-\infty}^{\infty} x^2 f_{\mathrm{QE}}(x)dx} = \sqrt{\frac{1}{V_{\mathrm{LSB}}}\left(\int_{-V_{\mathrm{LSB}/2}}^{V_{\mathrm{LSB}/2}} x^2 dx\right)} = \frac{V_{\mathrm{LSB}}}{\sqrt{12}}$$

when the quantization noise is uniformly distributed in the interval of $\pm V_{LSB}/2$. Since $V_{LSB} = V_{ref}/2^N$, where N is the number of bits of resolution of the ADC, for each additional bit there is a 6 dB decrease of noise power. If the input signal (V_{in}) is sinusoidal in nature, the RMS value of the signal would be $V_{ref}/2\sqrt{2}$ resulting in an SQNR of,

$$SQNR = 20log\left(\frac{V_{\mathrm{in,RMS}}}{V_{\mathrm{QE,RMS}}}\right) = 20log\left(\frac{V_{\mathrm{ref}}/2\sqrt{2}}{V_{\mathrm{LSB}}/\sqrt{12}}\right) = 20log\left(\sqrt{\frac{3}{2}}2^N\right)$$
$$= 6.02N + 1.76\,dB$$

which shows that the SQNR improves with the increase in number of quantizer bits. However, this equation shows the best possible value of SQNR for an N-bit ADC converter. The idealized SQNR is less than this best possible value, and the input voltage where SQNR is maximum corresponds to the full-scale value [60].

A.2 Oversampled converters

The quantizer can mathematically be modeled as shown in the figure A.2a, where x(n) is the input signal value, y(n), is the output that is also the closest quantized value of x(n), and e(n) is the quantization error [60].

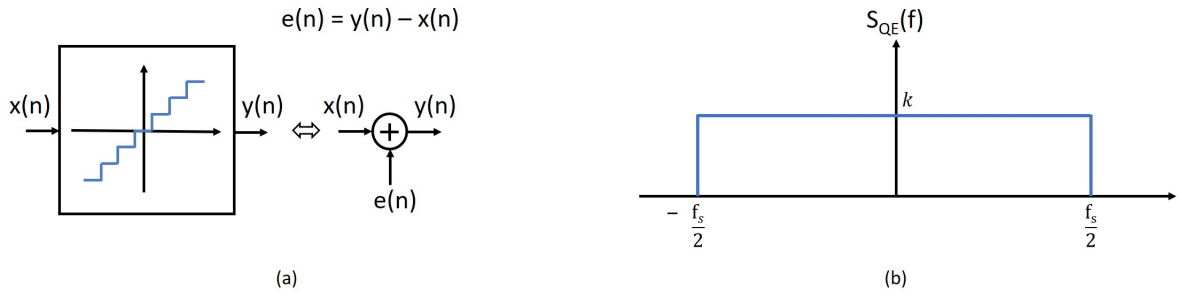


Figure A.2: (a) Linear model of a quantizer where e(n) is the error obtained during quantization (b) Power spectral density ($S_{QE}(f)$) of quantization noise

As stated in the previous section, quantization noise can be assumed as white noise and the two-sided noise power spectral density ($S_{QE}(f)$) can be modelled as shown in the figure A.2b. It can be seen from the previous section that the noise power of the quantization error is $V_{LSB}{}^2/12$ and is independent of the sampling frequency. The spectral density height value can be thus obtained from,

$$P_{QE} = \int_{-f_s/2}^{f_s/2} S_{QE^2}(f)df = \int_{-f_s/2}^{f_s/2} k^2 df = k^2 f_s = V_{LSB}{}^2/12$$

$$\Rightarrow k = \left(\frac{V_{LSB}}{\sqrt{12}}\right)\sqrt{\frac{1}{f_s}}$$

When the signals are sampled at a very high frequency ($f_s \gg f_0$), the oversampling ratio (OSR) is given by,

$$OSR = \frac{f_s}{2f_0}$$

where $2f_0$ is the Nyquist frequency. Assuming the input signal is a sine wave, the maximum peak value without clipping is $2^N(V_{LSB}/2)$. The signal power P_s of the sinusoidal wave is given by,

$$P_S = \left(\frac{2^N V_{LSB}}{2\sqrt{2}}\right)^2$$

After quantization, the output is filtered by a digital filter (D_F) to eliminate the quantization noise along with other signals greater than the outside the signal bandwidth (f_0) as shown in the figure A.3. This reduces the quantization noise power to,

$$P_{QE} = \int_{-f_s/2}^{f_s/2} S^2{}_{QE}(f)|D_F(z)|^2 df = \int_{-f_0}^{f_0} k^2 df = \frac{2f_0}{f_s}\frac{(V_{LSB})^2}{12} = \frac{(V_{LSB})^2}{12}\left(\frac{1}{OSR}\right)$$

improving the SQNR to,

$$SQNR_{\max} = 10log_{10}\left(\frac{3}{2}2^{2N}\right) + 10log_{10}(OSR)$$
$$= 6.02N + 1.76 + 10log_{10}(OSR)$$

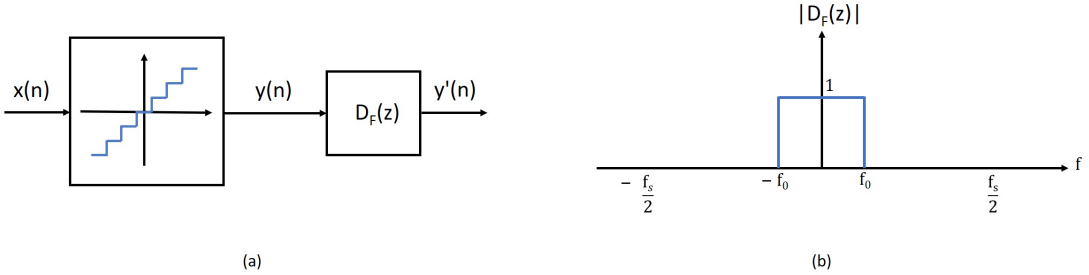


Figure A.3: (a) Block diagram with the digital filter implemented to eliminate quantization noise outside the signal band (b) Transfer function of the digital filter

A.3 First order ΣΔ modulator

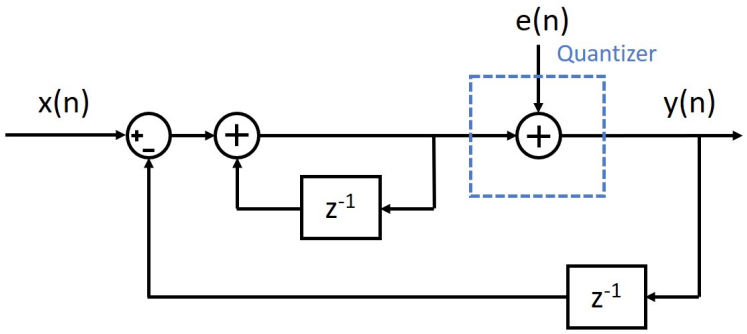


Figure A.4: Linear model of a first order **ΣΔ** data converter

The linear model of a first-order ΣΔ modulator is shown in figure A.4. The noise transfer (N(z)) for this model is $(1 - z^{-1})$, from which the quantization noise power can be calculated to be,

$$N(f) = 1 - z^{-1} = 1 - e^{-j\omega T} = 1 - e^{-j2\pi f/f_s}$$
$$= \frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j} \times 2j \times e^{-j\pi f/f_s}$$
$$= sin\left(\frac{\pi f}{f_s}\right) \times 2j \times e^{-j\pi f/f_s}$$

which gives a quantization noise power of

$$P_{\mathrm{QE}} = \int_{-f_0}^{f_0} S^2{}_{\mathrm{QE}}(f)|N(f)|^2 df = \int_{-f_0}^{f_0} \left(\frac{(V_{\mathrm{LSB}})^2}{12}\right) \frac{1}{f_{\mathrm{s}}} \left[2sin\left(\frac{\pi f}{f_{\mathrm{s}}}\right)\right]^2 df$$

which for OSR » 1 can be approximated as

$$P_{\mathrm{QE}} \approx \left(\frac{(V_{\mathrm{LSB}})^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_0}{f_{\mathrm{s}}}\right)^3 \left(\because \frac{sin(x)}{x} = 1 \quad when \quad x \to 0\right)$$

giving a signal to noise ratio of

$$SQNR_{\max} = 10log_{10}\left(\frac{P_{\mathrm{QE}}}{P_{\mathrm{S}}}\right) = 10log_{10}\left(\frac{3}{2}2^{2N}\right) + 10log_{10}\left[\frac{3}{\pi^2}(OSR)^3\right]$$
$$= 6.02N + 1.76 - 5.17 + 30log_{10}(OSR)$$

showing the improvement in SNR by $30\log_{10}(\mathrm{OSR})$ due to the first-order noise shaping.

A.4 Second order ΣΔ modulator

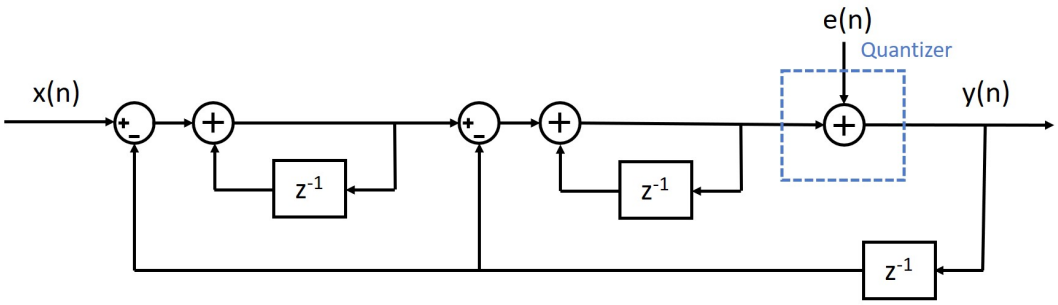


Figure A.5: Linear model of a second order ΣΔ data converter

The block diagram of a second order ΣΔ modulator is shown in the figure A.5 for which the noise transfer function is $(1 - z^{-1})^2$, from which the quantization noise power can be calculated as [60],

$$P_{\mathrm{QE}} = \int_{-f_0}^{f_0} S^2{}_{\mathrm{QE}}(f)|N(f)|^2 df = \int_{-f_0}^{f_0} \left(\frac{(V_{\mathrm{LSB}})^2}{12}\right) \frac{1}{f_{\mathrm{s}}} \left[2sin\left(\frac{\pi f}{f_{\mathrm{s}}}\right)\right]^4 df$$

$$P_{\mathrm{QE}} \approx \left(\frac{(V_{\mathrm{LSB}})^2}{12}\right)\left(\frac{\pi^4}{5}\right)\left(\frac{2f_0}{f_{\mathrm{s}}}\right)^5 \approx \frac{(V_{\mathrm{LSB}})^2\pi^4}{60}\left(\frac{1}{OSR}\right)^5$$

The maximum signal to noise ratio of a second order ΣΔ modulator is given by,

$$SQNR_{\max} = 10log_{10}\left(\frac{P_{\mathrm{QE}}}{P_{\mathrm{S}}}\right) = 10log_{10}\left(\frac{3}{2}2^{2N}\right) + 10log_{10}\left[\frac{5}{\pi^4}(OSR)^5\right]$$
$$= 6.02N + 1.76 - 12.9 + 50log_{10}(OSR)$$

showing the improvement in SNR due to the increase in the order of the ΣΔ modulation.

B Noise

B.1 Flicker and thermal noise

The most significant electronic noise sources are the thermal and flicker noise. Thermal noise which is also called as the Johnson-Nyquist noise is generated by the thermally agitated charge carriers in an electronic conductor at equilibrium and is present for any applied voltage. The spectral density of this noise is typically constant over frequency like white noise and its power is proportional to the absolute temperature. Thermal noise is the main source of noise in resistors and can be modelled as a voltage source in series with an ideal noiseless resistor as shown in the figure B.1a. The power spectral density of thermal noise is

$$V_{\text{n-R}}{}^2(f) = 4kTR$$

where k is the Boltzmann constant, T is the absolute temperature (in K) and R is the resistance (in Ohms).

Figure B.1: (a) Noise model of a resistor (b) Noise model of a MOSFET

The thermal noise is also present in MOSFETs but is more prominent at high frequencies. At low frequencies the flicker noise also known as 1/f noise dominates the thermal noise as shown in the figure B.1b. Flicker noise is generated due to the interaction between the charged carriers moving across the semiconductor. The charge carriers moving at the interface between the gate oxide and silicon substrate are randomly trapped and later released by the energy states created by the dangling bonds causing perturbations referred to as flicker noise. It varies from one technology node to another and depends on the cleanliness of the oxide substrate interface. Unlike thermal noise, flicker noise depends on the biasing conditions of the transistor. The noise in a transistor operative in the active region can

be modelled by a voltage source connected to the gate as shown in the figure above. The power spectral density calculated by combining the effects of flicker and thermal noise components is given by,

$$V_{\text{n-M}}{}^2(f) = V_{\text{tn-M}}{}^2(f) + V_{\text{fn-M}}{}^2(f) = 4kT\frac{2}{3}g_{\text{m}} + \frac{K}{WLC_{\text{ox}}f^{\alpha}}$$

where g_m is the transconductance of the MOSFET, W and L are the dimensions of the gate, C_{ox} is the gate oxide capacitance per unit area, α is a constant which is usually approximated as 1 and K is a process-dependent constant in the order of 10^{-25} V^2F. One of the parameters that is used to describe the noise is the corner frequency which is the frequency above which thermal noise dominates flicker noise as shown in the figure B.2.

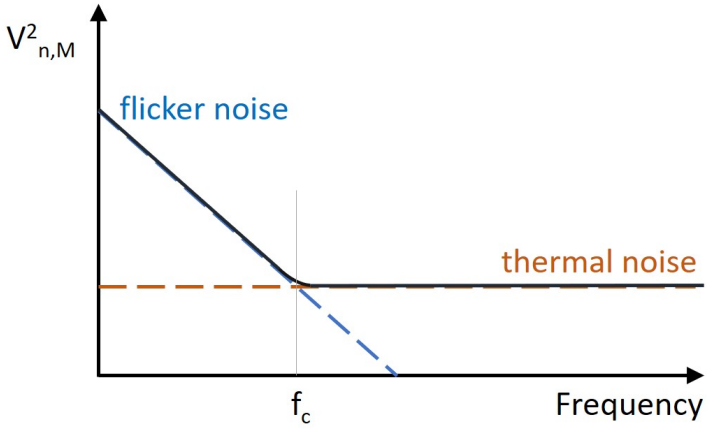


Figure B.2: Noise spectral density in MOSFETs

B.2 kT/C noise

The ideal capacitors are lossless devices which do not have thermal noise. However, when combined with the resistors in an RC circuit, the combination gives rise to kT/C noise. This noise will be present in the HPF in the input stage discussed above. The noise bandwidth of the RC circuit is given by $\Delta f = 1/(4RC)$ which when substituted in thermal noise PSD equation gives,

$$\overline{v_{\text{n}}{}^2} = \frac{4kTR}{4RC} = \frac{kT}{C}$$

Although it looks like the kT/C noise is independent of the value of resistance, this noise is only contributed by the resistor and not the capacitor. However altering the value of capacitance we can move this kT/C noise to the band that is outside our band of interest.

B.3 Phase noise

The phase noise in oscillator results in side bands in the spectrum around the fundamental oscillation (figure B.3a). According to Leeson's equation [64], the single-side band can be modelled as shown in the figure B.3b. The zoomed-in version of the side band shows different slopes of the phase noise with respect to the offset frequency. In the analysis for linear model of the VCO ADC we approximated the phase noise to have -20 dB/decade, which is in reality steeper where the effect of flicker noise is predominant and is 0 dB/decade for higher frequencies (which is debatable because the signal power cannot be infinite).

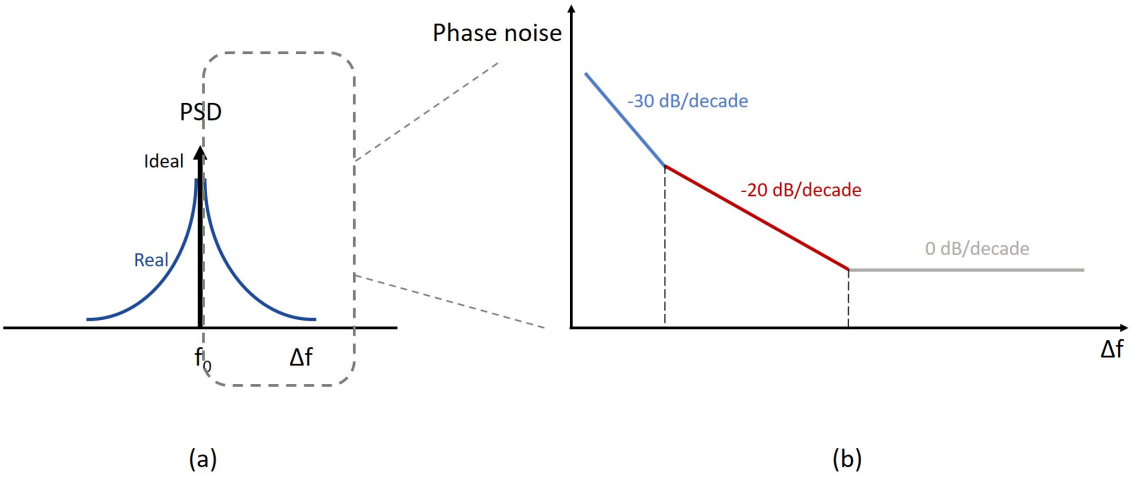


Figure B.3: Phase noise in the oscillator [64]

Bibliography

[1] C. Koch and G. Laurent, "Complexity and the nervous system," Science, vol. 284, no. 5411, pp. 96–98, 1999.

[2] A. Fornito, A. Zalesky, and E. Bullmore, Fundamentals of brain network analysis. Academic Press, 2016.

[3] I. L. Jones, P. Livi, M. K. Lewandowska, M. Fiscella, B. Roscic, and A. Hierlemann, "The potential of microelectrode arrays and microelectronics for biomedical research and diagnostics," Analytical and bioanalytical chemistry, vol. 399, no. 7, pp. 2313–2329, 2011.

[4] A. Hierlemann, U. Frey, S. Hafizovic, and F. Heer, "Growing cells atop microelectronic chips: interfacing electrogenic cells in vitro with CMOS-based microelectrode arrays," Proceedings of the IEEE, vol. 99, no. 2, pp. 252–284, 2010.

[5] M. E. J. Obien, K. Deligkaris, T. Bullmann, D. J. Bakkum, and U. Frey, "Revealing neuronal function through microelectrode array recordings," Frontiers in neuroscience, vol. 8, p. 423, 2015.

[6] G. Zorzi, M. E. J. Obien, M. Fiscella, N. Leary, and A. Hierlemann, "Automatic extraction of axonal arbor morphology applied to h-iPSC-derived neurons," in Conference Abstract: MEA Meeting 2018| 11th International Meeting on Substrate Integrated Microelectrode Arrays, Frontiers Media SA, 2018.

[7] M. S. Lewicki, "A review of methods for spike sorting: the detection and classification of neural action potentials," Network: Computation in Neural Systems, vol. 9, no. 4, pp. R53–R78, 1998.

[8] M. Ballini, J. Müller, P. Livi, Y. Chen, U. Frey, A. Stettler, A. Shadmani, V. Viswam, I. L. Jones, D. Jäckel, et al., "A 1024-channel CMOS microelectrode array with 26,400 electrodes for recording and stimulation of electrogenic cells in vitro," IEEE journal of solid-state circuits, vol. 49, no. 11, pp. 2705–2719, 2014.

[9] W. Gong, J. Senčar, D. J. Bakkum, D. Jäckel, M. E. J. Obien, M. Radivojevic, and A. R. Hierlemann, "Multiple single-unit long-term tracking on organotypic hippocampal slices using high-density microelectrode arrays," Frontiers in neuroscience, vol. 10, p. 537, 2016.

[10] S. P. Lacour, C. Tsay, S. Wagner, Z. Yu, and B. Morrison, "Stretchable micro-electrode arrays for dynamic neuronal recording of in vitro mechanically injured brain," in SENSORS, 2005 IEEE, pp. 4–pp, IEEE, 2005.

[11] T. A. Simeone, K. A. Simeone, K. K. Samson, J. M. Rho, et al., "Loss of the kv1. 1 potassium channel promotes pathologic sharp waves and high frequency oscillations in in vitro hippocampal slices," Neurobiology of disease, vol. 54, pp. 68–81, 2013.

[12] A. M. Tukker, M. W. de Groot, F. M. Wijnolts, E. E. Kasteel, L. Hondebrink, and R. Westerink, "Is the time right for in vitro neurotoxicity testing using human iPSC-derived neurons?," ALTEX-Alternatives to animal experimentation, vol. 33, no. 3, pp. 261–271, 2016.

[13] M. Hofrichter, L. Nimtz, J. Tigges, Y. Kabiri, F. Schröter, B. Royer-Pokora, B. Hildebrandt, M. Schmuck, A. Epanchintsev, S. Theiss, et al., "Comparative performance analysis of human iPSC-derived and primary neural progenitor cells (NPC) grown as neurospheres in vitro," Stem cell research, vol. 25, pp. 72–82, 2017.

[14] U. Frey, J. Sedivy, F. Heer, R. Pedron, M. Ballini, J. Mueller, D. Bakkum, S. Hafizovic, F. D. Faraci, F. Greve, et al., "Switch-matriX-based high-density microelectrode array in CMOS technology," IEEE Journal of Solid-State Circuits, vol. 45, no. 2, pp. 467–482, 2010.

[15] D. Jäckel, D. J. Bakkum, T. L. Russell, J. Müller, M. Radivojevic, U. Frey, F. Franke, and A. Hierlemann, "Combination of high-density microelectrode array and patch clamp recordings to enable studies of multisynaptic integration," Scientific reports, vol. 7, no. 1, pp. 1–17, 2017.

[16] X. Yuan, M. Schröter, M. E. J. Obien, M. Fiscella, W. Gong, T. Kikuchi, A. Odawara, S. Noji, I. Suzuki, J. Takahashi, et al., "Versatile live-cell activity analysis platform for characterization of neuronal dynamics at single-cell and network level," bioRxiv, 2020.

[17] M. Park and M. H. Perrott, "A 78 dB sndr 87 mw 20 mHz bandwidth continuous-time ΣΔ ADC with VCO-based integrator and quantizer implemented in 0.13μm CMOS," IEEE Journal of Solid-State Circuits, vol. 44, no. 12, pp. 3344–3358, 2009.

[18] F. Cardes, E. Gutierrez, A. Quintero, C. Buffa, A. Wiesbauer, and L. Hernandez, "0.04-mm^2 103-dB-a dynamic range second-order VCO-based audio ΣΔ ADC in 0.13 μm CMOS," IEEE Journal of Solid-State Circuits, vol. 53, no. 6, pp. 1731–1742, 2018.

[19] E. Prefasi, L. Hernandez, S. Paton, A. Wiesbauer, R. Gaggl, and E. Pun, "A 0.1 mm^2, wide bandwidth continuous-time ΣΔ ADC based on a time encoding quantizer in 0.13μ m CMOS," IEEE journal of solid-state circuits, vol. 44, no. 10, pp. 2745–2754, 2009.

[20] G. G. Gielen, L. Hernandez, and P. Rombouts, "Time-encoding analog-to-digital converters: Bridging the analog gap to advanced digital cmos-part 1: Basic principles," IEEE Solid-State Circuits Magazine, vol. 12, no. 2, pp. 47–55, 2020.

[21] J. Kim, T.-K. Jang, Y.-G. Yoon, and S. Cho, "Analysis and design of voltage-controlled oscillator based analog-to-digital converter," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 1, pp. 18–30, 2009.

[22] F. Cardes García, "Data acquisition techniques based on frequency-encoding applied to capacitive mems microphones," 2018.

[23] L. Berdondini, P. D. van der Wal, N. F. de Rooij, and M. Koudelka-Hep, "Development of an electroless post-processing technique for depositing gold as electrode material on CMOS devices," Sensors and Actuators B: Chemical, vol. 99, no. 2-3, pp. 505–510, 2004.

[24] G. Schmitt, J.-W. Schultze, F. Faßbender, G. Buß, H. Lüth, and M. Schöning, "Passivation and corrosion of microelectrode arrays," Electrochimica Acta, vol. 44, no. 21-22, pp. 3865–3883, 1999.

[25] T. D. Strong, H. C. Cantor, and R. B. Brown, "A microelectrode array for real-time neurochemical and neuroelectrical recording in vitro," Sensors and Actuators A: Physical, vol. 91, no. 3, pp. 357–362, 2001.

[26] T. Geninatti, G. Bruno, B. Barile, R. L. Hood, M. Farina, J. Schmulen, G. Canavese, and A. Grattoni, "Impedance characterization, degradation, and in vitro biocompatibility for platinum electrodes on biomems," Biomedical microdevices, vol. 17, no. 1, p. 24, 2015.

[27] L. Berdondini, M. Chiappalone, P. Van Der Wal, K. Imfeld, N. F. de Rooij, M. Koudelka-Hep, M. Tedesco, S. Martinoia, J. Van Pelt, G. Le Masson, et al., "A microelectrode array (MEA) integrated with clustering structures for investigating in vitro neurodynamics in confined interconnected sub-populations of neurons," Sensors and Actuators B: Chemical, vol. 114, no. 1, pp. 530–541, 2006.

[28] J. Guo, J. Yuan, and M. Chan, "Modeling of the cell-electrode interface noise for microelectrode arrays," IEEE transactions on biomedical circuits and systems, vol. 6, no. 6, pp. 605–613, 2012.

[29] M. E. J. Obien and U. Frey, "Large-scale, high-resolution microelectrode arrays for interrogation of neurons and networks," in In Vitro Neuronal Networks, pp. 83–123, Springer, 2019.

[30] O. Skorka and D. Joseph, "CMOS digital pixel sensors: technology and applications," in Nanosensors, Biosensors, and Info-Tech Sensors and Systems 2014, vol. 9060, p. 90600G, International Society for Optics and Photonics, 2014.

[31] C. M. Lopez, A. Andrei, S. Mitra, M. Welkenhuysen, W. Eberle, C. Bartic, R. Puers, R. F. Yazicioglu, and G. G. Gielen, "An implantable 455-active-electrode 52-channel CMOS neural probe," IEEE Journal of Solid-State Circuits, vol. 49, no. 1, pp. 248–261, 2013.

[32] K. Seidl, S. Herwik, T. Torfs, H. P. Neves, O. Paul, and P. Ruther, "CMOS-based high-density silicon microprobe arrays for electronic depth control in intracortical neural recording," Journal of Microelectromechanical Systems, vol. 20, no. 6, pp. 1439–1448, 2011.

[33] C. M. Lopez, J. Putzeys, B. C. Raducanu, M. Ballini, S. Wang, A. Andrei, V. Rochus, R. Vandebriel, S. Severi, C. Van Hoof, et al., "A neural probe with up to 966 electrodes and up to 384

configurable channels in 0.13 μm SOI CMOS," IEEE transactions on biomedical circuits and systems, vol. 11, no. 3, pp. 510–522, 2017.

[34] C. M. Lopez, H. S. Chun, L. Berti, S. Wang, J. Putzeys, C. Van Den Bulcke, J.-W. Weijers, A. Firrincieli, V. Reumers, D. Braeken, et al., "A 16384-electrode 1024-channel multimodal CMOS MEA for high-throughput intracellular action potential measurements and impedance spectroscopy in drug-screening applications," in 2018 IEEE International Solid-State Circuits Conference-(ISSCC), pp. 464–466, IEEE, 2018.

[35] X. Yuan, V. Emmenegger, M. E. J. Obien, A. Hierlemann, and U. Frey, "Dual-mode microelectrode array featuring 20k electrodes and high SNR for extracellular recording of neural networks," in 2018 IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 1–4, IEEE, 2018.

[36] J. Dragas, V. Viswam, A. Shadmani, Y. Chen, R. Bounik, A. Stettler, M. Radivojevic, S. Geissler, M. E. J. Obien, J. Müller, et al., "In vitro multi-functional microelectrode array featuring 59 760 electrodes, 2048 electrophysiology channels, stimulation, impedance measurement, and neurotransmitter detection channels," IEEE journal of solid-state circuits, vol. 52, no. 6, pp. 1576–1590, 2017.

[37] F. Heer, S. Hafizovic, W. Franks, A. Blau, C. Ziegler, and A. Hierlemann, "CMOS microelectrode array for bidirectional interaction with neuronal networks," IEEE Journal of Solid-State Circuits, vol. 41, no. 7, pp. 1620–1629, 2006.

[38] F. Shahrokhi, K. Abdelhalim, and R. Genov, "128-channel fully differential digital neural recording and stimulation interface," in 2009 IEEE International Symposium on Circuits and Systems, pp. 1249–1252, IEEE, 2009.

[39] J. N. Aziz, K. Abdelhalim, R. Shulyzki, R. Genov, B. L. Bardakjian, M. Derchansky, D. Serletis, and P. L. Carlen, "256-channel neural recording and delta compression microsystem with 3d electrodes," IEEE Journal of Solid-State Circuits, vol. 44, no. 3, pp. 995–1005, 2009.

[40] G. N. Angotzi, M. Malerba, F. Boi, E. Miele, A. Maccione, H. Amin, M. Crepaldi, and L. Berdondini, "A synchronous neural recording platform for multiple high-resolution CMOS probes and passive electrode arrays," IEEE transactions on biomedical circuits and systems, vol. 12, no. 3, pp. 532–542, 2018.

[41] B. Johnson, S. T. Peace, T. A. Cleland, and A. Molnar, "A 50μm pitch, 1120-channel, 20kHz frame rate microelectrode array for slice recording," in 2013 IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 109–112, IEEE, 2013.

[42] L. Berdondini, K. Imfeld, A. Maccione, M. Tedesco, S. Neukom, M. Koudelka-Hep, and S. Martinoia, "Active pixel sensor array for high spatio-temporal resolution electrophysiological recordings from single cell to large scale neuronal networks," Lab on a Chip, vol. 9, no. 18, pp. 2644–2651, 2009.

[43] A. Maccione, A. Simi, T. Nieus, M. Gandolfo, K. Imfeld, E. Ferrea, E. Sernagor, and L. Berdondini, "Sensing and actuating electrophysiological activity on brain tissue and neuronal cultures with a high-density CMOS-MEA," in 2013 Transducers & Eurosensors XXVII, pp. 752–755, IEEE, 2013.

[44] G. Bertotti, D. Velychko, N. Dodel, S. Keil, D. Wolansky, B. Tillak, M. Schreiter, A. Grall, P. Jesinger, S. Röhler, et al., "A CMOS-based sensor array for in-vitro neural tissue interfacing with 4225 recording sites and 1024 stimulation sites," in 2014 IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings, pp. 304–307, IEEE, 2014.

[45] B. Eversmann, M. Jenkner, F. Hofmann, C. Paulus, R. Brederlow, B. Holzapfl, P. Fromherz, M. Merz, M. Brenner, M. Schreiter, et al., "A 128× 128 CMOS biosensor array for extracellular recording of neural activity," IEEE Journal of Solid-State Circuits, vol. 38, no. 12, pp. 2306–2317, 2003.

[46] J. Ogi, Y. Kato, Y. Matoba, C. Yamane, K. Nagahata, Y. Nakashima, T. Kishimoto, S. Hashimoto, K. Maari, Y. Oike, et al., "Twenty-four-micrometer-pitch microelectrode array with 6912-channel readout at 12 kHz via highly scalable implementation for high-spatial-resolution mapping of action potentials," Biointerphases, vol. 12, no. 5, p. 05F402, 2017.

[47] D. Tsai, D. Sawyer, A. Bradd, R. Yuste, and K. L. Shepard, "A very large-scale microelectrode array for cellular-resolution electrophysiology," Nature Communications, vol. 8, no. 1, pp. 1–11, 2017.

[48] E. Lopez-Morillo, R. G. Carvajal, F. Muñoz, H. El Gmili, A. Lopez-Martin, J. Ramirez-Angulo, and E. Rodriguez-Villegas, "A 1.2-V 140-nW 10-bit sigma delta modulator for electroencephalogram applications," IEEE transactions on biomedical circuits and systems, vol. 2, no. 3, pp. 223–230, 2008.

[49] C.-H. Hsiao, W.-L. Chen, and C.-C. Hsieh, "A 0.8 V 80.3 dB sndr stage-shared $\Delta\Sigma$ modulator with chopper-embedded switched-opamp for biomedical application," in 2012 IEEE Asian Solid State Circuits Conference (A-SSCC), pp. 253–256, IEEE, 2012.

[50] F. Cannillo, E. Prefasi, L. Hernández, E. Pun, F. Yazicioglu, and C. Van Hoof, "1.4 V 13 μW 83 dB DR CT-$\Sigma\Delta$ modulator with dual-slope quantizer and pwm dac for biopotential signal acquisition," in 2011 Proceedings of the ESSCIRC (ESSCIRC), pp. 267–270, IEEE, 2011.

[51] J. Garcia, S. Rodriguez, and A. Rusu, "A low-power ct incremental 3rd order$\Sigma\Delta$ ADC for biosensor applications," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, no. 1, pp. 25–36, 2012.

[52] E. Farshidi and N. Alaei-Sheini, "A micropower current-mode sigma-delta modulator for biomedical applications," in 2009 IEEE 17th Signal Processing and Communications Applications Conference, pp. 856–859, IEEE, 2009.

[53] M. Rezaei, E. Maghsoudloo, M. Sawan, and B. Gosselin, "A 110-nW in-channel sigma-delta converter for large-scale neural recording implants," in 2016 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), pp. 5741–5744, IEEE, 2016.

[54] D. De Dorigo, C. Moranz, H. Graf, M. Marx, B. Shui, M. Kuhl, and Y. Manoli, "A fully immersible deep-brain neural probe with modular architecture and a delta-sigma ADC integrated under each electrode for parallel readout of 144 recording sites," in 2018 IEEE International Solid-State Circuits Conference-(ISSCC), pp. 462–464, IEEE, 2018.

[55] M. Bakula, F. Ceyssens, and R. Puers, "Polymer-CMOS hybrid neural probes for large-scale neuroelectronic interfacing," in Multidisciplinary Digital Publishing Institute Proceedings, vol. 2, p. 1066, 2018.

[56] J. G. Rocha, G. Minas, and S. Lanceros-Mendez, "Pixel readout circuit for X-ray imagers," IEEE Sensors Journal, vol. 10, no. 11, pp. 1740–1745, 2010.

[57] R. Figueras, J. Sabadell, L. Terés, and F. Serra-Graells, "A 70-μm pitch 8-μW self-biased charge-integration active pixel for digital mammography," IEEE transactions on biomedical circuits and systems, vol. 5, no. 5, pp. 481–489, 2011.

[58] Z. Ignjatovic, D. Maricic, and M. F. Bocko, "Low power, high dynamic range CMOS image sensor employing pixel-level oversampling $\Sigma\Delta$ analog-to-digital conversion," IEEE Sensors Journal, vol. 12, no. 4, pp. 737–746, 2011.

[59] A. Mahmoodi, J. Li, and D. Joseph, "Digital pixel sensor array with logarithmic delta-sigma architecture," Sensors, vol. 13, no. 8, pp. 10765–10782, 2013.

[60] T. C. Carusone, D. A. Johns, and K. W. Martin, "Analog integrated circuit design [m]. john wiley&sons," 2011.

[61] W. Bai, Y. Wang, and Z. Zhu, "A 0.8-V 1.7-μW 25. 9-fJ continuous-time sigma-delta modulator for biomedical applications," in 2016 IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 248–251, IEEE, 2016.

[62] J. A. Cherry and W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 46, no. 6, pp. 661–676, 1999.

[63] R. Schreier and B. Zhang, "Delta-sigma modulators employing continuous-time circuitry," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 43, no. 4, pp. 324–332, 1996.

[64] D. Lesson, "A simple model of feedback oscillator noise spectrum," proc. IEEE, vol. 54, no. 2, pp. 329–330, 1966.

[65] F. Cardes, A. Quintero, E. Gutierrez, C. Buffa, A. Wiesbauer, and L. Hernandez, "Sndr limits of oscillator-based sensor readout circuits," Sensors, vol. 18, no. 2, p. 445, 2018.

[66] K. Lee, Y. Yoon, and N. Sun, "A scaling-friendly low-power small-area ΣΔ ADC with VCO-based integrator and intrinsic mismatch shaping capability," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 5, no. 4, pp. 561–573, 2015.

[67] A. Iwata, N. Sakimura, M. Nagata, and T. Morie, "The architecture of delta sigma analog-to-digital converters using a voltage-controlled oscillator as a multibit quantizer," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 46, no. 7, pp. 941–945, 1999.

[68] Y. Liu, A. Urso, R. M. da Ponte, T. Costa, V. Valente, V. Giagka, W. A. Serdijn, T. G. Constandinou, and T. Denison, "Bidirectional bioelectronic interfaces: System design and circuit implications," IEEE Solid-State Circuits Magazine, vol. 12, no. 2, pp. 30–46, 2020.

[69] S. R. Norsworthy, "Effective dithering of sigma-delta modulators," in [Proceedings] 1992 IEEE International Symposium on Circuits and Systems, vol. 3, pp. 1304–1307, IEEE, 1992.

[70] F. Silveira, D. Flandre, and P. G. Jespers, "A g/sub m//i/sub d/based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota," IEEE journal of solid-state circuits, vol. 31, no. 9, pp. 1314–1319, 1996.

[71] E. Gutierrez, L. Hernandez, F. Cardes, and P. Rombouts, "A pulse frequency modulation interpretation of vcos enabling vco-adc architectures with extended noise shaping," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 2, pp. 444–457, 2017.

[72] S. Ardalan and J. Paulos, "An analysis of nonlinear behavior in delta-sigma modulators," IEEE Transactions on circuits and systems, vol. 34, no. 6, pp. 593–603, 1987.

[73] B. Razavi, Design of analog CMOS integrated circuits. Tata McGraw-Hill Education, 2002.

[74] D. Lee, K. Yoo, K. Kim, G. Han, and S. Kang, "Code-width testing-based compact adc bist circuit," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 51, no. 11, pp. 603–606, 2004.

[75] D. Jung, J. S. Park, G. V. Junek, S. I. Grijalva, S. R. Kumashi, A. Wang, S. Li, H. C. Cho, and H. Wang, "A 21952-pixel multi-modal CMOS cellular sensor array with 1568-pixel parallel recording and 4-point impedance sensing," in 2019 Symposium on VLSI Circuits, pp. C62–C63, IEEE, 2019.

[76] L. B. Leene and T. G. Constandinou, "A 0.006 mm^2 1.2μ W analog-to-time converter for asynchronous bio-sensors," IEEE Journal of Solid-State Circuits, vol. 53, no. 9, pp. 2604–2613, 2018.

[77] S. Ricci, L. Bassi, E. Boni, A. Dallai, and P. Tortoli, "Multichannel fpga-based arbitrary waveform generator for medical ultrasound," Electronics Letters, vol. 43, no. 24, pp. 1335–1336, 2007.

[78] K. Abugharbieh, S. Krishnan, J. Mohan, V. Devnath, and I. Duzevik, "An ultralow-power 10-gbits/s lvds output driver," IEEE transactions on circuits and systems I: Regular papers, vol. 57, no. 1, pp. 262–269, 2009.