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ABSTRACT

Electrons and holes confined in quantum dots define excellent building blocks for quantum emergence, simulation, and computation. Silicon and germanium are compatible with standard semiconductor manufacturing and contain stable isotopes with zero nuclear spin, thereby serving as excellent hosts for spins with long quantum coherence. Here, we demonstrate quantum dot arrays in a silicon metal-oxide-semiconductor (SiMOS), strained silicon (Si/SiGe), and strained germanium (Ge/SiGe). We fabricate using a multi-layer technique to achieve tightly confined quantum dots and compare integration processes. While SiMOS can benefit from a larger temperature budget and Ge/SiGe can make an Ohmic contact to metals, the overlapping gate structure to define the quantum dots can be based on a nearly identical integration. We realize charge sensing in each platform, for the first time in Ge/SiGe, and demonstrate fully functional linear and two-dimensional arrays where all quantum dots can be depleted to the last charge state. In Si/SiGe, we tune a quintuple quantum dot using the $N+1$ method to simultaneously reach the few electron regime for each quantum dot. We compare capacitive crosstalk and find it to be the smallest in SiMOS, relevant for the tuning of quantum dot arrays. We put these results into perspective for quantum technology and identify industrial qubits, hybrid technology, automated tuning, and two-dimensional qubit arrays as four key trajectories that, when combined, enable fault-tolerant quantum computation.

Quantum dots have been a leading candidate for quantum computation for more than two decades.[1] Furthermore, they have matured recently as an excellent playground for quantum simulation[2] and have been proposed for the design of new states of matter.[3,4] Pioneering studies on group III–V semiconductors led to proof-of-principles including the coherent control of electron spins,[5,6] rudimentary quantum simulations,[7] and signatures of emergent states such as Majorana fermions.[8] Group IV semiconductors, silicon and germanium, have the opportunity to advance these concepts to a practical level due to their compatibility with standard semiconductor manufacturing[9] and the availability of isotopes with zero nuclear spin, increasing quantum coherence for single spins by four orders of magnitude.[10] Furthermore, heterostructures built from silicon and germanium also offer a large parameter space in which to engineer novel quantum electronic devices.[11–13]

An initial advancement toward silicon quantum electronics[11] was the design of an integration scheme based on overlapping gates to build silicon metal-oxide-semiconductor (SiMOS) quantum dots.[14] This technique was later adopted in strained silicon (Si/SiGe)[15] and refined by incorporating metals with a small grain size and atomic layer deposition (ALD) for layer-to-layer isolation[16] and to enable tunable coupling between single electrons in SiMOS.[17] These developments in fabrication have led to a great body of results, including high-fidelity qubit operation[18,19] and two-qubit logic.[20–22] Controlling holes in silicon has been more challenging due to type II band alignment in strained silicon, limiting experiments to SiMOS.[23–25] Strained germanium, on the other hand,[12,26,27] exhibits type I band alignment and is thereby a viable platform in which not only electrons but also holes with light effective mass[28] can be confined[29] and coherently controlled.[30]

Here, we present the fabrication and operation of quantum dots in silicon and germanium, in linear and two-dimensional arrays. We compare integration schemes and find that while each platform has unique aspects and opportunities, the core fabrication of overlapping gates defining the nano-electronic devices is remarkably similar, thereby further accelerating the overall progress in group IV semiconductor quantum dots. In each case, fabrication starts from a silicon substrate, and integration is compatible with standard semiconductor

technology. We leverage off the Ohmic contact between quantum dots in Ge/SiGe and metals[31] to avoid the need for ion implantation and to provide a means for novel hybrid systems. We show the stability diagrams obtained by charge sensing and report double quantum dots in SiMOS, Si/SiGe, and Ge/SiGe, which can be depleted to the last charge state. Fabrication is most demanding in SiMOS due to requirements on the feature size, but we also find that the resulting devices have the smallest cross capacitance, simplifying tuning and operation. We put these results in perspective and outline a road map for quantum technology based on group IV semiconductor platforms.

Figure 1(a) schematically shows the SiMOS, Si/SiGe, and Ge/SiGe wafer stacks used in this study. The SiMOS 300 mm wafers are grown in an industrial complementary metal-oxide-semiconductor (CMOS) fab,[13,17,32] while the Si/SiGe and Ge/SiGe four-inch wafers are grown using an RP-CVD reactor (ASM Epsilon 2000).[12] Each platform is grown on a p-type natural Si wafer. The SiMOS structure consists of 1 μm intrinsic natural silicon (^{i}Si) followed by 100 nm ^{28}Si (800 ppm purity) and 10 nm SiO_2.[13] The Si/SiGe heterostructure begins with a linearly graded $Si_{1-x}Ge_x$ layer, where x ranges from 0 to 0.3. A relaxed

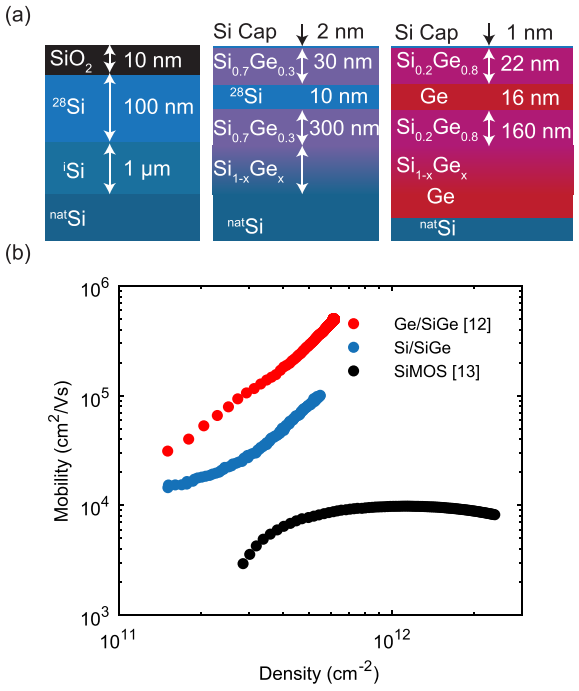

FIG. 1. Wafer stack schematics and mobility as a function of carrier density. (a) From left to right, SiMOS, Si/SiGe, and Ge/SiGe wafer stacks. For SiMOS, a ^{28}Si epilayer with 10 nm thermal oxide is grown on a 1 μm intrinsic natural Si buffer layer. The Si/SiGe heterostructure consists of a 1.5 μm linearly graded SiGe layer, a relaxed 300 nm SiGe spacer, a 10 nm ^{28}Si quantum well, a 30 nm SiGe spacer, and a 2 nm Si cap. The Ge/SiGe heterostructure consists of a 900 nm reverse graded SiGe layer, a relaxed 160 nm SiGe spacer, a 16 nm Ge quantum well, a 22 nm SiGe spacer, and a 1 nm Si cap. (b) Mobility as a function of carrier density measured in each platform. For Ge/SiGe, the peak mobility is greater than 5×10^5 cm^2/V s and the critical density is 1.15×10^{11} cm^{-2}.[12] The same measurements for Si/SiGe wafers give a peak mobility of 1×10^5 cm^2/V s and a critical density of 1.2×10^{11} cm^{-2}. SiMOS data taken from[13] shows a mobility of 1×10^4 cm^2/V s and a higher critical density of 2.5×10^{11} cm^{-2}.

$Si_{0.7}Ge_{0.3}$ layer of 300 nm lies below the 10 nm ^{28}Si (800 ppm purity) quantum well which itself is separated from the 2 nm Si capping layer by a second 30 nm relaxed $Si_{0.7}Ge_{0.3}$ spacer layer. The Ge/SiGe wafer stack starts with 1.4 μm of Ge and 900 nm of reverse graded $Si_{1-x}Ge_x$ where x ranges from 1–0.8. This lies below a 160 nm $Si_{0.2}Ge_{0.8}$ spacer layer, a 16 nm Ge quantum well under compressive strain, a second $Si_{0.2}Ge_{0.8}$ layer of 22 nm, and finally a thin Si cap of 1 nm.[12]

Figure 1(b) shows the carrier mobility vs density characterization of the three platforms. Hall bar structures were fabricated on coupons cut from the center of each wafer. Maximum mobility and critical density are extracted at 1.7 K. SiMOS 300 mm processed wafers give a peak mobility value of 1×10^4 cm^2/ V s, as well as a critical density of about 1.75×10^{11} cm^{-2} as shown in another work.[13] At higher densities, SiMOS mobilities falloff due to surface roughness scattering effects.[33–35] In Si/SiGe, we observe a lower critical density of 1.2×10^{11} cm^{-2} and a significantly higher maximum mobility exceeding 1×10^5 cm^2/ V s. Similar studies conducted on natural Si/SiGe grown in an industrial CMOS fab yielded mobilities of 4.2×10^5 cm^2/ V s.[36] This quality improvement observed by moving toward industrial CMOS fab also suggests encouraging prospects for Ge/SiGe, already exhibiting a high maximum mobility of 5×10^5 cm^2/ V s and a critical density of 1.15×10^{11} cm^{-2} despite being grown in an academic cleanroom via RP-CVD.[12]

Figure 2 summarizes the integration scheme utilized for each platform. The thermal budget is estimated based on the respective

Temperature	SiMOS	Si/SiGe	Ge/SiGe
Thermal Budget	1000 °C	750 °C	500 °C

Ohmics	SiMOS	Si/SiGe	Ge/SiGe
Dopant	P$^+$	P$^+$	-
Metal	Ti:Pt	Ti:Pt	Al
Annealing	1000 °C, 30 s	700 °C, 30 s	300 °C, 1h

Field Oxide	SiMOS	Si/SiGe	Ge/SiGe
Oxide Window	✔	(1)	(1)

Stack	All Platforms
Bondpads	SiN 150 nm
Gate Layer	Ti:Pd
Isolation	Al_2O_3 ALD

Control	SiMOS	Si/SiGe	Ge/SiGe
mw-Antenna	✔	✔	-
Micromagnet	✔	✔	-
Spin-Orbit	(2)	-	✔

FIG. 2. Overview of the fabrication scheme for SiMOS, Si/SiGe, and Ge/SiGe quantum dots. The thermal budget of each material prior to gate stack deposition is estimated based on the limiting mechanism of each platform as discussed in the text. In all cases, gates are fabricated from Pd metal with a thin (3 nm) Ti adhesion layer, with layer-to-layer isolation performed via atomic layer deposition (ALD) of Al_2O_3. These two steps can be looped at appropriate thicknesses to form the multilayer structure. (1) We note the possibility that such an etch exists for the remaining platforms in the case of a Schottky gate architecture (2) We note that spin–orbit based driving of electrons in SiMOS has been demonstrated for singlet-triplet qubits[37] and proposed for single spin qubits.[38]

limiting mechanisms. For SiMOS, thermal processing is limited by the self-diffusion of natural silicon from the substrate into the ^{28}Si epilayer. From the selfdiffusion constants measured by Bracht *et al.*,[39] we estimate the point at which the residual ^{29}Si concentration within 1 nm of the $Si - SiO_2$ interface increases by 1 ppm occurs at 1000 °C for time scales above 1 h, for furnace anneals in a pure argon atmosphere. Consequently, this allows for extensive thermal treatment and annealing of samples. This is highly advantageous, as we have observed that a 15 min anneal in forming gas at 400 °C after the deposition of every gate layer greatly improves the quality of metallic features with the smallest critical dimensions (see supplementary material Sec. I A for detailed comparison). In addition, a final end-of-line anneal is conducted to eliminate processing damage at 400 °C in forming gas for 30 min. In the cases of Si/SiGe and Ge/SiGe, the thermal budget is limited by strain relaxation of the quantum wells, thus the maximum processing thermal budget is given qualitatively by the temperature at which the quantum wells were grown. This is 750 °C for strained Si and 500 °C for strained Ge.[12]

The design of Ohmic contacts is tailored to the specific requirements of the device. For both Si platforms, an Ohmic contact is made via high fluence P ion implantation followed by evaporation of Ti:Pt metallic contacts, creating n^{++} doped, low resistance channels. The oxide (SiO_2) is etched locally directly before metal deposition using buffered hydrofluoric acid (BHF). In the case of Si/SiGe, stray capacitance is minimized to ensure maximum power is dissipated in the variable resistance of the sensing quantum dot for RF-readout. Germanium can make a direct Ohmic contact to metals,[31] avoiding the need for implants. We deposit Al and anneal at 300 °C for 1 h in a vacuum to assist in Al diffusion into the quantum well. The Al Ohmic contact is defined close to the quantum dots, resulting in a very low resistance channel ideally suited for RF circuits and enabling a tunnel contact that can even be made superconducting.[40] The implementation does however lower the thermal budget of further processing.

Fabrication of each device utilizes a titanium-palladium (Ti:Pd) gate stack with 3 nm of Ti deposited for each layer to assist with adhesion. Pd makes a good gate metal due to its small grain size.[16] Unlike the commonly used material Al, Pd does not self-oxidise and ALD can be used to define sharp dielectric interfaces. For the SiMOS and Si/SiGe devices shown in Fig. 3, we utilize a three layer gate stack that we refer to as the screening layer, the plunger layer, and the barrier layer. In order to assist climbing of overlapping gate features, the initial layer is deposited at 20 nm total thickness, while subsequent layers are deposited at 40 nm. The layers are isolated from one another via ALD of Al_2O_3 at 7 nm thickness. We measure the breakdown electric field of the Al_2O_3 to be greater than 6 MV/cm, allowing potentials of greater than 4 V to be applied between adjacent gates. To leverage off the high quality industrial CMOS fabrication facilities, we begin fabrication of SiMOS devices on wafers including a 10 nm SiO_2 oxide already grown. To further reduce the likelihood of leakage from the gate to substrate, we first grow a thick 10 nm Al_2O_3 blanket layer over the entirety of the substrate. Advantageously, one can etch Al_2O_3 on thermally grown SiO_2 selectively, allowing the definition of a 20×20 μm^2 area where the quantum dot system is defined, which we have measured to significantly reduce low-frequency drifts deduced from charge occupation stability[41] (see supplementary material Sec. I B for comparison).

The final deposition step is the qubit control layer. The spin–orbit coupling for holes in germanium enables qubit operation by simply applying microwave pulses to the quantum dot gates[30,43] and no further processing is required. In silicon, qubit driving can be realized by integrating on-chip striplines,[6,10] which we fabricate using Al or NbTiN, or micromagnets,[44] which we integrate using Ti:Co. Quantum dots in Si/SiGe generally have a larger and more mobile electron wave function as compared to SiMOS and thereby benefit most from micromagnet integration for fast qubit driving.

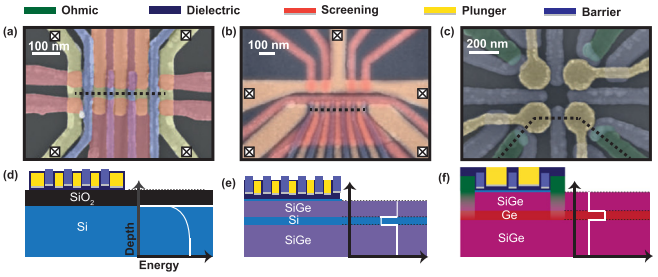

FIG. 3. Scanning electron microscope images and corresponding device schematics with band bending diagrams, substrate, and gate stack for each of the devices. The dotted lines in (a)–(c) indicate the cross section through the quantum dot channel illustrated in (d)–(f) respectively, and the crossed boxes indicate the gates that overlap with implanted regions to form Ohmic contacts. The plunger gates (yellow), the barrier gates (blue), and the screening gates (red) define the quantum dots. (a) SiMOS triple quantum dot linear array. Two SETs function as charge sensors and as reservoirs for the quantum dots on either side of the array (b) Si/SiGe quintuple quantum dot linear array. Two SETs (top) are used for charge sensing. (c) Ge/SiGe (2×2) quadruple quantum dot array. Each quantum dot is tunnel coupled to a metallic lead (green). Measurement can be performed in transport, or using charge-sensing by forming a sensor quantum dot under one channel to sense a double quantum dot in the opposite channel. (d)–(f) Cross section and band structure of metal, dielectric (black), and semiconductor (d) SiMOS, (e) Si/SiGe, and (f) Ge/SiGe.

A schematic of each material and associated device is shown in Fig. 3 and labeling of the relevant gates is shown in Fig. 4. The SiMOS device is a three-layer, triple quantum dot structure with dedicated plungers (P_{1-3}), inter-dot barriers (B_{12}, B_{23}), and dot-reservoir barriers (T_l, T_r).

Two large metallic gates (C_l, C_u) deposited in the initial layer and kept at constant potential serve to confine the quantum dots in one lateral dimension. They also serve to screen charge noise resulting from fluctuations near the quantum dot array.

Two single electron transistors (SETs) are positioned at either side of the quantum dot array, and function as charge sensors for spin and charge readout. The Si/SiGe device is a quintuple quantum dot linear array written in three layers utilizing a similar architecture to that of the SiMOS device. The quantum dot array contains five plunger gates (P_{1-5}) with inter-dot barriers (B_{12-45}) and dot-reservoir barriers. Here too, the quantum dots are confined laterally and screened from charge noise by two confinement gates. Two SETs are positioned parallel to the quantum dot channel. The Ge/SiGe device is a 2×2 quadruple quantum dot array written in two layers. Gates (P_{1-4}) are positioned anti-clockwise in the array and define the potential of the quantum dots. Each pair of adjacent quantum dots share a barrier gate (B_{12-41}) capable of tuning inter-dot tunnel coupling. Coupling of each quantum dot to its reservoir can be controlled via a barrier gate. This device can be operated as a quadruple quantum dot system in the transport mode, but for the present work, we

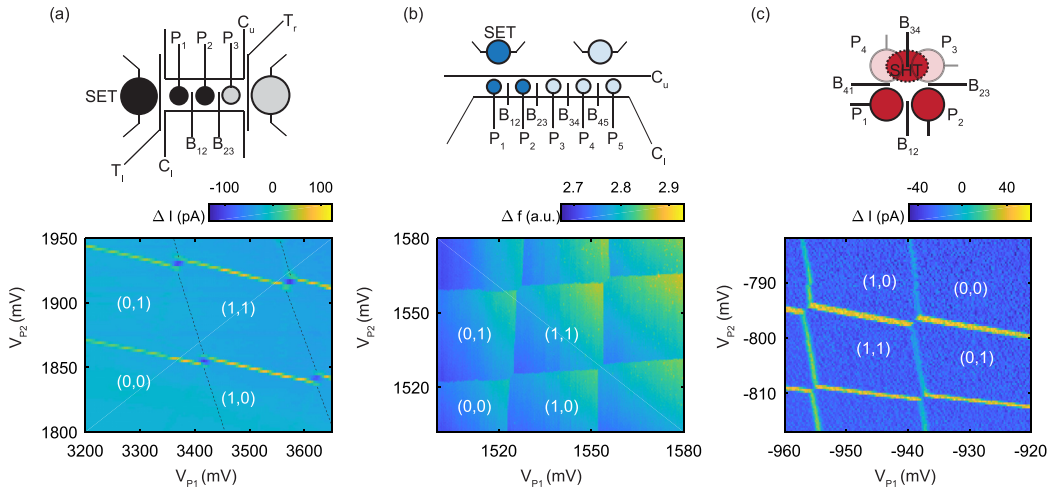

FIG. 4. Charge stability diagrams of double quantum dots depleted to the single electron/hole regime for the three platforms. (a) SiMOS double quantum dot. Charge addition lines under P_1 are not visible due to the low tunnel rate from the reservoir. Map taken at 0.44 K using lock-in charge sensing. The excitation is placed on the inter-dot gate B_{12}. (b) Si/SiGe double quantum dot formed under the first two plungers, sensed by the nearest charge sensor via RF-reflectometry utilizing a resonant LC circuit at 84 MHz. Here, the plunger gate voltages are in a virtual gate space correcting for weak cross capacitive coupling. (c) Ge/SiGe depleted to the single hole regime. A large single quantum dot is formed under P_3, B_{34}, and P_4, by adjusting the tunnel barrier voltage B_{34}, and is used to sense a double quantum dot under P_1 and P_2. The lock-in excitation is placed on the inter-dot tunnel barrier B_{12}.

intentionally tune the inter-dot barrier to form a single hole transistor (SHT) along a dot channel that we subsequently use for charge sensing of the double quantum dot along the opposite channel. For more information about device specific fabrication, see supplementary material Sec. II.

To demonstrate the success of this largely unified integration scheme, we show that we can create stable quantum dots in each platform. Figure 4 shows the charge stability diagrams for tunnel-coupled double quantum dots, measured by performing charge sensing. Lock-in techniques are used in the case of SiMOS and Ge/SiGe, where an excitation is placed on an inter-dot barrier gate B_{12} in each case, and the trans-conductance of the source-drain channel is measured. We use compensation to remain at a sensitive point of the SET/SHT Coulomb peaks.[45] In the case of Si/SiGe, charge readout is performed using RF-reflectometry techniques. A 3 μH kinetic inductor is bonded to the sample source which forms a resonant LC circuit when combined with parasitic capacitance to the ground. In each case, we measure a charge stability diagram and show that we can deplete down to the (0,0) electron/hole charge configuration. This is done by ensuring that the load rate of each quantum dot is sufficiently high, and depleting to the first charge state of each quantum dot by sweeping the associated plunger gate, until no further charge transition lines are detected (for details in tuning to the last state, see our previous works[17,46]) While operation in the single electron regime in silicon has been routinely achieved before, this work shows the first demonstration of the single hole regime using charge sensing of holes in Ge/SiGe. We attribute the slight difference in the slope of the first and second charge addition lines in Fig. 4(c) to a shift in the position of the quantum dot relative to the inter-dot tunnel barrier.

In Fig. 5, we demonstrate that quantum dots can be formed under each dedicated plunger gate. For Figs. 5(a)–5(c), in each SiMOS quantum dot, lock-in charge sensing is performed by placing an excitation on the respective plunger gates, while trans-conductance in the nearby SET channel is measured. In each case, the first charge transition is visible. For quantum dots formed under plungers P_{2-3}, electron loading is from the right SET which constitutes a reservoir. For the quantum dot under P_1, loading is from the left SET via the gate T_l. The Si/SiGe quintuple quantum dot system in Figs. 5(d)–5(g) is tuned using the N + 1 strategy,[42] reaching the few-electron regime simultaneously for all quantum dots. In Fig. 5, we show the stability diagrams, in each of which we scan two virtual plunger gates which allow to controllably load a single electron into each quantum dot. Double quantum dots are formed between each set of adjacent plungers, and sensed using RF-reflectometry like in Fig. 4(b) using the left SET for all configurations. As expected, an observable signal from charge transition lines fades as the quantum dot pairs are formed farther away from the SET. The derivative of the reflected signal is plotted, and shows the (0,0) charge occupancy for each charge stability diagram. For every double quantum dot, loading occurs via the left accumulation gate, leading to latching effects and low tunnel rates in the quantum dots formed farther away from the reservoir. Figures 5(h)–5(k) shows the charge sensing operation of the 2 × 2 quantum dot array fabricated in Ge/SiGe. In each case, a sensing quantum dot is formed in the channel parallel to the double quantum dot by opening the inter-dot barrier such that a large single quantum dot is formed. In the opposite channel, the inter-dot barrier is closed, forming a double quantum dot system in the low tunnel coupled regime.

A significant challenge for larger quantum dot arrays will manifest in tuning. The presence of large capacitive crosstalk in GaAs has led to development of virtual gates and approaches to tune larger systems.[42,48] To assess the relevance of these approaches for silicon and germanium structures, we measure the cross capacitance as shown in Fig. 6. To obtain the cross coupling, we measure the slope of the charge addition lines with respect to each gate and normalize by a cross

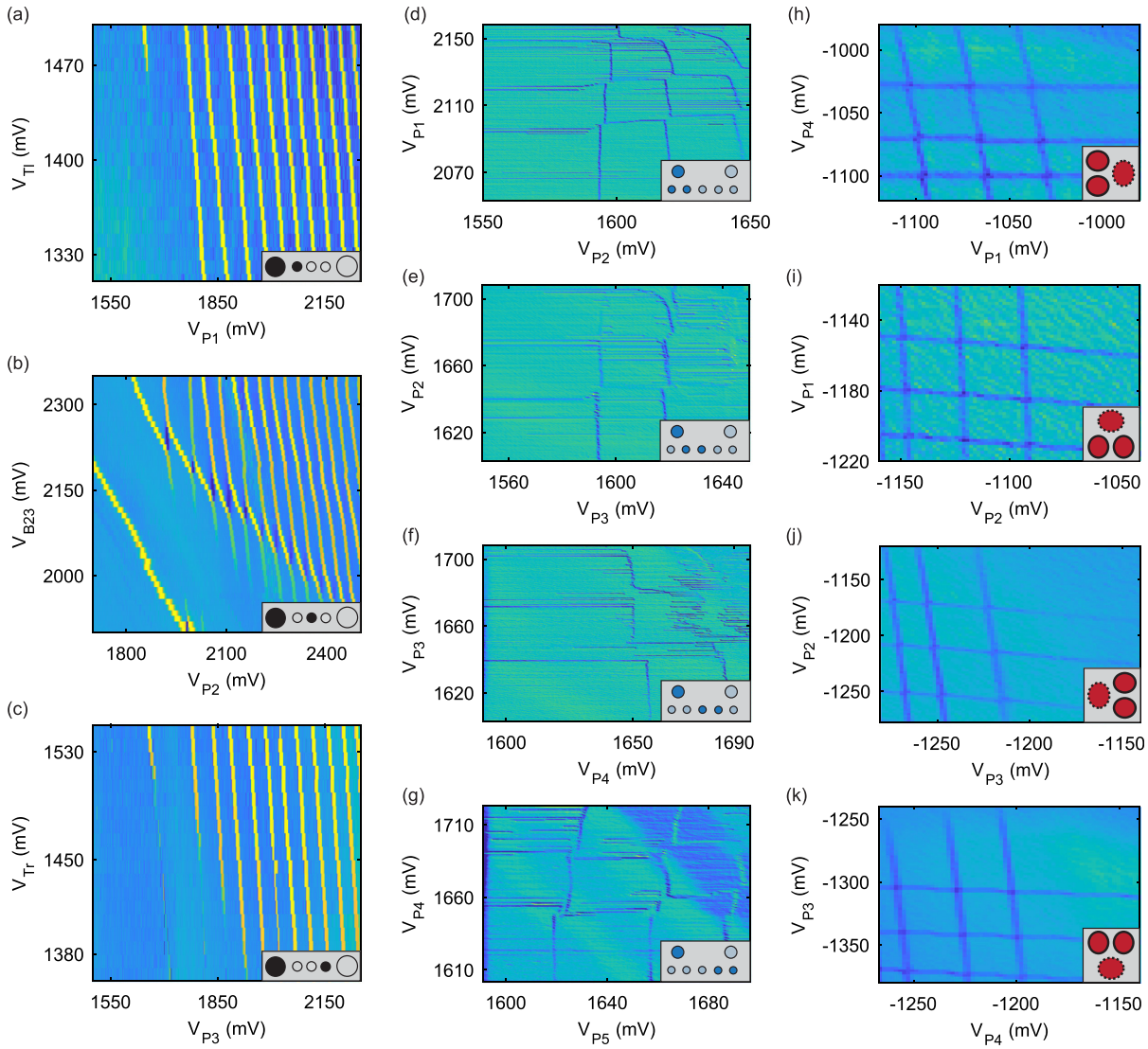

FIG. 5. Quantum dot arrays in SiMOS, Si/SiGe, and Ge/SiGe. (a)–(c) SiMOS triple quantum dot device stability diagrams. Each single quantum dot is formed under its respective plunger gate upon which an excitation is placed for lock-in charge sensing. Each quantum dot is depleted to the single charge state. (b) Shows the crossing of the adjacent quantum dot under P_3, through which the quantum dot is loaded. (d)–(g) Si/SiGe double quantum dots tuned up sequentially using the N + 1 method[42] to the single electron regime. True plunger gate voltages are plotted, though virtual gates are swept containing small corrections to adjacent barriers and plungers. Each double quantum dot pair is sensed using RF-reflectometry. The same SET is used for readout in each case, as indicated by the relative signals as each double quantum dot pair is formed farther from the charge sensor. (g) The data has been filtered to remove 50 Hz background noise for data clarity. (h)–(k) Ge/SiGe 2 × 2 array double quantum dots formed in each possible configuration. In each case, a charge sensor is formed in the parallel channel by raising the inter-dot coupling to form a large single quantum dot with high hole occupation. Each charge stability diagram shows RF-sensing of double quantum dots depleted to the last hole occupancy, in the low tunnel-coupled regime.

coupling of unity for the plunger gate associated with the respective quantum dot. Each slope is taken for the first charge transition and in the low tunnel-coupled regime. In SiMOS, cross coupling is almost negligible, as expected from quantum dots located only 17 nm (10 nm SiO_2 and 7 nm Al_2O_3) below the electrostatic gates. This compares favorably to the cross coupling observed in Si/SiGe, where falloff is significantly slower despite sharing equal gate pitch to the SiMOS array. While the cross coupling in the Ge/SiGe system is the largest and extends over multiple neighboring gates, it still falls off significantly faster than quantum dots defined in GaAs.[42] For Ge/SiGe, we also observe that the barrier gates have a relatively stronger lever arm to the quantum dots as compared to the plunger gates, due to definition in the lower layers of the multi-layer stack. Summarizing, we conclude that for SiMOS, tuning is most straightforward considering capacitive crosstalk only, while each platform compares favorably to GaAs using an open gate layout.[42]

With the ability to fabricate quantum dot devices in several group IV based platforms using a unified fabrication scheme, we look ahead

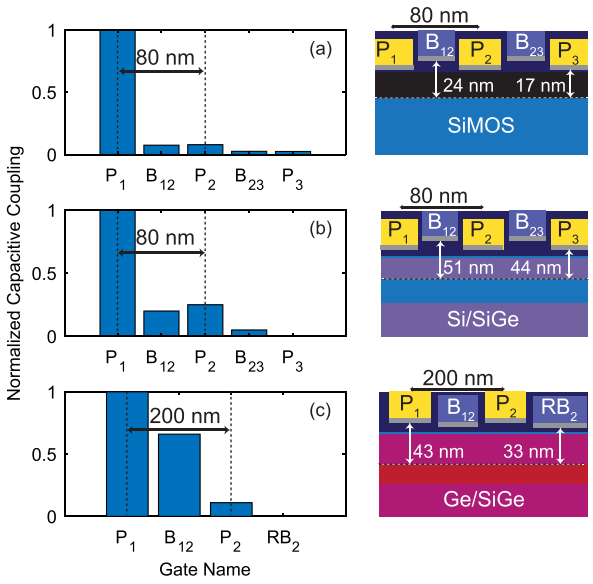

FIG. 6. Cross capacitance to neighboring gates of a quantum dot in the single charge occupancy regime under gate P_1 in each platform. For SiMOS (a), we observe an immediate falloff of cross coupling due to the tight quantum dot confinement present in SiMOS devices. Here, the inter-dot pitches match those of Si/SiGe at 80 nm. For Si/SiGe (b), we see significant cross coupling between adjacent plungers and barrier gates. Here, the plunger gates are written before the barrier layer and have an inter-dot pitch of 80 nm. Ge/SiGe (c) reveals as expected a slower falloff of cross coupling. We attribute this to the larger plunger gate design, made possible by lower hole effective mass. In this case, the plunger gates P_1 and P_2 are written in the layer above the barrier gates B_{12} and R B_2, decreasing coupling to their respective quantum dots. The plunger to plunger pitch is 200 nm. Each cross-sectional cartoon shows a plunger pitch and the distance between each relevant gate layer to the center of the quantum well.

to identify future challenges and opportunities related to quantum information processing with semiconductor quantum dot spin qubits. Moving forward, we identify four focus areas for the community that through shared co-development, will launch the field into new and practical ground.

Most quantum devices are fabricated in academic cleanrooms, where the turnaround and feedback from measurement to design and fabrication is fast. However as designs for various types of quantum dot devices converge, an opportunity exists to leverage off the excellent material quality[13,36,49] and processing facilities of industrial fabrication lines. Devices fabricated on industrially grown 300 mm wafers have led to CMOS fab spin qubits,[25] tunable tunnel coupling between single electrons in SiMOS,[17] and two-qubit gate operations beyond one Kelvin.[50] Furthering symbiotic partnerships with the industry may prove highly beneficial for the development of uniform quantum dots. The adoption of group IV based semiconductor platforms beyond SiMOS such as strained Si and Ge, as well as full 300 mm device fabrication lines would accelerate progress in the field of semiconductor quantum dot based quantum computing, like it has in other fields.[51]

Many quantum systems have been studied as qubit candidates for quantum information processing. It has also become clear that each of these quantum systems hold specific properties suited to the various requirements of quantum computation.[52] As a result, emerging research has targeted the combination of qubit implementation to leverage off specific advantages and improve qubit quality. These hybrid directions are extensive, including the coupling of spin to light allowing long range interactions as has been shown on silicon based platforms,[53–56] or the coupling of spins to systems that reliably conserve the quantum state, such as topologically protected qubits.[57–60] Here, holes in Ge/SiGe make an excellent candidate for hybrid spin-Majorana qubits, thanks to the Fermi level pinning at the valence band, allowing for tunnel-coupled contacts to superconductors.[30] An important milestone toward demonstrating such a hybrid qubit in Ge/SiGe will be to achieve hard gap superconductivity. This has already been demonstrated in Ge/SiGe core shell nanowires,[61,62] thus providing scope for planar structures. Such a hard gap would be the first step toward defining isolated zero energy states, key in many proposals for hybrid technology.[63]

As quantum devices grow in number of physical qubits, so too do the complexities related to tuning them. As a result, a great body of work on the automated tuning of quantum devices has emerged in the last few years in an attempt to address this concern. Due to the extremely low disorder of the material, these efforts were pioneered in GaAs based quantum dots, demonstrating automated tuning to the single electron regime[48,64] and controllable interdot tunnel coupling.[65] However quantum dot arrays have also emerged more recently in Si/SiGe[66] and computer automated single electron regime tune-up protocols therein.[67,68] Moreover, with the demonstrations of SiMOS, Si/SiGe, and Ge/SiGe quantum dots in this work, further development of automated tuning protocols will be necessary for the exploration of larger quantum dot systems. In particular, the automated tuning of interdot tunnel couplings and protocols for 2D arrays will be critical. Furthermore, high fidelity operation of qubits in large scale quantum devices will require precise operation at exact exchange interaction, resonance frequencies, and Rabi frequencies, accounting for potential drifts in these parameters over time. Tune up protocols will therefore have to go beyond charge state control, handling qubit operation also.

Scale up of the number of qubits on a quantum device requires the design and implementation of extensible two-dimensional qubit arrays. However, the wiring and fanout for each qubit at large numbers is impractical and there is a need for engineering architectures that obey Rent's rule.[69] Additionally, the limited cooling power of dilution refrigerators at mK temperatures poses a serious challenge for the scalability of quantum systems.[9] As a result, proposals for shared control using crossbar architectures[47,70] and on chip classical electronics[9] have been put forward, as well as work on the operation of qubits at high temperatures[50,71] to mitigate the cooling power requirements of dilution refrigerators. 2D scalability will also require improved operation of larger quantum devices. This includes the ability to tune all quantum dot couplings and to shuttle spin states coherently around a lattice, placing strict requirements on the uniformity of quantum dots. This positions Si/SiGe and Ge/SiGe as favorable platforms due to their very low disorder. A milestone in 2D scalability would be the routine ability to reach single charge occupancy in arbitrary quantum dots using the same cross-capacitance matrix for each quantum dot as this would enable shared control for scalable quantum operation as is proposed in crossbar architectures.[47] We observe Si/SiGe double quantum dots that can be tuned to the (1,1) charge state using identical plunger gates [e.g., Fig. 4(b)], but further progress is essential to enable shared control in large arrays. Solutions to these outstanding hurdles will be

crucial to further develop extensible qubit unit cells and therefore scale quantum devices into practically useful regimes.

In conclusion, we presented a cross-platform integration scheme for multi-layer quantum dot arrays in group-IV semiconductor hosts. We fabricated linear and 2D arrays of quantum dots in the group IV platforms SiMOS, Si/SiGe, and Ge/SiGe. We demonstrated single electron and hole occupancy in double quantum dots confirmed by charge sensing. We showed stable quantum dots under each plunger gate in a SiMOS triple quantum dot linear array, depleteable to the final charge state. In Si/SiGe, we demonstrated tune-up of a quintuple quantum dot array utilizing the N + 1 method, successfully reaching the few electron regime in each quantum dot simultaneously. Moreover, we formed and sensed double quantum dots in the single hole regime in each configuration of a 2 × 2 quadruple quantum dot array in Ge/SiGe. We furthermore compared the capacitive crosstalk between quantum dots and gates. We find that the cross capacitance can be small and therefore argue that future work on strategies for the initial tuning of quantum dot arrays should address disorder rather than capacitive crosstalk, in particular, for SiMOS quantum dots. We envision that our integration scheme for fabricating quantum dot arrays in SiMOS, Si/SiGe, and Ge/SiGe will boost collective development and enable the realization of devices capable of simulating and computing with quantum information.

See the supplementary material for a detailed description of key fabrication improvements, as well as a complete fabrication recipe for each platform.

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REFERENCES

[1]D. Loss and D. P. DiVincenzo, Phys. Rev. A **57**, 120–126 (1998).
[2]T. Hensgens, T. Fujita, L. Janssen, X. Li, C. J. Van Diepen, C. Reichl, W. Wegscheider, S. Das Sarma, and L. M. Vandersypen, Nature **548**, 70–73 (2017).
[3]M. Leijnse and K. Flensberg, Phys. Rev. B **84**, 140501 (2011).
[4]J. D. Sau and S. Das Sarma, Nat. Commun. **3**, 964 (2012).
[5]J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard, Science **309**, 2180–2184 (2005).
[6]F. H. Koppens, C. Buizert, K. J. Tielrooij, I. T. Vink, K. C. Nowack, T. Meunier, L. P. Kouwenhoven, and L. M. Vandersypen, Nature **442**, 766–771 (2006).
[7]J. P. Dehollain, U. Mukhopadhyay, V. P. Michal, Y. Wang, B. Wunsch, C. Reichl, W. Wegscheider, M. S. Rudner, E. Demler, and L. M. K. Vandersypen, arXiv:1904.05680 (2019).
[8]V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. Bakkers, and L. P. Kouwenhoven, Science **336**, 1003–1007 (2012).
[9]L. M. K. Vandersypen, H. Bluhm, J. S. Clarke, A. S. Dzurak, R. Ishihara, A. Morello, D. J. Reilly, L. R. Schreiber, and M. Veldhorst, npj Quantum Inf. **3**, 34 (2017).
[10]M. Veldhorst, J. C. Hwang, C. H. Yang, A. W. Leenstra, B. De Ronde, J. P. Dehollain, J. T. Muhonen, F. E. Hudson, K. M. Itoh, A. Morello *et al.*, Nat. Nanotechnol. **9**, 981–985 (2014).
[11]F. A. Zwanenburg, A. S. Dzurak, A. Morello, M. Y. Simmons, L. C. Hollenberg, G. Klimeck, S. Rogge, S. N. Coppersmith, and M. A. Eriksson, Rev. Mod. Phys. **85**, 961–1019 (2013).
[12]A. Sammak, D. Sabbagh, N. W. Hendrickx, M. Lodari, B. Paquelet Wuetz, A. Tosato, L. R. Yeoh, M. Bollani, M. Virgilio, M. A. Schubert *et al.*, Adv. Funct. Mater. **29**, 1807613 (2019).
[13]D. Sabbagh, N. Thomas, J. Torres, R. Pillarisetty, P. Amin, H. C. George, K. Singh, A. Budrevich, M. Robinson, D. Merrill *et al.*, Phys. Rev. Appl. **12**, 014013 (2019).
[14]S. J. Angus, A. J. Ferguson, A. S. Dzurak, and R. G. Clark, Nano Lett. **7**, 2051–2055 (2007).
[15]D. M. Zajac, T. M. Hazard, X. Mi, K. Wang, and J. R. Petta, Appl. Phys. Lett. **106**, 223507 (2015).
[16]M. Brauns, S. V. Amitonov, P. C. Spruijtenburg, and F. A. Zwanenburg, Sci. Rep. **8**, 5690 (2018).
[17]H. G. J. Eenink, L. Petit, W. I. L. Lawrie, J. S. Clarke, L. M. K. Vandersypen, and M. Veldhorst, *Nano Lett.* **19**(12), 8653–8657 (2019).
[18]C. H. Yang, K. W. Chan, R. Harper, W. Huang, T. Evans, J. C. Hwang, B. Hensen, A. Laucht, T. Tanttu, F. E. Hudson *et al.*, Nat. Electron. **2**, 151–158 (2019).
[19]J. Yoneda, K. Takeda, T. Otsuka, T. Nakajima, M. R. Delbecq, G. Allison, T. Honda, T. Kodera, S. Oda, Y. Hoshi *et al.*, Nat. Nanotechnol. **13**, 102–106 (2018).
[20]M. Veldhorst, C. H. Yang, J. C. Hwang, W. Huang, J. P. Dehollain, J. T. Muhonen, S. Simmons, A. Laucht, F. E. Hudson, K. M. Itoh *et al.*, Nature **526**, 410–414 (2015).
[21]D. M. Zajac, A. J. Sigillito, M. Russ, F. Borjans, J. M. Taylor, G. Burkard, and J. R. Petta, Science **359**, 439–442 (2018).
[22]T. F. Watson, S. G. Philips, E. Kawakami, D. R. Ward, P. Scarlino, M. Veldhorst, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith *et al.*, Nature **555**, 633–637 (2018).
[23]P. C. Spruijtenburg, J. Ridderbos, F. Mueller, A. W. Leenstra, M. Brauns, A. A. Aarnink, W. G. Van Der Wiel, and F. A. Zwanenburg, Appl. Phys. Lett. **102**, 192105 (2013).
[24]S. D. Liles, R. Li, C. H. Yang, F. E. Hudson, M. Veldhorst, A. S. Dzurak, and A. R. Hamilton, Nat. Commun. **9**, 3255 (2018).
[25]R. Maurand, X. Jehl, D. Kotekar-Patil, A. Corna, H. Bohuslavskyi, R. Laviéville, L. Hutin, S. Barraud, M. Vinet, M. Sanquer *et al.*, Nat. Commun. **7**, 13575 (2016).
[26]M. Failla, J. Keller, G. Scalari, C. Maissen, J. Faist, C. Reichl, W. Wegscheider, O. J. Newell, D. R. Leadley, M. Myronov *et al.*, New J. Phys. **18**, 113036 (2016).
[27]Y. H. Su, Y. Chuang, C. Y. Liu, J. Y. Li, and T. M. Lu, Phys. Rev. Mater. **1**, 044601 (2017).
[28]M. Lodari, A. Tosato, D. Sabbagh, M. A. Schubert, G. Capellini, A. Sammak, M. Veldhorst, and G. Scappucci, Phys. Rev. B **100**, 041304 (2019).
[29]N. W. Hendrickx, D. P. Franke, A. Sammak, M. Kouwenhoven, D. Sabbagh, L. Yeoh, R. Li, M. L. Tagliaferri, M. Virgilio, G. Capellini *et al.*, Nat. Commun. **9**, 2835 (2018).
[30]N. W. Hendrickx, D. P. Franke, A. Sammak, G. Scappucci, and M. Veldhorst, arXiv:1904.11443 (2019).
[31]A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, Appl. Phys. Lett. **89**, 252110 (2006).
[32]L. Petit, J. M. Boter, H. G. Eenink, G. Droulers, M. L. Tagliaferri, R. Li, D. P. Franke, K. J. Singh, J. S. Clarke, R. N. Schouten *et al.*, Phys. Rev. Lett. **121**, 076801 (2018).
[33]T. Ando, A. B. Fowler, and F. Stern, Rev. Mod. Phys. **54**, 437–672 (1982).
[34]A. Gold and V. T. Dolgopolov, Phys. Rev. B **33**, 1076–1084 (1986).
[35]G. H. Kruithof, T. M. Klapwijk, and S. Bakker, Phys. Rev. B **43**, 6642–6649 (1991).

[36]B. P. Wuetz, P. L. Bavdaz, L. A. Yeoh, R. Schouten, H. van der Does, M. Tiggelman, D. Sabbagh, A. Sammak, C. G. Almudever, F. Sebastiano *et al.*, arXiv:1907.11816 (2019).
[37]R. M. Jock, N. T. Jacobson, P. Harvey-Collard, A. M. Mounce, V. Srinivasa, D. R. Ward, J. Anderson, R. Manginell, J. R. Wendt, M. Rudolph *et al.*, Nat. Commun. **9**, 1768 (2018).
[38]W. Huang, M. Veldhorst, N. M. Zimmerman, A. S. Dzurak, and D. Culcer, Phys. Rev. B **95**, 075403 (2017).
[39]H. Bracht, E. E. Haller, and R. Clark-Phelps, Phys. Rev. Lett. **81**, 393–396 (1998).
[40]N. W. Hendrickx, M. L. Tagliaferri, M. Kouwenhoven, R. Li, D. P. Franke, A. Sammak, A. Brinkman, G. Scappucci, and M. Veldhorst, Phys. Rev. B **99**, 075435 (2019).
[41]E. J. Connors, J. Nelson, H. Qiao, L. F. Edge, and J. M. Nichol, Phys. Rev. B **100**, 165305 (2019).
[42]C. Volk, A. M. J. Zwerver, U. Mukhopadhyay, P. T. Eendebak, C. J. van Diepen, J. P. Dehollain, T. Hensgens, T. Fujita, C. Reichl, W. Wegscheider *et al.*, npj Quantum Inf. **5**, 29 (2019).
[43]H. Watzinger, J. Kukučka, L. Vukušić, F. Gao, T. Wang, F. Schäffler, J. J. Zhang, and G. Katsaros, Nat. Commun. **9**, 3902 (2018).
[44]E. Kawakami, P. Scarlino, D. R. Ward, F. R. Braakman, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, and L. M. Vandersypen, Nat. Nanotechnol. **9**, 666–670 (2014).
[45]C. H. Yang, W. H. Lim, F. A. Zwanenburg, and A. S. Dzurak, AIP Adv. **1**, 042111 (2011).
[46]N. W. Hendrickx, W. I. L. Lawrie, L. Petit, A. Sammak, G. Scappucci, and M. Veldhorst, arXiv:1912.10426 (2019).
[47]R. Li, L. Petit, D. P. Franke, J. P. Dehollain, J. Helsen, M. Steudtner, N. K. Thomas, Z. R. Yoscovits, K. J. Singh, S. Wehner *et al.*, Sci. Adv. **4**, eaar3960 (2018).
[48]T. A. Baart, M. Shafiei, T. Fujita, C. Reichl, W. Wegscheider, and L. M. Vandersypen, Nat. Nanotechnol. **11**, 330–334 (2016).
[49]V. Mazzocchi, P. G. Sennikov, A. D. Bulanov, M. F. Churbanov, B. Bertrand, L. Hutin, J. P. Barnes, M. N. Drozdov, J. M. Hartmann, and M. Sanquer, J. Cryst. Growth **509**, 1–7 (2019).
[50]L. Petit, H. G. J. Eenink, M. Russ, W. I. L. Lawrie, N. W. Hendrickx, J. S. Clarke, L. M. K. Vandersypen, and M. Veldhorst, arXiv:1910.05289 (2019).
[51]F. Arute, K. Arya, R. Babbush, D. Bacon, J. C. Bardin, R. Barends, R. Biswas, S. Boixo, F. G. S. L. Brandao, D. A. Buell *et al.*, Nature **574**, 505 (2019).
[52]D. P. DiVincenzo, Fortschr. Phys. **48**, 771–783 (2000).
[53]X. Mi, M. Benito, S. Putz, D. M. Zajac, J. M. Taylor, G. Burkard, and J. R. Petta, Nature **555**, 599–603 (2018).
[54]N. Samkharadze, G. Zheng, N. Kalhor, D. Brousse, A. Sammak, U. C. Mendes, A. Blais, G. Scappucci, and L. M. Vandersypen, Science **359**, 1123–1127 (2018).
[55]A. J. Landig, J. V. Koski, P. Scarlino, U. C. Mendes, A. Blais, C. Reichl, W. Wegscheider, A. Wallraff, K. Ensslin, and T. Ihn, Nature **560**, 179–184 (2018).
[56]F. Borjans, X. G. Croot, X. Mi, M. J. Gullans, and J. R. Petta, Nature **577**, 195–198 (2020).
[57]M. Leijnse and K. Flensberg, Phys. Rev. B **86**, 104511 (2012).
[58]S. Das Sarma, M. Freedman, and C. Nayak, Phys. Rev. Lett. **94**, 166802 (2005).
[59]T. Hyart, B. Van Heck, I. C. Fulga, M. Burrello, A. R. Akhmerov, and C. W. Beenakker, Phys. Rev. B **88**, 035121 (2013).
[60]S. Hoffman, C. Schrade, J. Klinovaja, and D. Loss, Phys. Rev. B **94**, 045316 (2016).
[61]J. Xiang, A. Vidan, M. Tinkham, R. M. Westervelt, and C. M. Lieber, Nat. Nanotechnol. **1**, 208–213 (2006).
[62]J. Ridderbos, M. Brauns, J. Shen, F. K. de Vries, A. Li, S. Kölling, M. A. Verheijen, A. Brinkman, W. G. van der Wiel *et al.*, Nano Lett. **20**, 122–130 (2019).
[63]J. Alicea, Rev. Prog. Phys. **75**(7), 076501 (2012).
[64]T. Botzem, M. D. Shulman, S. Foletti, S. P. Harvey, O. E. Dial, P. Bethke, P. Cerfontaine, R. P. G. McNeil, D. Mahalu, V. Umansky *et al.*, Phys. Rev. Appl. **10**, 54026 (2018).
[65]C. J. Van Diepen, P. T. Eendebak, B. T. Buijtendorp, U. Mukhopadhyay, T. Fujita, C. Reichl, W. Wegscheider, and L. M. Vandersypen, Appl. Phys. Lett. **113**, 033101 (2018).
[66]A. R. Mills, M. M. Feldman, C. Monical, P. J. Lewis, K. W. Larson, A. M. Mounce, and J. R. Petta, Appl. Phys. Lett. **115**, 113501 (2019).
[67]A. R. Mills, D. M. Zajac, M. J. Gullans, F. J. Schupp, T. M. Hazard, and J. R. Petta, Nat. Commun. **10**, 1063 (2019).
[68]S. S. Kalantre, J. P. Zwolak, S. Ragole, X. Wu, N. M. Zimmerman, M. D. Stewart, and J. M. Taylor, npj Quantum Inf. **5**, 1–6 (2019).
[69]D. P. Franke, J. S. Clarke, L. M. Vandersypen, and M. Veldhorst, Microprocessors Microsyst. **67**, 1–7 (2019).
[70]M. Veldhorst, H. G. Eenink, C. H. Yang, and A. S. Dzurak, Nat. Commun. **8**, 1766 (2017).
[71]C. H. Yang, R. C. C. Leon, J. C. C. Hwang, A. Saraiva, T. Tanttu, W. Huang, J. C. Lemyre, K. W. Chan, K. Y. Tan, F. E. Hudson *et al.*, arXiv:1902.09126 (2019).