

HIGH-ASPECT-RATIO CMOS ADD-ON
MODULES FOR RF PASSIVE
COMPONENTS

HUSEYIN SAGKOL

High-Aspect-Ratio CMOS Add-on Modules for RF Passive Components

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft;
op gezag van de Rector Magnificus prof. ir. K.C.A.M. Luyben;
voorzitter van het College voor Promoties,

in het openbaar te verdedigen op
dinsdag 22 maart 2011 om 10:00 uur

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Huseyin Sagkol,
High-Aspect-Ratio CMOS Add-on Modules for RF Passive Components,
Ph.D. Thesis Delft University of Technology.

ISBN: 978-90-8570-737-0

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Printed by CPI Wöhrmann Print Service in the Netherlands.

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Chapter 1

Introduction

1.1. Microwave Passives: A Brief History

Microwave theory has its roots deep in history going back to the formulation of modern electromagnetic theory by James Clerk Maxwell in 1873. However, the birth of microwave technology dates back to an unfortunate event in our history, World War II. Radar, owing its existence to this event, was the product that flashed the light of the microwave industry [1, 2]. Nonetheless, at the end of WW II there were still very few active components (microwave sources) available to engineers. Unlike today's designs, which tend to implement all possible functions with active devices or even digital circuitry, majority of the early electronic circuits relied mostly on passive components with the rectangular waveguide as the most important building block.

After WW II commercialization began and the ever-growing trend of miniaturization started to shape the future of microwave industry. With the introduction of semiconductor technology the number of available active devices and circuit functions started to increase. This led to the reduction of the passive component count in microwave circuits, and transformed their physical properties. Initially a microwave circuit would look like a combination of pipes and screws that could easily be mistaken for a part of a plumbing system (Figure 1.1). As semiconductor components were introduced, it became more and more difficult to integrate them into these pipes due to their miniscule sizes. The arrival of the planar printed circuit board (PCB) technology in the 1960's offered a solution. The bulky waveguides were now replaced by PCB-compatible, planar transmission lines such as the tri-plate, and microstrip (Figure 1.1), [1] which formed the basis of various

passive elements including 90° and 180° hybrids, directional couplers, power dividers, and filters. Active devices would now be soldered on PCB that contained the prefabricated passive circuitry (Figure 1.2).



Figure 1.1: Comparison of a tri-plate with a waveguide-based circuit. [1]

Prior to 1980's the microwave industry was heavily dependent on military applications. Products were power hungry, expensive and hefty devices that mainly worked in the 2-18 GHz range and higher frequency bands. As the military market started to saturate, the industry experts were predicting the end of the golden age of microwaves. The rescue came with the explosive growth of the personal communication market in the 1990's which created new opportunities for the industry. But the introduction of personal computers, internet, and mobile phones required a change of mindset. Now the driving force was not just high performance, but also reduction of cost, size, weight, and power consumption of microwave devices, which was considered less crucial for military applications. Besides, since most personal communication systems were operating at lower microwave frequencies (below 2 GHz), transmission line components were out of the game. Their

length being comparable to the propagation wavelength (centimeters at frequencies below 2 GHz), these components were simply too large to be integrated on a miniaturized circuit board. Instead, lumped elements such as inductors, capacitors, and resistors became the key components (Figure 1.3).

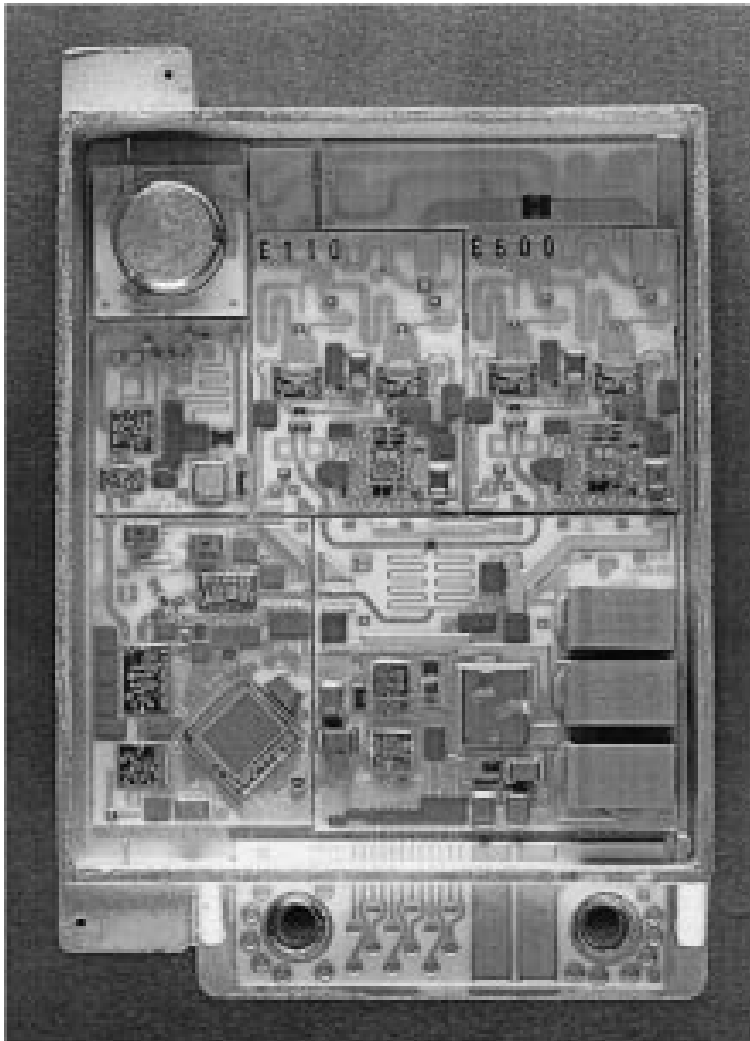


Figure 1.2: A T/R module [3]

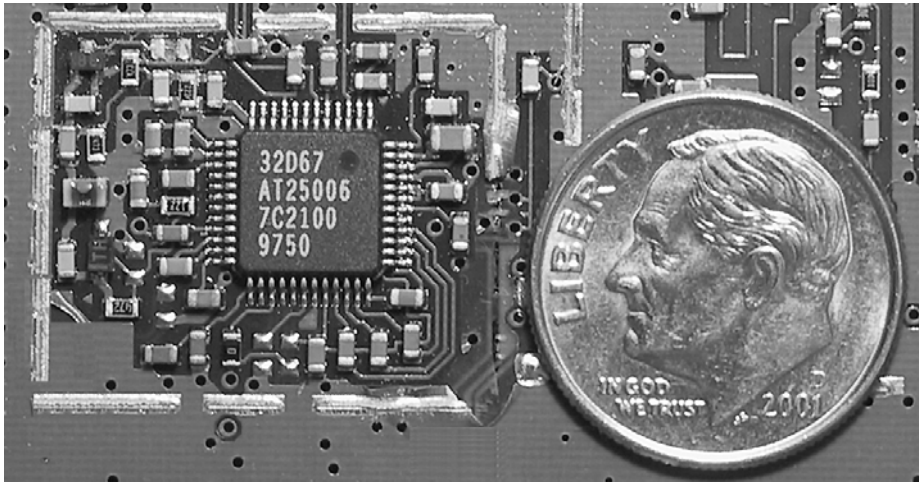


Figure 1.3: RF section of a cell phone with many surface-mount passives[4].

Those lumped elements, together with surface or bulk acoustic wave filters were fabricated independently and then integrated on the circuit board together with active components in a discrete manner. However, this approach was soon to be proven inadequate in view of the growing complexity of mobile wireless circuits. Introduction of different communication bands and digital communication methods, and the demand for multipurpose data transmission, imposed a multiband and multiprotocol structure on the mobile devices. Thus, the number of passive components increased tremendously reaching to a whopping 300 for an average mobile phone [4]. A fabrication error in just one component meant costly problems. Also performance tolerances became more and more stringent. In order to cope with the complexity and tight tolerances, and to increase repeatability, the RF industry had now to adapt the rules of microelectronics industry and had to shift most of its components from discrete to integrated devices.

1.2. Passive Integration

Initially, however, the integration of passive devices into the integrated circuit (IC) substrate was blocked by the textbook rule, which stated that it would be illogical to put inductors with meaningful inductance values on a substrate [6], since parasitics would have detrimental effects on the quality factor. Indeed this argument was correct for Si substrates, which were introducing significant amount of parasitics and substrate loss due to the very low substrate resistivity ($2\text{-}3\ \Omega\text{cm}$) required for active device integration. Yet, with the availability of larger GaAs wafers, a very good substrate for high-frequency active devices due to its high electron mobility, there was enough real estate on the wafer to accommodate the rather bulky inductors. Moreover,

these devices were of sufficient quality thanks to the high resistivity of GaAs (in excess of $1 \text{ k}\Omega\text{cm}$). This technological advancement paved the way for on-chip passive integration and, thus, the emergence of Monolithic Microwave Integrated Circuits (MMICs). Now lumped passive devices were fabricated together with the active components on a single chip. However, the high cost of GaAs wafers hindered its penetration into the commercial market. Since the commercial communication devices worked at relatively low frequencies (below 2 GHz), with a bit more relaxed requirements than military systems, it was a bit luxurious to implement passive devices on expensive GaAs substrates for commercial applications. Hence eyes were turned onto Si again.

Silicon mainly offered bipolar junction transistors (BJT) and metal oxide semiconductor (MOS). BJTs were more favorable in radio frequency (RF) design due to their resistive type of operation. Unlike BJTs, MOS transistors relied on a capacitive gate control for their operation. As frequency increased MOS gates would start leaking current and performance would drop. This made complementary MOS (CMOS) a low pass process in nature, hence they were not suitable for the current circuit techniques [6], which used mostly discrete elements such as transmission lines or filters with 5-10 BJTs as the active circuit based on well established heterodyne receiver. Therefore MOS appropriate circuit techniques had to be developed. As an example first reported CMOS RF amplifiers had an integrated micromachined inductor to inductively tune the transistor capacitance to convert inherent low-pass behavior to band-pass [7]. Integration of the inductor was crucial in order to reduce parasitics which would shift the pass band, hence jeopardize the whole operation. Nevertheless, as time went by, CMOS components improved with mind boggling pace following Moore's Law in feature size, hence gate capacitance, reduction. Soon active devices had sufficiently high cut-off frequencies to work in the low GHz range. In addition, researchers worked out new circuit topologies specifically suitable for CMOS [6]. Some of these innovative circuit designs required on-chip passive devices, hence came the first passives on Si. Eventually, the number of integrated passive devices increased with the research on RF CMOS circuits leading to an era of Si passive integration.

The first examples of integrated passives in RF CMOS circuits came out in early 90's and the efforts towards the development of single chip RF CMOS transceivers is going on ever since [7, 8]. However, industry acceptance of the concept is still away from completion. Current wireless communication devices employ a mixture of technologies forming a hybrid circuit. CMOS is used for baseband signal processing and for low intermediate frequency (IF) in general [9], GaAs heterojunction bipolar transistors (HBT) are preferred for power amplifiers (PA), and a mixture of on-chip and off-chip passives are used for various functions from biasing to matching. Considering the passives, there are several handicaps that are hampering fully-integrated, single-chip devices. The most pronounced problem is

the effect of the Si substrate which was originally adopted to meet the needs of digital CMOS, not RF. The conductive nature of Si causes various problems for RF passive devices having detrimental effects on inductors in particular. It is instructive to explain these effects using a lumped element spiral inductor model given in Figure 1.4.

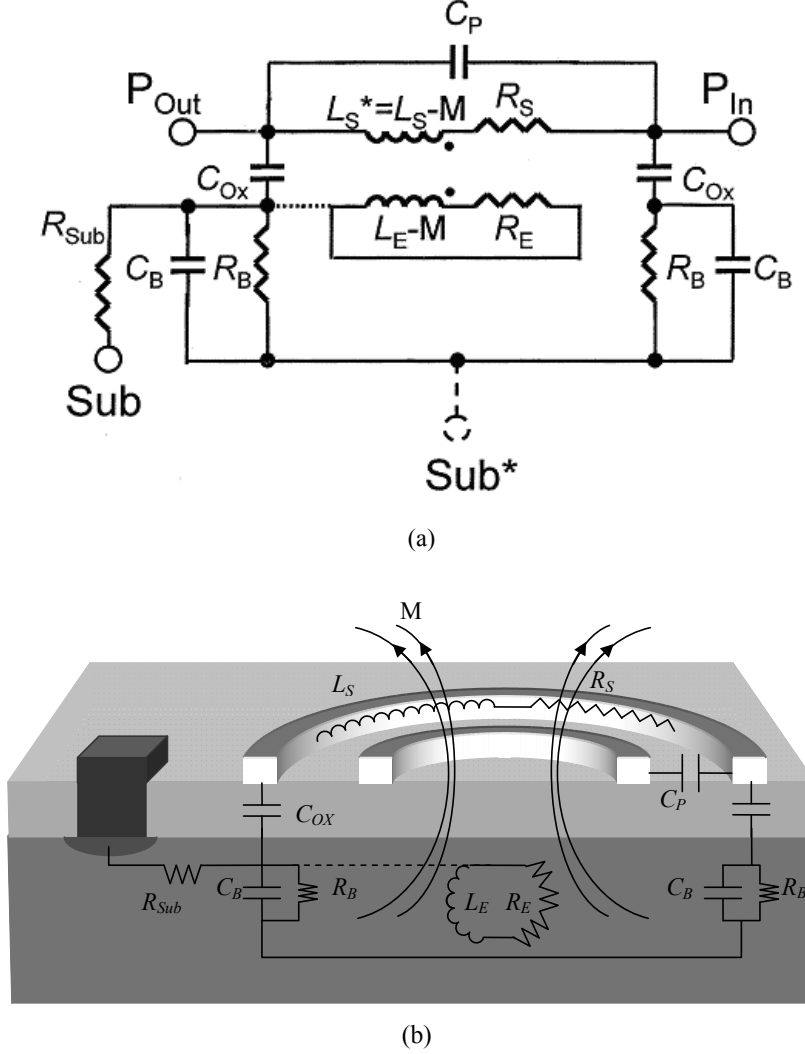


Figure 1.4: Lumped-element model of a spiral inductor on a lossy silicon substrate; a planar substrate contact (Sub) and an ideal substrate contact (Sub^*) are indicated. The spiral metal coil is represented by L_S^* , R_S , and C_P , the leakage current through the substrate by C_{Ox} , R_B and C_B , and eddy currents in the substrate by $L_E - M$ and R_E (including eddy currents in a ground shield). The resistor R indicates the electrical effect of a ground shield layer inserted between the spiral coil and the substrate (excluding eddy currents) [5].

The first and foremost effect is the RF power leaking into the substrate through the MOS capacitance formed between the metal windings comprising the inductor and the conductive Si substrate, modeled by the two lumped capacitors C_{OX} . The flow of the RF power into the substrate is accompanied by additional ohmic losses in the latter, causing a major reduction of the inductor quality factor (Figure 1.5). Besides, the RF current which enters the conductive substrate can travel long distances eventually reaching other devices on the chip. This causes major crosstalk problems and is a subject of intensive research. In addition to parasitic currents induced by the capacitive substrate coupling, one has to consider the effect of substrate eddy currents that are induced as a result of the relatively high magnetic field at the center of a spiral inductor. The flow of substrate eddy currents leads to a minor reduction of the device inductance but, most important, it generates extra ohmic loss leading to further aggravation of the inductor quality factor. Note, that although Si substrate loss is discussed here specifically for integrated spiral inductors, it is equally crucial for other lumped or distributed passive elements such as capacitors, transformers, and transmission lines. In addition to substrate loss, Si-based integrated devices may suffer from the relatively high dielectric constant of the substrate. In case of a spiral inductor, this leads to a large interwinding (C_P) which lowers the resonance frequency of the inductor.

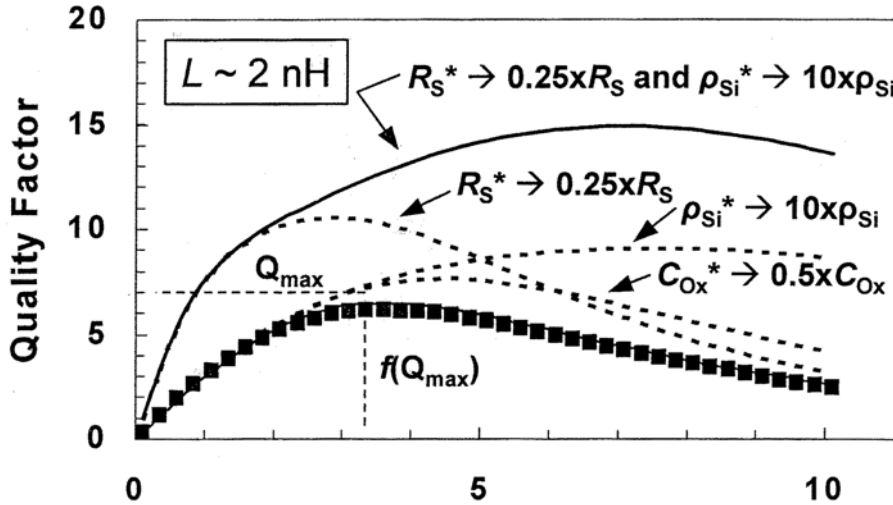


Figure 1.5: Simulated and measured (markers) quality factors (Q) of a circular spiral aluminum inductor ($R = 120 \mu\text{m}$; $W = 13.7 \mu\text{m}$; $S = 10.3 \mu\text{m}$; $N = 4$; $T_M = 1 \mu\text{m}$; $T_{OX} = 4 \mu\text{m}$; $\rho_{Si} = 5 \Omega\text{cm}$); the sensitivities to changes in metal thickness ($T_M \rightarrow 4 \mu\text{m}$, i.e., $R_s^* \rightarrow 0.25 \times R_s$), oxide thickness ($T_{OX}^* \rightarrow 8 \mu\text{m}$, i.e., $C_{OX}^* \rightarrow 0.5 \times C_{OX}$), and silicon resistivity ($\rho_{Si} \rightarrow 50 \Omega\text{cm}$) based on simulation are indicated [5].

It is important to note that the limitations of the contemporary passive integration techniques are not merely caused by the Si substrate. The CMOS process is optimized for digital circuits and the metal layers are primarily optimized for dense interconnections. Hence they require small pitch, leading to thinner metal layers (Figure 1.6) [10-15]. When used to implement passive elements, those thin metal layers lead to increased conductor loss. For a spiral inductor, this implies a large series resistance R_s , which directly adds to the power loss in an inductor. The second problem is associated with the 2D nature of passive elements integrated by using a conventional IC process. This limitation in the third dimension hinders the implementation of geometries such as vertical solenoids, which has some inherent benefits compared to planar spiral inductors [16-18]. Also fabrication of completely shielded transmission lines such as coaxial cable becomes unfeasible in a standard CMOS process. Besides, strict limitations in the third dimension make some designs such as microstrip lines unattractive or severely limited.

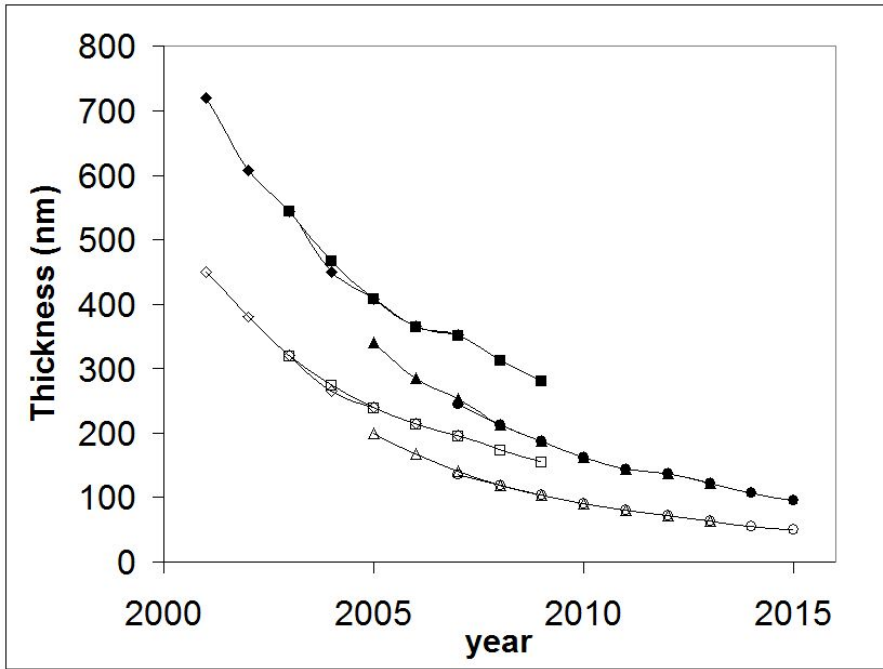


Figure 1.6: CMOS interconnect wiring pitch and thickness projections from the ITRS reports of 2001 (◇ pitch ♦ thickness), 2003(□ pitch ■ thickness), 2005 (△ pitch ▲ thickness), and 2007 (○ pitch ● and 2007 thickness).

1.3. Conservative vs. Innovative Approach

With every new CMOS technology node the performance of the passives degrade more and more [10]. For that reason, the above mentioned integration problems have been investigated thoroughly by the research community, and several optimization techniques and novel designs for CMOS technology have been proposed. Some of these novel designs such as differential inductor layouts [19], ground shields [20], tapered metal strips [21], and metal stacking [22] are accepted by the industry.

These techniques, although beneficial, do not provide enormous improvements to the circuit designers. Therefore researchers have also been working on solutions which involve deviation from mainstream CMOS technology, offering an additional degree of freedom and flexibility. Eventually, however, industry acceptance depends on CMOS compatibility and standardization. Hence, the field is converging towards techniques that can at some level be combined with CMOS. Technologies aimed at reducing the substrate loss try to either alter the substrate beneath the passive device or to increase the distance between the substrate and the device itself. Proposed strategies to alter the substrate include local silicon removal [23], local silicon dioxide [24] or porous silicon [25] well formation, increasing substrate resistance by local proton bombardment [26], or using high-resistivity substrate [27]. Separating the substrate from the device is achieved by using thick organic films such as benzocyclobutane (BCB) [28] or SU-8 [29]. As for the reduction of conductor loss switching from Al to higher conductivity Cu and using BCB, SU-8 type thick molds or lithographie-galvanaförmung-abformung (LIGA) technology to achieve thicker electroplated Cu metallization [30, 31, 32] are some of the technological solutions. These technological solutions are described in detail in Chapter 2 together with other technologies such as flip-chip packaging, through-wafer vias, and copper electroplating.

1.4. Objectives

This work intends to explore two innovative solutions to improve the performance of integrated passive elements on Si substrates. The first solution aims at the fabrication of interconnects and wires with a high-aspect-ratio (HAR) on the chip surface by means of Cu electroplating. The aim is to optimize the photoresist mold to achieve a near vertical wall profile, since this wall profile is the limiting factor in the aspect ratio of the final structures. The second solution to be explored is the fabrication of HAR passive elements embedded within a Si substrate. This will be based on deep reactive ion etching (DRIE) to etch trenches into the silicon substrate. Later these trenches are filled with electroplated Cu to form HAR conductors

embedded into Si substrate. The process intends to benefit from the vertical wall profile of DRIE to improve aspect ratio of the final structures.

HAR structures are expected to introduce vertical sidewalls that would serve as additional space for current reducing current density, hence resistance in RF passive devices that would in turn increase their RF performance. This benefit would be better observed in structures with tightly packed parallel conductors such as spiral inductors and coplanar waveguides. In order to observe the effects of HAR process, various devices will be implemented on both high resistivity (HRS) and low resistivity (LRS) silicon substrates and compared to standard components. Besides demonstrating the performance improvement introduced by the process, this work intends to show the changes in the design rules accompanying HAR devices.

In addition to the exploration of HAR devices, we will investigate the effect of metallization on the thermal behavior of spiral inductors in high-power RF circuits. In particular, we will focus on the thermal behavior of micromachined spiral inductors which have gained popularity in recent years due to their high quality factor.

The outline of the thesis is as follows. Chapter 2 will be dedicated to a discussion of technological solutions to problems encountered in passive device integration. Chapter 3 investigates the performance of spiral inductors fabricated using various technologies. These include two different metallization options and two substrate types to make comparisons and evaluate them in terms of RF performance. Chapter 4 explores self-heating of suspended inductors in high-power RF circuits. These inductors are fabricated using the processes described in Chapter 3 and an additional DRIE process. Finally, Chapter 5 focuses on both on-chip and substrate-embedded transmission lines fabricated using the HAR process.

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Chapter 2

RF Passive Device Integration in Silicon: A Technology Perspective

2.1. Introduction

A modern wireless communication device, such as the highly popular cell phone, is composed of different blocks that perform their designated functions. A controller unit for managing all functionality, a baseband processor to perform encode/decode and modulation of voice, message, and data, and an RF transceiver to adjust the frequency of the signal and transmit it to air and receive incoming signals. Controller and baseband processor are digital circuits that are implemented with silicon CMOS technology. However, an RF transceiver consists of different circuit blocks such as low noise amplifier (LNA), local oscillator (LO), mixer, and PA. Due to their difference in functionality, each block has different requirements. These requirements are met by using different device layouts, and by using a different technology for manufacturing each component [1]. For example LNAs can be fabricated in Si or SiGe technology, while PAs generally require GaAs-based processing. In order to achieve a high level of integration one has to aim not only for novel circuit designs but also for advancement in technology which would help in integrating an increasing number of circuit blocks on a silicon substrate. This chapter will summarize the efforts made on the technology side to improve the level of integration of passive devices.

Regarding their integration level, passive device technologies can be divided in three groups. In the system on board technology one or more active device chips are mounted and soldered onto a circuit board together with discrete passive components or chips containing a number of passives. At this level, passive devices can also be implemented using the metal tracks of the circuit board itself. This can be seen as the lowest level of integration for commercial systems. The system in package (SiP) concept defines the next integration level, where two or more chips are brought together in a single package and are connected via wire bonds or solder bumps. Finally, the highest integration level is offered by the system on chip (SoC) technology, where everything is fabricated on the same substrate and then packaged. Despite their differences, these technologies (especially SiP and SoC) share several technologies that originate from integrated circuit processing and micro-electro-mechanical systems (MEMS) or micromachining technologies. Since SiP and SoC are heavily dependent on micromachining technologies, they are viewed as the cradle of technologies that will enable monolithic implementation of multiple blocks and components on a Si substrate. Motivation behind this work is developing micromachining technologies that will improve passive elements both in performance and in the integration aspect. Therefore SiP, SoC, and the associated technologies will be explained in more detail in the following sections.

2.2. System in Package Technologies (SiP)

SiP is a concept where multiple chips are brought together inside a single package to form a complete system. Here the package is not merely viewed as a mechanical carrier and protecting physical cover but, as an integral part of the system that performs various functions such as forming an electromagnetic shield for better isolation, acting as a high quality substrate for passive device implementation, or even forming a cavity that can be used as a resonator as part of a filter. Such a mindset would require additional focus on packaging technologies and their implications on the system performance and functionality. Hence the system architecture is not just about the chip design, but the design of interconnects between chips and the connections from chip to package and the design of the package as well.

SiP designers are interested in technologies that improve chip-to-chip or chip-to-package connectivity and technologies that allow different packaging concepts as a result of the aforementioned design requirements. These interconnect technologies are very important for the passive device implementation on packages and their performance. Therefore, several interconnect technologies, used in SiP, and their implications on passive devices are investigated in the following section.

2.2.1. Interconnect Technologies

The early example of what would be called as SiP is a multi-chip module, where multiple chips are placed inside a Dual in-line Package (DIP) or similar package type and connected to each other as well as to the input and output terminals of the package via wire bonds. Hence, wire bonding is the first interconnect technology to be used for SiP. Bond wires are made of gold, aluminum, or copper [2]. They are 15-75 μm in diameter and several hundred μm long. Current wire bonding equipment supports 60 μm bond pad pitch. Advanced wire bonding devices can perform fine pitch multi-layer connections as seen in Figure 2.1.

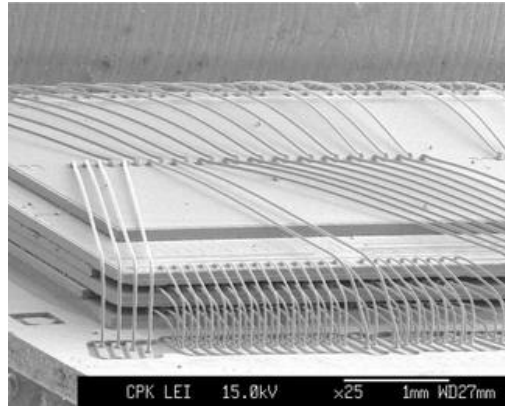


Figure 2.1: Multilayer fine pitch wire bonding example.

Wire bonding is the dominant interconnect technology for die to package connections. It is a well established process. Hence equipment, technology, and materials are abundant. Bond wires themselves provide low resistance per unit length, thanks to their relatively large cross sections. However, contact resistances and parasitic capacitances formed between the wire and the chip and/or the package reduce this advantage and create a low pass filter that limits RFIC performance [3]. Moreover, the parasitic inductance of a bond-wire is not negligible: a ~ 1 mm-long bond wire introduces a parasitic inductance of $\sim 1\text{nH}$. While this is a generally undesirable effect that degrades RF circuit performance, it can also be used to manufacture bond-wire inductors that are integrated into the circuit functions [4] in some cases. Nonetheless, for both applications wire bond length, curvature, and contact quality must be precisely controlled in order to anticipate the parasitic effects accurately, reduce the inductance and Q factor variation, and reduce design error margins. Since wire bonding is a serial process in nature, such parameter control is more difficult compared to planar on-chip interconnection, which is based on a batch process. Also serial processes have higher cost per unit compared to parallel processes. Another issue related to wire bonding is the integration density. Wire

bonding provides $60\text{ }\mu\text{m}$ bond pad pitch, which becomes an issue as the complexity of the modern systems require finer pitch for ever increasing number of connections.

In order to overcome the problems associated with wire bonding, flip-chip interconnects are developed. In this case bond pads are formed on both the chip and the package surface, the chip is flipped over and the corresponding pads on the die and package are connected together using either solder bumps, or conductive adhesives as seen in Figure 2.2. Flip-chip connections are vertical as opposed to lateral wire bonds. Hence the entire surface of the chip can be used for interconnects and only the area below the chip surface is required for package or board connection pads. This gives flip-chip connections an advantage in integration density compared to wire bonding.

Another advantage of flip-chip is the parallel nature of the process. All the connections on the chip are made at the same time. This reduces the risk of error, hence the cost by increasing yield.

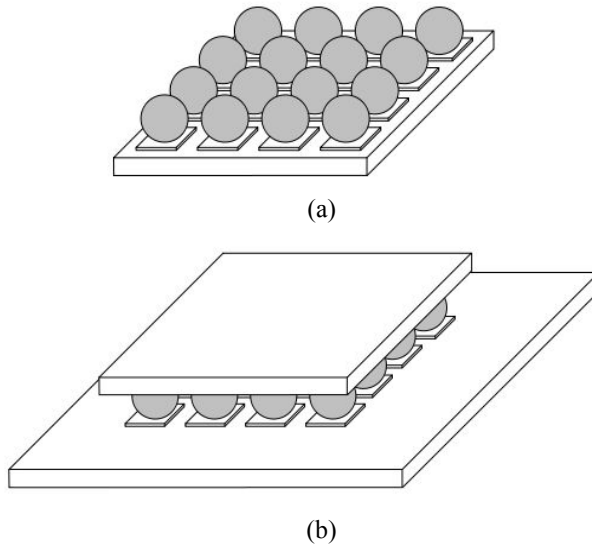


Figure 2.2: Flip chip bonding

The main disadvantage of this process is the problem of reliability due to stress induced on the mechanical connections. Since the solder balls are very small compared to bond wires, they are very rigid. They can not well distribute the stress generated by the mismatch between the thermal expansion coefficients of the two chips. This leads to fracture and, with time, the complete loss of connections. In order to overcome this problem, the underfilling technique is used to fill the voids between solder balls in order to redistribute and reduce the stress. Underfilling requires extra lateral space on the chip, hence reduces the integration density. Besides, underfill materials, which are highly protected trade secrets, that are a mixture of an epoxy

resin, fill powder from metals or ceramics, and a catalyst for curing, are costly, raising the final cost of the product. Although more costly than bond-wires, flip chip connections have significantly less parasitic inductance and resistance, hence they are preferable in terms of performance improvement and reduced design margins.

An important connection concept that can be used in conjunction with flip-chip bonding is the front-to-back connection. Such a connection, in combination with flip-chip bonding technology, can be used to implement multichip stacks as seen in Figure 2.3 to include all the functions necessary to form a complete system in a single package. Moreover, it offers the additional benefit of being able to use the backside of a wafer for various purposes such as implementing passive components, ground planes, or input/output pads. This concept is realized using different technologies grouped under the name micromachining. Initial step for such a connection is the realization of a via through the substrate material itself. In silicon this type of opening can be realized with various methods, such as anisotropic wet chemical etching [5], laser ablation or cutting [6], or DRIE [7]. Then inside of the via needs to be covered with an insulating layer. Next, a metallic connection should be made through this via that will electrically connect the front side to back side. In case of wet anisotropic etching this connection is made by laying metal tracks using lithography [5]. In case of a HAR vertical via, a complete filling of the via with metal using bottom up electroplating is preferred [7]. It should also be noted that, in case of a silicon substrate and copper metallization diffusion of Cu into Si occurs since Cu has a high diffusion coefficient. Diffusion of Cu or other metals into Si substrate results in them acting as generation recombination centers, which is detrimental for device operation and reliability. Therefore a diffusion barrier should be present between copper and silicon. It is possible to form such a layer by means of atomic layer deposition (ALD), which has the peculiar advantage of performing uniform conformal deposition on extreme geometries.

Although it is still a process that is only realized at laboratory level, and has not reached the maturity to implement repeatable and reliable connections, a via formed using DRIE and filled with copper using electroplating can be considered state of the art in terms of through wafer connections. Nonetheless, both technologies are also employed in IC processing and are expected to be cost effective. It is also a process that can have benefits for SoC approach, by allowing the use of backside of the chip for adding functionality.

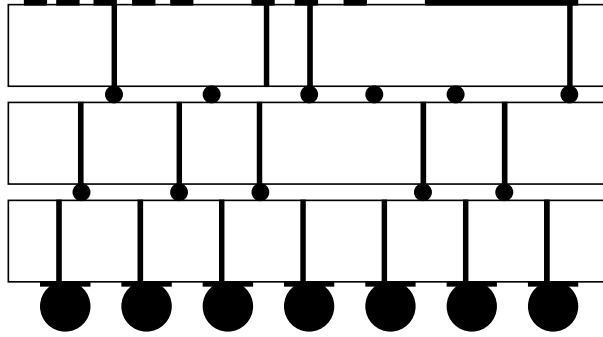


Figure 2.3: Example of a multichip stack SiP.

The chronological development of the three SiP interconnect technologies discussed above (bond-wire, flip-chip, through-wafer) can be viewed as an indication of what is to come in the future. As technologies advance they will either be eliminated or converge to a point where everything is batch produced and IC processing compatible, hence can be implemented in a single process flow on a common substrate. This convergence point is named SoC. The next section will briefly explain the technologies involved in SoC from the view point of RF passive device design and implementation.

2.3. System on Chip Technologies (SoC)

As the name implies, the goal of SoC is to implement all the functions required in a system on a single chip. Therefore everything must be fabricated on the same substrate wafer in a well-designed batch microfabrication process. Considering the dependence of modern wireless communication systems on digital processing and modulation, and the maturity of silicon CMOS processing, the substrate should be Si or SiGe type and the process should be compatible with CMOS. Since performance of passive devices fabricated on Si substrates using CMOS metal layers are generally poor, researchers have been working on process technologies that can be used to improve the performance of the passive devices. These processes aim at incorporating features and functions available in hybrid RF systems into a monolithic system.

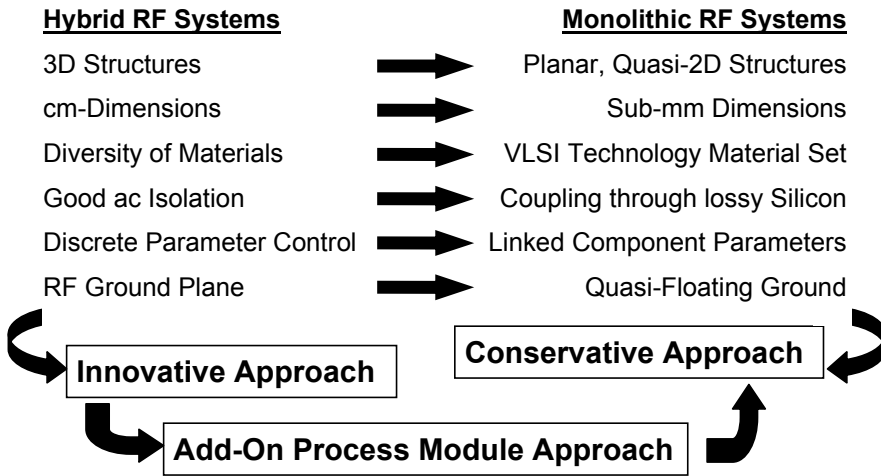


Figure 2.4: Differences between the natures of hybrid and monolithic systems are listed and possible connections are proposed [8].

Switching from a hybrid to a monolithic system concept requires a modification of a number of fundamental technological features as shown in Figure 2.4. Whereas it might be possible to adopt innovative and exotic processes to enforce these changes, such a policy is often incompatible with the short time to market requirements of the industry. Hence a more conservative approach, which allows for little change in the core process, is preferred. This conflict can be overcome by designing processes which, while innovative, can be introduced as enhancements to the core process. These add-on modules can introduce the required flexibility without the cumbersome work of changing the core process. In the following paragraphs add-on technologies that can be applied to improve passive device performance are discussed.

2.3.1. Substrate Removal

Since Si used in CMOS processing is lossy in nature, add-on processes aim to either get rid of the Si itself or separate the passive device from the substrate as much as possible. The first and foremost method of doing this is by (locally) removing the Si substrate by either wet chemical or reactive ion etching [9-13]. Substrate removal can be done from the front side of the wafer as seen in Figure 2.5 (a), (b), and (c). In case of front side wet chemical processing, anisotropic Si etching is preferred to isotropic etching in order to limit the chip area consumption by reducing the undercut. Yet, even with anisotropic wet etching, the area used for the inductor increases considerably as seen in Figure 2.6. Larger and deeper wells underneath the inductor

are preferred to reduce the amount of field travelling through the substrate, hence increase the isolation of the inductor and reduce the parasitic effects by actually lowering C_{OX} in Figure 1.4 (a). It is possible to get deeper wells by using a combination of isotropic and anisotropic RIE in a smaller area [14] as seen in Figure 2.5 (c). However, a better approach would be backside etching, which would reduce the amount of undercut as seen in Figure 2.5 (d), (e), and (f). In case of backside etching still anisotropic wet etching is preferable to isotropic wet etching due to better process control. Also DRIE can be used to remove the substrate from backside without increasing the area consumption [13].

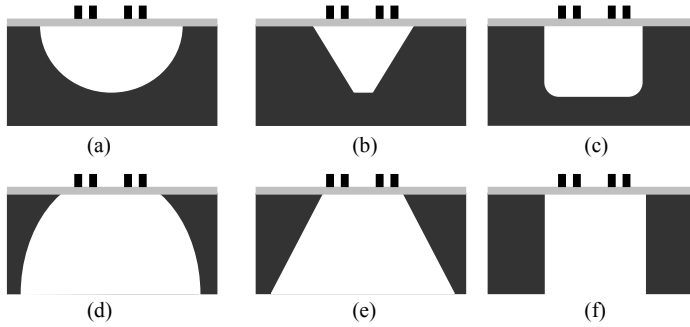


Figure 2.5: Cross section of various micromachining process (a) front side isotropic wet etch, (b) front side anisotropic wet etch, (c) front side DRIE, (d) back side isotropic wet etch, (e) back side anisotropic wet etch, (f) back side DRIE.

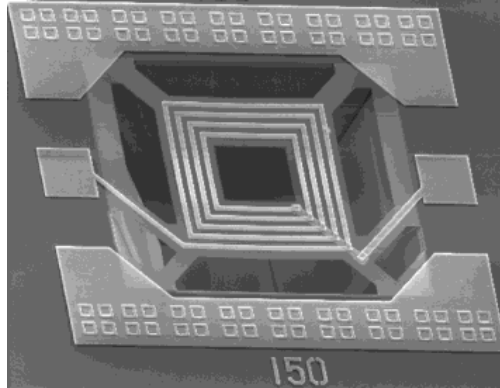


Figure 2.6: A spiral inductor fabricated using front side wet anisotropic etching [15].

Removal of the Si substrate improves the quality factor of inductors significantly. Also the resonance frequency of inductors is increased due to reduction in parasitic capacitances (Figure 1.4 (a)), which makes them more suitable for broadband RF applications. Moreover, the leakage of the electric field into the

substrate is further reduced, which diminishes the crosstalk. Note, that further reduction of crosstalk can be established by grounding the cavity i.e. by using electroless copper plating process to coat the inside of the cavity and to connect it to ground [16]. Substrate removal can also reduce the loss of transmission lines. Besides, it lowers the line dispersion as the medium surrounding the line gets more uniform after Si removal (important for high-frequency broadband applications) [17]. But, it also results in a lower effective dielectric constant, which leads to an increase in the propagation wavelength and, thus, the physical dimension of the device.

It is important to bear in mind that application of Si etching results in structures supported by thin layers of a dielectric material such as SiO_2 . Such suspended structures are not as mechanically stable as structures implemented on a solid substrate. Therefore extra care has to be taken during processing and packaging to ensure their mechanical reliability. Stress accumulated in the layers during fabrication can lead to buckling of the structures. Spiral inductors with a long thread of metal that is not held together with at least a dielectric membrane can have short circuiting of the windings due to shifts as a result of this buckling. Similar adverse affects can be also observed in the longitudinal axis of a transmission line.

Also suspended inductors owe their superior performance to the free space environment ($\epsilon_r=1$). Therefore, best results are obtained if this free space environment is preserved during packaging. The same applies to transmission lines if the packaging plastic is a low quality lossy dielectric. This leads to a demand for packaging schemes other than completely enclosing them in plastic. These packaging methods use technologies developed for SiP, such as flip chip bonding, using anodic bonding or soldering or gluing.

2.3.2. Substrate Modification

A process that is compatible with standard packaging schemes, yet offers a performance improvement, is local silicon dioxide thickening [18,19]. This is done by etching trenches into the substrate using deep reactive ion etching and then thermally oxidizing the remaining Si to form a SiO_2 well below the passive device. An additional step is deposition of plasma-enhanced chemical vapor deposition (PECVD) oxide to fill in possible gaps and to reduce the roughness of the surface. Since thermal oxidation is in the nature of CMOS processing, this process is completely CMOS compatible. The oxidation process can take place prior to any CMOS processing since thermal oxidation requires very high temperatures. Since a DRIE process has an aspect ratio limit, the distance between trenches and the width of trenches increase as the depth of the well becomes greater. This in turn results in increased oxidation time and oxide thickness, which results in higher stress in the film. Also, with increasing the trench width, the resulting surface roughness will increase proportionally.

Instead of a SiO_2 well, it is possible to make a porous Si well under the inductor itself [20]. Porous Si has a high resistance, hence very low substrate loss. Porous Si formation is an electrochemical process, which does not require very high temperatures. It can be applied as a post process module due to this low thermal budget.

Similar to porous Si well formation, proton bombardment of the Si substrate is a step that would generate a high resistivity high quality silicon well [23]. Bombarding the substrate with a proton beam would create localized isolation regions where the resistivity of the substrate is raised from as low as $2\ \Omega\text{-cm}$ to several $\text{k}\Omega\text{-cm}$. This is a post CMOS process module, hence it does not affect the core process itself in terms of process flow. However proton bombardment alters the active device characteristics significantly, therefore it is not a fully CMOS compatible process. In order to use this process in combination with CMOS, proton bombardment has to be restricted to regions with only passive devices by means of appropriate masking which is, however, difficult to fabricate. An experimented mask had been made of 1 μm thick Al [24]. Also any processing after proton bombardment that requires annealing at $200\ ^\circ\text{C}$ reduces the effects of the process.

2.3.3. Dielectric Spacer

Above mentioned processes aim to either get rid of the substrate or alter the substrate material beneath the device to reduce the related loss. As a result, area beneath the device becomes unavailable for active device processing. Although it is not common to introduce any kind of device, be it active or passive, beneath an inductor, it may be required as a result of strict area limitations. Hence, a process that allows such design flexibility is always welcome.

A post process or so-called back-end module that can allow for active device fabrication beneath a passive device is the use of a dielectric layer based on polyimides to increase the vertical distance between the substrate and the passive device. These layers are deposited on the finished CMOS wafer, and the process does not alter the substrate beneath in any way. Hence it is truly an add-on module that is independent from the substrate and previous processing. The process starts with the spin-coating of the polyimide layer. Then, it is baked at a low temperature ($<200\ ^\circ\text{C}$), patterned and hardened by a final bake ($\leq 300\ ^\circ\text{C}$). Final step is the deposition and patterning of the metal layer, which is generally electroplated to both fill the contacts and form metal tracks. As seen from the cross-section of such a multilayer process presented in Figure 2.7, the process is performed over the CMOS layers and does not affect them at all.



Figure 2.7: Cross section of an inductor fabricated using Cu electroplating and BCB film separation [21]. 5LM BEOL refers to 5 layers of metallization at the end of a CMOS process. Inductor is fabricated using WLP-M1 layer and BCB-1 is used for separation.

For best results, especially for inductors, the dielectric layers used should have a low relative permittivity and tangent loss. As an example two common materials used in this process are BCB and SU-8 which have relative permittivity of 2.5 and 3.6, and loss tangent of 0.002 and 0.08, respectively. Both have relative permittivities less than that Si (11.9) and even SiO_2 (~ 3.9). Hence, BCB would be a good candidate for this technology. But, these benefits will only be effective if the implemented layers are thick enough to accommodate a large fraction of the electric field beneath the device. Otherwise, the field will reach the Si substrate underneath, rendering the whole process useless. Examples of processes with SU-8 layers up to $200\ \mu\text{m}$ [22] have been demonstrated for RF inductors, whereas BCB processes for RF inductors have been demonstrated up to $16\ \mu\text{m}$ [21]. Therefore trade offs have to be made when choosing the material for such a process.

Regardless of their name, these materials are organic, and mostly polyimide type. Polyimides have been used in humidity sensors for a long time due to their ability to absorb the ambient humidity and to indicate this absorption by changes in their relative permittivity or loss tangent. Although this is a desirable effect for humidity sensing, it is not welcome in case of RF passives; the level of the ambient humidity will thus affect the electrical parameters of the passive device. Therefore such devices have to be isolated in a hermetic package, which is more expensive than a standard package, to ensure stable operation.

2.3.4. High Resistivity Silicon

Another option is to use HRS substrate as a starting material for CMOS processing [25]. Resistivity of this material is not affected by thermal processing hence it provides a stable and easily modelable substrate. HRS substrates are not standard in CMOS processing hence they are not as cost effective as LRS substrates.

Having an HRS wafer as a substrate introduces the problem of latch up for CMOS devices [26, 27]. However, this problem can be overcome by implementing an n-well in the core process [27]. This n-well step is a robust well known process; hence it would not complicate the core CMOS process significantly. Another issue related to HRS wafers is the formation of inversion layers due to accumulated charges in the Si/SiO₂ interface. This inversion layer is simply a higher conductivity layer, which helps reducing the effective resistivity of the substrate. It can be prevented by introducing irregularities to the Si surface by means of argon implantation (destroying the crystal structure on the surface), or surface deposition of amorphous or polycrystalline Si [26]. These processes are called surface passivation techniques.

2.3.5. Metallization

In addition to substrate loss, whose reduction was extensively discussed in the above sections, passive components also suffer from conductor losses in the thin metal layers often used for their fabrication. Reduction of metal loss offers another option to researchers for improving the performance of passive components.

Technological approach to reduce the conductor loss usually involves the use of a higher conductivity metal, e.g. Copper (Cu) instead of Aluminum (Al), or increasing the thickness of the metal layers. Switching from Al to Cu, for instance, provides an improvement of approximately 50%. The introduction of Cu damascene process has enabled Cu metalization. It is the combination of an electroplating process that is used to fill vias laterally and a chemical mechanical polishing (CMP) process that is used to remove excess metal and form the patterns. Instead of lateral filling, bottom up Cu electroplating is preferred in micromachining processes as a metallization scheme. This type of electroplating would not require very strict control of the electrochemical solution and its additives to achieve maximum uniformity. Also bottom up electroplating would not require CMP, and the layout limitations coming with it. Another advantage of bottom up Cu electroplating is its ability to fill extreme geometries such as vias with aspect ratios over 15 that can be used to obtain through-wafer connections [28].

2.4. Conclusion

Passive devices implemented in standard CMOS process suffer from severe substrate and metal losses. In order to reduce these effects several add-on process modules have been developed. Although problems with metal loss are solved by using a common Cu electroplating process, several options exist for reducing substrate losses. Some of these processes, such as local substrate removal, thick oxide formation, and porous Si formation, replace the substrate beneath the passive device with air, oxide or porous Si. Other processes separate the passive device from the substrate by introducing a thick dielectric layer based on polyimides. Another process locally bombards the Si substrate with a proton beam to increase the resistivity of the substrate. Introducing an HRS wafer as a starting material is another option offered to reduce substrate losses.

These processes have been explained briefly in this chapter. Their advantages and disadvantages have been discussed. Although evaluation of these processes based on these advantages and disadvantages is possible, there is no convergence in industry leading to a leading process. There is still need for further research in order to deepen our understanding of passive integration technologies.

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Chapter 3

High Aspect Ratio Spiral Inductors

As outlined in the previous chapters, several micromachining technologies have been introduced in recent years to improve the performance of integrated RF passive devices on silicon substrates. This chapter is dedicated to a new technology for implementing very thick copper interconnections whose height is comparable or even larger than their width (HAR). The first advantage of the HAR technique is the possibility for reduction in the footprint of integrated interconnections and wires, which would significantly reduce coupling of the passive devices to the lossy Si substrate (C_{OX} in Figure 1.4 (a)). This, in turn, would reduce substrate losses (for low resistivity silicon) and increase resonance frequency (for both low resistivity and high resistivity silicon). In addition, HAR devices potentially benefit from a more uniform current distribution on the cross section of the conductors comprising them. This effect, which results in less conductor loss, is pronounced for spiral inductors investigated in this chapter more than other devices due to their special geometry and magnetic field distribution.

In order to investigate the effectiveness of aforementioned advantages HAR process is developed and several spiral inductors are implemented with this technology. The process is designed as an add-on module to be used after the core CMOS process. The detailed description of the module is presented in Section 3.1. Next, in Section 3.2, application of this technology to integrated spiral inductors is discussed and design aspects are investigated. Finally, in Section 3.3, the experimental data from implemented designs are presented and compared to a standard process.

3.1. Fabrication Process

The fabrication of HAR interconnections is based on an add-on Cu electroplating process that utilizes the top metal layer of an already fabricated chip. Although Cu electroplating is now common in CMOS processing, the technique used is different in HAR method. In the standard technique, called damascene processing, a dielectric trench or gap is filled with copper by electroplating from both lateral and vertical directions on top of a continuous seed layer [1]. Then the Cu layer on the top flat surface is removed by CMP to realize the pattern. The reason for adopting such a technique is the lack of a suitable dry etching mechanism that can enable the required pattern densities.

To implement HAR devices, however, we employ the classical vertical Cu electroplating method that uses a mold on top of a flat seed layer. There are several reasons for selecting this structure. The first reason is the flexibility and robustness of vertical electroplating. Damascene processing requires strict control of the electroplating solution in order to maintain an electroplating profile that fills the bottom of the valley first and has a fairly planar surface on the whole of the wafer at the end. Such planarity is required for the CMP process, which is applied afterwards, to uniformly pattern the whole wafer. Also CMP requires a certain level of pattern density and feature size that limits the flexibility of the process. Pattern density requirements, for instance, force the designers to put dummy fill patterns in empty areas [1, 2]. Also larger patterns need small islands or slits of uncoated area to ensure uniformity. Finally, damascene process is limited to aspect ratios of 5 or 6 at most, but vertical electroplating can achieve aspect ratios in excess of 15 [3].

The Cu electroplating process used in this work is designed as an add-on, post-CMOS module that enables the deposition of a thick, top-metal-layer in selected areas required for passive device implementation [4]. This method, called saddle add-on metallization (SAM), utilizes a single mask layer which results in reduced cost. Although it may appear that such a thick metal layer could have been naturally included in the core CMOS process in the first place, one should note that such a layer could not meet the fine pitch requirements of CMOS since feature size increases with the thickness of the metal.

The SAM process starts from a finished CMOS wafer where the final metal layer is deposited and coated by a passivation layer to protect the chip from the environment. There are contact openings in this passivation layer over the bonding pads to make electrical connections to the outside. This contact mask can be modified to include the metal tracks of the passive devices. In this case both the bonding pads and the RF passive devices would come open as depicted in Figure 3.1.

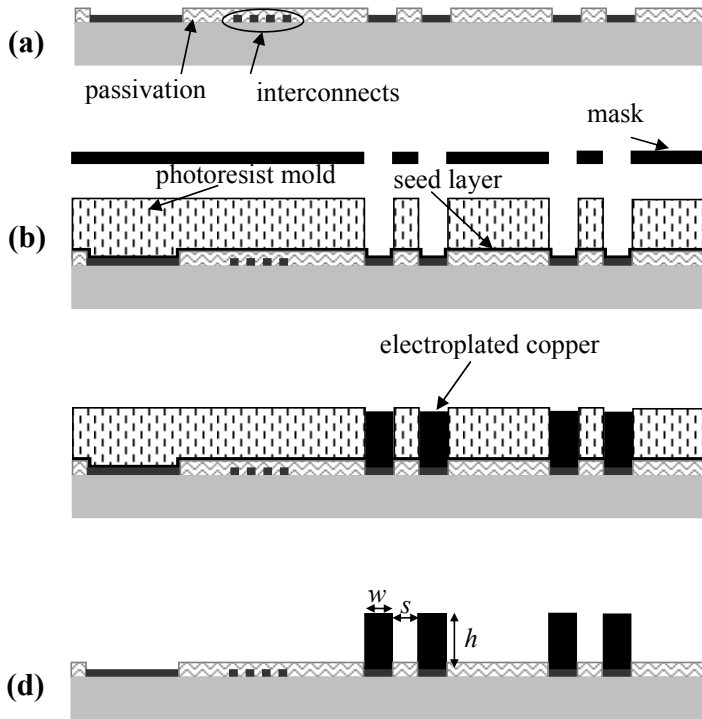


Figure 3.1: Graphical description of the process steps in the SAM process module. (a) Initial wafer with both interconnects, bonding pads, and inductor tracks on the same metal layer. Surface is passivated except for the bonding pads and inductor tracks. (b) Seed layer of Ti/TiN/Cu is coated on the wafer. AZ4562 photoresist mold is coated and patterned with the mask. Notice that bonding pads are not opened during patterning. (c) Cu is electroplated. (d) Photoresist and the seed layer is removed.

After receiving the finalized wafer, a Ti/TiN/Cu (10 nm/40 nm/300 nm) stack is sputtered onto the wafer as the seed layer. Ti acts as an adhesion layer, which ensures that subsequent layers are properly connected in physical terms to the underlying Si or SiO₂ layer. It is used due to the poor adhesion quality of Cu. TiN acts as a diffusion barrier to prevent Cu from diffusing into Si or SiO₂. It is an important layer since Cu in Si acts as generation-recombination center and impact active device characteristics. To form the mold, AZ4562 photoresist was spin coated at 800 rpm to obtain a layer approximately 18 μm thick. Then it was exposed with UV mask aligner, and developed to obtain a mold later to be filled with electroplated copper. Cross section of such a mold can be seen in Figure 3.2.

After electroplating, the photoresist is stripped by acetone and the remaining seed layer is etched with a wet etching solution of $\text{Na}_2\text{S}_2\text{O}_8/\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ (for Cu) followed by a H_2O_2 solution that is heated up to 60°C (for Ti/TiN). This etching step, while slightly different from the process described in [4], improves the selectivity of the solution to reduce the unwanted etching of any Cu or Al layer on the wafer. In the selectivity tests no measurable etching was recorded on both Al and Cu metal layers while etching the Ti/TiN layer. This would enable the use of both Cu and Al as the underlying layer as opposed to just Al in the reference case.

The bottom up electroplating scheme described above allows a diverse geometrical variation which, when combined with HAR photoresist molding, enables the implementation of HAR interconnections, inductors, and transmission lines. (Aspect ratio of a structure can be defined as the ratio between the height h , and width w or spacing s . When this ratio is greater than 1, the structure is called high aspect ratio or HAR).

It is important to bear in mind that the side walls of the photoresist mold are not ideally vertical because of the sloping of the line due to diffraction of light in the photoresist medium [6]. This phenomenon limits the aspect ratio of the fabricated devices since the width of the final structure is larger than the nominal width implemented on the mask. Similarly, the spacing s between adjacent lines would be smaller than the design value as shown in Figure 3.3. Hence, if the depth of the valley exceeds a critical value determined by the minimum s , the metal tracks would connect with each other and would thus result in short-circuit.

In this work an aspect ratio of three was obtained for the electroplated copper inductors. Minimum feature sizes, namely the minimum w and s and maximum target height h , were $5\text{ }\mu\text{m}$, $5\text{ }\mu\text{m}$, and $15\text{ }\mu\text{m}$, respectively. The key factor in determining these dimensions is the availability of a mold layer that can support this aspect ratio. In this case AZ4562 photoresist was selected as a mold layer due to its ease of deposition patterning and removal. Although AZ4562 can be spin coated with thicknesses in excess of $200\text{ }\mu\text{m}$ [5], this would require a special spinner machine that rotates its lid together with the wafer to achieve such thicknesses. In case of a standard spinner recommended thicknesses are around $10\text{ }\mu\text{m}$. As the speed of the spinner is reduced to achieve thicker layers, thickness profile of photoresist becomes nonuniform towards the edges forming a hill due to surface tension of the photoresist [6]. This makes part of the radius of the wafer unusable. Considering such a tradeoff photoresist thickness slightly higher than $15\text{ }\mu\text{m}$ is targeted in this work. This resulted in determining a target metal height of $15\text{ }\mu\text{m}$.

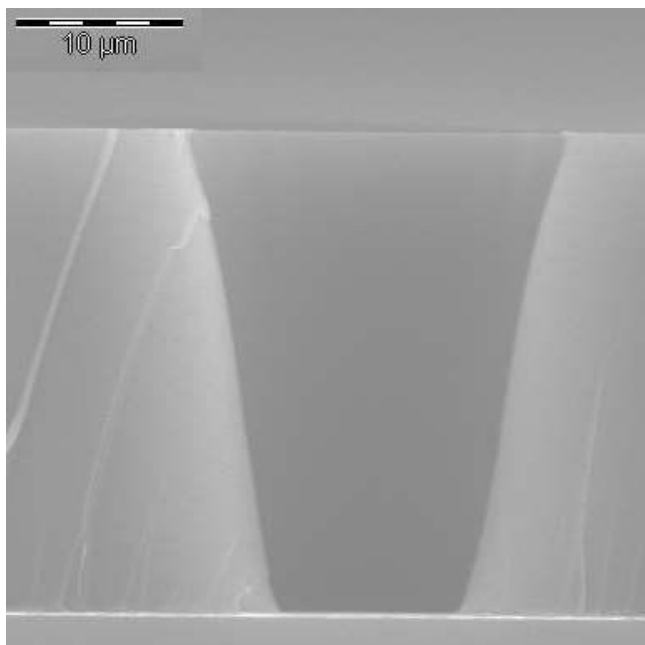


Figure 3.2: SEM Cross-section of an AZ4562 photoresist mold after exposure and development.

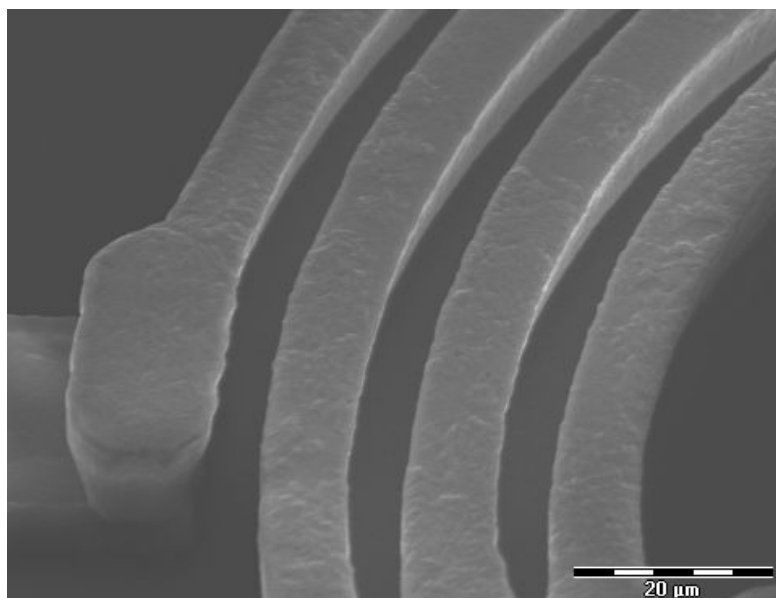


Figure 3.3: SEM picture of a final electroplated inductor. Slope of the sidewalls follows the photoresist profile given in Figure 3.2.

The components fabricated utilize two different metallization processes that are applied on two different substrates. The substrates are low resistivity silicon with a resistivity of 2-4 Ωcm , and high resistivity silicon with a resistivity of 1 $\text{k}\Omega\text{cm}$. The standard metallization process involves the deposition of a 3 μm -thick Al layer that is performed in two steps (1.5 μm each). After each sputtering step the 1.5 μm Al layer is patterned by lithography and dry etching to relieve the stress caused by the sputtering process. This Al layer is used as a reference process to represent the standard metallization layers in factory runs.

3.2. High Aspect Ratio Inductor Design and Performance

The process mentioned in the previous section is not just a simple means to reduce conductor loss. One should bear in mind that thickening the metal, while highly effective at low frequencies, is less useful at high frequencies due to the skin effect. Skin effect is the result of eddy currents forming inside the conductor in response to the alternating magnetic field of the current itself. These currents lead to a highly non-uniform distribution of the current inside the conductor, restricting it to a narrow region near the conductor surface. Moving into the conductor from its surface, the magnitude of the current density J drops exponentially and is given by

$$J = J_s e^{-d/\delta} \quad (3.1)$$

where J_s is the current density at the surface, d is the distance from the surface, and δ is the skin depth given by

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \quad (3.2)$$

where ρ is the resistivity of the conductor ω is the angular frequency and μ is the magnetic permeability of the conductor. As an example skin depth of a copper wire at 1 GHz is 2.06 μm and at 4 GHz it drops to 1.03 μm . Thus, since the current is restricted to the surface, using a metal layer much thicker than δ makes little sense as it will not carry the current anyway. (Actually, the usual rule of thumb is that making the metal thicker than 3δ will not further help reduce the overall resistance.)

So, what is then the advantage of building on-chip metal structures taller than their width? One should note that HAR process opens up the possibility to move from the usual planar 2D metal structures to true 3D conductors. This may, in future, lead to the realization of novel passive devices. But, what about the common inductors and transmission lines we are after? Is it not true that skin effect renders excessive conductor thickening useless? To answer this question one should note that skin effect is not the only phenomenon caused by the self induced magnetic field. Another

phenomenon is the non-uniformity of the current density distribution on the ‘surface’ of the conductor. In 2D planar conductors this effect – caused by the component of the magnetic field normal to the conductor surface – manifests itself as a current distribution which is high near the edges, but low near the center as seen in an HFSS simulation result presented in Figure 3.4. If two or more wires are brought close to each other, this effect gets worse (proximity effect). The microwave magnetic field of each conductor produces eddy currents inside the neighboring one, hence altering the current distribution. As a result, when two adjacent wires have current flowing in the same direction current density at the opposite sides of the wires tend to be higher than the current density at the sides facing each other.

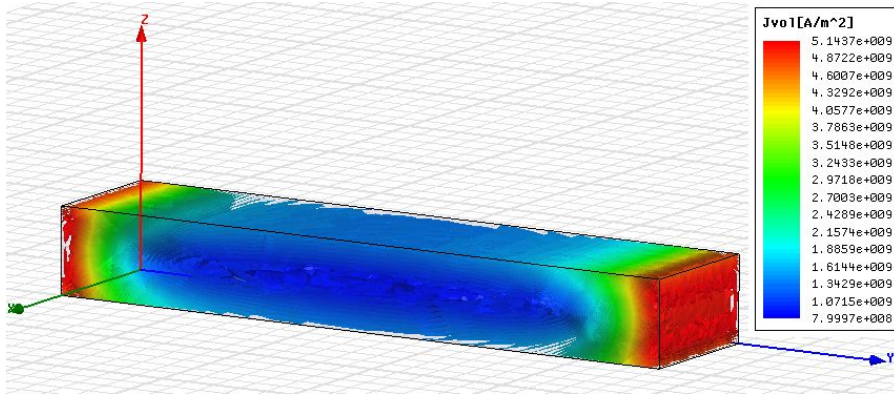


Figure 3.4: Current distribution inside a thin wide single conductor in x direction as seen from a cross section in y-z plane.

In case of a spiral inductor where several windings result in several parallel strips of conductors with the same direction of current, proximity effect is reduced in the middle conductors. However as we go to the inner and outer sides, this effect becomes more and more significant resulting in current crowding on the side walls. In case of a typical spiral inductor layout an expected current distribution is depicted in Figure 3.5.

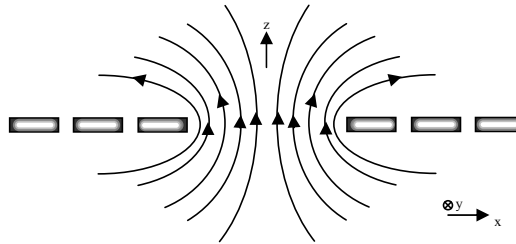


Figure 3.5: Current and magnetic field distribution for a spiral inductor cross section. Concentrated magnetic field in z direction in the center causes the current distribution to shift to the inner side wall.

The combination of skin effect and proximity effect reduces the effective cross sectional area of the conductors especially in the inner turns due to high magnetic field concentration. This results in higher total series resistance for the spiral (R_s in Figure 1.4 (a)). Three series resistance values are calculated for the same layout considering three cases to understand the effect of skin effect and proximity effect on inductor performance. The first case is the DC resistance where current flows through the whole cross section of conductor. The second case is the skin effect case where a single conductor is simulated to observe the current distribution under just skin effect. Finally, the third case is the spiral where both skin effect and proximity effect comes into play. For the sake of clarification it is important to mention that the calculations are done for the same layout, hence same cross sectional area and same total length. The resulting values of R_s for a conventional, 3- μm thick spiral inductor (inductor #5 in Table 3.2) are given in Table 3.1. At 0.8 GHz, for instance, the skin- and proximity effects cause a ~60% rise in R_s compared to the DC value. A proposed solution to this problem is the narrowing of the conductor towards the inner turns in a tapered manner [7]. However, this does not change the fact that the narrow conductor in the center still introduces a high resistance

Table 3.1: Simulated series resistances for two spiral layouts.

	Ind. #5 in Table 3.2 with 3 μm Al					Ind. #8 in Table 3.2 with 15 μm Cu				
F (GHz)	R_s DC	R_s skin	Skin/DC%	R_s skin+prox.	skin+prox./skin%	R_s DC	R_s skin	Skin/DC%	R_s skin+prox.	skin+prox./skin%
0	1.38					0.73				
0.3		1.41	2.59	1.71	21.4		0.78	6.56	0.88	12.6
0.4		1.44	4.38	1.86	29.47		0.81	11.1	0.94	15.67
0.5		1.46	6.36	2.01	37.27		0.84	15.54	1.01	19.42
0.6		1.49	8.45	2.16	44.73		0.88	20.32	1.08	22.93
0.7		1.52	10.64	2.31	51.7		0.91	25.11	1.15	26.34
0.8		1.55	12.77	2.46	58.21		0.95	29.8	1.23	29.65

It is here where the HAR structure, to move from 2D planar conductors to true 3D metal structures, is very effective. To understand this, consider a HAR spiral inductor. As seen in Figure 3.6, these conductors have tall vertical sidewalls, which provide enough space for the current to flow. Since these walls are parallel to the magnetic field distribution (normal to the substrate), the proximity effect is expected to have lesser implication for the current distribution and, thus, device performance. Note that the skin effect, though, will not change. In order to observe the current distribution of such a structure a 3D finite element electromagnetic (EM) simulation is performed using Ansoft's HFSS program. Calculated current distribution is given in

Figure 3.6. Current distribution tends to be higher in the inner sidewall of the innermost turn than the outer one. This imbalance changes in favor of the outer sidewall as we approach to the outermost turn. Table 3.1 shows the R_s values for a 15- μm thick HAR inductor (#8 in Table 3.2). The increase in resistance due to the proximity effect is much less compared to the conventional device.

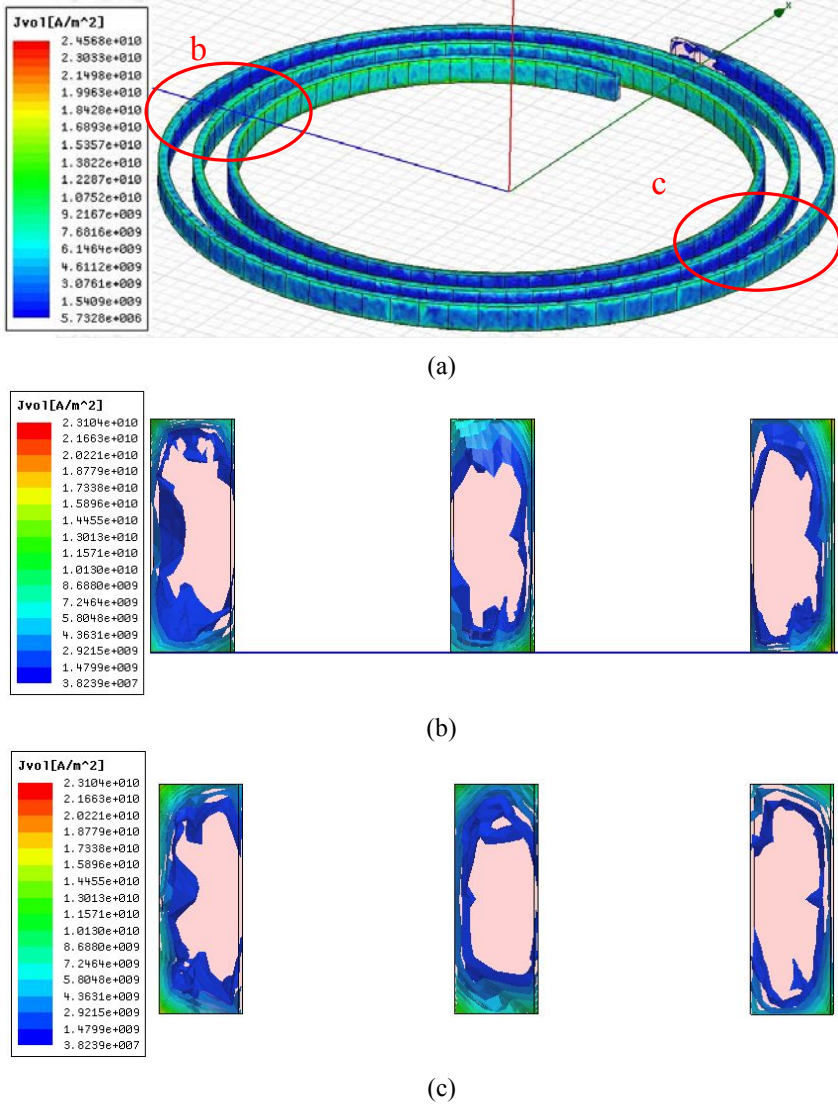


Figure 3.6: (a) Current distribution throughout inductor #8 of Table 3.2 simulated by Ansoft's 3D EM solver HFSS. (b) current distribution seen through a cross section on the left side of the spiral. (c) current distribution seen through a cross section on the right side of the spiral.

Besides current crowding, availability of HAR conductors can positively affect device performance in other ways. Since the conductor height is larger compared to a standard process, same series resistance R_s can be obtained with narrower conductors. For example a conductor cross section of $5\text{ }\mu\text{m}$ by $15\text{ }\mu\text{m}$ can either be implemented as a $15\text{ }\mu\text{m}$ wide $5\text{ }\mu\text{m}$ thick layer with standard processing or as a $5\text{ }\mu\text{m}$ wide $15\text{ }\mu\text{m}$ thick layer with high aspect ratio processing. The latter case would have $1/3$ of the oxide capacitance C_{ox} of the former case. This would increase the usable frequency range of the inductor itself especially for the lossy low resistivity silicon substrate.

3.2.1. Design Optimization and Benefits of High Aspect Ratio

The above discussion shows that the degree, to which a thick metal layer improves the performance of integrated passive components, depends on the device layout and frequency of operation. In addition, it depends on the relative importance of conductor loss and substrate loss. Therefore, general evaluation of the HAR technology requires detailed analysis of the performance improvement for different designs and substrates. In order to achieve this, a large matrix of inductors was designed. However, rather than randomly choosing the test inductor layouts, we first theoretically examined what the HAR technology can offer in terms of quality factor for a given value of inductance. This requires the application of layout optimization routines, which could simulate and compare a large number of inductors before choosing the right layout for the actual fabrication and characterization.

Inductor layout optimization demands time consuming 3D EM simulations, especially for thick conductors. Therefore, instead of full wave EM simulations, we employed a fast, but approximate technique based on the concentric ring model which is applicable to circular spiral coils and is shown to be fairly accurate [8]. We then looked for the inductor layout providing the highest quality-factor for a given inductance, frequency of operation, and fabrication technology (type of substrate and type, thickness, and width of metal layer). For a comparative study, the same optimization routine was applied to conventional inductors built using a $3\text{ }\mu\text{m}$ -thick Al layer. Moreover, comparable samples of HAR-based designs were also implemented in the standard Al technology. Finally, the optimization procedure was applied to both HRS and LRS substrates, to observe the effectiveness of the process for different substrate options. Two inductance values, 5- and 10 nH, were chosen for optimization. For each value the frequency of optimization was selected to yield $50\text{ }\Omega$ impedance, thus yielding 0.8 GHz and 1.6 GHz for 10 nH and 5 nH coils, respectively. In view of the practical limits set on the area consumption of (rather bulky) spiral inductors, we also considered the outer radius of the inductor as an additional parameter. Four different outer radii were chosen for each inductance value. Designs for 5 nH are presented in Table 3.2 and for 10 nH in Table 3.3.

Table 3.2: Design data for 5 nH inductors simulated with concentric ring model based inductor optimization program. L is the calculated inductance, r is the outer radius measured from the outermost wall of the spiral, N is the number of turns, W is the width of the spiral conductor, S is the spacing between each track, Q is the simulated quality factor at the optimization frequency of 0.8 GHz, l is the total length of the spiral, A is the area under the conducting tracks of the spiral, and ff is the fill factor, which is $100 * (1 - r_i/r)$, where r_i is the inner radius of the spiral.

#	Met. type	Subs. type	L (nH)	R (μm)	N	W (μm)	S (μm)	Q	l (μm)	A (μm^2)	ff %
1	Al	HRS	5	150	4	12.2	3.01	16	713	8694	48.7
2	Al	LRS	5	150	3	12.03	3.98	13.2	753	9064	40.0
3	Cu	HRS	5	150	4	5	9.91	25.2	739	3695	43.1
4	Cu	LRS	5	150	4	5	10.34	22.4	734	3668	44.2
5	Al	HRS	5	200	4	23.12	3.02	18.8	855	19770	63.8
6	Al	LRS	5	200	3	15.64	4.13	14.2	1021	15963	37.5
7	Cu	HRS	5	200	3	6.79	10.74	28.3	1070	7262	29.7
8	Cu	LRS	5	200	3	5.18	14.11	24.4	1058	5481	31.5
9	Al	HRS	5	250	3	25.3	5.77	23.6	1198	30306	47.4
10	Al	LRS	5	250	3	17.36	21.07	13.5	1153	20024	53.1
11	Cu	HRS	5	250	3	12.97	19.13	32.1	1227	15913	43.7
12	Cu	LRS	5	250	3	6.42	31.27	24.4	1195	7671	47.8
13	Al	HRS	5	300	3	35.33	10.69	26.7	1340	47326	57.8
14	Al	LRS	5	300	2	17.46	3.01	14.4	1701	29693	26.3
15	Cu	HRS	5	300	3	21.4	26.12	33.3	1369	29300	54.7
16	Cu	LRS	5	300	3	6.74	52.6	23.2	1304	8788	61.6

Table 3.3: Design data for 10 nH inductors simulated with concentric ring model based inductor optimization program. L is the calculated inductance, r is the outer radius measured from the outermost wall of the spiral, N is the number of turns, W is the width of the spiral conductor, S is the spacing between each track, Q is the simulated quality factor at the optimization frequency of 0.8 GHz, l is the total length of the spiral, A is the area under the conducting tracks of the spiral, and ff is the fill factor, which is $100 * (1 - r_i/r)$, where r_i is the inner radius of the spiral.

#	Met. type	Subs. type	L (nH)	R (μm)	N	W (μm)	S (μm)	Q	l (μm)	A (μm^2)	ff %
17	Al	HRS	10	200	5	14.31	3.01	13.1	939	13439	50.5
18	Al	LRS	10	200	5	14.99	3.01	11.5	926	13886	52.5
19	Cu	HRS	10	200	5	6.11	11.21	26.1	965	5895	46.4
20	Cu	LRS	10	200	5	5.83	12.02	24	957	5582	47.5
21	Al	HRS	10	250	5	21.6	5.22	15.1	1081	23352	62.3
22	Al	LRS	10	250	4	18.59	3	12.3	1240	23060	42.0
23	Cu	HRS	10	250	4	8.51	11.55	28.6	1291	10989	35.5
24	Cu	LRS	10	250	4	7.56	13.75	25.6	1279	9666	37.1
25	Al	HRS	10	300	4	26.24	4.07	17.3	1421	37285	49.2
26	Al	LRS	10	300	4	23.45	10.86	12.4	1379	32348	53.6
27	Cu	HRS	10	300	4	13.61	17.78	32.2	1447	19694	46.4
28	Cu	LRS	10	300	4	10.04	24.34	26.4	1421	14263	49.2
29	Al	HRS	10	350	4	34.22	7.53	19.5	1566	53594	57.5
30	Al	LRS	10	350	3	25.53	3.02	13	1849	47202	31.8
31	Cu	HRS	10	350	3	13.21	11.12	31.9	1927	25460	24.6
32	Cu	LRS	10	350	3	10.32	17.8	26.9	1901	19615	27.1

A number of conclusions can be drawn from these (theoretical) optimization results. First of all, it should be noticed that the optimal width of the turns is a result of the tradeoff between metal loss (which decreases with increasing width) and substrate loss (which increases with increasing width due to the enhancement of the metal-substrate capacitance). The optimal LRS-based coils generally have narrower turns and a smaller overall footprint than the HRS ones. This is because substrate loss is dominant in LRS wafers and must be minimized by reducing the line width as much as possible. By contrast, on HRS substrates, where the metal loss is relatively more important, the optimal width shifts to higher values in order to minimize the metal loss.

Note also, that on the same substrate, optimal HAR inductors end up having narrower turns than Al-based devices. This can again be understood in terms of the tradeoff mentioned above. The tall, Cu-based HAR coils have such low metal losses that the optimum line width is almost entirely determined by substrate loss minimization, leading to very narrow lines. It should be mentioned at this point that the narrowing of the minimum metal width is limited, as the minimum width is set by technology limitations (5 μm for Cu-based HAR inductors and 3 μm for conventional Al coils in our routine). As we can observe in Table 3.2 and Table 3.3, several Cu inductors have minimum or close to minimum width, yet none of the Al inductors have such narrow widths.

Al and Cu inductors mentioned in Table 3.2 and Table 3.3 are fabricated according to design specifications. Al inductors are fabricated with an in-house standard metallization that employs sputtered Al deposition and reactive ion etching for patterning. Cu inductors are fabricated using the process described in Section 3.1. These processes are repeated on LRS and HRS wafers to obtain the inductors listed in both tables. Resulting devices are then measured as described in the next section.

3.3. Measurement and Performance Analysis

The inductor measurements were performed using an HP8510c vector network analyzer with a frequency range up to 20 GHz. The on-chip inductors were measured by directly contacting the contact pads on the wafer by means of planar probes with a ground-signal configuration with a pitch of 100 μm (GS 100). The measurements were performed from 0.05 GHz to 5.05 GHz at 201 points with 64 times averaging. The measurement setup was calibrated using a given calibration substrate with the thru-reflect-line method.

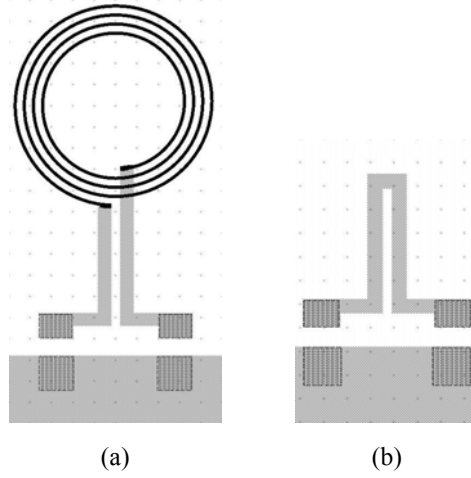


Figure 3.7: Layouts for the inductor (a) and the thru structure used for deembedding (b). Solid lines represent Cu structure and hashed areas represent Al layer. The boxes with different hash type are the contact areas for the probes.

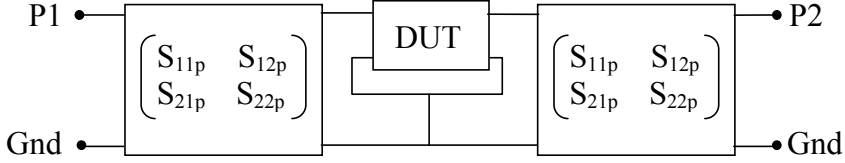


Figure 3.8: Schematic circuit of the measured spiral inductor with the deembedding structures depicted as 2 port networks and the resulting deembedded inductor as DUT.

The inductors were measured as a 2-port device, with the grounds connected to each other. The resulting 2-port scattering data (S-parameters) cannot be used directly due to the parasitic effects of the capacitance, resistance, and inductance of the connection pads. To extract the inherent parameters of the inductors, a 2-port de-embedding method [9] was employed where we used the calibration structure of Figure 3.7b. To carry out the de-embedding, the thru-structure of Figure 3.7b is viewed as the series (cascaded) connection of two two-port networks each representing one half of the structure (Figure 3.8). Since the two halves are symmetrical, the S-parameters of each halve (denoted by the subscript p) follow from the S-parameters of the overall structure according to [9]:

$$S_{11p} = S_{22p} = \frac{S_{11thru} + S_{22thru}}{2 + S_{21thru} + S_{12thru}} \quad (3.3)$$

$$S_{12p} = S_{21p} = \sqrt{0.5 * (S_{12thru} + S_{21thru}) (1 - S_{11p}^2)} \quad (3.4)$$

Here S_{11thru} , S_{22thru} , S_{12thru} , and S_{21thru} are the measured S-parameters of the thru. Next, the scattering matrix of each half is transformed into the transfer matrix or ABCD-matrix T_p . De-embedding is performed by

$$T_{DUT} = T_p^{-1} T_{meas} T_p^{-1} \quad (3.5)$$

where T_{meas} is the transfer matrix of the overall structure (inductor plus measurement pads) extracted from the raw measured S-parameters, and T_{DUT} denotes the transfer matrix of the coil alone. is Finally, T_{DUT} is transformed into admittance- or Y-paramaters Y_{DUT} , and the inductance L and quality factor Q are extracted with the following equations.

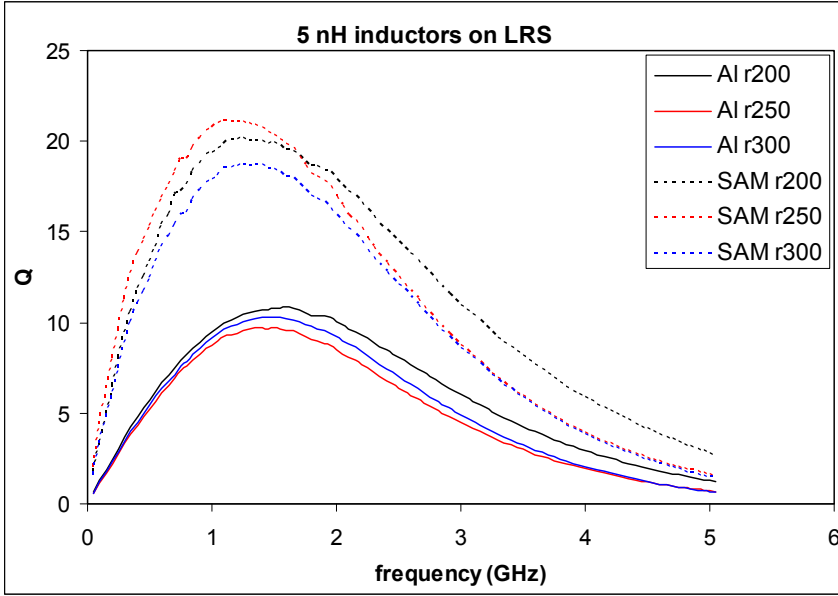
$$Z = \frac{1}{Y_{11}} \quad (3.6)$$

$$L = \frac{\text{Im}(Z)}{\omega} \quad (3.7)$$

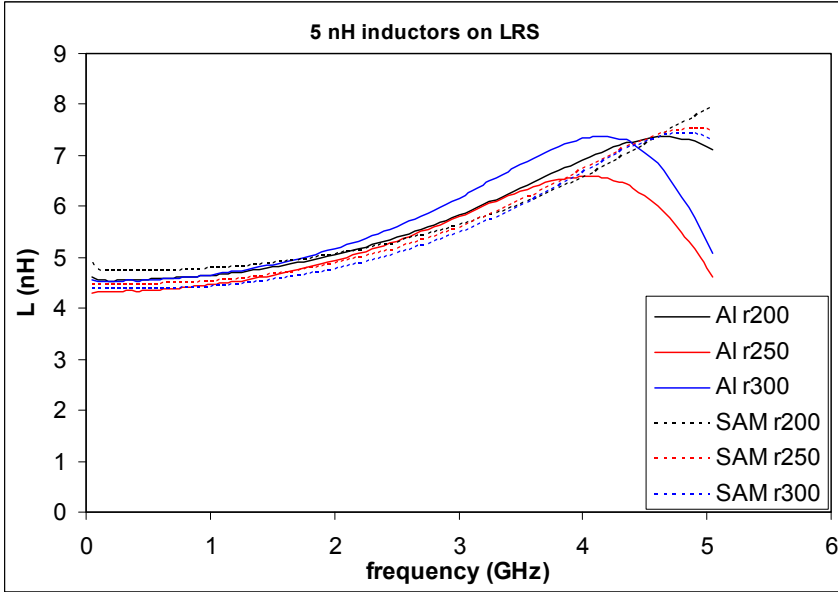
$$Q = \frac{\text{Im}(Z)}{\text{Re}(Z)} \quad (3.8)$$

It should be noted, that the above equations describe an inductor with its port 2 grounded. The measured impedance, and the resulting inductance and quality factor, are those viewed from port 1.

Measured and de-embedded values of the inductance (L) and quality factor (Q) are given in the following pages for several 5 nH and 10 nH inductors that are implemented on low resistivity (LRS) and high resistivity silicon (HRS) substrates.

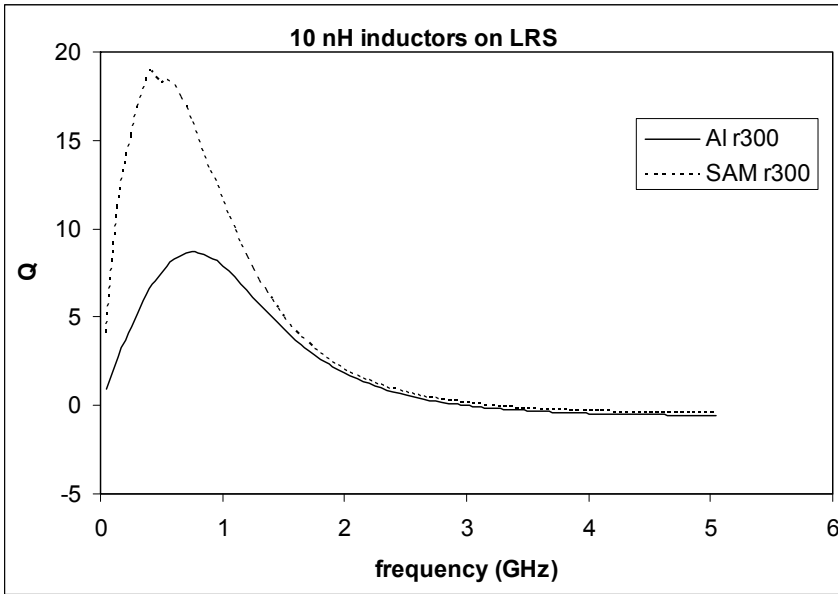


(a)

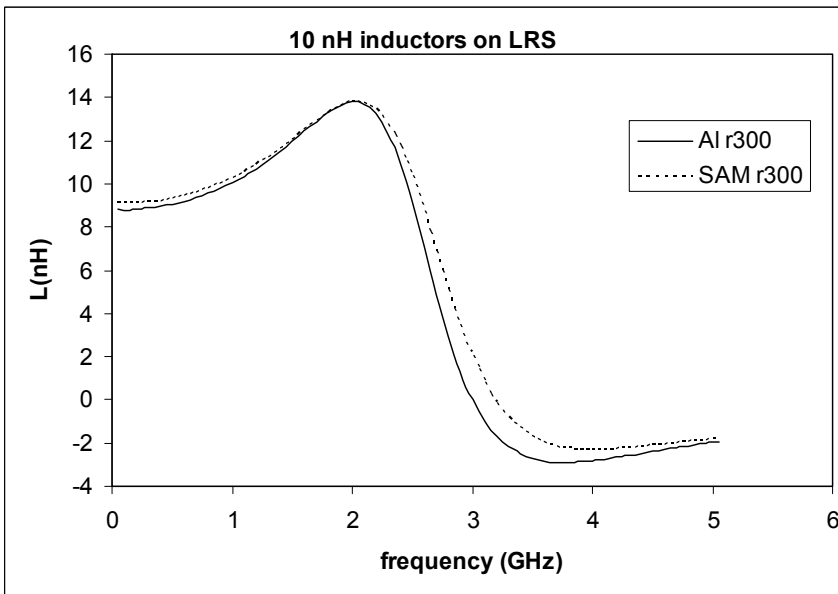


(b)

Figure 3.9: Quality factor (a) and inductance (b) values extracted from measurement results of 5 nH inductors fabricated on low resistivity silicon substrate. Solid lines are fabricated with Al (# 6, 10, 14 in Table 3.2) and dashed lines are fabricated with Cu (# 8, 12, 16 in Table 3.2).



(a)



(b)

Figure 3.10: Quality factor (a) and inductance (b) values extracted from measurement results of 10 nH inductors fabricated on low resistivity silicon substrate. Solid line is fabricated with Al (# 26 in Table 3.3) and dashed line is fabricated with Cu (# 28 in Table 3.3).

Figure 3.9 (a) for 5 nH inductors on an LRS substrate indicate a significant difference between the maximum achievable Q for the Al (# 6, 10, 14 in Table 3.2) and Cu (# 8, 12, 16 in Table 3.2) cases. Although the relative improvement due to HAR technology is not constant or does not follow a clear trend, on average a 95% increase in maximum Q value is observed for 5 nH inductors. The increase in Q is 117% for the 10 nH inductors on LRS as seen in Figure 3.10 (a). Since, at low frequencies, Q is mostly determined by metal loss (series resistance) the increase in Q in this region, as observed from Figure 3.9 and Figure 3.10, clearly indicates the significant reduction of the series resistance by HAR method.

Figure 3.9 (b) and Figure 3.10 (b) show L values for 5 and 10 nH inductors, respectively. Resonance is not observed for 5 nH inductors in the frequency range of measurement. However it can be seen that some of Al inductors are on the verge of resonance. Apparently, Al inductors have lower resonance frequencies than Cu inductors which is verified by the results for 10 nH inductors. This increase in the resonance frequency of Cu inductors can be associated with the smaller footprints achieved by this technology.

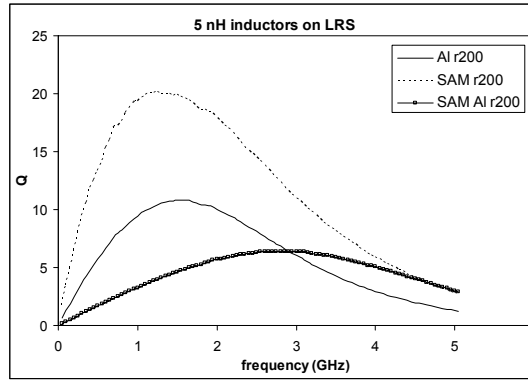
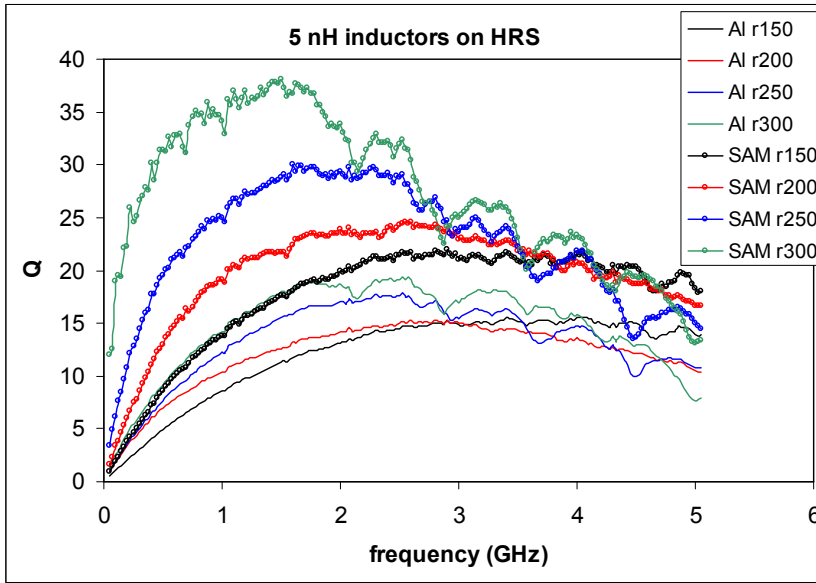
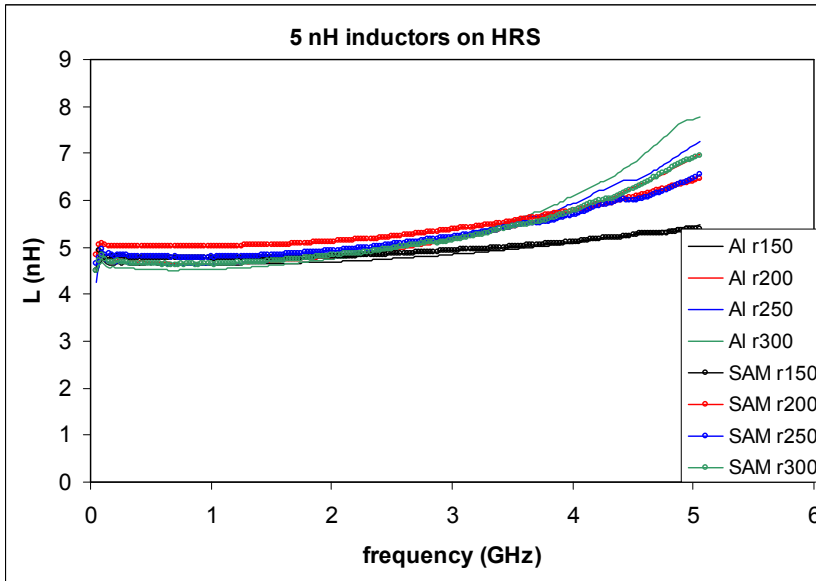


Figure 3.11: Comparison of quality factors of three 5 nH inductors fabricated on LRS substrate. Solid line is for an inductor that is optimized for Al process and is fabricated with Al process. Dashed line is for an inductor that is optimized for SAM HAR process and is fabricated with SAM HAR process. The line with (•) marker is for the same inductor that is optimized for SAM HAR process but is fabricated with Al process.

The performance improvements mentioned above are also a result of the optimization effort. As can be seen from Figure 3.11 the implementation of SAM HAR optimized inductor in Al technology results in a lower Q value than the optimized Al case. Using reverse analogy, it is possible to say that an inductor optimized for the Al technology would not introduce that much of a performance improvement, when implemented in SAM HAR technology. Separate optimization would be required to employ the full potential of the process.

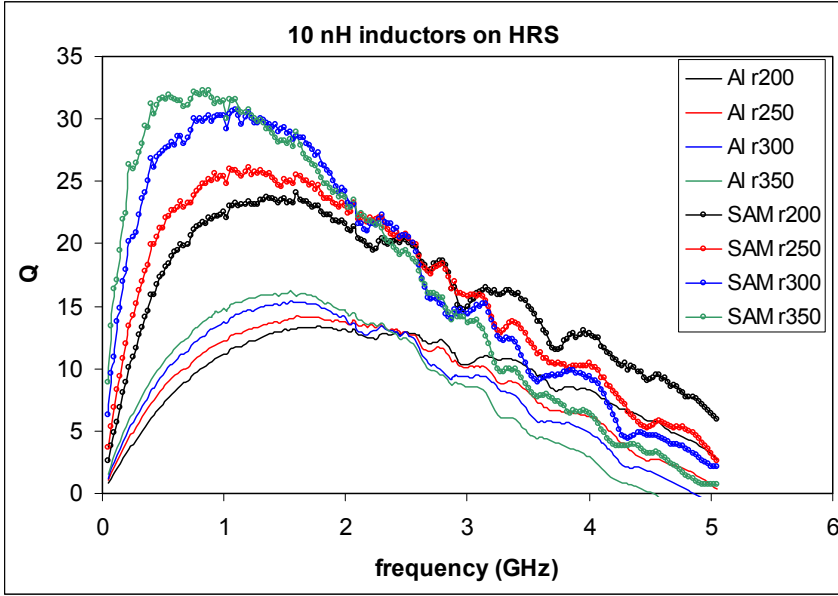


(a)

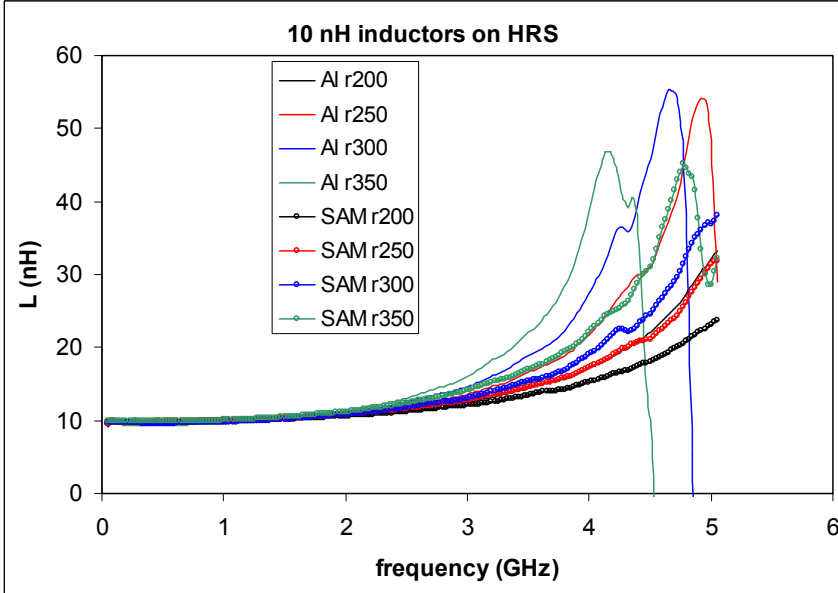


(b)

Figure 3.12: Quality factor (a) and inductance (b) values extracted from measurement results of 5 nH inductors fabricated on high resistivity silicon substrate. Solid lines are fabricated with Al (# 1, 5, 9, 13 in Table 3.2) and dashed lines are fabricated with Cu (# 3, 7, 11, 15 in Table 3.2).



(a)



(b)

Figure 3.13: Quality factor (a) and inductance (b) values extracted from measurement results of 10 nH inductors fabricated on high resistivity silicon substrate. Solid lines are fabricated with Al (# 17, 21, 25, 29 in Table 3.3) and dashed lines are fabricated with Cu (# 19, 23, 27, 31 in Table 3.3).

The performance improvement introduced by SAM HAR process on HRS wafers is apparent in Figure 3.12 (a) and Figure 3.13 (a). Q values show significant improvement compared to Al technology for both 5 nH and 10 nH inductors. The average increase in the maximum Q values for 5 nH and 10nH inductors is 65% and 90% respectively. It should be noted, that this improvement is more pronounced for inductors with larger radius. For instance, there is 40% improvement for 150 μm inductors and 95% improvement for 300 μm inductors. In terms of the frequency response similar characteristics can be observed in Figure 3.12 (b) and Figure 3.13 (b), when compared to LRS case. Al inductors have lower resonance frequencies compared to SAM inductors. The difference is more significant in 10 nH inductors compared to 5 nH inductors. When the performance improvement figures for maximum Q are compared with the LRS case, it is possible to observe that application of the HAR process to inductors on an LRS substrate is more effective than on an HRS substrate. It brings about 30% more improvement in maximum Q . Therefore processes based on LRS substrates would benefit the most from the SAM HAR add-on module.

In conclusion SAM HAR add-on process module improves the electrical performance of spiral inductors in terms of both the quality factor and the resonance frequency. The improvement can be attributed to availability of larger space for current flow in a better conductor for the non uniform current distribution, which would result in lower series resistance, reduction of the inductor footprint, and thus lower parasitic capacitances, and reduction of the fill factor, which would help reducing the eddy currents in the substrate. Moreover, the improvement in Q is more significant on low resistivity silicon than on high resistivity silicon substrates.

Besides having these advantages in terms of electrical performance, SAM HAR process could also help in another aspect of inductor design. This aspect is the thermal performance of the inductor. Thermal effects could play an important role in the inductor design especially for inductors that are suspended using micromachining technologies. Next chapter investigates this problem and presents insightful data in terms of self heating and thermal modeling of such inductors.

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Chapter 4

Thermal Issues in Suspended Inductors

4.1. Introduction

Inductors are key components in low-noise amplifiers, oscillators, filters, and impedance matching networks implemented in RF integrated circuits. Emphasis is on integration in Si technology, providing advantages in terms of reliability, cost, and integration density. The major drawback of Si-based inductors, however, is the high level of RF loss in the metal coil structure and in the conductive silicon substrate. These losses prevent, in general, from achieving high quality factors (Q) for spiral inductors on silicon.

In previous chapters we outlined how the use of thick metal can reduce conductor loss in integrated spiral inductors. Solutions to the substrate loss include the use of HRS [11]-[13], thick dielectric layers [14]-[17], proton bombardment of Si [18, 19], and oxidized deep trenches [20, 21]. Although effective, such methods involve major modification of the core device integration process, leading to process incompatibility and, thus, considerably higher cost. An alternative approach based on local removal of the Si substrate [22]-[24] has gained attention since it can be implemented by an add-on micromachining process, leaving the core integration process unaffected [25]. Moreover, the comparison of the process modification mentioned (Figure 4.1) shows, by far, the best results for Si micromachining in terms of the maximum Q obtained. However, while suspension of inductors by micromachining yields significantly higher Q 's in low power RF circuits [22]-[25], its application to high-power circuits like PAs is still an unexplored area. As the integration of PAs is considered a viable direction by industry [1], it is important to study the compatibility of suspended inductors with power circuit integration.

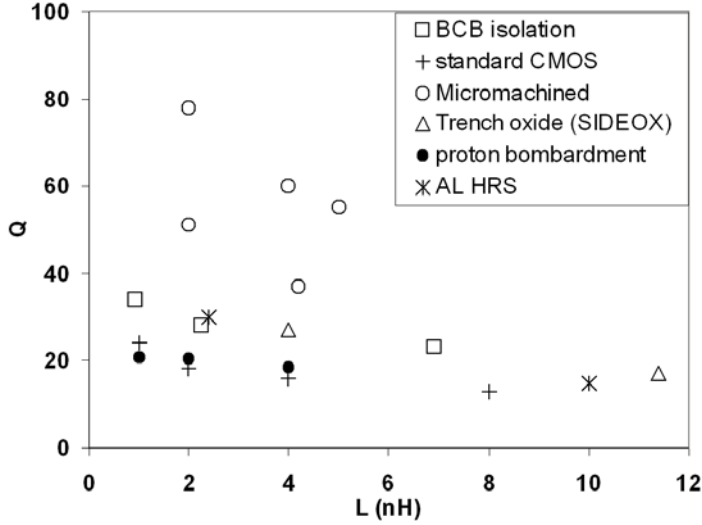


Figure 4.1: Inductance (L) and quality factor (Q) values for different technology options for the fabrication of integrated inductors. Data was taken from Refs. [11]-[28]. Hollow markers indicate the inductors that are prone to self heating.

The most serious problem faced by suspended inductors in PA applications is self-heating due to the flow of a high dc or RF current [2, 3]. The lack of an effective heat dissipation path, due to the removal of the Si beneath the coil, leads to elevated temperatures inside the current carrying coil. This, in turn, causes performance degradation and raises concerns about reliability [4]-[9]. The research presented in this chapter is dedicated to an experimental study, supported by modeling and simulations, of the self-heating of suspended spiral inductors under high-power conditions. We demonstrate that the average coil temperature may rise to several hundred degrees under the application of moderate to high currents (> 60 mA). In some cases, the local temperature of the coil can even be high enough to lead to melting of the metal lines, leading to device failure. We show that conduction through the coil's metal is the most effective heat dissipation path for a suspended inductor; although it does not prevent from self-heating if the metal lines have normal thickness. This is another argument in favor of the HAR process, presented in the previous chapter, which allows for fabrication of very thick metal tracks.

We shall also pay attention to the role of the underlying membrane and the surrounding free space. Simulation based on mapping the thermal problem onto a dc-conduction model will be employed to gain better understanding of the experimental data, as well as various heat dissipation mechanisms. Finally, we discuss possible solutions to achieve both a high Q and suppression of self-heating.

4.2. Self-Heating of Suspended Inductors

Under high-power conditions, the heat generated inside a conventional integrated spiral inductor is carried away through the underlying bulk Si, which has a high thermal conductivity (149 W/m-K at 300 K). The high thermal conductivity of Si makes it a very good heat sink, which is why self heating problems on bulk Si do not present a significant problem. In contrast, suspended inductors do not leverage from such a convenient heat sink underneath. A suspended inductor (Figure 4.2) has to suffice with alternate paths for the heat flow, such as through the metal of the spiral coil, the underlying dielectric membrane, and by conduction and convection through air. In comparison, heat dissipation through the conductor is expected to be dominant due to very high thermal conductivity of metal. For example Al and Cu have a thermal conductivity of 237 W/m-K, and 401 W/m-K at 300 K respectively. The internally generated heat will then flow through the coil outward to the leads that connect to the circuitry on the silicon substrate. The surrounding bulk silicon will thus act as a heat sink and set a reference ambient temperature.

Heat conduction through the dielectric membrane, in the case that such a membrane structure is used, is less significant since the thermal conductivity of commonly used materials (SiO_2 and Si_3N_4) is typically two orders of magnitude lower than that of metals. SiO_2 , for instance, has a thermal conductivity of 1.4 W/m-K at 300 K. Moreover, the membrane is usually thin (few micrometers). Nevertheless, the membrane's contribution to heat dissipation may not be fully negligible as the thermal path through the metal coil is much longer in comparison. The heat generated by the dissipation of power in the metal turns has to flow along the same turns to reach the inductor terminals which are on the bulk part of the Si substrate and, thus, in thermal equilibrium with the ambient (Figure 4.2). But, heat can flow through the membrane, spreading in all directions until reaching the thick Si region. For this reason, one should not underestimate the role of the membrane, despite its low thermal conductivity and small thickness.

Finally, heat can be dissipated through air, which, in spite of its very low thermal conductivity (0.025 W/m-K at 300 K), has to be considered since it offers conduction paths through the whole coil surface.

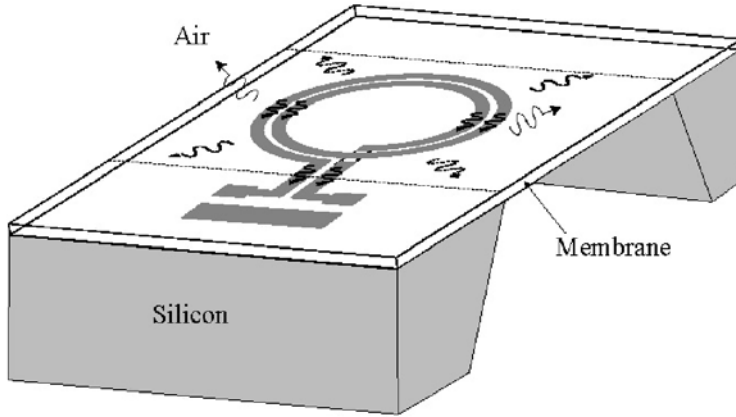


Figure 4.2: Graphical representation of heat dissipation paths for a suspended inductor.

4.3. Experiments

In terms of heat transfer efficiency, the paths outlined earlier can by no means substitute for the heat transfer through the bulk silicon, as for conventional integrated inductors. Consequently, suspended inductors operating under high-power conditions become prone to excessive self-heating effects, which degrade their performance and reliability. In order to gain more insight into this problem, we fabricated various suspended circular inductors with the geometrical parameters, i.e., number of turns (N), radius (r), linewidth (w), and spacing (s), listed in Table 4.1. The devices were built by using a Si micromachining post-process module added to an in-house standard active device process that has two aluminum (Al) metal layers with thicknesses of $0.8\text{ }\mu\text{m}$ at M1 and $3\text{ }\mu\text{m}$ at M2 levels. The M1 layer is used as the underpass for the inductors, and M2 is exploited for the spiral coil itself. There is a $0.8\text{-}\mu\text{m}$ -thick PECVD SiO_2 layer in between the M1 and M2 layers. The M1 layer rests on $3.2\text{-}\mu\text{m}$ SiO_2 , which results in $4\text{-}\mu\text{m}$ total membrane thickness for the spiral. Several inductors are placed onto a strip, with the entire strip of Si substrate being etched away by using deep reactive ion etching.

The high-frequency parameters (inductance and quality factor) of the coils were extracted from S-parameter data obtained with an HP 8510 network analyzer equipped with bias-T's to supply the dc bias current. The setup is calibrated as explained in Chapter 3. The high-power conditions were emulated by subjecting the inductors to a constant dc bias current between 0 and 100 mA while measuring their resistance using a voltmeter. The resulting dc power applied to the devices was considered as the self-heating power emulating the case of an inductor that has only high RF power passing through. Note that, although in the RF case current

distribution—and, thus, heat generation—in the cross section of the coil is nonuniform due to skin depth and proximity effects, the high thermal conductivity of metal makes the heat distribution in the cross section uniform, hence making it well comparable to the dc case. Since there is no added value in experimenting with RF load currents, we limited ourselves to the dc case, which is much easier to handle.

To estimate the average temperature of the suspended coils under the application of the different bias currents (I_{dc}), we measured the increase in the overall dc resistance (R_{dc}) of the device prior to the RF measurement. This was achieved by simply measuring the dc voltage between the coil terminals under application of I_{dc} . The resistivity ρ of the coil metal at any point is linearly related to the local temperature T , i.e.,

$$\rho(T) - \rho(T_0) = \alpha \rho(T_0)(T - T_0) \quad (4.1)$$

where T_0 is the room temperature, and α is the temperature coefficient of resistance of the metal ($\alpha = 0.0043$ $1/^\circ\text{C}$ for Aluminum and 0.00393 $1/^\circ\text{C}$ for Copper). For a coil with the length l and cross sectional area S , the overall resistance is thus given by

$$R_{dc} = \frac{1}{S} \int_0^l \rho(T) dx \quad (4.2)$$

where x denotes the position along the coil (the length of the wire segment between a point on the coil and one of its terminals). From the above equations it then follows that

$$T_{av}(I_{dc}) = T_0 + \frac{1}{\alpha} \left[\frac{R_{dc}(I_{dc})}{R_{dc}(0)} - 1 \right] \quad (4.3)$$

Therefore, measured R_{dc} values give a means to indirectly calculate the average temperature increase under bias.

The measurement and calculation results for several inductor geometries are given in Table 4.1 which show a dramatic increase in the average temperature (up to several hundred degrees) for some of the inductors under bias currents higher than 60 mA. One should bear in mind, however, that inductors with a different series resistance do not dissipate the same amount of power ($P = R_{dc} I_{dc}^2$) for equal bias currents. A more appropriate figure of merit for comparison of the thermal behavior of inductors is, therefore, the increase in average temperature per unit of dissipated power (ζ). The corresponding data are shown as the last column in Table 4.1.

Table 4.1: Inductance (L), number of turns (N), line width (w), spacing (s), radius (r), and total metal length (l) of suspended circular spiral inductors used in the experiments. For each coil the increase in average temperature with respect to the room temperature (ΔT_{av}) was measured as function of an applied DC bias current. The last column presents the calculated temperature increase per unit dissipated power.

#	L (nH)	Dimensions (μm)					ΔT_{av} ($^{\circ}\text{C}$) for different bias currents					ζ ($^{\circ}\text{C}/\text{mW}$)
		N	w	s	r	l	20 mA	40 mA	60 mA	80 mA	100 mA	
1	1	2	6	3	80	854.1	5.6	22.9	57.5	121.4	256.7	6.392
2	1	2	6.8	13.8	100	955.3	6.5	25.8	60.4	122.3	244.9	7.2
3	1	2	11.8	3.3	100	992.2	1.9	8.8	21.5	38.2	65.5	5.115
4	1	2	16.4	7.6	120	1102.5	1.8	6.8	19.4	33.0	51.9	5.32
5	1	2	6.5	28.9	120	1021.1	5.1	25.4	66.5	147.7	346.6	6.838
6	1	2	14.2	35.8	150	1167.1	4.2	8.1	22.3	42.1	73.1	5.56
7	1	2	23.8	14.9	150	1249	2.1	3.9	14.6	24.7	39.0	4.95
8	5	4	23.1	3	200	3421	2.8	10.9	28.5	55.2	98.3	4.038
9	5	3	25.3	5.8	250	3593.6	5.9	10.0	27.4	51.7	89.5	3.98
10	5	3	35.3	10.7	300	4019.5	1.0	11.0	21.3	38.9	63.2	3.65
11	5	3	15.6	4.1	200	3062	4.9	20.2	46.0	88.9	162.3	4.556
12	5	3	17.4	21.1	250	3460.4	4.7	20.2	49.3	98.5	182.5	4.759
13	10	5	15.00	3	200	4631.7	5.5	28.7	77.8	175.4	464.6	4.446
14	10	4	18.6	3	250	4961.8	4.1	20.1	51.6	106.5	206.0	3.785
15	10	5	21.6	5.2	250	5407.1	5.6	22.2	53.8	109.9	210.4	4.16
16	10	4	23.5	10.9	300	5517.7	4.7	21.2	49.5	100.3	187.1	4.078
17	10	4	26.4	4.1	300	5672.1	3.3	16.3	41.0	80.8	146.1	3.818
18	10	4	34.2	7.5	350	6267.4	2.8	11.9	30.2	58.9	102.5	3.38

The rise in inductor temperature as a result of applied bias is governed by the tradeoff between local heating by the dissipation of electric power and the transfer of the heat to the ambient environment. Given the expected dominance of heat transfer through the metal coil, one would expect ζ to be mainly a function of its thermal resistance. The latter is proportional to l/w . Close inspection of the results, however, reveals no clear correlation between ζ and l/w values. Instead, a correlation was found between ζ and $2\pi r_{av}/Nw$, where r_{av} is the average radius of the coil (Figure 4.3). Apparently, the different turns of the coil behave thermally as a single turn with the length $2\pi r_{av}$ and the width Nw . This implies that the turns are in local thermal equilibrium, so that neighboring points on different turns are essentially at the same temperature.

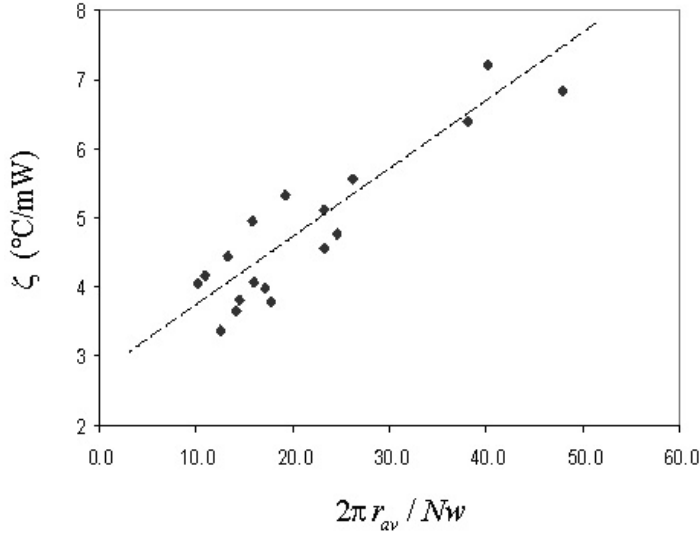
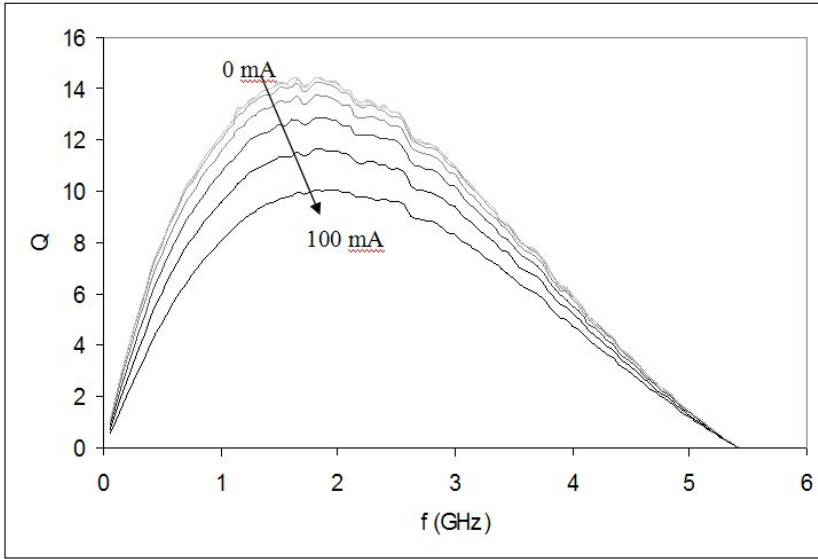


Figure 4.3: Average temperature increase per dissipated power (ζ) versus the ratio between the average circumference of the coil ($2\pi r_{av}$) and the total metal width (Nw). r_{av} equals to the average of the outer and inner radii of the coil. The correlation observed indicates that, from a thermal perspective, a suspended coil behaves as a single-turn inductor with the length $2\pi r_{av}$ and the width Nw .

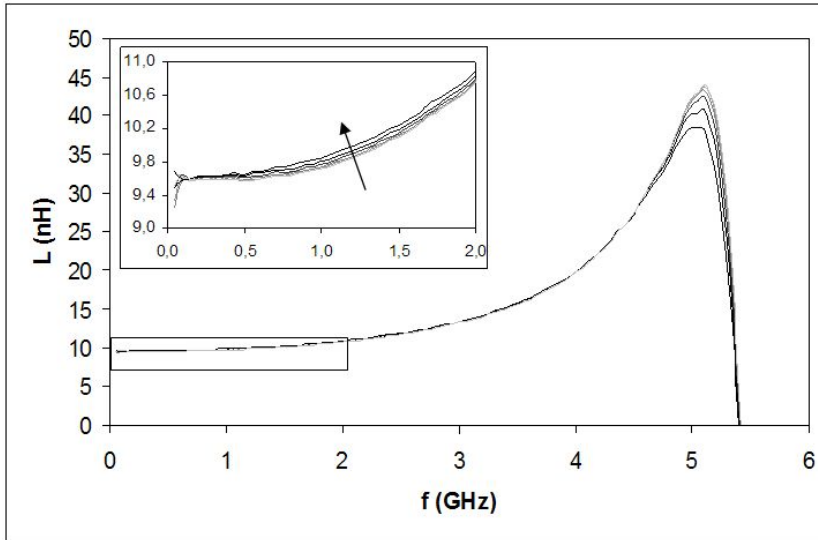
To understand this phenomenon, we should recall that the spacing (s) between the turns of the coil is small compared to their circumference. Despite its low thermal conductivity, the membrane can then act as an efficient lateral heat path locally shunting the neighboring turns. Hence, although heat transfer still takes place mainly through the metal, the inductor thermally behaves as a single-turn coil with an effective width given by the total width of the turns. These observations will be numerically verified in Section 4.5.

4.4. Detrimental Effects of Self-Heating

The self-heating of suspended coils degrades their RF performance by lowering their quality factor (Q) [2, 3]. Figure 4.4 shows the Q of a suspended inductor as a function of frequency for different bias currents. Up to 30% reduction of the maximum Q value can be observed. This can be attributed to temperature-induced increase of the series resistance of the coil.



(a)



(b)

Figure 4.4: (a) Quality factor (Q) (b) inductance (L) of a 10-nH suspended spiral inductor (coil #15 in Table 4.1) as function of frequency for different bias currents.

A related aspect of self heating is the transient response of the system to input power. The time constant for the temperature to reach the steady state situation is important for circuits that operate in the pulsed mode as a change in temperature is reflected in the quality factor of the inductor. If this time constant is comparable to the

duty cycle of the circuit then the operating point of the circuit would shift during operation, which is an unwanted phenomenon for circuit design. It should be noted that the effect of this transient behavior depends on the final temperature difference, which would be crucial in determining the change in series resistance, hence quality factor. The thermal time constant of an inductor is measured by monitoring the inductor voltage after switching on a dc current. This can be achieved by means of an oscilloscope using the step function current as a trigger input. The thermal time constant of the device can then be estimated from the resulting resistance curve (given in Figure 4.5 for inductor #9) by using equation 4.3. The measurement result is in agreement with a finite element based temperature simulation done by Ansoft's ePhysics software. An exponential curve fitting to the measurement data gives a time constant of 10.9 ms for the device tested. This time interval is similar to the duty cycle of switched power amplifiers for most applications hence shifting of the operation point can be an important issue to consider for designers.

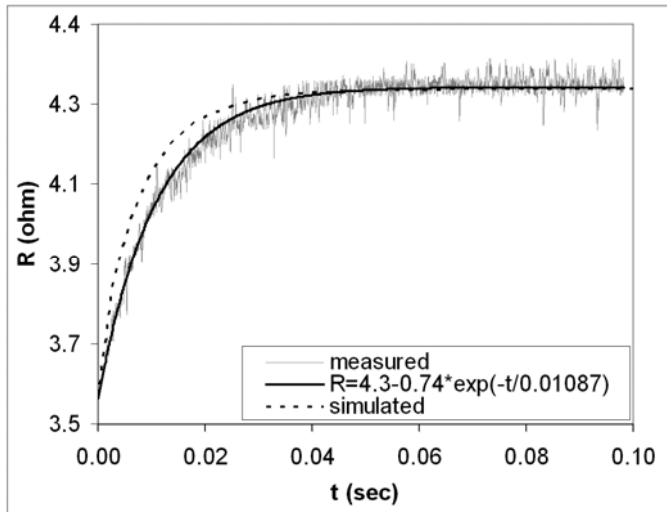


Figure 4.5: Transient measurement and simulation of the DC resistance. Also a curve fitting to the measurement is shown.

A more crucial problem, however, involves the reliability issue caused by excessive heating. While the values given in Table 4.1 represent average coil temperatures, the local temperature of the metal may rise up to much higher values. This may result in device failure due to local breakdown of the coil metal by electromigration effects, stress-induced cracks, or even melting. To experimentally study these effects, we monitored the dc resistance of inductors as the dc bias current was increased from 0 to 100 mA in steps of 20 mA. The current was then reduced back to 0 mA in order to verify if a permanent damage occurred to the coils after the current cycle. During the measurement, it was observed under a microscope that some of the inductors (listed in Table 4.2) were burned, resulting in a flash of light. Later,

those inductors were examined by using a scanning electron micrograph (SEM). One sample SEM is shown in Figure 4.6, where it is possible to observe small dots adjacent to the metal coil tracks. These little spheres were indeed molten Al, later solidified, which takes spherical form due to surface tension. This observation suggests the fact that Al tracks melt during breakdown due to excessive temperature.

Table 4.2: Geometrical parameters of the suspended inductors which failed during the experiments, together with the increase in their average temperature prior to the failure. The last column shows the computed (see next section) maximum temperature inside the coil metal at the breakdown bias current. Since the current was increased in steps of 20mA, the reported values of the breakdown current overestimate the actual ones. As a result, the computed maximum temperatures overestimate the true values.

Coil nr.		Dimensions (μm)			ΔT _{av} (°C) for different bias currents (mA)					Peak ΔT (°C)
		<i>N</i>	<i>w</i>	<i>s</i>	<i>r</i>	20	40	60	80	
19	4	10.04	24.34	300	15	71	205	x	x	782
20	3	10.32	17.8	350	15	71	205	x	x	782
21	3	5.18	14.11	200	27	156	x	x	x	811
22	3	13.21	11.12	350	3	32	91	198	x	597
23	4	13.61	17.78	300	11	46	124	301	x	1072
24	3	6.79	10.74	200	14	77	253	x	x	1070

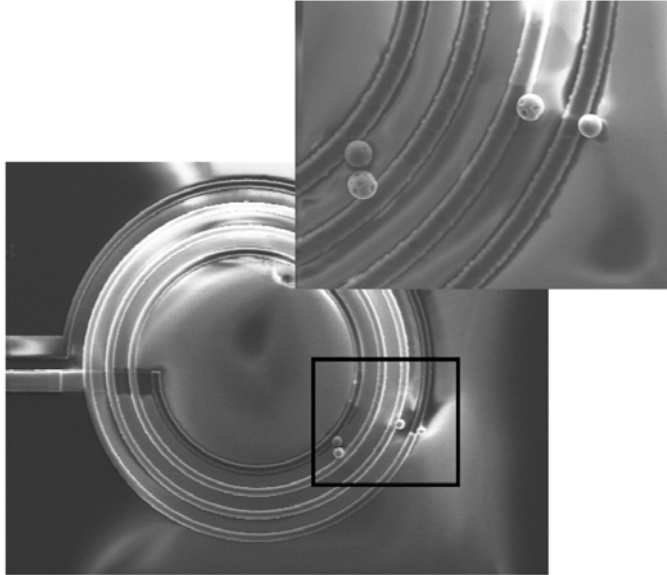


Figure 4.6: SEM image of a spiral inductor that has failed due to excessive self heating. Little spheres are molten aluminum metal of the spiral tracks that later solidifies. It is also possible to observe the voids in the metal tracks in the zoomed picture.

Figure 4.6 clearly shows that metal damage simultaneously occurs on several points far away from the coil terminals (although, most likely, complete breakdown occurs at only one of those points, cutting the current path). Evidently, since the coil interconnects partially lie on the silicon substrate (acting as a heat sink at ambient temperature), high temperatures can only develop at sufficient distance from those points. Furthermore, note that although the damaged points lie on different turns, they are closely neighbored. This indirectly verifies our previously made hypothesis that adjacent points on different turns essentially have the same temperature.

To gain more insight into the mechanism of device failure we carried out simulations (see next section) to compute the maximum local temperature inside the coil metal at the breakdown bias (Table 4.2). Although the values obtained overestimate the actual ones (see the caption of Table 4.2), they indicate that the local temperature inside the coils can easily rise to the melting point of Al (660 °C). This result explains the molten Al particle observed under the microscope. However, one should bear in mind that electromigration effects and stress-induced cracks in the metal due to warpage of the membrane can potentially accelerate the melting process. In particular, the stress- induced cracks can locally narrow down the current carrying wires, leading to increased local resistance and, therefore, heat generation. However, those effects could not be verified by our experiments.

4.5. Simulation and Modeling

The measurement results given in the previous section provide useful information in understanding the effects of self heating. Nevertheless, it is not possible to obtain the temperature distribution over the geometry of an inductor from the measurement of the average temperature data. This information would be useful in understanding the effectiveness of different heat dissipation mechanisms, and the effects of geometrical variations on self heating. It is possible to obtain such data by measuring temperature distribution over the structure by means of an infrared thermography system such as an infrared camera. However such a system was not available in the duration of research, hence alternatives had to be employed for obtaining such data.

For that reason we attempt to gain insight in the temperature distribution of a suspended inductor with a given input power using thermal simulation software. 3D thermal simulation using finite element model would lead to a 3D temperature distribution figure like the one given in Figure 4.7. The simulation result given in Figure 4.7 is for inductor #9, which has a measured T_{av} of 89 °C. The simulation result shows that more than half of the spiral is above 94 °C, and the adjacent segments of the spiral have similar temperature values. This supports the correlation given in

Figure 4.3, which means that the membrane acts as a means to thermally shunt the windings of the spiral.

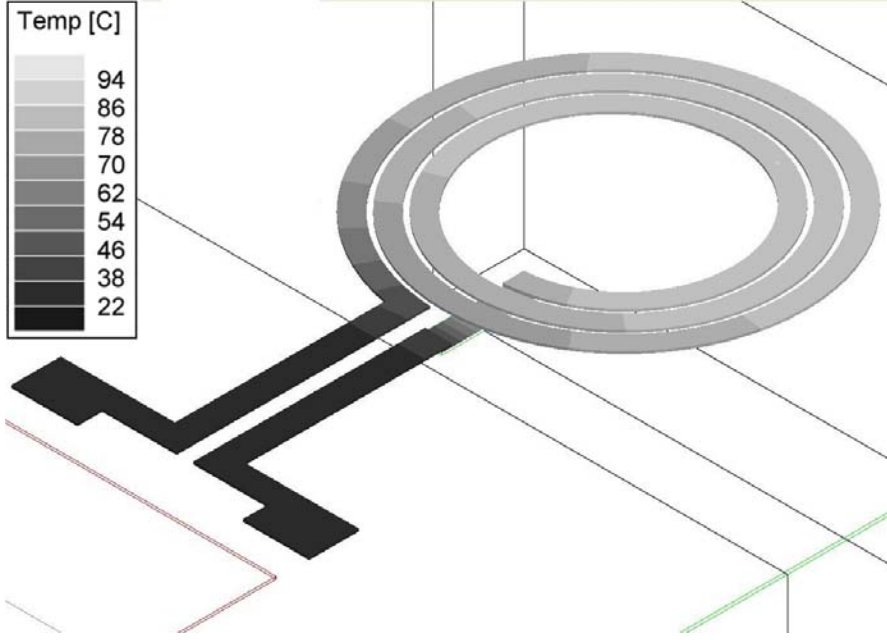


Figure 4.7: Temperature distribution of a suspended spiral inductor simulated with Ansoft's ePhysics software.

Although 3D thermal simulation based on finite element method would give the most accurate results, it would take too much time and computer resource to simulate these structures. An alternative solution would be beneficial especially for optimization problems. In order to achieve such a goal the similarity between the thermal- and electrical conduction problems may be exploited. Note, that the transfer of heat inside any medium is governed by the Fourier's law of conduction

$$\mathbf{q}(\mathbf{r}) = -k\nabla T(\mathbf{r}) \quad (4.4)$$

Here $\mathbf{q}$ is the heat flux density vector, $\mathbf{r}=(x,y,z)$, k is the thermal conductivity of the medium, $\nabla=(\partial_x, \partial_y, \partial_z)$, and T is the local temperature. For a time-independent problem the above equation is supplemented by the energy conservation equation:

$$\nabla \cdot \mathbf{q}(\mathbf{r}) = p(\mathbf{r}) \quad (4.5)$$

where p denotes the time rate of heat generation per unit volume. Compare these equations with those in an electrical dc conduction problem. There we have the Ohm's law $\mathbf{J}(\mathbf{r}) = -\sigma \nabla V(\mathbf{r})$ where $\mathbf{J}$ denotes the current density vector, σ is the

electric conductivity of the medium, and V is the electric potential. Besides, the conservation of electric charge (in the time-independent case) demands that $\nabla \cdot J(\mathbf{r}) = g(\mathbf{r})$ where g is the rate of heat generation per unit volume. Moreover, the boundary conditions at the interfaces separating different substances are also identical (continuity of temperature or potential, and continuity of the normal component of the current density vectors).

Hence, instead of solving the heat conduction problem, we can solve the dc conduction problem using the available electromagnetic software by interpreting the temperature as an electric potential and replacing k by σ . We just have to choose the coefficients correctly. But there is a catch here. In the actual heat-conduction problem the local generation of heat takes place due to local dissipation of electric power caused by the flow of the bias current I_{dc} . However, most electromagnetic simulation tools do not have facilities for including local charge generation $g(\mathbf{r})$ which is supposed to emulate $p(\mathbf{r})$.

To circumvent this problem, we divide the coil into a number of small segments along its length. The local generation of heat can then be approximately modeled by calculating the total heat generated inside each division

$$\Delta Q = \int_{\Delta V} p(\mathbf{r}) dV = I_{dc}^2 \Delta R \quad (4.6)$$

where ΔV and ΔR denote the volume and electric resistance, respectively, of a segment. In the dc-conduction language, this quantity is the rate of total charge generated inside the segment. To take account of charge generation we next assign a separate terminal (port) to each segment attached to a current source delivering a current equivalent to ΔQ as seen in Figure 4.8.

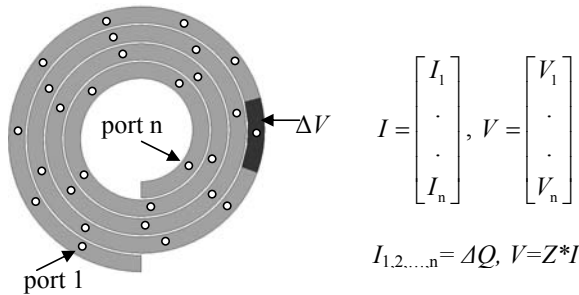


Figure 4.8: I_n values are input at each port point and the simulation results give the Z matrix and V matrix hence the potentials at port points. These potentials represent the average temperature for the given section.

Using this method in combination with Agilent's software tool ADS, we simulated the temperature distribution inside the suspended coils. While we could not

experimentally verify the local temperatures, good agreement (7%–15% error) was found between the calculated and measured average coil temperatures. Figure 4.9 shows these values for a 5-nH inductor (coil #11 in Table 4.1) as a function of the applied bias. The calculated temperature (T) distribution along the same coil is shown in Figure 4.10 (solid line) for a bias current of 100 mA. The start and end points of the curve correspond to the coil terminals that are at ambient (room) temperature. Notice the nearly periodic dependence of T on the location within the coil. This clearly suggests local thermal equilibrium between the windings. If simulations are performed for the metal alone, no periodic dependence is observed [see Figure 4.10]. Instead, the temperature along the coil exhibits the usual parabolic behavior in a metal wire and reaches extremely high values at the center of the coil above (2500 °C). Hence, the membrane is crucial for preventing excessive local self-heating not necessarily because of its ability to conduct the heat away from the coil but to thermally shunt the windings, thus decreasing the effective length and increasing the effective width of the metal with respect to thermal conduction. Interestingly, the surrounding air can also contribute to this effect. Simulations performed without the membrane but including conduction through air show a considerable lowering of the coil temperature with respect to those obtained for the metallic coil alone [Figure 4.10]. They also show a slight periodicity similar to the effect of the membrane.

Finally, in Table 4.3, we have summarized the percentage of heat dissipation through different routes available to a suspended inductor. For typical coils built on a 4- μm -thick silicon dioxide membrane, about 60%–80% of the heat is carried away through the metal, 12%–20% is dissipated through the membrane, and 7%–15% is conducted through the air.

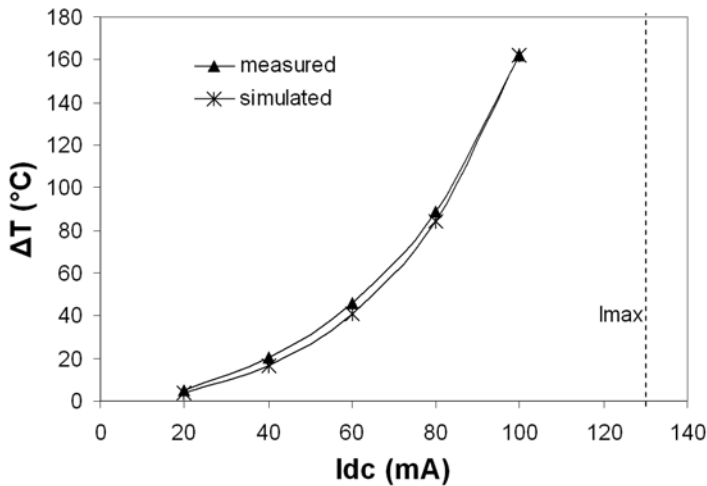


Figure 4.9: Simulated vs. measured average temperature of a 3-turn suspended inductor (coil #11 in Table 4.1) as function of the applied bias current. I_{max} line indicates the maximum applicable current before destruction of the coil.

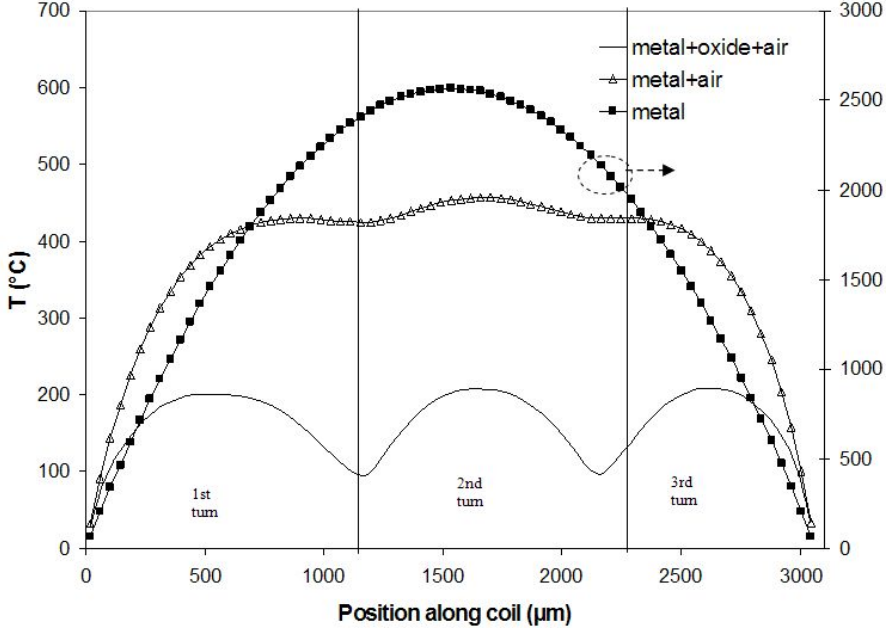


Figure 4.10: Simulation results for temperature as function of position along the same coil for an applied bias of 100 mA (solid line). The line marked with squares shows the results obtained for the metal alone. The line marked with triangles shows the results obtained in presence of air, but without the membrane.

Table 4.3: Heat dissipation percentages for a number of suspended inductors. Metal denotes the dissipation through the metal tracks, oxide is for heat dissipation through the 4 μm thick silicon dioxide membrane, and air is for the conduction through air.

Coil #	Metal (%)	Oxide (%)	Air (%)
1	76.9	14.9	8.2
2	80.3	12.6	7.1
8	74.5	15.5	10
11	63.6	22.5	13.9
13	72.8	13	14.2

4.6. Thermal Management of Suspended Coils

The results presented in the previous section show that the most effective way to prevent excessive heating of suspended coils in power applications is to increase the efficiency of heat transfer through the coil metal itself. This can be achieved by increasing the width of the metal turns. Yet, this solution is not always in support of RF performance, as it increases the parasitic interwinding capacitance for a given

metal pitch, leading to a reduction of the self-resonance frequency of the device [10]. Instead, increasing the metal thickness and/or using metals with a high thermal (and thus electrical) conductivity such as copper (Cu) is more favorable. To study this effect, we built suspended inductors from 13- μm -thick electroplated Cu using the HAR process described in Chapter 3. Figure 4.11 shows the comparison of suspended Al- and Cu-based inductors in terms of temperature increase as a function of applied current. The Cu-based coil apparently leads to a far more effective heat removal than its Al-based counterpart. Moreover, for a given current, the amount of electric power dissipated in the Cu-based inductor is less due to its smaller series resistance. Overall, the result is an almost tenfold reduction of average temperature.

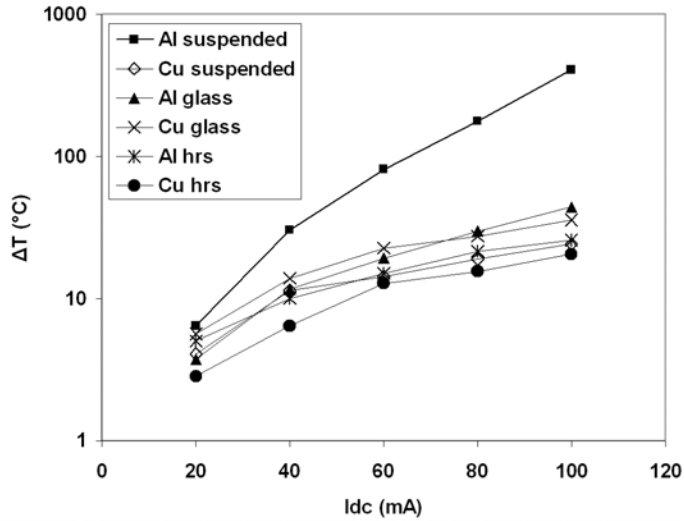


Figure 4.11: Increase in average temperature as function of the applied current for a 5 nH inductor (coil #9 in Table 4.1) fabricated using different technologies. All Al inductors have a thickness of 3 μm and all Cu inductors have a thickness of 13 μm . The suspended Cu-based coil shows a tenfold reduction of average temperature compared to the suspended, Al-based device. The same coil built on a HRS substrate shows almost no self heating effect.

In power applications, where thick highly conductive metal layers are not readily available, one should consider increasing the heat transfer efficiency of the nonmetallic thermal paths described earlier. Possible solutions are to increase the membrane thickness (to several tens of micrometers) or to cover the coil by a thermally conductive, but electrically insulating layer such as the encapsulating plastic packaging (heat shunt). The first option, however, is not technologically viable due to the excessive stress build up in the substrate. The second solution, on the other hand, adds to the complexity of the fabrication process. Moreover, the electrical properties (e.g., dielectric constant and loss) of such a heat shunt affect the device performance and should thus be applied with caution. The best alternative in this case,

in fact, is to use nonsuspended coils. In order to provide a coil structure that features both a high Q and a high thermal conductivity to the substrate, one should consider fabricating coils on substrates with low RF loss yet good thermal conductivity, such as HRS [11]-[13]. The comparison of experimental data obtained (see Figure 4.11) shows that HRS-based inductors suffer the least from self-heating effects. Evidently, the effectiveness of an HRS substrate as a heat conductor cannot be matched even by very thick Cu coils.

4.7. Conclusion

In this chapter we presented a study of self heating of suspended spiral inductors under high-power operating conditions. Experimental data obtained from typical spiral inductors show that the average device temperature may rise to several hundred degrees for moderate to high DC (or RF) currents (above 60 mA) applied. This leads to a degradation of the RF performance of the coils (lower quality factor) and, in some cases, even to the catastrophic failure of the device.

The excessive self heating of suspended inductors is caused by the limited efficiency of the thermal dissipation paths available. Among those paths, heat conduction through the coil metal is the most effective. Nevertheless, the underlying membrane and the surrounding air are crucial for preventing extreme self heating not necessarily because of their efficiency in dissipating the heat, but since they thermally shunt the metallic windings. This hypothesis was supported by simulations based on mapping the thermal problem onto a dc-conduction problem. The results were in good agreement with experiments.

A remedy to the self heating of suspended coil is offered by deploying thick, highly conductive metals. Experimental data obtained from coils built from 13 μm -thick electroplated Cu lines prove the absence of excessive heating even for very high values of dc supply currents. In the absence of a thick metal, the best alternative is to resort to conventional coils built on a low-loss, but thermally conductive substrate such as high resistivity Si.

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Chapter 5

High Aspect Ratio Transmission Lines

5.1. Introduction

With the advent of planar, integrated microwave circuits, transmission lines have become an important part of the microwave device spectrum. Despite what their name might suggest, the application of these elements goes far beyond the mere transfer of microwave power. Transmission lines are the building blocks of a large number of microwave passive components and networks such as impedance matching circuits, couplers, filters, and power dividers.

The primary quantities that determine the electric behavior of a transmission line are the complex propagation constant $\gamma = \alpha + j\beta$ and the characteristic impedance Z_c . Here $\beta = 2\pi/\lambda$ is the propagation constant where λ is the propagation wavelength of the primary (often quasi-TEM) mode guided along the structure. The attenuation constant α is a measure of per-unit-length power loss as the signal propagates along the line. Instead of β , it is customary to use the effective dielectric constant $\epsilon_{eff} = (\lambda_0/\lambda)^2$ where λ_0 is the wavelength of an electromagnetic wave propagating in vacuum at the same frequency.

Transmission lines are commonly analyzed by employing distributed element models where the line is represented as the cascaded connection of (infinitely) many small segments each modeled by a lumped-element network. One such model is shown in Figure 5.1 where L_0 , C_0 , R_0 and G_0 denote the inductance, capacitance, series resistance and shunt conductance of the line per unit length, respectively. In terms of these quantities, the complex propagation constant and characteristic impedance of a transmission line are expressed as

$$\gamma = \sqrt{(R_0 + j\omega L_0)(G_0 + j\omega C_0)} \quad (5.1)$$

$$Z_c = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}} \quad (5.2)$$

If the conductor loss (represented by R_0) and substrate loss (accounted for by G_0) are small, then the first order Taylor expansion of these expressions yields

$$\beta = \omega \sqrt{L_0 C_0} \quad (5.3)$$

$$\alpha = \frac{G_0 Z_0}{2} + \frac{R_0}{2Z_0} \quad (5.4)$$

$$Z_c = Z_0 + \frac{jZ_0}{\beta} \left(\frac{G_0 Z_0}{2} - \frac{R_0}{2Z_0} \right) \quad (5.5)$$

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \quad (5.6)$$

Despite their popularity in traditional hybrid microwave circuits, the application of transmission lines in RFIC has been rather limited. Like in case of integrated inductors, on-chip transmission lines are relatively bulky. Application in microwave devices often requires the line to be a well-defined fraction (like 1/2 or 1/4) of the propagation wavelength. The latter, however, can be very large at low GHz frequency. On Silicon, for instance, λ will be no less than ~ 3 cm at 3GHz, regardless of the transmission line type used. A half- or even quarter-wavelength component would then have a length comparable to or larger than the size of a modern RFIC. For that reason the application of on-chip transmission line components is mostly restricted to frequencies above 30 GHz [1].

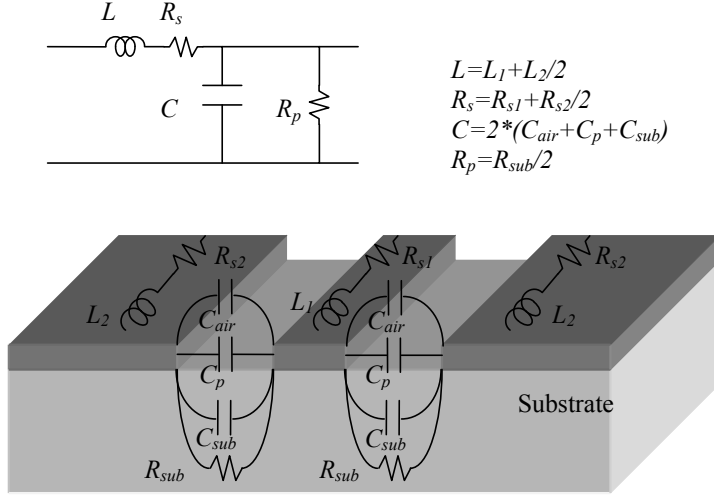


Figure 5.1: Circuit model for a unit length low loss transmission line. L is the series inductance, R_s is the series resistance, which is attributed to conductor loss, C is the parallel capacitance, and R_p is the parallel resistance, which is related to substrate loss. All parameters are defined as per unit length values. Inductance and capacitance values are related to magnetic and electric energy storage capabilities of the transmission line.

The second major bottleneck in on-chip implementation of transmission lines is their high loss, which is reflected in a relatively large attenuation constant. This is due to effects similar to the ones in spiral inductors: substrate loss and limited width of metals in IC processes cause the line attenuation to increase significantly [2]. As in integrated inductors, substrate loss in transmission lines can be reduced by using low-loss substrates such as high resistivity silicon, glass, or GaAs. These passive substrates can be later combined with the active substrate (usually low resistivity silicon) by wafer bonding and packaging techniques [3, 4]. An alternative is the local removal of the lossy substrate to obtain suspended transmission lines [5, 6]. These lines would have lower loss and lower dispersion, but they would be longer due to low effective permittivity which leads to a longer propagation wavelength. (For a more detailed discussion of these and other techniques please see chapter 2).

The common solution of circuit designers to reduce the conductor loss is to widen the conductors comprising the line in order to increase the cross section that will carry the current, hence reduce R_s . However, increasing the line width has diminishing returns due to non-uniformity in the current distribution, as explained in chapter 3 [Figure 5.2 (b)]. Moreover, a large line width will increase the overall footprint of the device.

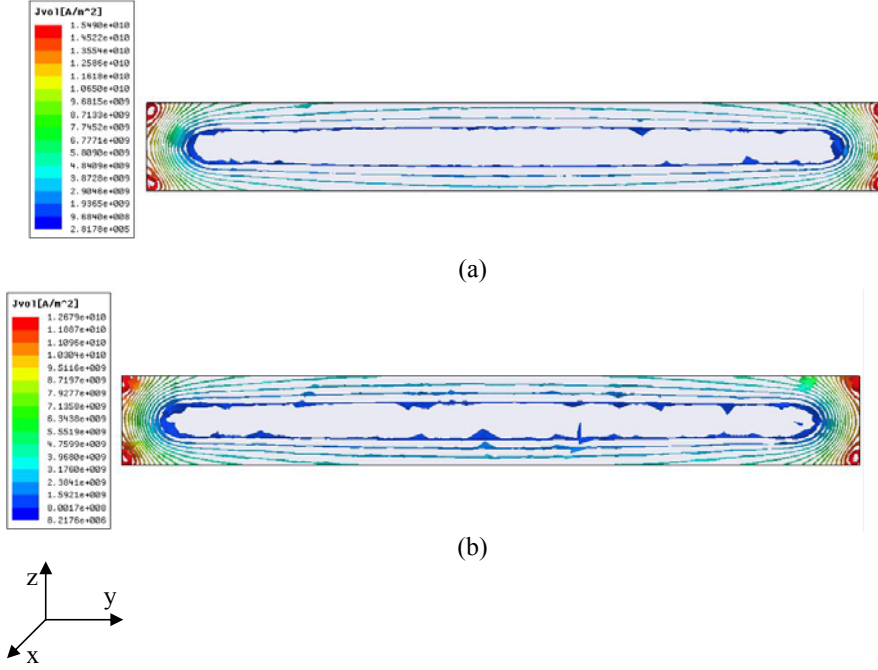


Figure 5.2: Current distribution in the cross section of (a) the signal line of a CPW (b) same geometry as a single conductor. Width of the line is $25\ \mu m$ and thickness is $3\ \mu m$.

In this chapter we investigate the application of the SAM HAR process to integrated coplanar waveguide (CPW) transmission lines to reduce their conductor loss. The expectation is that the application of high aspect ratio metal layers would help both in increasing the current-carrying cross-sectional area, and alleviating non-uniform current distribution due to proximity effect, which was demonstrated for spiral inductors in chapter 3. The following section presents the measurement results for SAM HAR CPW lines implemented on high resistivity silicon (HRS) and Af-45 glass substrates. In the third section another process developed for fabrication of HAR CPW lines embedded in HRS substrates will be introduced and the measurement results for the implemented lines will be given. Also the effect of embedding the CPW line into the substrate on the length of the line will be discussed.

5.2. High Aspect Ratio Coplanar Lines on High Resistivity Si and Glass substrates

5.2.1. Design and Implementation

To evaluate the improvement brought about by using HAR CPW lines, we intentionally consider CPW designs with a narrow signal line-width. CPW lines are preferred because their width and spacing can be changed for the same impedance, unlike microstrip lines which have fixed width for a given dielectric thickness and impedance. It is this flexibility in design that enables us to explore the effect of aspect ratio for narrow widths. Unlike planar CPW lines where metal loss is reduced by widening the signal line, here it is the high aspect ratio of the line which reduces the metal loss. Furthermore, similar to the inductors discussed in chapter 3, these transmission lines also benefit from the effect of the (more or less) uniform distribution of current density on the vertical walls of their conductors. A simulated current distribution cross section given in Figure 5.3 gives a good example of the utilization of the vertical walls for a CPW line with both narrow signal width and signal-to-ground spacing. In both Figure 5.3 (a) and (b) it is seen that most of the current is carried through the side walls of the conductor. Comparing the two cases, it is possible to observe that current is pulled to the surface and sides for the bottom and top walls of the conductor yet it is pushed inside for the side walls as we switch from a single conductor to the CPW configuration. This is expected to result in net reduction in R_s (Figure 5.1) as opposed to net increase for a thin wide conductor.

Table 5.1: R_s/mm (Figure 5.1) values for two conductor geometries in single conductor and CPW configurations. Standard represents thin wide conductors with width $25\text{ }\mu\text{m}$ and thickness $3\text{ }\mu\text{m}$ and HAR represents high aspect ratio conductors with width $5\text{ }\mu\text{m}$ and thickness $15\text{ }\mu\text{m}$. Therefore both designs have a cross-section of $75\text{ }\mu\text{m}^2$.

	Single conductor	CPW
Standard thickness	0.71	0.76
HAR	0.87	0.83

The resulting R_s values (Figure 5.1) extracted by taking the real part of simulated $1/Y_{11}$ are presented in Table 5.1 for single-conductor and CPW configurations. For a standard CPW line there is $\sim 7\%$ increase in R_s , whereas there is 4% reduction for HAR case. The differences are not as drastic as the spiral inductor situation since the magnetic field generated on the signal line by ground currents is reduced due to opposing magnetic fields of the two ground lines. It should be noted at this point that these changes are not constant and are dependant on the layout of the CPW. Also bear in mind that besides reducing the nonuniformity in current

distribution, the HAR process reduces the total footprint of the CPW line. This would be especially helpful on lossy substrate by reducing the capacitive CPW-substrate coupling and, thus, the resulting substrate loss.

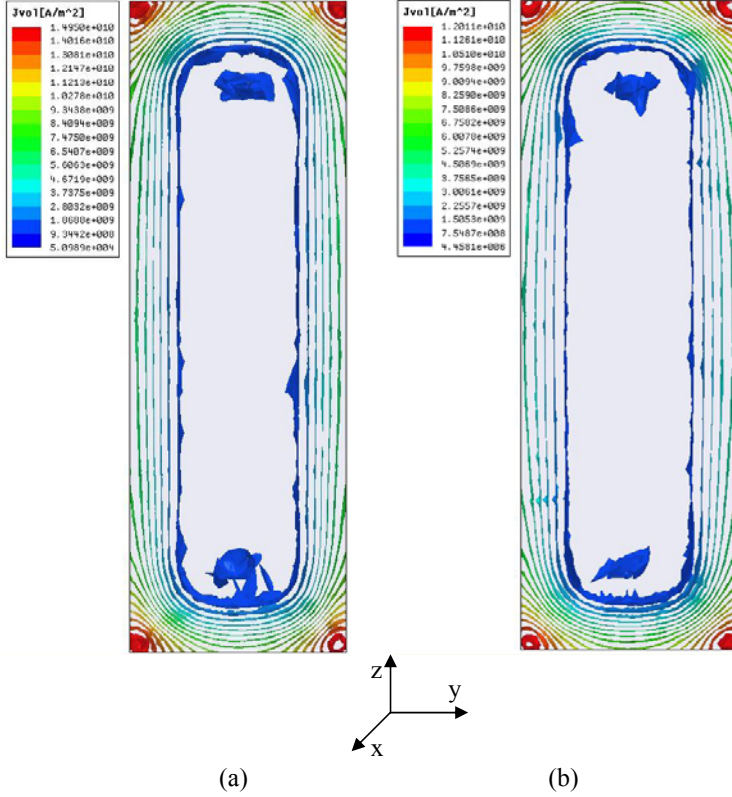


Figure 5.3: Current distribution in the cross section of (a) the signal line of a CPW (b) Same signal line as a single conductor without ground lines nearby. Dimensions of the line are: width = 5 μm , thickness = 15 μm .

For the actual device fabrication, signal line widths of 5, 10, and 15 μm were selected and the signal-to-ground spacing for each width is chosen such that the simulated devices have a nearly 50 Ω characteristic impedance on a HRS substrate, where substrate loss would be reduced to an insignificant minimum and differences in metal losses would be observed more easily. The resulting design geometries are summarized in Table 5.2.

Table 5.2: Design dimensions of CPW lines on HRS substrate.

#	Signal width (w)	Spacing (s)	Length (l)	Ground width (g)
1	5 μm	15 μm	5 mm	60 μm
2	10 μm	20 μm	5 mm	60 μm
3	15 μm	23.5 μm	5 mm	60 μm

Note that the $50\ \Omega$ transmission lines in Table 5.2 have a signal width smaller than the signal-to-ground spacing. The opposite would have been expected as the electric field surrounding the HAR line is mostly concentrated in the air-filled parallel-plate regions between the signal and ground conductors [Figure 5.4 (a) and (b)]. This would result in a relatively low line capacitance which may be compensated by reducing the signal-to-ground spacing in order to keep the same value of characteristic impedance. Yet, one should not forget that the HAR structure has a much lower inductance per unit length due to the close proximity of opposing currents flowing in the signal and ground lines. This effect overcompensates the decrease in line capacitance to the extent that the signal-to-ground spacing actually has to be increased in order to further decrease the capacitance and maintain the same characteristic impedance.

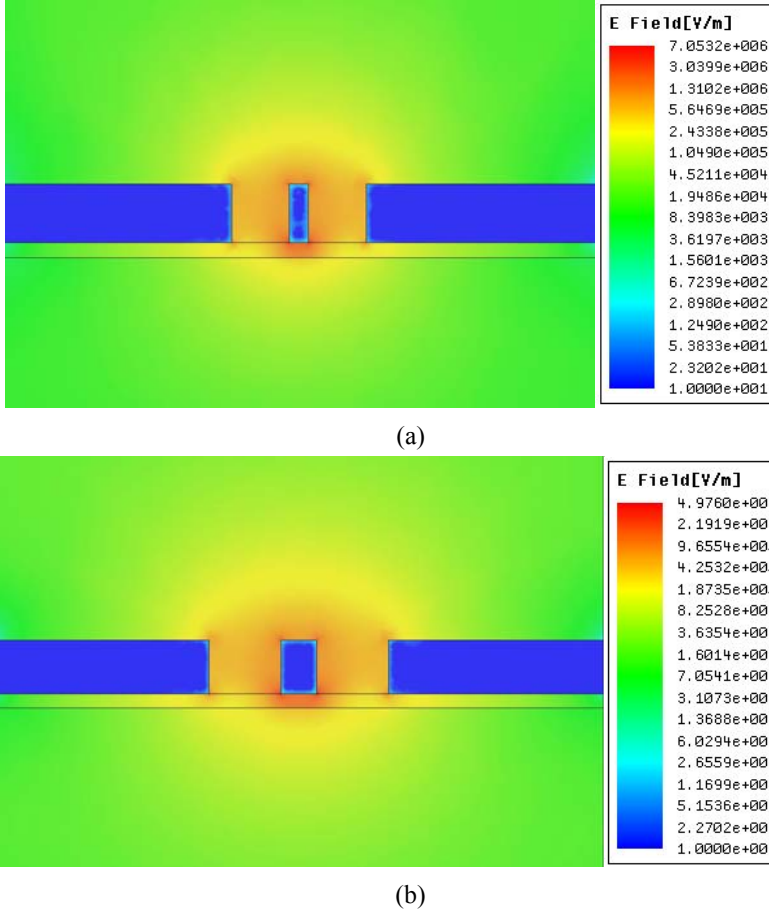


Figure 5.4: Electric field distribution in the cross section of HAR CPW designs (a) #1, and (b) #2.

The designs in Table 5.2 were implemented on HRS and glass substrates following the SAM HAR process described in chapter 3. During CPW line fabrication, deviations from the ideal case arise due to process limitations. As explained in chapter 3 diffraction of light causes a slope in the wall of photoresist mold, which in turn results in lines that become wider as they go upwards. This increase in width is expected to be less than $1\text{ }\mu\text{m}$ for a $15\text{ }\mu\text{m}$ thickness and 5° deviation from an ideal vertical wall. This is expected to alter the field configuration, hence the per unit length capacitance and inductance of the lines, This would result in $<10\%$ increase in total capacitance for the narrowest spacing design, which would mean a maximum error of 10% . Although this error can be considered acceptable, it can be possible to incorporate predictable fabrication errors in the design to reduce this amount.

5.2.2. Measurement

Fabricated transmission lines were measured by a HP8510 vector network analyzer. Due to the rather small spacing between the ground and signal conductors, the CPW designs listed in Table 5.2 were not suitable for direct measurement by means of microwave probes whose pitch is usually larger than $50\text{ }\mu\text{m}$. Therefore a tapered section as shown in Figure 5.5 is added to the ends of each line in order to widen the lines to match the dimensions of a GSG100 probe. Since these tapered sections are not part of the original transmission line, a thru structure shown in Figure 5.5 (b) was implemented for de-embedding their effect on line characteristics, by means of the technique described in chapter 3. Resulting 2-port S-parameters after de-embedding are then used to extract parameters of the transmission lines of Table 5.2.

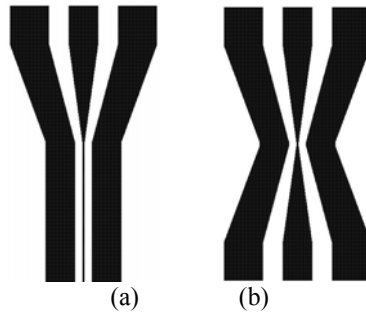


Figure 5.5: Layouts of a sample (a) CPW with a taper section (b) deembedding section.

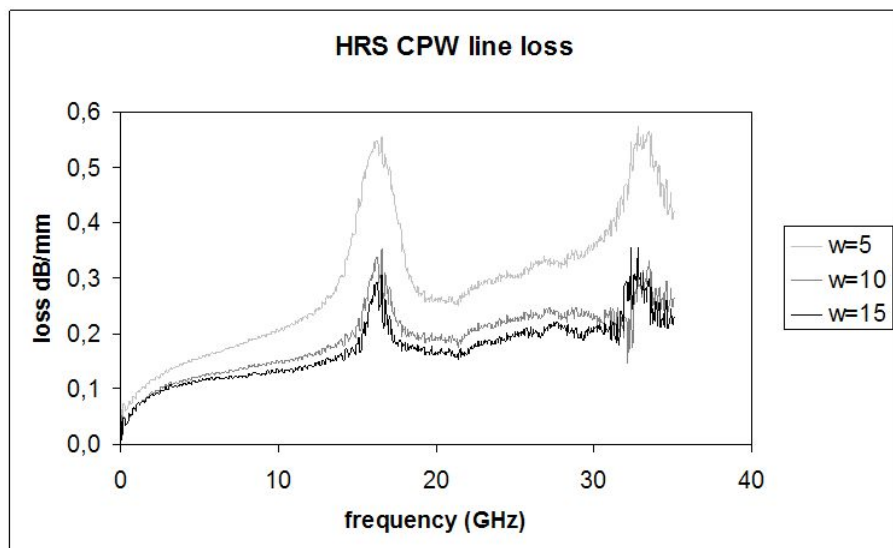
The effective permittivity of glass-based CPW lines increases with spacing, eventually reaching a value of 2.5, which is the approximate calculated value for a conventional CPW line on glass [7]. This is expected since for narrowly-spaced

designs most of the electric field is concentrated in the air-filled parallel plate region, leading to a low effective dielectric constant. Increasing the spacing will change the situation and the field distribution starts to look like that of a conventional CPW line. , In case of HRS the calculated approximate value for a thin metal CPW is 6.5, which is significantly higher than the measured value for the widely-spaced line. The reason for this discrepancy is the presence of the 4 μm -thick SiO_2 layer that has a much lower dielectric constant ($\epsilon_r=3.9$) than Si. Although the layer is very thin compared to whole substrate thickness of 500 μm , it is comparable to w , and s of the lines. Since electric field is concentrated around the gap between the signal and ground conductors in a CPW, the effect of oxide layer is amplified [Figure 5.4].

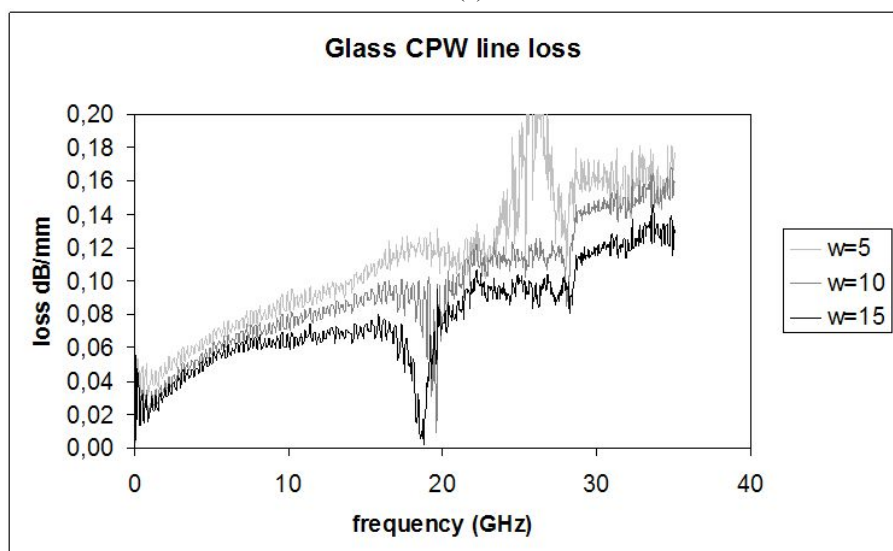
Table 5.3: Characteristic impedance Z_c , and effective permittivity ϵ_e results averaged over the frequency range 1-35 GHz. For the numbering of lines please refer to Table 5.2.

	Z_c	ϵ_e
#1 on Glass	123.7	1.39
#2 on Glass	86.2	2.41
#3 on Glass	81.9	2.57
#1 on HRS	64.3	3.47
#2 on HRS	67.1	3.45
#3 on HRS	67.5	3.48

The per-unit-length insertion loss of the CPW lines is presented in Figure 5.6 (a) and (b) for HRS and glass, respectively. It should be mentioned that increasing the width of the line reduces insertion loss with diminishing effect in all cases. This is an indication that the reduction of the nonuniformity in current distribution becomes less effective as the design becomes wider.



(a)



(b)

Figure 5.6: Insertion loss measurement results for CPW lines implemented on (a) HRS, and (b) Glass wafers. The dips observed near 19GHz are caused by line resonances.

Comparison of attenuation constants is justified when a transmission line is used for the transfer of microwave power over a given distance which is dictated by the circuit layout, e.g., when connecting two different circuit blocks. However, for the implementation of microwave components where the line length is a predefined fraction of the propagation wavelength, a better measure of quality is provided by the quality factor

$$Q = \frac{\beta}{2\alpha} = \frac{\pi}{\alpha\lambda} \quad (5.7)$$

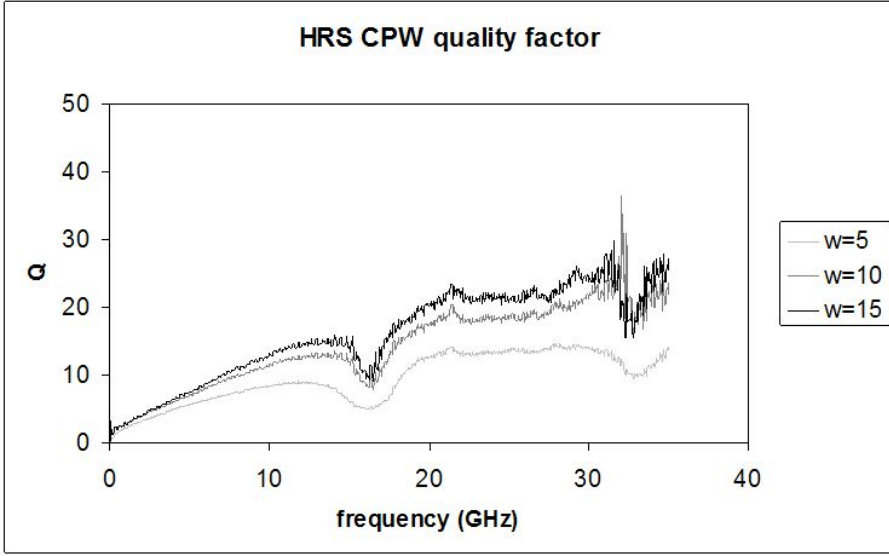
If the losses are small then the above quantity can be approximated by

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_C} \quad (5.8)$$

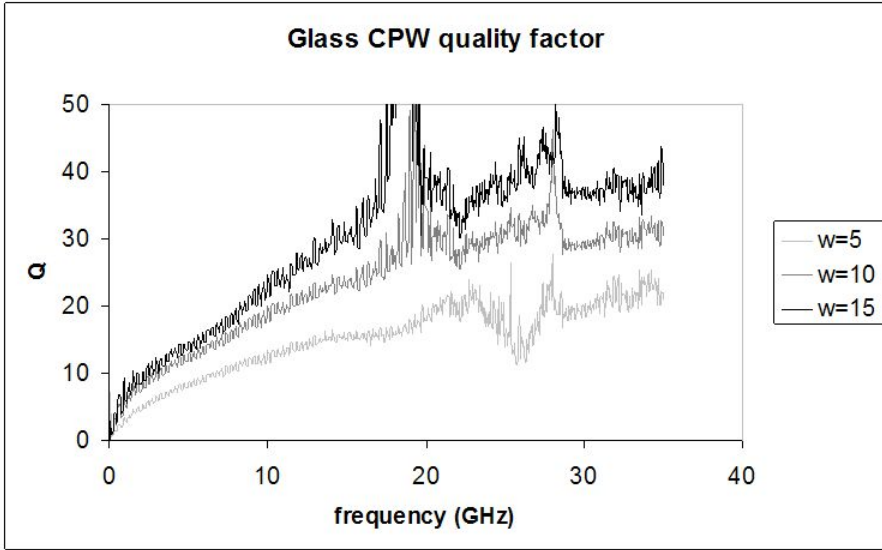
$$Q_L = \frac{\omega L_0}{R_0} \quad (5.9)$$

$$Q_C = \frac{\omega C_0}{G_0} \quad (5.10)$$

where we have used Eqs. (5.3)-(5.6). The quality factor Q given by equation (5.7) is shown for CPW lines on HRS and glass substrates in Figure 5.7 (a) and (b), respectively.



(a)



(b)

Figure 5.7: Quality factors of CPW lines implemented on (a) HRS, and (b) Glass substrates.

Glass-based CPW lines obviously have superior quality factors compared to HRS lines. This can not be caused by the conductor loss as the CPW lines are identical on the two substrates. Comparison of all results with the literature can be found in Table 5.6. The difference between glass and HRS should come from the substrate loss. It is well-known that relatively highly conductive channels are formed

on the surface of HRS substrates which can significantly increase device loss despite the highly resistive nature of the bulk substrate material. These channels are a result of accumulation of impurity charges present in the overlying SiO_2 at the Si/SiO_2 boundary [8, 9]. These charges would normally migrate to the impurities that are inherently present in LRS, however lack of such impurities in HRS and the availability of near perfect crystal structure and a surface results in the accumulation of charges and formation of so called inversion layer. These channels may be suppressed by a variety of techniques including the use of passivation layers [9]. These so called passivation layers actually aim to create imperfections near the surface to trap and redistribute these migrating charges or break the continuity of the inversion channel formed by them. However, if the surface passivation layer is not of high quality the additional substrate loss can still be present on HRS wafers.

5.3. High Aspect Ratio Coplanar Waveguide Lines Embedded in High Resistivity Si Substrates

The high aspect ratio lines demonstrated in the previous section are fabricated on the surface of the substrate. This would mean that the volume between the sidewalls of the conducting signal and ground lines are filled with air that has ϵ_r of 1. This causes ϵ_e to be lower than the theoretical value for conventional planar CPW lines with on a dielectric substrate given by

$$\epsilon_e = \frac{\epsilon_{sub} + 1}{2} \quad (5.11)$$

where ϵ_{sub} is the relative permittivity of the underlying substrate (11.9 for HRS).

If this space between the conductors were to be filled with the substrate material, then the resulting ϵ_e would be higher than the calculated theoretical value of ~ 6.5 . Therefore CPW lines with shorter physical lengths could be realized. The fabrication of embedded CPW lines and their measured electrical behavior is the subject of following sections.

5.3.1. Process Description

The difference between the process described in this section and the SAM HAR process described in chapter 3 can be understood by comparing the cross sections of two identical CPW lines built with these processes (Figure 5.8a and b).

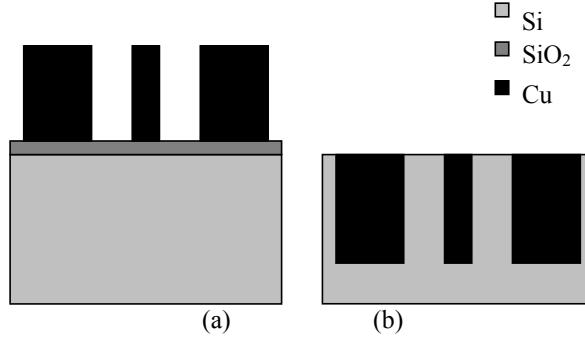


Figure 5.8: (a) Cross section of CPW lines fabricated with SAM HAR process. (b) Cross section of CPW lines fabricated with HAR embedded process.

In the embedded HAR process the first step is the opening of Si trenches that will be used as a mold for electroplating the Cu conductors. This is done by deep reactive ion etching (DRIE), which has the ability to etch trenches with relatively smooth and vertical sidewalls compared to photoresist molding as can be seen in Figure 5.9. The superior wall profile of DRIE removes the limitation on the aspect ratio due to mold problems. However, the second step of the process, which consists of seed layer deposition, reintroduces the limit on aspect ratio. Note that a continuous seed layer is a requirement for filling the trenches by electroplating. Sputtering the seed layer inside a trench including the sidewalls is not possible as the aspect ratio of the valley becomes more than 4. Hence the new limit on the aspect ratio of the structures is 4 instead of 3 in SAM HAR case. Taking minimum feature size $5\text{ }\mu\text{m}$, the maximum depth of the trenches is determined as $20\text{ }\mu\text{m}$. The seed layer used in this process is identical to the one used for HAR spiral inductors and CPW lines: a Ti/TiN/Cu sputtered seed layer with 20/80/300 nm thicknesses.

The next step of the process is the application of a photoresist layer that is used to form the patterns. Unlike damascene processing where electroplating is performed on the whole surface and patterns defined with the trenches are then realized by chemical mechanical polishing (CMP), this process requires a photoresist layer to define areas of electroplating hence features to be implemented due to lack of a final CMP step. This photoresist does not need to be as thick as the SAM HAR case, since the final thickness of the electroplated metal is dictated by the trenches anyway. However the photoresist needs to be uniformly coated on this non-uniform wafer surface poked by trenches. A suitable candidate for uniform photoresist coating on 3D surfaces is the electroplated photoresist. The Eagle 2100 ED electroplated photoresist coating is known to be applicable for patterning on 3D surfaces [10]. This is a so called negative tone photoresist. As opposed to positive tone photoresist, where regions exposed to light are dissolved during development, unexposed negative tone photoresist dissolves during development. This is an advantage for HAR embedded

process. In case of a positive photoresist all the photoresist in the valley, which is $\sim 25\text{ }\mu\text{m}$, needs to be exposed in order to be developed. However for a negative photoresist only exposure of the $\sim 5\text{ }\mu\text{m}$ -thick photoresist layer on the flat wafer surface is required. This would imply significantly less exposure time, which would increase the pattern resolution and repeatability.

After the photoresist is developed, Cu layer is coated by electroplating process. This step is critical for the end result. It is different from the electroplating process used in the SAM HAR module, which is done on a flat surface. It rather resembles the Cu –damascene electroplating process used in CMOS ICs, albeit with deeper trenches. The rate of deposition on the top edges of the trench are higher than the rate of deposition on the bottom sidewalls. This would result in a void in the centre of the trench as can be seen in Figure 5.9. Although for the purposes of CPW lines used in very high frequencies center of the line would not be so significant in terms of current flow, the process needs to be strictly controlled to achieve uniform device performance. The reason for this is the effect of process differences on the top surface of the conducting line, where there is considerable current flow. Differences in the depth of this surface or whether two sides of the trench are connected at the top or not would change the current distribution hence attenuation.

The final stage of the process is the removal of the photoresist and the seed layer, which is done with acetone and wet etching solutions described in chapter 3. At this point it should be mentioned that the process used in fabrication of the prototypes is not fully optimized for mass production. In case of mass production, making use of a CMP process for flattening the final surface is a better option to have flat surfaces on the top of the structures as shown graphically in Figure 5.8 (b) rather than uneven surfaces obtained in Figure 5.9.

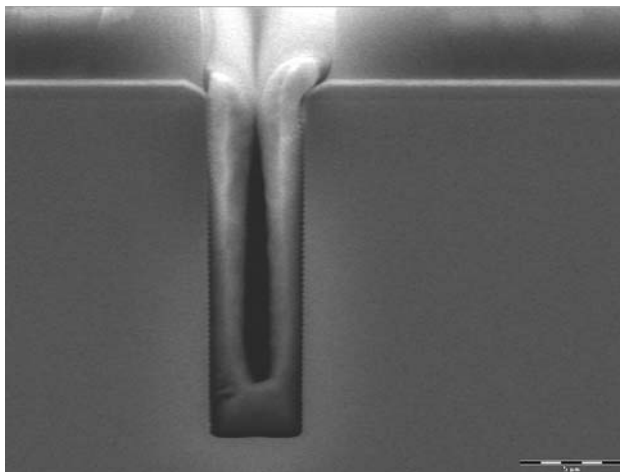


Figure 5.9: SEM cross section of an electroplated trench.

5.3.2. Design

From an electromagnetic point of view, the main difference between an embedded HAR CPW and a surface-mounted SAM HAR CPW is the move of the parallel plate region of the CPW from the surface into the substrate as depicted in Figure 5.8. As shown by the simulation in Figure 5.4 electric fields of HAR CPWs are concentrated in this region. Therefore the parallel plate region becomes important in determining the per unit length capacitance hence effective permittivity. Therefore changing the relative permittivity of this region from that of air ($\epsilon_r=1$) to that of Si ($\epsilon_r=11.9$) is expected to increase the effective permittivity of CPW which leads to a reduction of the physical length for a given electrical length.

In order to investigate this, embedded HAR CPW lines are designed and implemented. Similar to the SAM HAR case, 3 CPW lines are designed with fixed signal widths of 5, 10, and 15 μm (design geometries are given in Table 5.4). Like the previous case, lines are designed to have a $\sim 50 \Omega$ characteristic impedance.

Table 5.4: Design dimensions for CPW lines embedded in HRS.

#	Signal width (w)	Spacing (s)	Length (l)	Ground width (g)
1	5 μm	45 μm	5 mm	15 μm
2	10 μm	50 μm	5 mm	15 μm
3	15 μm	55.5 μm	5 mm	15 μm

Notice that s values are larger than their surface HAR counterparts given in Table 5.2. This would mean that for a given s , per unit length capacitance is higher in case of embedded HAR than surface HAR. An expected result of this wider spacing is the increase in the fringe electric fields, which in turn would reduce the significance of parallel plate region in determining the capacitance per unit length. Electric field distribution results for cross sections of design #1 and #3 given in Figure 5.10 (a) and (b) show an increase in fringe field strength and area. However one should note that at least half of the fringe fields travel through the high ϵ_r substrate, which helps in increasing effective permittivity. When the field distributions of embedded HAR in Figure 5.10 are compared to that of surface HAR in Figure 5.4 it is possible to see that most of the fringe fields in surface HAR travel through either air or the SiO₂ layer and little from the Si substrate. However in case of embedded HAR fringe fields travel equally from air and Si substrate. When the fields in the parallel plate region are added to this calculation it is possible to see that embedded HAR has majority of its fields in the Si substrate. Therefore it is possible to deduce from these field simulations that embedded HAR CPWs would have higher effective permittivities.

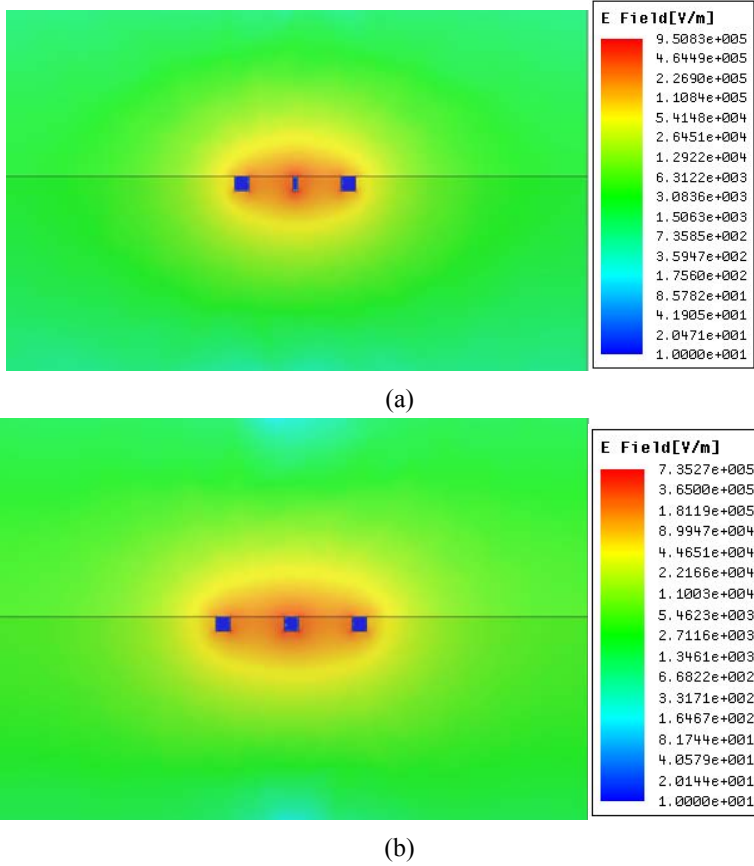


Figure 5.10: Simulated electric field distribution on the cross section of designs (a) #1, and (b) #3.

Another observation that can be made from comparing Figure 5.10 (a) and (b) is that as the spacing between ground and signal lines decrease so does the amount of fringe fields. This is important since the component of fringe field travelling through air would be critical in determining ϵ_c . Since designs are desired to have $50\ \Omega$ characteristic impedance these gaps are so wide. However if the characteristic impedance was to be reduced to a lower value then the gap would be narrower, hence ϵ_c would be higher.

Similar to the CPW lines on Glass and HRS, taper sections are added to the terminals of the embedded lines to enable microwave characterization by RF measurement probes. These sections are fabricated on the wafer surface to ensure a flat surface for the probe to land. Effects of these taper sections are deembedded during measurement by using appropriate thru taper geometries. Measurement results and comparison of these results with the previous ones are presented in the next section.

5.3.3. Measurement and Discussion

Transmission line parameters of the implemented structures are extracted from the scattering matrix that is obtained through measurement of the transmission lines and de-embedding of the taper structures as explained in section 5.2.2. Resulting characteristic impedances and effective permittivities are given in Table 5.5. Notice that effective permittivity values are significantly higher than the CPW lines fabricated on glass or HRS as expected. On average embedded lines introduce 79% reduction in length compared to conventional planar CPW lines on glass, 51% on HRS, and 11% compared to theoretical value of standard planar CPW lines calculated by equation 5.12. It should be noted at this point that ϵ_e values increase with decreasing the signal-to-ground spacing s as percentage of field travelling in the high permittivity parallel plate region increases with the reducing fringe fields, which can be seen in the simulation results given in Figure 5.10. Therefore one could advise reducing s to even shorten the physical length. However this would result in higher capacitance and lower characteristic impedance for a fixed w . Therefore it is possible to say that length reduction potential of the process can be better utilized in low impedance applications.

Table 5.5: Characteristic impedance and effective permittivity of CPW lines given in Table 5.4.

#	Z_c	ϵ_e
1	44.8	8.4
2	46.9	8.1
3	48.1	7.7

Insertion loss per unit length of embedded CPW lines is presented in Figure 5.11. The values are comparable to that of SAM HAR lines on HRS substrate. It is again possible to observe that as w increases insertion loss decreases with diminishing effect. Calculated quality factors of embedded CPW lines are presented in Figure 5.12. They are comparable with CPW lines implemented on glass.

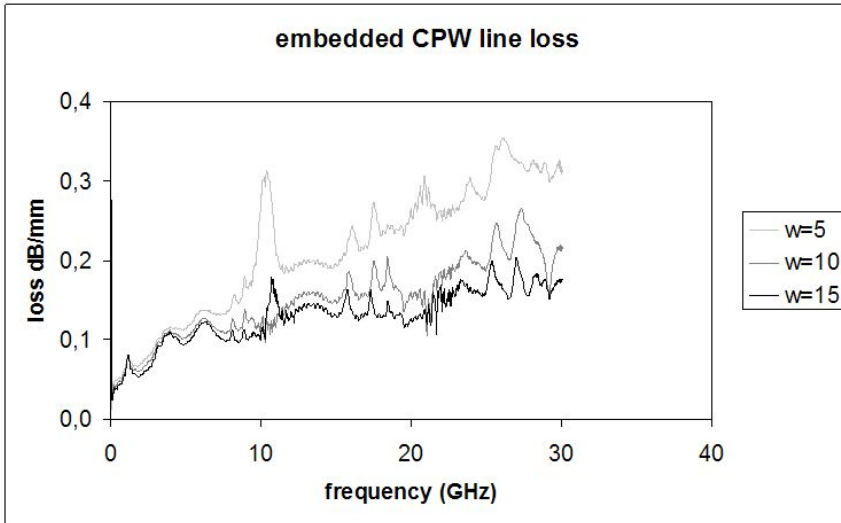


Figure 5.11: Insertion loss measurement results for CPW lines embedded in HRS substrate.

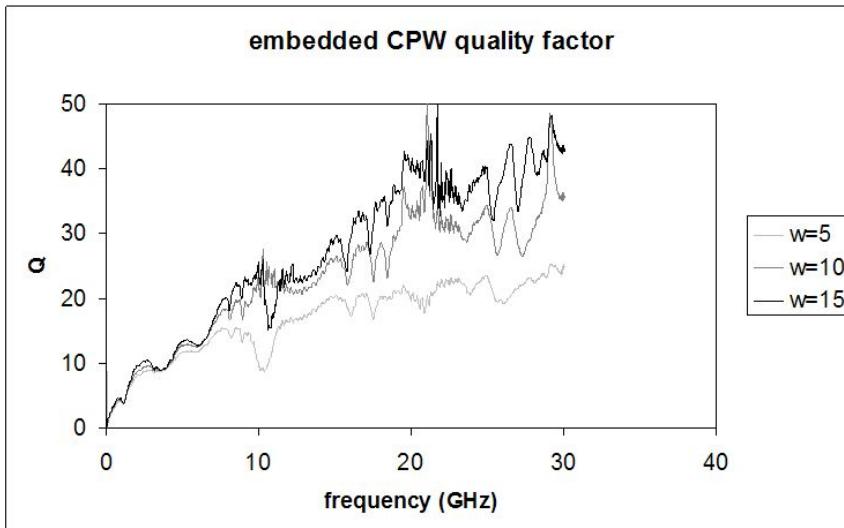


Figure 5.12: Quality factor results for CPW lines embedded in HRS substrate.

Comparison of quality factors given in Figure 5.12 with quality factors of CPW lines fabricated on glass and HRS substrates would be helpful in understanding the performance improvement introduced with each process. Such a comparison is given in Figure 5.13 for CPW lines with 15 μm signal width. Although insertion loss per unit physical length is higher for embedded lines, they make up for this loss in quality factor by having high effective permittivities. Glass and embedded lines have

same quality factors but embedded lines are $\sim 80\%$ shorter for a given electrical length. Since transmission line circuits are defined in electrical lengths, embedded lines would be on the same par with glass lines in loss comparison, but would excel in reduction in physical length.

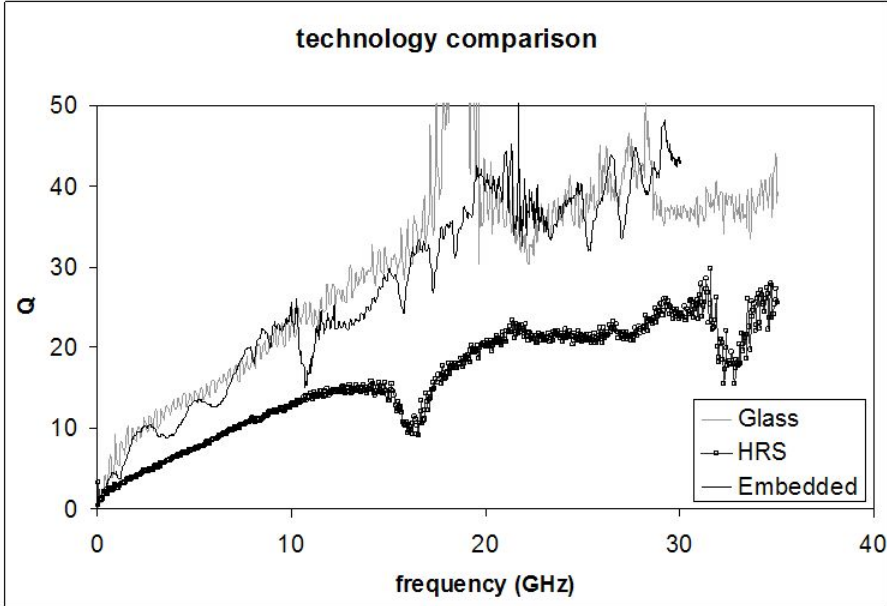


Figure 5.13: Quality factors of CPW lines implemented with different technologies. All CPW lines have a fixed w of $15\ \mu\text{m}$.

Although comparing just the attenuation or quality factor of different CPW lines in the literature with each other is a bit unfair since there are other figures of merit while fabricating the lines such as size, cost, bandwidth, and etc., it is a common practice which helps in understanding the position in the big picture in terms of loss performance. Such a comparison is presented in Table 5.6. Although insertion loss of embedded lines seem to be similar or higher than most of the cases, quality factor of embedded lines are in fairly good position among other devices in the literature. Therefore it is possible to say that high aspect ratio embedded CPW technology introduces short length transmission lines with good quality factors.

Table 5.6: Measured α (attenuation db/mm), Q (quality factor eq. 5.3), and ϵ_e (effective permittivity) data for several integrated transmission lines in the literature. Last three rows represent the results of this work.

Reference	α @10	α @20	α @30	Q @10	Q @20	Q @30	ϵ_e
[11]	0.164	0.315	0.535	38	40	36	48
[12]	0.17	0.23	0.25	17	23	33	8.3
[5]	0.02	0.025	0.03	45.4	72.7	90.9	1.1
[6]	0.23	0.3	0.34	5.6	8.6	11.3	2
[13]	0.16	0.18	0.24	-	-	-	-
[14]	0.05	0.1	-	-	-	-	-
[15]	0.008	0.018	-	-	-	-	-
[16]	0.17	0.21	0.29	6.5	10.6	11.5	1.5
[17]	0.025	0.045	0.08	36.3	40.4	34.1	1
[18]	0.055	0.08	0.09	27.1	37.3	49.8	2.7
[19]	0.03	0.055	0.1	30.7	33.5	27.7	1.03
[20]	0.03	-	-	38.3	-	-	1.6
[21]	0.05	0.08	-	-	-	-	-
[22]	3	4.5	5.5	1.5	1.8	2.1	-
[22]	2	3	3.8	1.8	2.4	2.6	-
[22]	1.4	2	2.4	2.3	2.9	3.4	-
hrs	0.1	0.14	0.17	12	20	24	3.48
glass	0.06	0.08	0.1	24	38	38	2.57
embedded	0.1	0.12	0.14	24	40	46	7.7

5.4. Conclusion

CPW transmission line integration is an ongoing process with focus areas on micromachining for loss reduction and high k materials, ferromagnetic materials, and slow wave periodic structures for length reduction. SAM HAR process is used for implementation of narrow width lines on HRS and glass substrates to observe process performance. Measured lines show decent insertion loss and quality factor results. A post process module that uses DRIE process is developed to implement CPW lines embedded in HRS substrate. Resulting lines show fairly good insertion loss and quality factor results with increase in effective permittivity hence further reduction in length. Both processes are single mask cost effective solutions to passive device performance problem. Latter module is especially suitable for CPW lines due to effective reduction of physical line length.

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Chapter 6

Conclusions and Recommendations

This thesis focuses on development and evaluation of add-on process modules that are intended for cost-effective implementation of quality-optimized RF passive components with the integrated circuit chip. The work is driven by a strongly increasing trend toward integrating the passive components rather than implementing them into the chip package or providing them as discrete. Since Si technology has been and will remain to be the dominating semiconductor manufacturing technology such add-on modules for PF passives need to be developed likewise and always with attention to low-cost and high-volume fabrication capability.

However, integrated passives on a Si substrate generally suffer from two kinds of loss mechanisms. Since the thickness of the metal interconnects in common Si fabrication processes is limited in order to meet fine pitch requirements metal losses are pronounced, particularly at low frequencies. At high frequencies the RF signal tends to propagate away from the metal structure of the RF component into the electrically conducting Si substrates, thus causing substrate losses.

To overcome (or at least alleviate) these limitations in a cost-effective way add-on modules have been proposed and introduced. The add-on processes developed in the course of this work focus essentially on reducing metal losses. Hence they provide a metal structure that leads to reduced RF metal losses at minimum effect on parasitic capacitances and inductances.

The most significant aspect of this add-on process is the compatibility with the core CMOS and BiCMOS process technologies. This is important because an add-on module should be able to be applicable to a wafer coming from any standard silicon factory. Any modification required to the core process would lead to excessively high cost.

Besides compatibility with the core Si process, an add-on process module should have no detrimental impact on the manufacturing aspects of that Si process. The overall fabrication cost, the device reliability, the packaging capability and the fabrication flow should be impacted as little as possible.

Following this intention two dedicated add-on process modules have been developed in this work. The High Aspect Ratio Saddle Add-on Module (HAR SAM) utilizes a thick photoresist mold and copper electroplating to form thick copper tracks with an aspect ratio of 3 on top of the chip. The process uses only one mask to place these tracks locally over designated interconnects, for which the ohmic metal losses should be reduced. The key benefit is that locally thick metal lines can be provided without sacrificing the fine metal pitch elsewhere, which is typically required for interconnecting dense circuitry. Therefore, the HAR SAM module allows for avoiding an unattractive compromise and costly modification of the IC interconnects. HAR metallization is also applied in the second add-on process module, which, however, positions that HAR structure into the Si substrate. There, instead of using photoresist as a mold trenches are etched in Si substrate by DRIE and isolated for that purpose. For cost reasons the metal refill of those trenches is arranged by lateral instead of bottom-up electroplating of copper like in a damascene process used for common interconnect integration. Structure aspect ratio as high as 4 could be imbedded into the Si substrate.

More detailed conclusions are given in the following for each of the thesis chapters separately.

6.1. Chapter Conclusions

Chapter 3

Metal loss in RF passives is effectively reduced when the Saddle SAM HAR process module is applied. This is evident from electromagnetic evaluation and high-frequency characterization of spiral inductor structures implemented on both low-(LRS), and high resistivity silicon (HRS) substrates. Inductor designs were optimized as seen from the good agreement of measurements and simulation based on an in-house developed concentric ring model. The following conclusions were drawn:

- Optimized SAM HAR inductors tend to have narrow metal tracks. This is in contrast to conventional, planar Al-based devices, which have rather wide tracks. This is an indication that metal losses in SAM HAR inductors are low compared to substrate losses, while planar inductors have relatively high metal

losses that are minimized by widening the metal tracks at the expense of a higher metal-to-substrate capacitance.

- Generally, the distribution of current density in the metal tracks of spiral inductors is such, that the current density is considerably higher near the vertical sidewall of the metal due to proximity effects. Therefore, the distribution of current density over the cross-section of the windings of a SAM HAR inductor is more uniform compared to a planar coil. The relatively reduced current-crowding leads to reduced metal loss.
- SAM HAR coils have a smaller footprint compared to a planar inductor. This reduction in footprint results in a smaller metal-substrate capacitance which reduces the substrate loss and leads to an increased resonance frequency. The smaller footprint allows for saving chip real estate and thus leads to cost savings.
- Overall, SAM HAR inductors exhibit 100% increase in Q_{max} values for inductors on LRS and 75% for inductors on HRS on average.

Chapter 4

In addition to evaluating electromagnetic performance of SAM HAR process, thermal characteristics have been investigated extensively in order to explore the issue of self heating in suspended inductors. The motivation behind this work is to investigate the feasibility of using micromachined inductors in high power circuits, such as power amplifiers. As a first step suspended inductors with 3 μm Al metallization and 4 μm SiO_2 membranes were fabricated. Then current is applied to these devices and their average temperature is measured using the DC resistance as an indicator. The following conclusions were drawn:

- Suspended Al inductors exhibit an increase in temperature as high as $\sim 450^\circ\text{C}$ at 100 mA DC current. This change results in a reduced Q due to increase in metal resistance and also leads to transient effects. The thermal time constant is of the order of 10 ms, which is comparable to operation cycle of switched power circuits in communication devices. This would result in an altered characteristics of the inductor during operation, which has to be considered in RF circuit design.
- During the experiments some of the inductors could not withstand to such high currents with melting of the metal as a result. SEM pictures of destroyed devices show a number of failure points which lie close to each other on the parallel tracks of a spiral at positions that are furthest from the contact points. This is because parallel tracks of a spiral coil can be considered thermally

shunted, as confirmed by simulations. This effect is caused by the underlying dielectric membrane which acts as a thermal shunt.

- SAM HAR module minimizes self heating of suspended inductors due to higher thermal conductivity of Cu and larger cross section of the fabricated inductors tracks due to the thick metal. Experiments show the average temperature rise of suspended SAM HAR inductors to be just 10% of their Al counterparts.

Chapter 5

Substrate embedded SAM HAR structures were evaluated by applying the module in fabrication of CPW lines on HRS and Af-45 glass substrates. Measurement results showed a very low attenuation per unit length for CPW lines on glass compared to those on HRS. However, glass lines have relatively low effective permittivities compared to HRS lines, which would cause them to be physically longer for a given design. Physically shorter lines lead to reduced chip area consumption and thus cost savings. Therefore, a special process module was developed for embedding HAR CPW lines in the silicon substrate. The process uses only two additional mask levels, i.e. trench etching into silicon by DRIE and damascene-like metal refill by Cu electroplating. The following conclusions were drawn:

- Attenuation of CPW lines is observed to reduce as the width of the signal line is increased. This is expected since increasing signal line width would mean reducing series resistance hence conductor loss. However A surprising observation was that the rate of loss reduction was dropping with each successive step. This is due to the higher current density near the vertical walls of the conductors. As the width of the lines is increased, the role of these currents hence performance improvements they introduce are reduced.
- Embedded lines also show a similar trend of loss reduction with SAM HAR lines. Results show attenuation per unit length values comparable to SAM HAR lines implemented on the HRS surface. This shows that effect of sidewall currents are similar for both SAM HAR and embedded HAR lines.
- The main advantage of an embedded HAR presents itself with the reduction in physical length. Although they have similar quality factors, embedded lines are on average 80% shorter than lines implemented above the substrate. This length reduction is due to higher effective permittivity of embedded lines, which show an upward trend as the gap between signal and ground becomes narrower.

6.2. Recommendations

Aspect ratio is the key element in the SAM HAR process. Therefore research on improved electroplating molds in case of SAM HAR is an area of high interest. Deposition of a reliable seed layer is the first and foremost problem limiting the increase in aspect ratio for the embedded SAM HAR. Therefore different metallization techniques should be compared to achieve this goal. Also the electroplating process itself can be refined to improve uniform and conformal coating inside the trench. A final CMP step would help in achieving better uniformity. Another option for embedded HAR is to design the trenches so that a final metallization step of the core integration process can be employed to fill in these trenches. Since embedded HAR is similar to damascene process this option would not require any modification in the core process. Such an option would also reduce the number of masks by one hence reduce the cost of fabrication.

The Second point of attention is the thickness of the metal layer. Larger thickness usually leads to a larger pitch of the metallization layer for a given aspect ratio. A smaller pitch would allow for a smaller footprint and hence an increased maximum frequency and less chip area consumption. Since skin depth reduces with increasing frequency, thinner layers might have an advantage as the operating frequency is increased. Therefore it might be of interest to formulate an optimal thickness for a given frequency range and substrate option.

Another important issue is the combination of these processes with a high resistivity silicon (HRS) substrate. Since HRS would require a surface passivation layer to display its full performance, it is important to investigate optimal surface passivation techniques. This is especially important for embedded HAR process since deposition of layers, or any kind of process becomes complicated once a high aspect ratio trench is etched. Techniques such as atomic layer deposition (ALD) are known to support conformal deposition on extreme geometries. Hence they might be ideal candidates whenever a suitable material that can be deposited with ALD that supplies sufficient surface passivation is available.

Another aspect of surface passivation is the behavior of these embedded lines on a poorly passivated or non-passivated HRS substrate. Since the charges collected at the inversion layer can be manipulated with DC bias a proper biasing scheme can be applied to deplete these regions and thus reduce losses. This option of minimizing the loss through DC biasing should be investigated

Introduction of silver electroplating in the SAM HAR process would result in lower metal losses due to higher conductivity of silver compared to copper. However one should pay attention to compatibility issues related to silver deposition patterning, and any additional diffusion barriers if necessary.

Summary

Commercial wireless communication technologies stemmed mostly from the research done during and after the World War II as outlined in Chapter 1. Earlier systems were intended for military applications, hence had high performance and were very expensive and bulky. Later, with the dawn of commercial microwave applications, the systems began to shrink in size and cost. This was possible due to technological developments in the fabrication of integrated circuits. These developments allowed for the integration of more and more active components into a single chip. However, passive components could not catch up with the trend due to integration problems. Passive components were very big and, when fabricated on a lossy substrate, suffered from metal as well as substrate losses. To overcome these drawbacks, researchers developed several technological solutions, some of which are explained in Chapter 2, to improve the integration of passive components. Some of the key points of these technologies are compatibility with the core fabrication processes such as CMOS, and cost and complexity of fabrication.

This work focuses on a technological process intended to reduce metal loss in passive devices. The process is based on the implementation of a thick top metal layer that will reduce the ohmic resistance and, thus, the metal loss. However, just increasing metal thickness would not be very effective at high frequencies due to the skin effect, which practically renders the core of a metal useless in terms of current carrying capability. Therefore rather than just increasing the thickness the focus in this work is on increasing the conductor aspect ratio (height/width). In this way it is possible to utilize side walls of metal tracks for carrying high current density and, thus, have a much lower resistance for the same metal cross sectional area if compared to a planar metal conductor.

The process is tested for spiral inductors fabricated on different substrates. The experimental results are presented in Chapter 3. Both experimental and theoretical results (simulations) confirm that concept. High-aspect-ratio conductors are effective

in increasing the quality factor of inductors on both low-loss (HRS) and lossy (LRS) substrates. Performance improvement is more significant on LRS, since high aspect ratio process reduces the inductor's footprint, hence the substrate loss.

In addition to evaluating its electromagnetic performance, thermal characteristics of the process are investigated. This became a necessity after experimenting on suspended inductors with thin metallization at high input power. As outlined in Chapter 4 under high-power conditions suspended inductors may heat up to temperatures as high as 400 °C. This was expected due to lack of an effective thermal power dissipation path in case of a suspended inductor. What was unexpected was the role of the underlying membrane, which acted as a thermal shunt and averaged the temperature between windings preventing from high temperature peaks within the inductor coil. After modeling the structure through simulation it was seen that majority of the power was dissipated through metal leads. Hence increasing the thickness of the metal conductor to achieve a high aspect ratio structure would help in alleviating the problem. Experiments done on suspended inductors with thick metallization indeed showed that the self-heating was significantly reduced.

The final part of the work deals with the impact of the high aspect ratio structuring on integrated coplanar waveguides (CPW). Therefore several CPWs on HRS and glass substrates were fabricated and characterized. The results given in Chapter 5 indicate lower loss due to high aspect ratio metallization. However metal loss is not the only problem that sets back transmission line integration. The chip area consumption of transmission lines is also a big issue that the cost associated with CPW integration. In order to reduce the size of the CPW a buried high aspect ratio CPW structure was introduced. The related fabrication process uses DRIE to etch trenches into the silicon substrate and electroplating to refill them with copper. These embedded CPWs have considerably higher effective permittivity, which results in ~80% shorter transmission lines for the same electrical length.

In conclusion, high aspect ratio metallization is effective in integration of passive devices such as spiral inductors and CPW lines by reducing their loss and physical size. Since the approach is simple and cost effective, as well as compatible with the core CMOS processes, it is expected to be widely applicable.

Samenvatting

Het grootste deel van de commerciële draadloze-communicatie technologie stamt af van de onderzoeken gedaan tijdens en na de tweede wereldoorlog, zoals staat aangegeven in hoofdstuk 1. Systemen die eerder zijn gebruikt, waren eigenlijk bedoeld voor militaire doeleinden, en hierdoor wél hoog in prestatie, maar duur in de aanschaf en grootschalig. Met de commerciële magnetron applicaties begonnen de systemen kleiner te worden, zowel in grootte als in kosten. Dit alles werd mogelijk dankzij de technische ontwikkelingen in het fabriceren van geïntegreerde schakelingen. Deze ontwikkelingen zorgden voor de mogelijkheid dat betrekkelijk om veel meer actieve componenten in een chip te integreren. Toch konden de passieve componenten deze trend niet bijhouden vanwege problemen met de integratie van deze componenten. Passieve componenten waren zeer groot, en wanneer ze op een substraat gefabriceerd werden, leden ze onder parasitaire effecten, zoals substraat- en metaalverlies. Om deze problemen te voorkomen, ontwikkelden onderzoekers een aantal technologische oplossingen om de integratie van passieve componenten te verbeteren. Sommige hiervan worden besproken in hoofdstuk 2. Enkele belangrijke punten van deze technologieën zijn verenigbaarheid met de kernprocessen, zoals CMOS, en de kosten en complexiteit van de fabricage.

Dit werk richt zich op een technologisch proces, dat bedoeld is om metaal-verlies in de passieve apparaten te reduceren. Het is gebaseerd op het uitvoeren van een dikke metalen bovenlaag die het metaal-verlies zal verminderen. Echter, simpelweg de metaaldikte verhogen zal niet zo effectief zijn in hoge frequenties door het “skin-effect”, welke er praktisch voor zorgt dat de kern van een metaal nutteloos wordt in termen van hedendaagse uitvoering van vermogen. Dus eerder dan alleen de metaaldikte verhogen, richt het proces zich ook op het verhogen van de “aspect-ratio” (hoogte/breedte). Op deze manier is het mogelijk om vooral de zijwanden van de metalen “tracks” te gebruiken voor het transporteren van stroom. Zodoende heeft deze

structuur een relatief veel lagere weerstand voor dezelfde metaal-dwarsdoorsnede bij hoge frequenties.

Het proces is getest met spiraalspoelen die gefabriceerd zijn op een aantal verschillende ondergronden. De resultaten van deze experimenten staan vermeld in hoofdstuk 3 van dit proefschrift. Zowel de experimentele- als de theoretische resultaten (simulaties) geven aan dat het idee om de zijwanden te gebruiken als stroomgeleiders een goed concept is, met een hoge kans op slagen. Het proces helpt de kwaliteitsfactoren van de spoelen te verhogen. Dit geldt zowel voor de “low-loss”- (HRS) als voor de “lossy” (LRS)-substraten. Prestatieverbetering is belangrijker en invloedrijker voor de LRS. De oorzaak hiervoor ligt in het feit dat het proces zowel de “device footprint” alsmede het substraatverlies reduceert.

Als aanvulling op het evalueren van de elektromagnetische prestaties, zijn ook de thermische eigenschappen van het proces onderzocht. Dit werd een noodzaak na het experimenteren met zwevende spoelen met een dunne metallisatie onder een hoge stroominput. Zoals uiteengezet is in hoofdstuk 4 van dit proefschrift, kunnen zwevende spoelen opwarmen tot wel 400 °C wanneer ze onder een hoog elektrisch vermogen staan. Aangezien dat er een tekort is aan thermische paden van de zwevende spoelen in het algemeen, was dit wel te verwachten. Wat echt onverwachts is te noemen, is de rol van de onderliggende membraan. De membraan werkt namelijk als een thermische “shunt” die de temperaturen tussen de wikkelingen regelt, en op deze wijze betrekkelijk zeer hoge plaatselijke temperaturen voorkomt. Na het modelleren van de structuur door middel van simulatie, is duidelijk geworden dat het grootste deel van de stroom verdreven word door de metalen contacten. Vandaar ook dat het verhogen van de metaaldikte met een hoge “aspect-ratio” processing zal helpen het probleem te verminderen. Experimenten die gedaan zijn op zwevende spoelen met een dikke metallisatie, tonen inderdaad aan dat het probleem aanzienlijk gereduceerd.

Het laatste deel van dit werk gaat over het onderzoek naar het effect van het “aspect-ratio-proces” op geïntegreerde golfgeleiders. Hiervoor is er een aantal CPW’s gefabriceerd op HRS- en op glas substraten. Tevens zijn hun prestaties gemeten. De resultaten zoals te zien in hoofdstuk 5, tonen een lager verlies aan ten gevolg van een “hoge-aspect-ratio” metallisatie. Metaalverlies is echter niet het enige probleem dat transmissielijnintegratie tegenhoudt. Het gebruik van transmissielijnen van de chip is ook een groot probleem dat deze integratie belemmerd. Om de grootte van deze transmissielijnen te verminderen, is er een ander “hoge-aspect-ratio-proces” geïntroduceerd. Dit proces gebruikt “DRIE” om sluisen te etsen in het siliciumsubstraat, en elektroplating om ze daarna te vullen met koper. Resulterende structuren zijn “hoge-aspect-ratio” CPW’s die zijn ingebed in het siliciumsubstraat. Zij hebben een betrekkelijk betere en effectievere permittiviteit, hetgeen resulteert in ~ 80% kortere transmissielijnen voor dezelfde elektrische lengte.

Concluderend kunnen we zeggen, dat “hoge aspect ratio” metaal process” helpt bij de integratie van de passieve componenten zoals spirale spoelen en CPW lijnen door het reduceren van zowel het verlies als de grootte. Omdat het een relatief eenvoudig en kosteneffectief proces is dat compatibel is met kernprocessen, is dit naar verwachting breed en algemeen toepasbaar.

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Acknowledgments

The research presented in this thesis is the culmination of strenuous efforts of many people in various departments and institutions such as High Frequency Technology and Components (HiTeC), Electronic Components Technology and Materials (ECTM), and Delft institute of Microelectronics and Submicron Technology (DIMES). Though it is a futile effort to completely acknowledge all these people aptly, it would be unfair not to try.

I would like to begin by thanking my supervisor Professor Achim Burghartz for his support and guidance through this research. I also would like to thank my daily supervisor Professor Behzad Rejaei for his invaluable help in completing this research. Patience, and continued trust of Professor Burghartz, and Professor Rejaei together with their never ending support were the key elements in continuing this work through hard times. Their proofreading and comments while writing this thesis have been vital.

I would also like to thank Professor Lina Sarro for her role in this work as a great help and a guide whose energy has motivated me throughout this work. Her insight in processing technology has helped me through many hurdles of fabrication. Also her great communication skills has been instrumental in my integration into the great family of DIMES.

DIMES has been the home that this work has grown in. This project would not have been successful without such a well equipped and well organized institution. I would like to thank all the people in DIMES for being there. I especially would like to thank to Wim Wien for being so helpful especially in photoresist coating techniques, Hugo Schellevis for helping in almost everything and helping realize my craziest process ideas, Mario Laros for helping with dry etching and giving detailed explanations to my endless questions. I would like to thank Tom Scholtes for giving me vital lessons on safety while working in cleanroom, and Silvana Milosavljevic for helping me in obtaining my cleanroom diploma. I would lie to thank Atef Akhnoukh

for his help in setting up and performing microwave measurements as well as his help in layout design.

I would like to thank my colleagues Hsien Chang Wu, Alexander Polyakov, Francesco DePaola, Maria Arcangelo Nigro, Saoer Sinaga, Marco Spirito, Koen Buisman, Edmund Neo, Yue Ma, Pedram Khalili Amiri, Pham Phuong Nga, and many others who have gone through the PhD process like me and has shared their friendship and invaluable advices.

I would like to thank Marysia Lagendijk-Korzeniewski, Birgit Rademakers, Marian Roozenburg, and many other administrative personnel for their help in many dreadful administrative papers and for their smile, which always gave a positive energy to me.

I would like to thank Tuncay Alan, Alper Koz, Umut Tabak, Suleyman Tursucu, and many other Turkish people who I met in a land far from home and who have been good friends.

Last but not least I would like to thank my family for supporting me through many hurdles of life, for guiding me with their experience in life to a better path, for being so patient and understanding, and for many things that I do not even know or realize.

Biography

Huseyin Sagkol was born in Ankara, Turkiye on the 8th of July 1976. He received his B. Sc degree and M. Sc degree from Middle East Technical University Electrical and Electronics Engineering Department in 1999 and 2002 respectively. His M. Sc project was the development of discrete and continuous phased shifters based on RF MEMS switches and adjustable capacitors. In September 2003 he joined ECTM group at the Delft University of Technology, where he worked towards his PhD degree in the field of micromachining. His research focused on development of post process micromachining modules for RF applications.