Large-Area Selective CVD Epitaxial Growth of Ge on Si Substrates

A. Sammak, W. deBoer, L. Qi and L. K. Nanver

Abstract— **Selective epitaxial growth of crystalline Ge on Si in a standard ASM Epsilon 2000 CVD reactor is investigated for the fabrication of Ge p$^+$n diodes. At the deposition temperature of 700˚C, most of the lattice mismatch-defects are trapped within first 300nm of Ge growth and good quality single crystal Ge is achieved within a layer thickness of approximately 1 µm on window sizes up to hundreds of µm^2. For p$^+$n junction fabrication, a sequence of pure-Ga and then pure-B depositions are utilized for the ultrashallow p-doping of As-doped Ge-islands. The I-V characterization of the diodes confirms the good quality of the Ge and ideality factors of ~ 1.1 with low saturation currents are reliably achieved.**

Index Terms— **chemical vapor deposition, Ge, Si, Epitaxy**

I. Introduction

Ge has always been interesting for its high mobility, low energy bandgap and for the match of its lattice constant with some of the III-V semiconductors such as GaAs. Nowadays, Ge is widely applied in infrared (IR) optoelectronics, as an epitaxy substrate for III-V multijunction solar cells, for SiGe alloying in state-of-the-art CMOS technology, in radiation-hard materials for the fabrication of nuclear-radiation detectors, and it is playing a major role in high performance fiber-optic systems [1]. All these applications of Ge together with its compatibility with Si CMOS technology and low price compared to III-V materials, have led to the development of numerous approaches to merging Ge and Si, most of which are based on Ge epitaxial growth on Si substrates [2,3,4]. However, for all these methods the 4.2% lattice mismatch between Ge and Si still presents a challenge for obtaining Ge-on-Si epitaxial growth that is not ridden with high densities of threading dislocations and poor surface roughness.

Many recent studies have aimed at overcoming the lattice-mismatch problem and some reports of good quality Ge-on-Si have appeared for approaches such as those using SiGe buffer layers [5,6], lateral overgrowth [7] and aspect ratio trapping (ART) by growth in high aspect ratio trenches [8,9]. However, Ge epitaxial growth on SiGe buffer layers that can be as thick as a micron or so, still results in some degree of dislocations degrading the quality of the Ge [10], and the lateral overgrowth and ART techniques developed up until now are dependent on critical nanoscale patterning and selective growth over window sizes in the 100 nm range.

In contrast, the method presented in this paper, while being based on selective Ge growth in windows to a Si substrate, allows defect-free filling with c-Ge in tens-of-microns large window sizes. Moreover, the transition region from Si to Ge is kept below 300 nm in thickness. The epitaxy is performed in a standard ASM Epsilon 2000 chemical-vapor-deposition (CVD) reactor for Si/SiGe deposition. For the further processing of the Ge-islands, we have made use of the fact the available system was recently modified for merging GaAs and Si epitaxial growth in one reactor, thus allowing the integration of good-quality crystalline intrinsic/doped layers of GaAs, Ge and Si, all in one system [11].

The quality of Ge epitaxy on Si is investigated by scanning electron-microscopy (SEM) and cross-section transmission electron-microscopy (TEM) analysis, not only of the Ge-islands themselves but also of GaAs deposited on the Ge, in the same growth cycle. It is shown that the inter-diffusion of Ge and Si at the interface at a deposition temperature of 700˚C leads to a sub-300-nm transition with a low threading dislocation density and single crystal Ge epitaxial growth is achieved within a thickness of less than 1µm.

The doping of the Ge is studied for Ga, B and As precursors. A novel processing procedure was developed for the fabrication of p+n Ge diodes, where the p+ region is created by a sequence of pure-Ga and pure-B depositions. Unlike the Si case, where pure-B depositions can be used to create high-quality ultrashallow p+n diodes [12], the exposure to diborane (B_2H_6) will not create the necessary p-doping on the Ge surface. This function can, however, be achieved by exposure to trimethylgallium (TMGa), while the subsequent growth of a B-layer, which is chemically resilient in many ways [13], can facilitate a reliable aluminum contacting of the junction.

The I-V characterization of the fabricated p+n diodes gives a clear confirmation that the quality of the Ge-grown by this method is excellent. The diodes characteristics are uniform over the wafer and have low series resistance, as well as exceptionally low saturation current and ideality factors.

II. Experimental Procedures

The starting material is Si (100) wafers with a resistivity of 2-5Ω-cm. An isolation layer of 300nm thermal plus 1000nm

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LPCVD SiO_2 is first formed on the wafers and the areas where Ge deposition is desired are opened by plasma etching to the Si with soft landing. Just before loading in the CVD reactor a HF dip-etch and Marangoni cleaning are performed, while in the reactor a 1-min baking step at 1100°C is used in order to ensure that the surface is free of native oxide. Then 2% diluted GeH_4 gas is lead into the reactor chamber at a pressure of 20Torr, as the precursor gas for Ge growth. Growth temperatures from 550˚C to 700˚C were found to render good selectivity to the exposed Si surface with only very few Ge nuclei growing on oxide masking regions.

For n-doping of the Ge epitaxy, 0.7% AsH_3 is utilized. Taking advantage of the dilution system of the reactor, AsH_3 is further diluted to allow a wider doping range while the minimum background doping of AsH_3 at the desired deposition temperature of 700˚C is observed to be 10^{18}atoms/cm^3. For p-doping, TMGa and B_2H_6 are used. Both these precursors have in the past been shown to dope the Si surface [12,14]. For Ga this was most effective at a temperature of 400˚C and the same conditions have been applied here to create a surface p-doping of the Ge. On the other hand, exposure of Ge to B_2H_6 does not effectively dope the surface even at 700˚C which is normally used for Si B-layer diodes. However, after doping with Ga, exposure to B_2H_6 will create a thin B-layer on the surface at temperature of 700˚C. The presence of the B-layer has two advantages: before metallization, in this case sputtered aluminum, it protects the surface against oxidation, and after metallization it protects against Al-spiking in the Ge that could otherwise short-circuit the junction.

In Fig.1 a schematic cross-section is shown of the fabricated Ge p^+n junction. In one deposition cycle, first around a 1-µm-thick n-Ge layer is grown at 700˚C on the exposed n-type (100) Si substrate. Then pure-Ga is deposited to form the shallow p-doping and finally a Pure-B layer of almost 3nm in thickness is deposited on the Ge. The term “PureGaB” is introduced for this combination of pure Ga/B depositions. Wafers are then loaded immediately into a sputter coater for a 675 nm Al/1%Si deposition. Also the backside of the wafer is coated with Al for contacting of the n-substrate. The Al on the front of the wafer is then patterned around the Ge-deposited windows. The quality of the diodes obtained with and without this deposition, is evaluated by electrical measurement of the I-V characteristics.

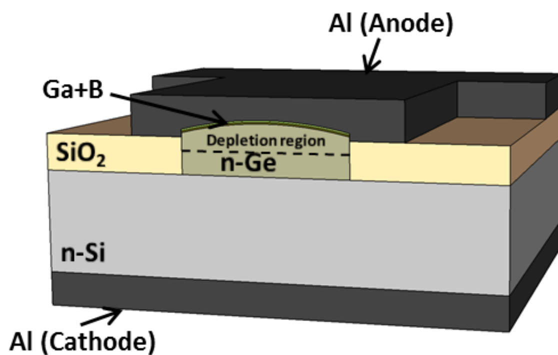


Figure 1. Schematic cross-section of the fabricated Ge p^+n diode.

III. Results and Discussion

In Fig.2 TEM pictures are shown of selective Ge epitaxy grown on patterned Si at deposition temperature of 700˚C and covered with a top layer of GaAs. At 700˚C a smooth and defect free surface of Ge is obtained after only growing a thickness of 1 µm. At 700˚C the Ge is dislocation-free at the interface, but numerous new dislocations are generated by the GaAs deposition. This can be due to some degree of stress built into the Ge at this higher temperature as a result of the increased diffusion of Si into Ge. The very smooth surface of the Ge grown at 700˚C is underlined by the SEM images shown in Fig.3 where the selective epitaxial growth of Ge in large windows to the Si is illustrated for sizes up to 10×20 µm^2.

To investigate the in-situ As and B doping concentrations of the Ge, SIMS analysis was performed. For this purpose, alternating layers of As and B doped Ge were grown. The result is shown in Fig.4. Due to the solid solubility limit of As in Ge, the maximum n-doping achieved is 2×10^{19}atoms/cm^3. The background As doping of the reactor for nominal intrinsic Ge growth at 700˚C is 10^{18}atoms/cm^3. At 700˚C, As tends to segregate at the surface, giving rise in As doping density at the Ge surface as compared to the bulk values. Moreover, it is concluded that at 700˚C, As doping does not affect the growth rate while it is decreased significantly, depending on the AsH_3 flux, at lower temperatures. Also the SIMS analysis of the Ge-island composition, as shown in Fig.4, shows that in a region of about 300nm from the interface there is a substantial inter-diffusion of Si and Ge. This is no doubt the effect that helps to keep the dislocation defects from propagating out of this very limited transition region.

Significantly high B-concentration levels can be introduced at the Ge surface by deposition of a thin layer of pure-B at 700˚C. However, while this procedure gives excellent doping results on Si surfaces [12], it appears that the much lower solid solubility of B in Ge as compared to Si, still prevents any substantial p-doping. In spite of this, the formation of a B-layer has a beneficial effect since it acts as a protection layer against oxidation of the Ge surface and also prevents Al-spiking during the metallization process.

In contrast to the B depositions, pure-Ga depositions do create a substantial p+-doping of the Ge surface. However, to obtain reliable diode characteristics, it was necessary to cap the Ga layer with a protective B-layer when Al was used as metallization. The resulting I-V diode characteristics are shown in Fig.5a for three different geometries of 1×1µm^2, 20×1µm^2 and 40×40µm^2. The ideality factors are low, from 1.1 to 1.2. Also a low reverse current of less than 10pA is found in all cases and the series resistance is as low as can be attained when measuring through the whole substrate. These excellent diode characteristics are measured over the whole wafer as it is shown in Fig.5.b for the diode size of 40×40µm^2. The observed spread is considered particularly low because no special attempts were made to passivate the Ge to SiO_2 interface at the diode perimeter.

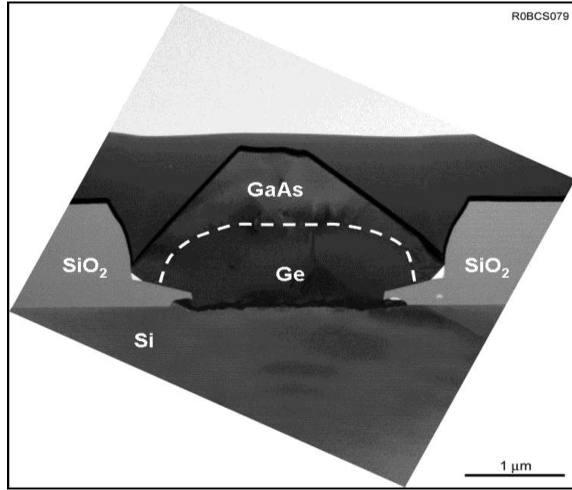


Figure 2. Cross-sectional TEM images of selective Ge epitaxy grown on pattened Si followed by in-situ growth of a GaAs layer at temperatures of (a) 550˚C and (b) 700˚C in line-shaped window sizes with a width of 2µm.

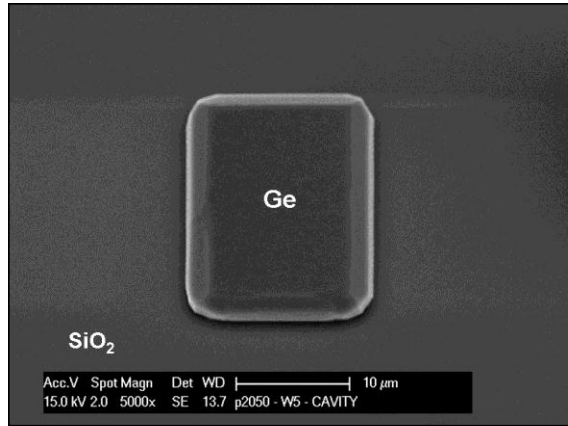


Figure 3. SEM images of c-Ge grown in large-area windows to Si.

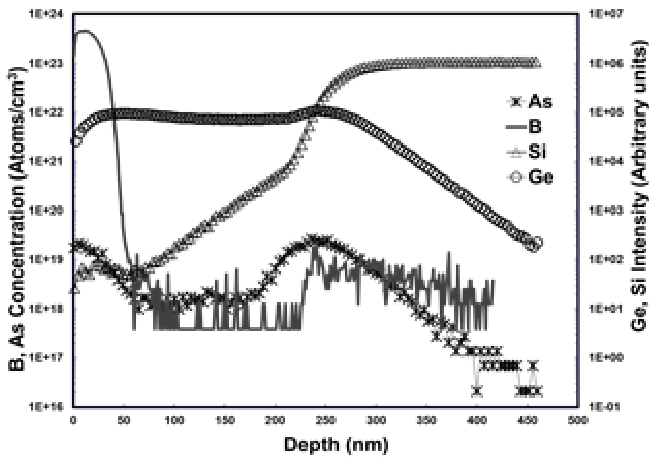
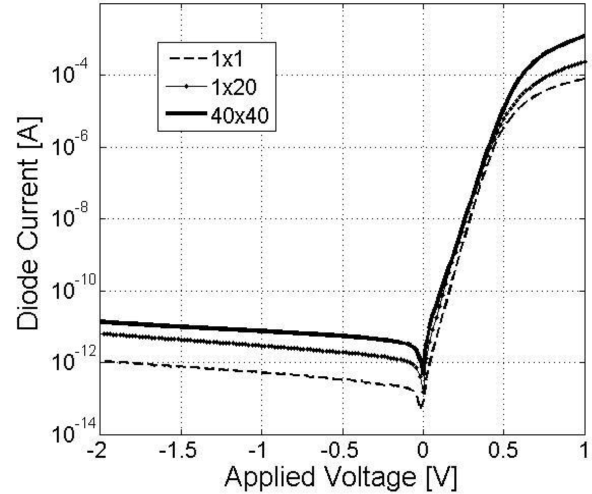
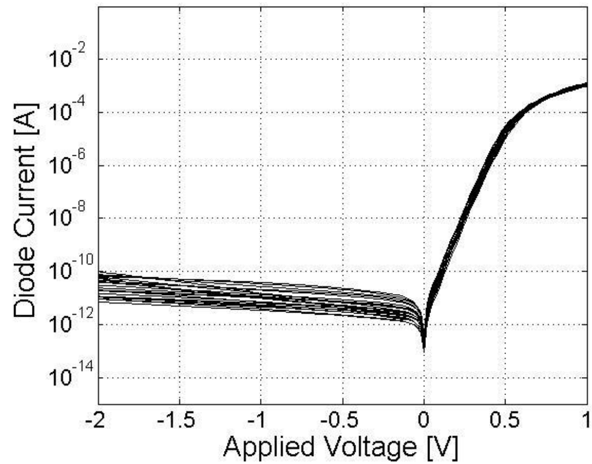


Figure 4. SIMS profiles of As- and B-doped Ge-on-Si for deposition temperatures of (a) 550˚C and (b) 700˚C.



(a)



(b)

Figure 5. I-V characteristics of Ge p^+n diodes with ultrashallow p^+-doping realized by a sequence of Ga and B depositions for (a) three different geometries of $1\times1\mu m^2$, $20\times1\mu m^2$ and $40\times40\mu m^2$ on one die and (b) over the wafer for $40\times40\ \mu m^2$ diodes.

IV. Conclusion

In a standard CVD reactor, Ge selective epitaxial growth on patterned Si substrates was developed with a transition region of less than 300 nm and smooth, flat and defect-free surfaces of Ge achieved at a deposition temperature of 700˚C.

For the fabrication of p^+n Ge diodes, all doping is achieved in-situ by As-doping during the Ge growth and then p^+-doping from a pure-Ga deposition followed by a pure-B deposition to form a barrier layer to the Al-metallization. To our knowledge the resulting I-V characteristics have uniquely low values of reverse current, series resistance and ideality factors as well as good uniformity over the wafer. The lack of extra processing to isolate of the p^+-region as well as the quite planar surface after Ge-growth make this an attractive and straightforward add-on to standard Si technology.

Acknowledgment

The authors gratefully acknowledge the processing support of the DIMES-ICP group, the technical support of ASMI, and the financial support of the SmartMix Memphis project.

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