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A CMOS Image Sensor with Thermal Sensing Capability and Column Zoom ADCs

Shuang Xie and Albert Theuwissen, Fellow, *IEEE*

Abstract—This paper presents a CMOS image sensor (CIS) with a zoom ADC, to quantize in-pixel temperature sensors, as well as for faster readout speed of the image pixels while maintaining low quantization noise. The proposed 15 bit zoom ADC has a 4 bit Unit Capacitor Array (UCA) SAR and a 13 bit incremental 2nd-order delta-sigma ADC (DSADC), as its first and second stage, respectively. The proposed UCA with improved switching and decoding technique minimizes capacitor area and switching energy, by 50 % and 75 %, respectively, compared to a conventional binary weight array (BWA) counterpart. Measurement results on 4 chips show the proposed zoom ADC could operate at least twice as fast, when maintaining the same signal-to-noise ratio (SNR), or improve its SNR by 9 dB, when maintaining its sampling speed, compared to a DSADC only alternative. The proposed 15 bit ADC is measured a SNR of 80.1 dB and INL and DNL within ± 1.5 LSB and ± 1 LSB (full scale voltage is 1 V_{p-p}), when operating at 31 kHz. The incorporated imager-based temperature sensors are measured to have inaccuracies within ± 0.6 °C on 4 chips, between -20 and 80 °C, when quantized by the same zoom ADC.

Index Terms—zoom ADC, CMOS image sensor, temperature sensor, delta-sigma ADC, SAR ADC

I. INTRODUCTION

FOR thermal sensing using existing imager sensor pixels, column-level delta sigma ADCs have been employed [1], as they are known for its compact area, low power consumption and low noise advantages [2]–[5]. They suppress temporal noise and provide fine resolution and high dynamic range with less accurate analog blocks, by oversampling as well as by noise shaping. Temporal noise is reduced to 2.4 e⁻ rms and to 3.5 e⁻ rms in [2] and [3], respectively. Their low noise levels make it possible to achieve higher dynamic range, e.g., 73 dB in [2] and 84 dB in [3]. In addition, they are combined with a SAR ADC for faster readout and low noise operating in [4]. Reference [5] proposes a low power 10 bit 20 MHz delta-sigma ADCs using an inverter based opamp for its delta-sigma modulator. SAR has been proposed to assist the delta-sigma ADC in its loop [6]; however, for DC-input ADCs, it is more energy and time

efficient to locate the SAR outside instead of inside the delta-sigma modulator [6]–[8], e.g., a zoom ADC. In contrast to the aforementioned publications [1]–[8], this paper has the following features: (1) Using a 4 bit UCA SAR to assist an incremental 2nd order 13 bit DSADC, it achieves 9 dB better SNR while maintaining the conversion speed, or twice sampling rate while keeping its SNR; in other words, a higher dynamic range, compared to a DSADC only counterpart, being experimentally verified. (2) The UCA SAR consumes 50 % less area and 75 % less power compared to a 4 bit BWA alternative. Considering its power and area efficiency, it is a good candidate as a low resolution first stage sub-ADC. (3) The zoom ADC is also employed to quantize an imager based sensor, intended for dark current compensation. In addition, compared to our previous publication in [1], the advantage of this work is a faster readout speed and a wide dynamic range, especially for quantizing the image pixel outputs. This paper is an extension of our work (only simulation results) presented at [9], with added measurement results. The temperature sensors have inaccuracies within ± 0.6 °C from 4 chips, when measured in a temperature range between -20 and 80 °C.

This paper is organized as follows. Section II explains the operating principles of the proposed zoom ADC, whose experimental results are shown in Section III. Section IV shows the measurement results of the CIS, including those of the temperature sensors, as well as the dark current measurements and compensation using thermal information from the imager based temperature sensors. Section V concludes this work.

II. ZOOM ADC

A. UCA SAR

Fig. 1 shows a UCA SAR's schematic: each time a bit switches, a voltage of $\pm VREF \cdot Cu / 2C_{total}$ ($\approx \pm VREF / 16$ if omitting the parasitic capacitance) is added or subtracted from the charge balancing node V_x , depending on the logic value of B_i (1 or 0), where Cu and C_{total} are the unit capacitor and the total capacitance weight in the ADC, respectively; $VCM = VREF / 2$. On one hand, during each switching, the charge balancing node V_x steps up or down by a voltage less than that in a BWA. However, in the conventional UCA as described in [10], V_x keeps switching up and down even after it comes close to the level of VCM , within a voltage of $\Delta = VREF / 2^N$, and this incurs unnecessary switching energy. show opposite signs, when V_x can be approximated to VCM , within errors of $\pm \Delta$.

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The proposed timing diagram in this paper is shown in Fig. 1, where the comparator and the following bits stop comparing or switching after two neighboring bits have opposite signs. The proposed switching method provides 4 bits instead of 3 bits as in [10], when using the same number of capacitors. In other words, the capacitor area is saved by 50 % for the same number of bits, compared to [10] or a conventional BWA. The reasons are in addition to positive and negative steps, there is a third switching mode of the capacitors—non-switching. In other words, as each time a bit switches, a voltage of $\pm V_{REF}/16$ is added or subtracted from V_x , making the its number of bits 4 instead of 3. If the positive and the negative steps generate digital output 1 and 0, respectively, the non-switching mode is analogous to a 0.5, and this helps double the number of ADC stairs and gains an extra bit. However, the thermometer to binary encoder, which is comparable to that for a delay-line based time to digital converter (TDC) [11], is still of 3-bit complexity, with an extra Most Significant Bit (MSB).

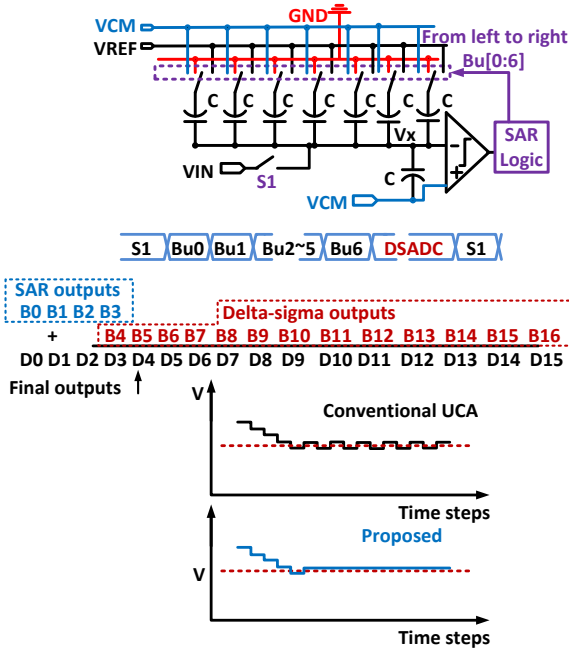


Fig. 1 Proposed UCA SAR ADC and its timing diagram.

Using the proposed UCA method, the switching energy dissipated by the capacitor array is saved, particularly around the middle of the input range— V_{CM} , where, in contrast, is the most energy-hungry region for the other two conventional techniques, as illustrated in Fig. 2. The reasons are that in the proposed method, the closer an input voltage is to the V_{CM} , the fewer the UCA SAR's active cycles are, before the comparator and the capacitors idle. The total number of capacitors in the proposed design is only half as much as those in [2] or in a conventional BWA. In this way, the switching energy is further reduced, by at least 75%, compared to a conventional BWA alternative. In this design, the averaged operating cycles of the comparator for a ramp voltage input is 4, which is the same as that in a BWA SAR. Moreover, most of the time the comparator output is monotonous, being static at "0" or "1". According to the simulation results in this technology, a non-switching step

consumes around 15 % energy as in a switching one. Assuming the leakage current in the comparator is negligible during its idling, the proposed 4-bit UCA also saves the total comparator energy by around 50 %. The UCA based SAR has more conversion cycles than a conventional alternative. However, the total conversion time of a 4-bit UCA SAR in this design is much less than 1 of the 16 or 128 cycles of the delta-sigma in the zoom ADC.

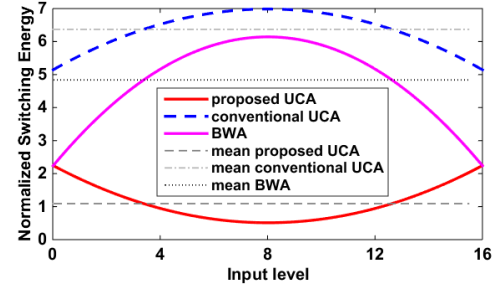


Fig. 2 MATLAB simulations of energy dissipation in a 4-bit capacitor array using BWA, conventional UCA [10] and proposed UCA method of the same unit capacitor size.

B. SAR assisted delta-sigma ADC

The proposed SAR-assisted 2nd-order incremental delta-sigma ADC (zoom ADC) is shown in Fig. 3, with the delta-sigma ADC in reference to [12]. Its opamp is a folded-cascode one. It should be noted that the DAC (capacitor) array shown in Fig. 3 is a different one from the UCA SAR shown in Fig. 1. It places the SAR-assisted DAC voltage at the position of that of the conventional common mode voltage. Once the comparison for all the 4 bits are complete in the SAR, whose outputs are employed to configure the capacitor array connected to $VDAC_SAR$ shown in Fig. 3, the conversion in the delta-sigma ADC begins. The charge sampled on $C11$ ($=C_{total}$, which is the sum of all the eight unit capacitors in Fig. 1) during phase 2 is approximately $(V_{IN}-VDAC_SAR) \cdot C_{total} \approx (V_{CM}-V_x) \cdot C_{total}$ (C_{total} and V_x are the total capacitance and final V_x value of the SAR and $C_{total} = C11$). This is mathematically similar to using a multi-bit quantizer in the delta-sigma loop. However, the fact that the input level does not change over a temperature/image sensor's conversion period makes it possible to move the SAR outside the delta-sigma loop. This act of moving the SAR outside the loop makes the conversion time of the UCA trivial compared to that of the whole zoom ADC, as the UCA SAR works sequentially with the DSADC. Using a 4-bit SAR, the input charge sampled ($V_{IN}-VDAC_SAR$) is suppressed by a factor of 8 (losing 1 bit for the digital error correction shown in Fig. 1). In other words, the input range of the delta-sigma modulator is reduced to its original 1/8, in theory. Meantime, the requirements of the output swing (in the opamp) in the delta-sigma modulator can also be reduced to its original 1/8. The capacitor size of $C12$ and $C22$ can be reduced accordingly.

The SAR DAC shown in Fig. 3 is physically a separate DAC from that in the SAR circuit shown in Fig. 1. Considering the mismatches between the two DACs, the reference voltage range of the delta-sigma ADC is designed to be at least twice larger than the resolution of the UCA SAR, to make sure it covers that of ($V_{IN}-VDAC_SAR$). $C11$ corresponds to the eight unit

capacitors (C) shown in Fig. 1.

As shown in the bottom figure of Fig. 3, rather than being a real voltage, $VDAC_SAR$ is an equivalent average voltage formed by the top plate voltages from the eight unit capacitors that comprise $C11$. At phase 2, the top plates of all the eight unit capacitors ($C11$) are connected to the fixed voltages ($VREF$, VCM , or GND). For this reason, $VDAC_SAR$ are not affected more by the switch charge injection, compared to a conventional design.

III. CIRCUIT IMPLEMENTATIONS AND MEASUREMENT RESULTS OF THE ZOOM ADC

Fabricated using $0.18\ \mu\text{m}$ CIS technology, a micrograph of the zoom ADC and the pixel array on the prototype chip are shown in Fig. 4 (a) and Fig. 4 (b), respectively. Each UCA SAR occupies an active area of $80\ \mu\text{m} \times 200\ \mu\text{m}$, while each delta-sigma ADC takes $35\ \mu\text{m} \times 600\ \mu\text{m}$. The CIS pixel pitch is $11\ \mu\text{m} \times 11\ \mu\text{m}$ (not shown). With a power supply voltage of $3.3\ \text{V}$, the zoom ADC consumes $140\ \mu\text{W}$ of power. The $3.3\ \text{V}$ voltage supply is to accommodate the pixel output voltage level. The UCA takes about 40 % of the total area, with less than 1 % additional power consumption, since according to the timing diagram shown in Fig. 1 and Fig. 3, its operation is in a sequence with that of the DSADC. It should be noted that the UCA has the potential for a more compact layout, and to be fitted into the pixel pitch, e.g., to layout the UCA to be narrower but a little bit longer.

The noise considerations are as follows. The opamp $A1$ is of folded-cascode architecture. Its input pair is sized $32\ \mu\text{m}/0.5\ \mu\text{m}$, whose g_m is simulated to be $384\ \mu\text{A}/\text{V}$, which corresponds to an input referred thermal noise spectral of $8\ \text{nV}/\sqrt{\text{Hz}}$. This is when the g_m of the pMOS and the nMOS common source devices in the output stage are $390\ \mu\text{A}/\text{V}$ and $105\ \mu\text{A}/\text{V}$, respectively in simulations. Taking into consideration the $1/f$ (flicker) noise, the integrated noise of $A1$ is simulated to be less than $15\ \mu\text{V}$, up to $300\ \text{kHz}$. The opamp $A2$ is sized to be $1/4$ of $A1$ and according to [12], $A2$'s noise is suppressed by the gain of the first stage ($A1$) and is hence negligible.

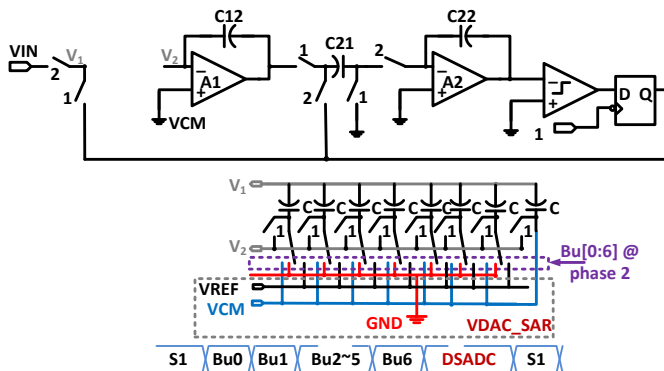


Fig. 3 Schematic of proposed 2nd order delta-sigma ADC for the zoom ADC. The DAC array is a different one from the UCA SAR shown in Fig. 1.

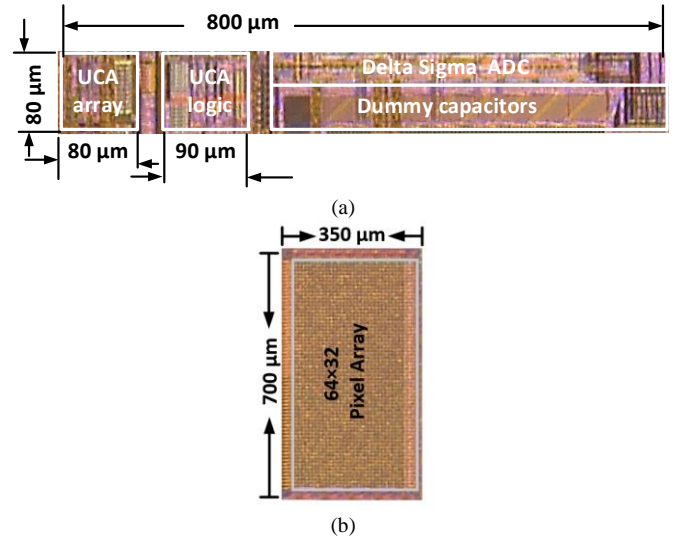


Fig. 4 Micrograph of the chip, with (a) each block (UCA, UCA logic, delta-sigma ADC, etc.) labelled, with its dimension and (b) the pixel array.

A. UCA SAR

The unit capacitor size and value are $4.5\ \mu\text{m} \times 5\ \mu\text{m}$ and $24.59\ \text{fF}$, respectively, in the UCA SAR shown in Fig. 1. It is a MIM (metal-insulator-metal) capacitor. The UCA is tested independently, using a ramp input between $0.75\ \text{V}$ and $1.65\ \text{V}$, and its digital outputs are shown in the top graph of Fig. 5. The residue voltages to be quantized by the following delta-sigma ADC is calculated and plotted in the bottom graph of Fig. 5. It should be noted that in practice due to the parasitic capacitance at the charge balancing node V_x (Fig. 1), the actual bit weight in the ADC becomes smaller and hence the residue voltage becomes larger. Accordingly, the quantization range of the SAR is also scaled by a factor with the value of the V_x 's parasitic capacitance.

The 4 bit UCA SAR has reasonable performances, with a measured ENOB around 4.1 (from its measured SNR) and INL less than $0.1\ \text{LSB}$. Similar to that in a pipelined ADC, the errors from the first stage UCA SAR ADC can be tolerated, as long as it does not cause any voltage overflow to the second stage. However, mismatches in the DAC array shown in Fig. 3 will add to those of the whole ADC. The solution to the aforementioned problem is to calibrate the bit weight of the DAC array, as follows. Firstly, the UCA SAR ADC/DAC is measured with either a sine wave or a ramp input. Secondly, the UCA SAR's transfer function as that shown in Fig. 5 is figured out and stored. Thirdly, the calibrated capacitor weights are applied to generate the final zoom ADC outputs.

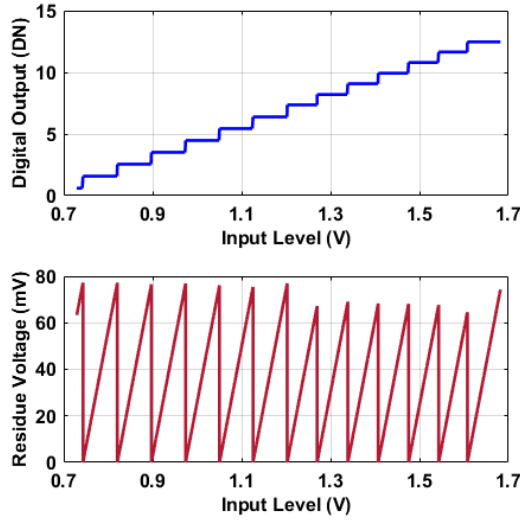


Fig. 5 The measured digital outputs (top) and the calculated corresponding residue voltages (bottom) using $V_{IN}-VDAC_SAR$. $VDAC_SAR$ for the bottom figure is calculated using the digital outputs shown in the top figure and the capacitor weight.

B. Zoom ADC

The first opamp $A1$ shown in Fig. 3 has a gain and a UBW of 65 dB and 40 MHz, respectively, in simulation, when loaded with a capacitor of 400 fF. The second opamp $A2$ has a similar gain but its UBW is a quarter as much as in the first one. For flexibility, the decimator filters for the zoom ADC shown in Fig. 3 are implemented off-chip, using two cascade 5.5 bit (max bit weight=64), rather than a 13 bit (max bit weight=128) cascade integrator as that in [2]. Their design considerations are to further suppress high frequency noise.

The zoom ADC is tested with an input signal of 800 mVp-p (-3 dB of full scale voltage, which is 1V), 349 Hz sine wave, generated by an Agilent 3220A function generator. The reference voltage range of the SAR ADC is 1 Vp-p (0.7 V and 1.7 V) and that of the zoom ADC is 200 mVp-p. The digital outputs are captured by Labview. Fig. 6 and Fig. 7 show the measured DNL and INL, and the Faster Fourier Transform (FFT) plot of the 13 bit zoom ADC (on chip #1), indicating an INL within ± 1.5 LSB and a SNR of 80 dB, when operating at an oversampling ratio (OSR) of 128 and a sampling rate of 2 MHz.

To get a better idea of the process variability, four chips have been measured and compared to a DSADC only alternative, which has the identical schematic and was measured with the same test setup as the one employed in the zoom ADC. Their measurement results are shown in Fig. 8, which indicates that by introducing a UCA based SAR to assist our delta-sigma ADC, its operating speed can be twice as fast while maintaining its resolution (SNR). Otherwise, without any increase in speed, it gains at least an additional 9 dB in SNR. In other words, the UCA SAR assists the delta-sigma ADC to extend its dynamic range, by 9 dB. The trade-off is less than 1 % additional power incurred by the UCA SAR, which only operates for less than 1/128 of the entire ADC period.

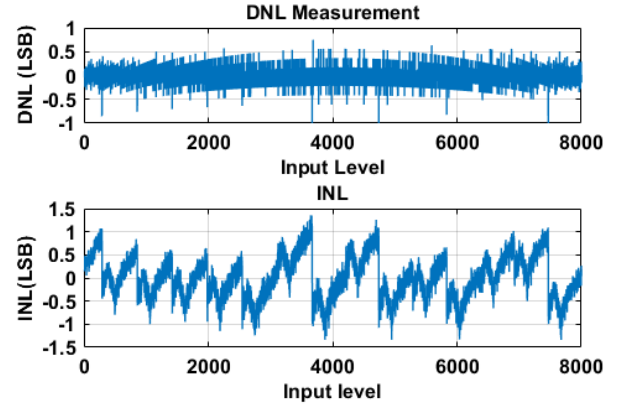


Fig. 6 Measured DNL (top) and INL (bottom) of the zoom ADC, when OSR=128 and sampling at 2 MHz. Its full scale voltage is 1 Vp-p.

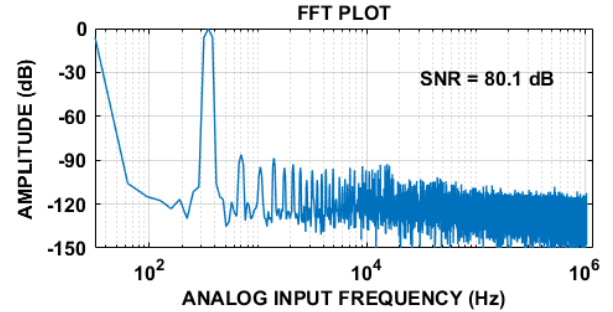


Fig. 7 Measured FFT plot the zoom ADC, when OSR=128 and sampling at 2 MHz, indicating a SNR of 80.1 dB. Its full scale voltage is 1 Vp-p.

IV. CIRCUIT IMPLEMENTATIONS AND MEASUREMENT RESULTS OF THE CIS

A. Temperature Sensor: Circuit Implementation

The proposed temperature sensors are based on image pixels [1] shown in Fig. 9. When the row select switch (RS) is on, the pixel output voltage $V_{PIX} = V_{PIX_SUP} - V_{GS}$ (V_{GS} is the gate-source voltage of M_{SF}), when ignoring the voltage drop on M_{RS} . TG has to be turned off to avoid light induced charge disturbance into V_{FD} , when the pixel is reconfigured for thermal sensing. When biased in subthreshold region and with ratiometric currents, the differential voltages between sequential outputs of an nMOS transistor, has an I-V characteristic [1][13] of:

$$\Delta V_{GS} = \frac{nkT}{q} \ln(N) \quad (1)$$

which is proportional to the absolute temperature T ; where N is the ratiometric current ratio, which is 4 in this design and ensured by the dynamic element matching circuits. k is the Boltzman constant; q is electron charge while n is a process dependent factor.

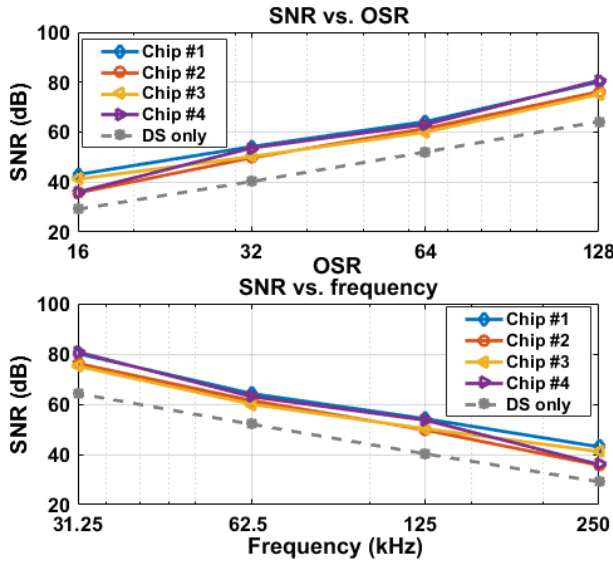


Fig. 8 Measured SNR versus OSR (top) and SNR versus sampling rate (bottom), for 4 chips, and compared to a DSADC only “DS only” alternative. The frequency is the sampling frequency f_s divided by the OSR.

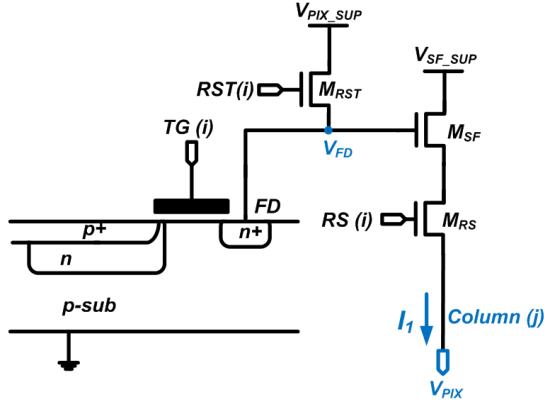


Fig. 9 Schematic of a 4T PPD image pixel. All the transistors are nMOS.

B. Temperature Sensors: Measurement results

The temperature sensors are built from one column of image pixels, which are all selected as one larger area SF. They are quantized by the proposed zoom ADC. A detailed description of the operating of the imager (source follower, SF) based temperature sensor front-ends can be found in [1]. Fig. 10 shows the measured outputs from 4 chips and their errors, between -20 and 80 °C. Each temperature sensor is calibrated as follows. First of all, the sensor digital outputs measured over the temperature range are captured and stored in MATLAB. Secondly, each temperature sensor's outputs are trimmed to certain values, at two temperature points, e.g., -10 °C and 60 °C, by assigning a gain and an offset correction factors to the each sensor's measured outputs. This process is called “two-point calibration”. Finally, a 2nd order global curve fitting is applied to all the sensors' outputs, after the two-point calibrations are performed to each sensor. The “two-point calibration” procedures are further explained as follows. For example, at -10 °C and 60 °C, each temperature sensor' outputs are trimmed to 3000 DN (Digital Numbers) and 4000 DN, respectively. To realize this, a gain g and an offset off factor are applied to its

outputs so that the trimmed outputs $c(T)$ become $c(T)=g \cdot d(T)+off$, where $d(T)$ is the untrimmed (uncalibrated) outputs and T is the temperature. Each temperature sensor has a different gain g and offset off correction factor, to compensate for its process variations. The above “two-point calibration” procedures are off-chip (post-processing). The measured temperature T is calculated using each sensor's calibrated outputs $c(T)$ and the 2nd order master curve fit, which is obtained using the trimmed temperature sensor outputs (upon the aforementioned two-point calibration) and the reference temperature sensor (PT100, of an accuracy of 20 mK)'s measured temperature. It can be observed from Fig. 10 that the measured outputs change by 600 DN (digital numbers), over 100 °C, indicating a resolution of 0.16 °C /DN). The 15.5 bit ADC has a resolution of 21 μ V (with an input range of 1 V, 21 μ V=1 V/2^{15.5}). Meantime, considering the thermal coefficient of approximately 130 μ V/ °C (when $N=4$ in equation (1)), the calculated thermal sensing resolution is also around 0.16 °C (=21 μ V /130 μ V/ °C).

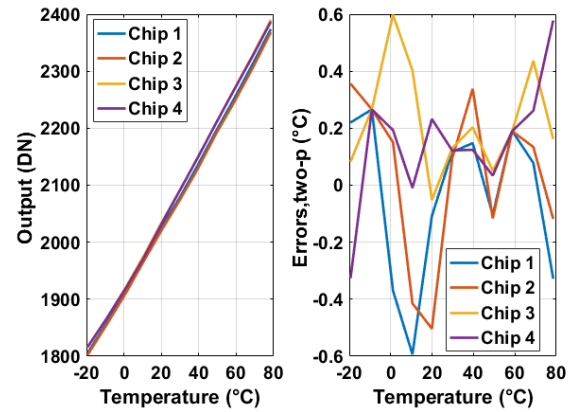


Fig. 10 Measurement results of the temperature sensors (left) and their errors (right), from 4 chips, when quantized by the zoom ADC, from -20 to 80 °C. Each temperature sensor is calibrated at two points, -10 and 60 °C, respectively, followed by a 2nd order master curve fitting for all the sensors.

C. Image Sensor

The image pixel column is quantized by the zoom ADC. Firstly, the dark current of the column has been measured between 30 and 80 °C, as shown in Fig. 11 (a). Secondly, an exponential fit $y=a \cdot \exp(b \cdot T)$ (where a and b are constants, and y is the dark current's fit while T is the temperature) has been extracted from the measured dark current versus temperature, which was obtained in the first step. Thirdly, the errors between the measured dark current and the estimation are shown in Fig. 11 (b). The estimation is based on the exponential fit $y=a \cdot \exp(b \cdot T)$ obtained from the previous step and the temperature provided by the in-pixel temperature sensors. It can be seen that the dark current's temperature dependency can be predicted and compensated by up to 90 %, using the temperature information provided by the in-pixel temperature sensors, which have been measured in Section B. The explanations for larger estimation errors at lower temperatures (e.g., 30 °C) are the increased noise (including dark shot noise, thermal noise, etc.), relative to the average dark current. However, it is more helpful to predict and compensate dark current at higher temperatures, where the dark

Table I A summary of performances of the proposed zoom ADC, compared to the state-of-the-art CIS ADCs

	This work	[1]	[3]	[4]	[5]
Process	0.18 μm	0.13 μm	0.35 μm	90 nm	0.18 μm
Column ADC speed	31 kHz	200 kHz	40 kHz	125 kHz	156 kHz
ADC bits	15.5	13	15	10	10
ADC ENOB ^b	13	N/A	N/A	10.5	9.3
Power consumption	140 μW	40 μW	122 μW	437 μW	29.5 μW
FOM ^a (pJ/conv)	0.55	N/A	N/A	2.4	0.3

^aFOM= $P/2^{\text{ENOB}}/f$, where P and f are the power consumption and the sampling frequency of the ADC, ^bENOB = (SNR-1.76)/6.02

Table II A summary of performances of the proposed imager based temperature sensor, compared to the state-of-the-art works

	This work	[14]	[15]	[17]	[16]
Sensor Type	MOS	MOS	MOS	MOS	MOS
CMOS Technology	0.18 μm	65 nm	0.18 μm	28 nm	0.18 μm
Area (μm^2)	No additional area	4000	220000	1000	89000
Temperature Range ($^{\circ}\text{C}$)	0 to 100	0 to 100	-20 to 80	-5 to 85	-20 to 80
3 σ accuracy ($^{\circ}\text{C}$)	± 1.4	± 2.3	± 0.76	-3.3/1.9	± 1
Power Consumption (μW)	144	154	0.57	56	0.8
Conversion time (ms)	0.032	0.022	8	0.036	800
Resolution ($^{\circ}\text{C}$)	0.16	0.3	0.09	0.76	0.09
Resolution FOM (pJ·K ²) ^a	117	304.9	36.9	1.2	5.3
RELIA (%) ^b	2.8	4.6	1.6	5.8	2

^a Energy/Conversion \times (Resolution)², in reference to [18]

^b 3 σ accuracy / temperature range, in reference to [18]

currents are much higher.

The reasons that the dark current is measured from 30 $^{\circ}\text{C}$, instead from a lower temperature (e.g., -20 $^{\circ}\text{C}$), are as follows. Firstly, according to our measurement results shown in Fig. 11, the average dark current doubles for almost every 6 $^{\circ}\text{C}$. As a result, the interests for dark current prediction are mostly with higher temperatures where the dark current levels are higher. Secondly, in Fig. 11, the dark current measured at 30 $^{\circ}\text{C}$ is 30 e^-/s . At 500 ms, this dark current translates to 15 e^- . If the input referred temporal noise is 0.5 e^-_{rms} (a state-of-the-art level), the temporal noise takes up around 3 % of the total measured average dark current. At 20 $^{\circ}\text{C}$, the average dark can be approximated to be around 4 e^-/s and the input temporal does not reduce proportionally (to the dark current) and equals approximately 12 % of the dark current. As the temperature drops, the ratio of the temporal noise versus the average dark current increases exponentially. As a result, if one still predicts

the dark current using the exponential fit shown in Fig. 11, the estimation errors will increase (e.g., to approximately 50 % at 10 $^{\circ}\text{C}$). Fortunately, as mentioned in the first point, the motivations to predict dark current are mostly with temperatures higher than room temperature.

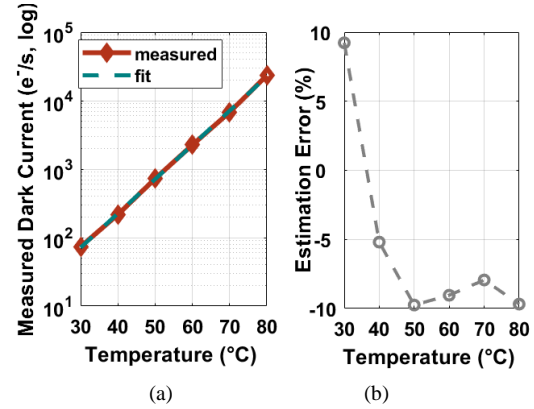


Fig. 11 Measured dark current (a) and the errors (b) between the measured and the exponential fit $y=a\cdot\exp(b\cdot T)$.

V. CONCLUSIONS

A zoom ADC has been proposed in this paper, intended to be used as a column ADC in CISs with thermal sensing features. It is able to quantize imager based temperature sensors, resulting in a measured inaccuracy within ± 0.6 $^{\circ}\text{C}$. The dark current's temperature dependency in the CIS can be compensated by 90 %, in experiments, using the thermal information provided by the in-pixel temperature sensors. In addition, the zoom ADC has been measured to achieve 9 dB better SNR within the same conversion time, or at a twice faster sampling frequency while maintaining its SNR, compared to a DSADC only alternative. Specifically, it has a measured SNR of 80 dB, when sampling at 31 kHz. In addition, The UCA SAR that assists the zoom ADC, has 50 % less area and 75 % less power, compared to a 4 bit BWA alternative and is hence proven a good candidate as a low resolution first stage sub-ADC. Although it takes around 40 % of the total area at this moment, its size has the potential to be minimized, using place and route digital logics and more compact layout of the capacitor array. Its power consumption is less than 1 % of the whole zoom ADC. Table I has compared the proposed zoom ADC with other CISs' delta-sigma ADCs in literature. Table II shows a summary of the performances of the imager-based temperature sensor, when quantized by the proposed zoom ADC. The future plan is to increase the pixel count of the CIS using column-level zoom ADCs with an optimized layout of the UCA SAR.

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