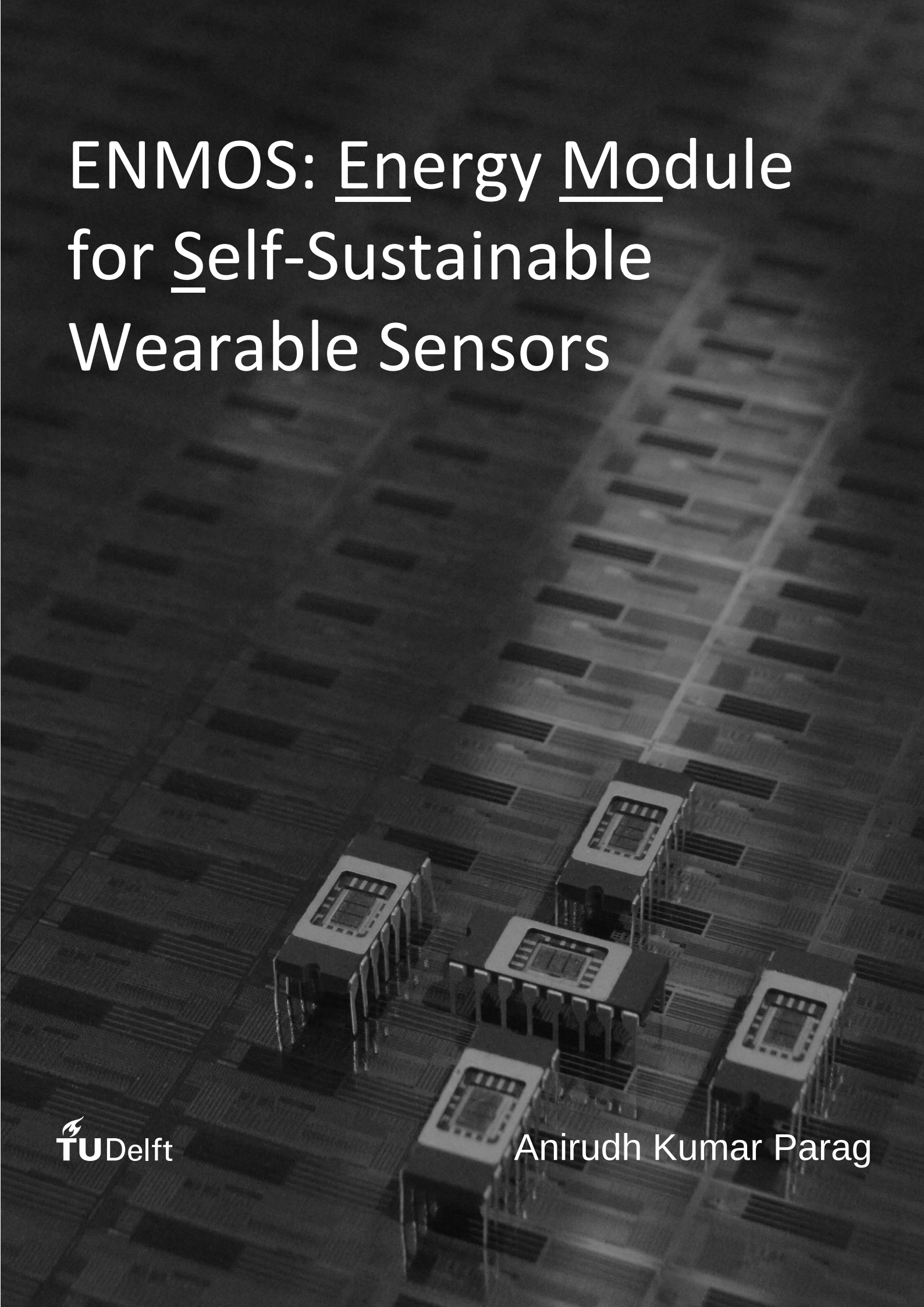
ENMOS: Energy Module for Self-Sustainable Wearable Sensors



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ENMOS: Energy Module for Self-Sustainable Wearable Sensors

By

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Preface

असंयतात्मना योगो दुष्प्राप इति मे मतिः |
वश्यात्मना तु यतता शक्योऽवाप्तुमुपायतः ||

asaṅyatātmanā yogo duṣhprāpa iti me matiḥ
vaśhyātmanā tu yatatā śhakyo 'vāptum upāyataḥ

This is the essence of the journey I have been through here at the Bioelectronics group and the TU Delft as well. This Sanskrit shlok (song) from the epic Bhagavad-Gita (an Indian historical sacred scripture), in essence means, in order to achieve perfection in one's trade or practise, one should strive earnestly for an unabridged mind, having a singular focus towards his/her yog or resolve.

Anirudh Kumar Parag
Delft, August 2019

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Abstract

Biomedical devices aimed at monitoring a patient's health have been investigated into for quite over a century now, presenting ground-breaking solutions that are now capable of potentially detecting almost all forms of known diseases and their possible symptoms. However, for most of these technological marvels, diagnosis comes at a cost. One of the costs being unavailability of such technologies everywhere a patient can roam around, while another being the bulkiness of such technologies that in turn renders it to be unavailable everywhere. A widely inquired into solution, for about a couple of decades now, focuses on bringing these devices closer to the patient than the other way round. A vision called tele-monitoring, that essentially is observing a patient's health through the employment of unobtrusive body-wearable biomedical devices. However, for such a futuristic vision to be a reality, the electronics aspect of these devices need to be designed quite deftly. For a patient would not want to be disturbed, every now and then, to recharge the device or to buy it all over again whenever its battery runs out. To address these practical issues, researchers have looked into energy sources on or around the body that could potentially power up such devices without the need for any external interferences, rendering it self-sustainable.

To this extent, the difference in temperature a human body has with its ambiance is quite a lucrative source of free and constant energy, which if harvested, could make the entire system self-sustainable. Thermoelectric energy harvesting for body wearable applications, thus, presents a promising prospective for designing battery-less sensors that could, theoretically speaking, facilitate this autonomy of operation for almost forever. Still, one major complication remains. A human body can only provide a temperature difference of about 0.45 K – 2 K with respect to its ambiance, which limits the thermoelectric element's output voltage to 25 mV – 50 mV. How would the sensor, then, be started-up from a completely depleted state, say, when it is used for the very first time or if the energy source intermittently falls short of providing the required energy, and the system shuts down?

Hence, this work focuses on addressing the fundamental limitation on the minimum cold start-up voltage that could be harvested from a thermoelectric element (TEG). For ultra-low DC voltages, the challenge translates to generating a timed-signal to amplify it up to a value that could be used to drive, say, a boost converter which can then start-up the entire energy module. Contemporary works have, thus, strived to accomplish this using a charge-pump-based or a transformer-based approach, which in turn imposes a limit on the minimum TEG voltage that can be harvested. The solution this work proposes is to decouple the Cold Start-up system from the TEG altogether and instead, use a piezoelectric element (PEH). This element being capable of producing a well-timed (AC) signal for free, based on human body vibrations, can potentially drive a boost converter. To this end, an IC is designed that can utilize the voltage from the PEH, amplifying it up to generate a well-controlled signal that could operate the boost converter. At the heart of this IC, is a self-reconfigurable charge pump that arranges its stages in different boosting ratios (without any complex logic or DSP) based on the input voltage, to allow for a maximum harvested power. The proposed self-reconfigurable architecture can potentially lead the charge pump to be load-variation-resistant. It achieves this by providing an almost constant voltage while increasing the power for higher load demands, at the same time maintaining a constant efficiency. Thus, the fully on-chip implementation in TSMC 0.18 um CMOS, can cold start-up the system from 25 mV of thermoelectric voltage to deliver an output voltage of 1 V at 56.5 % converter efficiency, consuming only 240.5 pW of dynamic power (simulation). The minimum Cold Start-up voltage and dynamic power were found to be 18 mV (ΔT = 0.1 K) and 231.6 pW respectively, to supply 1 V at 44 % converter efficiency. Moreover, in order to prove that the fundamental limitation on the Cold Start-up voltage has been addressed successfully, the IC was also simulated to check whether it can further be lowered. In this case, by providing a piezoelectric excitation voltage 73.3 mV_{RMS} higher, the Cold Start-up voltage was found to be reduced to 15 mV to supply a constant 1 V at the load. It was also found that increasing the inductor value in this case, can also allow the energy module to support even lower Cold Start-up voltages.

Acknowledgements

In here, I would like to express my gratitude to all the people who have played an important part in this thesis as well as my life over the course of time this thesis progressed.

First and foremost, I am grateful to my guru, Prof. Wouter A. Serdijn, who accepted my idea with great enthusiasm and have been a constant pillar of motivation to me in all the difficulties I have faced during this work. Scolding me at the right times and steering the course of my endeavour in the right direction each time I faltered, without ever telling me a single straightforward answer, this charismatic guy has inspired me to one day follow in the path he has so guided me upon (and possibly one day surpass him as well). From teaching me how to look at a problem from a more fundamental perspective to literally spoon feeding me with the concepts of designing a circuit from a system-oriented point of view, he has essentially raised me in the past one year on the 18th floor to be capable of undertaking any kind of quest in the field of analog IC design. It would not be an overstatement to say whenever I look at him, I learn something new (and that happens every time!). But this also holds in personal life as well, observing him start-up the monthly movie nights, the monthly evening drinks and perform in the BELCA Band, one cannot help but learn how can a person live up to everybody's expectations and yet do well in everything.

My PhD guides, Alessandro Urso and Samprajani Rout, are the backbone for the successful completion of this work. Being a consistent support and an always-available guides, these two people have literally picked me up whenever I fell, and dragged me out whenever I sunk too deep into a problem, where even I thought of myself to be beyond rescue. If this thesis is received well, these are the guys to cheer! From helping me to look at the situation from a system level (Sampi) to a more technical level (Alessandro) to cheering me up every time I discovered something new or concluded that the discovery cannot be proven (happened a lot of times), with equal excitement and willingness to help, I can say I have come a long way into approaching problems and innovating concepts, maturely. Thank you for reviewing my work in all the time-crunch submissions I presented to you and providing me with such insightful feedback.

And now comes the awesome Bioelectronics group. Whatever happens you can always count on these guys for help, be it the presentations, technical details of circuits, intricate details of career or just fun. This is a one big family and these guys have got it all covered. Stimulating discussions about life-&-circuits with Gustavo, Kambiz, Can, Vivo, Ronaldo, Auro, Tim, Koen, Tasos and Marc (forgive me if I forgot someone) have really helped me a lot and cheered me up throughout this journey. Thank you Marion for all the administrative support, specially booking the room for my defense!

I would also like to express my regards to my parents for supporting me all throughout this journey and encouraging me every time I take on a new challenge. Usually for a person from India coming from a completely non-engineering background, it gets a bit difficult to communicate with his family about the unexplored endeavours he wishes to take in life, but not for me and not to these guys. My parents are way too cool for such considerations, exuberantly backing me up in whatever kind of unknowns I plan to explore. Here, I would also like to thank my little brother for taking care of my parents in my absence and assuring me all the time 'All is well!'.

Lastly, I would like to thank the ME House and all the people there for being like brothers to me. Every single person there - Padalia, Rautmare, Kahndelwal, Saparia, Nagarkar, Abhairaj, Khusro, Das, Yadav, Venky, Ramesh, Manchanda and all the other guys – Thanks a ton for being there!

Credits for the picture on the cover page goes to Smit Saparia's photography.

If there is one thing that this journey and TU Delft has taught me here, then that would be humility, something I could have never understood had I not come here. I am heartily grateful that I was selected to do my Master's at TU Delft.

।। हे शिव शम्भो ।।

Let's begin …

1 Introduction

Energy harvesting has evolved into a field where it now finds applicability in driving the world's energy needs from the level of a large-scale community to within an individual person's context, constituting that community. Also referred to as energy scavenging, on a fundamental note, it means extracting energy from the ambient environment, that, along with an untapped potential is virtually inexhaustive. Literature suggests various phenomenon to exercise the transduction of this energy from the form it is available in to the form it can be utilized, to perform specific activities or just stored. While such phenomenon might stir interest and entice a researcher into exploring them, it may be of essence to identify a particular application, before one gets too clogged up in unnecessary nitty-gritty details.

Over the past couple of decades, in the domain of tele-monitoring, researchers have identified a fertile field of energy-autonomous sensors. Such sensors have the capability to derive their energy needs locally from the surroundings, without having to be stuck with a limited-energy supply source such as a pre-charged battery. Often touted as a rising domain in itself, a major demand towards such investigation arises from the fact that wireless sensor nodes can be used to monitor a variety of conditions, for which the deployment can range from on-the-skin to on-the-organ of a human body. Thus, depending on the specific use-case, it might not be feasible to cater to the needs of battery recharge or replacement every now and then, since it gets depleted. One of the leading research works in this field focuses on utilizing the temperature difference between the human body and the ambiance and as such, is based on thermoelectric energy sources to obtain a reliable, (almost) constant supply of DC voltage, throughout its operation period.

Thermoelectric energy sources are well suited for applications concerning temperature gradients, however small, and can theoretically power a given sensor forever, i.e. if mechanical fatigue and wear-out are omitted. But the caveat in using such energy sources lies in the phrase 'however small'. Smaller the temperature difference, smaller is the output voltage as well as the power that can be harnessed from such a source. An obvious remark could be to use a circuit to boost-up the DC voltage and design the succeeding circuits such that they can be operated on a minimum power budget. While, a remark like that may be welcomed as a suggestion and circuit techniques might be looked into, to implement such a system, a major concern still remains at large.

How to power these circuits such that they could do the magic they have been designed for and the sensor works dutifully, especially in the beginning when the sensor is devoid of any power to even start-up the boosting circuit?

This is a classic problem referred to as the 'Cold Start-up'. Standing up to its name, it has fancied the attention of researchers for quite over a decade now. Here one may be forced to wonder, if such a problem can be solved at all. Well, there are approaches proposed in the literature that are worth appreciating, but when compared to the progression of the state-of-the-art in this area that is long past its scientific curiosity phase, it has been rather slow with not many elegant solutions to report a much awaited significant improvement in the cold start-up voltages.

1.1. Energy Harvesting: A Walk through the Clock

It may come as a surprize that mankind has already been up to date with such an eccentric idea since Bronze age. One could argue that it all began with the invention of sails, when wind energy began to be harvested for sailing across the Mediterranean region 5500 years earlier [1]. Moreover, the fact that wind energy was actually harvested in windmill arrangements in India, 2500 years ago [1] also suggests a similar notion, although world-wide commercialization only began during the late 1970s when the wind turbine industry was setup in Denmark. At this point one may argue, that it might appear cheating to allow for such easy credits to the earlier generations when the design and wide-scale employment of such a technological marvel, that converts wind energy to electricity, only started of late. Thus, it would be worthwhile to remember that energy harvesting essentially is allowing the nature to power human invention, that could aid in its propulsion to achieve a desired consequence. Utilization of a transduction mechanism to extract energy from the ambiance in a suitable form so as to power up a given process, is only a finer, aesthetic version of the crude-&-crux definition discussed formerly. History has made it evident, time and again that mankind has always struggled with definitions while exemplifying exceptional grasp of concepts. Take for example the simple invention of small scale water-powered manoeuvring systems such as the waterwheel designed in the early 200 BC by Philon [1]. It was only later in the 19th century that the photovoltaic effect (PV) was documented by Bacquerel in 1839, with the successful implementation of PV panels, converting solar energy to electricity, starting in 1954 lead by Bell Laboratories [1], that such fine-tuned definitions of energy harvesting came into picture and intrigued researchers to look for more alternatives to address the growing energy needs of the time. Thus began the ordeal, to discover different transduction mechanisms that could be used to scavenge energy from different environmental phenomenon. Following this up with not a large time lag, came demonstrations of kinetic energy harvesters capable of converting hydro-power to electric power, in 1878 and wind turbines converting wind-power to electrical-power while being stored in a battery, in 1887 [2]. And thus, it may be justified to argue that a field of opportunities, with plenty to cultivate and ample to harvest, opened up.

A careful glance over the many illustrious works and powerful inventions proposed in this field over the last century may easily reveal that most of the efforts from the research community had been towards the large-scale generation and consumption of the harvested energy to satisfy the ever-growing energy needs of the population that proliferates by the minute. It was only during the last few decades that the scientific curiosity shifted towards accommodating an emerging need for energy-autonomous sensor systems in its research prospective. Due to scientific advancements and the recognition conferred upon the growing demand for wireless sensor networks, the field of micro-energy harvesting experienced a major boost-up. A major research question during those times transpired as how would one ensure the availability of energy to drive the wireless sensor nodes in remote areas, and locations abundant with such nodes? One demands strenuous efforts while the other incurs cost.

Consequently, over the last couple of decades this curiosity progressed and developed towards having a more engineering orientation. And eventually, an array of solutions were brought about and presented onto a designers bench [3] to pave way for the development of energy-autonomous sensor systems for micro-scale operations. One of the earliest works on this sprouting topic was reported in 1984 [4]. Researchers from the University of Saarland, Germany identified the breathing movement of thorax as a potential energy source and implanted a PVDF (Polyvinylidene fluoride) based piezoelectric film on the middle ribs at the lateral thorax of a mongrel dog, to obtain a power output of 17uW and proposed to enable an implantable sensor. Following this up in the wearable domain, researchers at the MIT Media Labs in 1998 [5] proposed to generate electrical power by parasitically scavenging the walking movements of a human body. They implemented the idea with a couple different transduction mechanisms including an electromagnetic sensor (magnetic rotor generator) and piezoelectric sensors (PVDF film & PZT unimorph strip) and concluded with a comparison that favoured the latter for shoe-wearable applications to power an RFID tag. It may be interesting to note that the magnetic rotor sensor extracted a peak power of 1W and the PZT unimorph extracted a peak power 80mW from those movements, that only showcases the potential such energy harvesters propose.

Would you not agree now, if a comment is made to laud the researchers whose life's mission [3] is not only to remove the cords restraining their sensors but also to forsake the need to limit its lifetime that the archaic pre-charged batteries impose?!

At this point it might be wise to ponder, why would the scholarly community want to get rid of such technology that led humanity to embark on a new journey of technological advancements, so impatiently?

A simple answer could be, because now it seems to thwart that very age of opportunities it once flourished, which would become more evident in the next section.

1.2. Case Scenario: Tele-Monitoring

Tele-monitoring [6], as literature defines it, is observing a patient's key health parameters like heart-rate, respiratory-rate, temperature, humidity, etc. remotely, without making any physical interactions, through the use of wireless telemetry via internet, Bluetooth etc. Such an approach towards patient monitoring could lead to a reliable and on the go methodology to provide point-of-care diagnostics. Moreover, it also allows the patient to remain in the cosy atmosphere of one's home without having to go through the hassles of finding a hospital room or a home attendant. The reduction in healthcare costs such a methodology enables, also makes it affordable while being convenient at the same time.

So far so good. Now we're ready to consider a case scenario representing the above notion:

Suppose a situation - A young little innocent child had to go through a traumatic accident that caused her to suffer from major injuries inflicted to her thigh bones restricting her upper-leg movements. The doctor has prescribed the child to use a wheelchair till the time her leg recovers, virtually leaving her crippled for the time being. After a couple of weeks of hospitalization the doctors have permitted her parents to take the child home but have warned them to be wary of convulsions, although rare, the kid might have to go through during days.

Owing to the adversity their kid is going through, ideally the parents would want to keep a close eye on their child's health throughout the entire time till she recovers. However, one can't always rely on ideality in the face of hostility. Due to prior engagements and work appointments scheduled prior to the sudden and unfortunate accident, the parents are left with little options but to leave their child during certain office hours.

Worry not, for these were the times a concept as unconventional and as astounding as Tele-monitoring was introduced to humanity and this thesis (above). Thus, under the umbrella of such a vivid notion, a multitude of options [7] have been made available over the years to the humankind, from which a couple of noteworthy ones (broadly speaking) are listed below:

1. Attaching health monitoring leads to patient – The little kid might have to be hooked up to a large monitoring framework consisting of a swarm of sensors around the house constantly keeping a watch over her along with a bunch of sensors attached to her body through leads and belts worn by her to monitor vitals such as body temperature, heart-rate, respiratory-rate, body posture, humidity, blood pressure, etc [7]. While such a system might be effective in having an all-round, around the clock surveillance of the child, it may not be a convenient idea for the child herself as she might want to get rid of all the wires and the restraining belts wrapped around her, once her parents are gone. A smart and holistic system like that may often be perceived as imprisoning from the patients perspective, if not the observers and in some cases may actually work against the very comfort it's designed to create.
2. Patch-Biosensor – On a fundamental note, if a patient needs to be monitored, certain key vitals are important to ascertain his/her well-being given the condition, while launching an alert in case of any abnormalities observed, to the nearby hospitals and responsible guardians. In other words, not every nitty-gritty information needs to be recorded to ensure the status of the patient. Such is the innovation proposed by VitalPatch Biosensor [8]. It is available in the form of a compact, light-weight, patch-like disposable package and comes fully equipped with integrated sensors to measure 8 physiological biometrics such as ECG, heart-rate, respiratory-rate, body posture, temperature, activity and fall detection.

In this case, the problem is the disposable zinc-air battery used in the proposed biosensor that could only last for a period of 96 hours or 4 days. What that would mean for the application is that the patient would have to change the patch biosensor every 4 days, considering a prolonged ailment. This could not only be uncomfortable to the patient but would also mean an increased expenditure on healthcare that the stellar concept of Tele-monitoring was catering to solve. Well that wouldn't be so great, isn't it?

Thus, there's an emerging need for engineering solutions that would empower such sensors to operate autonomously on a self-sustainable basis, for longer durations of time, as is required by the patient and the application. 'Self-sustainable' being a fancy term, means the sensor is capable of powering itself on its own and functioning without any external intervention, apparently, via the concept of energy harvesting.

A small detail like powering-up, in a complex and advanced system like the biosensor – designed to accomplish an array of functionalities; can raise doubts on its continuance in the longer run. Such is the significance of the concept we are now going to dive in, next.

1.3. Energy Harvesting: Candidates

Energy harvesting, as discussed earlier, in its most aesthetic forms is the transduction of energy available in the environment to the energy it is most suitable in, to power a given application, in this case, electrical energy to drive a sensor. But what is the exact transduction mechanism that should be considered, prior to inquiring further into the design of such a module?

A look into the literature reveals that the research community has been pretty enthusiastic into investigating about the various mechanisms that could advance our goal. This has been summarized in figure 1 below, that has been plotted taking into account a quarter of the works (no. of publications) and ideas propounded by the community over the last two decades, from IEEE Xplore:

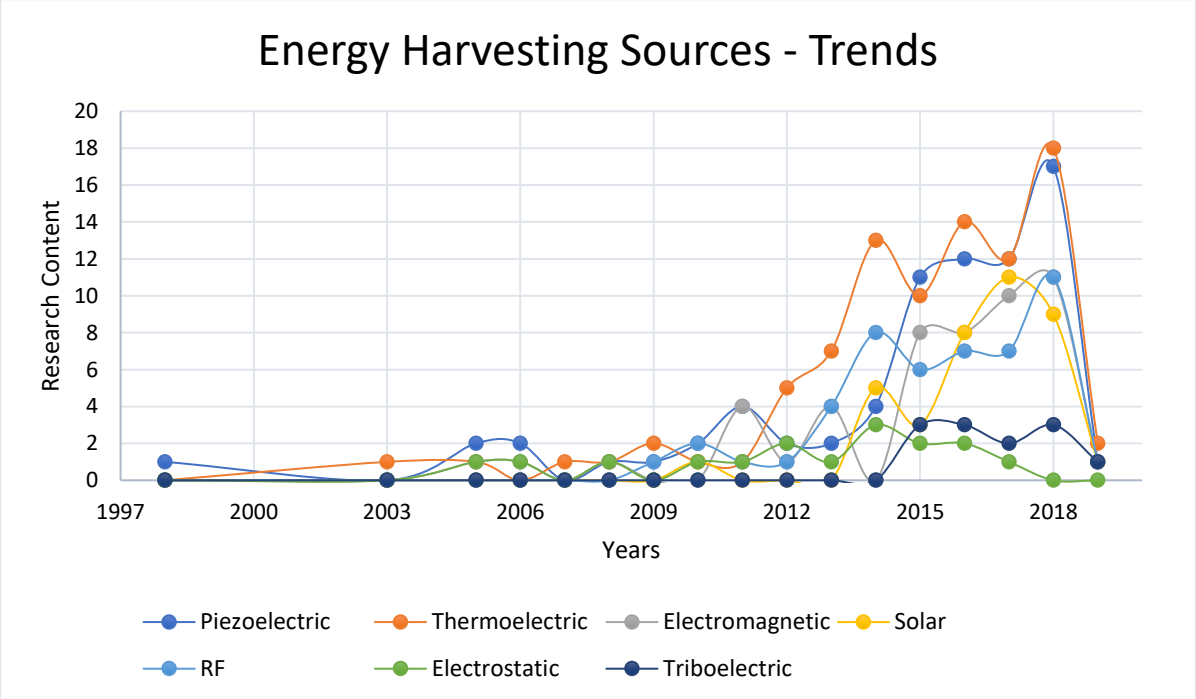


Figure 1. Energy harvesting sources – Trends over the years in the wearable domain

From the graph above, it might be worthwhile to note that, as research into the various transduction mechanisms unravelled new techniques of harvesting energy employing the same mechanism over the decades, two particular transduction techniques stand out. One has its root in the annals of human history namely the kinetic energy harvesting and the other being a more recent discovery that has gained wide-spread adulation as thermoelectric energy harvesting, over the last few years. The technique of

harvesting kinetic energy in this case is the piezoelectric effect that converts mechanical movement of a cantilever beam (in the research papers referred above) to electrical energy.

One may wonder, if it may be rational to follow the current trends and proceed with the flow of research community's fervour. Well, in that case it would be wise to at least discuss the available transduction phenomena briefly and examine their suitability with the application at hand, to guarantee not a single avenue was left unexplored while making an unbiased rationale.

Candidates, under the microscope, are elucidated below:

1.3.1. Kinetic Energy Harvesting

On a general note, any mechanical movement accompanies with itself energy, that allows the subject/object to move from one point to the other. In terms of linear movement characterized by a moving mass 'm' and velocity 'v', this energy called the Kinetic Energy (KE), is given by:

$$KE = \frac{1}{2}mv^2 \tag{1}$$

In theory, if this energy is harvested, the entire *KE* part of the equation should be available to be utilized. In practice, that is not the case, since part of the energy is lost in heat, a part is lost in overcoming the friction imposed by the medium it is in and part of the energy is lost in the actual movement of the mass. Although the last part of the previous argument may sound as a logical consequence of events, a counter argument could be, in an ideal world this energy would get transferred/extracted before the mass has any time to use the energy for itself. However, as real as the world is, practise affirms that the mass moves to cause an impact on its surroundings such that the force produced could transfer this energy from one form to the other, such as raw electric power. This impact and the method with which it is realized or performed gives rise to the various techniques of kinetic energy harvesting, as discussed below:

1.3.1.1. Piezoelectric energy harvesting:

Working on the piezoelectric effect, which broadly speaking, means the formation of an electric dipole when a strain is applied on the lattice of a crystalline material and vice-versa, these energy harvesters are an excellent source for transducing mechanical to electrical domain, without requiring any separate moving parts with respect to a given reference. However, here one needs to be cautious of the word 'broadly speaking', as it often motivates the reader to think there's only one direction the piezoelectric effect can take place. It's true, that for this effect to occur, formation of an electric dipole is a necessity. This is evidenced in the case of materials (GaAs, ZnO) having an asymmetric crystalline lattice whereby due to the shifting centre of gravity of the positive and negative charges acting under a strain, an electric dipole results [9]. Nevertheless, one should be also wary of the fact that there are materials like ceramics (PZT, $BaTiO_3$) that already have such dipoles even without the application of stress. For such ceramics, the piezoelectric effect occurs as a result of the rotation of dipoles that creates a potential difference across the lattice [9].

Although different structures, for the piezo-material under consideration, have been studied in the literature to exercise the piezoelectric effect, choice of a specific structure depends, to a great extent, on the application and the environment its being used in. For example, in the application the presented work is designed for, a cantilever beam structure is identified as suitable, by leading researchers as proposed in their respective research [2]. One possible reason could be that such a structure allows for low impact force, low acceleration and low frequency of operation to produce the required energy that could drive such applications [2] as the present one.

Also, the fact that even a small section of a piezoelectric material is capable of generating an alternating voltage when under stress, allows for small-scale miniaturization of such energy harvesting elements (EHE), which in itself is its own substantial proponent towards the cause.

1.3.1.2. Electrostatic energy harvesting:

Often a hotly debated topic on whether or not such a technique can be termed as an energy harvesting methodology, nonetheless, this technique has strived to create its own thriving niche of a research field. The principle of such a transduction technique focuses on the development of electrostatic forces

between the two charged plates of a capacitor under the action of stress. The electrostatic force being responsible for coupling the mechanical and electrical domains [10]. On a more rudimentary level, consider a charged capacitor with capacitance 'C', voltage 'V' and charge 'Q', the relationship among these quantities stands as:

$$Q = C.V \tag{2}$$

Now, if under the application of stress on the plates of this hypothetical capacitor, the plates move apart, the value of the capacitance 'C' would get affected and decrease. Assuming, the charge 'Q 'remains constant with no leakage or mechanical failure (degradation), the voltage 'V' would increase by an amount proportional to the value, capacitance 'C' goes down. This in terms of energy representation would mean:

$$EE = \frac{1}{2}QV \tag{3}$$

Thus, quite a favourable outcome results, since 'Q' remains constant and 'V' increased, the total energy content of the system rises by the same amount. While the outcome favours the mechanism to be called energy harvesting, a counter argument often raised by fellow researchers, questions the initial condition the system must be kept in, that in itself demands some energy to be stored. Well, whichever part of the court the ball may land in, one cannot deny the transduction of energy between the two domains (mechanical to electrical).

With such an EHE one may find it quite natural for it to be fabricated on a micro-scale level and designed into miniature form-factors using various micro-fabrication techniques [2]. However, there are some caveats that are still being tried to be addressed, thus forcing researchers to look for alternative means, such as low charge retention over longer periods of time, low surface charge density, and the fact that it needs to be pre-charged to be useful at all.

1.3.1.3. Electromagnetic energy harvesting:

Often touted as one of the more primordial forms of energy transduction mechanism, that has been, since the discovery of Faraday's Laws in 1831, used to convert energy existing in the forms of hydro, wind, coal or nuclear to electrical energy. However, it all transpired to be known for large-scale electricity generation. Then, what about the poor designers who were in hopes of finding a better solution for micro-energy needs of the society?

A scientific discovery is almost rendered useless if it does not fit in an engineer's little tool-box. How could it make people's life better?

Thus, a newfound interest stirred up the research community and small-scale solutions started to be revealed around the late-20th century, with the 1998 demonstration of MIT media lab's wearable shoe-based energy-harvester being one of the prominent proponents of the idea [5].

In layman's terms, this idea corresponds to the generation of electric current (AC in nature) when a magnet moves inside a coil, thus transferring the kinetic energy of the hypothetical magnet into electrical energy for the hypothetical (as well) coil. But the very employment of magnets and coils prevents such EHE from have micro-form factors. Prototypes available in literature suggest volumes from 0.1 cm^3 to 100 cm^3 with output power ranging from 1uW to 100mW respectively [10]. Also, such EHE have been communicated for delivering higher values of currents but lower values of output voltages. Micro-fabricated forms are not reported to have much larger voltages than 100mV either [10].

Therefore, with respect to the presently considered application, such micro-energy harvesters may not turn out to be a good choice owing to their volume to power/voltage ratio.

1.3.1.4. Triboelectric energy harvesting:

Originally regarded as a wasteful form of electrostatic energy, researchers prior to its discovery, ensured such effects be suppressed. The phenomena was thought for many years to have a negative effect on the performance of a material, due to dissimilar materials charging each other up when in agitative

contact. However, in 2012, the scientific community was taken by a storm when [11] published their work propounding the practicality and feasibility of such an effect to generate and use this electrostatic energy.

In plain text, when two polymer sheets with different triboelectric properties are stacked atop each other, they produce equal and opposite charges that accumulate over the two sides, under the impact of mechanical deformation that causes them to rub against each other, due to nanoscale roughness [11]. The electric dipole formed at the interface, called the triboelectric potential layer [11], also serves as a 'charge pump' to force the flow of charges towards an external load due to the change in capacitance. This variation in capacitance is ensured, by design, to occur due to a mechanical impact. An expression [11] that demonstrates the working principle is:

$$I = C \cdot \frac{\partial V}{\partial t} + V \cdot \frac{\partial C}{\partial t} \tag{4}$$

Where, 'I' is the generated current, 'V' is generated voltage (AC in nature) due to the electrostatically induced charges and 'C' is the capacitance of the triboelectric structure.

Although, high voltages have been reported in literature owing to this phenomena, not very high currents have been observed, thus keeping the output power to be in the lower range [12]. Take for example the case presented in [11] itself, a peak output voltage of 3.3V was harvested with output current of only 0.6uA and a peak power density noted to be at 10.4mW/cm^3. Works have been reported to increase the output power to about 1.5W, although the short circuit current was still very low, around 3mA at 0.8MΩ load, with the open circuit voltage at around 850V [12].

Materials employed to obtain this effect can be pure-polymer based like Kapton and Polyester (PET) [11] as well as nanocomposite based like BTO (BaTiO3) nanoparticles in a copolymer matrix—poly(vinylidenefluoride-*co*-trifluoroethylene) (P(VDF-TrFE)) [2], with latter delivering a relatively higher current.

Among the discussed Kinetic energy harvesters, a careful observation into the operation and fabrication of such EHE may reveal that one particularly stands out for the proposed application. The piezoelectric energy harvester fairs well in comparison to its sister EHE techniques due to:

a. The phenomena that allows for its working, does not demand any mechanically moving parts as in the case of electromagnetic and triboelectric energy harvesters. So wear and tear is fundamentally not an issue.
b. The phenomena as well allows for the generation of potential due to intrinsic charge arrangements and so does not necessitate any externally applied electric fields as in the case of electrostatic energy harvesters.
c. Since the phenomena can also occur in a small piece of piezo-material, its micro-fabrication is well supported but only limited by technology or material, as opposed to electrostatic and electromagnetic energy harvesters.
d. The current output of piezoelectric energy harvesters is reported to be higher than triboelectric energy harvesters [2,12], although this comparison is only based on a more practical ground than a fundamental one.

Now, coming to the point of suitability of such Kinetic EHE towards the application of wearable Tele-monitoring, one may note that the critical and elemental requirement for any of the above listed effects is an impact. Such an impact might not always be very practical to expect from a human body specially in cases where a body is in a state of rest and the vibrations are only intermittent not continuous. Also, with regards to the amplitude of vibrations and operating frequencies that can be harnessed, current-state-of-the-art kinetic energy harvesters are not specifically suited for lower amplitude sub-Hz frequency vibrations that are pretty much abundant on a human body. This one might not come as a fundamentally justified comparison but it does hold on a practical level.

1.3.2. Thermal Energy Harvesting

A more popular approach in literature for harvesting energy from the human body, thermoelectric EHE fundamentally drives its principle of operation from the Seebeck effect. Originally discovered by Seebeck

in 1822 [9], the observation related the coupling of thermal to electrical domain. Seebeck effect is the generation of potential along a given material (metal or semiconductor) when one of its ends is heated causing a temperature gradient to form along form that side. This effect is measured when two dissimilar materials (having different Seebeck coefficients) are joined together and the junctions are kept at two different temperatures, say 'T' and 'T+ΔT'. Due to the difference in temperature, an electromotive force (Seebeck Voltage) is generated between the two junctions, namely, hot and cold junction. The phrase, Seebeck coefficient, used before, refers to the difference in potential generated between the two junctions per unit difference in temperature applied two the same, for small temperature differences [9]. Thus, the Seebeck voltage can also be expressed as [13]:

$$V_S = S_{AB}.\Delta T = (S_A - S_B).(T_H - T_C) \quad (5)$$

Where, 'V_S' is Seebeck voltage (DC in nature), S_A & S_B are Seebeck coefficients of the two materials and T_H & T_C are the temperatures of the hot and the cold junctions.
A close look on the working of such EHE may reveal that better is the conduction of electrical energy, higher will be the electrical power produced, since more conduction electrons between the junctions means more current. On the same note, lower is the thermal conductivity, better is the efficiency of energy transduction, since higher thermal conductivity means sooner neutralization of the temperature difference. The efficiency is thus defined as the ability of the thermoelectric material to conduct electrical energy while impeding thermal conductivity. Another important parameter that measures the performance of a given thermoelectric EHE is called the Figure of Merit (ZT) and is defined as [2]:

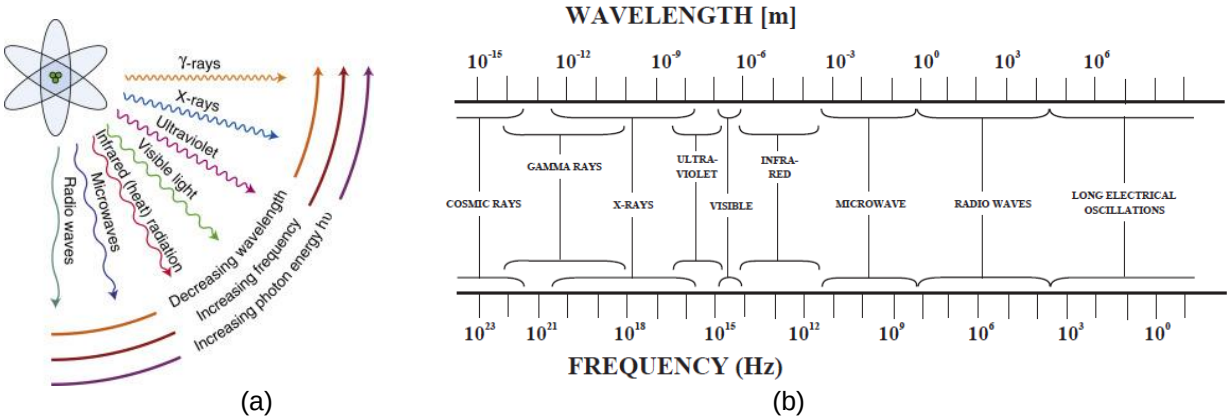
$$ZT = \frac{S^2.\lambda}{\kappa}.T \quad (6)$$

Where, 'S' is Seebeck coefficient, 'λ' is electrical conductivity, 'κ' is thermal conductivity and 'T' is temperature.
Therefore, higher is the parameter ZT, better will be the thermoelectric efficiency (of energy conversion). One of the approaches to increase ZT that has gain quite some momentum over the recent years, is to increase the phonon scattering independently to reduce the lattice contributions of thermal conductivity. This has been shown to yield ZT ≥ 2, by using nanostructured bulk thermoelectric materials [2].

Regarding the suitability of such an EHE towards the considered application, it may be worthwhile to note that the human body always maintains an almost constant temperature throughout itself, that, with regards to the ambient room temperature could easily provide a reliable & sufficient temperature difference. By employing a highly efficient (Be_2Te_3) EHE to generate energy suitable for a given sensor application, this can be taken advantage of. Moreover, with no moving parts (no maintenance), simple structure and almost 20 years of lifetime [13], these harvesters can emerge being an excellent choice.

1.3.3. Electromagnetic Radiation Energy Harvesting

Electromagnetic (EM) radiations are, as the name implies, packets of energy propagating with an alternating electric and magnetic fields. Such radiations consist of a wide range of particle-like waves / wave-like particles distinguished on the basis of frequency and wavelength, that also are responsible for their unique characteristics. Figure 2 gracefully represents this entire electromagnetic spectrum.



(a) (b)

Figure 2. The electromagnetic Radiation (a) Figurative Representation (b) Numerical Representation

Humankind since ancient times has always strived to use this abundant energy stored in these radiations. The development of sundial in 3500 BC marked one of the first attempts to use electromagnetic radiations coming from sun, although not to transform energy as such, but to give an idea about time. So, now the question arises, can we benefit from it in our case?

Visible and Infrared light waves being the most abundant forms of energy on this planet, bestowed upon us directly by the sun, proposes an important challenge and a solution for energy harvesting. In the meanwhile, radio-frequency (RF) has also got quite prolific specially in the metropolitan areas with increasing reach towards the countryside across the globe, since the advent of radio-operated cellular phones. Here, one may argue if the artificially available RF waves can be treated as a reliable source to harvest since it's not originally provided by nature. Nonetheless, such an omnipresent EM energy (now-a-days) cannot be left to waste if it has even the slightest potential to be a reliable source of energy. The other forms are not considered as they are not abundant and in some cases even harmful.

1.3.3.1. Solar energy harvesting:

Based on the photovoltaic effect, originally discovered by Becquerel in the 19th century, and the successful commercialization by Bell Laboratories (for space explorations, though) in mid-20th centuries [1], the field of solar energy harvesting has really taken a deep plunge into effecting the lives of ordinaire, over the years.

The phenomena in itself is quite intriguing (from a microelectronics point-of-view). In a p-n junction, electrons from the n-side diffuse across to the p-side and holes diffuse towards the n-side, due to electrostatic forces of attraction resulting in a free-charge depleted region called the depletion region around this junction. This diffusion and accumulation of opposite charges at the two sides of the depletion region creates a net electric field that cancels the effect of the electrostatic forces of attraction and maintains an equilibrium condition across the junction. Now, when a photon carrying just enough energy to ionize an electron from the valence band, hits the so-formed depletion region, the electron-hole pair thus released are swept towards their respective sides (holes → p-side, electrons → n-side), due to the depletion region's electric field. When such an arrangement is connected to a load, the flow of electrons create a current across it and result in a certain voltage (DC in nature) that is proportional to the photon flux [14]. Thus, the conversion of light energy into electrical energy takes place.

Parameters such as the bandgap and energy conversion efficiency are treated to be a key in determining the capability of a photovoltaic cell [2]. Bandgap being an intrinsic property of a semiconductor material, specifies the Shockley-Queisser (S-Q) limit [2]. This limit decides the maximum (theoretical) energy conversion efficiency a single-junction photo-cell can produce with each bandgap corresponding to an S-Q limit. For a bandgap of 1.34eV, the S-Q limit predicts 33.7% achievable efficiency [2]. Practical implementations have shown GaAs to have the maximum efficiency of >28% while silicon achieves 20-27%, not lagging far behind [2].

While this energy harvesting scheme is known to provide high energy densities than the previously discussed ones, it suffers on accounts that not the entire different wavelength radiation emitted by the sun can be utilized [15] and the fact that such an EHE needs to be lit-up for the energy conversion to take place. Nonetheless, such a scheme provides an interesting energy harvester that does not rely on moving mechanical parts, is reliable, has longer lifetime with low maintenance costs.

Moreover, since our application would require the user to wear the sensor module on the body and under the clothes, at a location ranging from the neck to the knee depending on the use-case, the user would find it difficult to always expose the sensor to light for it to work. Thus, this approach might not present the best suitable EHE.

1.3.3.2. RF energy harvesting:

Another abundantly available energy source due to the presence of WLAN, GSM and Radios around, RF EHE proposes to be a good prospect for wearable applications. The working principle is based on the

ability of the antenna designed for receiving the incoming RF signal to extract energy as well from the available RF waves lying around in its vicinity that it ideally would have rejected. It has been shown that the RF power density that could be harvested from a GSM base station 25m-100m apart ranges from 0.01uW/cm^2 to 0.1uW/cm^2 (around -30dBm to -20dBm) [15]. Such harvesters tend to be limited by their rectifiers and the minimum voltage, called the threshold voltage, needed by them to conduct any current [15]. The start-up power i.e., the minimum power needed by the energy harvesting unit to start its operation, thus need is given by [15]:

$$P_{start-up} = \frac{V_{rec,threshold}^2}{2.\eta_A.R_{rec}} \quad (7)$$

Where, '$V^2_{rec,threshold}$' is rectifier threshold voltage, 'η_A' is receiving antenna radiation efficiency, '$R_{rec'}$ is rectifier equivalent parallel input resistance and '$P_{start-up}$' is input power needed for the rectification and then harvester to start.
If a practical scenario is considered where $V_{rec,threshold}$ = 0.3V, R_{rec} = 1KΩ, η_A = 0.8, the $P_{start-up}$ = 56.25uW (-12.5dBm), that is quite large as compared to the power that could be extracted from such a technique as of now [15].

Thus, if not on a fundamental basis, then may be on a more practical basis, the RF energy harvesting technique may not propose a very good solution for the presently considered application. Although once such a highly sensitive rectifier is available/designed, such an EHE could be of essence in this field. Also, RF energy cannot be relied to be available wherever a patient can go about that includes remote locations and countryside areas, that poses a major challenge for this EHE scheme.

On a similar note, there are though literature one could find on reputed platforms that talk about design of antennas with sensitivities as high as -30dBm [16], here one should also keep a track of the distance between the receiver antenna and transmitter that generally is around 30cm, which is quite low for practical applications. Such antennas also happen to be quite narrowband, while in practice a range of RF can be discovered in ambiance lying to be harvested which is not quite efficient. Literature has also reported successful design and demonstration of human body based RF EH antenna with a novel voltage-threshold compensated rectifier to achieve -22.5dBm sensitivity & 1V output voltage [17]. However, the applicability was proven for narrowband applications and the distance between transmitting and receiving antenna was only about 30cm with the channel being human body and not air.

After taking in, all the popular energy harvesting techniques, under due consideration, and discussing about their working phenomena, merits and demerits, we have almost reached a conclusion about the perfect EHE that is befitting for the (previously) discussed application that represents the essence of this work. But before the winner is announced let us address some practical nuances regarding power output of state-of-the-art and summarize the results as follows:

1. Comparison of output quantities, under wearable application-specific conditions, of the state-of-the-art EHE in their respective domains is tabulated in Table I as (courtesy of [2]):

TABLE I. Quantitative comparison of state-of-the-art energy harvesting elements (EHE)

Energy Source	Working Principle	Material/Configuration	Output Voltage (V)	Output Power (mW)	Output Power Density
Solar	Photovoltaic	GaAs thin-film, single-junction cell	-	-	28.8 mW/cm^2
Triboelectric (6 kgf pushing force at 5Hz)	Triboelectric	5 wt% BTO nanoparticle–P(VDF-TrFE) nanocomposite, poled BTO and P(VDF-TrFE), contacting mode	1130	6.4	0.71 mW/cm^2
Electrostatic (750 rpm rotary)	Electrostatic (Electret)	Rotor (PMMA+PTFE) + stator (Cu+FR4)	324	10.5	0.42 mW/cm^2

Electromagnetic (vibration 2.1Hz)	Electromagnetic	Magnet suspended by springs on both sides in a vertical tube	6.5	0.432	14.16 uW/cm^3
Piezoelectric (vibration 1Hz)	Piezoelectric	Prestressed multilayer PZT diaphragms	-	11.3	10.55 mW/cm^3
Thermoelectric [18]	Seebeck	High density BiTe pellet placement	0.0501	0.176	-
RF (GSM) [15]	Far-field EM Coupling	Dipole antenna	-	-	0.1 $uW//cm^2$

2. Summary of comparison based on individual characteristic EHE and application is tabulated in Table II as:

TABLE II. Quantitative comparison of energy harvesting elements (EHE)

Domain	**Electromagnetic**		**Thermal**	**Mechanical**	
EH Technique	**Radio Frequency**	**Solar**	**Thermoelectric**	**Piezoelectric**	**Electromagnetic**
Energy Harvested	Electromagnetic radiation	Electromagnetic radiation	Temperature gradient	Mechanical vibrations	Mechanical vibrations
Working	Dedicated antenna catches RF energy floating around in its vicinity in the ISM band and converts it into electrical energy which is then AC-DC Up converted to power a sensor [15]	Solar cell converts ambient light energy into electrical energy based on the Photovoltaic effect, which may then be DC-DC Up converted to power a sensor [15]	Temperature difference across two dissimilar semiconductor devices (P-N) is exploited to convert the thermal energy to electrical energy based due to Seebeck effect, which then is DC-DC Up converted [19]	Mechanical Vibrations are converted to AC electrical potential exploiting the sensor crystal orientation based on the Piezoelectric effect, which may be AC-DC Up/Down converted [20]	Mechanical Vibrations are converted into electrical domain when a magnet moves inside a coil inducing an AC current into it, exploiting Lorentz force, which may be AC-DC Up converted to power a sensor [21]
Availability	Mostly where strong WLAN or GSM Network exists [15]	Specific to day (outdoors) or good lighting condition inside [15]	ΔT = 0.5K-2K can be found anywhere across the body anytime [19]	Continued supply of power would need persistent vibrations all time	Continued supply of power would need persistent vibrations all time
Suitability to patient care	NO (Not available everywhere a patient can go)	NO (Not available everywhere a patient can go)	**YES** (Available all the time everywhere - Reliable)	NO (Only when body moves can it be used - Erratic)	NO (Only when body moves can it be used – Erratic)

Hence, a thermoelectric energy harvesting element is reasonably justified to be the most suitable one for the scope of the entire project work.

1.4. Power Conversion: The Supply Gap

Now that the thermoelectric energy harvesting has been deemed fit for our application, lets have a look at what are the range of temperature differences that can be expected on a human body at room temperature (25˚C). This has been aptly tabulated in Table III as (courtesy of [22]):

TABLE III. Temperature difference at T_{Room} = 25˚C for human body in various states of action

Site	Rested ΔT (speed=0.2 m/s)	Walking ΔT (speed=1.56 m/s)	Running ΔT (speed=4.25 m/s)
Abdomen	1.73 K	3.80 K	4.75 K
Biceps	0.45 K	1.22 K	1.7 K
Calf-posterior	0.65 K	1.74 K	2.4 K
Chest	0.94 K	2.37 K	3.18 K
Forearm	0.44 K	1.16 K	1.63 K
Hamstring	0.91 K	2.32 K	3.14 K
Lumbar	0.85 K	2.18 K	2.96 K
Quadriceps	0.82 K	2.12 K	2.89 K
Triceps	0.78 K	2.02 K	2.75 K

As can be observed from the above Table III, not very high temperature gradients can be obtained (or expected) from the human body. The author here finds it important to state about the expectations of rather significantly larger temperature gradients that could also imply that the patient might be in a really unhealthy state, and as such, they are also not being looked forward to.

Hence, with due regards to the above observation, a suitable thermoelectric element needs to be selected that can support the application (sensor) even at ΔT=0.45 K. But before one jumps to concluding the search for the perfect thermoelectric energy generator (TEG), there's another key parameter called power output that needs attention along with the form factor of the TEG. The input power needed by different state-of-the-art implementations of sensor modules working for the intended application or in a similar domain (implantable) is tabulated in Table IV as:

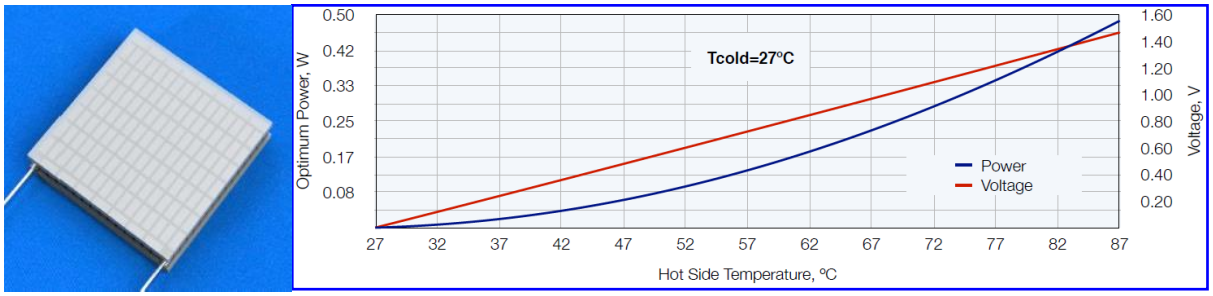
TABLE IV. Power consumption of different wearable/implantable sensor modules

Application	Component	Supply Voltage	Power Consumed	Reference
Wearable (ECG)	SiP - EHPPM SoC, NVM, FSK TX	1.5 V (max.)	5.98 uW (SoC+NVM)	[27]
Wearable (ECG)	Mixed Signal Monitor System-on-Chip	1 V	82.4 uW	[23]
Wearable (ECG)	Analog Front End	1 V	8.49 uW	[25]
Wearable (ECG)	Analog Front End - ADC	1 V	0.30 uW	[26]
Implantable (Neuromodulation)	Analog Front End	1 V	3.20 uW	[24]

Please Note: SiP – System in Package, EHPPM – Energy Harvester Platform Power Manager, NVM – Non Volatile Memory, FSK TX – Frequency Shift Keying Transmitter

From the above Table IV, it can be noted that the minimum power required to drive a system-on-chip (SoC) based sensor module [25] for the intended application should be >82.4 uW. Table IV also gives an idea about the power consumption of the individual components that can be embedded inside the SoC module with state-of-the-art implementations.

This completes the list of the key issues and specifications that needs to be considered while selecting a suitable TEG. Hence, with due respect to these parameters, the following TEG element – 1MD06-97-05TEG is selected as shown in figure 3 (courtesy of [18]):



(a) (b)

Figure 3. (a) TEG element – 1MD06-97-05TEG, (b) Voltage & Power characteristics with respect to temperature difference

The suitability of this TEG element to the proposed application is represented in the following Table V:

TABLE V. Parameters of the TEG element – 1MD06-97-05TEG

Parameter	Value
Temperature Difference ΔT	0.45 K
Voltage Output ($\mathbf{V_{TEG}}$)	25.06 mV DC
Power Extractable (Optimum Load Condition)	103.76 uW
Source Resistance ($\mathbf{R_{TEG}}$)	2.69 Ω
Volume	11.4 mm X 11.4 mm X 1.1 mm

The values of the parameters are interpolated from figure 3.(b) and the datasheet provided by the respective vendor [18].

In order to model the TEG voltage source [19], the source resistance, R_{TEG}, has to be taken into account and the entire DC voltage source is represented as shown in figure 4:

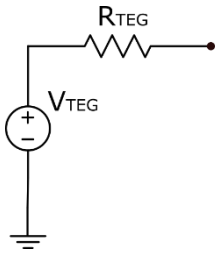


Figure 4. TEG voltage source representation

At this point, it may be worthwhile to note that although the selected TEG element qualifies to fulfil the minimum specification requirement for power output, while being a compact solution specially fit for wearable monitoring applications, it still is not capable enough to drive a sensor module as discussed in Table IV. The DC voltage output of the TEG is largely insufficient being only 25mV as compared to the mammoth required value of 1V which renders the presented solution for a self-sustainable power module, jeopardized.

One of the most sought after solution proposed by the literature to overcome this practical limitation of such a TEG element is to boost-up this small (apparently insignificant) output voltage, V_{TEG}, to the desired value.

The next section explores this very possibility and the potential solutions that could be considered:

1.5. DC-DC Boost Conversion: Fundamentally Speaking

There are many prominent approaches described in the literature for boosting a given DC voltage to higher values, while not altering the signal too much. But before we delve into discussing the intricacies

of such converters, it might be worthwhile to start at a more fundamental level and build-up our understanding up to the system level design of the said converter.

Hence, the discussion would start from selecting a primary boosting element first that could either potentially store energy in the electrical or magnetic domain (capacitor & inductor respectively) or directly up-convert the signal without any storage while simultaneously playing at both the electrical and magnetic fronts (transformer). In the below Table VI, a detailed comparison of the above said elements is provided:

TABLE VI. Comparison of potential voltage boosting elements Part I

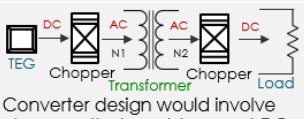
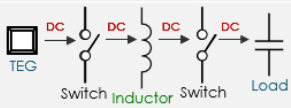
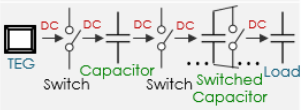
Energy Converter	Transformer	Inductor	Capacitor
Topology	Instantaneous Conversion	Time Dependent Conversion	Time Dependent Conversion
Nature	Electrical energy is transferred due to electromagnetic coupling through the core from primary (N1) to secondary (N2) winding as: $\frac{d\emptyset}{dt} = \frac{V1}{N1} \rightarrow V2 = \frac{N2.d\emptyset}{dt}$	Electrical energy from source creates voltage across coil that forces current through it building up magnetic flux & gets stored as Magnetic energy $I_L = \frac{N.\emptyset}{L}$ (Source, Quantity stored, Storage element)	Electrical energy from source creates electrical field between plates inducing charge to form a potential across the plates storing energy electrically $V_C = \frac{Q}{C}$ (Source, Quantity stored, Storage element)
Function	Voltage applied to primary (N1) winding induces magnetic flux into the core that when coupled to secondary (N2) winding produces a voltage across it as: $\frac{V1}{V2} = \frac{I2}{I1} = \frac{N1}{N2}$	Voltage across coil builds up current creating magnetic flux. Now, since voltage is constant, flux builds up, increasing current which could transfer this energy $V_L = N\frac{d\emptyset}{dt} \rightarrow V_L = L\frac{dI_L}{dt}$	Electric field b/w plates moves charges(e-) against it, causing a current, inducing charges on the plates creating voltage that can be used to transfer energy $Q = \int I_C.dt \rightarrow V_C = \frac{1}{C}\int I_C.dt$
Implementation	 Converter design would involve choppers that would convert DC-AC & AC-DC at the interface of transformer since DC could saturate(ideally not) its operation.	 Converter design would involve switches to allow the flow of energy from source to inductor to load in a controlled manner.	 Converter design would involve switches to allow flow of energy from source to capacitor to load in a controlled manner.

Table VII below lists the potential merits and demerits of using the elements described above:

TABLE VII. Comparison of potential voltage boosting elements Part II

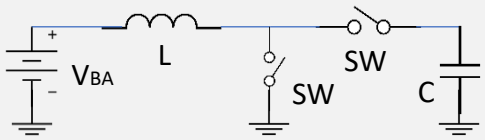
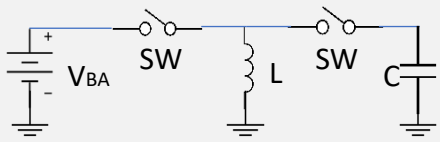
Energy Converter	Transformer	Inductor	Capacitor
Topology	Instantaneous Conversion	Time Dependent Conversion	Time Dependent Conversion
Advantages	1. Instantaneous processing 2. Voltage matching 3. Impedance matching 4. Electrical isolation	1. Energy Reservoir 2. Smoothens power flow 3. Protects circuit against high current stresses	1. Energy Reservoir 2. Smoothens power flow 3. Protects circuit against high voltage stresses
Comparison			
Topology	Instantaneous	Time Consuming Approach	Time Consuming Approach
Nature	None	None	None
Function	Requires time-varying magnetic flux	Requires additional components to deliver power, cannot work independently	Requires additional components to deliver power, cannot work independently

Implementation	1. Can only operate on AC as DC might saturate it 2. Choppers (including timing generators & switches) would consume unnecessary energy in the DC-AC & AC-DC conversion 3. Non-ideal filter to recover DC signal would result in energy loss 4. Off-Chip – Large-form factor 5. On-Chip – No options available on market, needs to be fabricated, very expensive	1. Controlling circuits (timing generators, etc) for the switches consume unnecessary energy 2. Non-ideal switches would themselves consume energy 3. Optimally, only one switch needs to be operated, even for high boosting ratios 4. High Q at high frequency 5. Off-Chip – Small-form factor 6. On-chip – low 'Q'(<10), low value (~nH), expensive [28] 7. Voltage transients not catered	1. Controlling circuits (timing generators, feedback, etc) for the switches consume unnecessary energy 2. Non-ideal switches would themselves consume energy 3. Higher the boosted voltage greater the number of stages (switches & controls) needed, higher the loss of energy 4. High Q at low frequency 5. On-Chip – Feasible 6. Current transients not catered 7. Limited current capability due to repeated charging and discharging
Preference	NO	**YES**	NO

Therefore, as has been inferred from the above two tables, Inductor turns out to be the best possible option as a primary boosting element for the DC-DC up-conversion process.

Now that the primary boosting element has been decided, converters based on the inductor's time-dependent conversion topology can be studied and compared. This is presented in Table VIII, below:

TABLE VIII. Comparison of inductor-based boost converter topologies

Topology	Boost Only Converter	Buck-Boost Converter
Function	**Cycle I**: Potential from source charges the inductor **Cycle II**: Inductor current charges load capacitor **USP**: Energy from source is never unutilized	**Cycle I**: Potential from source charges the inductor **Cycle II**: Inductor current charges load capacitor **Note**: Energy from source is left unutilized during Cycle II, being disconnected
Implementation		
Comparison		
Source Utilization	Utilized in both cycles, controls discharge rate of inductor in Cycle II not allowing it to starve delivering energy to output	Utilized only in Cycle I
Voltage Output	Positive voltage output on capacitor	Negative voltage output on capacitor
Current Ripple	Due to the inductor being present at the input side only, higher current ripples can be seen on the output side	Higher current ripples on both the output & input sides

Impedance Matching	Could be difficult if the source impedance varies (generally speaking), if load varies	Is relatively easier since source impedance is never seen by the load
Preferred	**YES**	NO

Thus, as can be observed, the Boost-Only Converter emerged as the more suitable option for the proposed power module, also since the buck conversion operation of the buck-boost converter would not be needed among other points, as discussed. This goes very well with the selected TEG element as it can only provide lower DC voltages.

1.6. The Research Challenge: 2005-2019?

Since we have explored in detail about the ingredients and the choices falling in each category from the energy source down to delivering the energy from it to the potential load, we are ready to bake our gourmet recipe for the perfect power module solution to a wearable monitoring-sensor application.

Lets have a look at the scenario as it now stands, presented in figure 5.

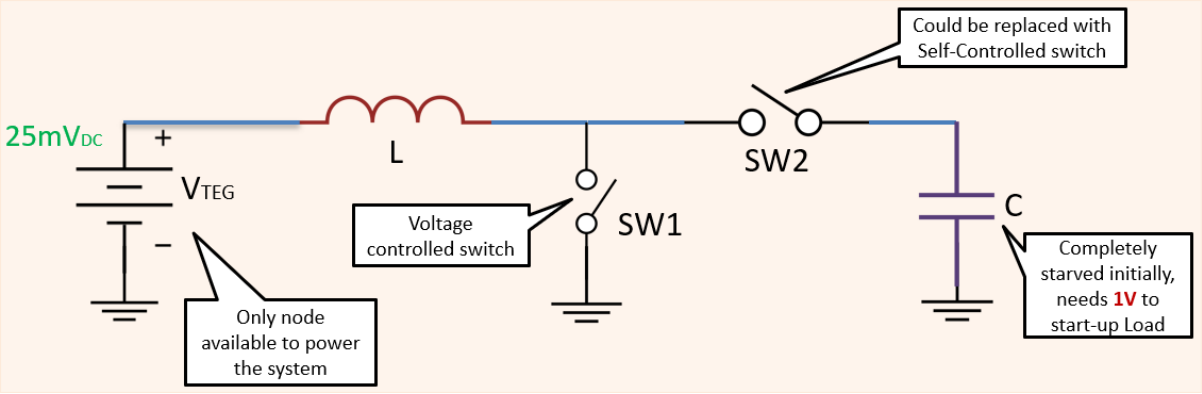


Figure 5. Power module solution for the wearable sensor depicting subtleties and caveats about different components

As can be witnessed above, there are some details that still need further attention:

a. **SW1** – This switch is responsible to charge the inductor in the first cycle by allowing a ground path and then block this very path such that the current from the inductor can flow towards the capacitor and deliver energy. Thus, this switch needs to be controlled in order to control the charging and discharging times of the inductor to appropriate a given output voltage over the capacitor. Hence, as depicted in the diagram above it has to be designed as a voltage controlled switch (VCS) (practically) and more fundamentally, a controlled switch.
b. **SW2** – This switch is responsible for connecting the inductor to the capacitor in the second cycle and preventing the capacitor to discharge to ground in the first cycle. Thus, the switch may be designed as a one-way flow device that blocks everything from the other direction. Hence, as shown in the diagram above it can be a self-controlled switch (SCS) that can only work with one direction of current flow, fundamentally and more practically be replaced with a diode.
c. **Load** – The load needs to be powered from this arrangement with a suitable voltage of 1V from the capacitor.
d. **V_{TEG}** – Thermoelectric voltage source that can only generate 25 mV from a temperature gradient of 0.45 K across it. One diligent glance and it becomes quite apparent that this voltage might turn out to be the most important caveat here. Remember the discussion about the classic 'cold start-up' problem that we originally started the chapter with? Lets phrase it in a more suitable manner:

"How could a designer approach and develop a circuit that could cold-start the operation a boosting module powered from an energy harvesting source, that could only supply a voltage of 25 mV at 104 uW of power when the temperature gradient across it is just 0.45 K?"

Given: SW1 needs a control voltage of ≥ 250mV Low-Voltage-Threshold MOS (LVTMOS) at a certain frequency to charge the energy reservoirs.

This is one of the most famous research questions engineers across the globe over a period of 15 years have been trying to solve, in this seminal field of self-sustainable sensors for wearable/implantable health monitoring applications.

1.7. Scope: Research Output Expectations

This work focuses on the design of a novel cold start-up circuit that could allow the power module of a wearable sensor to start-up from source voltages as low as 25 mV.

The focus of this research is to present the design of a power module that could allow the wearable sensor to be self-sustainable, such that it does not require its battery to be charged from an external source or more-so replaced, thus, allowing only longer periods of sensor operation.

This power module should be capable of starting itself, by means of powering the boost converter to enable the charging of the primary energy reservoir i.e., the inductor and storing a desired voltage at the secondary energy reservoir i.e., the capacitor. After the boost converter has been able to successfully deliver a certain voltage onto the capacitor, the capacitor should take control of the entire boost converter and boot-strap its voltage, increasing it to a desired output value. The 'cold start-up + boost converter' are so designed that the output values would practically be able to control, if not an entire SoC, then at least some of its major components as detailed in Table IV and [27].

The power module is proposed to be designed in a manner that makes it capable of supplying a constant voltage of 1V at the output while delivering a current of 1uA to the load. These values are so selected such that they can be treated as a representative of a more involved power module (design-wise) that would form the core of a power management solution capable of driving any load within the energy range that can be delivered by the energy harvesting source.

This 'more involved' power module is, thus, treated to lie outside the scope of this research as it would ideally involve various other functionalities such as management of harvested power and its efficient transfer to systems integrated in the wearable unit such as non-volatile memory, RF Transmitter, accelerometer sensors, temperature sensors, ECG sensors, etc., while employing different power management techniques like power gating, on-time reduction of integrated systems, parallel bus architecture, monitoring of input power, regular power alerts, reduced instruction set for communication etc. [27], to satisfy the overall power consumption needs within the set bounds.

Next On,

Chapter 2: This brief tries to examine the current cold start-up architecture proposals propounded by the research community over the years and critically review it while striving to learn from it as well. The chapter completes with the architecture level proposal of the novel cold start-up circuit.

2 Architecture

Over the past decade the research community has contributed to a variety of start-up techniques for getting the power module to deliver just the right amount of voltage at the output from ultra-low voltages produced by the thermoelectric generator (TEG). Among the start-up techniques literature proposes, four in-particular can be recognized as the broad umbrellas under which all the other cold start-up methodologies can be categorized in.

Lets begin with a brief overview of what our learned research fellows have strived to achieve over the last decade:

2.1. Start-up Technique Trends

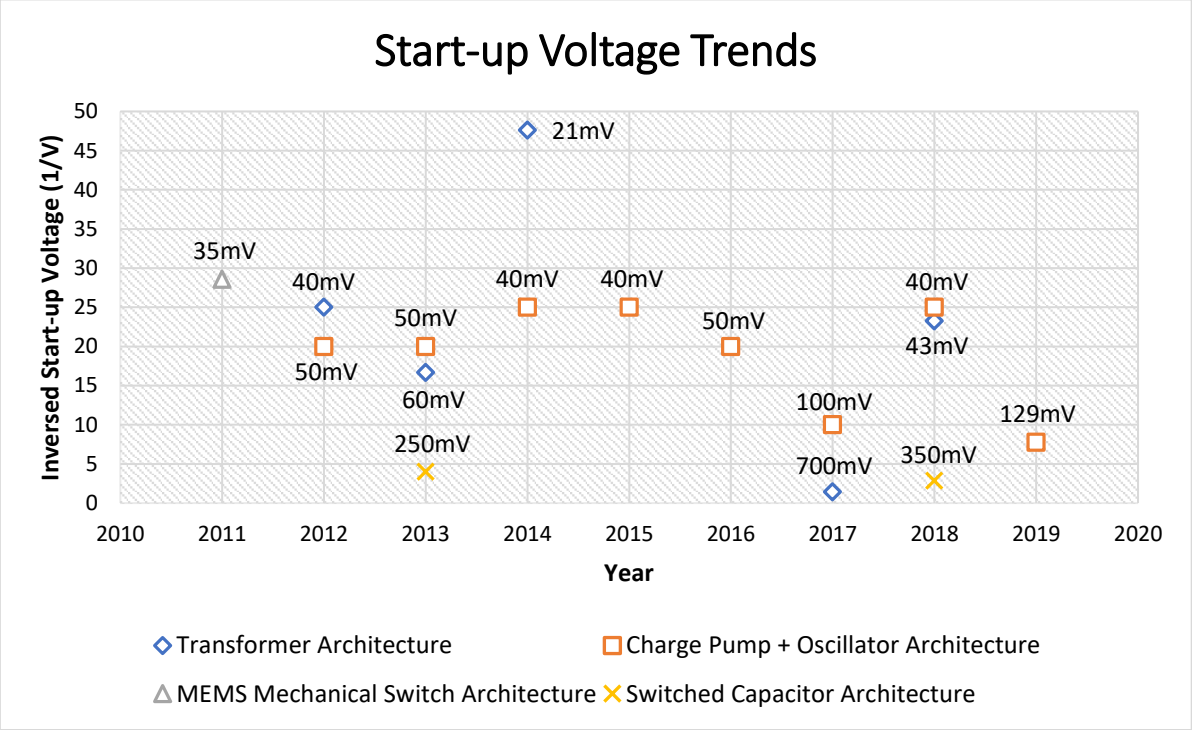


Figure 6. Start-up Voltage Trends depicting the progress of State-of-the-Art over the years

As can be observed from the figure 6 (realized for the first time in this work), showing the progression of the State-of-the-Art in terms of start-up voltages achieved over the years with respect to the four broadly categorized start-up techniques. The lowest start-up voltage achieved till this date is limited to 21 mV, and no further progress can be noted after that particular work.

The Y-axis shows the '1/V', i.e. the inverse of the start-up voltage recorded in these observations to make the plot more discernible, while the X-axis displays the years.

On a general note, steps to a successful 'cold start-up' are, to:

a. Take the voltage produced by the TEG element as an input
b. Boost-up this voltage through a transformer or a charge pump
c. Deliver the boosted voltage to a timing generator, e.g. clock generator (that can be external to the boost circuit or embedded into it)
d. Clock the voltage controlled switch of the boost converter with the required voltage to start it up

A more in-depth discussion on these techniques can be found in the following section:

2.2. Start-up Architectures

The discussion below endeavours to give an idea towards the essence of the broadly categorized start-up techniques and the limitations as has been observed (by the author) with regards to their respective architectures:

a. Transformer Based Architecture: One of the more popular architectures that is widely regarded to be a potential solution to the whole deal about the 'cold start-up' trends and an elegant approach in itself. Thus, it may not be surprizing to know that it has its own classification as:

   i. Transformer Oscillation Mode (TOM) Technique: Based upon the crux of a transformer operation, i.e., playing with voltages with respect to the turns ratio, it might come as a no-brainer. The beauty of this approach lies in the manner the chopper implementation, discussed in section 1.5 Table VI & VII, is carried out [29-30], as shown in figure 7 (courtesy of [31]).

   Using an LC resonant tank [29-30], composed of the secondary coil and a capacitor, on the secondary side positively feeding back its positive-phase voltage to the gate of a native NMOS connected to one end of the primary side, it effectively creates a timing generator that causes the transformer to repetitively boost (high turns ratio) the source voltage to reach the desired output level. This boosted voltage oscillating upon the LC resonator gets deposited onto the output capacitor during the positive-phase, when the diode is forward biased or switched 'ON'.

   On a **fundamental** note, the issue of the minimum voltage that can start-up the power module in this scenario, would thus depend on this configuration being able to achieve a positive feedback loop gain greater than unity. This, in various designs [29, 30], is addressed by selecting a minimum current, that could be conducted through the primary coil by means of the native NMOS transistor, sufficient enough to produce the required *Gm*. Also, the smallest voltage on the primary coil should be adequate enough, such that when boosted, it could turn 'ON' the diode D_1 to charge C_L. This sets the limit on the start-up voltage which could facilitate such current to be sourced by the TEG. The remaining parameters, like no. of turns etc., of the positive feedback loop gain are also adjusted to satisfy this condition and other practical considerations.

   On a **practical** note, limitations may be implicated with respect to the bulkiness of the transformer employing a high turns ratio, and values of the resistors and capacitors that can be used. Also, such a configuration has a lower efficiency [31] due to parasitic transformer losses and can only provide a limited output power.

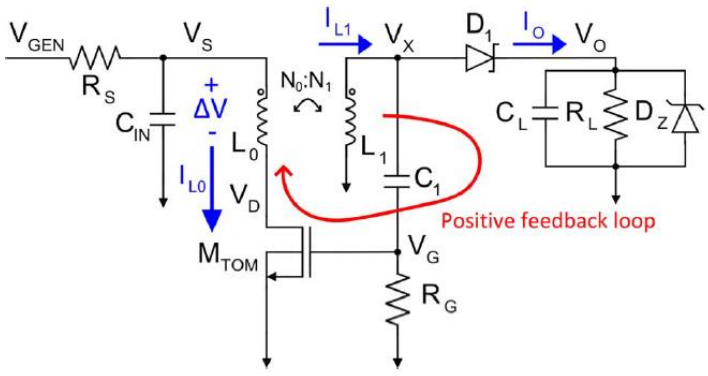


Figure 7. Transformer Oscillation Mode Technique [31]

   ii. Transformer based Boost Converter (TBC) Technique: The approach that achieved the lowest start-up voltage reported till date of 21 mV adopts an iconoclastic approach [31] to using transformers for boost-up applications. The charisma lies in the ingenuity with which all the possible steps to a successful 'cold start-up', as outlined in the previous section, are implemented.

In order to minimize the parasitics imposed by the use of a high turns ratio transformer, this methodology proposes to use a 1:1 turns ratio transformer with inversed polarity coils, as shown in figure 8 (courtesy of [31]). Instead of connecting the native NMOS M_1 with the primary coil, this approach does the opposite and connects it to the secondary coil, with the primary coil being responsible for driving it.
Application of a source voltage V_S induces a small current to flow in the primary coil effectively charging the gate capacitance of M_1 to a voltage V_G. Once a sufficient V_{GS} is applied at M_1, a corresponding current starts to grow through the secondary coil until it reaches $I_{D(sat)}$. At this point, the voltage V_X reaches to a point where it is sufficiently larger than V_S and is induced in the negative polarity onto the primary coil. This acts as a positive feedback. It charges the gate capacitor of M_1 to a negative voltage, effectively switching M_1 'OFF', while charging the primary coil to an even higher current value, due to the voltage difference across the primary coil being greater than previous time. Thus, this would effectuate a larger current flow through the secondary coil that would then charge the output capacitor to an even higher value when it forward biases (or switches 'ON') the diode D_1, once M_1 is switched 'OFF'. The secondary branch acts as a boost converter with inductor L_1 (secondary coil) being charged when M_1 is conducting, and discharged into output capacitor C_L when M_1 switches 'OFF'.

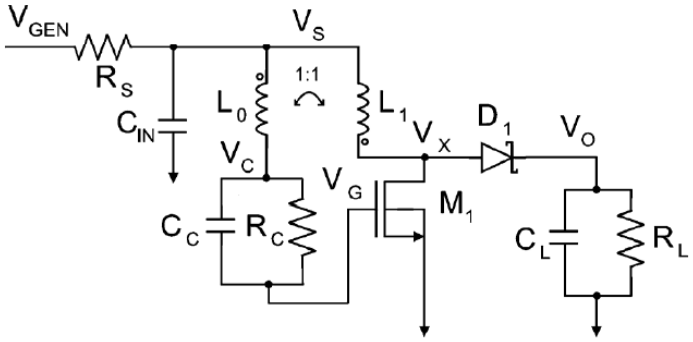


Figure 8. Transformer based Boost Converter Technique [31]

On a **fundamental** note, it may be observed that the initial current through the primary branch should be sufficient enough to charge the gate capacitance of M_1 to V_G. The value of V_G should be such that the current through the secondary coil can rise large enough to produce a voltage V_X, which when coupled to the primary coil, can lead the gate capacitance of M_1 to charge to a negative voltage, which increases the charging current of gate capacitance M_1, in the next cycle. Thus, a positive feedback can be ensured due to mutual coupling feedback property of transformer [31]. The value of the initial charging current can be noted to be of essence here, and thus can be regarded to be fundamental to the architecture. This sets the limit on the start-up voltage that facilitates the flow of current through the primary coil, sourced by the TEG.
On a **practical** note, in order to minimize the switching losses the research in [31] proposes to use high inductance values of 10 mH. Even for a 1:1 pulse transformer, this would add to the bulkiness of the entire system and may be inconvenient to integrate into a wearable patch sensor. This approach also faces challenges when it comes to maintaining the output voltage, as a result of which a Zener diode is proposed to be used at the output implying 'burn excess energy'. Ideally, if the input voltage increases the inductor charging time or 'ON' time, would need to be decreased. This could be possible if the secondary coil charging current's final value is decreased, which in turn depends on the voltage V_G. To change the voltage V_G, the gate capacitance of M_1 would need to be changed [31] continuously. This is not possible and thus, a large number of such transistors would have to be used in a parallel configuration to select between gate cap., adding to switching losses and area of the chip.

b. Charge Pump + Oscillator Architecture: As one may proceed through the intriguing approaches described previously, it might be intuitive to think why only transformers, when there is a separate class of voltage boosters tailored for these kind of purposes as well. These voltage boosters are called charge pumps and ideally, they do not require any off-chip components proposing a complete on-chip solution, that indeed can be regarded as lucrative.

Such an architecture works by supplying the available source voltage (TEG) to a timing generator, which could be a fully on-chip solution such as a ring oscillator (RO) [32] or an alternative requiring off-chip components such as an LC oscillator [33-34]. The timing generator facilitates the charge pump with clock signals that allow it's capacitors to charge and transfer the charge in an alternating fashion, thus boosting up the input voltage to a higher output voltage. This high output voltage can then be used to control the voltage controlled switch of the boost converter to charge the inductor in one phase and deliver the inductor energy to the output capacitor in the next phase.
On a **fundamental** note, to be able to drive an oscillator, be it an inverter (ring) [32] or LC based oscillator [33-34], a necessary oscillation condition has to be met. This condition generally states that there should be a positive feedback loop gain that needs to be greater than unity. In order to meet such a condition, the source, input to the said timing generator, needs to supply a positive feedback producing device (MOS-T) with a minimum voltage and current to ensure that the generator always achieves a positive feedback loop gain > 1 and starts oscillating.
On a **practical** note, it is also of essence to observe that since this timing generator drives the charge pump, it needs to output a high enough voltage that can bias the pass elements (diodes, transistors) of the charge pump sufficiently, to reduce reverse leakage currents. Also, though fundamentally high voltages are not a requirement to bias these pass elements, not having such voltages might reduce the forward to reverse bias current ratio. This could in turn not only lead to higher losses due to increased reverse current but would also force the designer to use a large number of charge pump stages [32,35,36] to achieve a given output voltage with current source capabilities.

c. MEMS based Mechanical Switch: One of the most beautiful and elegant approaches developed towards solving the 'cold start-up' roadblock was propounded by a research work in 2010 [37] by Dr. Yogesh K. Ramadass.
All that the design proposed (in this regard) was the use of a mechanically assisted cold start-up. A MEMS (micro-electro-mechanical-system) based switch that was designed to vibrate at a specific frequency when subjected to external forces due to human body motion served as the controlled switch in the boost converter. So instead of using a voltage controlled switch, as in our case, the proposal was to replace that with a mechanical switch. Since vibrations that result from a human body in motion can be abundant, also depending upon the movement, the switch can utilize that to open-up and close-in the converter circuit to charge the output capacitor and deliver enough voltage for the capacitor to take over the boosting operation by itself.
On a **fundamental** note, such a simple implementation compared to all the complex 'cold start-up' ideas as discussed previously may just be the perfect solution, except for the part where it starts to hinder the process of efficiently transferring power to the output, once 'cold start-up' has been achieved. One quick glance at the proposed architecture and it could be easily noted that the mechanical switch cannot be controlled i.e., stopped from opening and closing the converter loops (phase I & II) if there are ambient vibrations due to human motion. Thus, this random nature of the MEMS switch might decrease the efficiency of the converter, when the output capacitor has taken control over the operation of driving the voltage controlled switch, to meet power and efficiency requirements. Unnecessary charging and discharging of the inductor at random instances, at each vibration the human body produces while moving, is not ideal or desirable when source energy is of the essence.
On a **practical** note, manufacturing such MEMS switches and integrating it to the proposed circuit might come at a price which could be high enough to hinder the prospects. Also, being a mechanical device the MEMS switch would also have a limited lifetime due to mechanical wear and tear the switch may go through over its course of operation. In some cases it might happen that it had already started working without being shipped yet and the lifetime has decreased to some extent before it reaches the user.

d. Switched Capacitor Architecture: A rather bold approach. Given the fact that the boosting ratios can be as high as 40X, using a switched capacitor converter instead of a switched inductor based boost converter would not only require a large number of capacitors but also incur higher switching losses, as discussed in Table VI, VII.
On a **fundamental** note, to begin the charging process of the output capacitor and boost its voltage to a specific value, a timing generator would be required, RO in [38], to charge the switched capacitor stages and transfer these charges successively to the output stage. Pertaining to the discussion presented previously in part (b) of this section, it can already be observed that

such an approach can only allow a minimum start-up voltage, before the oscillation condition fails.
On a **practical** note, a switched capacitor approach may be attractive due to the prospects of a full on-chip implementation, but the voltage boosting ratios can only be altered by switching between the different number of stages or smartly arranging the capacitors in different boosting configurations as has been demonstrated by [38]. Such smart play of arrangements requires a dedicated processing block such as a digital signal processor (DSP), as showcased in [38], that monitors the output and the input operating conditions (V_{IN} & I_{LOAD}) to decide for a specific boosting ratio and then controls the number of stages. The processing block has its own voltage and power needs that should be satisfied before it starts operating, that in turn brings up the minimum start-up voltage the converter can achieve. Also, since achieving very high boosting ratios (40X) would only mean a large number of switching stages, [38] chose to increase the start-up voltage to 350mV instead.

2.3. Proposal: Decoupling the Problems

It may be worthwhile to note, for all the discussion we had on the different architectures propounded by the research community, one aspect or technique was particularly common, the presence of a 'positive feedback loop'. Be it to generate a timing signal to boost-up (section 2.2.a.i, 2.2.b & 2.2.d) or to boost-up the input voltage on a repetitive scale (section 2.2.a.ii), thus, again to provide timing. Thus, in a nutshell, the fundamental limitation to boosting up an input voltage to cold start-up can be described as the 'Timing Generator Problem'. This 'timing generator' has its own requirements to function properly and thus, sets a limitation on the minimum start-up voltage (& current) to satisfy its hunger. So, for as long as this positive feedback loop (to generate timing) would need to be fed from the TEG, there will always be a question on the minimum start-up voltage with regards to TEG and the ordeal to how much lower can a system go.

But what if that was not the case? What if this fundamental limitation imposed on the TEG can be broken?

Before we move into the nitty-gritty details of the above question, lets have a look at figure 9 that sums up this entire argument.

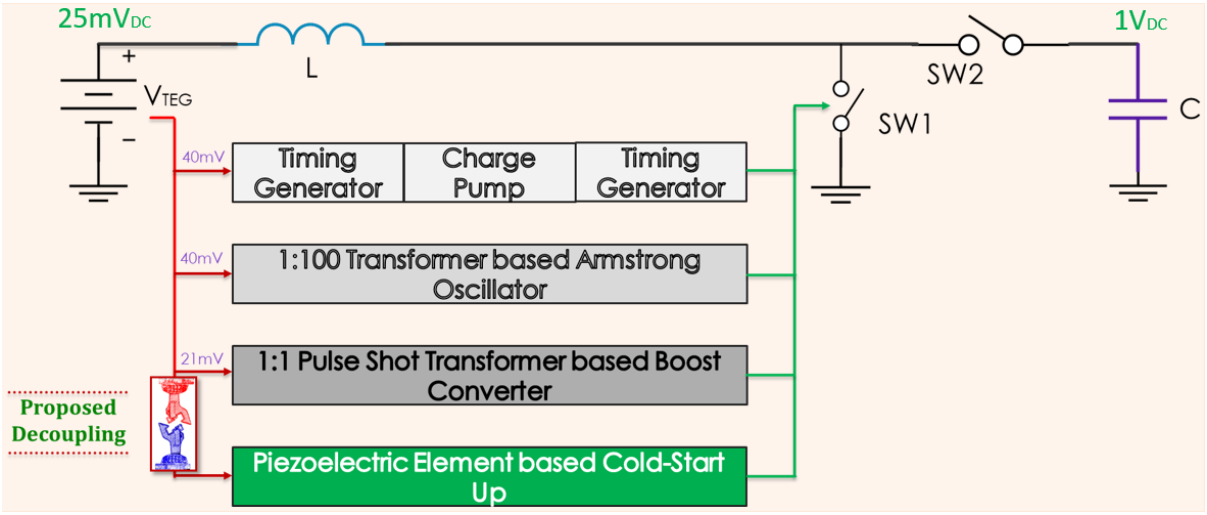


Figure 9. Contemporary Techniques & Proposed Solution

The red line shows the signal path from the TEG to the start-up architecture and the green line shows the signal path from the start-up architecture to the voltage controlled switch of the boost converter. The voltages above the individual start-up block represent the minimum figure achieved by these implementations.

As shown in figure 9, the proposal is to decouple the problem of minimum 'cold start-up' from the TEG and to take it to a different element that is capable of providing the necessary power to the start-up

system. The idea is to free the TEG with the task of providing sufficient power to the start-up system, which limits the minimum voltage that it can provide in order to sustain the system by itself. Hence named 'The Decoupling Solution'. Such a solution also gains importance with regards to the scenario where the temperature gradient across the TEG is not suitable enough to allow it to power the whole sensor, as a result of which the system shuts off. The system would thus be required to start-up and gain normal operation from the point it stopped, as early as possible with as little of a temperature gradient across the TEG as possible. It might be important to bear in mind that for TEG based start-up architectures the minimum cold start voltage is different from minimum input voltage (after cold start-up) the design can handle. This problem has been suitably addressed in [27], although, again the start-up voltage and required temperature gradient were quite high (with regards to our case). The proposition here is to use an EH element that could provide the timing generation for 'free'.

There can again be a debate over what element to use in a case like this, although arguments proposed in favour of a piezoelectric element in section 1.3 appear to be quite suitable to the proposed application. Moreover, one of the fundamentally limiting arguments against it, also does not hold much significance here. The argument was that the piezoelectric element can only supply adequate power whenever it is excited i.e., the human body vibrates (or moves) and thus a continuous supply of constant power should not be expected. Well, in the case of a start-up, a continuous supply of power is not required for longer period of times, since all this system has to do is allow the output of the boost converter to reach a value where it can take control of itself. A short period may be lasting over a few seconds, that in turn pertains to a short pulse of excitation for the piezoelectric element, may be all that the proposed system needs. And intermittent, non-frequent excitations of the piezoelectric energy harvesting (PEH) element may not be a problem anymore. An advantage of PEH is that its output is an oscillating (AC) waveform and thus the necessity to force a positive feedback into the circuit to generate a timing waveform (for 'free') from the available DC voltage of TEG to boost it up through a charge pump or a transformer, can be circumvented.

But would entrusting this crucial 'cold start-up' problem over to the PEH element could be the best choice? For that the following Table IX (courtesy of [39]) could serve as a credible reference:

TABLE IX. Output of Piezoelectric energy harvesting element at different human body movements

Action	V_{RMS} (V)	I_{RMS} (uA)	P_{RMS} (uW)
Walk	0.225	0.479	0.190
Fast Walk	0.198	0.420	0.153
Brisk Walk	0.271	0.576	0.286
Marching	0.280	0.594	0.320
Run	0.301	0.641	0.321
Jump	0.215	0.457	0.183
Get Up From Ground	0.177	0.377	0.121

The piezoelectric element used in the experiments [39] leading to Table IX is an MFC-P2 sold by Smart Material GmbH. The same piezoelectric EHE is proposed to be considered for this work as well due to its proven record for the supposed applications as showed above. One might argue that the Table IX depicts results better suited for a patient different from the case scenario of the girl discussed in section 1.2, however, it should be remembered that this is not fundamental, as the same PEH can be placed on the neck or any other moving joint and it could be tuned (specific orientation/configuration/clamping) to produce more or less the same/better results. The Table IX is a representative and should not be treated for exact face value. It might be interesting to look at the frequency response of the vibrations, a human body motion can produce. Figure 10 (courtesy of [40] & [41]) shows this for two such motions:

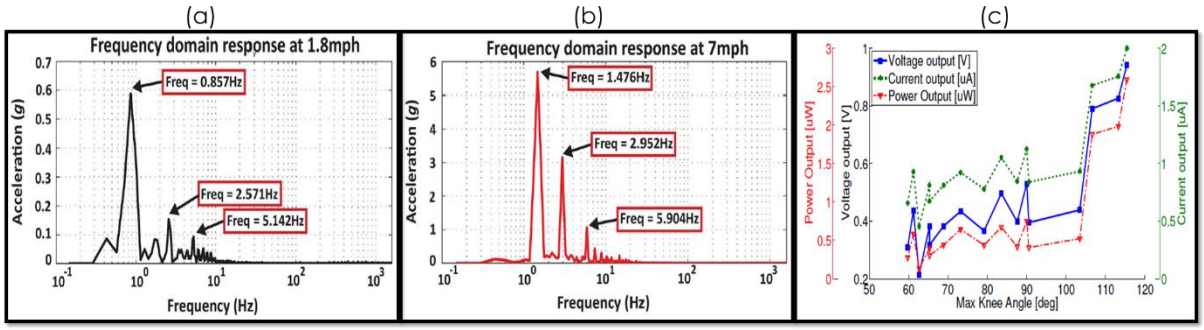
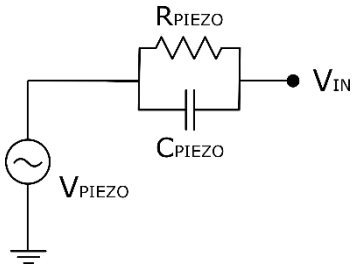


Figure 10. Frequency Response at different human body motion (a) Walk (b) Run; (c) PEH Output v/s Bending Angle of PEH (MFC-P2)

It should again be noted that figure 10 as well is only for representative purposes and numbers should not be taken for their face value as they are subject to change depending on the setup used for measurement, PEH orientation (axis), configuration (for two: series/parallel), attachment to human body (on joints/near joints; sticker/wound around) etc.

Thus, with regards to the above discussion, a PEH with $F_{HARMONIC1}$=2.5 Hz, $F_{HARMONIC2}$=5 Hz, $V_{PEAK(2.5Hz)}$=300 mV and $V_{PEAK(5Hz)}$=100 mV, with an $V_{OUT(RMS)}$=222 mV can be treated as safe to assume. Frequencies < $F_{HARMONIC1}$ could make the cold start-up too slow and also the selected PEH is not designed to work below 2 Hz.

Figure 11 below shows a model of the PEH proposed by its original designers in [41] and as such used in this work as:



R_{PIEZO} = 1 MΩ

C_{PIEZO} = 4.5 nF

Figure 11. PEH Electrical Model

From the figure above, it can be observed that the PEH element does not act as an ideal AC voltage source, instead, it has elements that represent parasitic behaviour of the PEH element itself. For instance, the resistance R_{PIEZO} signifies the dissipative losses that would be incurred to the generated AC signal as it propagates through the piezoelectric material (that is resistive to the flow of electrons) to the load. Another parasitic parameter that is not usually discussed in literature (not that the author is aware of) is the capacitance C_{PIEZO}. This parasitic component of the electrical model results from the very fundamental principle of the piezoelectric effect, i.e. the movement of charges to form a dipole. Since the development of this dipole essentially implies the separation of charges so as to cause a potential difference that allows it to power EH applications, it also leads to the formation of a capacitor due to the separated charges. This is the capacitor that is modelled in figure 11. What the capacitor does is to impede the flow of current at lower frequencies, which is the case in this work.

Now that we have elaborated on the primary innovation that can create the possible solution, lets have a look at the design procedure that lays the foundation of the proposed work.

2.4. Conceiving the Start-Up

Before we begin, it may be worthwhile to consider some case scenarios about how the piezoelectric element can be utilized for powering up the cold start-up system. The following points enumerate these scenarios:

a. The Perfect Solution: PEH is able to deliver a high enough output voltage > 250 mV, at a frequency > 1KHz (say) to power the voltage-controlled-switch (VCS) of the boost converter directly. This represents an ideal solution where the necessity of a separate cold start-up circuit could entirely be negated. However, such a PEH element, although fundamentally possible, has not been seen in a practical implementation as of yet.

b. Transformer Approach: Assuming the PEH is able to resonate at the frequency of operation needed for the boost converter, it might happen that it is not able to deliver the required voltage to the VCS. In this case a simple transformer can be placed at the output of the PEH, to boost it up to the required value. A limiting factor here can be the fact that the designer never knows to what output the PEH can reach at different levels of excitation and thus, the turns ratio of this transformer might be difficult to select, not to burn the VCS. One proposal could be to use a clamp but that would unnecessarily waste power. Also, based on the excitation, the output power v/s $F_{Resonance}$ might vary a lot which may lead the transformer core, not being able to handle such variations (Output power of a piezoelectric element depends on square of acceleration, not frequency [10]).

Please Note:

$F_{Resonance}$ – Piezoelectric resonant frequency

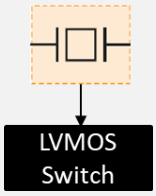
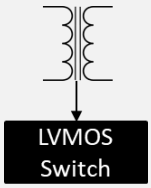
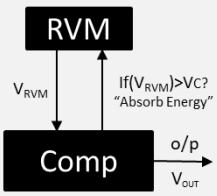
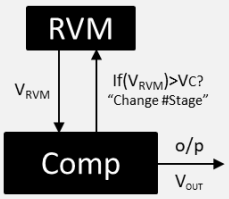
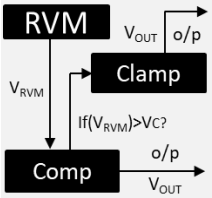
Transformer: *(Area of Core) α (Voltage/Frequency)* – here o/p voltage variation with o/p frequency is non-linear and can be highly abrupt based on a piezo-crystal's design [42].

c. A Non-Ideal Case: Consider a more practical case where the PEH element is not able to provide the required output voltage nor the required frequency. This assumption makes sense since there aren't many PEH that are capable of harvesting energy at frequencies a human body vibrates (moves) and even less PEH that can resonate at such frequencies or have high enough Q-factors to attain resonance even at such low frequency excitations. In order to tackle such scenarios an option can be to transform the AC waveform to a specific DC counterpart and then use this signal to power up a timing generator. Now, this timing generator can operate the VCS and start-up the boost converter to reach a given output voltage. However, a question still remains unanswered, how would a designer account for possibilities of PEH output voltage variations? A possible postulate could be to assume a minimum PEH output voltage and design for that. But then again, excitations leading to a higher PEH output voltage can't just be ignored as they might breakdown the MOS-T gate-oxide. This one question gains further significance, since it has not been properly catered to in a majority of the research work presented by the community, over the last decade. Following points present different approaches that could accomplish this:

- **i.** **Power Clamp:** One of the most popular approaches to counter the problem of excess output voltage. It involves a simple implementation of a Zener diode [31] that burns up the excess energy when the output voltage rises too high above a certain level. The output voltage can be easily checked by employing a comparator.
- **ii.** **Configurable Number of Stages:** In case the input AC waveform is rectified to a DC and boosted up through a number of pumping stages, having a fixed number of stages can raise alarms in case of a PEH source. Thus, a popular opinion is to control the number of stages [38], while keeping a tab at the input PEH signal and employing a complex DSP architecture to estimate the number of stages needed to meet the load (in our case VCS) needs. Thus, unnecessary wastage of energy can be prevented at the expense of increased circuit complexity.
- **iii.** **Absorption:** A new methodology, proposed for only the first time in this work, takes its inspiration from a moving vehicle (reference – Prof. Serdijn's example). Depending upon the road and its traffic conditions (viewed as load) the gears of a vehicle (viewed as pumping stages) can be adjusted on the go and excess energy can be absorbed to move it slower or utilized to move it faster. No need to keep a tab at both the initial and final condition. It can reduce the complexity of the overall architecture compared to the previous approach but is more complex than the 'power clamp' approach. Each pumping stage output can be monitored while automatically connecting them in parallel or series depending on their output to prevent unnecessary voltage boost-up.

The Table X depicts the above approaches and compares them to find the most suitable approach.

TABLE X. Comparison of alternative techniques for PEH power management

Core Technique	One-off Piezo Crystal	Transformer	Absorption	Configurable No. of Stages	Power Clamp
Topology					
Nature	Piezo-crystal V_{AC} directly energizes LVTMOS switch @$F_{Resonance}$	Energy from piezo-crystal directed to LVTMOS switch with voltage matching @$F_{Resonance}$	Energy from piezo passed to load after RVM is checked for exceeding limit or absorbed by RVM	Energy from piezo passed to load after RVM is checked for exceeding limit or #stages lowered	Energy from piezo passed to load after RVM is checked for exceeding limit or excess's removed
Function	High-'Q' piezo o/p voltage @$F_{Resonance}$ capable of cold-start up	High-'Q' & $F_{Resonance}$ piezo with low o/p voltage is scaled to start-up boost converter	Low-'Q' & $F_{Resonance}$ piezo o/p rectified-amplified to match LVTMOS V_{Gate}, with excess voltage absorbed back in	Low-'Q' & $F_{Resonance}$ piezo o/p rectified-amplified to match LVTMOS V_{Gate}, with monitored no. of stages for matching	Low-'Q' & $F_{Resonance}$ piezo o/p rectified-amplified to match LVTMOS V_{Gate}, with excess voltage burned up @ clamp
Implemen-tation	Assuming such piezo-crystal exists, fairly simple connection	Assuming such piezo-crystal exists, fairly simple connection needed	Each RVM stage has to be designed to restart from '0' if o/p voltage exceeded	Excess no. of stages are disconnected from main o/p line for excess o/p voltage	A separate clamp would need to be designed along with a 2-output-comparator
Drawbacks	None as such except for non-availability. Also for high o/p, clamp needed	Power variations with excitations of piezo are non-linear to $F_{Resonance}$, could make transformer core-flux handling inefficient	Could result in a more complex circuit for RVMs	**E**nergy consumed in decision making block to cut-off stages of RVM. **C**ould result in more complex RVM circuit	**E**nergy could be consumed by the clamp along with excess energy that would be burned. **H**ighly inefficient
Selection	NO	NO	**YES**	NO	NO

Please Note: LVMOS = LVTMOS = Low-Voltage-Threshold MOS; In the diagrammatic representation $V_{OUT} = V_C$, RVM = Rectifier & Pumping Stage

Thus, in the next section an answer to the figure 12 below would be looked into, that basically shows the different methods to achieve the Cold Start-up, obtained from the discussion above.

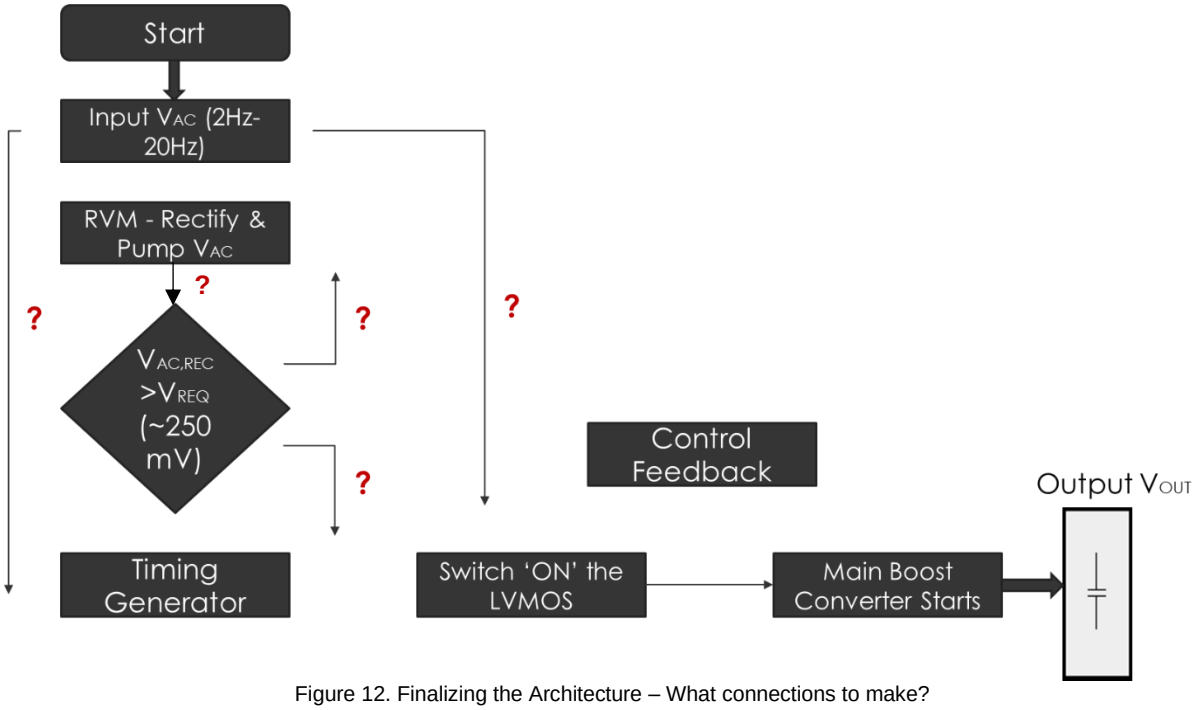


Figure 12. Finalizing the Architecture – What connections to make?

2.5. Architecture Proposal

Lets begin with following a step-by-step progression of the PEH signal, right from the source to the load (LVTMOS), considering the arguments discussed in the previous section:

1st. The PEH element produces an AC signal with an amplitude, say 'V_{IN}', and a frequency in the range of 2 Hz-20 Hz (considering harmonics). Nor the source voltage 'V_{IN}' neither its frequency, say 'F_{IN}', are sufficient enough to drive the VCS of boost converter.

2nd. Thus, this AC signal 'V_{IN}' would need to be rectified and pumped up to a higher value. It may be worthwhile to note that using a transformer to boost this signal may not be a good option as in any ways the 'F_{IN}' is not sufficient and would need to be increased as well, thus would any ways require rectification.

3rd. Now that 'V_{IN}' has been rectified and pumped up to a DC value, say 'V_{RVM}', it needs to be checked if it is high enough to drive the VCS, i.e., V_{RVM} > 250 mV.

4th. If this voltage is higher than 250 mV then a control voltage should be generated to signal the RVM stages to start absorbing the signal. This would ensure a lower voltage ~250 mV at the output of the comparator. In any case, it would be beneficial to ascertain that V_{RVM} is not too big of a value so as to cause breakdown of the succeeding circuitry.

5th. Now, that everything is in line with the amplitude requirements, the output of the comparator would be fed to the input of a timing generator. Thus, an oscillating waveform at the required frequency of operation would result with its peak value at ~250 mV. This waveform can then be applied to the gate of the VCS and the boost converter can then be cold started-up.

6th. Also, applying a feedback to keep a check over the output voltage of the boost converter can be really fruitful since it would regulate the output voltage to the desired level and make the power module more reliable. Thus a control feedback is recommended from the output of the boost converter to the timing generator. Here, it may be noted that this timing generator to which the feedback is applied may not be the same as that of the start-up circuit, but a separate one that controls the VCS with respect to the converter output, implying that the converter has taken over its own operation in a bootstrap fashion.

Hence, according to the direction of events, with regards to the PEH output signal 'V_{IN}', from the source to the load, as has been elaborately prescribed above, the following figure 13 demonstrates the architecture proposed for this project:

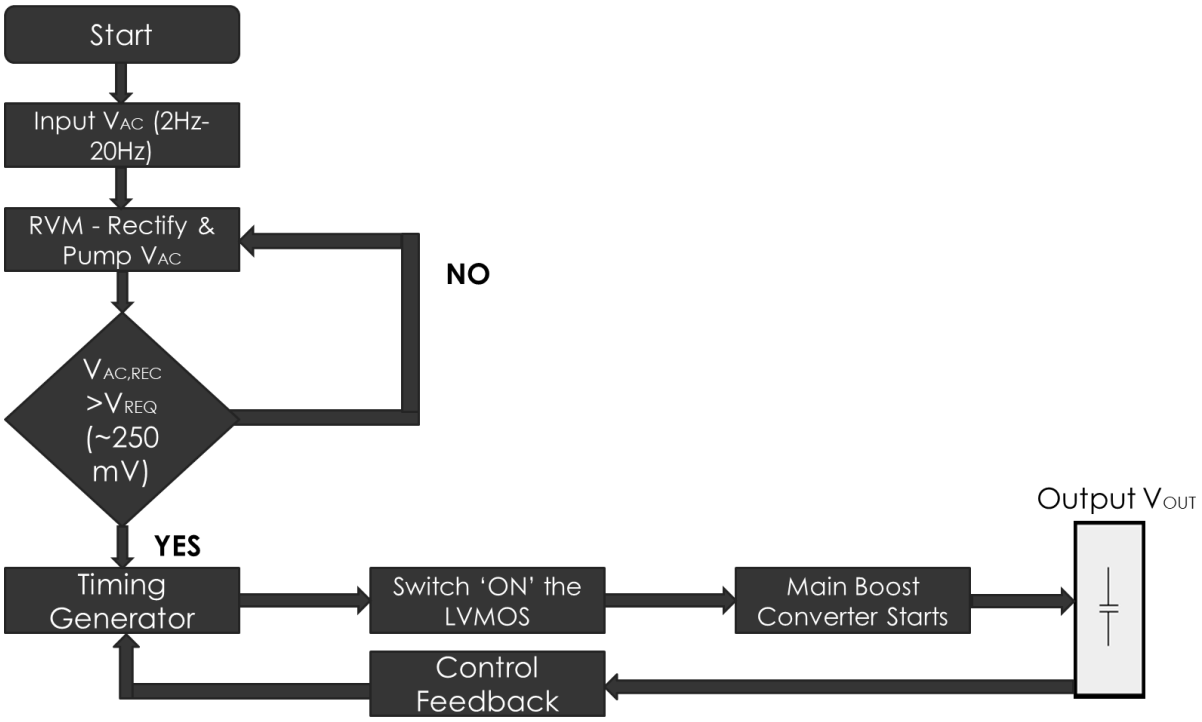


Figure 13. Proposed Architecture

The overall proposal for the Cold Start-up circuit-operated Energy Module is summarized in figure 14.

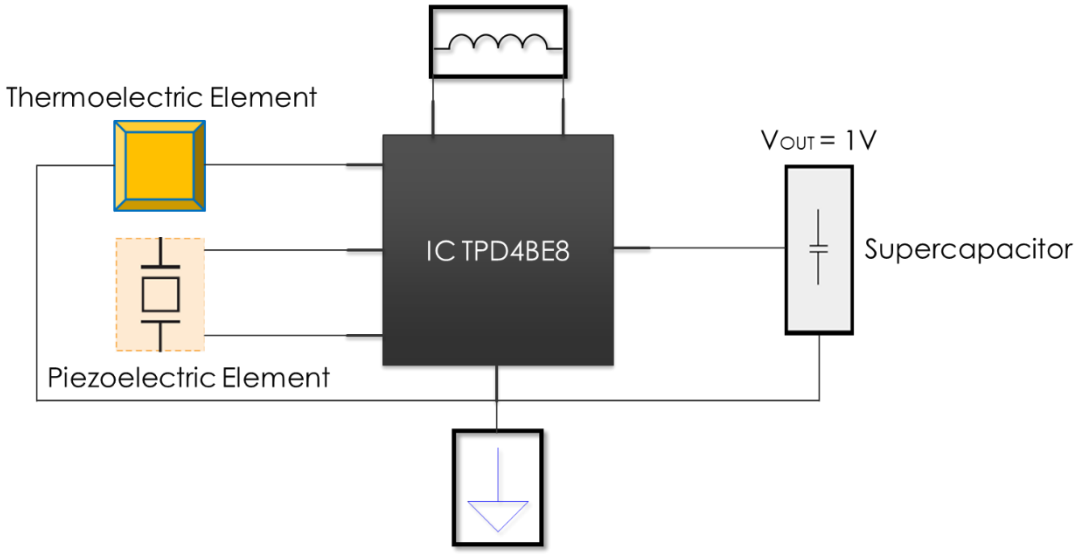


Figure 14. Scope – Overall Proposition for Cold Start-up Circuit operated Energy Module

Chapter 3: One layer down into this IC.

3 System Level Design

Before we delve into nitty-gritty circuit details, it is crucial to understand how the architecture proposed in the Chapter 2 would convert into a circuit that could satisfy the design specifications and may be help the little girl from Chapter 1 as well.

A system level design is essentially a more granular decomposition of the architecture level, that can help bridge the principal ideas therein into efficient circuit implementations.

Hence, the following sections would concentrate more towards exploring the pivotal points about the different blocks discussed in the architectural composition of the research question. Emphasis would be laid on executing the principal ideas discussed in chapter 2 while considering different alternatives for their circuit level synthesis.

3.1. RVM: Rectifier-cum-Voltage Multiplier

As the name states, a circuit that is capable of rectifying an input AC signal into its DC counterpart while pumping or boosting it up to a higher value at the same time is referred to as a Rectifier-cum-Voltage Multiplier (RVM). An RVM is a simple and a deft technique to obtain, ideally speaking, a 2X gain in the input peak AC waveform while it is being transformed into a DC signal [43].

In this work, an RVM is represented as shown in figure 15.

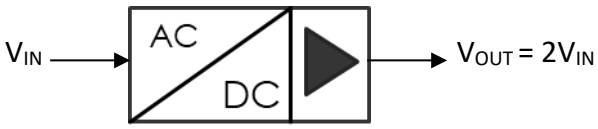


Figure 15. Rectifier-cum-voltage multiplier representation.

An RVM, on a general note, is implemented using a switched capacitor approach. In such an approach the capacitors are responsible for storing the charge in one clock phase and releasing it to the succeeding capacitor in the second clock phase [44]. This can be thought of as filling a water bucket in one attempt and emptying the bucket into a water tank in the second attempt such that each alternate attempt fills this water tank to a higher level. With regards to the rectifying operation, diodes are used that only allow charge to flow in one direction or switches are employed to control the flow of charge in one particular direction.

Broadly speaking, the entire operation is executed by establishing a voltage difference across, a big capacitor and then applying a positive voltage onto the most negatively charged (or grounded) plate. The boosting happens when the capacitor strives to maintain a constant voltage difference across it, and thus raises the potential at the most positively charged (other) plate by the same amount as the applied positive voltage on its negative plate. The magic element here is the assumption of a big capacitor, which having a larger time constant, finds it difficult in following the voltage applied and thus, being lazy enough, it just shifts the potential of the other plate to a higher value hence maintaining the same voltage difference across it, that it originally had. One can also view this operation in the frequency domain. Now, if the value of the capacitor is pretty big and a high frequency (HF) signal is applied across one of its plate, say most negatively charged, then the impedance offered by the capacitor would be really small and the HF signal would simply pass through it while being level shifted, if the capacitor had a DC bias already applied to it. At this opportune moment, all that needs to be done is to store the increased plate voltage of this capacitor onto an output capacitor to achieve the desired boosted voltage. This operation can be repeated many times in a stage wise implementation to boost the input voltage to a higher value.

There are many different architectures designed under the switched capacitor topology from where a suitable circuit can be selected from. However, before such a selection is made there are a few key points that need to be elaborated upon to gain a qualitative understanding of the comparison:

a. Reverse leakage currents: As referred by some research articles as reverse current or I_{OFF}, for subthreshold operation, it essentially is a consequence of the threshold voltage and the difference in voltage of the drain and source terminals of a MOS transistor (MOS-T) when its gate is held at a potential such that $V_{GS} = 0$ V. An argument can be made stating the region of operation for this transistor being cut-off to refute the importance of such reverse leakage currents. However, it should be remembered that the concept of cut-off region exists for convenience than practical grounds, since a transistor is never 'OFF' even when its V_{GS} is forced to be negative for NMOS and positive for PMOS. There is always a small amount of current flowing through it due to the threshold voltage as long as a potential difference between the drain and source terminals exists as demonstrated in [45]:

$$I_{D,p} = \frac{W}{L} I_0 e^{\frac{-V_{GS}+V_{TH}}{nV_t}} (1 - e^{\frac{V_{DS}}{V_t}}) \quad (8)$$

This equation (8) describes the current through a PMOS-T in the subthreshold region, where 'I_0' is characteristic current related to technology, 'L' & 'W' are MOS-T length and width, 'V_{TH}' is threshold volt., 'V_{GS}' is gate to source volt., 'V_{DS}' is drain to source volt., 'V_t' is thermal volt and 'n' is the subthreshold slope.
Hence, for ultra-low voltage operation below the threshold voltage of a transistor, the effects of reverse leakage currents need to be taken into account. For the case of a charge pump, having a high reverse leakage current means losing the voltage gained by the storage capacitor through reverse flow of current back into the RVM. For any general IC operating at sub-nanowatt power levels, it translates to loss of significant amount of power from a source node to a sink node (such as ground), thus increasing static power losses.
Therefore, as a rule of thumb:

i. Less number of switching nodes should be present to minimize static losses
ii. MOS-Ts should preferably have a higher channel length to minimize I_{OFF}
iii. High voltage-threshold (HVT) devices can also be employed that have a higher channel resistance in the OFF state;

A major concern in such designs could be that the circuit operates at a slower rate, which is a trade-off a designer has to concede with. But for the application this work aims at, cold start-up circuit being slow is not a major concern. The RVM that loads the PEH needs a minimum number of cycles to charge up to a desired voltage and since the PEH operates at such a low frequency, the cold start-up circuit can afford to be slow.

b. Gate Parasitic capacitances: A major concern while considering capacitors and switches for RVM implementation. Bigger the value of gate parasitic capacitance (C_{GS}), larger would be the charge lost from the pumping and storing capacitors, lower would be the output voltage and current. Since the current that can be sourced to the load depends on the charge available with the last stage, for serial capacitor arrangement based RVM this could be a major concern as the output current would also have to cater to the parasitic capacitances of the previous stages connected in series, while supplying the load [44]. Also, for RVMs having only one or two (single phase or dual phase) inputs, they usually employ a serial configuration for voltage boosting, thus no matter how high the boosting ratio is, if the parasitic capacitances are high or number of stages with such parasitics is large, then the entire RVM would suffer from increased charge losses.

c. Current Drive Capability: With respect to the assumed source conditions from the PEH and required load conditions of the VCS, following constraints hold, provided the PEH has low current output as compared to its high voltage output [2,12,39]:

i. The following RVM stages should boost the PEH voltage only enough to strongly turn 'ON' VCS. However, the PEH current drive capability should be improved such that the succeeding blocks are adequately powered while delivering sufficient current to charge-discharge the VCS gate capacitor. At ultra-low power operations, the gate capacitor of a MOS-T can be an important factor to consider, specially if the MOS-T channel width is designed to be large to reduce its R_{ON}. Although this argument does not hold on fundamental grounds since a MOS-T is a voltage controlled device, practically, such limitations arise due to the nature of the metal-oxide-semiconductor layer present at the

gate terminal which effectively acts as a capacitor and can get pretty big depending on the dimensions selected.

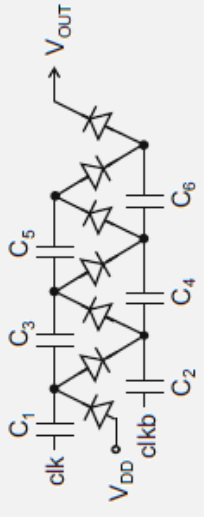
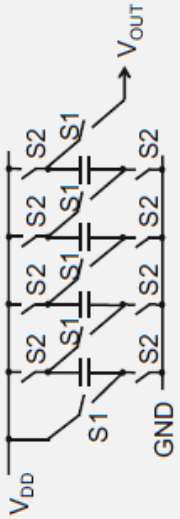
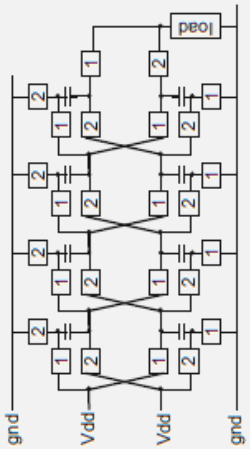
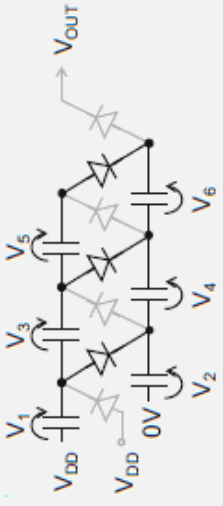
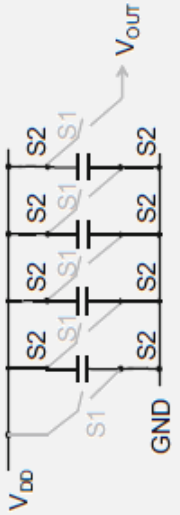
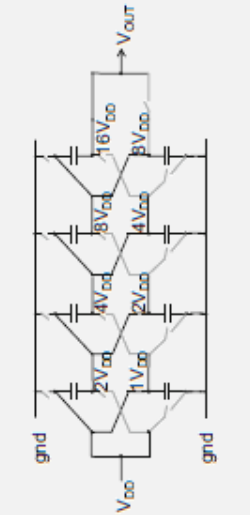
ii. Due to lack of drive current from RVM, oscillating signals from the timing generator to the VCS gate can be rendered distorted with trailing edges. This may disturb the oscillating frequency as well as the turn 'ON' or turn 'OFF' time for VCS making it highly sensitive to process variations.

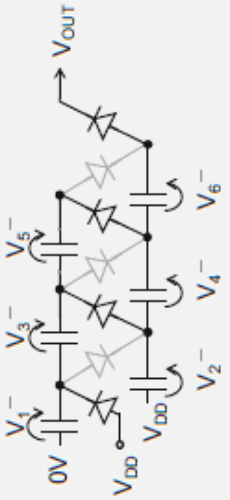
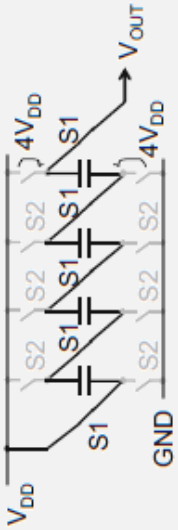
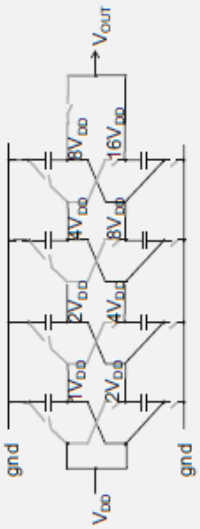
iii. Also, with regards to the VCS of the boost converter, higher is its gate voltage, lower is the 'R_{ON}' offered by this switch in its 'ON' phase. Reduced R_{ON} could significantly decrease the converter conduction losses. Thus, it can play an advantage if the RVM output voltage is higher.

iv. To reduce switching losses, the timing generator can be tuned to operate at a lower frequency which can also facilitate a low current output from the PEH. However, this frequency should be carefully selected not to affect the start-up time and required output voltage of the boost converter.

Now that the key parameters for the comparison are discussed, lets have a look at some of the switched capacitor architectures [44] as shown in Table XI. Also note that for the above comparison dual phase charge pump based RVMs are considered to maintain a fairness.

TABLE XI. Comparison of alternative step-up switched capacitor architectures

Architecture	Cockcroft – Walton ladder	Marx – Brugler serial-parallel	Cernea 2^N	Dickson Linear
Implementation				
Phase I Operation				

Phase II Operation				
Comparison				
Switches/Stage	1	3	6	1
Capacitors/Stage	1	1	2	1
Effect of Reverse Leakage Current	Low	High	Very High	Low
Effect of Parasitic Capacitances	High	Higher	Very High	Low
V_{DD} or Clock Inputs	2	1	1	N
Number of Switch Controls	0 (SCS)	4 (VCS)	6 (VCS)	0 (SCS)
Switching Losses	Low	High	Very High	Low
Conduction Losses	Low	High	Very High	Low
Volt. Boosting ratio	N+1	N+1	2^N	N+1
Preference	NO	NO	NO	**YES**

Please Note: Figures are courtesy of [44]; SCS=Self-Controlled-Switch; VCS=Voltage-Controlled-Switch

What is required from the RVM is a DC output voltage higher than its peak AC input voltage and current drive capability to power the entire cold start-up architecture.

From Table XI, it can be observed that with respect to our design constraints regarding the reverse leakage currents, parasitic capacitances, switching & conduction losses, output drive currents, and number of voltage controlled switches needed, the Dickson charge pump based RVM turns out to be the most suitable choice. Note that having a higher reverse leakage current and increased parasitic capacitances reduces the amount of charge present at the output capacitor and degrades its overall current drive capability. Also, a higher boosting ratio does imply a lower drive output current since the overall power from the input to output of an RVM is essentially conserved. Hence, for ultra-low power operations a higher output current can also imply a lower output voltage with respect to the voltage boosting ratio. Since the application deals with such low input PEH power, having a greater number of precisely timed voltage controlled switches may not be an option, specially at the cold start-up when the PEH AC input power is all that the system has, to offer.

For a Dickson-RVM (DRVM), the architecture incorporates diodes to perform the switching operation. When these diodes are conducting, the input voltage is boosted-up as charges are passed to successive

capacitors. The flow of charges in one direction is what these diodes facilitate and thus, this behaviour is fundamental to a DRVM implementation. Hence, it makes sense to elaborate a bit on the diode behaviour.

Ideally, all a diode has to do, the manner in which it is designed, is to allow the flow of charge in only one direction and block any reverse flow. However, such near perfect ideals does come with their own drawbacks in practicality. For instance, diodes incur a voltage drop, thus, the charges passing through the depletion region of the diode are bound to lose some energy before arriving at the storage capacitances. This results in a net energy loss for the system. This voltage drop also known as the 'diode drop' can be reduced, as has been the case with off-chip diodes that can have diode drops as low as 50 mV [46] and Schottky diodes with a diode drop of 200 mV [32]. A problem often encountered with these diodes is the fact that they usually are off-chip and seldom not available with the technology. In such cases diode implementations of MOS-Ts can be employed as readily available on-chip diodes can have larger diode drops.

Before going into further detail about various MOS-T diode realization, it is worthwhile to be vary about the effect of reverse leakage currents, as discussed previously and its cause.

Hence, let's take a closer look on the different MOS-Ts realizations:

a. Diode connected MOS-T: One of the more popular realizations of a diode, in here, a MOS-T's gate terminal is connected to it's drain terminal while the bulk terminal is connected to it's source terminal, effectively transforming the MOS-T into a two terminal device much like a diode. In this configuration, the MOS-T either operates in the saturation region (in our case, weak inversion saturation region) or the cut-off region. However, it might be important to note that the effect of reverse leakage currents, here, can be significant. For instance, when this 'diode' is reverse biased, MOS-T being a symmetrical device, in case of a reverse polarity signal, would change its source and drain terminal resulting in V_{GS}=0 V while the drain terminal would be held at positive potential and source terminal at negative potential for NMOS and vice-versa for PMOS. Hence, such a 'diode' may not be suitable for ultra-low power operation due to the ratio I_{ON}/I_{OFF} being low.

b. Parasitic Bulk-Drain MOS-T diode: An iconoclastic approach as compared to the conventional diode connected configuration, it utilizes the parasitic p-n junction formed by the bulk and drain semiconductors. Often disregarded due its undesired conduction of currents in reverse bias situations as may happen in our case, this diode can itself be looked into for higher I_{ON}/I_{OFF} ratio, i.e., for subthreshold voltages. In this realization, the bulk, source and gate of a MOS-T are connected together and treated as a single terminal while the drain, now, becomes the second terminal of the 'diode' thus formed. Here, the bulk, source and gate terminals are held at the same potential, thus, mitigating the case, where due to reverse biasing, a MOS-T, being symmetric, may change its source and drain terminals giving rise to higher reverse leakage currents. Since it is literally the diode a.k.a. the parasitic diode that's being employed, and MOS-T behaviour, broadly speaking, is not being utilized anymore. Although, on a more device level, it can be easily noted that the gate terminal, when held at a positive potential, would form an n-channel in NMOS (vice-versa for PMOS) and the current would flow from both the source to drain and bulk to drain which might lead to more conduction losses than expected. In case of a reverse bias being applied to the 'diode', it may be observed that the parasitic diode will not conduct anymore except for a small diode characteristic current, while the gate being at negative potential will not effectuate an n-channel formation (vice-versa for PMOS) and conduction even from a parasitics point of view will be significantly reduced. A pictorial representation is shown in figure 16 below.

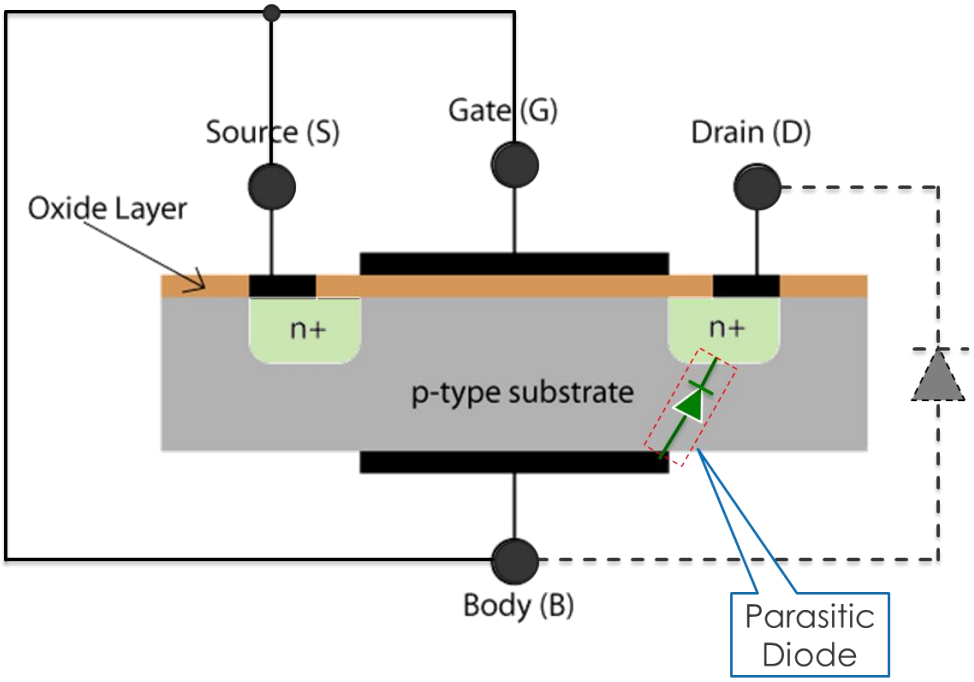


Figure 16. Parasitic diode implementation of a MOS-T

A more qualitative comparison is presented in figure 17 and figure 18 below, as follows:

- **Config. 1**: PMOS used in a parasitic diode configuration
- **Config. 2**: NMOS used in a parasitic diode configuration
- **Config. 3**: An N-Well diode available in the TSMC 0.18 um technology
- **Config. 4**: NMOS used in a diode connected MOST configuration
- **NOTE**: All MOS transistors have the same Widths & Lengths

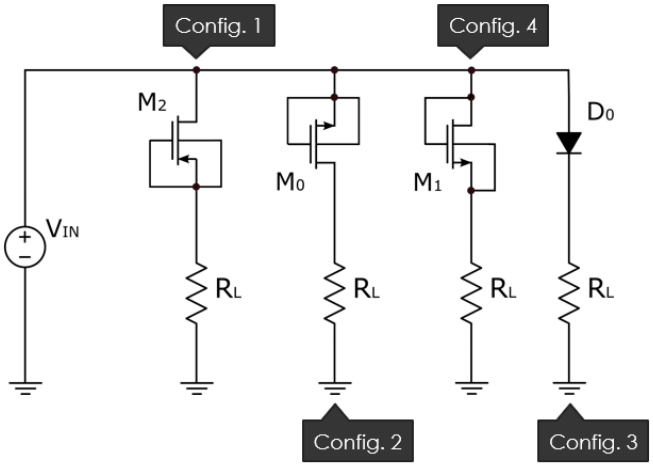


Figure 17. MOS-T based diode configurations along with an available on-chip diode

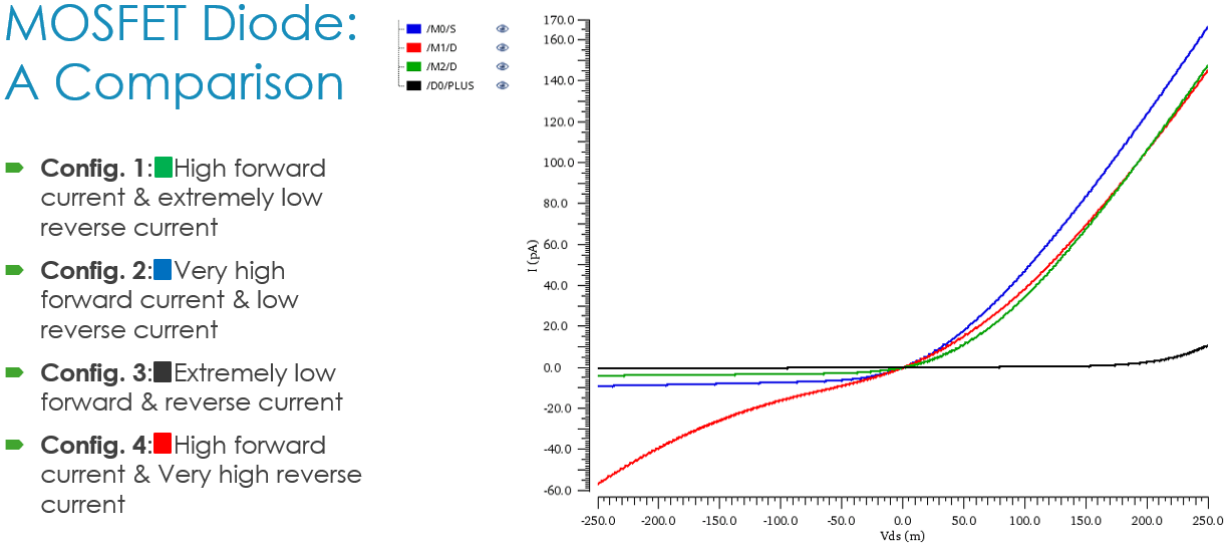


Figure 18. Comparison of I_{ON} & I_{OFF} for different diode configurations

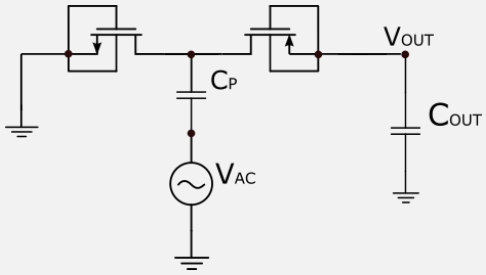
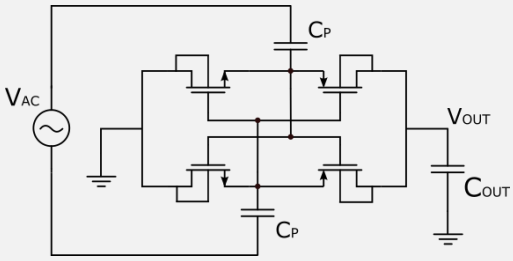
As can be observed from figures 17 and 18 above, comparing quantitatively the forward current, I_{ON} & reverse leakage current, I_{OFF} for different MOS-T based diode configurations as well a diode available in the technology, the 'Parasitic Bulk to Drain MOS-T Diode' appears to be the best suitable option with respect to its high I_{ON} and very low I_{OFF} currents. Moreover, it can be noted from figure 17 that the I_{OFF} for PMOS based parasitic diode configuration is lower than the NMOS based one, while the I_{ON} for NMOS based parasitic diode configuration is higher than the PMOS based one, which can also be ventured into for possible application in the switched capacitor implementation. In the selected config., lower I_{ON} & I_{OFF} for the PMOS is as expected due to its lower charge-carrier (hole) mobility for the same channel width and length, as compared to its NMOS counterpart.

It may be worthwhile to remember that the switching operation can also be implemented by MOS-T switches. However, the effect of reverse leakage currents could be higher degrading the I_{ON}/I_{OFF} ratio, as compared to the parasitic diode configuration. One reason is due to the change of drain and source terminals, on the application of a reverse bias which can increase the reverse leakage currents, if there is a potential difference, much like the case with a diode connected MOS-T config.

Till this point, the discussion about the switched capacitors was mainly concentrated on the various architectures with the assumption of a dual phase RVM circuit. Therefore, it would be beneficial if now a comparison can be laid out with regards to the single and dual phase DRVM, to select a more appropriate RVM realization. Table XII shows this:

TABLE XII. Comparison of single and dual phase RVM methodology

Topology	Single Phase Dickson Rectifier-Voltage Multiplier	Dual Phase Cross-Coupled Rectifier-Voltage Multiplier
Nature	Signal is stored on one energy storage element in the first cycle and then the pumped-up energy is transferred to another storage element in the second cycle, thus increasing the overall positive voltage across it (ideally doubled) [47]	Signal is stored on first arm's energy storage element in the negative clock cycle while its opposite phase is transferred to the load from the second arm having the positive clock cycle (ideally doubled). Then the process repeats for the second arm, thus requiring two clock phases [45]

Implementation		
Advantage	Beauty of this methodology lies in the manner the MOS-T based parasitic diodes can be utilized and the need of only one clock phase	Beauty of this methodology lies in the manner self-$V_{THRESHOLD}$ of the MOS-T switches are cancelled using the opposite phases of clock at V_{GS} with the requirement of two separate clock phases
Comparison	1. Can be realized with self controlled switches, i.e. diodes 2. Brings down voltage drop (& power loss) if the diode threshold voltage is low enough (Schottky) 3. MOS-T parasitic diodes can be explored as switches to allow for high I_{ON}/I_{OFF} 4. Since only two switches are needed per stage, parasitic losses are minimized 5. Single phase architecture allows to have the entire input waveform on the signal path to load 6. Only one pumping capacitor implies lower chip area per stage	1. Needs voltage controlled switches (MOS-Ts) 2. Brings down voltage drop if lower $V_{THRESHOLD}$ MOS-Ts are used but that could increase reverse leakage currents 3. MOS-T parasitic diodes cannot be explored as switches, since it has low I_{ON}/I_{OFF} 4. Since four switches are needed per stage, parasitic losses incurred are higher due to factors discussed previously (Table XI) 5. Two phase architecture only places half of the input waveform on the signal path to load 6. Two pumping capacitors may lead to higher chip area per stage 7. Control requires the source to use both the negative & positive terminals, that could lead to different peak-to-peak values at the input of the two arms if the load seen by these terminals differ, may disturb voltage gain
Preference	**YES**	NO

Hence, as can be witnessed from Table XII, the DRVM with a single phase operation can be considered as the more suitable methodology to realize the DRVM topology. Also, it can be noted from the table above that an NMOS parasitic diode is used in series with a PMOS parasitic diode in the single phase DRVM. This is implemented so as to reduce the ripple voltage on the output capacitor due to reduced I_{OFF} of the PMOS parasitic diode. While, since the NMOS parasitic diode has a higher I_{ON}, the pumping capacitor is charged up to a more negative value at its lower plate in the first cycle. Thus, in the second cycle, it can pump up a higher voltage value onto the output capacitor, when a positive voltage is applied to its more negative charged plate.

Figure 19 summarises the entire discussion on the RVM block, depicting the selected architecture of DRVM along with the respective voltage waveforms of the nodes to provide a brief (surface) overview on its working.

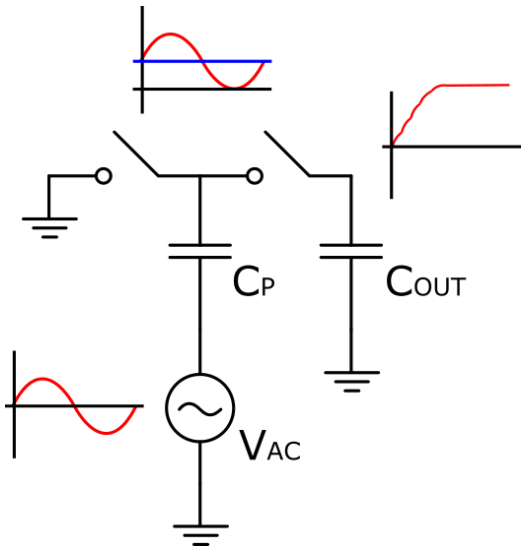


Figure 19. Dickson charge pump based RVM along with its voltage behaviour at the two nodes

3.2. Self-Reconfigurable Rectifier-cum-Voltage Multiplier (SRRVM)

Before going directly to the involving details, it might be worthwhile to remember the technique from Chapter 2, that was only discussed via a block level perspective, called 'Absorption'. It is defined as a technique that could facilitate self-adjustment of the RVM stages based on the input voltage amplitude, resulting in a given configuration. What such a technique has to offer is called the **Concept of Self-Reconfigurability** as:

a. Regulated output voltage even in cases where shock excitations of PEH can produce higher source voltages. Having such a technique to facilitate output voltages within a certain acceptable range, to sufficiently power the load and to not destroy the gate oxide of the succeeding circuits or even the load (VCS), could be a boon with regards to unreliable, randomly-varying input source voltages.

b. Higher output current specially in cases where the PEH voltage is sufficiently high enough to be directly used to power the succeeding circuits along with the load. Herein, a parallel arrangement of all the stages of RVM, thus employed, would allow for the same output voltage through each stage while contributing to a higher output current, ideally N-times assuming N-stages. Such an approach can be advantageous provided the fact that in ultra-low power operations, driving the devices, MOS-Ts and capacitors alike, becomes a huge challenge due to the unavailability of the required current. Thus, if all the stages of the RVM are put to series under all circumstances, in many cases it would mean that the current drive capability of the cold start-up circuit is not adequate enough to allow the circuit itself to follow the huge supply voltage and hence, the circuit would either become far too slow or not work at all due to the MOS-T's '*Gm*' being too low.

c. Time to cold start-up heavily depends upon the amount of time the output capacitors of the RVM take to charge. This charging time is a consequence of the frequency of operation i.e., the frequency at which the PEH supplies AC power to the RVM. For this particular application, it has already been witnessed that such a frequency is extremely low, i.e. 2.5 Hz-5 Hz, which some may call 'almost DC (not really)'. Hence, the start-up can take quite some time until the output capacitor reaches a desired value. This could translate to the fact that the person with the wearable device would have to initiate quite a number of excitations and then be patient for some time so that the sensor can finally start-up. An approach to prevent this could be, to use a large pumping capacitors. This would allow the last stage to charge-up to the required value in a pretty short period of time, being pumped up by the proceeding stages utilizing only the first few cycles of the shock excitation. Thus, the last stage could start powering the succeeding circuits, while earlier stages are charged to the required voltage. When this happens, all the stages would appear in parallel providing the same required voltage but with a higher drive current resulting in the cold start-up circuit gaining momentum and higher drive capability for the load. At this point it

is not difficult to get swayed by the notion of having higher pumping capacitances and RVM stages, however, one should be vary of the trade-off payed in terms of the chip area. Therefore, a careful analysis needs to be made before arriving at any conclusions, paying close attention to the practicality of solution (time & AC cycles needed to cold start) and affordable chip area.

Figure 20 shows a pictorial representation for this Concept of Self-Reconfigurability**.**

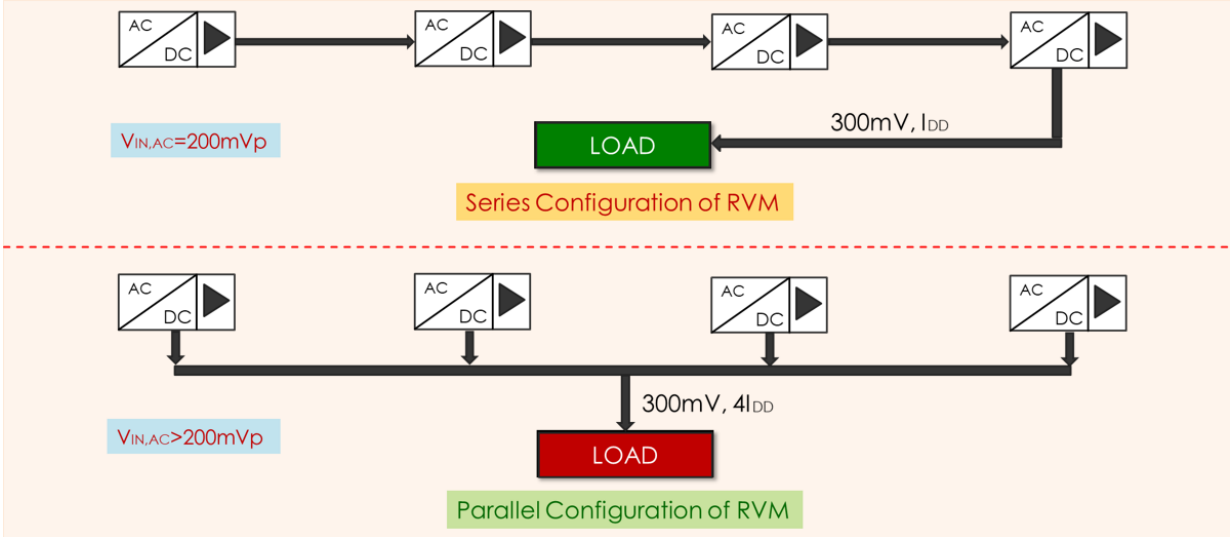


Figure 20. Self-Reconfigurable RVM concept, ideal operation

Here, it should again be remembered that the voltage values in figure 20, are only for representative purposes to bring out the exact idea and not to be mistaken for exact face value.

3.3. Decoupling Stages

In order for the SRRVM to get into different configurations, it would need some kind of suitable arrangement of switches to decouple it from the succeeding and proceeding stages when in parallel and to couple it again when a serial voltage boosting operation is needed. One such arrangement of switches is shown in figure 21.

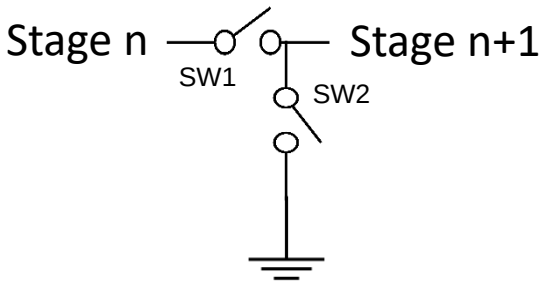


Figure 21. Decoupling switches (Ideal)

A simple implementation, shown in figure 20, of the proposed decoupling switch would do the trick. For instance, all that this switch has to do is disconnect the adjacent stages and connect their respective DC biasing point to ground, when in parallel and connect these stages together and disconnect their DC biasing point from ground, when in series. Also, an important point to observe here is that the more complex the switching network is, the higher will be the losses due to switching, R_{ON} conduction, parasitics and reverse leakage currents as discussed in section 3.1.

A transistor level representation of the decoupling network employing MOS-T based switches & operational-logic is shown in figure 22.

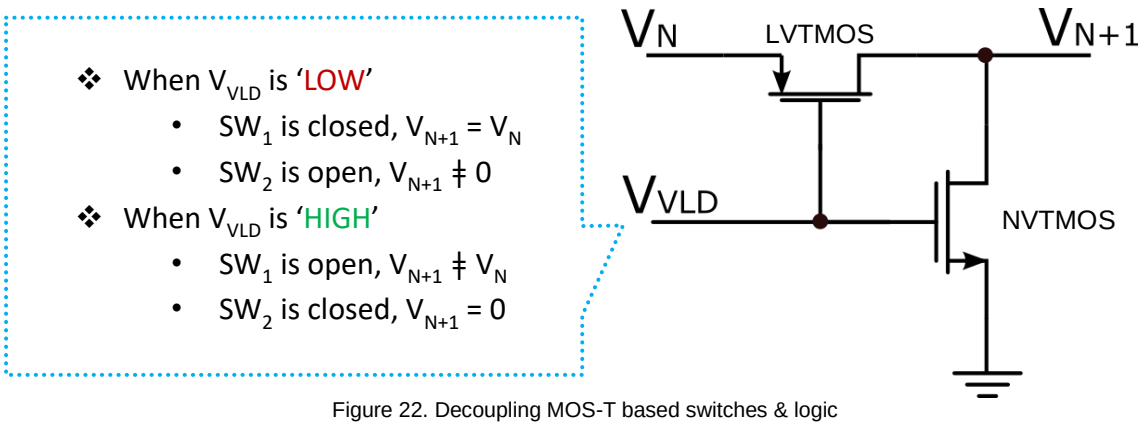


Figure 22. Decoupling MOS-T based switches & logic

While implementing figure 22 into an IC, there are a few key points that would need attention such as:

a. MOS-T $V_{THRESHOLD}$: In such cases it might be tempting to use LVTMOS as switches since they require a low voltage as their V_{GS} to operate and have a lower R_{ON} than their Nominal $V_{THRESHOLD}$ (NVTMOS) or High $V_{THRESHOLD}$ (HVTMOS) counterparts. However, with such transistors leakage current I_{OFF} becomes a major concern for efficiency. Consider for instance, using an LVTMOS as SW2. In this case since there is a relatively high leakage current than an NVTMOS, thus during series configuration a significant amount of current can be sunk to the ground node. This could significantly reduce efficiency, with current being a scarce and important resource here. Although, on the other hand, use of an LVTMOS as SW1 might serve better prospects, since when in series config., V_N and V_{N+1} would need to be the same, thus implying very low R_{ON} for higher efficiency. Moreover, if an NVTMOS (preferably NMOS) is used as SW2 to obtain high R_{OFF} and lower I_{OFF} for series config., its high gate control voltage requirement can be used for SW1 LVTMOS (preferably PMOS) to strongly turn it 'OFF' reducing any I_{OFF} significantly, if a parallel config. were to result next. Also, since I_{ON} and R_{ON} are less of a concern in parallel config., since all that SW2 has to do is force a ground at the input, NVTMOS can be regarded as a suitable switch.

b. Gate Control Voltage: A designer must be vary of the fact that voltages available on-chip are the only voltages that can be used for this purpose. An NVTMOS might need a gate voltage as high as 600 mV while an LVTMOS might need around 250 mV. To this extent, it might be beneficial to look how higher node voltages can be obtained on-chip using less area and resources. Another stage for RVM with very low pumping and storage capacitances, only to get a higher node voltage to drive smaller the gate capacitances of high voltage controlled MOS-Ts, can also be treated as a good option.

3.4. Voltage Level Detector (VLD)

For the SRRVM to decide on whether to switch configurations from series to parallel and vice-versa, it would need to know where to draw the line, i.e. whether it has obtained an adequate voltage or not, to reconfigure. Therefore, there arises a need for a detector that can signal the SRRVM once a predetermined voltage has been reached at its output. But a question arises, what kind of detectors can be used, given the fact that comparators consume a lot of power [48]. Since power, and specially current is a scarce and valuable commodity in this design, a different approach to measure the output voltage of the SRRVM has been utilized. This approach is known as the 2T Voltage Level Detector. Simply put, a voltage level detector [32,49] is a circuit where the output voltage starts following the input voltage once a pre-designed $V_{THRESHOLD}$ has been reached.

The working of such a circuit technique can be explained with the help of figure 23 as follows:

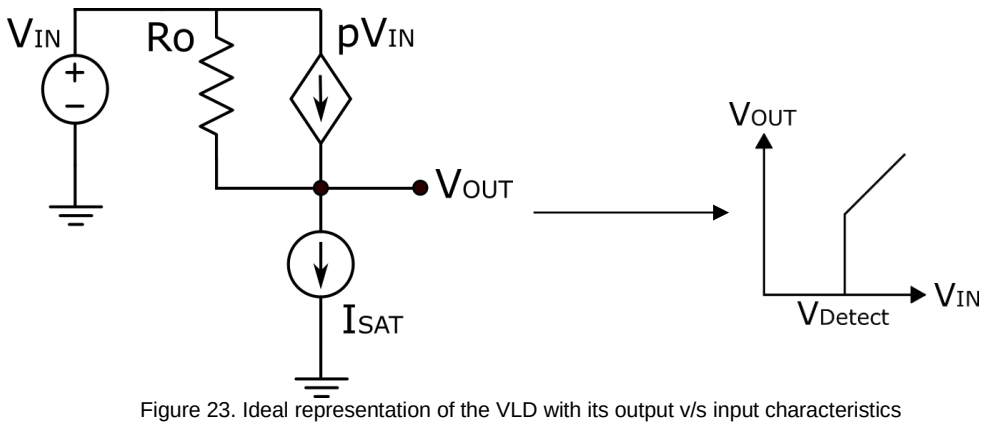


Figure 23. Ideal representation of the VLD with its output v/s input characteristics

It might be worthwhile to note that figure 23 shows a representation of the VLD and not the actual circuit. A VLD essentially is a current source matching problem. The following points tend to present and elaborate on this problem:

a. The VLD comprises of a voltage controlled current source 'pV_{IN}' and an independent current source 'I_{SAT}'.

b. By tuning the values of 'p' and 'I_{SAT}', the respective detection/threshold voltage, 'V_{DETECT}' can be set.

c. The VLD technique is all about changing the value of 'V_{IN}' (increasing it from 0 V) such that when '$pV_{IN}=I_{SAT}$', it elicits '$V_{IN}=V_{DETECT}=V_{OUT}$', after which '$V_{OUT}$' readily follows '$V_{IN}$', with excess current delivered to load or sunk.

d. To understand why '$V_{OUT}=V_{IN}$' at this point, it may be important to realize that the current flowing through the entire circuit is constant at V_{DETECT}, and the value of this current is only determined solely by the independent current source. Hence, the circuit acts as if there is only one big resistor in terms of 'I_{SAT}' that is responsible for setting the current and thus, all the input voltage drops across it. Moreover, at this point, there is no current flowing through 'Ro', thus, resulting in '$V_{OUT}=V_{IN}$'. Therefore, '$pV_{IN}=I_{SAT}$' dictates '$V_{IN}=V_{DETECT}=V_{OUT}$'.

e. In terms of circuit implementation, the 'I_{SAT}' is generally designed using a gate to source connected PMOS-T that operates in the cut-off region with only its saturation current to account for 'I_{SAT}'.

f. The dependent current source 'pV_{IN}' is usually implemented via a gate connected to ground, source connected to 'V_{IN}' to allow the MOS-T to be ON, and drain connected to the 'V_{OUT}' node. This PMOS-T is generally operated in the weak inversion triode region for low 'V_{DETECT}'.

The circuit thus formed for the VLD, since it operates with one MOS-T in the cut-off region working only on its saturation current can be designed for ultra-low power consumption in the sub-nanowatt range. The power consumption can be further reduced to the picowatt domain by using large channel length MOS-Ts and if available in technology, HVTMOS-Ts. The trade-off again would be slow operation but if the VLD is not used for fast transient responses, it would not affect the VLD transfer characteristics.

3.5. Timing Generator

Final block towards the implementation of the cold start-up is the timing generator. The function of this block is to provide a periodic signal, either square wave or a sine wave, to the VCS of the boost converter to control the charging of the inductor current and its discharging into the output capacitor. Thus, a higher output voltage at the output of the boost converter can be ascertained from an extremely low TEG voltage. There are different implementations of the timing generator as elaborated and compared in Table XIII. A note worth paying attention to is that a sine wave signal at the gate of the VCS would not be able to switch

it strongly ON for a longer period of time as compared to a square wave of the same period. Thus, a sine wave driven VCS would find it difficult to charge the inductor current to a higher value which may degrade the voltage gain of the boost converter.

TABLE XIII. Comparison of different architectures of timing generators

Topology	Phase Shift Oscillator	Tank Oscillator	Ring Oscillator	Relaxation Oscillator
Nature	Signal supplied from source is 180˚ phase shifted using filters satisfying Barkhausen criteria to produce positive feedback at the inverting element [50]	Signal supplied from source cycles between magnetic and capacitive energy storage elements to produce oscillations [33, 50]	Signal from source is inverted repeatedly and fed back to the input to produce oscillations thus, satisfying Barkhausen criteria [32, 50]	Signal from source is stored on energy storing element which is repeatedly charged and discharged due to inverting elements being switched at each cycle
Function	An inverter connected to a series of R-C filters with a unity gain feedback produces oscillations due to signal being amplified repeatedly at the output when overall gain>1 and overall system phase=360˚	An inductor and a capacitor repeatedly exchange the signal due to one's stored quantity when charging becomes another's charging quantity when discharging, in an inverted fashion	Inverters connected to each other in a series repeatedly switch the signal such that when connected back to input in unity gain feedback, the system has 360˚ shifted in phase and positive feedback produces oscillations	Signal is built up in a capacitor due to noise starting up the system, giving rise to increased gate voltage of one inverter and vice-versa for another, which reverses the flow of current and gives rise to repeated charge cycles
Implemen-tation	RC Oscillator	LC Oscillator: Colpitts	CMOS Inverter based Ring Oscillator	Source-Coupled Voltage Controlled Oscillator (SCVCO)
Comparison				
Qualitative	1. Could be used to obtain a range of frequencies with R-C banks 2. Energy is dissipated due to resistive components 3. Discontinuous control of frequency 4. Requires energy storage elements	1. Low tuneable range, suited for narrowband applications due to LC tank 2. Ideally no energy loss 3. Discontinuous control of frequency 4. Requires energy storage elements	1. High tuneable range 2. Ideally no energy loss 3. Frequency varies continuously with current 4. Requires no energy storage element	1. Not highly tuneable 2. Energy loss depends on type, SCVCO ideally has no energy loss 3. Frequency varies continuously with current 4. Requires energy storage elements
Quantitative	1. High chip area 2. High power consumption	1. High on- & off-chip area	1. Very low chip area	1. High chip area

		2. Low Power consumption 3. Minimum $V_{STARTUP}$= 40 mV 4. Minimum $I_{STARTUP}$ > 1.25 uA	2. Ultra-low power consumption 3. Minimum $V_{STARTUP}$= 60 mV 4. Minimum $I_{STARTUP}$ > 1 nA	2. Low Power Consumption [51] 3. Minimum $V_{STARTUP}$= 0.6 V 4. Minimum $I_{STARTUP}$ > 7 nA
Preference	NO	NO	**YES**	NO

Hence, as can be observed from Table XIII, the Ring Oscillator(RO) turns out to be the best suitable option for the cold start-up circuit satisfying the power and area budget along with offering a wide tuneable frequency that is highly linear with the supply voltage. Moreover, a ring oscillator based timing generator can be designed in a current starved fashion to account for ultra-low power consumption and reduce oscillation frequency sensitivity to process & supply variations [52].

3.6. Bootstrap Feedback

Once the cold start-up circuit accomplishes in driving-up the boost converter, it may occur that the piezoelectric energy harvesting element is not capable of producing a sufficient number of AC cycles. If this were to happen, the entire architecture would fail as the output voltage of the boost converter might fall to zero and the entire endeavour might be nullified. Thus, there arises a need for a bootstrapping technique such that after a sufficient voltage has been delivered at the output (capacitor), the converter takes over control of itself. This would not only reduce the dependence on PEH to provide a higher number of AC cycles, which in many cases could be infeasible, but also allow a degree of freedom to the designer to select the number of AC cycles needed to guide the boost converter to the bootstrapping stage. This might be advantageous, given the fact that the whole operation can be rendered autonomous with respect to only one EH element working (TEG) while also allowing the PEH to be utilized for different applications such as a human activity recognition through kinetic energy harvesting (HARKE) framework that is used to track human body gait and behavioural patterns.

Now the question arises, how to implement such a bootstrapping operation? While deciding this aspect, I might be important to remember that the bootstrapping circuit should be:

a. Ultra-low power consuming or the output capacitor would deplete before the boost converter can replenish it to an even higher level. As a rule of thumb, charge stored into the capacitor should be greater than charge released by it to the bootstrapping circuit. Attention should be paid to the fact that the bootstrapping circuit is an auxiliary circuit that only drives the boost converter and thus, should be less power hungry.
b. Providing a feedback to maintain the voltage at the output capacitor at a constant level. A careful design of the bootstrapping circuit can ensure this by either:
    i. **Pulse-width modulating** its output frequency which it uses to control the boost converter operation. This could lead to a higher power consumption since modulating the pulse-width of a constant frequency signal might incur more energy consuming components like a ramp generator, comparator, digital logic, etc. Still, it might be beneficial to accomplish it since the duty cycle is, fundamentally speaking, a primary control for achieving a desired output voltage and has a better control over it.
    ii. **Frequency modulating** its output to control the boost converter operation. This could be easily accomplished by using a voltage controlled oscillator like the previously discussed ring oscillator that has a linear voltage control over a wide range of frequencies. Although this kind of control is not fundamental to a boost converter operating in Continuous Current Mode(CCM), however, it plays well with a Discontinuous Current Mode(DCM) control. Also, such an approach would be the least power hungry, hence quite favourable to the stated cause.

Since the bootstrapping is now also expected to be operating with a feedback control, hence, the name ‘Bootstrap Feedback’.

3.7. System Level Design: Proposal

Figure 24 illustrates the system level design proposal for the presented architecture in chapter 2. This work would focus on the IC design based on this proposal and thus, would cater to solve the undertaken research question.

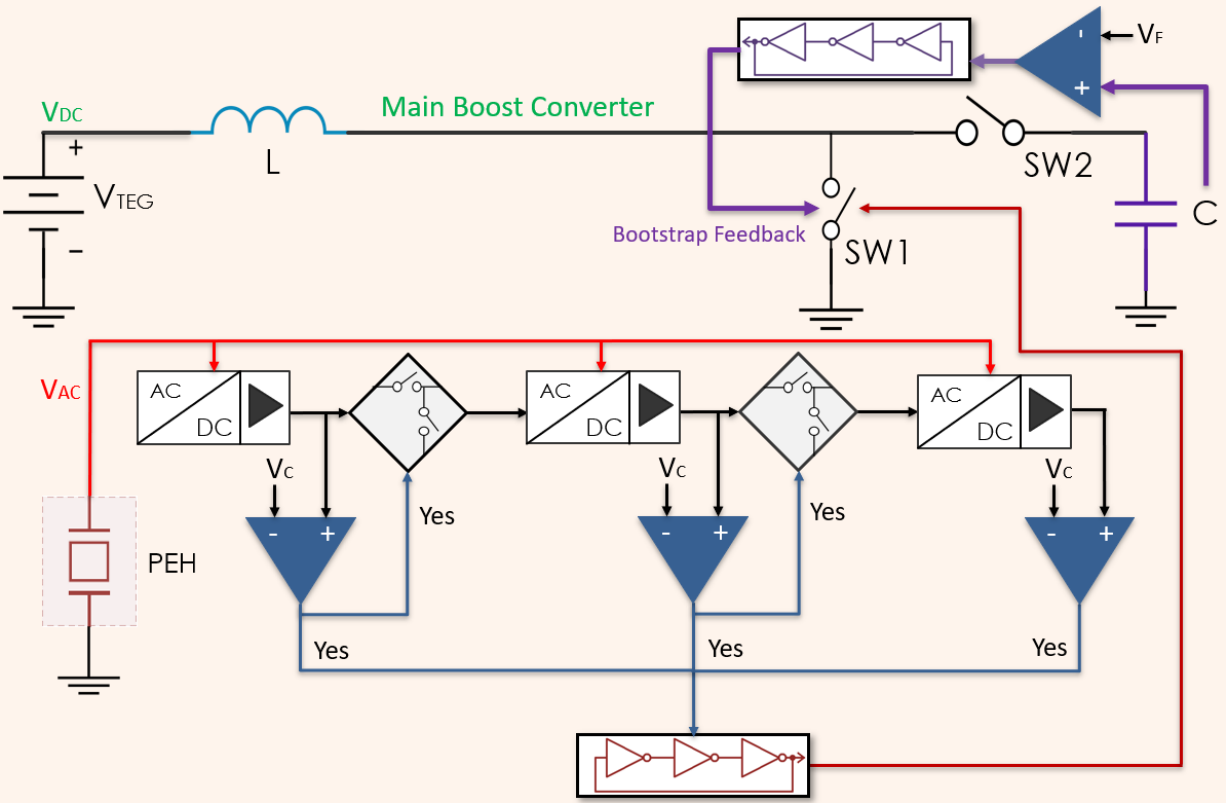


Figure 24. System level design - proposal

As can be observed, the design, thus proposed, strives to present a neat and simple implementation for a cold start-up circuit without employing any complex logic [53,54] or DSP [38] to perform the self-reconfigurability operations, which also sets it apart from what has been presented in literature as of yet. The author believes it to be a responsibility to design this system as intuitive as possible with as less complexity so as to make it not only intelligible but also reproducible.

Figure 25 presents the essence of the proposal, this work strives to propound.

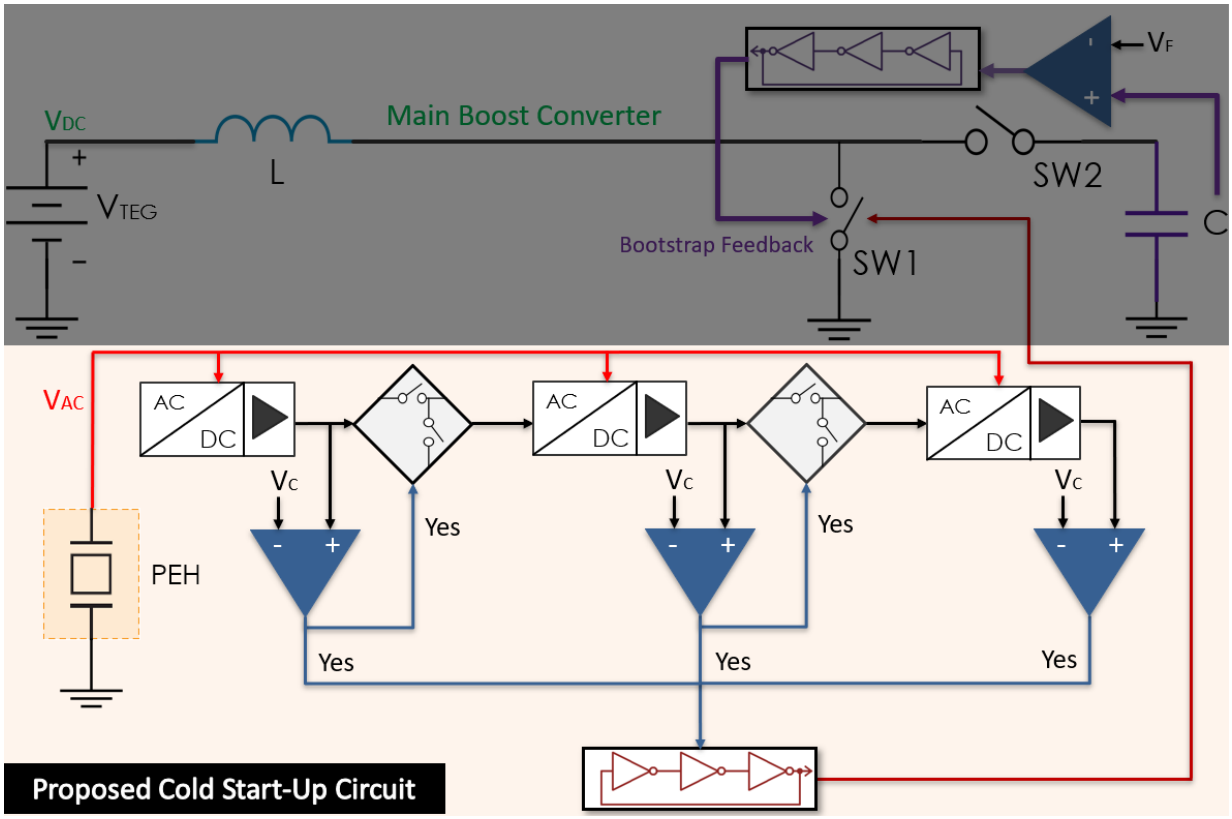


Figure 25. Cold start-up circuit - proposal

Note that the voltages V_C & V_F are produced and compared on-chip with the help of a VLD.

The value of V_C, as has been described above is 250 mV, while the value of V_F deserves a discussion which can be found in the next chapter.

Chapter 4: Into this System, towards IC design

4 Circuit Level Synthesis

In order to begin with the most intriguing part of the work, 'Circuits', it would be worthwhile to have a discussion on the design level challenges that could be encountered and may have the potential to haunt, in due course of this endeavour.

The three most important challenges that have been recorded during this phase of the work, are as follows:

1. Technology Node: The circuit level implementation of the proposed system level design is carried out in TSMC 180 nm CMOS technology node. While there are different technology nodes that are available to select from, they have their own idiosyncrasies such as:
   a. **500 nm**: With such high minimum channel length devices, the threshold voltage of the MOS-Ts increases. Hence, the conduction (charge inversion) for lower gate voltages would be reduced and may impede the strategies to design for ultra-low voltage cold start-up since at such voltages, since the MOS-Ts can never be completely 'ON'. Moreover, a higher drive voltage would be needed to operate the MOS-Ts at relatively higher speeds, or a long cold start-up time can become a major concern.
   b. **40 nm**: With such low minimum channel length devices, the threshold voltage of the MOS-Ts decreases. However, free lunch is a myth. With lower threshold voltages the characteristic currents increase, thus giving rise to a higher leakage in MOS-Ts. Such a scenario may induce higher losses, specially in cases, where voltage boosting is a major concern along with high I_{ON}/I_{OFF} current ratio. Hence, to deliver a higher power at the output from an RVM, say, negative gate voltages for NMOS-Ts and higher positive gate voltages for PMOS-Ts would be required, which may be difficult to generate at such low voltage and power levels. Moreover, to lay a precise control over the MOS-T current at such a technology node can be challenging due to extremely small device dimensions as variability increases.
   c. **180 nm**: With a threshold voltage not too low or not too high, such a technology node can present the perfect solution for ultra-low power IC designs. Moreover, with the employment of low-V_{TH} and high-V_{TH} devices available in the technology, the advantages of both the previously mentioned technology nodes in terms of extremely low leakage currents (500 nm) and lower gate drive voltages (40 nm) may be obtained. Such a technology node can be employed to provide a better suitable compromise with respect to the ION/IOFF ratio and high speed operations to allow for a low cold start-up time, once sufficient voltages are available from the RVM (in this case).

   There can again be a discussion about 180 nm being the perfect sweet spot for such an application, however, this was the only technology node available for the project and thus further debate might not be fruitful. Furthermore, the presented work drives inspiration from a western contemporary (WIMS^2, University of Michigan) that famously designed the smallest computing system/micro-sensor node in the world called the Michigan-Micro-Mote (M^3) with the dimensions of 2 mm X 4 mm X 4 mm [55]. In the M^3, 180 nm technology node was favoured to design the main processor module [55, 56] that consisted of an ARM Cortex-M0+ processor, 3kB SRAM and a power management unit [53-57], the energy harvester module [58, 59], and the communications module [60], for similar reasons as has been discussed in this text.

2. Transistor Sizing: One of the major concerns while designing for ultra-low power operations is about the current consumption of the circuit or more precisely, how much current should be allowed to flow in the dynamic and static state of the circuit?
   In order to restrict the flow of current, the MOS-T operation would need to be pushed towards the weak inversion (WI) region. This can be ensured by applying a voltage at the gate that maintains V_{GS}-V_T < 80 mV. Moreover, larger channel length MOS-Ts can be preferred as they lead to an increase in the channel resistance thus impeding the flow of larger currents and also, as I_{DS} is inversely proportional to channel length, it is favoured. A trade-off here is that the circuit becomes slower but since the operating frequency of the energy source (PEH) is anyway 'near' DC, this would hardly present a radical issue in the overall cold start-up. The reason the circuit slows down

is due to the existence of parasitics. Fundamentally, being a voltage controlled current device, the MOS-T should barely be affected by extremely low currents as long as an adequate voltage is applied at it's gate, however, practically it's a completely different ball-game. With parasitic capacitances coming into the picture such as the gate capacitance, that needs to be charged to the value of the voltage that has been applied across it (gate-oxide), current flowing into the circuit and its fan-out, assume a significant role in determining the speed. Larger the channel length or width, higher will be the gate capacitance and the drive current needed to switch the MOS-T in a given time period. In such scenarios, a sweet spot can generally be found, as due to the presence of gate capacitance and the output impedance of the previous stage, a time constant for the charging of the driven MOS-T elicits. By carefully tuning the channel length and width, requirements of an ultra-low dynamic as well as static current can be met, while preserving speed to a maximum possible level. However, it could be important to note that the optimum sizes (channel length & width) can vary for different MOS-T configurations/circuit-blocks. Criteria that effect such decisions may be fast switching, low current, high supply voltage (in inverters, gate is typically expected to be charged to this level), ripple, time to start-up, output settling time, power consumption and chip-area. Overall design budget, hence, is influenced by these parameters.

3. Selection of V_{TH} (MOS-T Threshold Voltage): Designing for an ultra-low power operation implies controlling the flow of unnecessary current while utilizing the full expanse of the supply voltage available. In such ventures, employing MOS-T devices having different V_{TH} can be a deft and an eloquent approach, provided they are available in the technology. For instance, consider a situation where the available voltage is only around 300 mV to switch a MOS-T or control a succeeding stage. Requirement here is, since the MOST is expected to work as a switch with minimum 'ON' resistance, it should be strongly turned 'ON', thus only favouring strong inversion. An intuitive tactic can be to use a low-V_{TH} MOS-T, with a trade-off paid in the leakage current. This trade-off, however, would depend upon the specific use case with due consideration to I_{ON}/I_{OFF} ratio. Moreover, a different situation may arise that requires extremely low I_{ON} currents while still maintaining a sufficient I_{ON}/I_{OFF} ratio. In this case, one option could be to ridiculously increase the length of the channel, increasing the channel resistance, decreasing the I_{ON}/I_{OFF} ratio accompanied by a similar increase in the parasitic capacitances and chip-area as well. A smart alternative could be to use High-V_{TH} devices. With such MOS-Ts, since V_{TH} is higher, if the V_{GS} voltage is kept sufficiently low (i.e. comparable in magnitude to Nominal-V_{TH} MOS-T's), the device is inherently driven deeper into weak-inversion pulling down the I_{ON} to a lower value. Also, High-V_{TH} devices have lower I_{OFF} currents (low dopant concentration), thus being capable of maintaining sufficient I_{ON}/I_{OFF} ratio even at lower I_{ON}. And since they do not need high channel lengths, they do not present a significantly larger parasitic capacitances. A concern here can be the speed, such devices can offer. While this could be a major deterrent in their employment, an astute approach could be to identify the speed-critical areas in the system and separate the non-critical ones where lower I_{ON} currents can be afforded to decrease the power consumption. In this project, VLD blocks following the RVM blocks present a favourable case scenario to use High-V_{TH} devices. Since the energy source (PEH) is operating at 'near' DC frequencies, the system at this point is inevitably slower, hence the VLDs and their buffers (if need be) can be designed with High-V_{TH} devices. Also, a key point to note can be the fact that even if there is a short delay (could be avoided) between the detection and response, for instance, of the VLD to arrange the RVM stages in parallel, the resulting rising-output voltage would not be of much consequence so as to destroy a succeeding MOS-T's gate, since being slow this voltage would be pulled down before long (through parallel config.).

4.1. Boost Converter: A Non-Ideal Perspective

Designing an IC in the ultra-low power domain introduces parasitics, that are capable of severely affecting the overall performance characteristics of the design. Parasitics in case of the boost converter usually comprise of the input voltage source resistance, inductor winding resistance, VCS 'ON' resistance and SCS 'ON' resistance. Affects of such parasitics can overwhelm the design considerations, as they start playing a major role when the input voltages and currents are quite low and the output requirements place stringent gain ratios of 30X-40X. For instance, with regards to the design of the Cold Start-up, to be commenced in the next section, it would be observed that the output power of this most critical block

would be just sufficient to switch 'ON' and 'OFF' the VCS to start the boost converter. Even then, the VCS being operated in the moderate inversion region with its gate parasitic capacitance getting just enough charge to pull up and down the voltage across it, the 'ON' resistance of the VCS would be significant to cause a large voltage drop across it with respect to the current that the inductor would be charged with. Because the state-of-the-art equations does not hold when the effect of the VCS MOS-T resistance comes into the picture and becomes non-negligible to the point of degrading the design outputs, this study was compelled to undertake a different analysis approach as a part of the thesis. The analysis presented below strives to derive the output voltage of the converter in light of the above discussion (on parasitics).

Lets begin by considering a model of the boost converter in the first phase of its operation as depicted in figure 26:

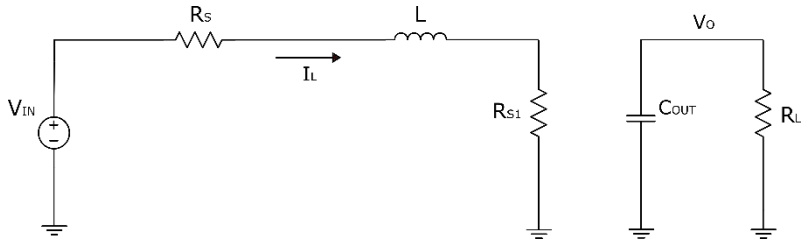


Figure 26. Phase I of boost converter operation, runs for time '*DT*'

Where,
V_{IN} = Input voltage source,
R_S = Source resistance + inductor parasitic resistance,
L = Inductor value,
R_{S1} = VCS 'ON' resistance,
C_{OUT} = output capacitor (also written as *'C'* in equations below),
R_L = output load (assumed to be very large here)
I_L = Inductor current
V_O = Output voltage of converter

The boost converter is operated in the discontinuous conduction mode (DCM) of operation, as discussed in Chapter 3 – Section 3.6. Figure 27 presents the said operation in steady state, in terms of the waveform of inductor current *'$i_L(t)$'* with *'time'*:

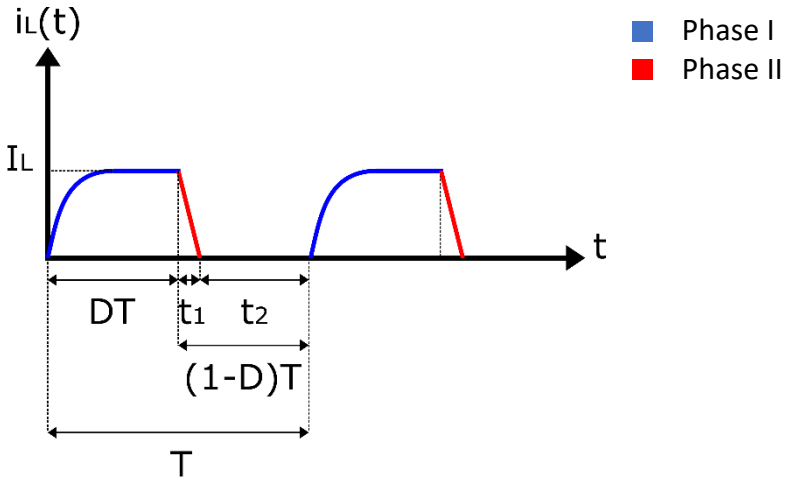


Figure 27. Inductor current waveform with respect to time, of the DCM boost converter

Where,
D = Duty cycle of operation
T = Time period of operation

From the figure above, some assumptions are made as follows:

a. Steady state operation is considered for this derivation for the output voltage of the boost converter.

b. Since the inductor current $i_L(t)$ in Phase I almost covers the entire square formed by I_L & DT, it is assumed to be constant throughout Phase I with a value of *'I_L'*.
c. In Phase II, the inductor current $i_L(t)$ falls sharply as it charges the capacitor and thus, its waveform is assumed to form a right-angled triangle with sides I_L & t_1, with an average value of *'$I_L/2$'*.

During Phase I, the input voltage source provides energy to the inductor that stores it in the form of a current while a part of the source's energy is also wasted/dissipated in the resistors R_S & R_{S1}. The time period for which this phase runs is *'DT'*, where *'D'* is the duty cycle and *'T'* is the time period of operation. Thus,

$$V.I_L.DT = \frac{1}{2}LI_L{}^2 + I_L{}^2.(R_S + R_{S1}).DT \tag{10}$$

implying,

$$I_L = \frac{2.V_{IN}.DT}{L+2(R_S+R_{S1})DT} \tag{11}$$

Also in Phase I, the output capacitor provides the load current to R_L for time *'t_2 + DT'* or *'$T - t_1$'*. Therefore, final charge, *'Q_F'*, left on the capacitor after this time, assuming the capacitor was charged to a voltage *'V_O'* in the previous phase, is calculated in equation (12) as:

$$Q_F = CV_O - \frac{V_O}{R_L}(T - t_1) \tag{12}$$

Phase II operation is shown in figure 28 as:

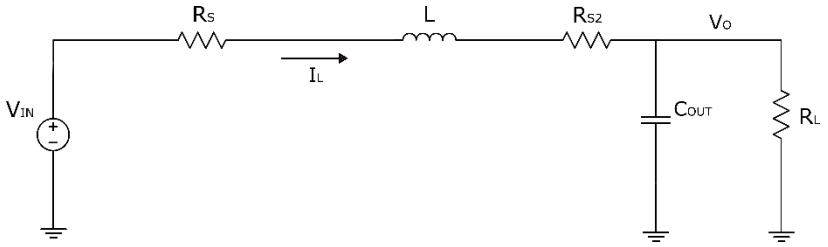


Figure 28. Phase II of boost converter operation, runs for time *'(1-D)T'*

During Phase II, the inductor current will charge the output capacitor for time *'t_1'* from *'V_F (= Q_F/C)'* to *'V_O'* or *'Q_F'* to *'Q_O (= CV_O)'*. Moreover, during this time a part of the inductor current also maintains a constant output voltage of *'V_O'* across the load R_L. Hence,

$$\frac{I_L}{2} - \frac{V_O}{R_L} = \frac{C(V_O - V_F)}{t_1} \tag{13}$$

Thus, the time for which the output capacitor charges, *'t_1'*, can be found in equation (14) as,

$$t_1 = \frac{2V_O T}{I_L R_L} \tag{14}$$

In Phase II, the input voltage source and the inductor provide energy to the output capacitor and the load while a part of this energy is also dissipated in resistors R_S & R_{S2}, given in equation (15) as:

$$\frac{1}{2}V_{IN}.I_L.t_1 + \frac{1}{2}LI_L{}^2 = \frac{1}{2}CV_O{}^2 + \frac{I_L{}^2}{4}.(R_S + R_{S2}).t_1 + \frac{V_O{}^2}{R_L}t_1 \tag{15}$$

Solving the above equation would provide the value of output voltage V_O as recorded in equation (16):

$$V_O = \frac{-\left(\frac{T}{CR_L}\right).\left(\frac{I_L}{2}(R_S+R_{S2}+R_L)-V_{IN}\right)+\sqrt{\left(\frac{T}{CR_L}\right)^2.\left(\frac{I_L}{2}(R_S+R_{S2}+R_L)-V_{IN}\right)^2+\frac{4LI_L^2}{C}}}{2} \tag{16}$$

Since the load R_L is assumed to be very large here, as initially the output capacitor will not be connected to the load, the contribution of the last term in equation (15) to the overall losses in phase II of operation can be taken as null. Also, since the duration for time *'t_1'* is found to be in the order of 10 ps, the contribution of 'R_S & R_{S2}' term can also be safely taken as null, given that 'I_L' is also pretty small. The simplified for of *'V_O'* thus obtained is illustrated in equation (17) as:

$$V_O = \left(\frac{TV_{IN}}{CR_L}\right) + \sqrt{\left(\frac{TV_{IN}}{CR_L}\right)^2 + \frac{LI_L^2}{C}} \tag{17}$$

Now, that the equation of output voltage *'V_O'* is derived, it can be employed to extract the values of all the variables of the aforementioned boost converter. Please note, that since R_L is assumed to be very large, the contribution of the first & second term of equation (17) is negligible. However, before proceeding on to the actual calculations, lets have a look at what equation (17) has in offer with respect to variations in different parameters of the converter. Following points tend to illustrate this, as:

1. Boost Converter output voltage variation with VCS parasitic resistance R_{S1}
   Figure 29 shows how the output voltage of the non-ideal boost converter derived above varies with changing R_{S1} value:

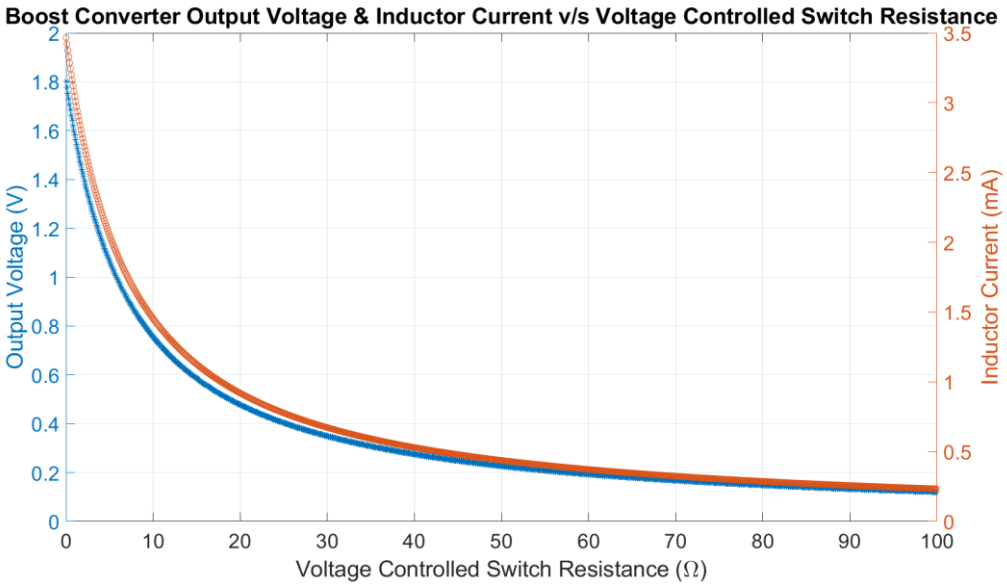


Figure 29. Output voltage & inductor charging current variation with VCS 'ON' resistance

   As can be noted from the figure above, the output voltage and the inductor charging current as well reduces quite drastically as R_{S1} increases. This is due to the fact that as R_{S1} rises, the voltage drop across it rises during Phase I and consequently the inductor has a very small voltage difference across it to build up a current. Thus, a smaller value of inductor current results as R_{S1} rises in Phase I, which charges the output capacitor with an equally small energy in Phase II and subsequently, a smaller output voltage results. In this work the gate-source voltage driving the VCS NMOS-T is 320 mV (would be discussed later in the proceeding sections) which transforms to the VCS having an 'ON' resistance of 25 Ω, with the assumed W/L.

2. Boost converter output voltage variation with inductor value
   Figure 30 displays the variation in output voltage and inductor current with changing inductor value:

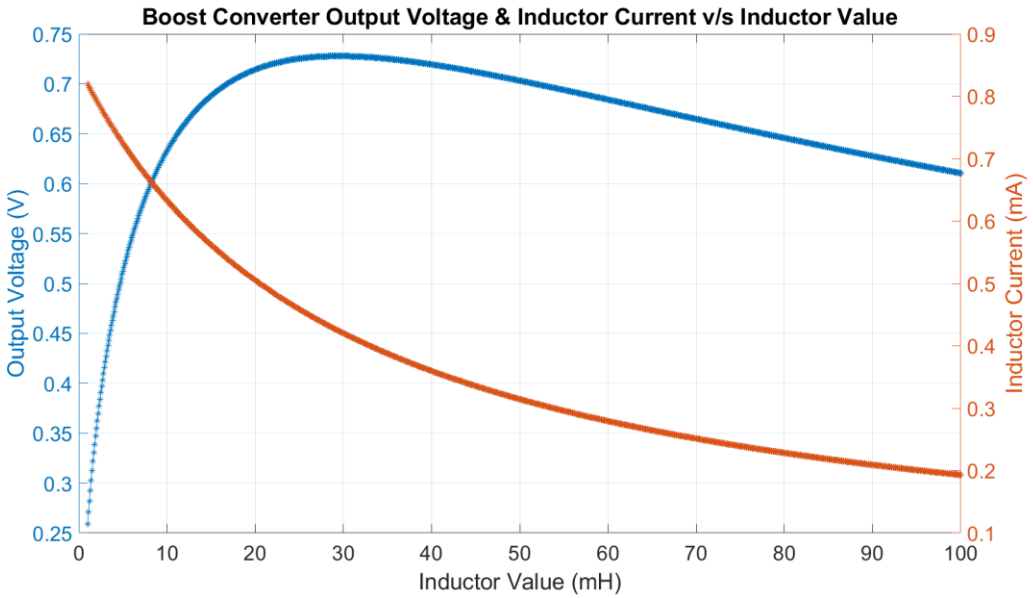


Figure 30. Output voltage & inductor charging current variation with inductor value

From the figure above, it can be seen that the inductor current as expected decreases with rising inductor value, however, the output voltage first rises to a value of about 28 mH and then it begins to fall with rising inductor value. Initially when the inductor gets big (value rises) it stores a higher magnetic energy (due to higher magnetic flux), thus, a larger energy is delivered to the output capacitor. This changes when the inductor current falls too low and the inductor is not able to build and even deliver the energy it has built, to the output capacitor forcing the output voltage to fall as well, i.e. after the plotted value of 28 mH in this case. Being an off-chip component, inductor size is limited to how much can be fit in a given wearable package and hence, its form factor is desired to be as small as possible. Thus, in this case an inductor with a value < 5 mH can be looked into to get sufficient output voltage at reasonable form factor.

3. Boost converter output voltage variation with switching frequency
   Figure 31 depicts the variation in output voltage and inductor current with changing switching frequency:

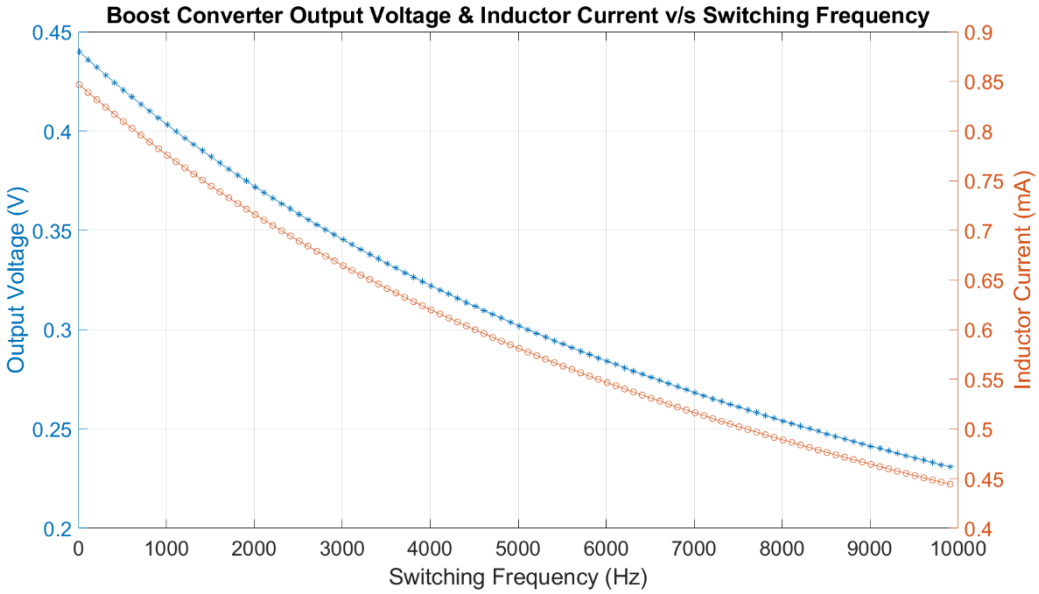


Figure 31. Output voltage & inductor charging current variation with switching frequency

It can be observed from the figure above, that as the switching frequency increases the output voltage as well as the inductor charging current decreases. This is as expected since the inductor being quite big, as was discussed previously, will not be able to follow the switching frequency if

it gets too large. Thus, for higher switching speeds, the inductor may not be able to charge to a sufficient current value which would in turn deposit a smaller amount of charge at the output capacitor, forcing the output voltage to reduce. Hence, attention must be paid while selecting a specific switching frequency as lower switching rates can make the entire converter equally slow, compelling the wearer to wait for considerable amount of time before the sensor starts. Switching frequency values of about 1000 Hz seem to be quite favourable in this regard.

4. Boost converter output voltage variation with switching frequency at different inductor values
   Figure 32 presents the variation in output voltage with the said parameters:

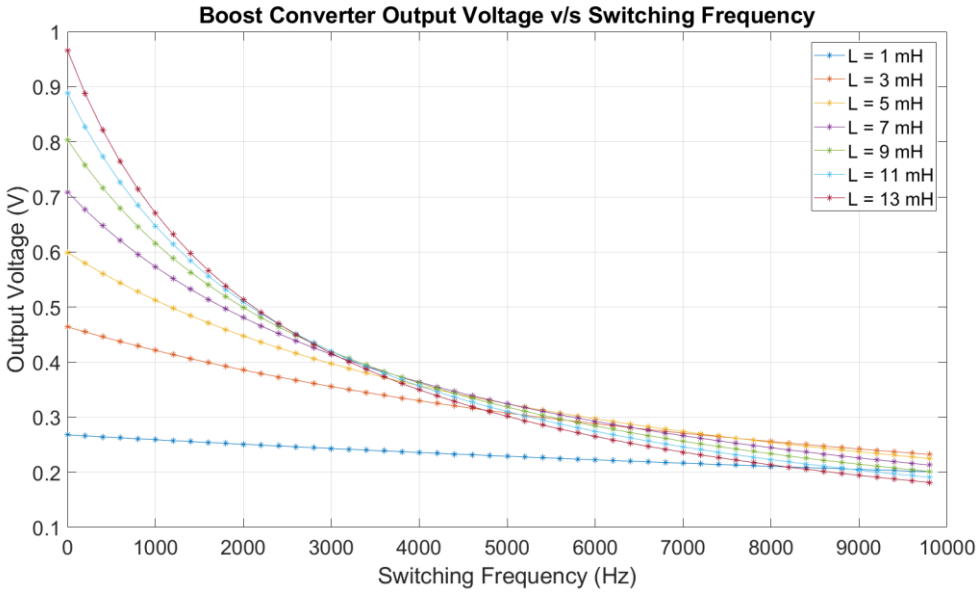


Figure 32. Output voltage variation with switching frequency at different inductor values

From the figure above, it can be viewed that the output voltage decreases with increasing frequency and decreasing inductor value initially while there is a sharp decline in output voltage with increasing frequency and inductor value as well later on. Also, worth noting is the fact that there is not much variation in the output voltage where inductor values are much lower i.e. around 3 mH. This is also as expected, since for smaller inductors, following the frequency is much easier at higher switching speeds, as being small they can only store as much energy and to charge to those current values, as such, they take considerably less time.

5. Boost converter output voltage variation with changing inductor values at different switching frequency
   Figure 33 illustrates the variation in output voltage with the said parameters:

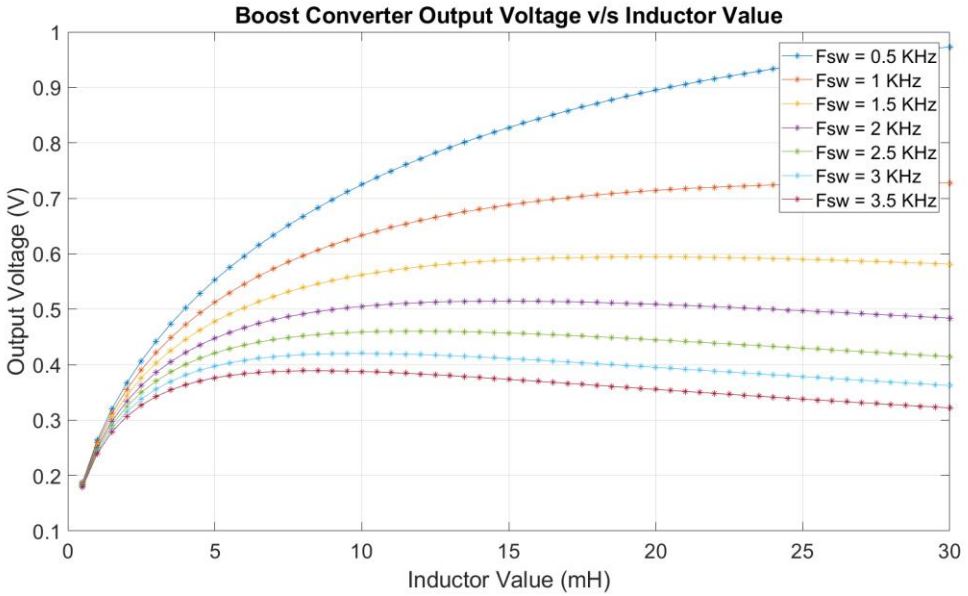


Figure 33. Output voltage variation with switching frequency at different inductor values

From the figure above, it may be noted that for lower inductor values around 3 mH, the output voltage of the boost converter does not vary to any considerable extent for even a wide range of frequencies, for reasons explained previously. This could be particularly beneficial to the proposed design process since the frequency output of the timing generator employed here can vary drastically across process corners and can easily spread across the expanse of the frequency values showed in the figure above. Thus, low inductor values (~ 3 mH) would be preferred.

Hence, from the illustrations and their discussion above, for the proceeding design process following parameter values are assumed as:

a. **Inductor value** – *2.7 mH*. This was preferred over a 3 mH inductor since it has a smaller parasitic resistance (1.8 Ω) and comes at a slightly lower form-factor with almost the same performance.
b. **Switching frequency** – *1000 Hz.*
c. **VCS W/L** – *W = 200 um* (gate parasitic capacitance for a greater value could not be driven by the Cold Start-up circuit), *L = 300 nm* (kept at the minimum possible value for a low-V_{TH} NMOS-T).
d. **SCS W/L** – *W = 200 um & L = 180 nm*. Parasitic diode implementation of an NMOS-T discussed previously is used here for a higher I_{ON}/I_{OFF} ratio at low applied voltages. W is kept large & L is kept minimal, to ensure a higher I_{ON} and faster output capacitor charging.
e. **Capacitance value** – *100 nF*. Although it makes the converter slower than lower values, this is done to ensure that the capacitor has enough charge to cater to the bootstrap feedback and the load simultaneously.
f. **Output voltage before feedback** – *400 mV*. With the selected values as mentioned above, this voltage is highly attainable, along with a reduced period of time to reach at such a point (verified through simulations).

4.2. RVM (Rectifier-cum-Voltage Multiplier) Design

As has been discussed in Chapter 3 - Section 3.1 with due consideration to design nuances, the single-phase Dickson RVM topology has been selected to be implemented as a suitable RVM methodology.

Let's start with listing the input conditions to the DRVM or PEH output specifications first as specified in Table XIV as:

TABLE XIV. PEH output specifications

Parameter	Value (Expected)
Excitation Frequency	1 Hz – 10 Hz
V_{IN} @ 1st Harmonic (2.5 Hz)	300 mV
Power Output	1 nW (max)

Now that the input specifications to the RVM are determined, the expected RVM output parameters can be set, as given in Table XV as:

TABLE XV. RVM output specifications

Parameter	Value (Expected)
V_{OUT}	320 mV
Current Output	100 pA (min)
No. of Cycles to Start Oscillation	2 (optimistic min)
No. of Cycles to Pass VLD	2 (optimistic min)

It may be worthwhile to note that in terms of the minimum voltage required to run the timing generator, from the PEH, the limitation stands as:

$$V_{GS} - V_{TH} \geq 70\ mV \tag{18}$$

The equation (9) implying that the voltage delivered to the gate of the VCS MOS-T (main boost converter) by the timing generator should be sufficient enough to at-least drive it at the edge of weak and strong inversion (to a first order approximation). Such a value of V_{GS} would make sure a higher amount of current flows through the VCS MOS-T with as low an $R_{DS,ON}$ as possible, to ensure ultra low power (& low-voltage) operation of PEH, making it suitable for the proposed application. Since the V_{TH} of the VCS MOS-T is around 250 mV, the average output voltage of the DRVM is expected to be around 320 mV DC. This voltage would supply the timing generator which in turn would ensure the same supply voltage appears at the gate of VCS MOS-T in a clocked fashion.

No. of cycles to cross VLD or pass the VLD check is a crucial parameter in determining the speed of the cold start-up circuit. Too many no. of cycles would make the system too slow to be of any practical relevance. Thus, a maximum of 2 cycles is selected to ensure the cold start-up system wakes up at the earliest, i.e., ~ 0.8 s to PEH excitation.

Similarly, the expected no. of cycles to start the timing generator also plays an important role in determining how long will the system take to charge the main boost converter's output. Thus, a maximum of 2 cycles is selected to start the timing generator, essentially meaning that once the VLD passes the output voltage of the RVM, the oscillations should start almost instantaneously. This would ascertain that the output capacitor starts to charge right after these 2 cycles, i.e., ~ 0.8 s.

Now, for a given DRVM with respect to the input and output conditions, the values of the various constituents such as the pumping and the storage capacitors can be derived. Literature [33] presents such a complexity into a one line equation (10) that could be easily played with to get an approximate measure of those values, as:

$$V_{DD} = V_{IN} + N\left[\left(\frac{C_{VD}}{C_{VD}+C_P}\right)V_L - 2V_D\right] - \frac{N \times I_{DD}}{(C_{VD}+C_P)f} \tag{19}$$

This equation is for an N stage single-phase Dickson RVM, given C_{VD} as pumping & storage capacitance, I_{DD} as current drawn, V_L as input AC voltage (pk-pk), V_{IN} as applied DC bias, C_P as parasitic capacitance of diode, V_D as diode voltage drop, f as frequency of operation.

As can be observed as,

$$C_{VD} \propto {I_{DD}}/{f.V_L}$$
$$C_{VD} \propto V_D,\ C_{VD} \propto V_{DD}$$

thus, greater the expected output voltage with lower input (AC & DC) voltage and frequency of operation, higher will be the value of C_{VD} & N. Moreover, greater the expected output current with lower input (AC & DC) voltage and frequency of operation, higher will be the value of C_{VD} & N, as is also evidenced in Table XVI:

TABLE XVI. Dependence of V_{DD} & I_{DD} on C_{VD}, V_{IN} & f, from literature

Work	Phase	Excitation	Frequency	V_L (V_{IN})	V_{DD}	I_{DD}	N	C_{VD}
[33]	Single	Sinusoidal	5MHz	400mV (40mV)	1V	<21nA	10	2.4pF
[34]	Two	Sinusoidal	30MHz	90mV (0 V)	300mV	500nA	12	0.46pF
[32]	Two	Pulse	1kHz	60mV (60mV)	600mV	1nA	40	40pF

Thus, a lower input (AC & DC) voltage at an extremely lower frequency will have a major consequence on the chip-area due to an increased pumping and storage capacitance needed to produce the required output voltage. Furthermore, it will also have a stringent effect on the output current that can be drawn, exerting a limitation on the succeeding circuitry to work at lower currents. This is going to be the case for this project. The factor 'N' plays a role in deciding the output parameters too, but larger this factor, more will be the capacitors, so, greater will be the chip-area.

Table XVII depicts the design choices that can be obtained from the above expression:

TABLE XVII. Design parameters for DRVM

Frequency	N	V_L (mV_{PP})	V_{DD} (mV)	I_{DD} (nA)	C_{VD} (pF)	Chip-Area (mm^2) 2 X N X C_{VD}
2.5 Hz	1	600	320	0.12	600	0.6
	1	600	320	0.2	1000	1
	2	600	320	0.12	200	0.4
	2	600	320	0.2	333	0.66
	3	600	320	0.12	160	0.48
	3	600	320	0.2	272	0.8
	5	600	320	1	1190	5.95

Please Note:
1. The above table assumes V_D = 100 mV.
2. Chip-area is calculated assuming MIM capacitors with capacitance to area ratio as $2nF/mm^2$.

Hence, as has been recorded in the table above, designing the DRVM for the required output voltage and a higher value of current could incur larger chip-areas that may increase the cost of production. This may still be an underestimation as the voltage drop V_D could still be higher, the effect of parasitic is not yet taken into account and the behaviour of the MOS-T parasitic diodes (or for that matter any diode) is not modelled in equation (10) as it assumes an ideal diode. This is to say that the exponential relationship that the voltage across the diode has with the current flowing through it is not modelled, rather a mechanical ON/OFF behaviour has been assumed to derive equation (10).

And as was expected from the discussion above, the values calculated from the table XVII did not hold when operated on the simulator. The assumptions too fell short when considered with the real parasitic effects suffered, for ex. the value of VD turned out to be 124 mV. Moreover, parasitic capacitances decreased the output voltage and the MOS-T parasitic diode I-V relationship along with the reverse leakage currents too severely effected the output voltage driving a 120 pA current sink.

Following this deliberation, the optimum design parameters were found to be as follows in Table XVIII:

TABLE XVIII. Optimum design parameters for DRVM

Frequency	N	V_L (mV_{PP})	V_{DD} (mV)	I_{DD} (nA)	C_{VD} (pF)	Chip-Area (mm^2)
2.5 Hz	2	600	320	0.12	300	0.6

And verified in simulations as:

Figure 34 below depicts the circuit schematic of the 2-Stage DRVM:

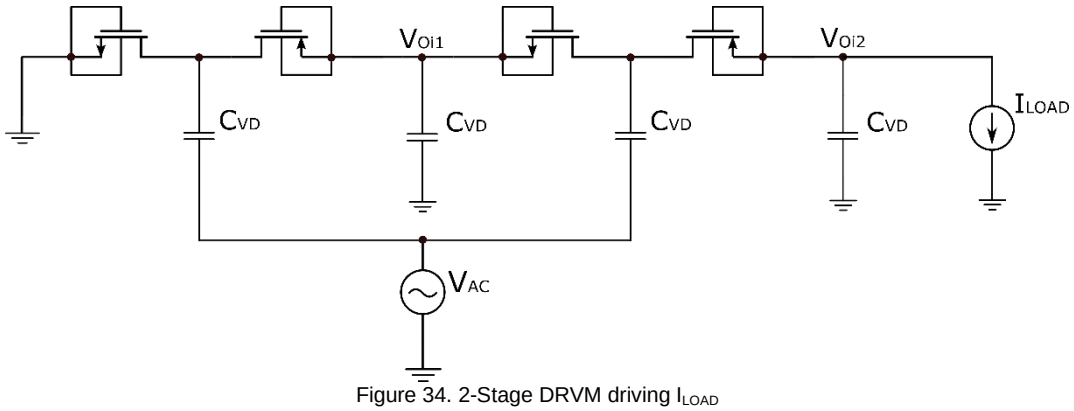


Figure 34. 2-Stage DRVM driving I_{LOAD}

Figure 35 below shows the output waveform of the 2-Stage DRVM driving 120 pA load, note that the load is switched at a point where the output voltage is expected to pass the VLD test of $V_{OUT} > 250$ mV.

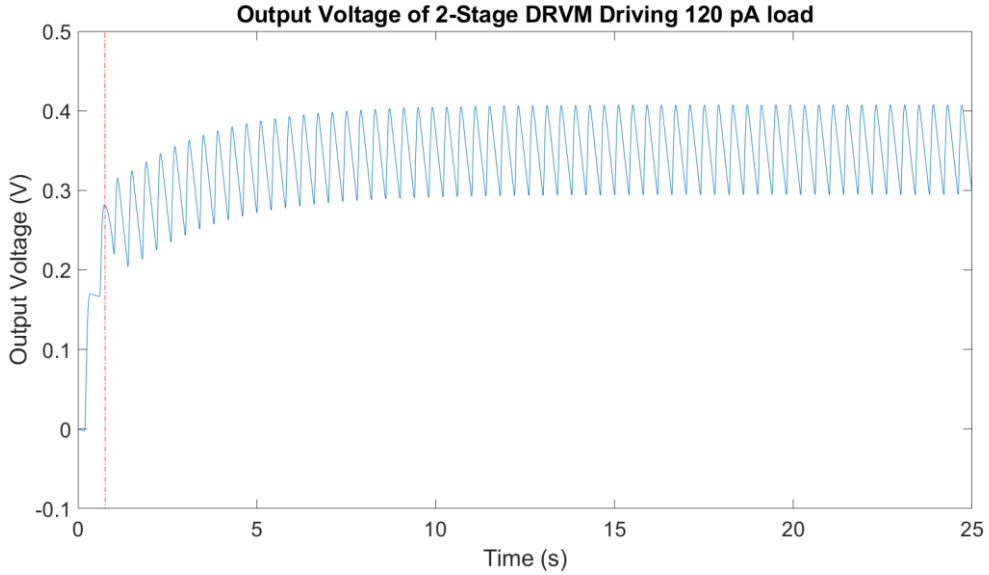


Figure 35. Output voltage of 2-Stage DRVM driving 120 pA load. The red line depicts the point at which the load is switched 'ON'.

As can be observed from the figure above, the DRVM can pass the VLD check in less than two cycles (730 ms) and start the oscillations of the timing generator satisfying the set target. It may be worthwhile to note that the average output voltage in the first 10 seconds is 327.4 mV which also does satisfy the output voltage requirements of the DRVM stage. Besides, as one may note that the ripple is quite large, as long as the lower value of the ripple is such that the DRVM output could still switch 'ON' the VCS of the boost converter, increasing the capacitance as well as the chip-area might be avoided. For 1-Stage & 3-Stage DRVM, while both could pass the VLD check in similar number of cycles, the average output voltage was less than what was desired in the first 10 seconds period. 1-Stage cannot be preferred as starting-up the system for such cases can be critical to the cold start-up architecture, for random PEH excitations that decay very quickly, and thus would need to be boosted to higher ratios, if not for the first excitation cycle (assuming sufficiently large) then for the lower amplitude excitation cycles that follow it. 3-Stage cannot be preferred as it would lead to a higher chip-area and would take a longer period of time

to achieve the desired average value and since it has 3 stages, would not be capable of supporting high output load currents. At this point, it may be worthwhile to note, assuming an ideal case of power transfer in a DRVM, the output current decreases as the output voltage increases with the no. of stages, since power is conserved. Thus, for cases of high output voltages, considering power loss due to reverse leakage and diode drops, it would not be a good idea to execute a 3-Stage DRVM when power is a scarcity.

The PEH excitation frequency severely limits the amount of current that can be drawn from the DRVM. Moreover, Due to the area overhead that would be incurred, drawing currents any higher than 120 pA could impede the performance severely. This is the reason none of the works in literature have ever focused on using the PEH for such ultra-low frequencies, specially since there isn't any PEH available in the community that could resonate at such frequencies, providing a really large (~1-2V) output, or have a high enough Q-factor to vibrate the PEH at its resonance frequency from such 'near' DC frequency excitations.

Before proceeding forward, it is crucial to simulate how this DRVM would perform with regards to different process corners with the same input voltage of 300 mV_{PEAK} and load current of 120 pA, as is depicted in Table XIX:

TABLE XIX. Process corner simulation for 2-Stage DRVM

Process Corner	$V_{OUT(avg)}$ (First 10 seconds)
TT	327.4 mV
FF	367.8 mV
SS	266.9 mV
SF	324.1 mV
FS	317.5 mV

The total variation in V_{OUT} with regards to all the process corners is 100.9 mV which can be accounted for later on.
It may be worthwhile to note that since a current load of 120 pA is identified as the maximum load that can be driven by the DRVM, a margin > 25% would be taken in due consideration while designing the succeeding stages to allow for unexpected and non-ideal variations. Thus, the succeeding stages will be so designed to consume 90 pA of current.

Also equally important is to analyse how much load current can the 2-Stage DRVM support if the first 2-Harmonics i.e., 2.5 Hz & 5 Hz, of the PEH were to be used to excite the DRVM configuration, as is shown in Table XX as:

TABLE XX. 2-Harmonic excited 2-Stage DRVM output specification

Frequency	N	V_L (mV_{PP}) 2.5 Hz + 5 Hz	V_{DD} (mV)	I_{DD} (nA)	C_{VD} (pF)	Chip-Area (mm^2)
2.5 Hz + 5 Hz	2	600 + 200	321.8	0.16	300	0.6

4.3. VLD (Voltage Level Detector) Design

Following the discussion on a comparator that could check the DRVM output voltage for being sufficient enough to power the timing generator and the VCS MOS-T, while consuming ultra-low power, ideally < 10 pW, a 2T based VLD configuration was selected.

Lets begin by defining the expected output parameters of the VLD as shown in Table XXI:

TABLE XXI. VLD output specifications

Parameter	Value (Expected)
V_{DETECT}	250 mV
Peak Current Consumption	5 pA (optimistic max)
Power Consumption	5 pW (optimistic max)

The current consumption is kept at bare minimal such that the VLD wouldn't drain unnecessary current out of the DRVM which may hinder the operation of the timing generator, current being a scarce and vital quantity here.

Peak current consumption is the point where the input voltage passes the VLD check, i.e., V_{IN} ~ 250mV, after which the current consumption of the VLD drops sharply. Max. power consumption is calculated as the max. voltage expected to pass through the VLD times the current at that point (lower than peak current @ V_{DETECT}).

Design procedure for such a circuit involves sizing the two transistor that form the independent and voltage-dependent current sources as discussed in Chapter 3 – Section 3.4. Figure 36 shows one such 2T VLD with PMOS-T M_1 being a voltage-dependent current source with current I_{DEP} and PMOS-T M_2 acting like an independent current source with a current I_{SAT}, being forced to operate in the cut-off region. A complete PMOS-T config. is selected as it is more resistant to process variations than its PMOS-T-NMOS-T counterpart [49].

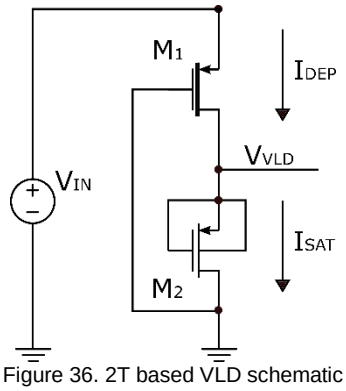


Figure 36. 2T based VLD schematic

[49] outlines the procedure to design such 2T VLDs as:

1. The voltage V_{DETECT} is calculated at the point where $I_{DEP} = I_{SAT}$. Note that the entire circuit is operating in the weak-inversion region, hence the current through the MOS-Ts M1 & M2 are, in equation (11) & (12):

$$I_{DEP} = \frac{W_1}{L_1} I_{01} e^{\frac{V_{IN} - V_{TH}}{nV_t}} \tag{20}$$

$$I_{SAT} = \frac{W_2}{L_2} I_{02} e^{\frac{-V_{TH}}{nV_t}} \tag{21}$$

   The current I_{DEP} of M_1 has an exponential relation to the input voltage V_{IN}, while for M_2, by connecting the gate to the source, thus, forcing V_{GS}=0 V, the current I_{SAT} is essentially kept constant. Note that I_{SAT} can be easily tuned by varying M_2's size (W_2 & L_2). Hence, I_{SAT} acts as an independent current source and I_{DEP} acts as a voltage dependent current source. Moreover, since the MOS-Ts M_1 & M_2 may not be of the same $V_{THRESHOLD}$, thus, they have different characteristic currents I_{01} & I_{02} respectively. The above equations are in a simplified form where the effect of V_{DS} is not taken into effect, assuming V_{DS} is sufficiently large to allow this postulation.

2. The voltage V_{DETECT} is found by equating equations (11) & (12) as given in equation (13):

$$V_{DETECT} = V_{IN} = nV_t . ln\left[\left(\frac{W_2}{L_2}\right).\left(\frac{L_1}{W_1}\right).\left(\frac{I_{02}}{I_{01}}\right)\right] \quad (22)$$

As can be observed from equation (13), the value of V_{DETECT} depends on the ratio of the sizes of MOS-Ts M_2 & M_1 respectively. Moreover, since the two MOS-Ts have different characteristic currents, their ratios also play a role in determining V_{DETECT}. It may be worthwhile to note here, that if the MOS-T M_1 is selected to be a high-V_{TH} device, i.e., I_{01} is lower than I_{02}, the ratio of the sizes of MOS-Ts M_2 & M_1 can be decreased to a lower value to achieve the same V_{DETECT}. This could be specially useful in cases where V_{DETECT} has to be designed for higher voltages, which also happens to be the case for this project. Besides, having a high-V_{TH} device as M_1 would also reduce the current consumption of the circuit configuration. One other thing to note is the dependence of V_{DETECT} on the temperature as $V_{DETECT} \propto V_t$ or KT/q, thus, essentially meaning V_{DETECT} would vary with temperature. Although, since the presented application is supposed to cater to human-body wearable scenarios, temperature variation is not considered to be of much concern.

Following the procedure above, the selected length and width of the 2T circuit is depicted in Table XXII as:

TABLE XXII. Width & Length of MOS-Ts M_1 & M_2

MOS-T	Parameter	Value
M_1 (HVTMOS)	W_1	300 nm
	L_1	1.75 um
M_2 (NVTMOS)	W_2	300 nm
	L_2	1 um

Now that the length and width of the devices are confirmed, simulations can be performed as follows:

Figure 37 shows the circuit diagram of the 2T VLD succeeded by two buffer stages, composed of HVTMOS, so as to prevent any unnecessary loading that may deteriorate the performance of the configuration:

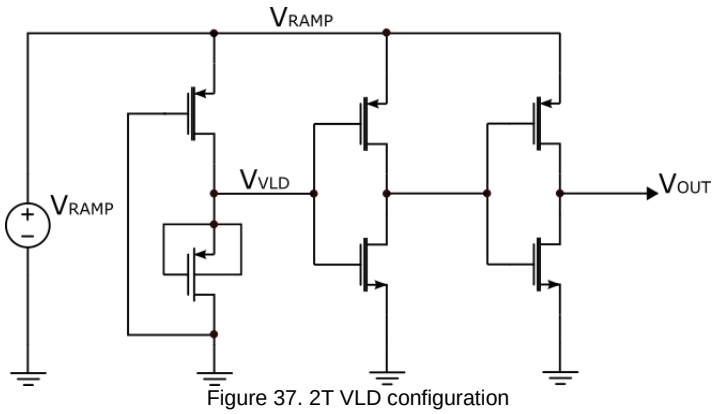


Figure 37. 2T VLD configuration

Note that the input voltage is a ramp waveform V_{RAMP}, that allows to accurately observe the point at which the voltage level is detected and trace the current consumption at different instances of the rising input voltage.

Figure 38 displays the simulation result of the proposed 2T VLD as:

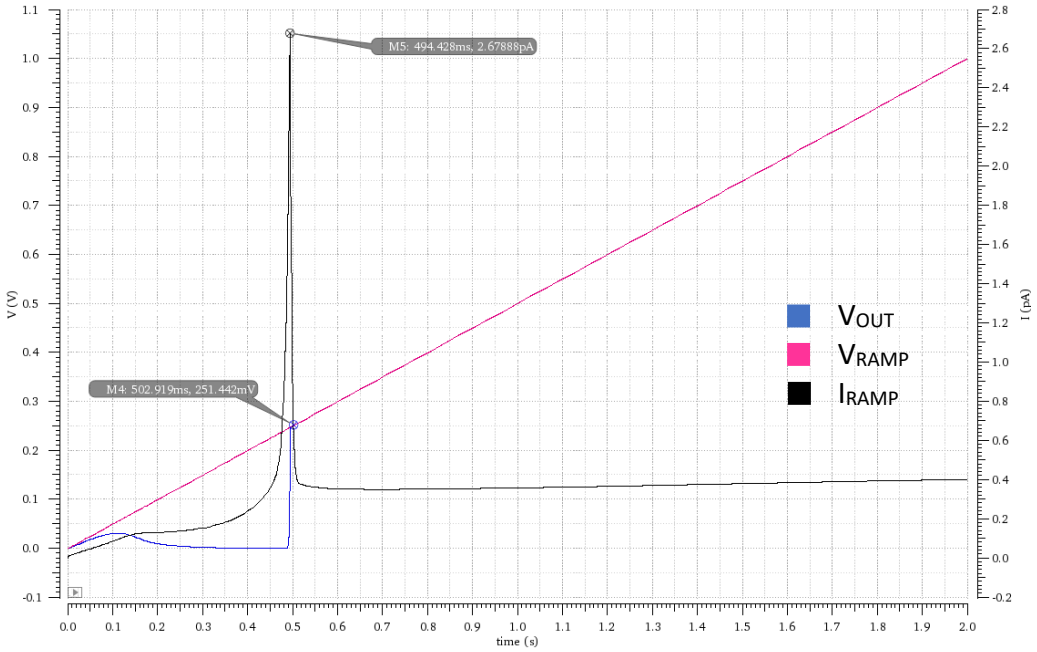


Figure 38. Simulation result of the proposed 2T VLD with V_{DETECT} = 251.44 mV

It may be worthwhile to note the effect of process variations at different process corners in order to ascertain whether the circuit would be able to execute as per expectations, as given in Table XXIII as:

TABLE XXIII. Circuit performance under different process corners

Process Corner	V_{DETECT} (mV)	I_{PEAK} (pA)
TT	251.44	2.68
FF	245	13.5
SS	270	1
SF	275.5	4.9
FS	225.7	1.62

The total variation in all the process corners with respect to V_{DETECT} is ΔV_{DETECT} = 49.8 mV and with respect to the peak current consumption is ΔI_{Peak} = 12.5 pA. This turns out to be acceptable and the succeeding circuits would be tuned to account for sufficient margins, specially with current loading. It would be worthwhile to note that the peak power consumption of this circuit, at the point of detection, is 0.67 pW (TT corner).

4.4. Design for Self-Reconfigurability

The proposed 'Concept of Self-Reconfigurability' states that depending upon the varying input voltage amplitude and the required output voltage amplitude (assumed to be fixed in the presented case), the stages of a DRVM would reconfigure themselves in series or in parallel to support the required output specifications of voltage and current, without the need for complex logic or DSP controllers. The circuit is designed in a manner such that it could essentially 'sense and react' with respect to the input conditions, to provide a calibrated output.

Consider for instance, a setting where with respect to the output voltage and current load conditions, at a given input voltage the DRVM stages would need to be all in series. Here, two different case scenarios can arise with regards to the changing input voltage due to random PEH excitations and output loading conditions due to any of PVT variations:

1. Scenario – Random PEH excitation increases the DRVM input voltage amplitude:
   Lets consider a case where the PEH contributes to two different harmonics of sinusoidal excitation, such that the input voltage to the RVM is not just $V_{IN(2.5\ Hz)}$ = 300 mV_{PEAK} but also has

a component of $V_{IN(5\ Hz)}$ = 100 mV_{PEAK} as well. This scenario actually is the case that is assumed for this project, however, it could also serve as a means to perceive the operating principle of self-reconfigurability, as it is supposed to supply a load of slightly less than its maximum capacity.

Figure 39 shows the circuit schematic of the self-reconfigurable DRVM architecture (SR-DRVM) supplying a 150 pA load.

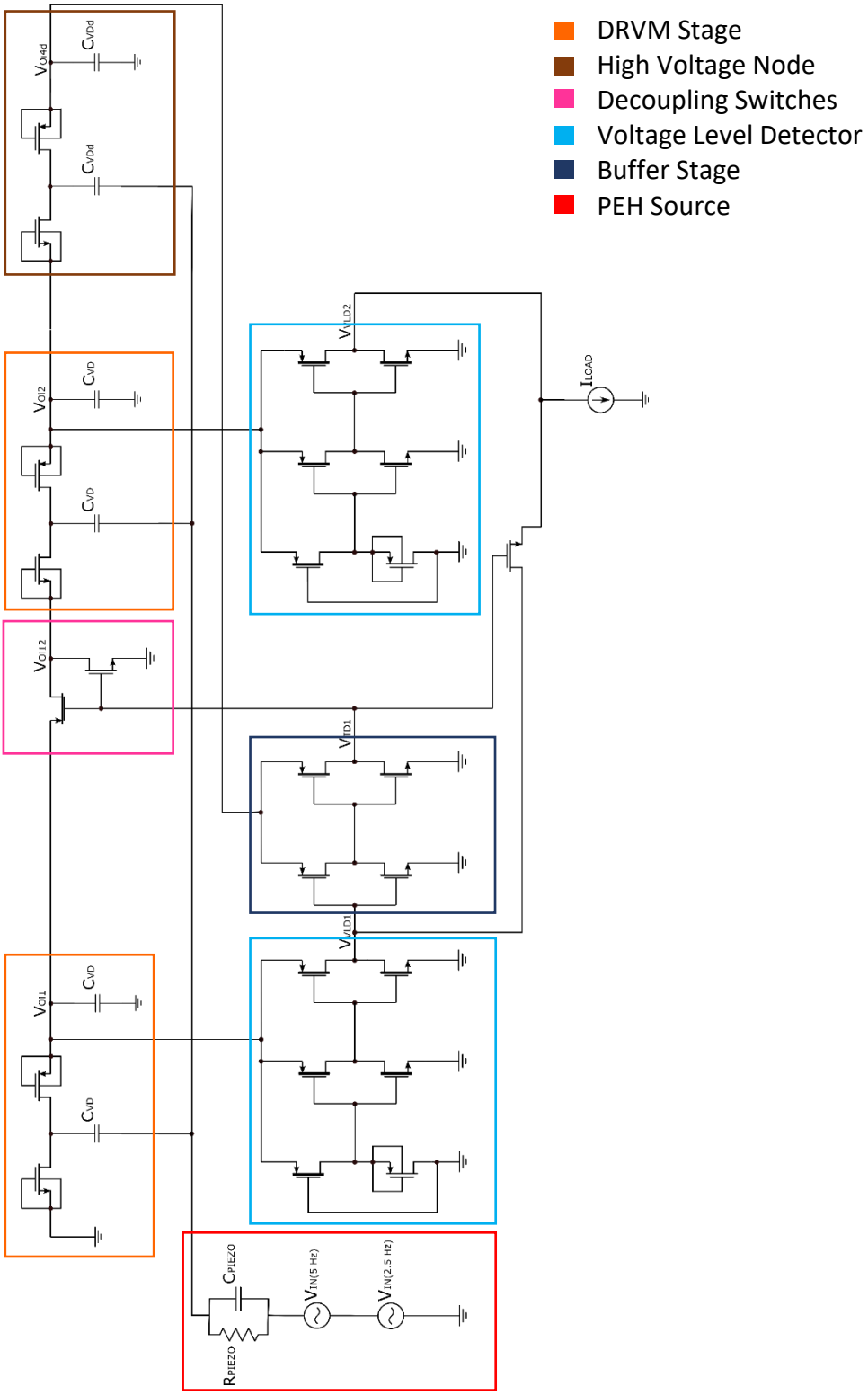


Figure 39. Circuit schematic of self-reconfigurable 2-Stage DRVM supplying 150 pA load with 2-Harmonic input excitation

Before proceeding further into the nitty-gritty details of this fancy concept, it might be of interest to note that there are indeed two circuit blocks in figure 30, that have not yet been introduced in this chapter. The first one is the decoupling switch (pink outline) composed of a Low-V_{TH} PMOS-T as SW1 and a Nominal-V_{TH} NMOS-T as SW2. The rationale for selecting the aforesaid threshold voltages of the above devices has already been discussed in Chapter 3 – Section 3.3. However, selection of the device itself, whether a PMOS-T or an NMOS-T, seeds from the fact that a Low-V_{TH} PMOS-T and a Nominal-V_{TH} NMOS-T need a high gate voltage to strongly turn 'OFF' and 'ON' respectively, which can be deftly generated on-chip. This could be convenient from a design perspective while incurring a lower overhead of reverse leakages and parasitics. In case of such roles being reversed, i.e., Low-V_{TH} NMOS-T being used as SW1 and Nominal-V_{TH} PMOS-T being used as SW2, turning the NMOS-T strongly 'ÓFF' and the PMOS-T strongly 'ON' would then demand a negative gate voltage. To generate it would imply a separate circuit altogether for negative-bias generation which could lead to increased reverse leakages and parasitics to take care of, in the wake of PVT variations for such ultra-low power applications. The reason why it is believed to be convenient for a designer to generate a high positive voltage is due to the fact that in effect the DRVM stages are exactly doing the same. Thus, getting a higher voltage would in essence translate to designing a third DRVM stage, all that would do is to provide a higher voltage node that could be used to control the decoupling switches without consuming, ideally speaking since it only has to drive the gate of SW1&2, any significant currents. Hence, any further increase in parasitic losses and reverse leakages can be avoided as this node only acts as an extra unlike an actual current-load driving stage. This brings us to the second circuit block in figure 30 that essentially is doing just this, i.e., being a high voltage node (brown outline) designed to drive the decoupling switches.

Figure 40 depicts the simulation result of the proposed SR-DRVM.

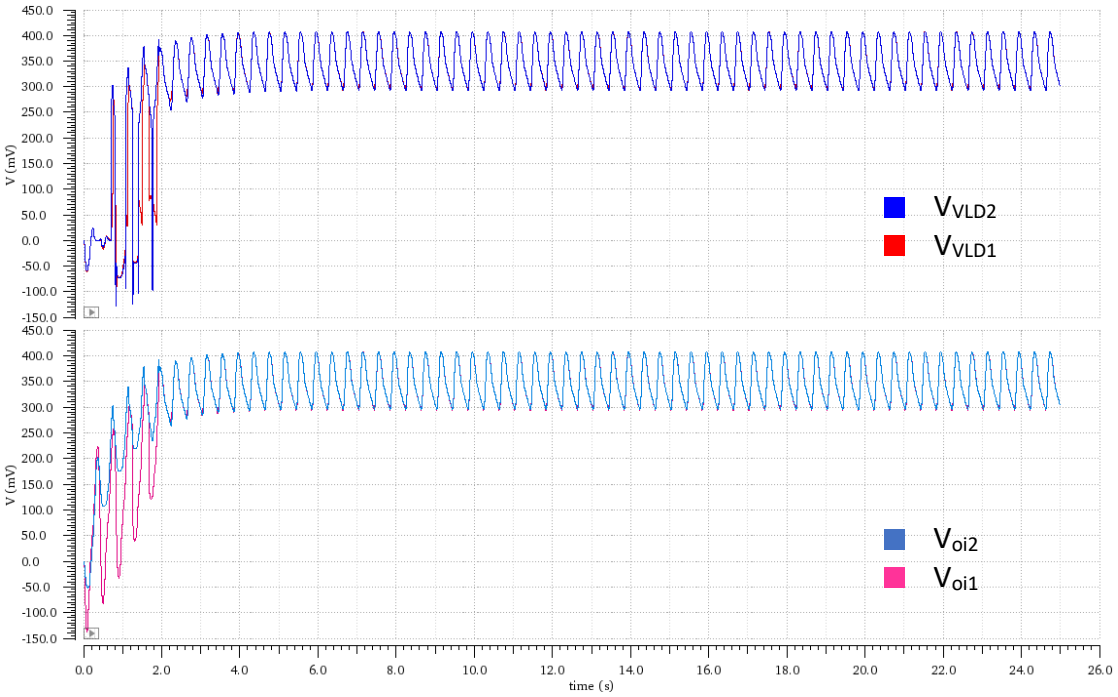


Figure 40. 2-Harmonic-input self-reconfigurable DRVM simulation result at constant load

As can be observed for the figure above, initially the two stages depicted by plots Voi1 and Voi2 are arranged in series. In this configuration, the DRVM architecture has an ideal gain of 2X, readily amplifying small input voltage amplitudes to the desired value in a short period of time. While for large input voltage amplitudes, as is shown in figure 31, after a certain period of time, 1.92 seconds here, the stage-1 output voltage Voi1 begins to follow the stage-2 output voltage Voi2 and eventually becomes equal, ascertaining that the two stages have indeed arranged themselves in parallel. Note that at this point, Vvld1 and Vvld2, the output voltages, after being checked and passed by the VLD, of the 1st and 2nd stage respectively, also have become equal implying that they both drive the load now. In this configuration, both the stages contribute equally to the load current and the voltage output for the entire DRVM architecture, depicted by Vvld2,

stabilizes at a point close to the vicinity of the desired output voltage. Hence, it can rightfully said that the self-reconfigurable DRVM architecture can be trusted to take care of input voltage variations while supplying a calibrated voltage to the output load. Additionally, bringing the two stages in parallel also prevents the DRVM architecture to produce large (2X) output voltages in cases of high impact PEH excitation, which could protect the gate-oxide of MOS-Ts from being damaged by unnecessarily large voltages. Arranging itself in different boosting ratios certainly performs a neat trick in this regard. It can be observed from figure 10.(c) that the largest voltage produced by the selected PEH due to a random excitation can be around 1 V, in which case the parallel configuration would ensure not more than a 1X voltage amplification while supplying the required current to the load. It may be of essence to note that a Current-Starved Ring Oscillator's (CSRO) current appetite increases as its supply voltage increases, which if not fed would lead to low 'gm' of the constituting MOS-Ts which might decrease the gain in turn, impeding any possibilities of sustained oscillations at all or the oscillations would be of very low-duty cycle. A low duty-cycle oscillation waveform results when the current is too low to charge the gate parasitic capacitance of the next stage MOS-T to the required level of the supply voltage, followed by this gate capacitor being drained of its charge in the very next cycle without even reaching anywhere close to the level of the high supply voltage. Therefore, if a large input voltage to the DRVM is amplified using a constant boosting ratio, the configuration may not be able to support the high current needs of the CSRO. While on the other hand, a parallel configuration allows for the DRVM stages to individually contribute to the load current while the output voltage is kept at ~ 1X amplification only.

Hence, a SR-DRVM architecture is well suited for random changes in the input voltage due to PEH excitation.

2. Scenario – Changing output load-conditions due to PVT variations

Being followed by a CSRO, which is known to exhibit large center-frequency deviations with regards to PVT variations, the cold start-up architecture is going to be equally very-susceptible to such variations. For a CSRO, frequency variation essentially means variation in the current consumption. Hence, if frequency varies by larger margins, say, for different process corners, the driving current too follows suit and can upset the design, if proper attention is not paid. For instance, current consumption of a CSRO in the FF process corner can increase ridiculously, due to the MOS-Ts strongly draining more I_{ON} and I_{OFF} currents, as compared to other corners. For trade-offs like chip-area & power, it could translate to more complicated designs. In light of this, the concept of self-reconfigurability is so designed such that the DRVM architecture is capable of supplying for varying output-load demands.

A noteworthy part of this proposed concept/architecture is the fact that it allows for load stepping. Load stepping is a technique where the output load is stepped up in a stair-like fashion from a lower value to a high value, with the no. of steps and the step-period being tunable for a given DRVM config. This technique in conjunction with the proposed architecture could allow for an adroit handling of loads, it otherwise was never capable of.

Figure 41 displays the circuit schematic for the SR-DRVM architecture sporting two current-loads of 100 pA each.

Note that the current-load I_{LOAD1} is switched 'ON' at 737 ms, i.e., when Voi2 passes the VLD check and the current-load I_{LOAD2} is switched 'ON' at 3 s to perform the load stepping resulting in a total load of 200 pA. This magnitude of current-load, as has been seen in Table XX, was way beyond the capabilities of a 2-Stage DRVM to support output requirements.

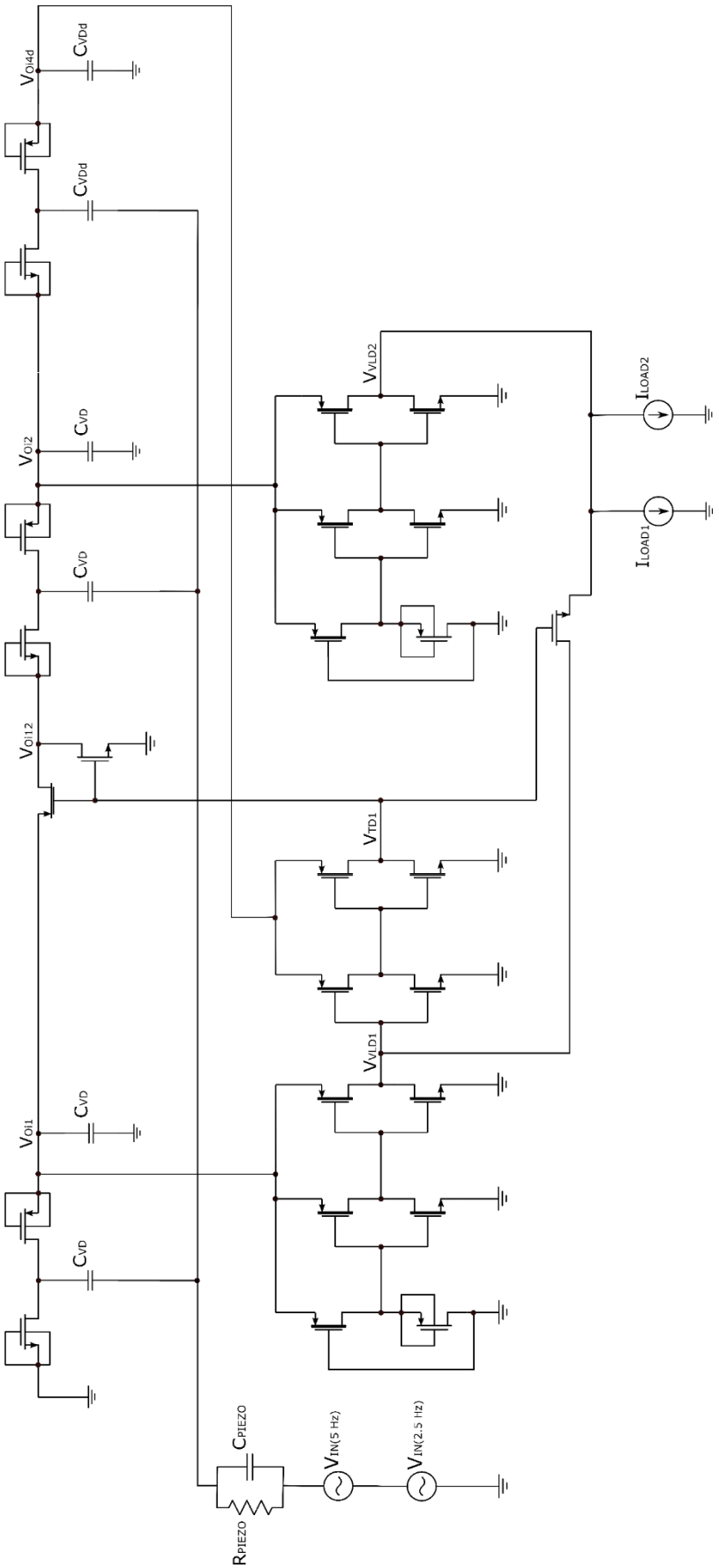


Figure 41. Circuit schematic of the self-reconfigurable DRVM architecture driving two current-loads of 100 pA each

Figure 42 shows the simulation result for the SR-DRVM architecture with two 100pA current-loads.

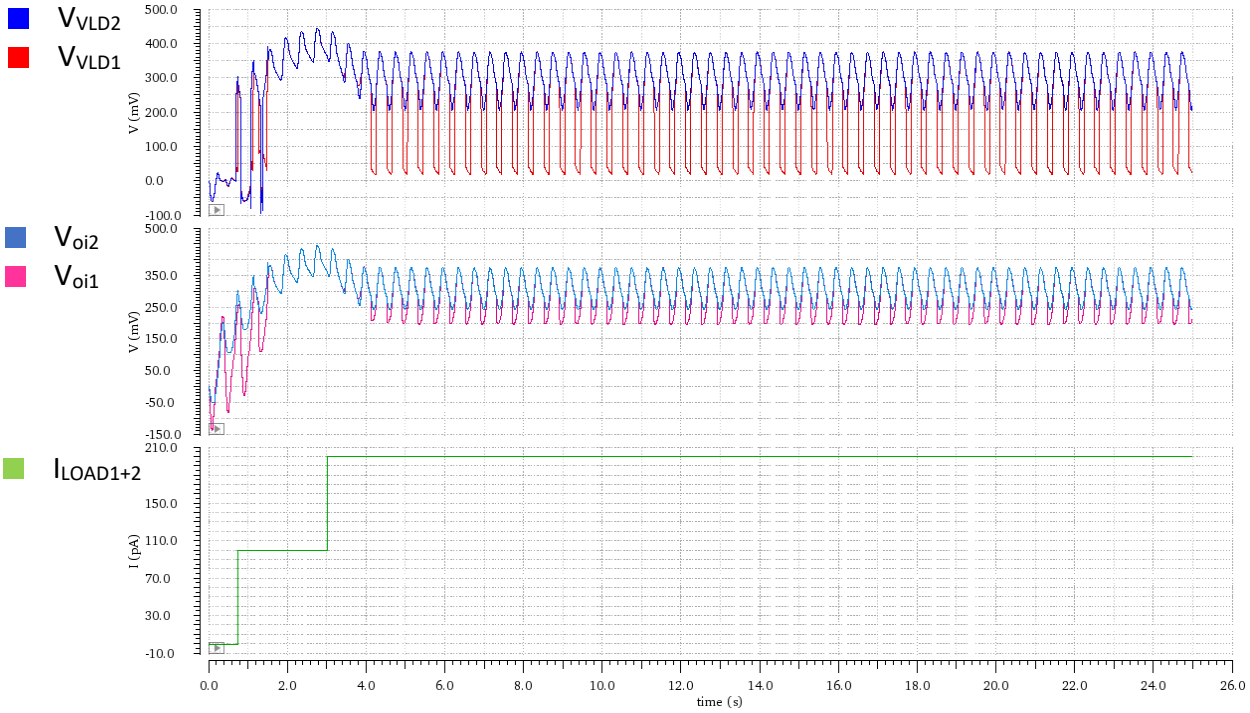


Figure 42. Simulation of the self-reconfigurable DRVM architecture driving two current-loads of 100pA switched at 737ms & 3s

As can be observed from the figure above, the Vvld2, i.e., the output of the SR-DRVM architecture stabilizes from 4 seconds onwards and is able to deliver an average voltage of 298.9 mV while supplying a load-current of 200 pA, which is quite close to what is desired from the SR-DRVM stages. The waveform E2 in figure 33 depicts the stepped-up load-current driven by the SR-DRVM. The magic here is the continuous switching of the 1st stage output voltage – below and above the V_{DETECT} of the VLD. When Voi2 goes above the V_{DETECT}, it contributes a high output current (1X boost – parallel config.) to the SR-DRVM, while when it goes lower, it contributes to a high output voltage (2X boost – series config.) to the SR-DRVM.

Figure 43 presents the simulation result for a standard 1-Stage & series 2-Stage DRVM architecture driving a 200 pA current-load.

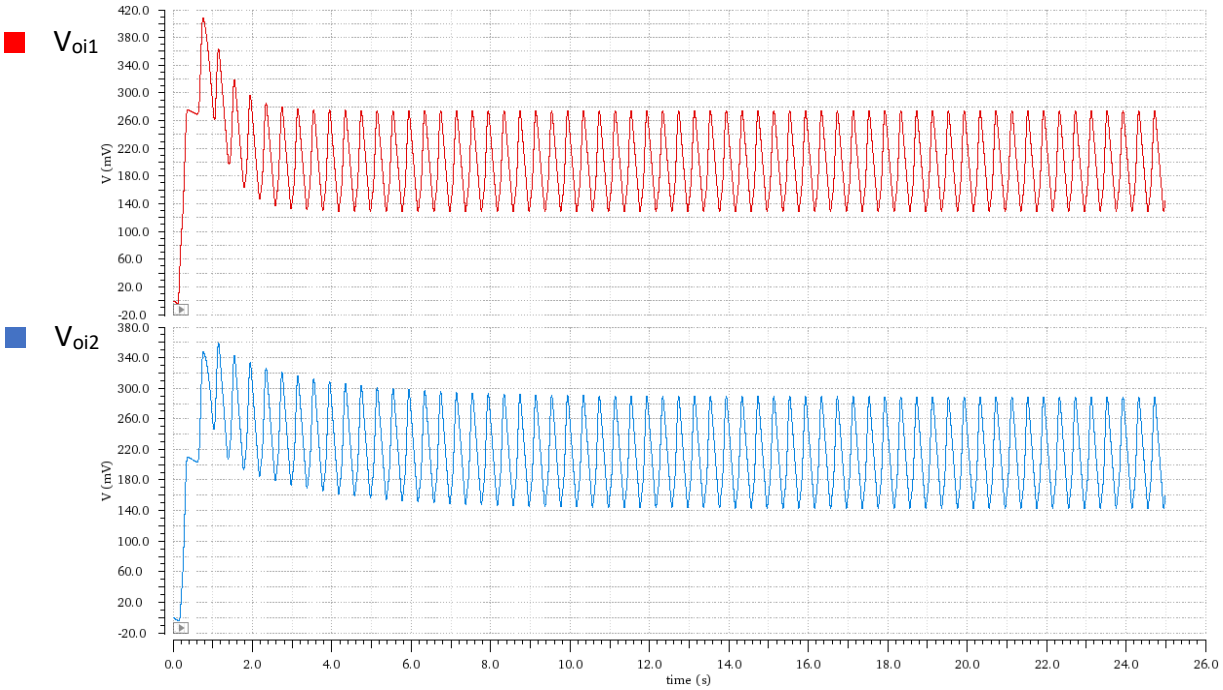


Figure 43. Simulation result for a 1-Stage & series 2-Stage DRVM architecture driving a 200 pA current-load

As can be noted from the figure above, both 1-Stage & series 2-Stage standard DRVM architectures are not able to support a current-load of 200 pA. The average output voltage for 1-Stage DRVM is 197.5 mV, while for a 2-Stage DRVM is 212 mV. Thus, using any of the above 1-Stage or 2-Stage standard DRVMs could severely damage the circuit performance with respect to PVT variations, specially considering the CSRO load that this DRVM is supposed to drive. Note here, that the values of the pumping and storage capacitors in all the DRVM implementations considered in this discussion is as decided in the section 4.1, i.e. 300 pF, with the input voltage being a 2-Harmonic sinusoidal excitation of $V_{IN(2.5\ Hz)}$ = 300 mV_{PEAK} & $V_{IN(5\ Hz)}$ = 100 mV_{PEAK}.

Hence, the SR-DRVM circuit, in its entirety is capable of supplying to even higher loads (in the FF corner) than what a standard DRVM architecture could support, confirming that it might be better suited to support large PVT variations at load.

Before proceeding further to the next circuit block, it may be worthwhile to investigate the behavior of the proposed SR-DRVM with regards to load variations and validate if it could hold up its performance, as has been discussed in the previous two points, with respect to maintaining a calibrated voltage output while supplying the required load-current, when compared to standard DRVM 1-Stage, 2-Stage & 3-Stage implementations, in the FF corner (the most challenging corner with respect to PVT variations).

Figure 44 displays the variation in output voltage of various DRVM implementations with respect to changing loads.

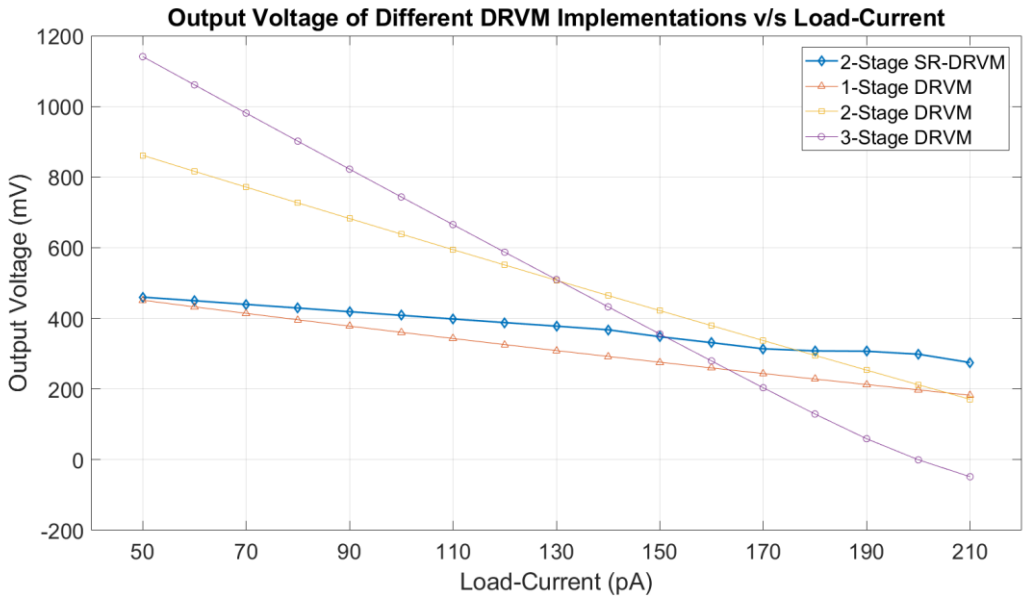


Figure 44. Output voltage of different DRVM implementations versus load-current

Table XXIV records the variation shown in the figure above as:

TABLE XXIV. Output voltage v/s load-current variation for different DRVM implementations

Architecture	Load-Current Variation, ΔI_{LOAD} (pA)	Output Voltage Variation, $\Delta V_{OUT(avg)}$ (mV)	Output Voltage (mV), Upper Bound-Lower Bound
2-Stage SR-DRVM	150	161.5	460.1 – 298.6
1-Stage DRVM	150	268.9	451.4 – 182.5
2-Stage DRVM	150	690.6	861.5 – 170.9
3-Stage DRVM	150	1189.2	1141 – (-48.2)

Thus, as can be observed from the figure and the table above, for a 2-Stage SR-DRVM the variation in output voltage with respect to changing load-currents is the least as compared to the other standard DRVM implementations. Hence, it can be confirmed that the SR-DRVM can successfully produce an output voltage in close vicinity to what is required even under the effect of variations at load. This test-bench easily models how the proceeding circuits to the DRVM stages may behave due to PVT variations, as would be seen in the next section.

Also equally important is to inquire into the behavior of the SR-DRVM when compared to other DRVM implementations with respect to output power & efficiency.

Figure 45 shows the variation in power output for different DRVMs with respect to load-current variations.

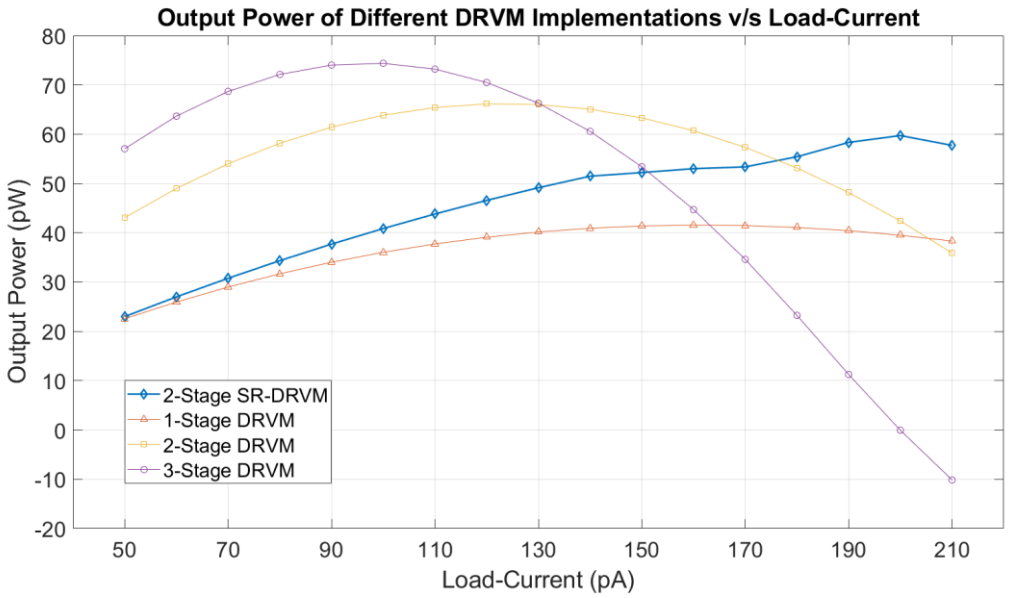


Figure 45. Output power of different DRVM implementations versus load-current

As can be seen in the figure above, the output power of the SR-DRVM increases with the increasing load-current almost linearly, effectively meaning it produces more current when needed while maintaining a steady output voltage. Thus, the SR-DRVM consistently produces more when more is required, although to a certain limit i.e. 210 pA load-current here. For other DRVM implementations, it can be noted that although they sport a higher output power (2-Stage & 3-Stage) when driving low load-currents, their consistency quickly degrades when faced with higher loads. Thus, they are not suitable for ultra-low power operations where load-variations can be substantial. It may also be worthwhile to note that the low power output of the SR-DRVM at low drive currents, as compared to the standard 2-Stage DRVM, is not fundamental. This is a characteristic of the SR-DRVM designed for this particular project as in here, the stages go from series-to-parallel once the output voltage exceeds 250 mV mark. If the VLD is designed to check for an even higher V_{DETECT}, the power output of the 2-Stage SR-DRVM would follow or more so be better than a standard 2-Stage DRVM even for low load-currents, while eventually taking over for higher loads.

Figure 46 depicts the variation in efficiency for different DRVMs with respect to load-current variations.

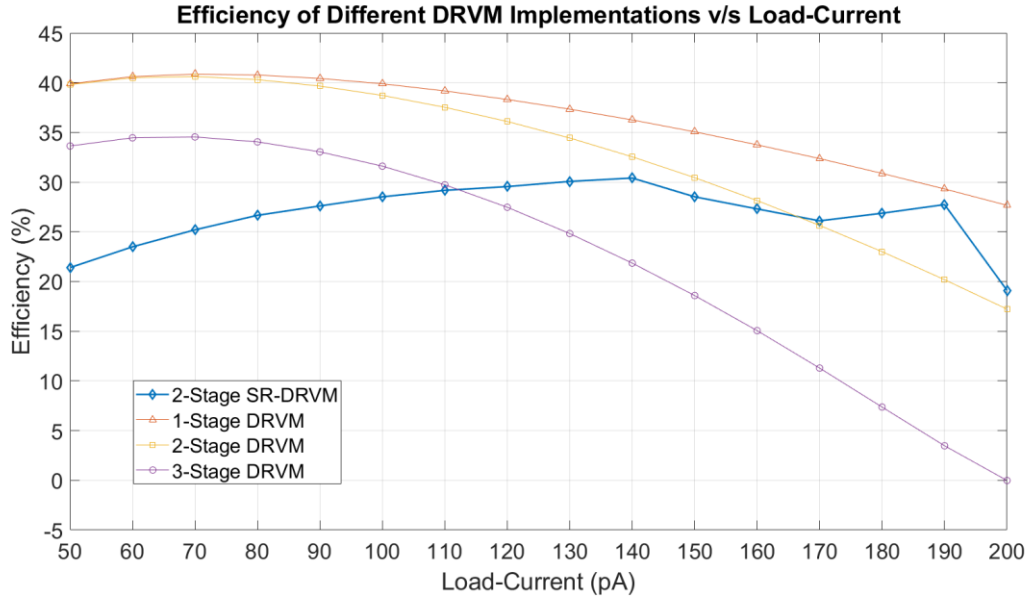


Figure 46. Efficiency of different DRVM implementations at varying load-currents

As can be noted from the figure above, the efficiency of the proposed 2-Stage SR-DRVM architecture varies only by a small amount. In fact, this efficiency remains bounded between 20% and 30%, being

almost unaffected by increasing load-current. While for the standard DRVM implementations of 1, 2 & 3 Stages, the efficiency is quite high at lower load-currents but drastically degrades as the load-current increases to higher values. This is especially the case for 2 & 3 stage standard DRVMs. For the 1-Stage standard DRVM, its efficiency seems higher than the proposed SR-DRVM which looks quite favorable, although, the output voltage and power being quite low, it is not favored. Nonetheless, the efficiency plot of the 1-Stage standard DRVM does suggest an important fact that there is still room for improvement in the efficiency of the 2-Stage SR-DRVM. One other crucial insight into this figure to note, is the trend in the efficiency of 2-Stage SR-DRVM that increases as the load-current increases till 140 pA and then again from 170 - 190 pA, something that none of the other implementations exhibit. This observation may also allow for room to develop this proposed architecture such that it has a constant efficiency curve or better so increasing efficiency curve, up till the point desired.

Again, note here, that the values of the pumping and storage capacitors in all the DRVM implementations considered in this discussion is as decided in the section 4.1, i.e. 300 pF, with the input voltage being a 2-Harmonic sinusoidal excitation of $V_{IN(2.5\ Hz)}$ = 300 mV_{PEAK} & $V_{IN(5\ Hz)}$ = 100 mV_{PEAK}. For the SR-DRVM the second load current is switched at 1.15 seconds and is half the value of the total load current that the architecture needs to cater to.

Hence, from the above two cases, it can be confirmed that the proposed SR-DRVM architecture is better suited for ultra-low power operations than the standard DRVM architecture, being almost load-variation-resistant. This can be attributed to the fact that the SR-DRVM is essentially using two 1-Stage DRVM implementation, once parallel, to cater to its varying output loading conditions which could be a result of large PVT variations of the succeeding stages. This realization also allows an insight as to how the efficiency of the entire SR-DRVM architecture can be improved further. One key insight here is to note the role of V_{DETECT} in deciding the aforesaid behavior.

4.5. CSRO (Current Starved Ring Oscillator)

Following the discussion in Chapter 3 – Section 3.5, a current starved ring oscillator (CSRO) was selected as a suitable timing generator to operate the VCS of main boost converter.

Lets begin by defining the expected output parameters of the CSRO as shown in Table XXV:

TABLE XXV. CSRO output specifications

Parameter	Value (Expected)
Frequency	1000 Hz
Average Current Consumption	90 pA (optimistic max)
Average Power Consumption @ V_{DC} = 320 mV	~ 30 pW (optimistic max)

Figure 47 below presents a circuit schematic of the CSRO:

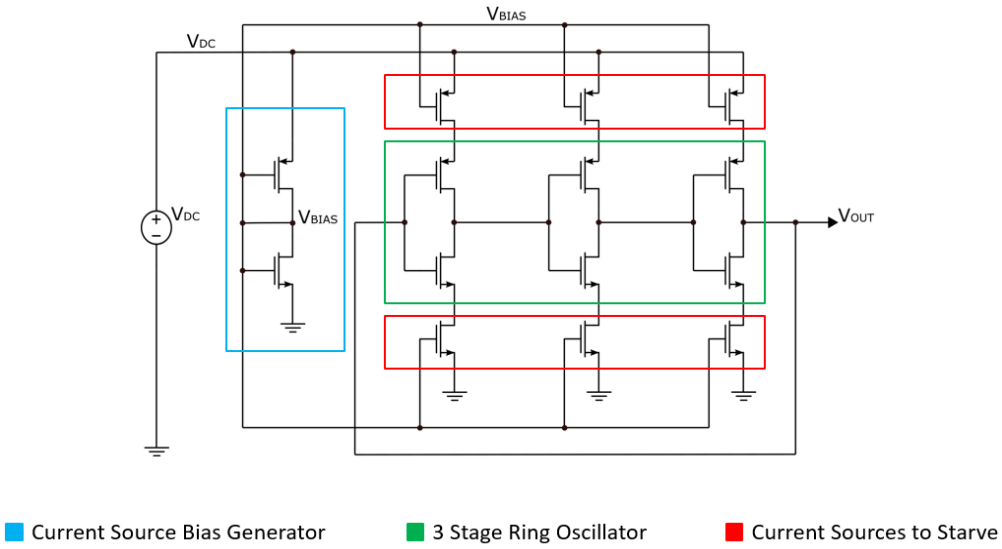


Figure 47. Circuit schematic of current starved ring oscillator (CSRO)

From figure 38 above, it can be seen that the CSRO has 3 parts in its design. The green box represents the core of the oscillator and is responsible to produce the required timing waveform of the desired frequency, at a given DC input.
A 3 stage implementation is selected to allow for high frequency output with low current consumption at the TT corner.
The red box represents the current sources used to starve the ring oscillator. The presence of these current sources is what allows the oscillator to operate at ultra-low power consumption as they restrict the architecture from draining freely the maximum amount of current it possibly can, from the source. Since frequency of this oscillator is directly proportional to the current it drains, the presence of these current sources also limit the frequency. Another important thing to note here is that these current sources also reduce the frequency-sensitivity of the oscillator to process and voltage variations, as they effectively tie the two ends of the oscillator to fixed current values, not allowing it's frequency to go all over the place consuming any amount of current it possibly wants. The CSRO basically consumes current during voltage transients (Low-High or High-Low), the value of which is dictated by these current sources, otherwise (static state) it does not consume any current, ideally speaking. The blue box is essentially a simple circuit used to bias the current sources to the desired value. At this point, it may occur that there are CSRO that are biased at only one of the sides and as to why is it not considered here. One reason for a dual-starved ring oscillator selection is due to the fact that both the NMOS-T & PMOS-T of the inverter are equally degenerated with the presence of the current sources which essentially allows a similar strength in pulling up and pushing down the output voltage of the CSRO. This allows the configuration to be less sensitive to process and voltage variations which is not the case for a single-side starved CSRO. For a single-side starved CSRO the variation in the frequency and the duty cycle of the timing waveform is quite large which reduces increases the sensitivity, due to one of the sides having a stronger influence on the output voltage than the other. Also, for a single-side starved CSRO one sharp and one trailing edge can be seen in the timing waveform due to the same reason, which could hamper in presenting a strong 'ON' and a strong 'OFF' needed to drive the VCS of main boost converter.

While designing the CSRO too, it is recommended to consider about the relative strength of NMOS-T & PMOS-T with regards to the difference in mobility. Selecting the length and width of the MOS-Ts for a CSRO can be quite tricky. One reason for this is the fact that parasitics start playing a significant role when designing for ultra-low power operations. For instance, in a CSRO the parasitics would essentially present themselves as the gate capacitor of the driven stage and the 'ON' resistance of the driving stage that form a time constant. Now, if the current needs to be ultra-low, which is the case here, an intuitive approach can be to increase the length of the devices while keeping the width to a minimum. What could happen here is that the output resistance of the MOS-T increases with increasing length but so does the gate capacitance, which could make the CSRO extremely slow as a very large time constant would result. Also equally important here is to not assume that the current sources used to starve the ring oscillator can just take care of its current needs and the oscillator core in itself would come for free, since these very current sources are not ideal. Hence the current source's current values would too depend on the length & width of the oscillator core MOS-Ts as it effects the V_{DS} across these MOS-Ts. Thus, what should

rather be inquired for in the circuit is a sweet spot where the desired frequency can result from a low-enough value of current by tuning the length & width of the oscillator core MOS-Ts, once the size of the MOS-Ts comprising the current source is decided. Also the 'gm' of the MOS-Ts should be taken in due consideration while selecting the length & width as each stage needs a gain of 1 (little bit greater) to allow for sustained oscillations. If the supply voltage is too high while the driving current is too low, the output will not be able to follow the supply and the oscillations will die out.

Table XXVI records the intricacies seen in MOS-T sizing to identify the sweet spot:

TABLE XXVI. MOS-T sizing intricacy for CSRO

Length (um)	Width (nm)	Process Corner	Frequency (Hz)	Average Current Consumption (pA)
4	250	FF	6500	232
		SS	357	23
		TT	1532	68.6
4	400	FF	4800	247.5
		SS	319	29.5
		TT	1256	81.16
6	400	FF	3117	194.5
		SS	234	22.8
		TT	845	63.7
6	250	FF	4232	183.9
		SS	273	18
		TT	1079	54.4

Please Note: Length & width values are for NMOS-T, for PMOS-T the width is 2X times while the length is kept same. Supply Voltage = 320 mV.

The selected length & width for all the NMOS-Ts is L = 6 um & W = 250 nm, while for PMOS-Ts it is L = 6 um & W = 500 nm. One reason for this selection is because of the maximum current the SR-DRVM architecture can supply which is 210 pA at FF process corner. Another reason is the frequency of oscillation at this MOS-T size which is exactly what is desired for the TT corner and quite acceptable for the other process corners with respect to variation, as compared to other choices.

Figure 48 shows the output waveform of the CSRO as:

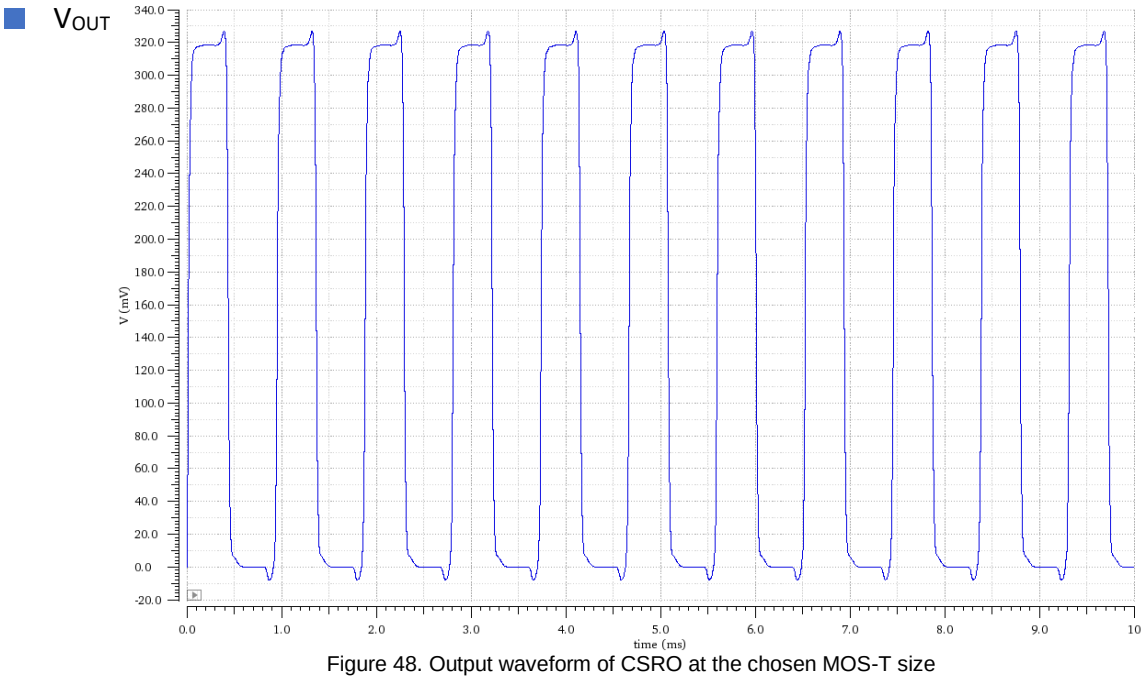


Figure 48. Output waveform of CSRO at the chosen MOS-T size

It may also be worthwhile to note whether the SR-DRVM architecture can sufficiently drive the CSRO at different process corners, as recorded in Table XXVII as:

TABLE XXVII. SR-DRVM performance under different process corners to drive the CSRO

Process Corner	CSRO Average Current Consumption (pA)	SR-DRVM Load-Current (pA)	SR-DRVM Output Voltage (mV)
FF	183.90	190	307
TT	54.47	55	656.6
SS	18.05	20	790.6
FS	52.10	55	445.8
SF	56.45	60	674.8

Hence, it can be observed from the table above that the SR-DRVM is well-equipped to drive the CSRO under different process corners. It would be worthwhile to note that the aversge power consumption of the CSRO circuit is 8.72 pW (TT Corner).

4.6. Integrated Cold Start-up Architecture

Now that all the ingredients for the Cold Start-up recipe has been prepared, lets get started with integrating them all together, as shown in figure 49:

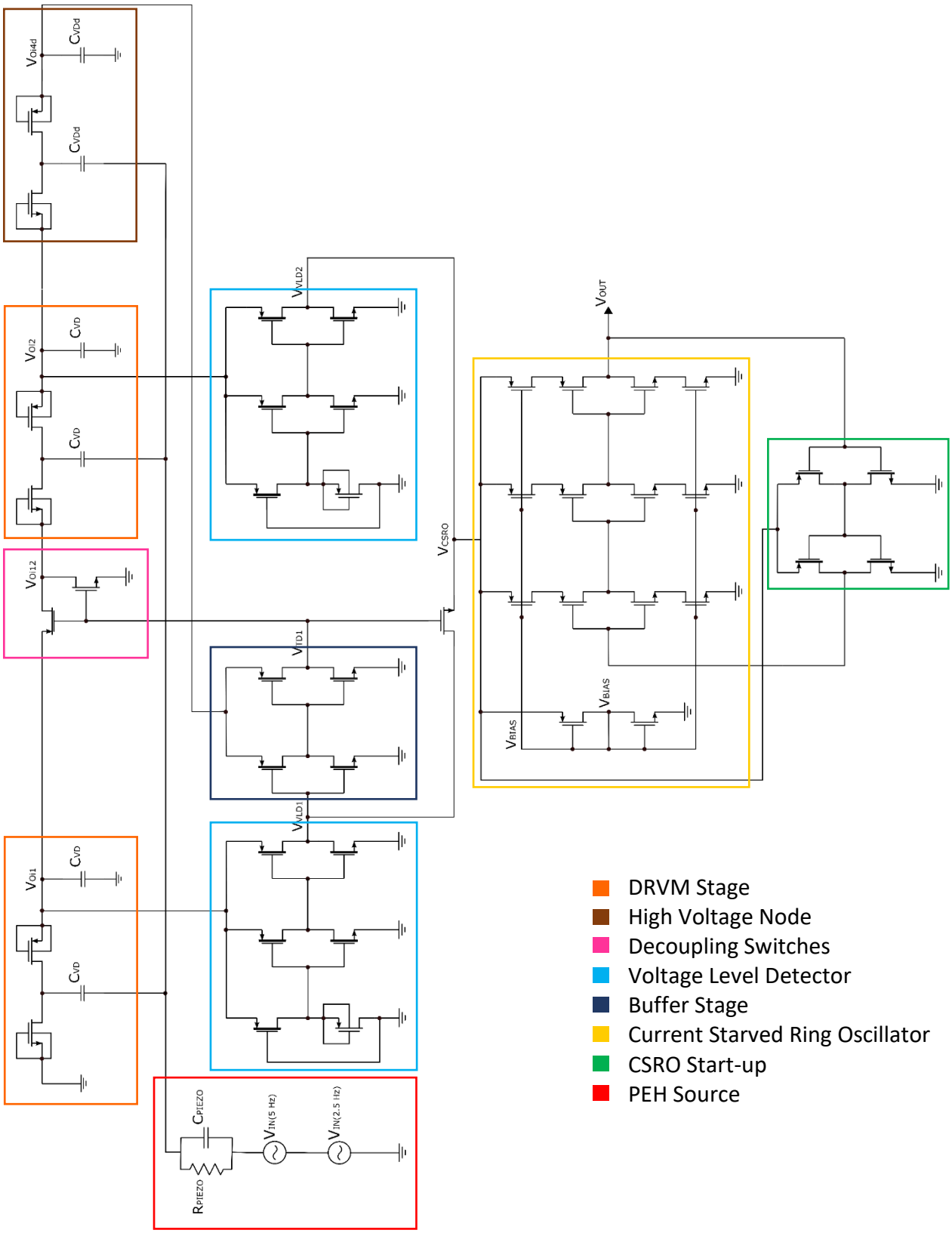


Figure 49. Cold Start-up integrated architecture

Please Note: $V_{VLD2} = V_{CSRO}$

In figure 49 above, the two inverters composed of High-V_{TH} devices highlighted in the green box act as a start-up circuit for the CSRO. It connects the output of the CSRO to its input, essentially completing the

positive feedback loop when the supply voltage V_{CSRO} is sufficient enough to start oscillating, i.e. when the CSRO has enough gain. In the present use-case the two-inverters essentially act as comparators that compare the value at their input (i.e. CSRO output) to half of V_{CSRO}, closing the loop when the condition is satisfied. The inverter MOS-Ts have been sized such that the condition is generally met at V_{CSRO} > 200 mV. This ensures that the CSRO would produce oscillations in all the process corners when it has sufficient gain only. Contrary to this, had there been no start-up circuit for the CSRO, the output would have stabilized at 0 V. This happens because V_{CSRO} begins with 0 V initially, which forces a 0 V at the output. The output remains as such even though V_{CSRO} rises, as 0 V is a stable condition for the designed CSRO and thus, it would not leave this state once at it. Hence, it is important to open the loop in the beginning and only close it when there is enough gain in the circuit to start the oscillations. Although the presence of two High-V_{TH} inverters does decrease the output frequency, it has already been taken care of during the design process in section 4.4.

Lets have a look at the figures below to verify if this Cold Start-up architecture could perform as per expectations, having been subjected to different process corners.

Figure 50 shows the performance (V_{OUT}) of the designed architecture at TT Corner:

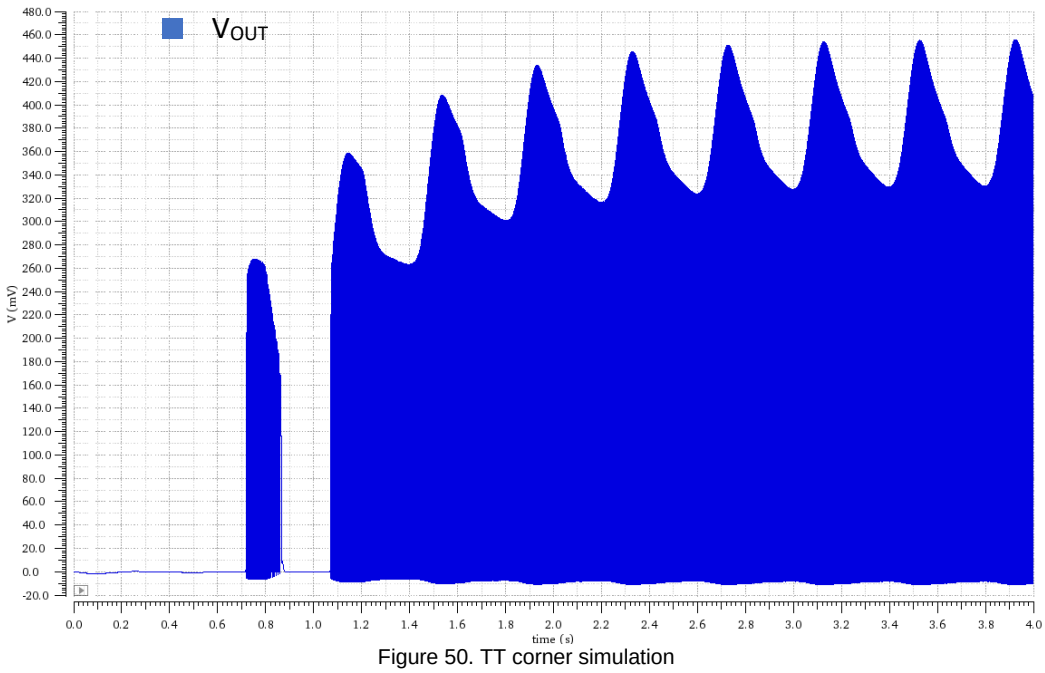
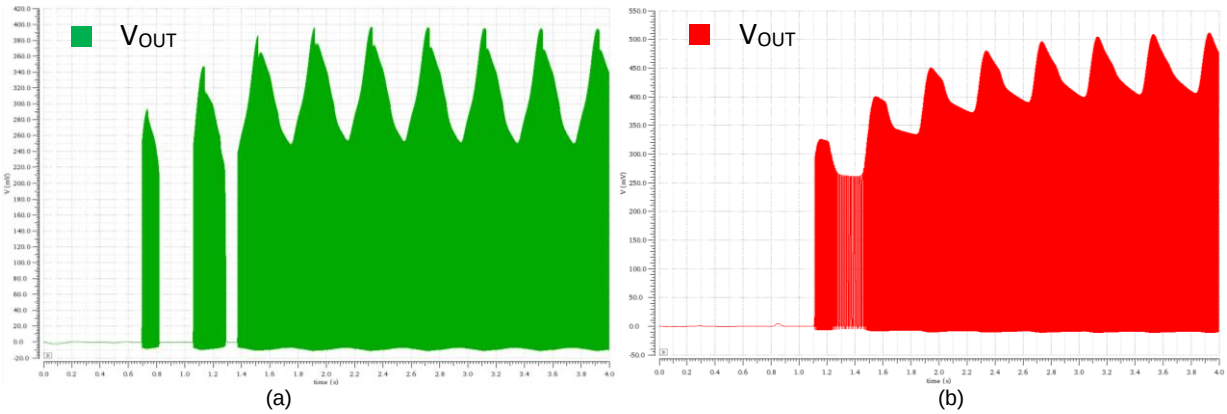
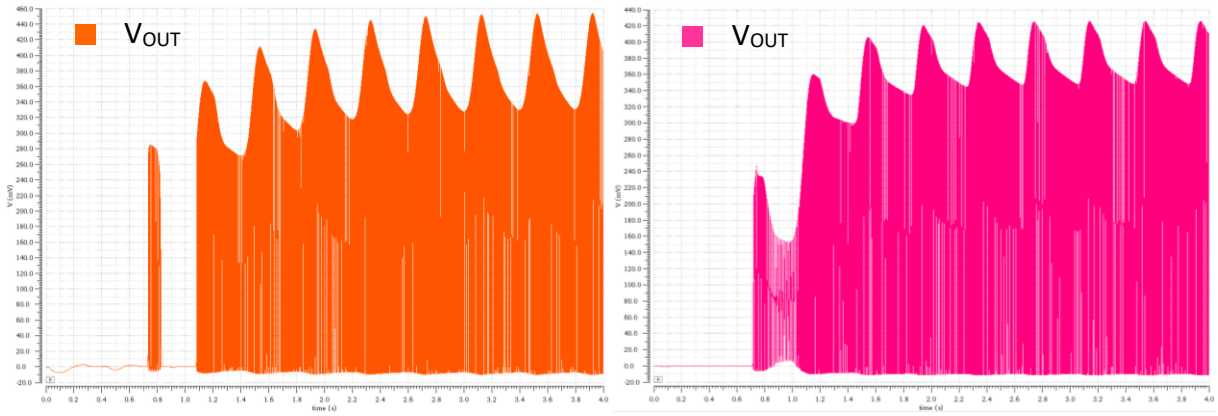


Figure 50. TT corner simulation

Figure 51 depicts the performance (V_{OUT}) of the designed architecture at (a) FF Corner, (b) SS Corner, (c) SF Corner, (d) FS Corner:



(a) (b)



(c) (d)

Figure 51. Corner simulation of the proposed Cold Start-up architecture at (a) FF Corner, (b) SS Corner, (c) SF Corner, (d) FS Corner

Hence, as can be witnessed, the proposed Cold Start-up architecture can successfully perform in all the process corners and should be able to start the main boost converter, so as to allow the TEG to supply a constant voltage of a desired amplitude to the load of the designed power module.

4.7. Cold Start-up Architecture Powered Boost Converter

With the Cold Start-up architecture designed and performing well, it may be worthwhile to note if it can really start the main boost converter and charge the output capacitor to a large voltage value, for starters.

Figure 52 presents the circuit schematic of the Cold Start-up architecture powered boost converter:

Note in figure 52 that there are two buffers following the CSRO output. Buffers after the CSRO are needed to prevent the gate parasitic capacitance of the VCS MOS-T from loading the CSRO output. These buffers are basically driven by the CSRO and are used to directly deliver the required current, from the CSRO supply, to the VCS gate. This allows the Cold Start-up architecture to build up the required current capability without providing the CSRO with a large amount of current to drive the load along with producing a timing waveform. Directly loading the CSRO can make it sensitive to PVT variations since even a little more current drawn from it can disturb its operating point and severely damage the performance of the Cold Start-up architecture. Note that, the boost converter's R_{IN} is taken to be 4.5 Ω ($R_{IN} = R_{TEG} + R_L$) for all simulations. Here, R_L = 1.8 Ω & R_{TEG} = 2.7 Ω.

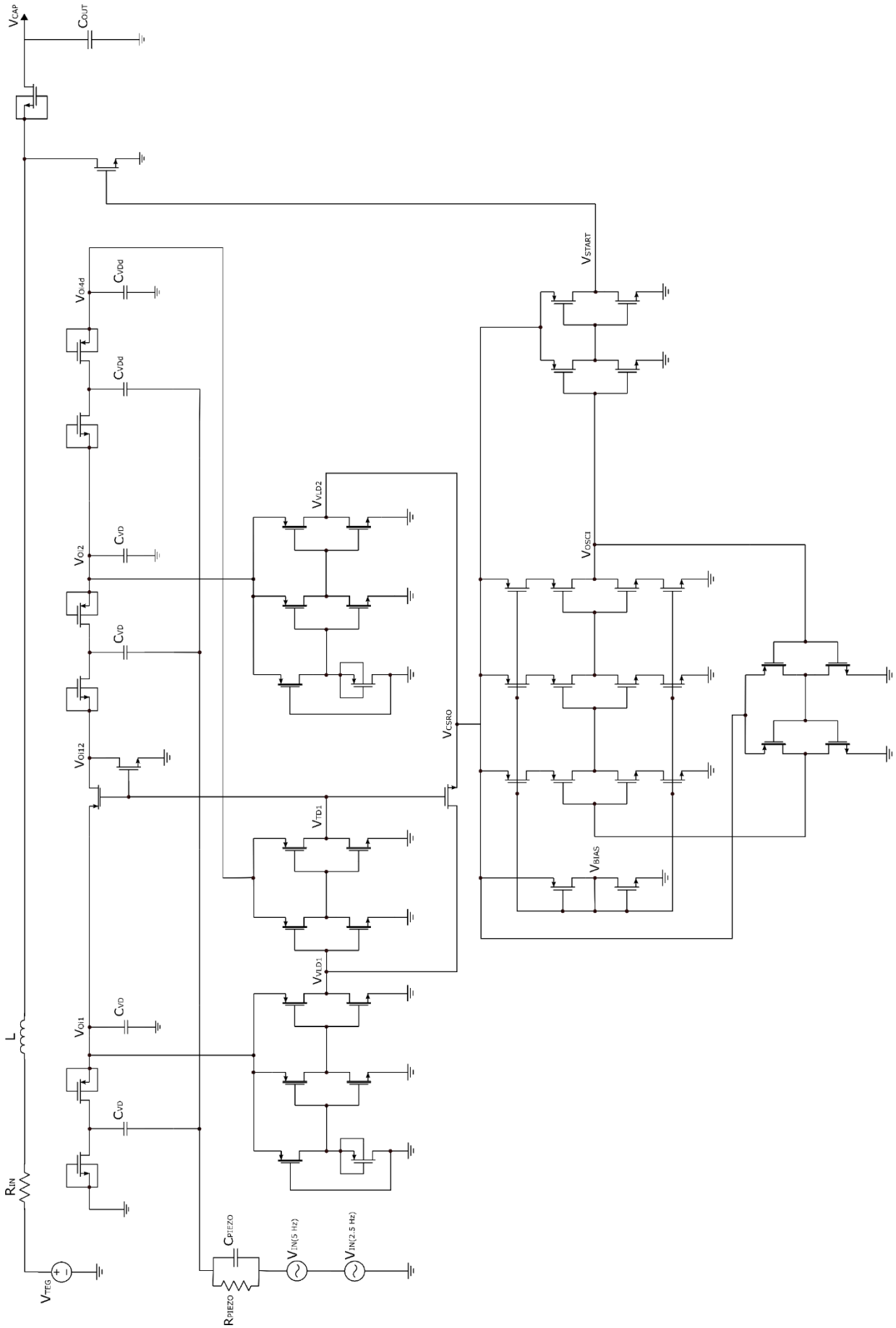


Figure 52. Circuit schematic of the Cold Start-up architecture powered boost converter

Figure 53 below displays the simulated output voltage of this boost converter (shown in figure 52):

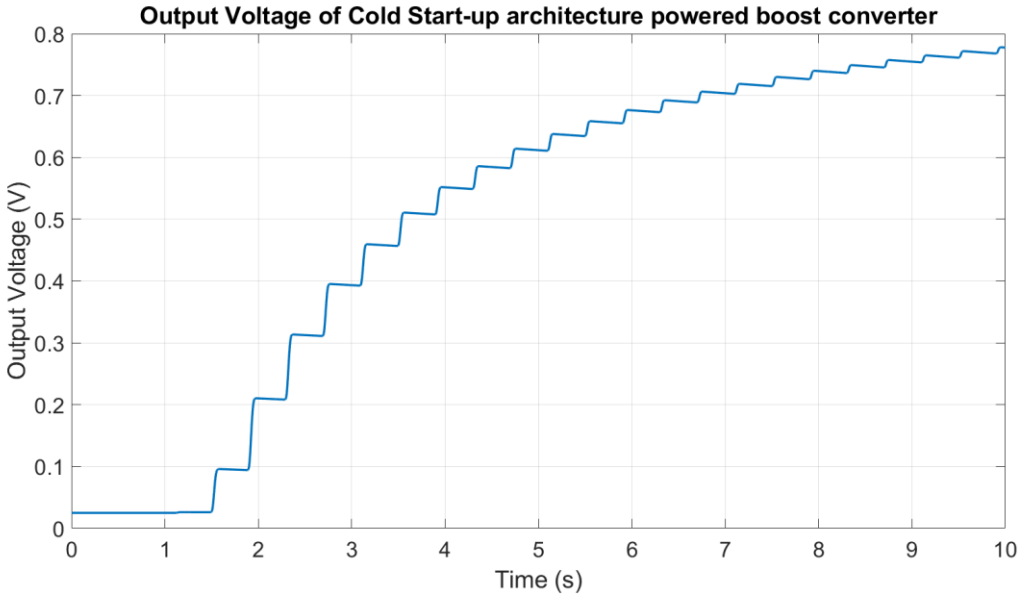


Figure 53. Simulated output voltage of the Cold Start-up architecture powered boost converter

From the figure above, it can be observed that at 3.7 seconds since the start of the Cold Start-up architecture which effectively takes 10 cycles from the PEH excitation output, the output capacitor only charges to 509.4 mV. To assume that the PEH would be able to supply any no. of cycles greater than 15 would be too optimistic. Thus, the proposed power module needs to be so designed that it can achieve the desired output voltage of 1 V, right after 10 cycles of PEH excitation are completed. Note that 10 cycles of PEH excitation are taken to keep a sufficient safety margin in case one of the process corner actually takes 15 cycles due to PVT variations. Hence, what is desired of the design to present a complete power module solution, is some kind of a bootstrap feedback such that the output capacitor, after charging to a value, say 400 mV, owns absolute control of the boost converter driving its output to 1 V by itself. Design, thus, should henceforth focus on autonomy of operation independent of the PEH excitations. Output capacitor's voltage value of 400 mV is selected to again keep a sufficient margin to account for process variations, as opposed to ~ 500 mV.

4.8. Bootstrap Feedback Architecture

As has been discussed in Chapter 3 – Section 3.6, and the previous section of this chapter as well, right after the output capacitor of the boost converter has been charged to a sufficient value, in this case 400 mV, another circuit called the 'Bootstrap Feedback' is desired to take over the reins of the power module to charge it up to 1 V and regulate the output right at that point. A key point to consider while designing this circuit is to ensure that once it starts operating, it should raise the output voltage of the power module to 1 V in preferably a very short period of time to expedite the whole process, the speed of which is already limited by the PEH excitation frequency.

As per the discussion in Chapter 3 – Section 3.6, the bootstrap circuit would consist of a comparator, which essentially is again a VLD, and a CSRO performing as a timing generator to control the VCS of the main boost converter and hence, the entire power module.

The following sections would elaborate on their (bootstrap circuit constituent's) respective designs.

4.9. Bootstrap VLD

As has already been demonstrated in section 4.2, the VLD can be designed to achieve pWs of power consumption while delivering an excellent voltage response with limited PVT variations. However, one should be wary of the speed of response, a VLD can exhibit, at such ultra-low power operations.

The following figure 54 shows the schematic for the feedback VLD:

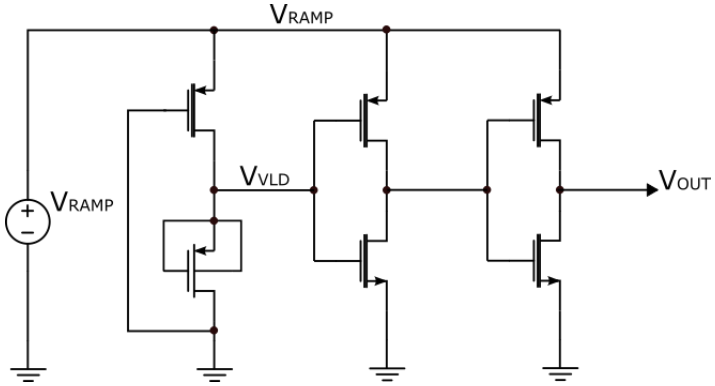


Figure 54. Feedback VLD configuration

Following the procedure in section 4.2, the selected length and width of the VLD circuit is depicted in Table XXVIII as:

TABLE XXVIII. Width & length of MOS-Ts M_1 & M_2

MOS-T	Parameter	Value
M_1 (HVTMOS)	W_1	250 nm
	L_1	10 um
M_2 (NVTMOS)	W_2	50 um
	L_2	10 um

Please Note: As in the previous case, M_1 is the High-V_{TH} device & M_2 is the Nominal-V_{TH} device producing I_{SAT}.

The values of lengths are again kept quite larger to reduce the current consumption of the circuit, while width of M_2, in this case, is the one deciding the V_{DETECT}, since it is quite high (400 mV) this time.

Figure 55 presents the circuit simulation of the abovesaid configuration:

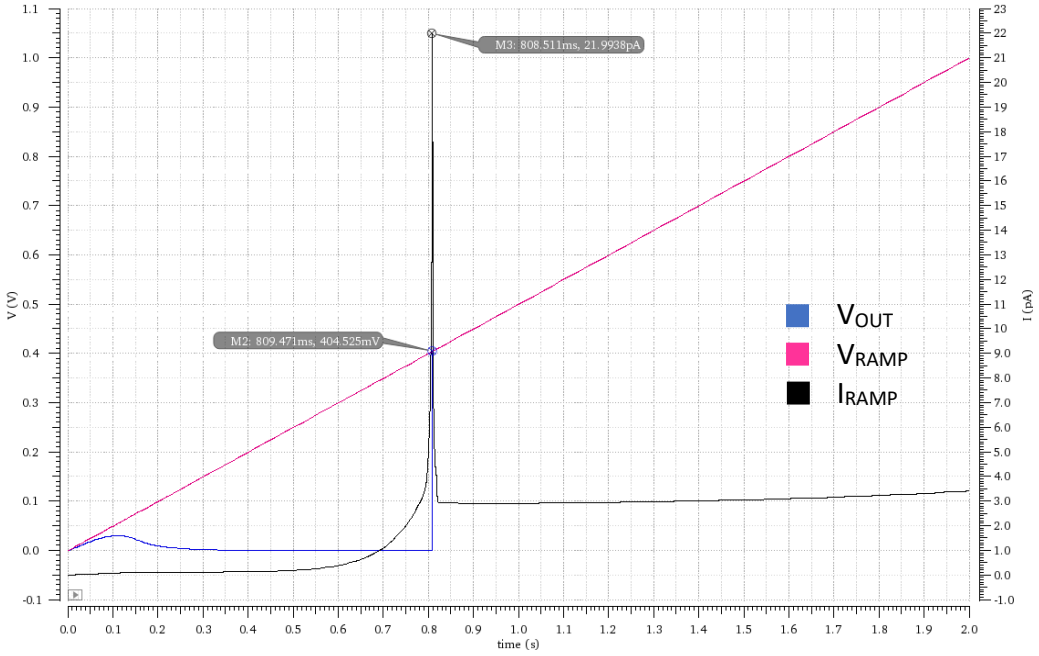


Figure 55. Simulation result of the proposed Feedback VLD with V_{DETECT} = 404.52 mV

Output specifications of the feedback VLD, thus designed, is given in Table XXIX as:

TABLE XXIX. Feedback VLD output specifications

Parameter	Value
V_{DETECT}	404.52 mV
Peak Current Consumption	22 pA
Power Consumption @ Peak Current	8.9 pW

4.10. Bootstrap CSRO

The next part of the bootstrap feedback consists of a timing generator which in this case too is a CSRO, for the same reasons as stated previously. The feedback CSRO would take its supply from the output capacitor and deliver a well timed waveform to the VCS of the main boost converter. One key design consideration is to ensure that it does not consume more current than the capacitor could possibly provide or the entire power module may get stuck at 400 mV or more so even less. This concern gains even more significance in light of the fact that, as the supply voltage of a CSRO increases, not only does its output frequency increase but also its current consumption exponentially (weak-inversion) or quadratically (strong-inversion) increases. Thus, there is a two-fold risk if the feedback CSRO does not follow per considerations:

1. Frequency goes too high: If the frequency is allowed to increase beyond a certain point, without check, the inductor would not be able to follow the switching rate and thus, the current delivered to the output capacitor may decrease. This decrease in the current would certainly bring down the voltage which if not controlled can even deplete the capacitor due to the CSRO consuming too much current than desired, in some cases.
2. Current consumption goes too high: If the current is allowed to increase without check, it will most certainly deplete the capacitor of charges that would in any case not allow the power module to deliver the required current or voltage at the output/proceeding circuitry.

To begin the procedure, lets have a look at the current consumption and output frequency of the CSRO, designed for the Cold Start-up, for varying supply voltages, as shown in figure 56:

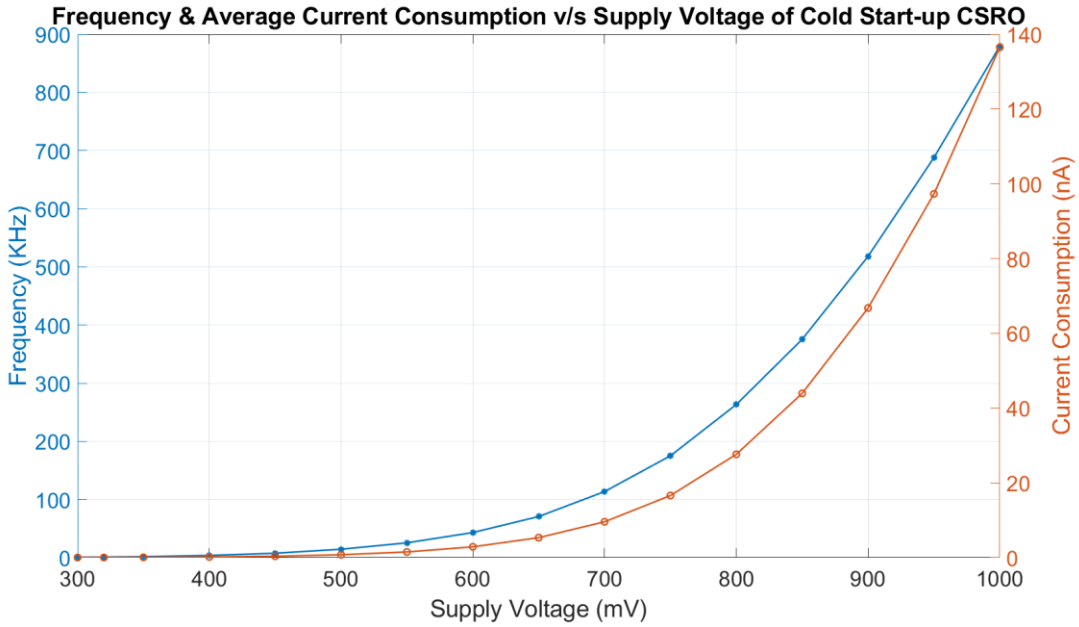


Figure 56. Frequency & Current consumption of Cold Start-up CSRO with respect to increasing supply voltage

From the figure above, it can be observed that if at 1 V output voltage the CSRO needs 136.5 nA of current. Thus, for a capacitor of 100 nF with a voltage of 1 V and a total charge of 100 nC ($Q = C.V$), it

can only supply a current of this magnitude for a period of ~ 0.7 seconds which is highly undesirable. In this case, the output capacitor will not be able to replenish its charge, also since the switching frequency gets ridiculously too high with increasing supply. This result translates to the same fact discussed earlier in this context, about the CSRO consuming all the current out of the output capacitor, not leaving it with any charge for the load of this power module.

Fundamentally speaking, the problem here lies in the design of the CSRO's biasing circuit which dictates the current consumed by the CSRO, which in the present case does not regulate any current except for the desired supply voltage. Hence, if a biasing circuit can be designed that controls the current consumed by the CSRO as the supply voltage increases, that would serve the cause. It may not be a good idea here to fix the current constant at one specific value for all the supply voltages, as this carries the risk of the oscillator's 'gm' getting too low to even satisfy the oscillation condition. Moreover, such an assumption could also cause the CSRO current being too low to follow the large supply voltage resulting in either a very small duty cycle or no oscillations at all. Thus, in light of this, it may be a good idea to design a biasing circuit that would allow the current consumed by the CSRO to rise in a fashion similar to how it would without any biasing circuit, i.e. exponential for weak-inversion & quadratic for strong-inversion, while only controlling the amount by which the CSRO current increases with the supply voltage. This would also provide a degree of freedom with regards to the output frequency, as though it would increase with supply voltage, its value still could be designed to be well within the limits.

Hence, the proposed bootstrap feedback architecture can be modified a bit to accommodate the current-limited current-starved ring oscillator (CL-CSRO) as demonstrated in figure 57 below:

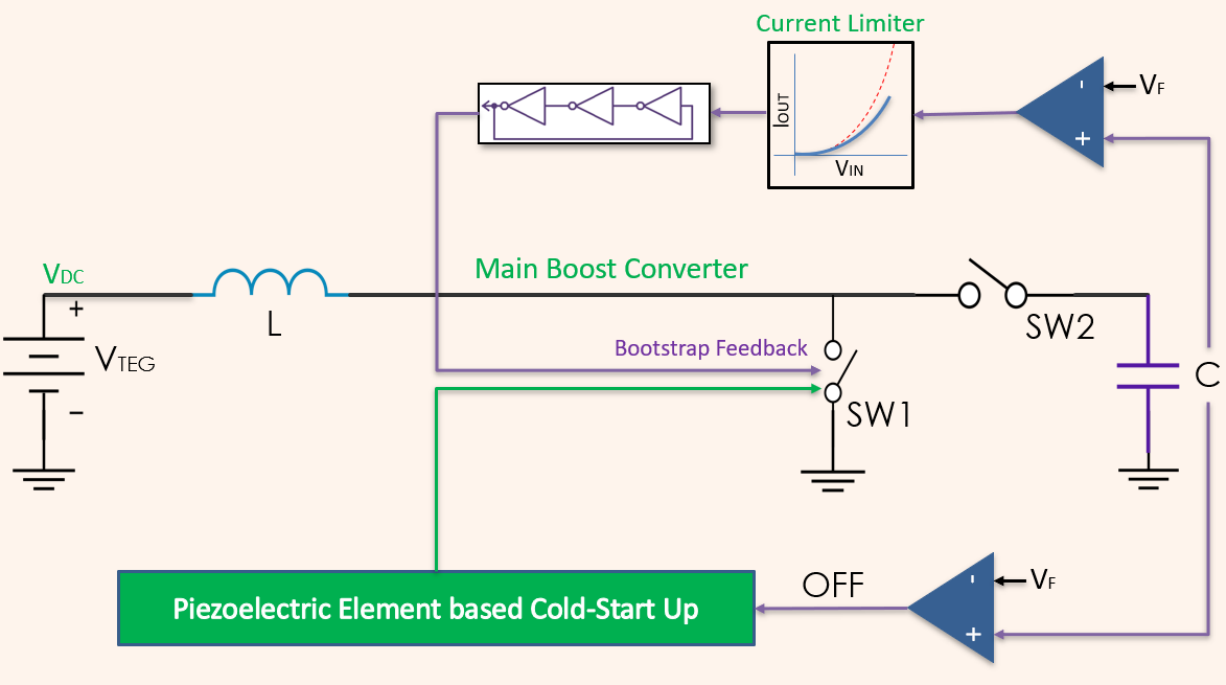


Figure 57. Proposed modified bootstrap feedback architecture

Next section would demonstrate how current limiting could be done.

4.11. Current Limiter Biasing Circuit

To begin with designing the current limiter, one possible inspiration could be found in a PTAT current reference generator [61] as shown in the following figure 58:

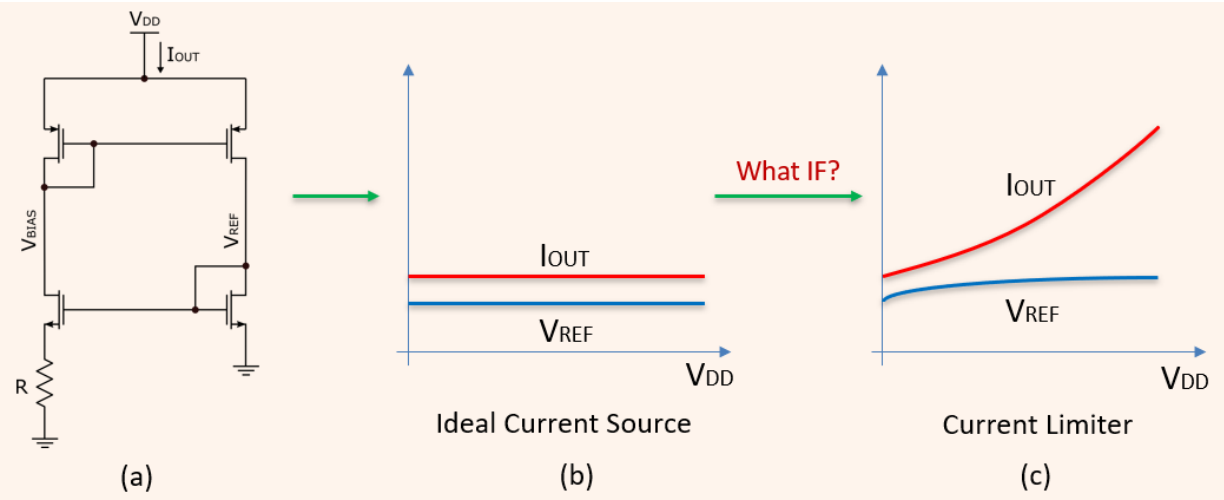


Figure 58. (a) PTAT current generator, (b) Ideal current behavior of PTAT current generator, (c) Non-Ideal design of PTAT current generator may lead to an ideal current limiter

As can be observed in the figure above, an ideal PTAT current generator produces a constant reference current and voltage irrespective of the varying supply voltage. The question is, can it's design be modified in a way such that the generated current would follow the supply voltage? A key insight into the PTAT current generator's working principle is the role the resistor 'R' plays in deciding the value of the reference current. Indeed, 'R' also tends to be the only parameter that can be designed to vary here. Hence, if 'R' can be replaced by a MOS-T that essentially acts like a resistor but its value can be controlled with respect to the changing supply voltage, that would just do the trick. Figure 59 displays the schematic of the designed current limiter circuit:

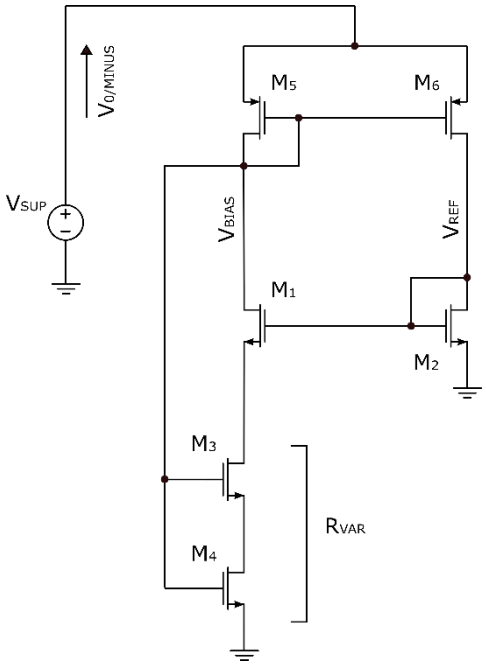


Figure 59. Proposed current limiter circuit

Note in the figure above that the MOS-Ts M_3 & M_4, comprising a variable resistor 'R_{VAR}', are biased to operate in the triode region, thus, basically acting as a resistor. The gate voltage of M_3 & M_4 are tied to V_{BIAS}, thus directly being controlled by a scaled down version of V_{SUP}. The choice of having two MOS-Ts as R_{VAR} is made to ensure the presence of a large resistance in order to control the amount of current flowing through the two branches. The value of the supply current, $V_{0/MINUS}$, and the biasing voltages, V_{BIAS} and V_{REF}, are primarily determined by tuning the sizes of the MOS-Ts M_1, M_2, M_3 & M_4 in the circuit configuration. For instance, the length/width ratio of M_3 & M_4 is kept to be quite large to ensure a low reference current, at a given V_{SUP}. Furthermore, the width/length ratio of MOS-Ts M_1 & M_2 decide the steepness of the reference current curve, and thus can be used to tune it such that even at higher values

of V_{SUP} the current consumption can be kept to a minimum, while ensuring sufficient current to drive the CSRO. Therefore, their width/length ratio is used to determine the exact reference current biasing the CSRO from 400 mV to 1 V of V_{SUP}.

The sizes of the MOS-Ts used in the current limiter circuit can be seen below in Table XXX as:

TABLE XXX. Width & length of MOS-Ts in the proposed current limiter

MOS-T	Parameter	Value
M_1	W_1	1.32 um
	L_1	180 nm
M_2	W_2	220 nm
	L_2	180 nm
M_3	W_3	220 nm
	L_3	12 um
M_4	W_4	220 nm
	L_4	18 um

Figure 60 depicts the behavior of the reference current for varying V_{SUP}:

Figure 60. Variation of the reference current & the supply current with supply voltage

Hence, as is evidenced in the figure above, the reference current, given by I_{M6}, varies from 175.4 pA at 400 mV to 6.8 nA at 1 V of V_{SUP}, which is not quite low for the CSRO to produce a well-timed waveform at 400 mV or even 1 V. This would also ensure that the output capacitor of the main boost converter is minimally depleted of available charges and a majority share of these could be dedicated to meet the load demands. Note that the reference current, I_{M6}, would correspond to the current flowing in one branch of the CSRO.

4.12. Entire Bootstrap Feedback: Current-Limited CSRO (CL-CSRO)

Now that all the components for the proposed 'Bootstrap Feedback' circuit are developed, lets begin by observing their behavior with respect to what is expected, before the integration of the complete power module is commenced.

Figure 61 presents a 5-Stage CSRO biased with the proposed current limiter circuit:

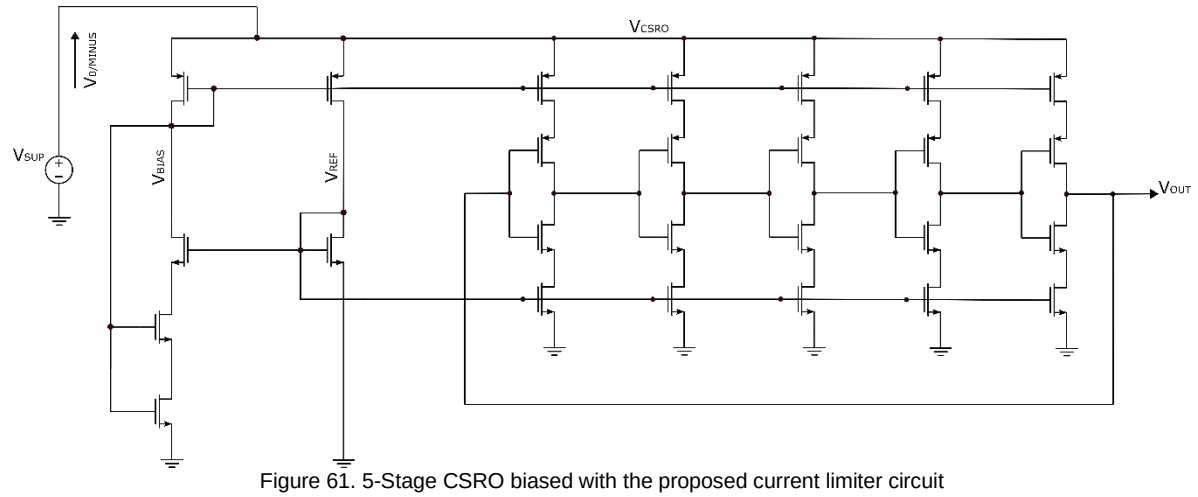


Figure 61. 5-Stage CSRO biased with the proposed current limiter circuit

It may be important to note in the figure above that a 5-Stage CSRO is used as opposed to a 3-Stage one in the Cold Start-up circuit. One reason for this choice is that a 5-Stage CSRO introduces an additional 2-Stage worth of delay to the signal propagating from the first stage to the last, as compared to a 3-Stage CSRO, thus reducing the frequency of oscillation. This is crucial since as the supply voltage here increases, the frequency as well follows it which may not serve well if the frequency gains a large momentum as was shown in figure 46. Thus, limiting it by adding another 2-stages could be helpful. A 5-Stage implementation is also optimum since the current consumption does not increase as significantly as the no. of stages added.

Figure 62 compares the effect of biasing a 5-Stage CSRO with the current limiter as compared to the one used in the Cold Start-up case:

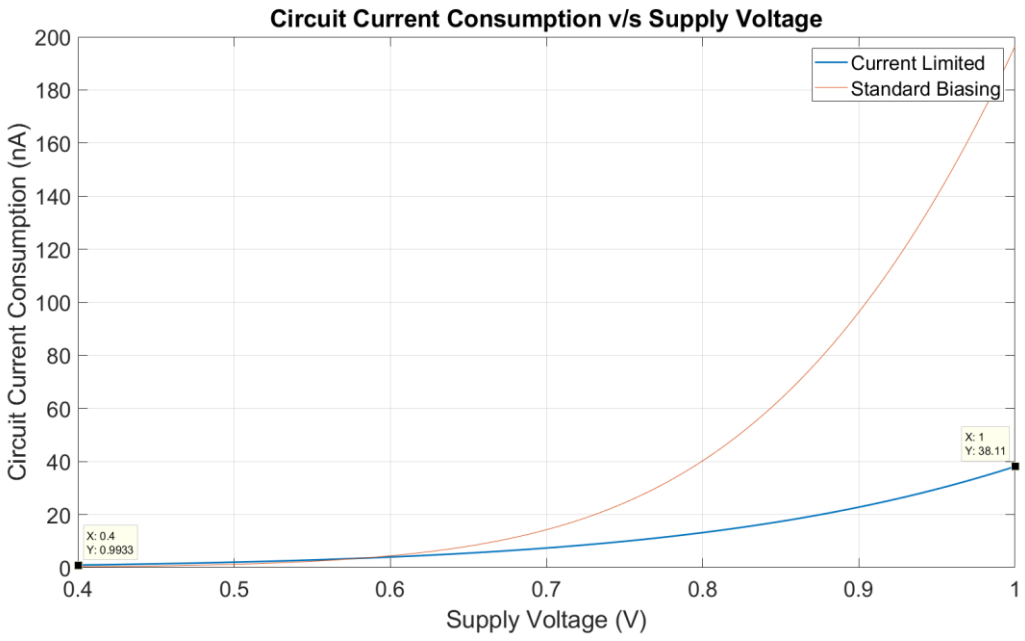


Figure 62. Comparison of different biasing schemes for CSRO

As can be observed from the figure above, compared to the standard biasing (refers to the one used in Cold Start-up) the proposed current limiter biasing performs exceedingly well limiting the circuit current consumption to 1/5th of the original value as voltage supply reaches 1 V. This is also complimented by the CSRO producing a well-timed waveform for the entire supply voltage range, which turns out to be just right for the boost converter's output to be well-maintained at 1 V (proved later on). Table XXXI below shows the output frequency of the CL-CSRO at different V_{SUP}:

TABLE XXXI. Output frequency of CL-CSRO

Supply Voltage	Frequency (KHz)	Power Consumption (nW)
400 mV	2.098	0.25
1 V	18.255	37.19

As can be noted from the table above, the due to the proposed biasing not only did the current consumption reduced at 1 V but also the frequency of oscillation reduced by more than a factor of 35 which is quite considerable.

4.13. Power Module Load Connection

How should the load be connected to the power module? – Is the last design question confronted in this project, towards the development of a completely autonomous solution for a power module that is capable of sustaining itself without any external interferences or use-case-concerns.

One idea could be to keep it connected to the power module right from the beginning of its operation, i.e. since the Cold Start-up. The demerit of such an approach is that the load would be draining the current from the output capacitor even when the output voltage is not sufficient enough to support its operation. Such static-state power consumption of the load, if not accounted for properly, could deprive the output capacitor of the charge required to even initiate the bootstrap feedback phase. Since the load is not known a priori in this project (out-of-scope), it is considered to be a black box of resistance 'R_L = 1 MΩ'. Hence, such an approach could instead deteriorate the entire architecture's operation and therefore purpose.

The solution this project proposes is to connect the load only when the output voltage of the power module has been checked to be 1 V. From an implementation point of view, the proposal is to use a VLD that forces a check condition of 'V_{DETECT} = 1 V'. Once the condition is satisfied the load would be connected to the output capacitor, while being maintained at 0 V otherwise rendering any OFF-state power consumption of the load at 0 W (ideally). Such an approach has the advantage of rendering the design quite reliable in case the load is unspecified, except for the power consumption. The feedback architecture working along with the VLD also ensures that the load will be connected to the output capacitor only when sufficient output power is available in conjunction with output voltage. This would also allow the designer of the proceeding circuitry/load a degree of freedom with respect to its static-state (OFF-state in this case) power consumption being not too stringent. Moreover, this approach can also eliminate the requirement of a separate Power-on-Reset (PoR) circuit. A PoR circuit is generally desired, specially in ultra-low power applications, to monitor the supply voltage which when reaches a predetermined value, the load could be started accordingly, thus preventing unnecessary power consumption. Until this condition, the PoR and depending upon the configuration even the load circuit, consume static (OFF-state) current which needs to be minimized.

Figure 63 depicts the circuit schematic of the proposed voltage output monitoring VLD circuit:

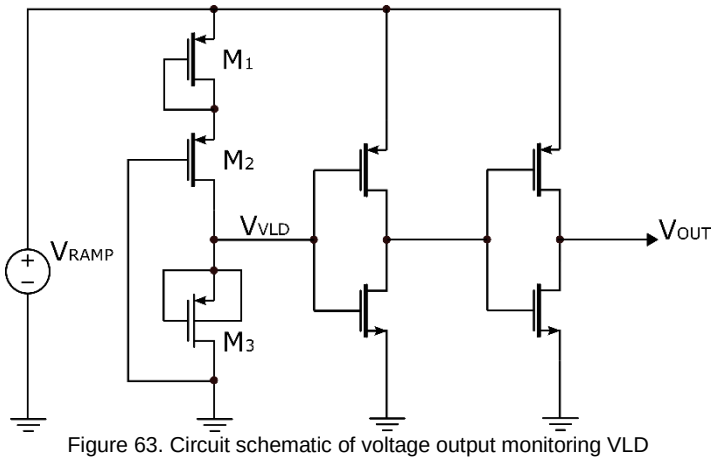


Figure 63. Circuit schematic of voltage output monitoring VLD

The VLD configuration shown in the figure above consists of an extra gate-drain connected high-V_{TH} PMOS-T M_1 above the regular voltage controlled current source High-V_{TH} PMOS-T M_2, to allow for a reduced width/length ratio of the original PMOS-Ts (M_3/M_2) at very high V_{DETECT} [49]. M_1 is designed to be of the same size as M_2. As such M_1 drops half the supply voltage at its drain, thus generating an equal V_{GS} voltage level for both M_1 & M_2. The 2T configuration of the original VLD consisting of PMOS-Ts M_2 & M_3, now gets only half of V_{RAMP} as their supply. Hence, the ratio of M_3/M_2 need only be designed to obtain a V_{DETECT} half of what is originally needed. In this case, for a 1 V V_{DETECT}, the supply voltage for M_3 & M_2 would be 500 mV and therefore, they should be sized such that V_{DETECT} = 500 mV to ensure V_{OUT} starts following V_{RAMP} from 1 V. The output buffers take care of driving the load, as well as ensuring V_{OUT} follows V_{RAMP} even though V_{VLD} is literally halved. An added advantage of this configuration is that the current consumption also reduces to half along with V_{DETECT}.

Following the procedure in section 4.2, the selected length and width of the VLD circuit is depicted in Table XXXII as:

TABLE XXXII. Width & length of MOS-Ts M_2 & M_3

MOS-T	Parameter	Value
M_2	W_2	250 nm
	L_2	50 um
M_3	W_3	3.8 um
	L_3	250 nm

Please Note: M_1 has the same size as M_2

Figure 64 shows the circuit simulation of the abovesaid configuration:

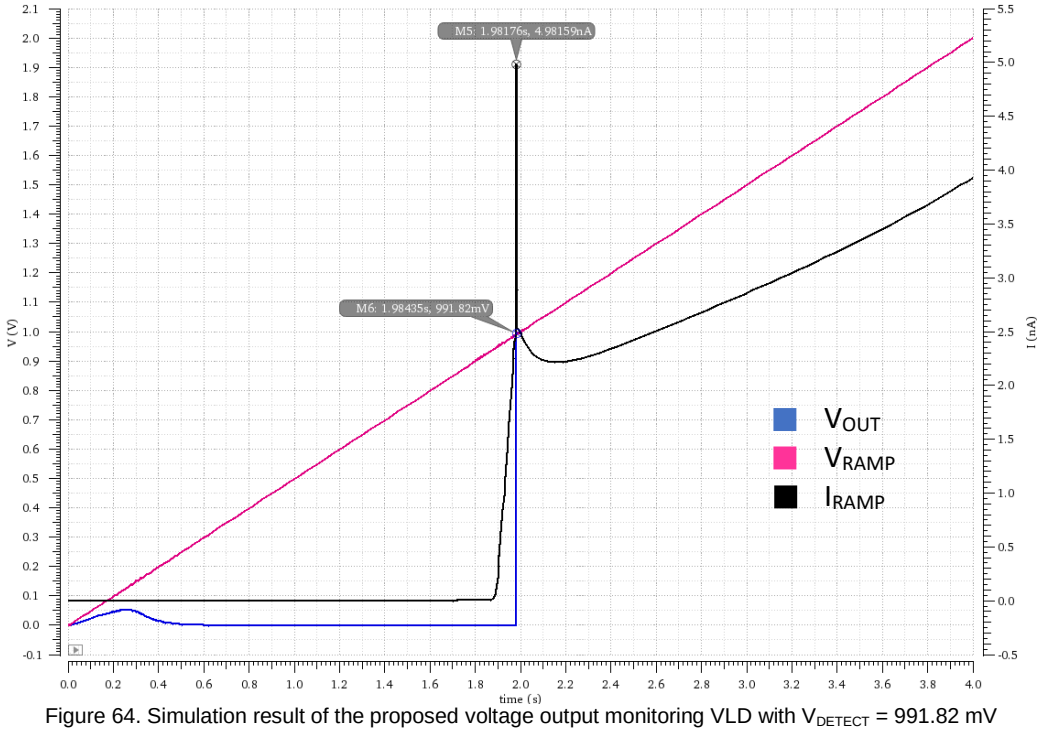


Figure 64. Simulation result of the proposed voltage output monitoring VLD with V_{DETECT} = 991.82 mV

Output specifications of this Load-side VLD, thus designed, is given in Table XXXIII as:

TABLE XXXIII. Load-side VLD output specifications

Parameter	Value
V_{DETECT}	991.82 mV
Peak Current Consumption	4.98 nA
Power Consumption @ Peak Current	4.94 nW

Note that the V_{DETECT} = 991.82 mV is purposefully set instead of the desired V_{DETECT} = 1 V. Since the output voltage is desired to be at 1 V, keeping the V_{DETECT} at this voltage level would mean continuous power consumption at peak current by the VLD and thus, unnecessary wastage of power at all times.

It may be worthwhile to note the effect of process variations at different process corners, as given in Table XXIV as:

TABLE XXIV. Circuit performance under different process corners

Process Corner	V_{DETECT} (V)	I_{PEAK} (nA)
TT	0.99	4.98
FF	0.98	28.71
SS	1	0.78
SF	1.07	13.53
FS	0.93	2.38

The total variation in all the process corners with respect to V_{DETECT} is ΔV_{DETECT} = 140 mV and with respect to the peak current consumption is ΔI_{Peak} = 28.6 nA

4.14. Complete Energy Module

Figure 65 presents the circuit schematic of the complete Energy Module solution proposed in this work as:

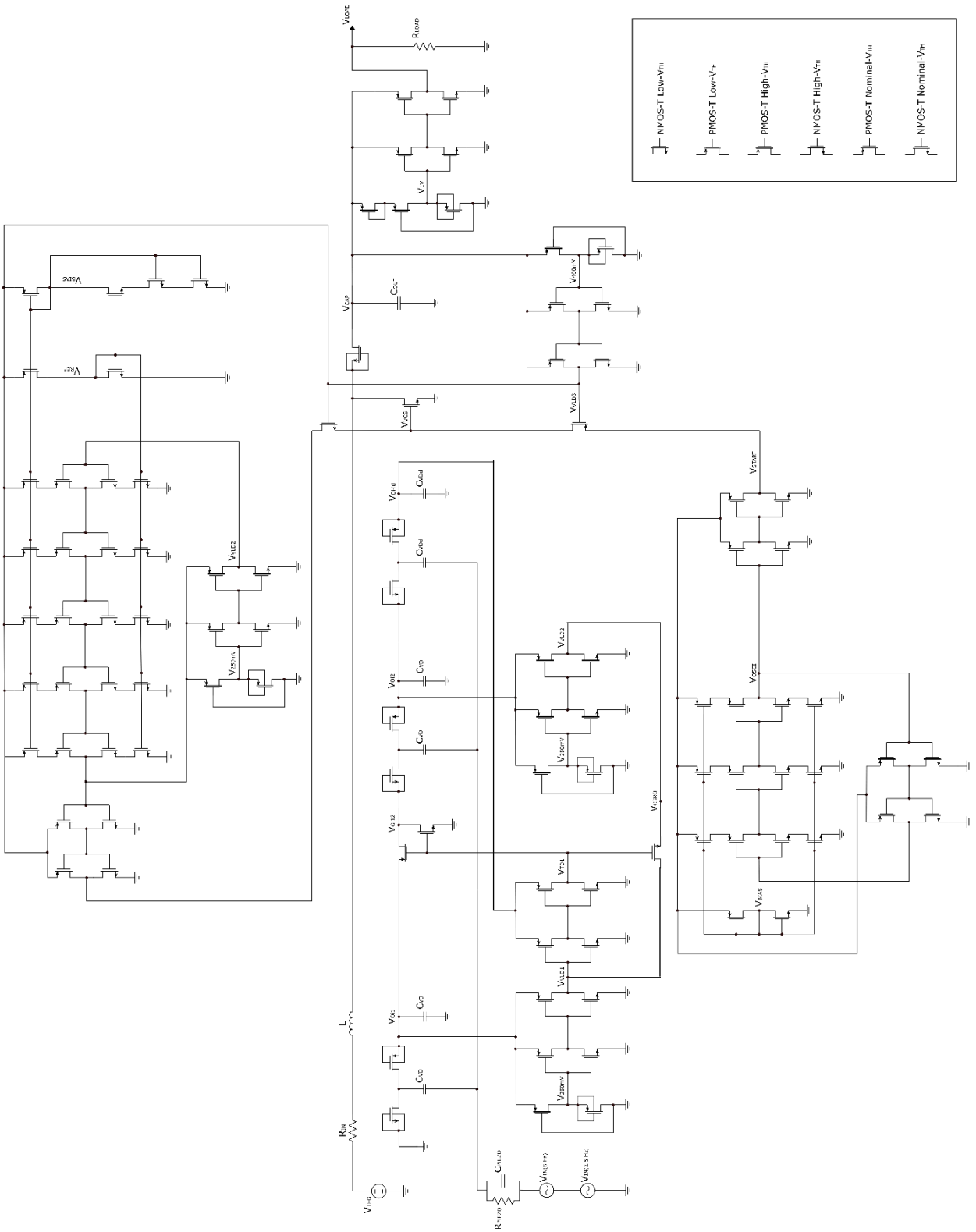


Figure 65. Circuit schematic of proposed Energy Module

Fun Fact – The proposed Energy Module consists of 100 MOS-Ts.

Now that we have finally integrated the entire proposal into one complete solution for a self-sustainable Energy Module, lets have a look as to how it performs under different situations:

1. Performance under different process corners:

Figure 66 depicts the output voltage of the Energy Module in the **TT process corner**:

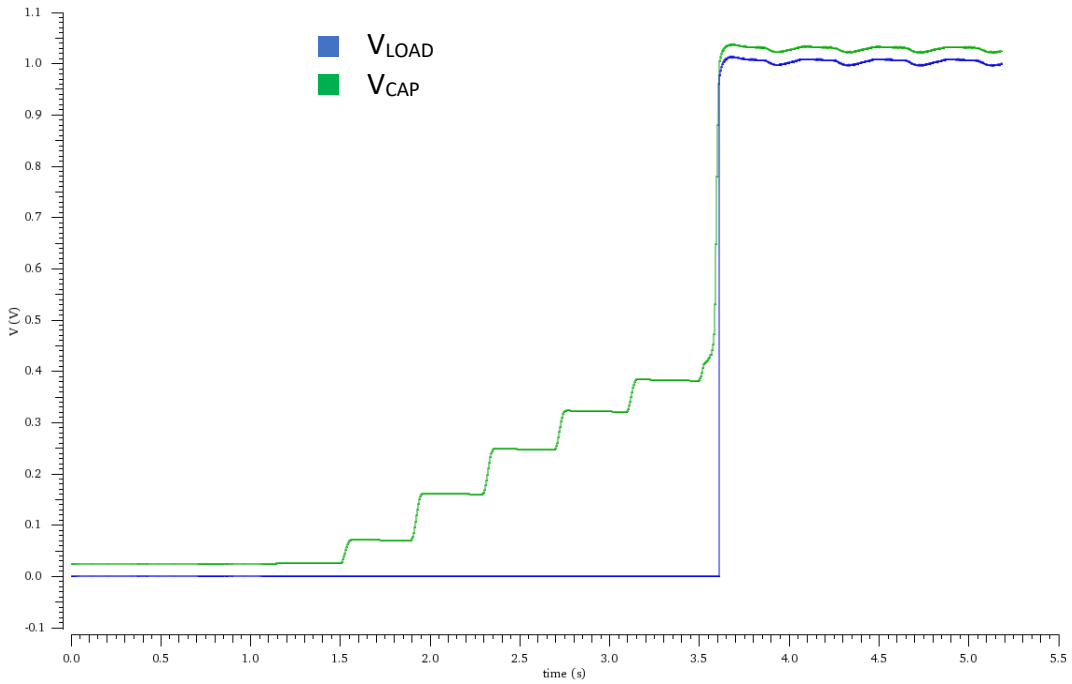


Figure 66. Energy Module load voltage and output capacitor voltage at TT process corner

Note in the figure above that once V_{CAP} or the output capacitor voltage reaches 1 V, the voltage and corresponding power is immediately delivered to the load. All that the load sees, is a sharp 1 V input from the power module capable of driving it without having to be concerned about any possible supply drops or droops (assuming load remains constant in this case) to lower values, which if delivered, may render the load to behave abruptly.

Output specifications of the Energy Module, simulated above, is given in Table XXXV as:

TABLE XXXV. Energy Module output specifications (TT Corner)

Parameter	Value
V_{PIEZO}	300 $mV_{PEAK(2.5\ Hz)}$, 100 $mV_{PEAK(5\ Hz)}$
PEH Power Consumption	240.5 pW
V_{TEG}	25 mV
V_{Load}	1 V
TEG Input Power	1.77 uW
TEG Output Power	1 uW
TEG Power Conversion Efficiency	56.5 %
No. of PEH excitation cycles needed	9
Load Voltage Settling Time	3.6 s
Ripple	12.4 mV (1.24 %)

Figure 67 depicts the output voltage of the Energy Module in the **FF process corner**:

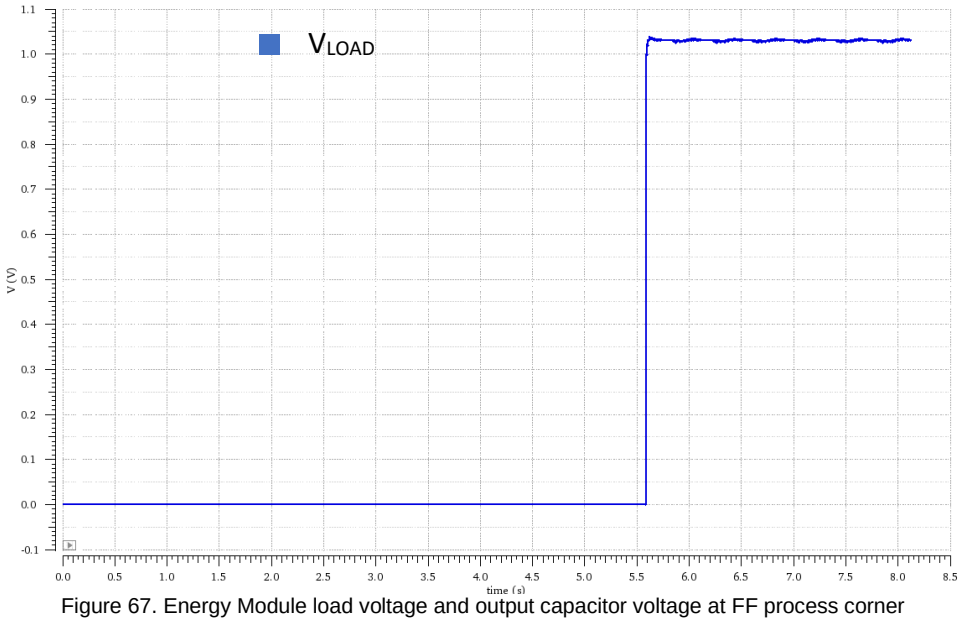


Figure 67. Energy Module load voltage and output capacitor voltage at FF process corner

Output specifications of the Energy Module, simulated above, is given in Table XXXVI as:

TABLE XXXVI. Energy Module output specifications (FF Corner)

Parameter	Value
V_{PIEZO}	300 $mV_{PEAK(2.5\ Hz)}$, 100 $mV_{PEAK(5\ Hz)}$
PEH Power Consumption	233.8 pW
V_{TEG}	25 mV
V_{Load}	1.03 V
TEG Input Power	2.05 uW
TEG Output Power	1.06 uW
TEG Power Conversion Efficiency	51.63 %
No. of PEH excitation cycles needed	14
Load Voltage Settling Time	5.59 s
Ripple	9.37 mV

Figure 68 depicts the output voltage of the Energy Module in the **FS process corner**:

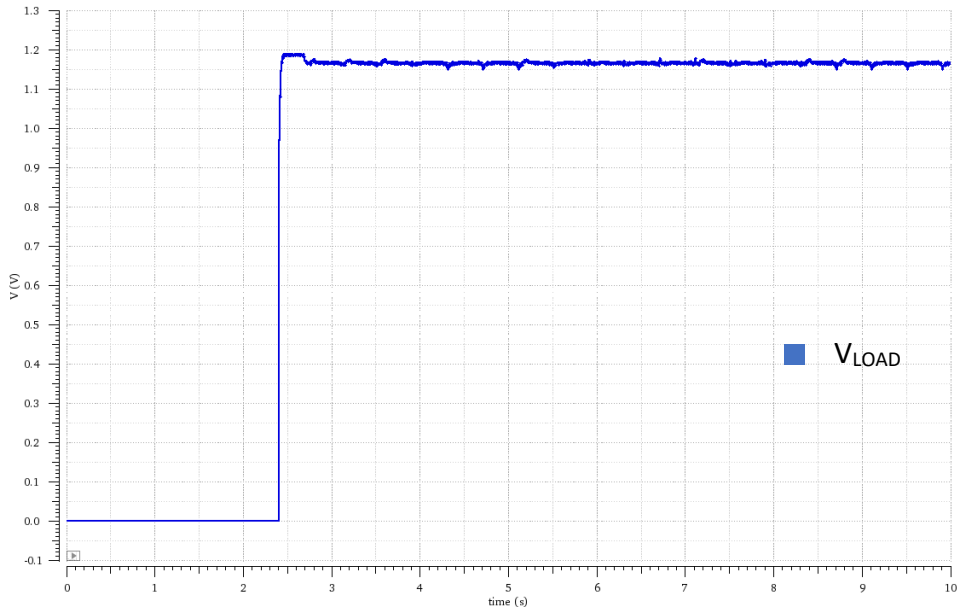


Figure 68. Energy Module load voltage and output capacitor voltage at FS process corner

Output specifications of the Energy Module, simulated above, is given in Table XXXVII as:

TABLE XXXVI. Energy Module output specifications (FS Corner)

Parameter	Value
V_{PIEZO}	300 $mV_{PEAK(2.5\ Hz)}$, 100 $mV_{PEAK(5\ Hz)}$
PEH Power Consumption	256.1 pW
V_{TEG}	25 mV
V_{Load}	1.17 V
TEG Input Power	3.47 uW
TEG Output Power	1.36 uW
TEG Power Conversion Efficiency	39.19 %
No. of PEH excitation cycles needed	6
Load Voltage Settling Time	2.41 s
Ripple	26 mV

Hence, the proposed Energy Module is able to perform well in the TT, FF & FS process corners, as was expected, with a constant output voltage of ~ 1 V while delivering ~ 1 uA current to the load, that also verifies the concept of the proposed Cold Start-up. For the simulation runs in the SS & SF process corner, it was found that the IC would need to be optimized further. In these corners the current consumption of the circuit decreases considerably, thus the circuit, in this case the bootstrap feedback, although has a high output voltage but it has a really low current drive. The circuit can only give what it can take, right! Thus, in order to maintain the capacitor at a constant voltage, the feedback took a lot of current from it with regards to the supply voltage it had. Thus, the capacitor was not able to deliver a constant load current of 1 uA. This was also evidenced in simulations as the output capacitor's voltage was maintained at 1 V but it didn't have sufficient power to drive the load. This problem was also faced with the Cold Start-up system in the SS & SF corner, thus a higher voltage of PEH excitation was given. In this case the PEH rms voltage was increased by 36.5 mV. Due to lack of time in this thesis work, the observed problem and its recommended solution (given in Chapter 6) is left to be addressed in future works. This observation, although not favorable, still verifies a claim made in Section 4.13 about the VLD preventing the Energy Module to power the load in case of insufficient power on the output capacitor even when its voltage is 1 V.

2. Performance under different input TEG voltages:

Figure 69 presents the output voltage of the Energy Module at **V_{TEG} = 18 mV** with a load of 3 MΩ:

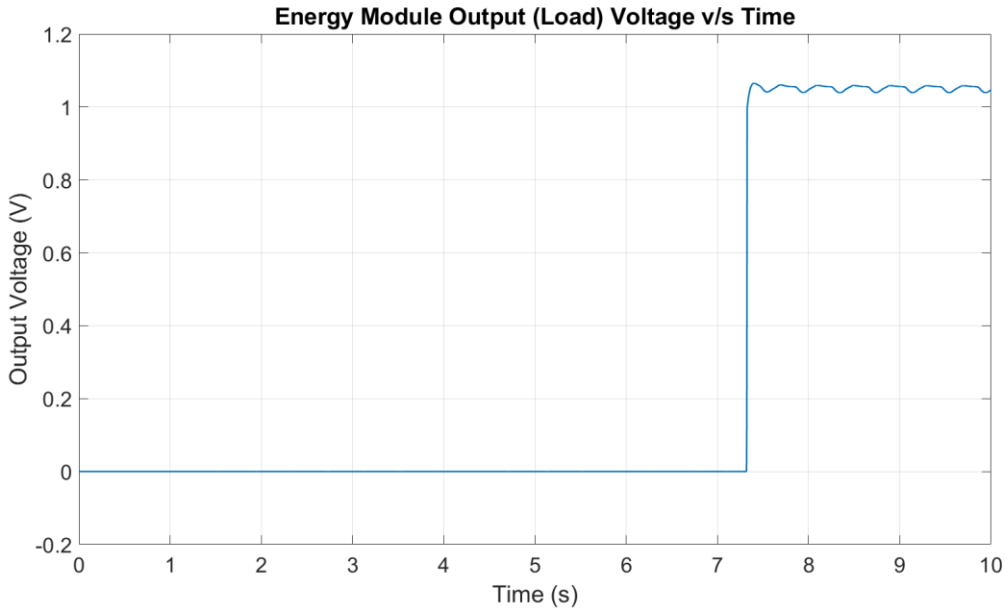


Figure 69. Energy Module output voltage at V_{TEG} = 18 mV

Figure 70 presents the output voltage of the Energy Module at **V_{TEG} = 20 mV** with a load of 2 MΩ:

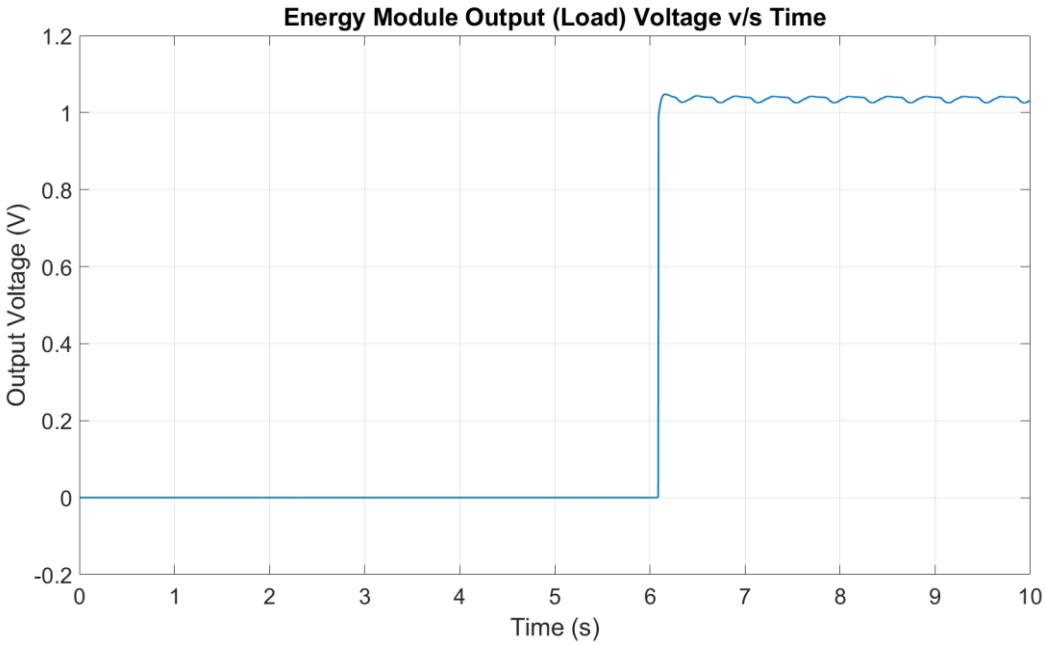


Figure 70. Energy Module output voltage at V_{TEG} = 20 mV

Figure 71 presents the output voltage of the Energy Module at **V_{TEG} = 15 mV** with a load of 10 MΩ, only this time with V_{PIEZO} = 400 $mV_{PEAK(2.5\ Hz)}$ & 133 $mV_{PEAK(5\ Hz)}$ as:

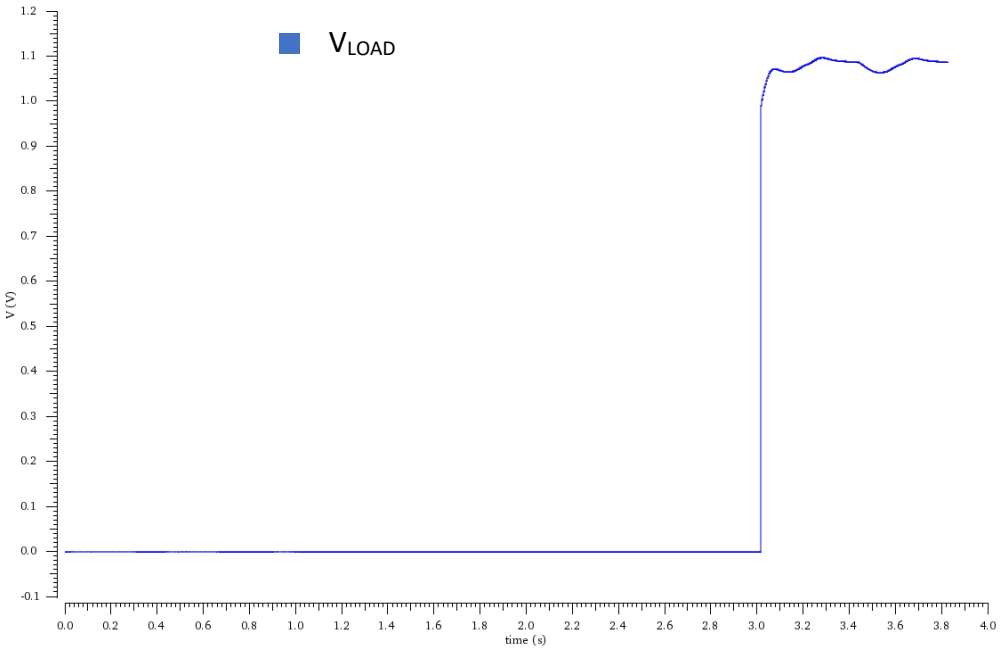


Figure 71. Energy Module output voltage at V_{TEG} = 15 mV

Output specifications of the Energy Module for different V_{TEG}, is given in Table XXXVIII as:

TABLE XXXVI. Energy Module output specifications at different V_{TEG}

V_{TEG} (mV)	R_{LOAD} (MΩ)	V_{LOAD} (V)	P_{PIEZO} (pW)	P_{IN} (uW)	P_{OUT} (uW)	Power Conversion Efficiency (%)	Ripple (mV)
15	10	1.08	503.2	0.55	0.12	21.8	28
18	3	1.05	231.6	0.84	0.37	44	19.5
20	2	1.04	234	1.08	0.54	50	17.3
25	1	1	240.5	1.77	1	56.5	12.4
50	1	1.25	252	3.72	1.55	41.7	7
100	1	1.47	258.3	7.96	2.16	27.1	8.5

Please Note:
V_{PIEZO} = 300 $mV_{PEAK(2.5\ Hz)}$ & 100 $mV_{PEAK(5\ Hz)}$ for cases of V_{TEG} = 18 mV – 100 mV
V_{PIEZO} = 400 $mV_{PEAK(2.5\ Hz)}$ & 133 $mV_{PEAK(5\ Hz)}$ for V_{TEG} = 15 mV
R_{IN} = 4.5 Ω for cases of V_{TEG} = 20 mV – 100 mV, while R_{IN} = 4 Ω for cases of V_{TEG} = 15 mV – 18 mV

It may be worthwhile to note that with respect to the discussion in Section 2.2 and figure 6, the issue and the subsequent limitation in the minimum Cold Start-up voltage and power has been successfully addressed with the help of the proposed Energy Module. With regards to the simulations in figures 69-71, it can be observed that the minimum Cold Start-up voltage has been pushed down to 15 mV while the output voltage remained maintained at 1 V. In this case, the piezoelectric excitation voltage was raised, although one could also increase the inductor value to achieve even lower TEG voltages, as has also been seen in simulations while experimenting with the converter. Considering power output, the bootstrap feedback circuit still has room to be optimized further to allow for a higher output power and efficiency. At this point, it falls out of the scope of this work to focus on such parameters.

Figure 72 shows a plot of power conversion efficiency with varying V_{TEG} for the proposed Energy Module:

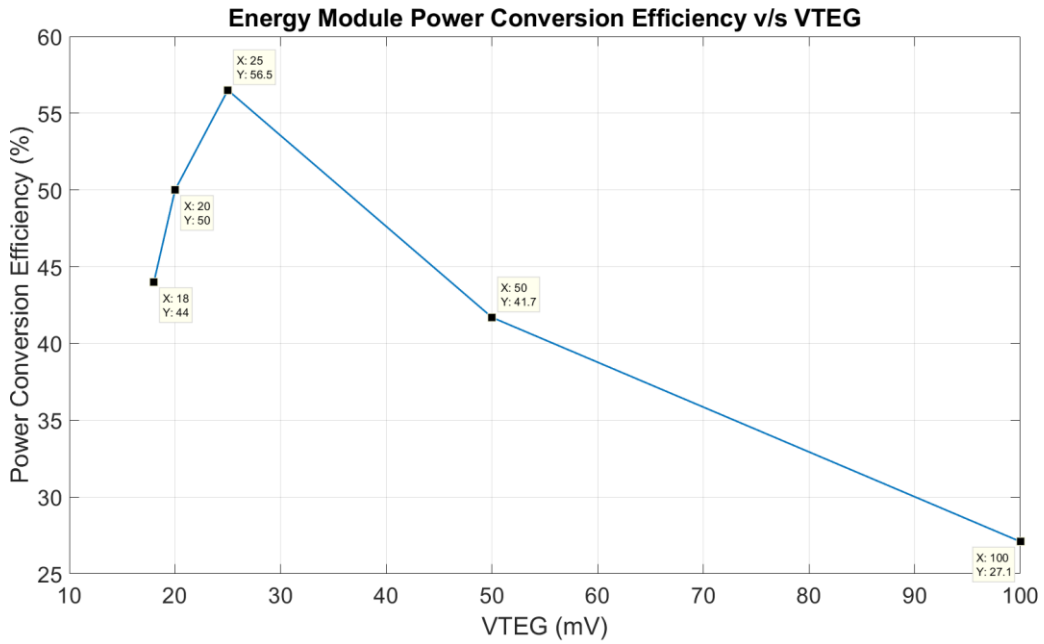


Figure 72. Plot of Energy Module's power conversion efficiency with different V_{TEG}

The fall in efficiency, as observed in the figure above, at high V_{TEG} can be attributed to the fact that the output voltage is held at a constant voltage at a constant load, while due to an absence of a precise VCS control circuitry there is nothing much that can be done with respect to either varying the switching frequency or it's duty cycle to control the efficiency of the entire power conversion process or even the output voltage. The present bootstrap feedback only ensures, with respect to its high oscillation frequency, that the output voltage does not exceed 1 V or the oscillation frequency becomes too large for the inductor to follow, forcing the output voltage to fall to 1 V again. However, it may be noted that for temperature differences of up to 2 K (V_{TEG} = 50 mV), the proposed Energy

Module performs quite satisfactorily with a converter efficiency > 40 %. Performance up to this temperature difference range should be acceptable as it presents a more realistic scenario.

3. Performance under different input resistances comprising of TEG source & inductor parasitic resistance:

Output specifications of the Energy Module for different R_{IN}, is given in Table XXXIX as:

TABLE XXXIX. Energy Module output specifications at different R_{IN}

R_{IN} (Ω)	PEH Excitation Cycles	V_{LOAD} (V)	P_{PIEZO} (pW)	P_{IN} (uW)	P_{OUT} (uW)	Power Conversion Efficiency (%)	V_{LOAD} Settling Time
4.5	9	1	240.5	1.77	1	56.5	3.6
5	9	1	240.5	1.78	1	56.1	3.6
5.5	9	1	240.5	1.78	1	56.1	3.62
6	9	1	240.5	1.79	1	55.9	3.64
6.5	9	1	240.5	1.79	1	55.9	3.64
7	9	1	240.5	1.79	1	55.9	3.64
7.5	9	1	240.5	1.79	1	55.9	3.67
8	9	1	240.5	1.8	1	55.5	3.69
8.5	9	1	240.5	1.8	1	55.5	3.71
10	9.5	0.99	240.5	1.8	0.98	54.4	4.17
15	10	0.98	240.5	1.82	0.96	52.7	4.17
20	10.5	0.96	240.5	1.84	0.92	50	5.13

Please Note: R_{LOAD} = 1 MΩ, V_{TEG} = 25 mV, V_{PIEZO} = 300 $mV_{PEAK(2.5\ Hz)}$ & 100 $mV_{PEAK(5\ Hz)}$ for all cases above

Figure 73 shows a plot of power conversion efficiency with varying R_{TEG} for the proposed Energy Module where it can be noted that even with ΔR_{IN} = 15.5 Ω, the variation in V_{OUT} = 0.04 V and efficiency = 6.5 % which makes the proposed energy module quite reliable with inconsistent R_{IN}:

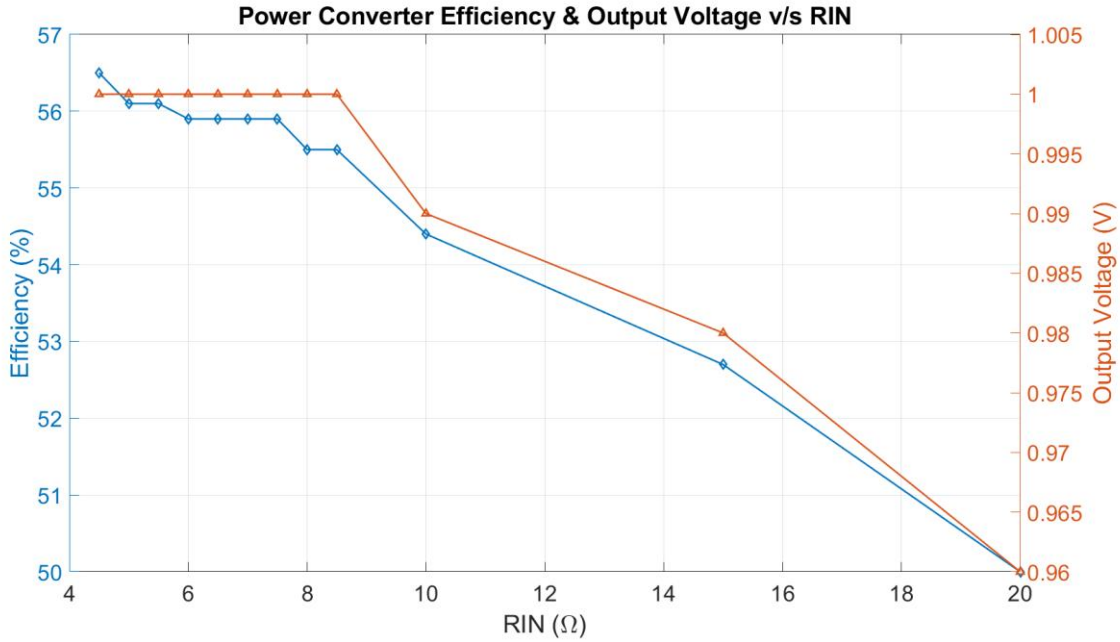


Figure 73. Plot of Energy Module's power conversion efficiency with different R_{IN}

Hence, a low Q-factor inductor would not be able to affect the operation of the proposed Energy Module to a large extent.

4. Performance under highest expected PEH excitation voltage, V_{PEH} = 1 $V_{PEAK(2.5\ Hz)}$ & 0.33 $V_{PEAK(5\ Hz)}$

Figure 74 presents the output voltage of the Energy Module at V_{TEG} = 25 mV with a load of 1 MΩ:

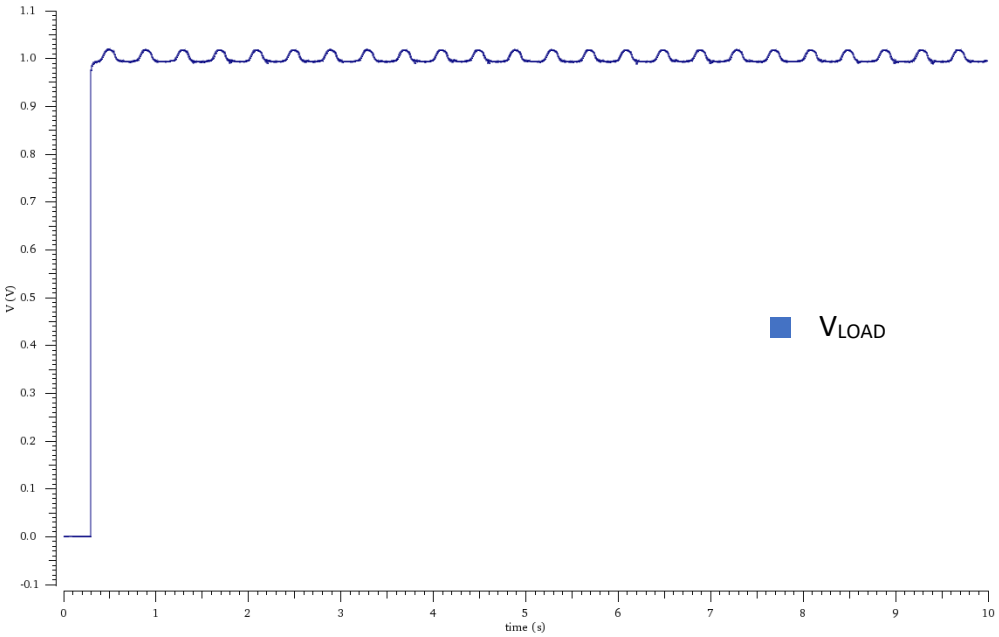


Figure 74. Energy Module output voltage at V_{TEG} = 25 mV with the highest expected PEH excitation voltage

Output specifications of the Energy Module at maximum PEH excitation, is given in Table XL as:

TABLE XL. Energy Module output specifications

Parameter	Value
V_{PIEZO}	1 $V_{PEAK(2.5\ Hz)}$, 0.33 $V_{PEAK(5\ Hz)}$
PEH Power Consumption	3.95 nW
V_{TEG}	25 mV
V_{Load}	1 V
TEG Input Power	1.79 uW
TEG Output Power	1 uW
TEG Power Conversion Efficiency	55.9 %
No. of PEH excitation cycles needed	1
Load Voltage Settling Time	295.4 ms
Ripple	28.4 mV

Please Note: R_{LOAD} = 1 MΩ

It may be worthwhile to note that as expected from the SR-DRVM architecture, its output voltage and consequently the supply voltage to the CSRO did not exceed maximum voltage ratings for the gate-voltage of the respective MOS-Ts employed in there. The maximum supply provided by the SR-DRVM stages and thus, oscillation-voltage output of the CSRO delivered to the VCS gate was 500 mV which is well within the maximum ratings. Hence, the proposed architecture would be safe to use even in cases of accidental high-impact PEH excitation scenarios.

At this point, it might be important to observe the individual power consumption of each circuit block designed in this work for possible propositions on future work, given in Table XLI:

TABLE XLI. Energy Module individual circuit block power consumption

Circuit Block	Power Consumption
VLD (V_{DETECT} = 251 mV)	0.67 pW (Peak)
Cold Start-up CSRO (V_{SUP} = 320 mV)	8.72 pW
Cold Start-up (V_{PIEZO} = 300 $mV_{PEAK(2.5\ Hz)}$, 100 $mV_{PEAK(5\ Hz)}$)	240.5 pW
VLD (V_{DETECT} = 404 mV)	8.9 pW (Peak)
VLD (V_{DETECT} = 991 mV)	4.94 nW (Peak)
Bootstrap Feedback (400 mV – 1 V)	0.25 nW – 37.19 nW

Please Note: Evaluation conditions of V_{TEG} = 25mV, R_{LOAD} = 1 MΩ, TT corner case for all observations above

Table XLII presents a comparison of the performance of the proposed work with respect to the existing state-of-the-art:

In the table, there are some terminologies used, that need attention as follows:

a. End-to-End power conversion efficiency: is defined as the power output of the converter as compared to the maximum available power that can be harvested from the TEG source, i.e.

$$\eta_{e-e} = \frac{P_{OUT}}{P_{\max\,(TEG)}} \tag{23}$$

Where,

$$P_{max} = \frac{P_{TEG}}{4} \tag{24}$$

b. DC-DC boost converter efficiency: is defined as the efficiency of the power converter to transfer the available power from the TEG source to the load, this available power is generally regarded to be less than $P_{max(TEG)}$.

From Table XLII, it can be noted that most of the literature available presents their max. or peak efficiency at a voltage that is quite infeasible for body wearable applications, i.e. V_{TEG} > 100 mV. Moreover, to attain a V_{TEG} of that magnitude could already mean that the wearer, in our case the little girl from Chapter 1, is in an alarming medical situation. Since V_{TEG} corresponding to that magnitude implies, in most cases, a temperature gradient of more than 4 K, between the body and its ambience, that is quite undesirable for any human, healthy or not. Hence, as a proposal for future research works, this thesis recommends for the optimization of power conversion efficiencies for V_{TEG} < 100 mV.

Hence, as can be observed from Table XLII, the proposed Energy Module fares well with its contemporaries. With regards to the minimum Cold Start-up voltage and the minimum power that could be harvested from the energy source, be it the piezoelectric element (231.6 pW for V_{TEG} = 18 mV at V_{PIEZO} = 300 $mV_{PEAK(2.5\ Hz)}$ & 100 $mV_{PEAK(5\ Hz)}$) or the thermoelectric element (840 nW for V_{TEG} = 18 mV & 550 nW for V_{TEG} = 15 mV), the proposed Energy Module is able to prove its purpose of addressing the fundamental limitation encountered in this domain and justifies its concept under different test case scenarios. The fundamental limitation being in the minimum voltage and power that could be harvested from an energy harvesting element with respect to the circuit techniques that could be invented to address it, fundamentally and practically. Note that even under the SS & SF corner simulations, the output capacitor was still charged to 1 V although it was not able to deliver 1 uA of current, which is more of an optimization issue that could be dealt with through proper converter-feedback tuning and does not impose any major hurdles for the validation of the concept from a more fundamental and practical point of view.

With respect to minimum voltage and minimum power harvested from the TEG & the PEH as well, the Energy Module presents a potentially favorable scenario that has never been observed before.

TABLE XLII. Comparison of the presented work with state-of-the-art thermoelectric energy harvesting power management ICs

Parameters	Im [29]	Garcha [30]	Teh [31]	Dezyani [32]	Lim [33]	Weng [34]	Chen [35]	Goeppert [36]	Ramadass [37]	This Work
Process	130 nm	180 nm & 600 nm	130 nm	180 nm	65 nm	65 nm	65 nm	130 nm	350 nm	180 nm
Start-up Mechanism	TOM Technique	TOM Technique	TBC Technique	Charge Pump + Oscillator	Charge Pump + Oscillator	Charge Pump + Oscillator	Charge Pump + Oscillator	Charge Pump + Oscillator	MEMS Mechanical Switch	Piezoelectric Energy Harvester
Min. Start-up Voltage	40 mV	50 mV	21 mV	60 mV	40 mV	50 mV	80 mV	70 mV	35 mV	18 mV
Output Voltage	2 V	1.2 V	1 V	1 V	1.1 V	1.2 V	1.3 V	1.25 V	1.8 V	1 V
$P_{START-UP}$	> 12 nW	NA	NA	NA	NA	16 uW	NA	NA	0	231.6 pW
Efficiency @ $V_{START-UP}$	37.5 % @ $V_{START-UP}$*	NA	70.5 % @ $V_{START-UP}$**	33 % @ $V_{START-UP}$**	10 % @ $V_{START-UP}$*	65 % @ $V_{START-UP}$**	60% @ $V_{START-UP}$**	58 % @ $V_{START-UP}$**	> 50 % @ $V_{START-UP}$*	44 % @ $V_{START-UP}$**
Max. Efficiency	61 % @ 300 mV*	NA	74.5 % (Unspecified) *	47 % @ 300 mV**	75 % @ 150 mV*	73 % @ 200 mV**	72 % @ 50 mV	58 % @ $V_{START-UP}$**	58 % (Unspecified) *	56.5 % @ 25 mV**
MPPT	YES	NO	YES	NO	YES	NO	NO	NO	YES	NO
# Inductors / Transformer	Transformer	On-chip Transformer	Transformer	1	2	4	1	1	3	1

Please Note: * - End-to-End power conversion efficiency, ** - DC-DC boost converter efficiency

5 Conclusion

In a nutshell, the essence of this work can be found in the methodology with which the Cold Start-up system is approached and that forms the substance of innovation proposed in this thesis. For over a decade, researchers have focused on addressing the fundamental limitation for this Cold Start-up circuit with a singular focus of getting to lower harvestable voltages, employing and innovating circuit techniques in the process that could just squeeze out the minimum possible voltage. In due course of time, the singularity became too focused on the minimum voltage figure, that many works lost sight of the fundamental limitation itself. Hence, this limitation deserves a special note here, as:

> "Generation of a well-timed signal that could potentially drive a boost converter composed of any of the switched capacitor or switched inductor or transformer based architectures to convert an ultra-low DC voltage into a desired waveform, DC or AC, of a specific amplitude to power the load"

The entire ordeal of this Cold Start-up quest is thus, about utilizing the available voltage from the thermoelectric element to generate a timing waveform, that could drive a switched converter to boost up this TEG voltage to a desired value. The solution this thesis proposes, is to utilize another equally abundant source of energy from the body and ask the nature itself to aid in the Cold Start-up. In the presented case, this abundant source of energy is the mechanical vibrations a human body produces, when doing possibly anything. While the aid that nature provides, is in manifesting itself in the various phenomena that allow a possibility to harvest a well-timed AC waveform from those vibrations. This well-timed AC waveform, in the present work, is harvested by employing a piezoelectric element, capable of harvesting even several Hz of vibrational frequencies. Now that the timing waveform is already being catered to by another harvesting source, the fundamental limitation imposed on the TEG source could be lifted off. Hence, the current work finds itself capable of standing out from the contemporary works in achieving the lowest Cold Start-up voltage with respect to the TEG element. Even for the sub-uW power the proposed Energy Module is shown to harvest (from the TEG source), it is simply this precise understanding of the problem and the simplicity of the solution proposed, that enables it.

However, with regards to the Cold Start-up, it is the Concept of Self-Reconfigurability and the SR-DRVM architecture that can be attributed for its ultra-low power operation. This concept in itself is a result of inquiring into the problem of Cold Start-up from a more system oriented point of view. Moreover, even the implementation of this concept was carried out considering its operation initially at the fundamental level to develop circuit techniques, prior to actually referring to what the literature had in offer. This allowed for the employment of uninvolved circuit techniques to address the issue of ultra-low current and high voltage output of the DRVM stages, that finally rendered the entire design to operate at sub-nW levels of power. Circuit concepts regarding reconfigurable charge pumps exist [38,54,55,57], although they often require a complex logic or a DSP based implementation that not only increases the overall power consumption, but also leaves the system more intricate and difficult to design. Such systems have never been shown to be exhibiting behaviour such as the proposed SR-DRVM in terms of being load-variation-resistant and being able to autonomously 'sense & react' to varying input and output conditions, for which the system is not programmed (in case of contemporaries). Moreover, the SR-DRVM architecture also proves to be quite reliable with respect to high impact PEH excitations, not allowing the output voltage of the DRVM stages to exceed maximum limits, thus preventing potential gate-oxide breakdown.

A major role in the design of the complete system, was played about by the realization that parasitics such as the series resistance of inductor and the 'ON' resistance of the MOS-T switches dictate the performance of the design at ultra-low power domains. Since the state-of-the-art equations does not take into account such parasitics, assuming them to be non-existent, they could not be used in the design process. This propelled the study to come up with its own mathematical analysis for the operation of the boost converter in the presence of non-ideal parasitic resistances, specially of the VCS MOS-T. The study dealt with the boost converter in steady-state operation and analysed the system from an energy transfer perspective. The results of this derivation were further verified with respect to circuit simulation results under similar conditions. Also, it should be noted here that since the parameters of the boost converter like the inductance and the switching frequency were solely decided by the derived equations to achieve the desired output voltage from such ultra-low input voltages, efficiency of the boost converter remained

limited to the reported value. The obtained efficiency also stems from the fact that a more precise control-feedback was indeed needed that could have varied the duty cycle of operation along with the switching frequency to achieve a more efficient value of power conversion, which fell out of the scope of this work.

Finally, the proposed Energy Module employed a bootstrap feedback implementation. Such an approach allowed the output capacitor to take the reins of the converter and pull itself up from an intermediate value of 400 mV to the desired value of 1 V. Once again in this case too, the power consumption of this bootstrap feedback was kept to a minimum by employing only two circuit components to lay out the entire operation. At the core of this feedback was a voltage controlled oscillator (CSRO) that depending upon the output capacitor's voltage varied its frequency. For a higher value of capacitor voltage the switching frequency increased, leading to the inductor of the boost converter not being able to follow it, thus decreasing the output voltage of the capacitor and vice versa for a lower value of capacitor voltage. The second component of this feedback was the current limiter that essentially restricted the CSRO from consuming just any amount of current from the output capacitor. This was done so that the CSRO does not drain the output capacitor or go haywire with its centre frequency from several KHz to several GHz, which could have degraded the entire feedback operation instead (low or no output voltage).

The Energy Module was tested under different conditions of varying input voltages, input resistances, process corners and PEH excitations to ascertain whether it will be able to stand up to the expectations. For the case of varying input voltages and input resistances, the converter performed well matching up to the expectations, providing a constant supply of 1 V with not much degradation in its efficiency. The credit here can be attributed to the mathematical analysis that allowed for the assumed values of the different components of the boost converter and the bootstrap feedback that led to a fast settling of the output voltage to the desired value. For catering to the impact of the high PEH excitations and the performance under the different corners the major contribution was laid out by the Cold Start-up system which was able to function well beyond expectations. The SR-DRVM architecture in such cases proved to serve its purpose quite elegantly, by always being able to drive the VCS MOS-T in all the process corners (TT, FF, SS, SF, FS) and high impact PEH excitations, ensuring maximum limits are respected. Although the system was not able to provide the load with 1 uA of current in the SS and SF process corner, still it did serve a purpose of validating a claim from the load-connection module's perspective. The claim was that the system would not power the load even if it reaches 1 V if it cannot deliver the required current to it, thus potentially eliminating the need for a separate PoR circuit. In cases where the load is still driven without sufficient power being available, it could easily lead to a degradation in the performance, which is highly undesirable in biomedical monitoring applications. Such reduction in performance may lead to false alarms regarding a patient's health or missed alarms when a patient's health actually needed to be checked, that in itself is alarming. Recommendation section of the next chapter discusses on improving the operation of the proposed Energy Module in the SS and SF corner.

Hence, it can be concluded that the proposed Energy Module:

1. Validates the concept it was designed for, successfully addressing the fundamental limitation
2. Proves its reliability with respect to input resistance variations, considering the constant voltage output along with a small degradation in converter efficiency
3. Can be driven for the entire expanse of temperature variations a human body can go through, i.e. 0.1 K – 4 K (V_{TEG} = 18 – 50 mV) while providing a constant 1 V output at its load to drive it successfully
4. Can successfully work for different PEH excitation source voltages while allowing the circuit to operate well within the maximum limits
5. Is able to deliver performance in the TT, FF, FS process corners while the Cold Start-up system is able to deliver on its promise in all the process corners
6. Allows to harvest 840 nW of power at a minimum TEG voltage of 18 mV, to drive a load at 1 V
7. Allows to harvest 231.6 pW of power at a minimum PEH excitation frequency of 2.5 Hz (human body vibrations), while driving the boost converter successfully
8. Delivers on its promise and the target of this work, to perform at a temperature difference of 0.45 K, at 25 mV of TEG source voltage to deliver an output voltage of 1 V to a load deriving 1 uA of current from the TEG source.

6 Research Contributions & Future Work

Research contributions of the presented work are listed below with respect to the chapters in which the entire work was laid out:

1. **Chapter 1**: The plot presented in figure 1 regarding the 'Energy Harvesting Sources - Trends' shows how the state-of-the-art has evolved over the past few decades with respect to the emergence of different energy harvesting techniques and their respective follow-up till early 2019. An idea on the feasibility of the different techniques can be gathered from this plot with respect to how much following it could inspire in the end. A total of 500 research articles from IEEE Xplore were analysed to complete this plot.

2. **Chapter 2**:
   a. The plot presented in figure 6 regarding the 'Start-up Voltage Trends' shows how the state-of-the-art has developed over the past decade with respect to the different fundamental techniques invented to cater to the problem that Cold Start-up presents. Here, it can be noted that the research has mostly saturated with most of the literature only focusing to achieve a better start-up voltage with regards to the 4 established techniques that were already propounded more than half a decade ago. As a result the minimum start-up voltage remained to be at 21 mV over the last 4 years with most of the research work exploring the extent of these established techniques now. Research articles from IEEE Xplore were looked into to complete this plot.
   b. The Cold Start-up architecture comparison discussed in Section 2.2. gives a brief overview and analysis on the working of the different architectures predominantly employed in the literature. The discussion strives to present the elegance and drawbacks of these architectures with respect to a fundamental and practical perspective, and analyses why the research works have stagnated with the minimum start-up voltage and power that they respectively could harvest with respect to the discussed techniques. So far, such a study has never been presented before on this topic, as per the authors knowledge.
   c. The proposal to decouple the TEG from the Cold Start-up and to employ a PEH instead to take care of it, is the major novelty propounded in this chapter. This proposal also allows the TEG signal path to directly contribute all of its energy to the output load, not wasting any on the Cold Start-up operation thus potentially improving efficiency from the very first instance.
   d. Alternative techniques are discussed in Table X that lead to the selection of an approach called 'Absorption', that forms the basis of the Concept of Self-Reconfigurability proposed in the next chapter. Such an approach, from an architecture level perspective, has never been discussed in the literature before and thus, allowed to come up with the said concept for the first time in this work.

3. **Chapter 3**:
   a. The comparison of the different RVM architectures from the architecture level down to the implementation level as shown in Table XI.
   b. The Concept of Self-Reconfigurability allowing the DRVM stages to arrange themselves in series and parallel depending on the input conditions is a major novelty proposed in this chapter.
   c. The operation of the voltage level detector (VLD) from a fundamental perspective.
   d. Bootstrap Feedback proposal with the output capacitor controlling the converter from an intermediate voltage level with the help of a VCO to boost and monitor its own voltage. Contemporary works focus on implementing a similar solution only after the capacitor is charged to its maximum desired value. What this approach proposes is that, by allowing the capacitor to take control at an intermediate step permits a faster autonomy of the operation from the Cold Start-up which in this case also reduces the number of cycles and thus, time to get the desired output voltage.
   e. The PEH is proposed to be used for HARKE, after it completes its Cold Start-up obligations.

4. **Chapter 4**:
    a. One major contribution proposed in this chapter is the mathematical analysis with respect to the presence of parasitic resistances of a boost converter. These resistances start playing a significant role in deciding the converter output at ultra-low power operations and thus can easily degrade the output. Since state-of-the-art equations are derived assuming an ideal converter and thus, non-existent parasitics, they do not hold in such applications. Thus, this research was motivated to take a different analysis route to derive the equation for output voltage. The derived equations have compared well with respect to circuit simulations and are responsible for the ultra-low TEG source voltage and power operation of the proposed Energy Module.
    b. The research approaches using the PEH element from a different perspective, i.e. utilizing the first two harmonics of the produced excitation source voltage. Contemporary works only focus on employing the PEH at its resonance frequency such that they can get a higher excitation without having to deal with the PEH source parasitics such as the C_{PIEZO}. However, that is not a realistic case scenario to assume since the human body vibrates at frequencies close to 2-2.5 Hz and currently no piezoelectric element is available to resonate at those frequencies. Hence, using the 2-Harmonic approach with minimum PEH source voltages of 300 mV_{PEAK} at 2.5 Hz & 100 mV_{PEAK} at 5 Hz along with a PEH model using a R_{PIEZO} = 1 MΩ and C_{PIEZO} = 4.5 nF in itself is a major novelty that this work proposes, making it more realistic.
    c. Self-Reconfigurable Rectifier-cum-Voltage Multiplier (SR-RVM): This is a major novelty proposed in this research work. It essentially is a 'sense & react' architecture that can arrange its various stages in series and parallel configurations to allow for a constant output voltage while reacting to the different input voltage conditions. The proposed architecture was also simulated and verified to support different loading conditions while providing a constant output voltage with a power output that increased with increasing load demands, employing a load step-up technique, all while maintaining an almost constant efficiency throughout. Hence, the SR-RVM architecture renders itself load-variation-resistant and opens up possibilities for designing an RVM architecture that could basically be PVT resistant. This is for the first time such an architecture is proposed in the literature, to the best of the author's knowledge.
    d. Current-Limited CSRO: This work proposes to use a current limiter to tightly constrain the CSRO within a set values of current consumption and consequently a defined set of values the centre frequency will be allowed to vary with respect to the changing supply voltage.
    e. Power Module Load Connection: The proposal is to allow the load to be independent of the Energy Module output voltage if this voltage is not sufficient of the Energy Module cannot deliver the required amount of current to the load. This approach has the potential to eliminate the need for a separate PoR circuit and allow the 'OFF' state power consumption of the load to be 0 since it would be connected to ground.

5. **Specifications**:
    a. One major contribution this work strives to accomplish is rooted in the fact that the value of minimum source power that can be harvested from an energy harvesting source has been pushed down with significant margins to:
        i. Piezoelectric Energy Harvester: The IC designed in this work has been simulated to shown that it is capable of harvesting a minimum of 231.6 pW of power from the PEH, operating at 'near' DC frequencies of 2.5 Hz & 5 Hz. This has previously never been demonstrated in the literature before.
        ii. Thermoelectric Energy Harvester: In this regard too, the designed IC is able to stand-out when compared to contemporary designs being able to harvest a minimum power of 840 nW from the TEG to deliver an output power 370 nW with a converter efficiency of 44 %, that has also never been reported before.
    b. The output voltage of the Energy Module was maintained at ~1 V while ~1 uA of current was delivered to the load, for V_{TEG} variations ranging from 25 mV to 50 mV corresponding to temperature gradients from 0.45 K to 2 K, making it quite reliable to temperature variations.
    c. The variation in output voltage and boost converter efficiency with regards to an inconsistent R_{IN} varying from 4.5 Ω to 20 Ω was found to be ΔV_{OUT} = 0.04 V and ΔEfficiency = 6.5 %, which renders the Energy Module quite stable with respect to low Q-factor inductors.
    d. The minimum TEG Cold start-up voltage achieved by the design was 18 mV. This figure was also shown to be decreased further to 15 mV with a slightly higher PEH excitation voltage.

Also, even lower Cold Start-up voltages could be harvested with the proposed architecture by employing higher inductor values if high PEH excitations are not feasible.

e. The minimum PEH excitation voltage needed to start-up the entire architecture was found to be V_{PIEZO} = 300 $mV_{PEAK(2.5\ Hz)}$ & 100 $mV_{PEAK(5\ Hz)}$. This is the lowest PEH voltage that is harvested as of yet for a complete on-chip implementation.

Recommendations for Future Work are listed below:

1. The performance of the Energy Module could be improved in the SS & SF process corner with respect to supplying 1 uA to the load. In order to do this, one recommendation is to look into the bootstrap feedback circuit and check for possible tuning of W/L ratios of the MOS-Ts in the buffers that follow the CL-CSRO. If the buffer MOS-Ts loading the CL-CSRO can be tuned to be strong enough to pull-down adequate current from the capacitor so as to sufficiently drive the VCS MOS-T, than the problem could be solved without any major circuit modifications. In case this does not work, then the proposal made by Dezyani et. al. in [32] on a process corner detection circuit can be looked into to derive inspiration to design a similar circuit for this case, allowing the operation in the SS & SF corner without increasing the source voltage of the TEG or the PEH.
2. After the problem of powering the load in the SS & SF corners is tackled, designing the layout and completing the post-layout simulations is recommended before the IC is given for a possible tape-out. In the present work, since the IC was not supposed to be given for a tape-out, due to time considerations, laying-out the circuit was not considered.
3. Finally, if the chip is taped-out, measuring it is recommended to ascertain whether the figures obtained from the simulations can hold as well on the fabricated chip. Fabrication in itself is only a step towards verifying the simulations and as such does not propose any innovation with respect to the IC design itself, i.e. it does not validate a concept but a numerical figure to ascertain feasibility.
4. In order to increase the efficiency of the IC, one recommendation could be to implement an MPPT as the contemporary works do. The fundamental question here is, though, whether the source resistance of the TEG element would vary over a wide range or not. Provided that the TEG element would be used for body wearable applications and the temperature of the body does not vary by more than 2 K (up to 4 K if a person is diagnosed with fever), from the data sheet it could be seen that it's R_{TEG} hardly varies by any significant amount. For temperature differences from 0.1 K to 58 K, the variation in R_{TEG} is less than 1 Ω. Thus, a separate circuit for implementing an MPPT is rendered redundant. Instead, in this case, the author recommends adding another simpler circuit that ensures that the switching frequency and its duty cycle are at a value so as to provide the maximum harvester efficiency obtainable with the present component values of the boost converter, see [33] for reference. Note that once this circuit starts, the bootstrap feedback should be switched 'off'. [33] has achieved the highest efficiency following the abovesaid method.
5. Also, maximum efficiency of such Energy Modules should be designed for TEG voltages that would allow the IC to work at its max. efficiency at temperature differences of 0.1 K – 2 K and not for temperature differences of 5 K or more, as the contemporary works generally report for. Otherwise the IC could be rendered useless for realistic case scenarios. Also, some works [31] focus on reporting maximum efficiencies at TEG input powers in the range of several mW, so that even a microcontroller based MPPT architecture could be driven at such high input powers. This is again not a realistic scenario as the TEG presently available in the industry can support only 100 uW range of input powers at ultra-low TEG input voltages as discussed above.
6. Furthermore, it would also be interesting to check whether the proposed IC design would be able to work under different ambient temperatures. This was not done in this work due to the temperature variations on a human body are really minimal (0.1 K – 2 K) and as such it didn't make sense with respect to the time to check for large temperature variations.
7. The last recommendation would be to incorporate this proof-of-concept design into a more involved power module as was discussed in Chapter 1 – Section 1.7, to check whether the concepts formed in this project would be able to support such intense and demanding applications as a full-fledged biomedical device.

7 Bibliography

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Appendix A: Energy Harvesters

STATE-OF-THE-ART ENERGY HARVESTER COMPARISON

Energy Domain	Electromagnetic Radiation		Mechanical Vibration					Bio-Organic	Thermal Gradient	Electrochemical Gradient		
Energy Harvester	**Radio Frequency**	**Solar Radiation**	**Electromagnetic Vibration**	**Piezoelectric**	**Triboelectric**	**Ultrasound (US)**	**Magnetostrictive**	**Methanol-Feul Cell**	**Thermoelectric**	**Bio-Galvanic Cell**	**Glucose-Fuel Cell**	**Endocochlea**
Paper Title	A fully integrated 28nm CMOS dual source adaptive thermoelectric and RF energy harvesting circuit with 110mv startup voltage	Wide-input-voltage-range and high-efficiency energy harvester with a 155-mV startup voltage for solar power	A low-power integrated power converter for an electromagnetic vibration energy harvester with 150 mV-AC cold startup, frequency tuning, and 50 Hz AC-to-DC	A Parallel-SSHI Rectifier for Piezoelectric Energy Harvesting of Periodic and Shock Excitations	A 4.5-to-16µW Integrated Triboelectric EnergyHarvesting System Based on High-Voltage Dual-Input Buck Converter with MPPT and 70V Maximum Input Voltage	StimDust: A 6.5mm3, Wireless Ultrasonic Peripheral Nerve Stimulator with 82% Peak Chip Efficiency	Modeling and Design of an Efficient Magnetostrictive Energy Harvesting System With Low Voltage and Low Power	A 450-mV Single-Fuel-Cell Power Management Unit With Switch-Mode Quasi- V2 Hysteretic Control and Automatic Startup on 0.35-µ m Standard CMOS Process	A –8 mV/+15 mV Double Polarity Piezoelectric Transformer-Based Step-Up Oscillator for Energy Harvesting Applications	Prolonged energy harvesting for ingestible devices	A 6.1nA Fully-Integrated CMOS Supply-Modulated OOK Transmitter in 55nm DDC CMOS for GlassFree, Self-Powered, and Fuel-Cell-Embedded Continuous Glucose Monitoring Contact Lens	Energy extraction from the biologic battery in the inner ear
Paper Publication	CICC 2018	ESSCIRC 2017	CICC 2018	JSSC 2016	ISSCC 2018	CICC 2018	Trans. on Magnetics 2018	JSSC 2012	TCAS-I 2018	Nature BME 2017	TCAS-II 2018	Nature Biotechnology 2012
Start-up Voltage	85mV	155mV	150mV 50Hz AC	670mV	NA	NA	NA	450mV	31mV	0.1V-0.2V	NA	30mV
Power Output	520uW	60mW (50mA @ 1.2V)*	800uW	NA		142uW***	0.77mW Pavg (max. o/p by element)	200mW	NA	0.23uW/mm2 (load-transmitter)	2.3uW/cm2 (max. output by cell)	1.12nW(element) 60-2840pW(load)
Technology	0.028um	0.18um	0.18um	0.35um	0.18um	0.065um	standard components (no chip)	0.35um	0.32um	Commercially available components	0.055um DDC CMOS	0.18um
Input Voltage	85mV	20mV-1.7V	20mV	670mV	<70V	3V-5V	0.48 Vac(peak)	450mV-900mV	-8mV/+15mV	0.1V-0.2V	0.32V	30mv-55mV
Conversion Efficiency (EE)	10%	92,80%	71%(Resonance) 50%(Off-Resonance)	95.4% (chip) @ PIN=408uW**	51.10%	82%	44%	85.2% (Avg.) 89.4% (Max. @ 150mW)	NA	NA	NA	53.4% (BC)
Chip Area	0.46mm2 (w/o antenna)	899µm×837µm	1.5mm2	1.17mm2	2.844mmX0.776 mm	1mm2 (Chip) 6.5mm3 (Sensor Vol.)	5X5cm2 (sensor-PCB)	3.84mm2	2.25mm2	10mmX30mm (Sensor)	0.36mm2 (Chip) <1mm3(sensor)	11mmX9mm(sensor) 2.4X2.4X0.2mm3(chip vol.)
Output Voltage	-	1.8V	1.8V	0.7V-5V	1V-5V	Vstim = 2V(max) Output Current Istim = 48uA	3.3V(Rload=15k ohm)	2V	5V	2.2V-3V	NA	0.9V
Start-up Technique	Adaptive boost oscillator with Super-regenerative operation	Ring oscillator + Voltage multiplier	Meissner oscillator	Parallel-SSHI	Dual Input Buck with High Voltage Protection (Harvesting Technique)	Piezoelectric voltage generation on Ultrasound application (Harvesting Technique)	Batteries start-up the sensor and the sensor strives on vibrations that disturb the magnet-in-coil config. to generate	Subthreshold start-up	Double Polarity Piezoelectric Transformer-Based Step-Up Oscillator	Voltage generation through redox reaction in gastric fluid electrolyte, followed by boost conversion	Glucose oxidation (anode) & oxygen reduction (cathode) drive the fuel cell which is followed by boost operation.	Wireless kick-start energy reciever
Off-Chip (L+C+T)	None	1+2+0	1+2+1+2 MOSFET	1+3+0+6 Resistors	1+1+0	0+1+0	0+2+0+2MOST+ 2OPAMPS	NA	0+1+1 (Piezo)	1+1+1(Switch)+1(uP)+2(Resistors)+1(Crystal)	0+0+0	1+2+0

Start-up Technique in Literature (2010-18)	Published in different implementations	Published in different implementations	Published in different implementations	Published in different implementations	NA	Published in different implementations	Published in different implementations	Not much follow-up of the harvester	Published in different implementations except for the double polarity implementation	First Implementation as such	Techniques published in different implementations. This work has the first on-chip implementation (all components) in this	Published in different implementations
Circuit Complexity	High	Medium	High	High	Medium	High	Low	Medium	High	Low (due to the use of commercially available components)	Low	Medium
Requirement	Native NMOS	Mid-Vth MOSFET	Native NMOS	No Specific	No Specific	No Specific	No Specific	No specific	Native MOSFET	NA	Native MOSFET	No Specific

Comments	Dual source implementation with thermoelectric transducer	PFM with DCM to overcome limited available power from ambient energy	On-chip H-bridge circuit & Off-chip microcontroller for impedance matching and frequency tuning	Low-power active rectifier for AC/DC conversion with Optimal Power Point to execute maximum transfer of harvested power with single Inductor Sharing.	Synchronous Pulse Skipping Modulation (PSM) is used to drive the buck converter using the output voltage of Dual-Output-Rectifier (DOR) as a control in ZCS implementation.	The need for higher output voltage was eliminated through efficient fabrication of stimulation electrodes (Au electroplated with PDOT:PSS) which eliminated the need for high-voltage blocks by decreasing the stimulation headroom also contributing to overall chip efficiency. Thus, no voltage boosting circuits can be seen. Power & bidirectional comm. with US. Edge detection instead of clocks and i/p US structure controlled stim. waveform enable lower power consumption.	Materials - Terfenol-D & Galfenol. Model & Design of Magnetostrictive energy harvester exhibiting low input voltage & power. Results are for acceleration = 0.7g and Rload = 120ohm. Boost converter utilizes the built-in inductor of the energy harvesting element to perform the boost operation in DCM (fixed Duty cycle 0.7). External DC batteries are used for start-up of the entire sensor. 240uW dissipated by EH circuit with max 450uW. OPAMPs require +2Vsup/-2Vsup.	Single Direct methanol fuel cell (DMFC) implemented with switch-mode quasi-V2 hysteretic controlled PMU	Lowest start-up Voltage w/o magnetic components. CS Inverter leading to high input impedance for boost oscillator. 15nW Hysteretic voltage monitor. Schottky diode rectifier preferred over diode-connected MOSFETS due to low Vth.	Capsule powered by Zn-Cu cell in gastric fluid electrolyte. Voltage generated through the redox reaction is boosted by a low efficiency boost converter for strat-up which then shifts the conversion to a high efficiency one, once, sufficient voltage is acquired which then closes a switch to power a microcontroller(uP) that transmits temp. data at a variable rate based on input power. Potential to implement drug delivery in gold membrane is also shown that dissolves electrochemically.	The output power of the fuel-cell can always operate the entire sensor since human body glucose level is always greater than a certain threshold value. The boost converter is controlled by self oscillating voltage doubler which also ensures that the transmitter (through LC power oscillator) works even at low input voltages that cannot sustain the boost converter. Thus, glucose data can always be available at distances greater than 5cm. Also, frequency increases with input supply voltage.	Sensor drives its power from Endocochlear potential found in the inner ear. The potential is due to the electrochemical gradient present and actively maintained there. Addresses the lack of in-vivo demonstration of other energy harvesting sensors in the vicinity of ear and brain. 5h sensor operation in guinea pig with wireless data transmission @ 2.4GHz per 40-360s. Mechanotransconduction of sound pressure waves to neurotransmitter release and successive excitation of auditory nerves depends on EP. EP results from difference in ionic conc. of endolymph(K+) and perilymph. Wireless kick-start charging packet of 2s from external source to charge 200nF cap. to 1.4V. 573pW of system power consumption. Results are for short term (6h) only.

Appendix B: Cold Start-ups

The following Table presents a design arena from the perspective of the contemporary research, specially those, that have demonstrated state-of-the-art performance in the field of ultra-low power IC design for Cold Start-up applications (TEG), for a prospective IC designer to get started-up!

STATE-OF-THE-ART START-UP TECHNIQUES COMPARISON OVER THE YEARS												
Paper Title	A Battery-Less Thermoelectric Energy Harvesting Interface Circuit With 35 mV Startup Voltage	50 mV-Input Batteryless Boost Converter for Thermal Energy Harvesting	A Miniaturized 0.78-mW/cm2 Autonomous Thermoelectric Energy Harvesting Platform	A 25 mV-Startup Cold Start System With On-Chip Magnetics for Thermoelectric Energy Harvester	A −8 mV/+15 mV Double Polarity Piezoelectric Transformer-Based Step-Up Oscillator for Energy Harvesting Applications	A Thermal Energy Harvesting Power Supply With an Internal Startup Circuit	A 60mV Input Voltage, Process Tolerant Start-up System for Thermoelectric Energy Harvesting	Design of Transformer-Based Boost Converter With 21 mV Self-Startup Voltage	A Single-Inductor-Cascaded-Stage Topology for High Conversion Ratio Boost Regulator**	A High-Efficiency Energy Harvesting Interface for Implanted Biofuel Cell and Thermal Harvesters
Paper Publication	2011 JSSC	2013 JSSC	2017 T-BIOCAS	2017 ESSCIRC	2018 TCAS-I	2016 T-VLSI	2018 TCAS-I	2014 JSSC	2016 ICCD	2018 TPE
Start-up Voltage	35mV	50mV	65mV	50mV	31mV	60mV	60mV	21mV (LVLT)	NA	NA
Power Output	10uW(25mV) 300uW(100mV)	282.2uW	645uW (dT=3.5K)	NA	NA	130uW (max.)	4.5uW (max. @ min. Vin)	2mW	830uW (max.)	0.5uW(min)
Technology (CMOS)	0.35um	0.065um bulk	0.065um	0.18um (Switched Cap. DCDC) 0.6um(transformer+NMOS interface)	0.32um	0.18um	0.18um	0.13um	0.13um	0.18um
Input Voltage	25mV	30mV	32mV	25mV	-8mV/+15mV	40mV	50mV	1V (max.)	25mV	10mV(min) 60mV(typical)
Conversion Efficiency (EE)	58%	73%* (cnv)	68%	NA	NA	48%	47% (cnv.)	74% (LVZT)	74%	90%
Chip Area	1.6mm2 (Chip) 7.5cm2 (PCB)	1.05X0.95mm2 (Chip) 2.6X2.6cm2 (TEG)	1.4X1.4mm2 (Chip) 1cm3 Vol. (Sensor)	1.5mm2 (Transformer) <6mm2 (circuitry)	2.25mm2	No Fabricated Implementation	3.3mm2	1.5mmX1.5mm	0.42mm2	2.3mm2
Output Voltage	1.8V	1.2V	1.8V	1.2V	5V	1V-3V	1V	1V	3V	1.9V
Start-up Technique	MEMS Mechanical Switch	LC Oscillator with 12-Stage Voltage Multiplier	Inductive Load Ring Oscillator + Charge Transfer Switch Charge Pump	Meissner Oscillator with on-chip magnetics	Double Polarity Piezoelectric Transformer-Based Step-Up Oscillator	Ring Oscillator + Modified-Dickson Charge Pump	Standard CMOS Technology Modified Inverter Cell + off-chip Inductor	1:1 Transformer	Single-inductor-cascaded-stage topology (No cold start-up)	Shared inductor dual input dual output (No cold start-up)
Off-Chip (L+C+T)	3+4+0	3+4+0	1+2+0	0+0+0	0+1+1	No Fabricated Implementation	1+1+0	NA+NA+1	1+3+0+4 Resistors	1+4+0+1Switch
Start-up Technique in Literature (2010-18)	Widely followed-up paper but with not much follow-up on the Mechanical Switch technique	Published in different implementations	Published in different implementations	Published in different implementations w/o on-chip magnetics as this	Published in different implementations except double polarity	Published in different implementations	Published in different implementations with the cross-coupled Voltage Detector being the first of its kind. Also, process tolerent inverter cell implementation (for this case) has not been reported before.	Published in different implementations	Published in different implementations	Published in different implementations. First ever GBFC interface for implantable applications (highly efficient)
Circuit Complexity	Medium	High	High	Low	High	Medium	Medium	Medium	Medium	High
Requirement	No Specific	Native NMOS	Native NMOS	Negative-Vth NMOS & custom on-chip transformer design	Native MOSFET	No Specific	No Specific	Native MOSFET	No Specific	No Specific

Comments	Simple yet elegant design with the only disadvantage that the MEMS switch cannot be controlled and thus with unnecessary vibrations may hinder the overall efficiency of the sensor.	3-Stage step-up converter with last stage as ZCS boost converter working in DCM.	Complete proven solution as an implantable sensor with in-vivo testing. The chip operating in DCM with ZCS boost converter configuration, uses along with the start-up elements, an Low Voltage Drop Active Diode as a part of the boost converter in conjunction with a Thyristor Based Oscillator that regulates the Gate Control Block of the Switching Transistor.	This approach proves that lower start-up voltages can still be achieved with lesser area and complexity. Other than that, no circuit level innovations reported here.	Lowest start-up Voltage w/o magnetic components. CS Inverter.high input impedance of boost oscillator. Hysteretic voltage monitor (Pcons.=15nW) used to connect load capacitor to boosted voltage once required value is reached. Schottky diode rectifier preferred over diode-connected MOSFETS. Bulky Implementation.		Cross-coupled Voltage Detector implementation (with positive feedback reducing the switching time) allows for a full-swing output that reduces power consumption. Regulated output (somewhat) results for every input voltage which remains almost constant without dropping much with increasing load due to the voltage controlled oscillator functioning of the pulse generator circuit.	Off-chip components - Microcontroller unit, schottky diode. Use of 4 different types of MOS i.e., 1.2V native (LVZT), 1.2V standard low threshold (LVLT), 3.3V native (HVZT), 3.3V standard low threshold (HVLT) along with 4 different types of 1:1 Transformers (A,B,C,D) were undertaken in a modified armstrong oscillator configuration with MCU controlled duty cycling, to achieve the said claims of the paper.	Works on multi-stage regulation through time-multiplexing an inductor to generate 120X conversion ratio. Moreover, the system uses bias gating to cut current consumption while components experience idling during the sensor operation. ZCS in DCM is used in conjunction with PFM to achieve high efficiency. PFM helps to generate different (2) phases for the circuit as well as control the Duty cycle of the boost converter.	The chip operates under three different modes with both of the harvestore and with any one. Bias gating is used. Alternate selection of harvestors is made in a TDM fashion to charge the same cap(s). MPPT is implemented by controlling the ON-time and switching frequency. Control circuit uses digital functionality to lower power consumption working at lower Vsup. State machine dictates the behaviour of the control circuit (controlling the delay elements). I/p caps. are used to store the energy when harvester not in use. Delay elements implemented as loaded current starved buffers. ZCS is used to generate PMOS switch-ON time and ZVS is used to generate dead time.
* => Not End to End										
**=> Dedicated to any Harvesting System										