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19.6 A 0.2V Trifilar-Coil DCO with DC-DC Converter in 16nm FinFET CMOS with 188dB FOM, 1.3kHz Resolution, and Frequency Pushing of 38MHz/V for Energy Harvesting Applications

Chao-Chieh Li[1], Min-Shueh Yuan[1], Chih-Hsien Chang[1], Yu-Tso Lin[1], Chia-Chun Liao[1], Kenny Hsieh[1], Mark Chen[1], Robert Bogdan Staszewski[2,3]

[1]TSMC, Hsinchu, Taiwan, [2]Delft University of Technology, Delft, The Netherlands, [3]University College Dublin, Dublin, Ireland

Energy harvesting (EH) is a topic of intensive research promising battery-free operation of massive networks of wireless IoT devices. To simultaneously satisfy the EH and IoT, ultra-low-power (ULP) consumption with ultra-low-voltage (ULV) supply are required. Some, e.g., photovoltaic, EH output voltage (<0.3V) is below the threshold voltage (V_t) of even the most recent FinFET CMOS transistors, which makes it extremely challenging for circuit designers. Thus, new special circuit techniques are needed to make the IoT devices work properly with supplies below V_t.

A transformer-feedback oscillator [1] is a promising topology for ULV operation due to its passive RF voltage gain. However, the gates and drains of the cross-coupled transistors in [1] share the same DC voltage. This causes the resonance frequency, mainly due to its voltage-dependent gate capacitance, Cg, to strongly track (i.e. be pushed by) the supply voltage, V_{DD}. For EH, the supply pushing must be very low due to the temporal variability of harvested voltage. A Class-F oscillator [2] also provides a passive voltage gain; however, the gates there are separated from the drains via the transformer, thus resulting in a very-low frequency pushing. Unfortunately, its V_{DD} still cannot go below V_t. Further, the gate voltage (unlike the drain) lacks the beneficial 3rd-harmonic tone for ISF reduction, thus preventing full benefits of the reduced phase noise up-conversion through lower impulse-sensitivity function (ISF).

In this paper, a trifilar-coil oscillator topology providing large passive voltage gain is proposed to enable the sub-V_t operation. The gate-source V_{GS} reshaping technique with a 3rd-harmonic injection can further improve the phase noise (PN). Due to the gate/drain DC isolation, as well as smaller voltage-dependent capacitance in an advanced FinFET technology, this work achieves very low frequency pushing. The bias and control voltages of nearly zero DC power are generated with a tiny switched-capacitor-based DC-DC converter.

An attempt of merely shrinking V_{DD} in conventional LC-tank oscillators inevitably degrades its signal swing leading to severe PN and FOM performance issues. Figure 19.6.1 shows the conventional Class-F oscillator [2] providing a nearly 2× passive voltage gain due to the 1:2 turns-ratio transformer from the drains (D) to gates (G) of the MOS transistors. In the proposed trifilar oscillator, the passive voltage gain is enhanced by another winding in the source of the 'cross-coupled' transistors. The tertiary winding is coupled through a weak magnetic coupling Km_{DS} from the original primary winding. Consequently, the NMOS source signal (VS) oscillates around the ground DC level and produces an opposite voltage swing to that at the gate (VG), thus enhancing V_{GS} = VG-VS by about 100mV. Furthermore, the switched-capacitor at the source side can reach a very fine resolution of 1.3kHz due to the source degeneration, which could help to eliminate the power-hungry delta-sigma modulator in an all-digital PLL. The coarse bank with 23MHz/b is split into the transformer primary and secondary to achieve the maximum quality-factor (Q) enhancement [2].

In the half-circuit model of Fig.19.6.2, there are three windings of inductances L_D, L_G and L_S inserted at the drain, gate and source sides, respectively. Two magnetic-coupling mechanisms exists with coefficients Km_{DG} and Km_{DS}. In the former, the turns ratio between L_D and L_G is N_{DG}=1:2 with a strong Km_{DG} of 0.75. In the latter, the inductance ratio between L_D and L_S is N_{DS}=1:0.73 with a weak Km_{DS} of 0.32. The small-signal model shows the voltage loop gain could be derived approximately by the formula for V_{OUT}/V_{GS} shown at the middle of Fig. 19.6.2. The voltage loop gain is enhanced by the term: ($km_{DG}N_{DG}+km_{DS}N_{DS}$). In the same start-up condition, the required device Gm could be reduced 55% at sub-V_t bias while the passive voltage gain is already boosted up by 220%. Thus, the supply voltage could be brought down to 0.2V or lower while still ensuring the reliable oscillation start-up. The effective Q of the trifilar transformer could be calculated by $Q_{Trifialr}=Im(Z_{Total})/Re(Z_{Total})$. The total $Q_{Trifilar}$ is a combination of Q-factors of the three coils. Two thick metals and one ultra-thick metal are combined to achieve the lowest possible series resistance for the maximum Q-factor and minimum voltage drop in the supply path. The highest $Q_{Trifilar}$ exceeds 11 within 3 to 4GHz of the DCO tuning range (TR).

To reduce the ISF at the NMOS gates, and thus to further improve PN, the normally sinusoidal VG voltage waveform of the Class-F oscillator is turned sharper with higher amplitude. Figure 19.6.2 shows the idea of the third-harmonic resonator placed at the source of M1,2. VS, containing both ω_0 and $3\omega_0$ components, gets coupled to VG, which contains only the fundamental at ω_0. The fundamental *A* and *C* components reinforce, whereas $3\omega_0$ makes the waveform sharper. Consequently, the effective V_{GS} now has a higher amplitude and sharper rising/falling edges than in the conventional topology, thus shows more immunity to noise.

If the only available supply is somewhat below V_t, then the subthreshold control voltage of the switched capacitor could result in a narrow tuning range. Furthermore, this topology separates the drains and gates to enhance Gm at a low V_{DD}. A VB higher than V_{DD} is needed in the sub-V_t operation. Consequently, a tiny DC-to-DC converter coupled to the harvested voltage is proposed to provide the nearly static control, Vctrl, and bias VB voltages for the trifilar DCO, as shown in Fig. 19.6.3. A multiphase single-ended ring oscillator (RO) generates non-overlapping clocks CLK/CLKB for the switcher inverters. The number of series-connected MOSFETs do not exceed 2, and the voltage booster could operate at a V_{DD} lower than 0.2V. Vin = V_{DD} provides the input to the voltage booster and directly controls the drain side of oscillator switching transistors. Five stages of voltage booster, driven by the non-overlapped clock generator from RO, provide a sufficiently high voltage to turn on the switched capacitors. Thus, the tuning range of this circuit can be brought back to 'normal' (i.e. >20%). VB then uses the selected voltage-booster output. A low-pass filter of 600Hz corner is adopted to eliminate the ripple from the voltage booster and to prevent the DCO PN degradation, especially in IoT packetized operations.

The proposed trifilar DCO with the DC-DC converter is implemented in 16nm FinFET CMOS. Figure 19.6.4 shows on-wafer phase-noise measurements. In the V_{DD}=0.4V mode, the phase noise reaches -120 to -123dBc/Hz and -143 to -145dBc/Hz at 1MHz and 10MHz offsets, respectively. The FOM is 188 to 190dBc/Hz with a power consumption of 3.8mW. In the V_{DD}=0.2V mode, the phase noise worsens to -111 to ~-113dBc/Hz and -132 to ~-135dBc/Hz at 1MHz and 10MHz offsets, respectively, but the power consumption reduces to 0.6mW, giving FOM of 186 to 188dB. The flicker noise corner is 40kHz and 120kHz at 0.2V and 0.4V, respectively. The frequency pushing of the DCO supply shows a small value of 3.6 to 27MHz/V at 0.4V and 12.6 to 38.2MHz/V at 0.2V. The coarse step size is 23MHz/b and the fine step is 1.3kHz/b. The DC-to-DC converter can operate as low as V_{DD}=0.15V and consume only 0.2μW for the 0.2V input while the ring oscillator operates at tens of MHz. The proposed approach allows the DCO to ultimately operate at as low as 0.17V of the harvested voltage. Figure 19.6.6 shows the comparison table of state-of-the-art low-voltage LC-tank oscillators. Our V_{DD} is the lowest in the figure while delivering state-of-the-art performance. The area 0.11mm^2 is among the lowest in Fig. 19.6.6. Among results in Fig. 19.6.6, the frequency pushing and flicker noise corner frequency are both the lowest, mainly due to the trifilar topology and FinFET devices.

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The authors would like to thank Hung-Yi Kuo, Chester Kuo and Herman Chiang for all lab measurements.

References:
[1] K. Kwok, et al., "Ultra-Low-Voltage High-Performance CMOS VCOs Using Transformer Feedback," *IEEE JSSC*, vol. 40, no. 3, pp. 652-660, Mar. 2005.
[2] M. Babaie, et al., "A Class F oscillators", *ISSCC*, pp. 348-349, Feb. 2013.
[3] L. Fanori, et al., "A 2.5-to-3.3GHz CMOS Class-D VCO" *ISSCC*, pp. 346-347, Feb. 2013.
[4] M. Shahmohammadi, et al., "A 1/f Noise Upconversion Reduction Technique Applied to Class-D and Class-F Oscillators" *ISSCC*, pp. 444-445, Feb. 2015.
[5] D. Murphy, et al., "A Complementary VCO for IoE that Achieves a 195dBc/Hz FOM and Flicker Noise Corner of 200kHz" *ISSCC*, pp. 44-45, Feb. 2016.
[6] D. Murphy, et al., "A VCO with Implicit Common-Mode Resonance," *ISSCC*, pp. 442-443, Feb. 2015.

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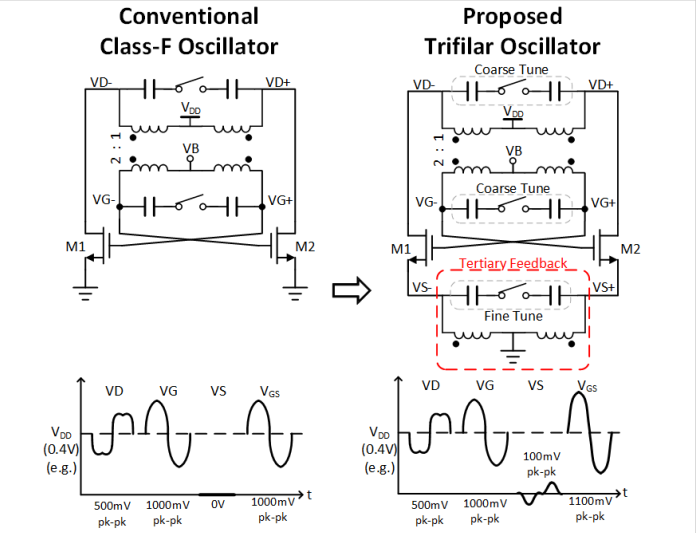

Figure 19.6.1: Class-F DCO and proposed trifilar-coil DCO with tertiary feedback.

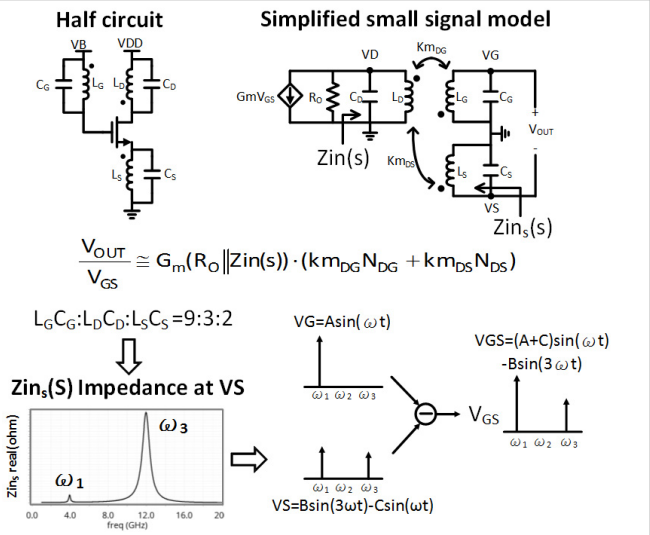

Figure 19.6.2: Half-circuit model and gate-source-voltage (V_{GS}) reshaping technique with 3rd-harmonic injection.

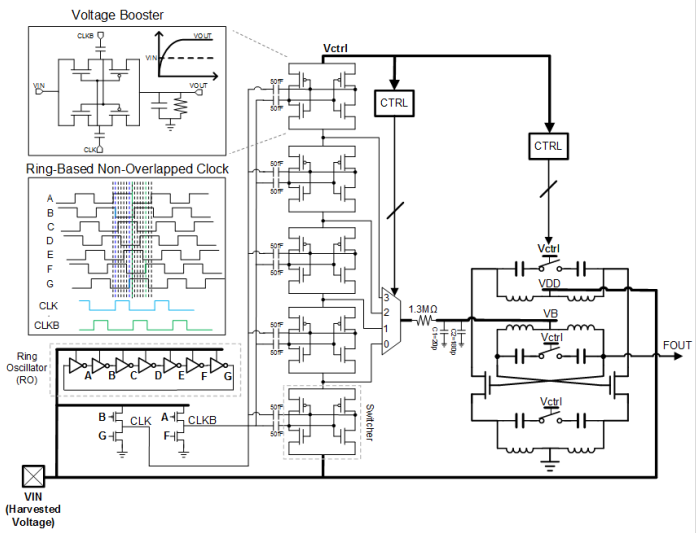

Figure 19.6.3: Trifilar DCO powered by harvested voltage VIN with DC-DC converter only for VB biasing and switched-capacitor controls.

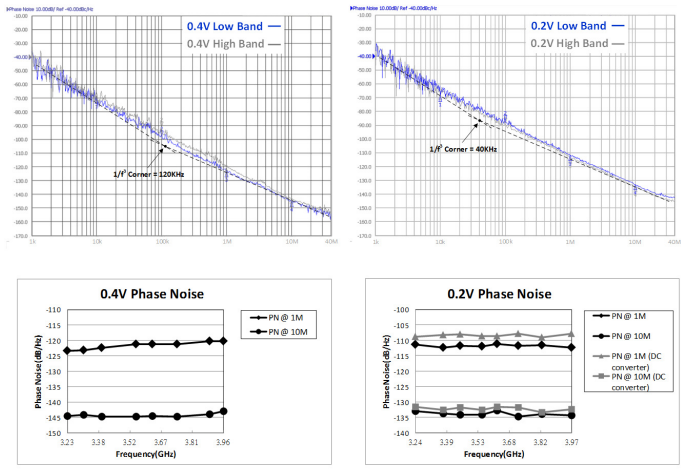

Figure 19.6.4: Measured phase noise at V_{DD} of 0.2V and 0.4V across the tuning range.

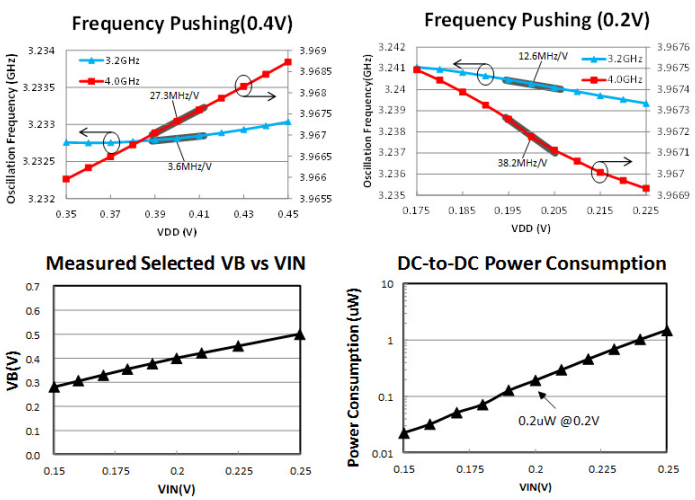

Figure 19.6.5: Measured frequency pushing of DCO at V_{DD} of 0.2V and 0.4V and measured DC-to-DC converter performance.

	This work		[3] ISSCC'13	[4] ISSCC'15	[5] ISSCC'16	[6] ISSCC'15
	Low power	High perform				
Technology	16nm FinFET		65nm	40nm	28nm	28nm
VDD[V]	**0.2**	**0.4**	0.4	0.5	0.7	0.9
Tuning Range[GHz]	3.2-4.0 (22%)		2.5-3.3 (27%)	3.3-4.5 (31%)	4.7-5.4 (14%)	2.9-3.8 (27%)
Phase Noise [dBc/Hz] @ 10MHz	-134	-145	-147	-143	-138	-150
Power [mW]	0.6	3.8	6.8	4.1	0.5	6.8
FOM	**188**	**190**	189	188	195	192
Frequency Pushing(MHz/V)	12.6 - 38.2	3.6-27.3	180	46-60	NA	NA
1/f³Corner(KHz)	40	120	2000	60	200	200
Core Area [mm²]	0.11		0.15	0.1	0.18	0.19

$$^{*}\text{FOM} = -\text{PN} + 20\log_{10}\left(\frac{f_{osc}}{\Delta f_{offset}}\right) - 10\log_{10}\left(\frac{P_{DC}}{1\text{mW}}\right)$$

Figure 19.6.6: Performance summary and comparison with state-of-the-art oscillators.

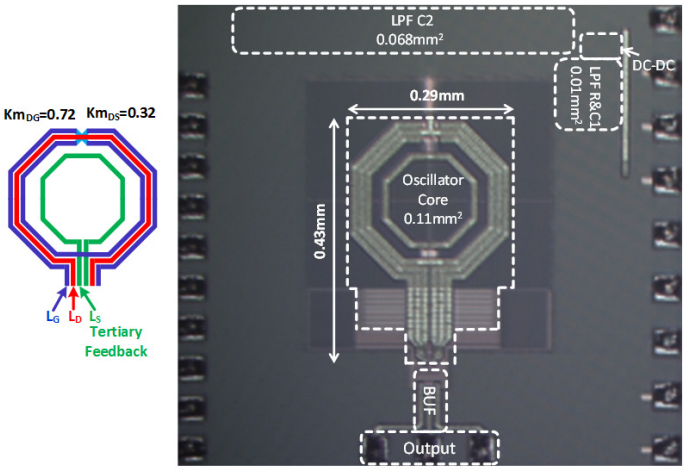

Figure 19.6.7: Die micrograph of the trifilar DCO and a tiny DC-DC converter. The core size is 0.11mm².

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