A 3-Mode Wide Operational Range Reconfigurable Regulating Rectifier for Wireless Power Transfer

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A 3-Mode Wide Operational Range Reconfigurable Regulating Rectifier for Wireless Power Transfer

Master's Thesis

To fulfill the requirements for the degree of
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Contents

List of Figures

List of Tables

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Abstract

This article presents a novel wide operational range reconfigurable regulating rectifier for wireless power transfer. The proposed 1X/2X/3X rectifier achieves wide range voltage regulation without global loop control to minimize the area occupation. Compared with previous work, more working modes and greater magnification allow the proposed rectifier to regulate smaller signal, which extends voltage regulation range. A novel local loop control system is proposed for voltage rectification with three modes. The local loop adaptively senses the duty cycle of mode signal to determine which two working modes the rectifier should work with and configure the rectifier in these two modes. Then the rectifier are switching between two working modes according to the comparison result with reference voltage. Also, the change of which two working modes are also triggered by a window comparator to make sure the change happens when the output voltage is far away from reference voltage. The system is designed and simulated in a 0.18-μm BCD technology. The measurement results show that the proposed system can rectify wide-range input AC power to a regulated output. The achieved voltage conversion ratio (VCR) is 0.95$\sim$2.68 with a peak power conversion efficiency (PCE) of 87.4%.

1 Introduction

In recent years, more and more smart devices are entering people's daily life. Due to the fact that they need to operate continuously, a more convenient way to charge these devices is urgently needed to replace conventional wired charging. Wireless power transfer (WPT) is experiencing rapid growth, it has been widely used to charge smartphones, electric cars, smart watches, biomedical implants, and other wearable electronic devices, especially for implantable medical devices (IMDs)[1]. Many implantable medical devices can be charged by WPT techniques, such as deep brain neurostimulators, cochlear implants and so on. WPT techniques can reduce the size of power units of implanted devices by eliminating bulky batteries[2]. Limited battery capacity also requires regular replacement by operations, adding extra risks to the patients.

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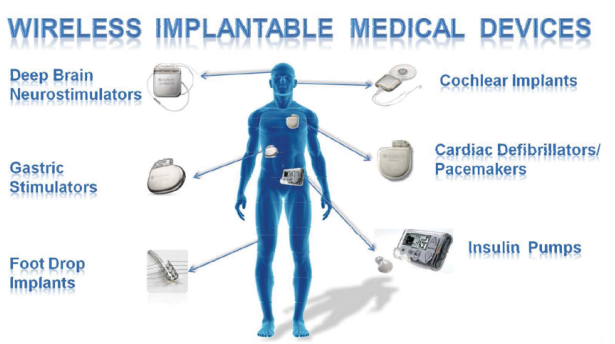

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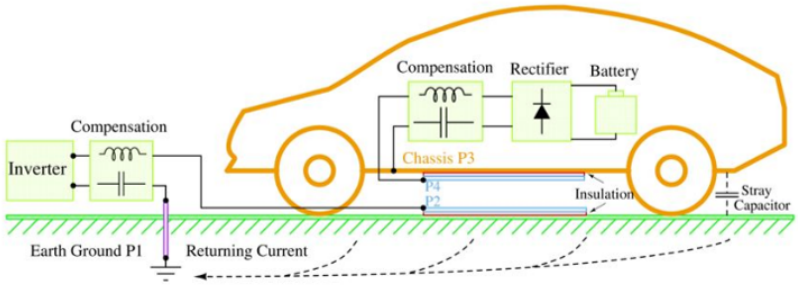


(c)

Figure 1.1: (a) Smartphone charging station. (b) Biomedical implants. (c) Electric vehicles

1.1 WPT System

Depending on the distance, the WPT system can be divided into near-field WPT and far-field WPT, as shown in Figure 1.2. The near-field WPT can be divided into short-range system and

mid-range system. The smartphone chargin and wireless implantable medical devices canbe defined as near-field system. The electric vehicles, since the distance between the coils can be tens of centimeters. it is defined as far-field system. Today we mainly focus on near-field system, since our design is mainly used for implantable biomedical devices. For the near-field WPT system, there are two coupling ways to transfer the energy, which is inductive coupling and capacitive coupling[3], their structures are shown in Figure 1.3. Inductive coupling happens when current flow creates a changing magnetic field, it doesn't have transmitted power limit and it is difficult to stop a magnetic field. Capacitive coupling happens when voltage establishes an electric field[4]. It can only be used in very low power application and will be stopped by conductive material. Our WPT system is designed to charge the biomedical implants inside the human body, there are bones and blood vessels to hinder energy transfer. Capacitive coupling may not transfer enough energy to the implants. Thus, resonant inductive coupling is a suitable option for our design, since resonance can reduce the dissipated energy between coils and improve efficiency[5]. When the coil system is resonant system, we will have

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{1.1}$$

f is the resonant frequency, L is the inductance of the coil, C is the compensation capacitance.

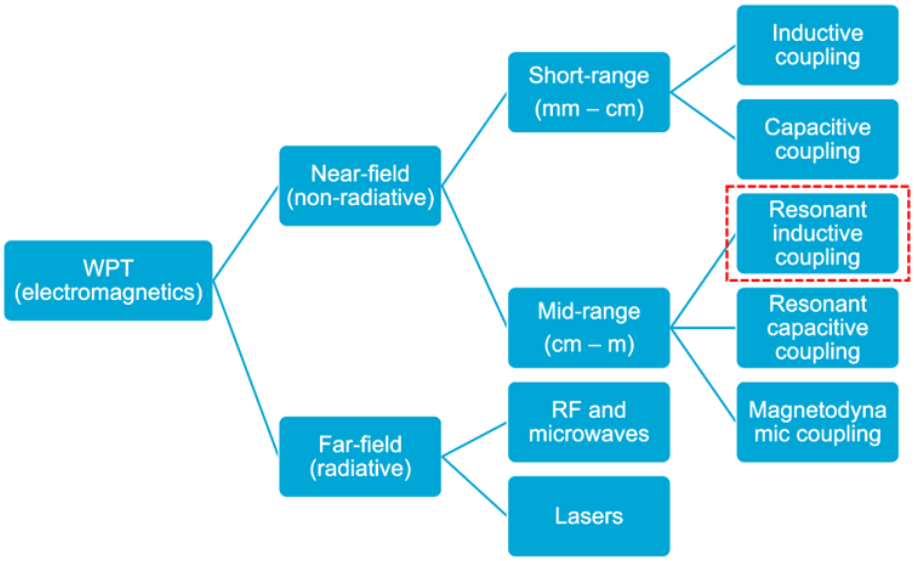


Figure 1.2: WPT System Categories

A WPT system consists of power transmitter (TX) and power receiver (RX) as shown in Figure 1.4. On the TX side, the primary coil driven by power amplifier (PA) can generate magnetic

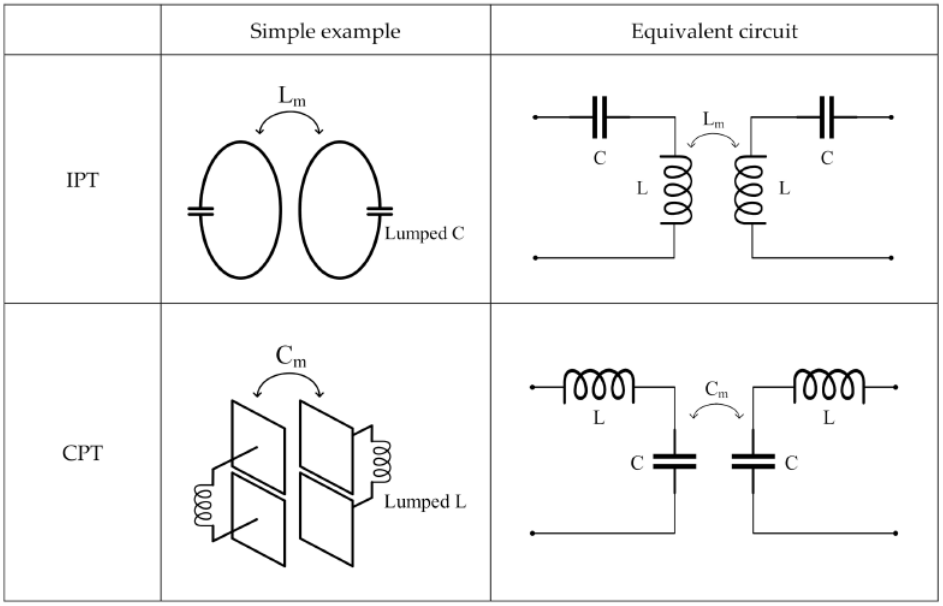


Figure 1.3: Inductive power transfer(IPT) and Capacitive power transfer(CPT)

fields and couple AC power to the secondary coil. The power RX rectifies the received AC power followed by a low dropout regulator (LDO) to provide a stable DC voltage for the load. For different design, they might add some blocks between rectifier and load, which is shown in Figure 1.5. For example, we can add low-dropout regulator to offer a stable output, a DC-DC converter to get higher or lower output. Also, we can use one-stage system to improve system efficiency. High system efficiency is important for biomedical implants charging. it can reduce the dissipated energy inside the human body. Therefore, our design is a one-stage system, and we will focus on reconfigurable regulation rectification, the reason will be explained later.

For a WPT system, the commonly used frequencies are 6.78MHz, 13.56MHz, and 40.68MHz[6]. It is inevitable that part of energy come from the coil will be absorbed by human tissue[7]. The specific absorption rate(SAR) is frequency independent. Higher frequency can cause larger SAR. In this work, 6.78MHz is used to reduce the SAR as much as possible.

In actual applications, the coupling coefficient may vary with the unpredictable direction and distance, which means the received AC power amplitude varies time by time. System efficiency and voltage gain can be insufficient due to poor coupling with the primary coils. Thus, to make the IMDs operate in varying conditions, the output voltage of the rectifier should keep stable while the input AC power varies in a large range, which is decided by system voltage gain. The system voltage gain A_{sys} is the result of the power-link voltage gain A_{link} multiplied by the

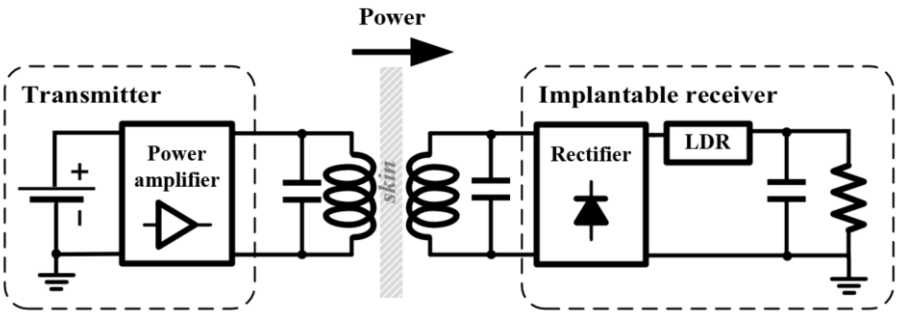


Figure 1.4: A WPT system for IMDs

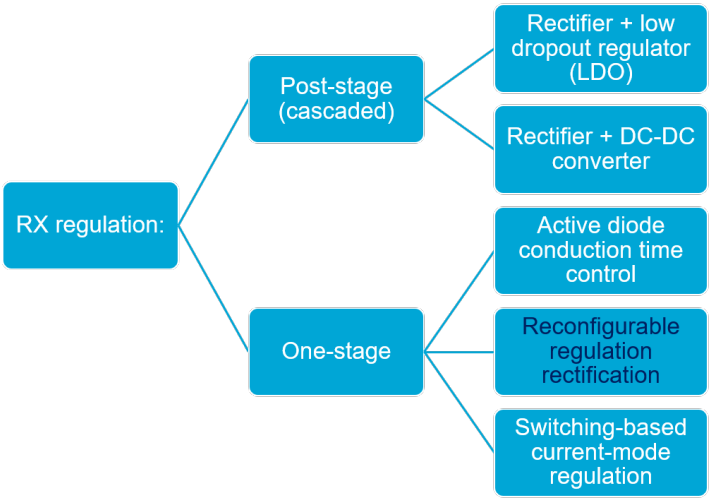


Figure 1.5: RX regulation

voltage conversion ratio (VCR) of the rectifier M ($A_{sys} = A_{link} \times M$). Power-link gain A_{link} is the ratio of the voltage collected by secondary coil to the input voltage supplied by primary coil. The rectifier's voltage conversion ratio (VCR) is the ratio of DC output voltage to the peak value of AC voltage. Closer distance between primary coil and secondary coil will achieve better power-link voltage gain, which leads to higher output voltage. so the VCR should adaptively change to gain a stable output voltage. The reconfigurable rectifier can achieve multiple VCRs by switching between different working modes. That is why we choose to focus on this kind of design.

High system power efficiency can help to reduce the absorbed energy by human tissue, the system power efficiency η_{sys} is determined by the power-link efficiency η_{link} and the rectifier power-conversion efficiency η_{rec} ($\eta_{sys} = \eta_{link} \times \eta_{rec}$). Power-link efficiency η_{link} is the ratio of power collected by secondary coil to the input power supplied by primary coil, depending on the size of coil, quality factor and coupling factor between two coils. The rectifier power-conversion efficiency η_{rec} is the ratio of output DC power to received AC power of secondary coil. Both power-link efficiency and rectifier power-conversion efficiency need to be as high as possible to realize satisfied system power efficiency.

1.2 Literature review

In previous work, post-stage and one-stage WPT systems have been implemented, which provide a regulated output voltage.

In [8], a 13.56 MHz CMOS near field inductive-link power supply for implantable medical devices (IMDs) is proposed. Its maximum delivered current is 20mA. The receiver utilize active voltage doubler rectifier (VD) and low-dropout regulators (LDOs) to provide a stable DC output, the general structure is shown in Figure 1.6. The received AC signal are rectified to DC output with ripple voltage. The voltage doubler rectifier consists of two symmetrical comparator with delay compensation control, NMOS and PMOS switches and fly capacitors C_{R1} and C_{R2}. The structure is shown in Figure 1.7. The voltage limiter can limit the rectified voltage V_{REC} at nominated voltage 2V even though the input power is too large. Bulk regulation techniques are applied in the circuit to adaptively connect the bulk to higher or lower voltage. The comparator-controlled NMOS and PMOS switch will replace the diode and periodly charge two fly capacitors, which works as a voltage doubler. Start-up control system are also applied in this design, since it is a self-powered system. Then the output V_{REC} are pass to LDOs. We can

see that the LDOs can significantly decrease the ripple voltage from the rectifier. It can achieve 10mV ripple voltage of active rectifier and 85% peak conversion efficiency. The measured dropout voltage is 384mV.

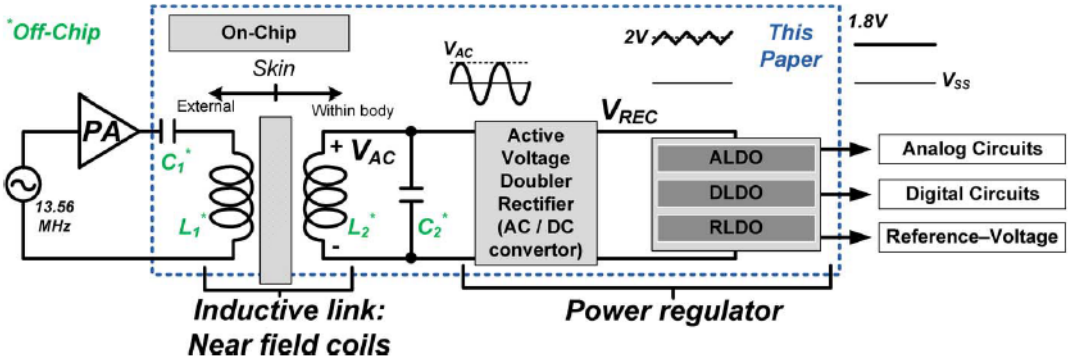


Figure 1.6: Rectifier+LDOs

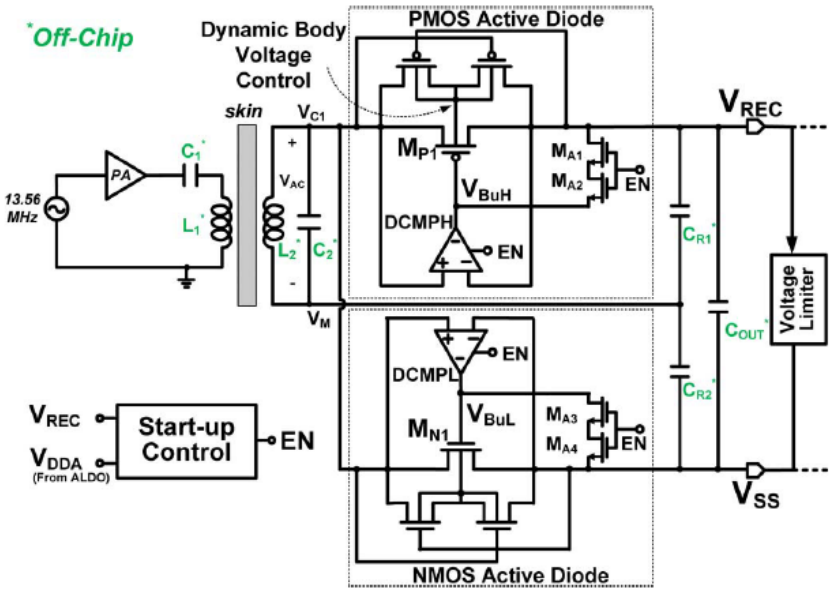


Figure 1.7: Voltage doubler rectifier

In [9], a fully integrated 6W resonant-type 6.78MHz wireless power receiver is described, the general structure is shown in Figure 1.8(a). The rectifier generated DC voltage V_{rect} pass to buck converter to be regulated at 5V for battery charging. Linear regulator LDO1 are used for generating internal power supply. The our-band communication unit power is supplied by LDO2 and LDO3. Since a 6.78Mhz or 13.56Mhz WPT system is sensitive to any time mismatch, which may degrade the rectifier efficiency. The rectifier design is mainly focus on PVT robustness,

which is shown in Figure 1.8(b). The optimized schottky diode is implemented for this design. Linear regulator can guarantee the voltage V_{L1} and V_{L2} at $V_{L5R} - V_{th1}$ and $V_{L5R} - V_{th2}$. Hence, the parasitic resistance along the current path can be significantly reduced, which can reduce the switching loss and conduction loss, the rectifier can finally achieve 92.8% efficiency. The buck converter is applied in this design to step down the rectified voltage V_{RECT} to 5V to charge the battery. An inductor is applied in this design. 91% efficiency are achieved over light load for this buck converter. The die area is $14.44mm^2$ and the design shows up to 84.6% system efficiency.

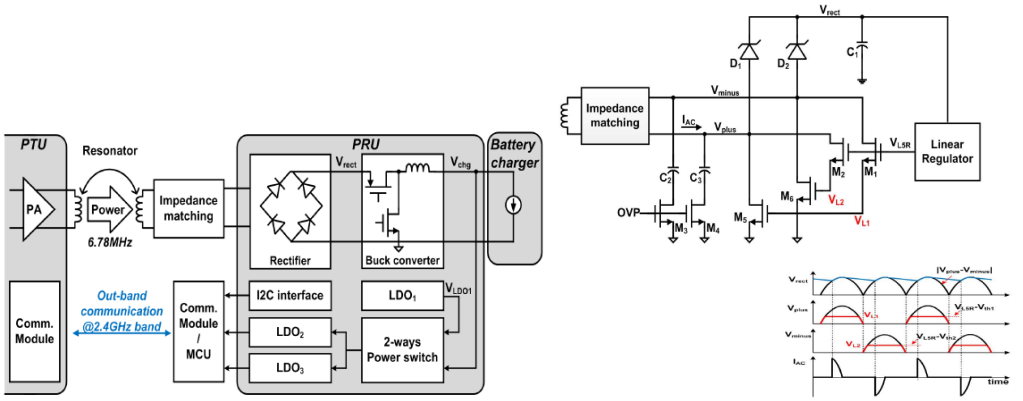


Figure 1.8: (a) Rectifier+Buck converter (b) Schematic of AC-DC rectifier.

Previous two design are both post-stage design, they add LDOs or DC-DC converter after the rectifier to stablize output or get a higher or lower output. We can notice that for these two post-stage designs, although their rectifier efficiencies are high enough. They still can not achieve high system efficiency due to multiple stage. But the efficiency is important for the WPT system for biomedical implants. Also, the area occupation of post-stage design are larger, the inductor may be applied. Thus, one-stage systems are preferred, which are more proper ways for biomedical implants.

In [10], a 6.78MHz resonant regulating rectifier (3R) is proposed for voltage regulation, which consists of a bridge rectifier and a charge pump. This 3R system includes three switches M_1, M_2, M_3, along with the output capacitor C_{OUT} and flying capacitor C_{FL}. Their switching can control the up and down of V_{XH}. During on-duty cycle, both capacitors are parallelly charged to V_{XH}, I_{RT} is increasing. During off-duty, two capacitors become series-connected, I_{RT} decreases. The level of V_{OUT} is related with PWM duty ratio. Limiting capacitor C_{LM} are added to control

the amplitude of input current I_{RS}, which can help to reduce the conduction loss proportional to I_{RS}^2. The voltage stress on M_1 can also be managed by adjusting the value of C_{LM}. Also, for realizing zero current switching to improve efficiency. Inverter sync and comparator sync are merged into one pulse and become the *CLK* signal of D-flipflop. This rectifier finally achieve 86% peak efficiency and 6W Max power. However, the transmitted energy is controlled manually, five off-chip diodes and three off-chip capacitors are used in the circuit, which significantly increase the voltage drop.

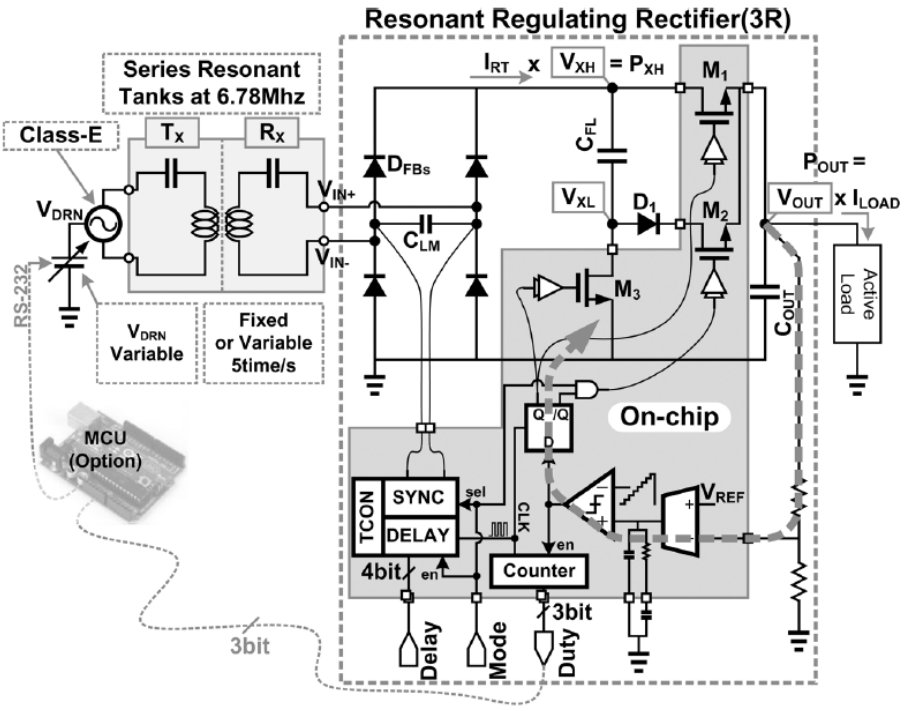


Figure 1.9: 3R Rectifier

In [11], the 13.56Mhz reconfigurable resonant regulating rectifier (R^3) with 1X/2X mode is an alternating way to offer stable output without LDO or DC-DC converter. This system consists of two NMOS switches and cross-coupled PMOS switches. The active switches are controlled by comparator $CMP1 \sim 3$. There are two working modes for this system, which is 1X mode and 2X mode. The rectifier can be configured to work as full bridge rectifier or voltage doubler according to *Mode* signal. The output voltage will first be compared with reference signal $VREF$, the output of error amplifier will then be compared with the ramp signal to get *Mode* signal. The result is synchronized with clock signal by D-flipflop. The rectifier can keep a stable output voltage by switching between 1X mode and 2X mode. The duty ratio can adjust

the output voltage level. The backscattering technique is applied in this design, *Mode* signal is coded with Manchester code and send back to primary coil, when the *Mode* signal changes, the input impedance will also changes. The load shift result can be used for backscattering. The data receiver will decode the message and adjust the pulse controller inside the Class-D amplifier, which will adjust the transmitted power. The output voltage can be regulated at 3.6V, with the help of global power control, the peak receiver efficiency is 92.6%. The maximum output power is 102mW. However, it requires a data communication unit to send information back to the TX side and utilizes FPGA to code and decode the message. The minimization of the system is limited by large data communication units. Also, for some loading and coupling conditions, the power voltage gain of 2x can be lower than the power voltage gain of 1x. But that paper doesn't address these issues.

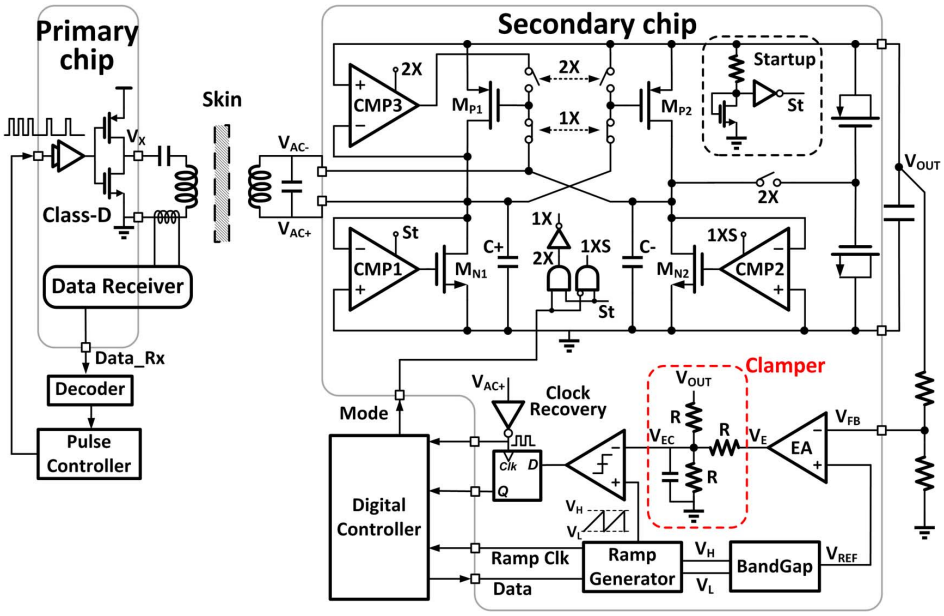
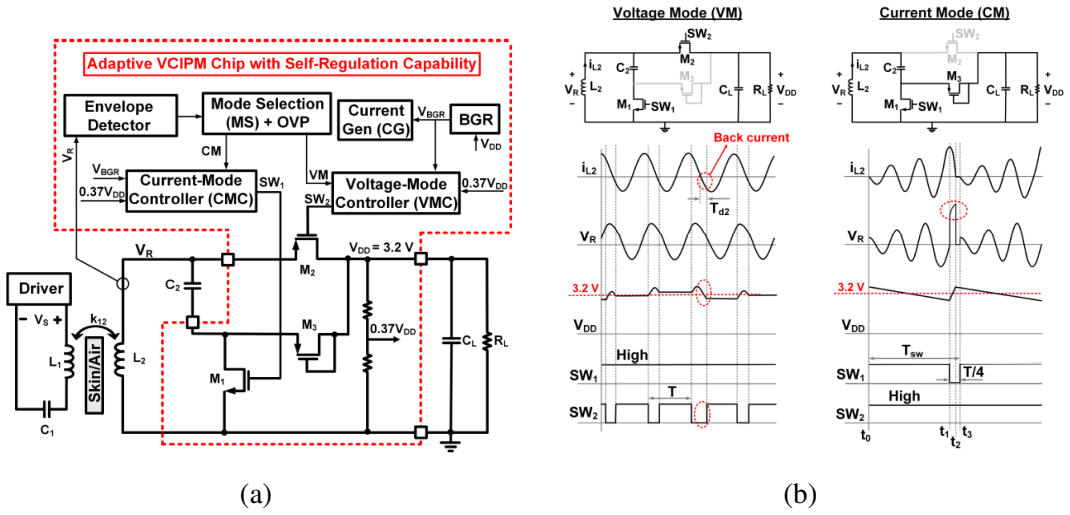


Figure 1.10: R^3 reconfigurable rectifier

In [12], an adaptive reconfigurable rectifier with voltage/current mode to achieve higher voltage conversion ratio. The proposed VCIPM system utilize two off-chip capacitors and adaptively find optimal working mode to work in wider range of coil arrangements, the structure is shown in Figure 1.11(a). When the received input is larger than required voltage, the rectifier will work in voltage mode to get higher power conversion efficiency. When the received input is smaller than the required voltage, the rectifier will then switch to current mode to gain higher voltage conversion efficiency. The proposed system can adaptively sense V_R and get an optimal working mode to generate a regulated V_{DD}. The received signal from the secondary coil will

first be sensed by envelope detector, the mode selection unit will decide the working mode of rectifier. The voltage mode controller and current mode controller is used to get optimal control pulse for SW_1 and SW_2. The waveform when rectifier works in voltage mode and current mode are shown in Figure 1.11(b). In voltage mode, SW_1 remains high to keep parallel resonant, SW_2 controls back current to regulate V_{DD} by remaining on for a little bit longer time. In current mode, SW_2 remains high, which means M_2 turns off. When SW_1 turns on, C_2 is charged until i_{L2} reaches its maximum, V_{DD} slowly decrease since the load is powered by load capacitor C_L. Then, SW_1 periodically turns off to form series resonant structure. The input will then work as current source and charge C_L, V_{DD} will then increase to keep a stable output. V_R will be higher than V_{DD} to turn M_3 on, leading to high voltage conversion efficiency. The maximum voltage conversion efficiency and power conversion efficiency is 3.55 and 77%. The operational range and orientation of the inductive link could be extended from 6cm to 13.5cm (125%) and 30° to 75° (150%), respectively.

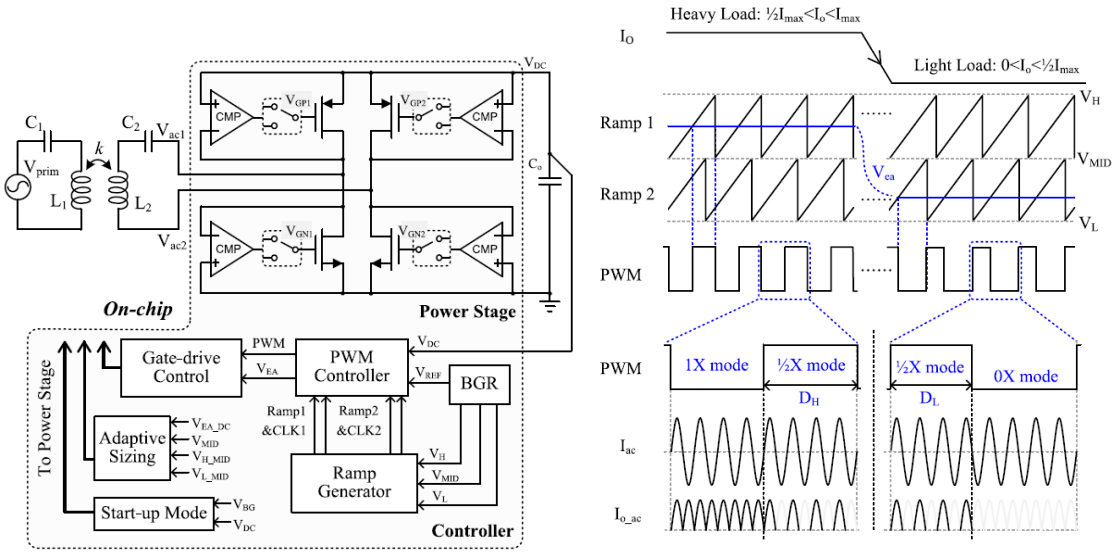


(a) (b)

Figure 1.11: (a) Block diagram of VCIPM (b) Key waveform of VCIPM chip.

In [13], a 6.78Mhz three-mode (R^3) rectifier utilizes 0X/½X/1X mode operation to achieve voltage rectification, series resonant is applied in this design. The system consists of four comparators, two NMOS switches and two PMOS switches. There are switches between the gate of MOS transistors and comparators to configure the rectifier to three working modes. The structure is shown in Figure 1.12(a). If the amplitude of AC current could be I_{ac}, then the output current of 1X mode, ½X mode, and 0X mode will be I_{max}, ½I_{max} and 0. The rectifier will switch between 1X and ½X in heavy load and between 0X and ½X in light load. Depending on the PWN duty ratio, the output current can be any value between 0 and I_{max}. It improves the system

efficiency and reduce ripple voltage by adding extra working mode between 0X and 1X mode in one cycle. The operational waveform is shown in Figure 1.12(b). The PWM controller senses the output voltage V_{DC} and compare with reference voltage. The ramp generator generate two ramp signal Ramp1 and Ramp2. They have same frequency but different amplitude. When the rectifier works in heavy load, the V_{EA} is in Ramp1, the duty ratio of 1X and ½X is determined by comparison result. When the rectifier works in light load, the V_{EA} is in Ramp2, the duty ratio of 0X and ½X is determined by comparison result. Type-II compensation are applied to offer loop compensation for stability. The adaptive sizing method is also used to reduce the conduction loss, the size of M_{N1} and M_{N2} can be adaptively adjusted depending on the working mode. The mechanism is not affected by coupling and loading conditions. The output voltage is 5V and the system achieve 92.2% peak efficiency. The maximum output power is 6W. The chip area is $4.77mm^2$. But it requires large input amplitude AC power to reach desired voltage level, which leaves a smaller margin for preferable human tissue-specific absorption rate (SAR)[7].



(a) (b)

Figure 1.12: (a) Block diagram of three mode rectifier (b) Key waveform of system.

1.3 Research Requirement

To summarize, this thesis focuses on the following problems:

Q1. A stable output is very important for the biomedical implant devices. The maximum ripple voltage should be lower than 200mV.

Q2. Wide input-range can help the rectifier to work under varying input condition due to weak coupling. The VCR should achieve 1∼2.5. The rectifier can accept smaller input AC amplitude, which also benefits human specification rate(SAR).

Q3. High efficiency is also necessary for biomedical WPT system, higher efficiency means smaller dissipated energy inside human body, less energy loss benefits patients health. The peak operating efficiency should be higher than 85%.

Q4. Small area occupation can also help to achieve a better design for biomedical implants, since the receiver side of WPT system will be implanted inside human body with other function components. A small area occupation of die area can lead to less harm for patient health.

1.4 Thesis Outline

The rest of this article is organized as follows.

In Section II, We introduce the architecture and operation principle of our system. The operational waveform of proposed system and rectifier structure will be discussed. The start up mechanism is also very important since our system is a self-powered system. The delay compensated comparator are also described to reduce the conduction loss.

In Section III, we will introduce the inductive coupling and compare series-resonant and parallel-resonant. The impedance analysis of the reconfigurable rectifier and the system voltage gain and efficiency in different loading conditions will also be presented.

In Section IV, the key component implementation including duty ratio detector, state control unit, window comparator unit, independent current source and frequency divider are discussed.

In Section V. Measurement and simulation results are shown.

Section VI concludes this article and discuss future work.

2 The Proposed WPT Receiver System

2.1 Architecture of Proposed System

The architecture of the proposed wide input-range rectification system is shown in Figure 2.1, which consists of a 3-mode reconfigurable rectifier, one comparator $CMP1$, two duty-ratio detectors, two 2-to-1 multiplexers, state control unit and digital controller. This work applies parallel-resonant connection as RX, since it is better for low-power application[6]. The detail of resonance will be discussed in Section III. For low-power IMD application, the conduction angle is small, so the input can be regarded as an ideal AC voltage source. To minimize the ripple voltage, the rectifier should only switch between two adjacent working modes for each reference signal in the steady state, depending on the comparison result of $CMP1$. Thus, which two modes the rectifier should work with need to be determined. Here we use two duty ratio detectors to determine the working mode. Since we have three working modes 1x, 2x, 3x. When $MODE\_1$ is $'0'$ and $MODE\_0$ is $'0'$, the rectifier will work in 1x mode. When $MODE\_1$ is $'0'$ and $MODE\_0$ is $'1'$, the rectifier will work in 2x mode. When $MODE\_1$ is $'1'$ and $MODE\_0$ is $'1'$, the rectifier will work in 3x mode. Thus, we get two mode-switching periods, which are $1x \sim 2x$ and $2x \sim 3x$. These two mode-switching periods are represented by $State$ signal. As shown in Table 1, when the rectifier is switching between 1x mode and 2x mode, $State$ signal is $'0'$. When the rectifier is switching between 2x mode and 3x mode, $State$ signal is $'1'$.

Table 1: MODE SIGNAL VERSUS STATE AND CMP1

$MODE\_1,0$ \ CMP1 / State	1	0
0	0, 0	0, 1
1	0, 1	1, 1

The mode-switching period that the rectifier works with is determined by the duty ratio of signal $MODE\_1$ and $MODE\_0$. When the duty ratio of signal $MODE\_1$ and $MODE\_0$ reaches 0% or 100%, it means the current mode-switching period cannot reaches required reference voltage, $State$ signal will change to realize larger or smaller amplifying ability. For example, when $State$ signal is $'0'$, the rectifier works with 1x mode and 2x mode, signal $MODE\_0$ is switching

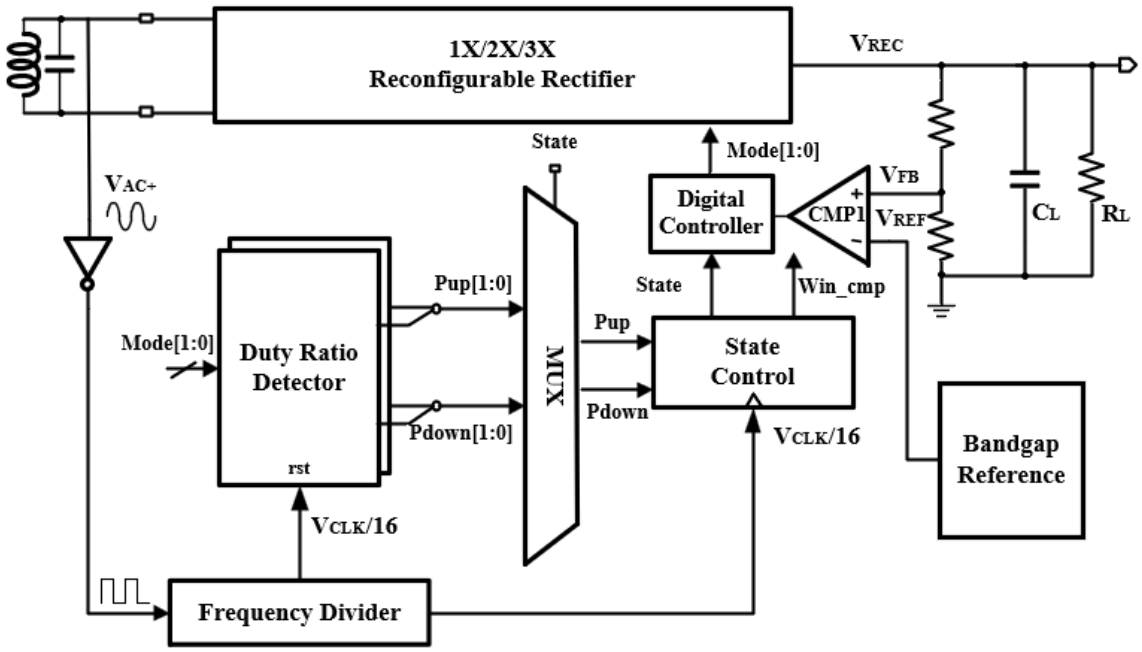


Figure 2.1: Architecture of Proposed System

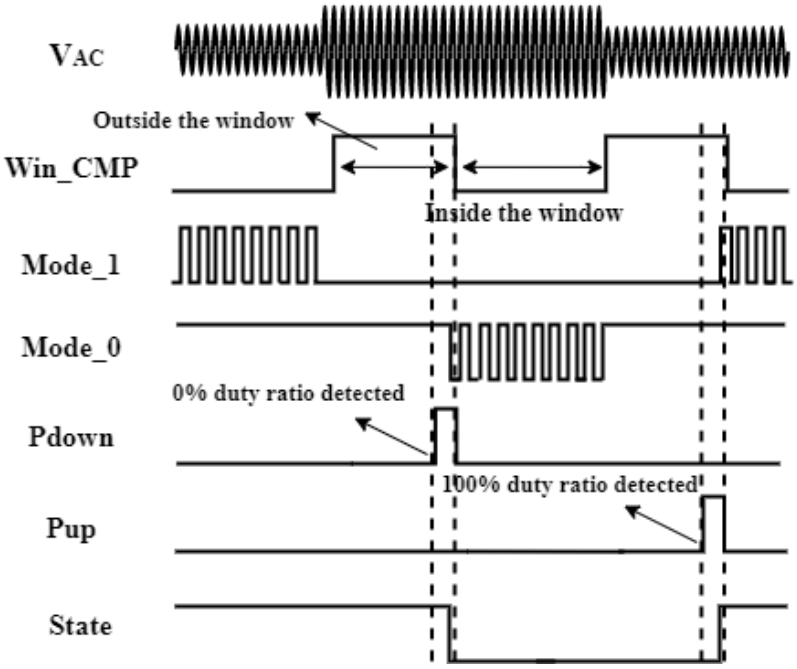


Figure 2.2: Waveform of proposed system

between $'0'$ and $'1'$. If $MODE\_0$ continues to be $'1'$ for more than 16 periods of input AC signal, it means 2x mode cannot make the output of rectifier V_{REC} reach required voltage level. Signal Pup will be high and signal $State$ will switch to $'1'$. The rectifier will then work with 2x mode and 3x mode to get larger output voltage, the waveform of this process is shown in Figure 2.2. During this process, we only need to pay attention to the duty ratio of signal $MODE\_0$, the 2-to-1 multiplexers are used to make sure that only $Pup0$ and $Pdown0$ from $MODE\_0$ duty ratio detector are used for state control unit.

2.2 1x/2x/3x Rectifier Structure

2.2.1 Basic structure

Figure 2.3 shows the basic structure of full-bridge rectifier. Since parallel-resonant is applied in our design, the input can be regarded as AC sinusoidal voltage source. The AC signal will then pass to the rectifier and get an DC output. An output capacitor is added at the output to work as a low-pass filter. Then the ripple at the output can be smaller. The equivalent structure of 1X/2X/3X mode rectifier is shown in Figure 2.4. At the 1X mode, the rectifier is configured as full-bridge rectifier. The DC output level equals to the input amplitude of AC signal. At the 2X mode, during negative half cycle, capacitor C_2 is charged to input amplitude V_{AC}. Then during the positive half cycle, the top plate voltage of C_2 is clamped at input amplitude V_{AC}, C_1 is also charged to V_{AC}. Thus, the output level will be 2 times V_{AC}. For the 3X mode, it is a voltage doubler and a half wave rectifier. At the negative half cycle, capacitor C_2 and C_3 are charged to V_{AC}. Then at the positive half cycle, the top plate voltage of C_2 is clamped at V_{AC}, so the voltage at the bottom plate of C_2 is 2 times V_{AC}, since the voltage across C_3 is also V_{AC}, finally, the DC output level is 3 times V_{AC}.

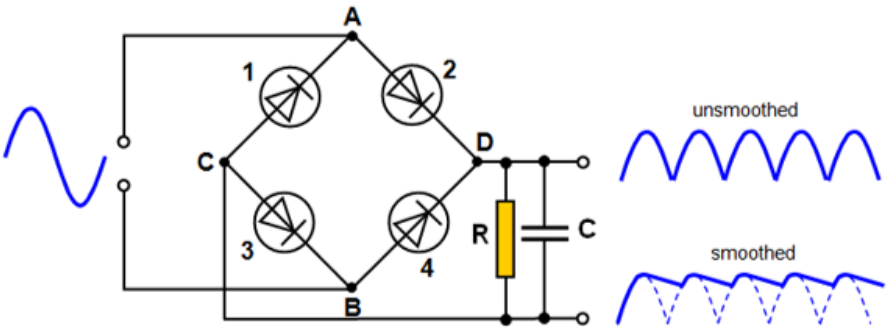


Figure 2.3: Basic rectifier

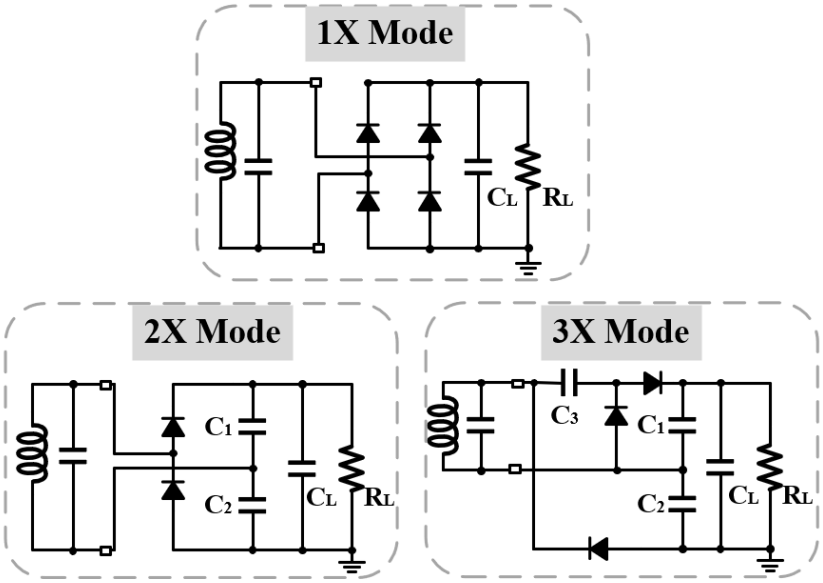


Figure 2.4: Equivalent structure of 1X/2X/3X rectifier

2.2.2 Proposed rectifier structure

Figure 2.5(a) shows the architecture of the proposed 3-mode reconfigurable rectifier. There are eight power switches ($M_{n1\sim2}$, $M_{p1\sim3}$, $S_{5\sim7}$), four comparators ($CMP2\sim5$) and three capacitors in this design. The startup mechanism we use in our design is to steer away from the initial relaxed state. In the initial relaxed state, capacitor C_1 and C_2 are slowly charged and V_{REC} starts increasing. St does not switch to '1' until V_{REC} reaches a certain level. Then the rectifier enters into the normal mode. The proposed rectifier has three working modes, depending on the feedback mode signal $Mode\_1$ and $Mode\_0$, the signals driving all the switches in the rectifier are generated according to $Mode\_1$ and $Mode\_0$ to configure the rectifier to one of the 1X, 2X and 3X modes. The ON/OFF states of all the 7 switches are given in Table 2. The operation of each mode is explained as follows:

Table 2: DRIVEN SIGNAL FOR SWITCHES

$Mode\_1$	$Mode\_0$	S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	0	ON	ON	OFF	OFF	OFF	ON	OFF
0	1	OFF	OFF	ON	ON	ON	ON	OFF
1	1	OFF	OFF	ON	ON	ON	OFF	ON

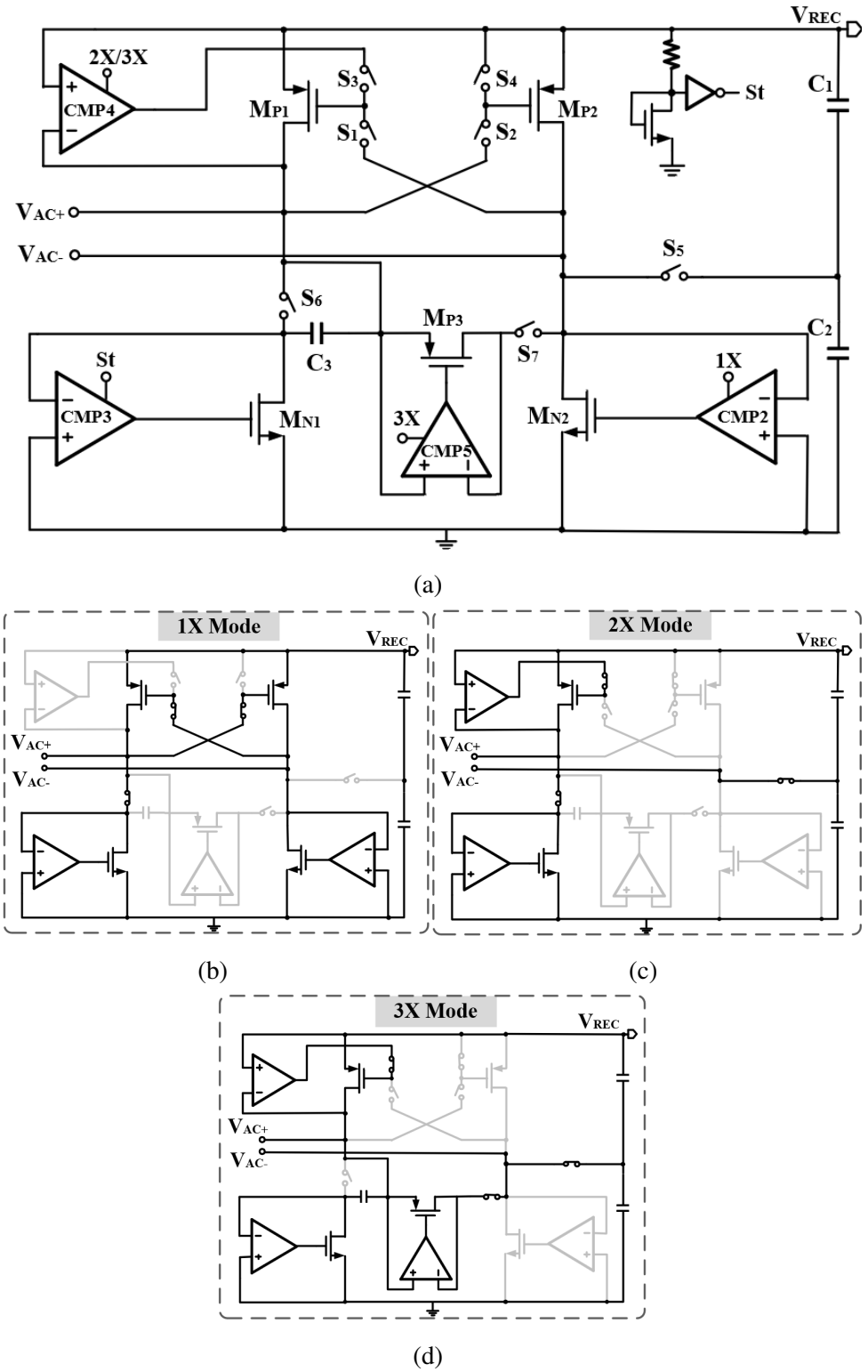


Figure 2.5: (a) /1X/2X/3X rectifier circuit implementation. (b) 1X Mode. (c) 2X Mode. (d) 3X Mode.

When $Mode\_1$ is '0' and $Mode\_0$ is '0', the rectifier works in 1X mode as illustrated in Figure 2.5(b). The switches S_1, S_2 and S_6 turn ON. M_{P1} and M_{P2} are cross-connected. The comparator $CMP2$ and $CMP3$ are enabled, forming a full-wave bridge rectifier.

When $Mode\_1$ is '0' and $Mode\_0$ is '1', 2X mode is activated as shown in Figure 2.5(c). S_1 and S_2 turn OFF, S_3, S_4, S_5 and S_6 turn ON. $CMP3$ and $CMP4$ become enabled. M_{P1} and M_{N1} become active diodes controlled by comparators. V_{AC-} is clamped at $V_{OUT}/2$ due to connection with capacitors. The full-wave voltage doubler is composed of two series-connected half-wave rectifiers.

When $Mode\_1$ is '1' and $Mode\_0$ is '1', 3X mode is activated, which is shown in Figure 2.5(d). S_3, S_4, S_5 and S_7 turn ON. S_6 turns OFF, extra capacitor C_3 is inserted in the circuit. M_{P3} becomes active diode, which is controlled by $CMP5$. The voltage tripler combines a voltage doubler and a half wave rectifier.

2.2.3 Input impedance analysis

Figure 2.5(e) shows the equivalent structure of proposed 1x/2x/3x rectifier, assume all equivalent diodes of the proposed rectifiers are ideal, all fly capacitors C_1, C_2 and C_3 have the same value. Here we analyze the input impedance of 3x mode rectifier, we already know that:

$$P_{out} = \frac{V_{DC}^2}{R_L} = \eta_{rec}\frac{V_{AC}^2}{2R_{in}} = \eta_{rec}P_{in} \tag{2.1}$$

where P_{in} and P_{out} are the input and output power of rectifier. R_{in} and R_L are the input impedance and load resistance of the rectifier. η_{rec} is the power conversion efficiency. From [14], It can be described as

$$\eta_{rec} = \frac{E_0}{E_{in}} \approx \frac{V_{DC}\cdot Q_0}{V_{AC}\cdot Q_{in}} \tag{2.2}$$

Where E_{in} is the input energy of the rectifier and E_{out} is the output energy of the rectifier. Q_{in} and Q_{out} are the input and output charge of the rectifier in one cycle.The output capacitor of the proposed system is large enough. In the 1x mode, the rectifier is configured as the full-wave bridge rectifier, in each half cycle, the capacitor is being charged. In the steady state, the same amount of charge is removed from the capacitors. so $Q_{in} = Q_{out}$, the input resistance is approximately $R_L/2$. In the 2x mode, the rectifier forms a voltage doubler, at the negative half

cycle, capacitor C_2 is being charged. If we assume $C_2 = C_1 = C$, the amount of charge that flows in one half cycle can be expressed as

$$Q_{2x} = C \cdot V_{AC} = \frac{1}{2} Q_{in} \tag{2.3}$$

At the positive half cycle, the same amount of charge is stored in capacitor C_1, from the point of output, capacitor C_1 is series-connected with C_2, the total capacitance is ½ C, the output voltage at the top plate of C_1 is 2 times V_{AC}, Thus, the amount of charge that flows out if rectifier in steady state is:

$$Q_{out2x} = \frac{1}{2} C \cdot 2V_{AC} = \frac{1}{2} Q_{in} \tag{2.4}$$

Combining equation (2.1), (2.2), (2.4), the equivalent input resistance is $R_L/8$.

In the 3x mode, the rectifier is configured as a voltage doubler and a half-wave rectifier. Capacitor C_3 and C_2 are charged to the peak value of the input voltage V_{AC} in parallel at the negative cycle of the input voltage source. From the point of view of the output V_{REC}, capacitor C_1 is stacked on the capacitor C_2. During the positive cycle of the input voltage source, the top plate of capacitor C_1 sees a total of 2 times peak value of the input voltage V_{AC} due to voltage clamper C_3. Then we get 3 times peak value of input voltage source V_{AC} at the output. From the point of view of the output V_{REC}, capacitor C_3 is parallel-connected with capacitor C_1 and series-connected with capacitor C_2. All fly capacitors C_1, C_2 and C_3 have the same value C. In the negative half cycle, all output charge come from capacitor C_1. Thus, the charge Q_1 from C_1 is $Q_{out}/2$. In the positive half cycle, the charge from C_3 flows to C_1 and the output, the charge from C_2 is the difference between Q_1 and Q_3. According to Kirchhoff Circuit Laws, we can get:

$$Q_1 = \frac{Q_{out}}{2} \tag{2.5}$$

$$Q_3 = Q_1 + \frac{Q_{out}}{2} \tag{2.6}$$

$$Q_2 = Q_3 - Q_1 \tag{2.7}$$

Combining equation (2.10), (2.11), (2.12), here we get

$$Q_{in} = Q_3 + Q_1 + Q_2 + Q_3 = 3Q_{out} \tag{2.8}$$

The voltage conversion ratio(VCR) is defined as

$$M = \frac{V_{REC}}{V_{AC}} \tag{2.9}$$

According to the equation (2.2), the rectifier's power conversion efficiency can be:

$$Q_1 = \frac{Q_{out}}{2} \tag{2.10}$$

$$Q_3 = Q_1 + \frac{Q_{out}}{2} \tag{2.11}$$

$$Q_2 = Q_3 - Q_1 \tag{2.12}$$

Combining equation (2.10), (2.11), (2.12), here we get

$$Q_{in} = Q_3 + Q_1 + Q_2 + Q_3 = 3Q_{out} \tag{2.13}$$

The voltage conversion ratio(VCR) is defined as

$$M = \frac{V_{REC}}{V_{AC}} \tag{2.14}$$

According to the equation (2.2), the rectifier's power conversion efficiency can be:

$$\eta_{rec3X} = \frac{M_{3X}}{3} \tag{2.15}$$

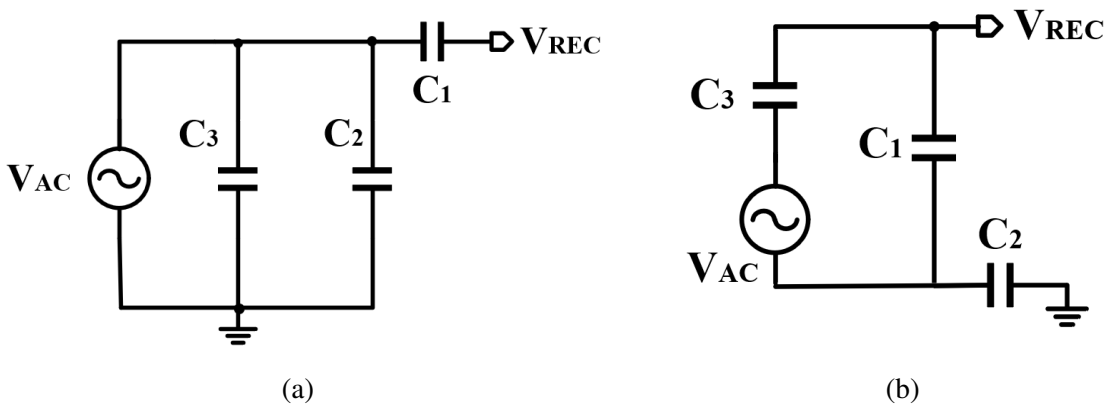
Combining the equation (2.1), (2.14), (2.15), the input resistance under 3x mode is:

$$R_{in3X} = \frac{R_L}{6M_{3X}} \tag{2.16}$$

The input impedance of the rectifier can hugely affect the quality factor of the secondary LC tank loaded by the rectifier, which has an impact on the system power efficiency η_{sys} and system voltage gain A_{sys}. The coupled voltage may vary with the change of working modes. The details will be discussed in the next subsection.

2.3 Start-up mechanism

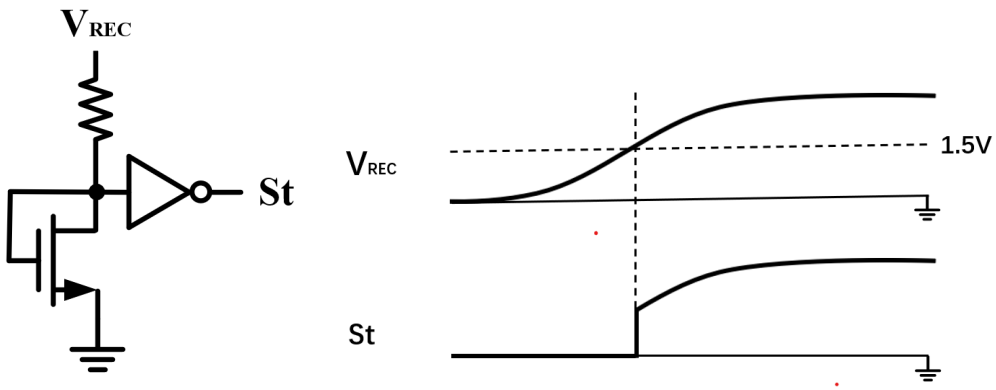
The implants is a self-powered system, the supply voltage is the output voltage and it starts from 0. It requires a startup circuit to steer away from the relaxed state. The start up consists of a very large resistor with a diode-connected transistor, which is shown in Figure 2.7(a). The threshold voltage of this diode-connected transistor is about 0.7V. The drain of this transistor is



(a) (b)

Figure 2.6: (a) Negative cycle. (b) Positive cycle.

connected with an inverter powered by V_{REC}. When V_{REC} is about 1.5V, the threshold voltage of this inverter is about 0.7V. The operational principle of start up is shown in Figure 2.7(b). When V_{REC} starts from 0V, the circuit is in relax state, St is 0. The rectifier is in passive mode, all comparator are disabled, which is shown in Figure 2.8. M_{N1} and M_{N2} are connected to ground, M_{P1} and M_{P2} are cross-connected with the one gate connected with the other drain. The transistor becomes passive diode. The output capacitor and C_1 and C_2 is slowly charged, V_{REC} is gradually increasing. When V_{REC} increases to 1.5V. The inverter start working and St switch to 1. The rectifier will then works in normal mode. The comparators are enabled.



(a) (b)

Figure 2.7: (a) Start up Circuit. (b) Start up waveform.

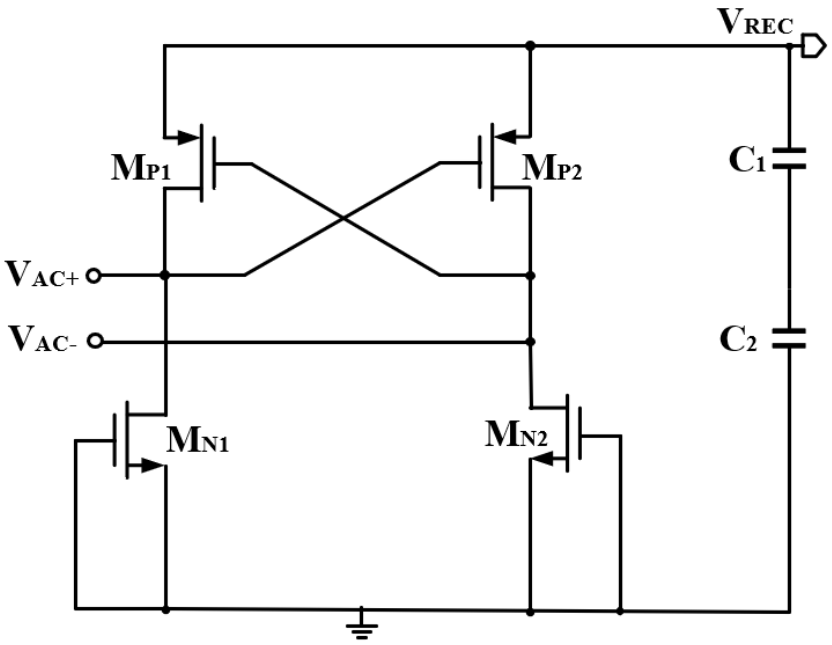


Figure 2.8: Passive Recitifer

2.4 Delay compensation technique

According to Figure 2.5, the operational principle of the active rectifier is comparing the drain and source voltage of MOS transistor and control the ON-OFF process. For example, for NMOS switch, when $V_{AC+} < 0$, the output of CMP3 becomes high, M_{N1} turns on. After V_{AC+} swings above 0, M_{N1} is turned off by CMP3. To reduce the conduction loss through switches, MOSFET switches should be well designed with large sizes, which result in the comparator delay and large gate capacitance driving the active rectifier inaccurately. Besides, the reverse leakage current from the load capacitor may flow back into the rectifier, which degrades the efficiency of the rectifier[15][16]. As shown in Figure 2.9, the turn-on delay shortens the conduction time, the turn-off delay make M_{N1} turn on when V_{AC+} has risen above 0, the charge in the load capacitor will flow to the ground. For the parallel-resonant secondary coil, both on delay and off delay can degrade the PCE and VCR of the active rectifier.

In order to compensate for the comparator and improve PCE and VCR of the active rectifier, switching-delay compensated techniques are applied. Figure 2.10 (a) shows the delay compensated comparator structure for NMOS switch M_{N1} and M_{N2}, the comparator is activated when enable signal EN becomes high. The non-overlapping structure generate control signal Sn and $\overline{Sn}$ to add positive or negative offset for the comparator. For example, When Sn is high, M_{N5}

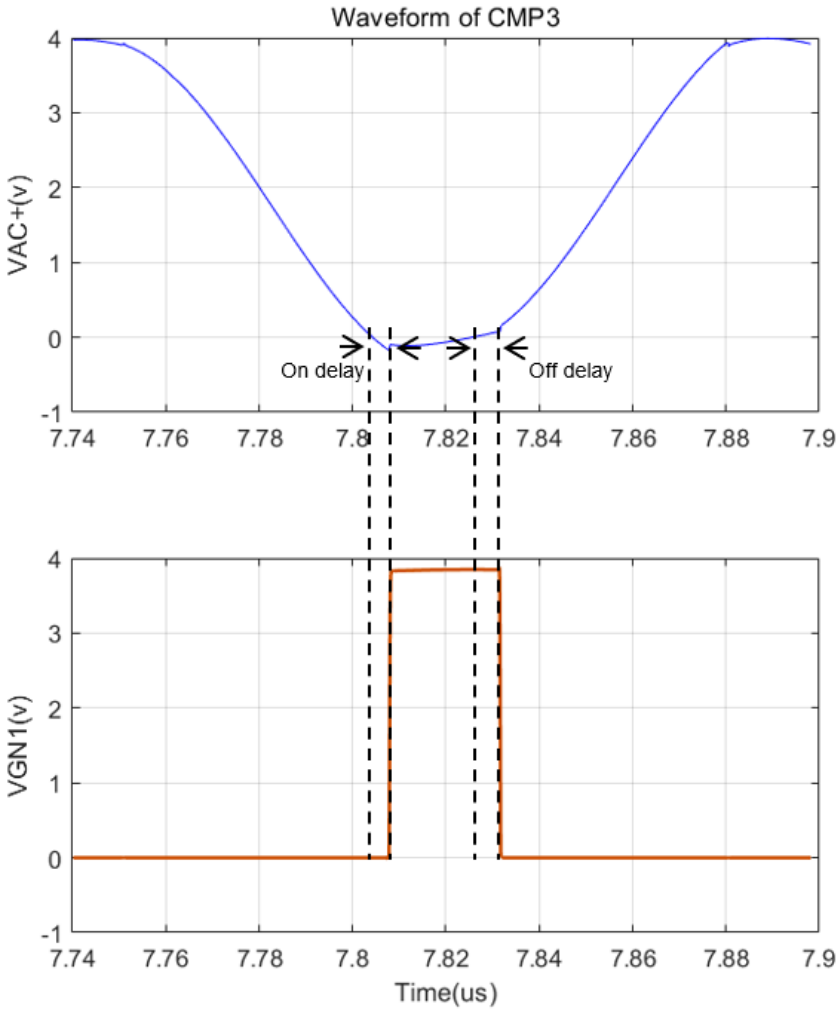


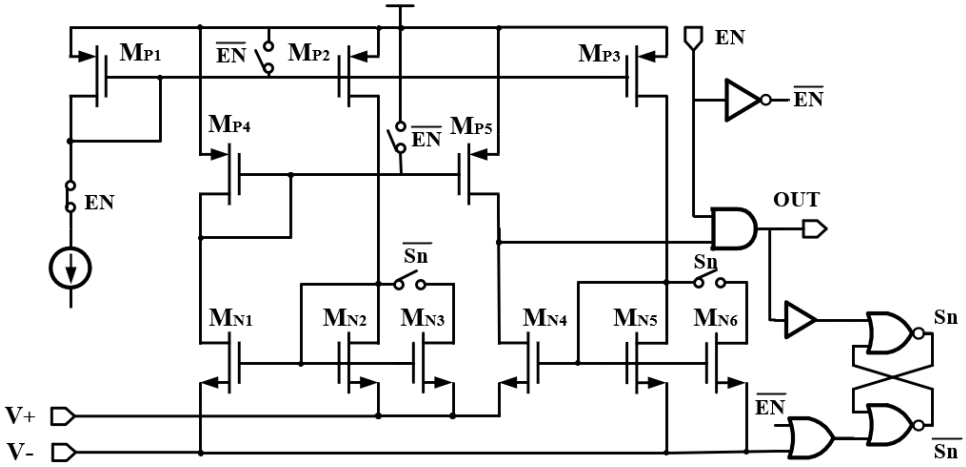
Figure 2.9: Waveform of CMP3 without delay compensation

and M_{N6} are parallel-connected, the on-resistance of this branch will be lower, but the biasing current from M_{P3} is stable, so the drain voltage of M_{N5} will be lower enough to turn off M_{N4} earlier, resulting in a positive offset for the comparator, so the output OUT can be high earlier to compensate the turn-on delay. Conversely, when Sn is low, $\overline{Sn}$ is high, M_{N2} and M_{N3} are parallel-connected, and the size of M_{N4} is larger than M_{N5}. so the on-resistance of M_{N4} is smaller. the current that flows through M_{N4} are higher, the current will be mirrored at M_{N1} and M_{N2}. Their gate voltage will be high enough to turn on earlier, resulting in a negative offset, then the output OUT will be low earlier to compensate for the turn-off delay. To generate the non-overlapping signal Sn and $\overline{Sn}$, when OUT is low, if $V-$ increases to about $VREC/2$, Sn is switching from low to high, and $\overline{Sn}$ is switching from high to low. The turn-on delay will be compensated. When OUT is switching from low to high, Sn is switching from high to low after the delay introduced by delay cell, and $\overline{Sn}$ is switching from high to low if V- is smaller than $VREC/2$. The negative offset is added, the comparator can prevent from turn-off delay and the reverse current from the ground. When enable signal EN is low, the biasing MOS transistor are all closed. There is no current flowing inside the comparator to save the energy.

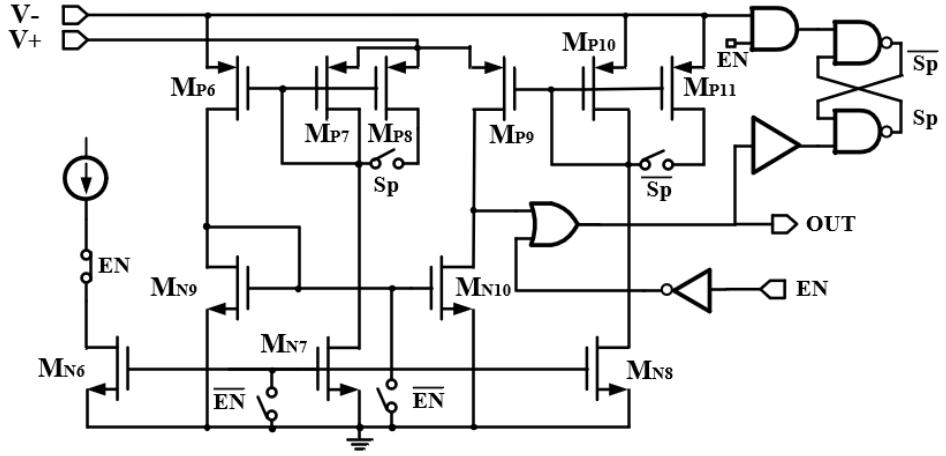
Figure 2.10 (b) shows the comparator schematic for PMOS switch CMP4. It is an up-down mirror image of structure of CMP2 & CMP3. $V+$ is connected to $VREC$ and $V-$ is fluctuating. The operation is similar to NMOS switch comparator, but the transistor sizes are different.

In Figure 2.11(a), the comparator structure for CMP5 is shown. When the rectifier is in 3X mode, $V-$ equals to $VAC-$. $V+$ is fluctuating. Thus, the input of $CMP5$ can not directly connect to logic gate. The output of this comparator cannot pull down. A level shifter is applied to solve this problem[17], which is shown in Figure 2.11(b). Since there is no delay compensation technique applied for this comparator. A series of delay cell is used at the output. In this way, M_{P3} can only be open for a fixed period in each cycle, which can reduce the conduction loss.

Simulation results were performed to verify the effectiveness of this delay compensation method. The load condition is 800Ω, the output is 3.2V. The proposed reconfigurable rectifier is configured as 1X mode. The simulated waveform is shown in Figure 2.12. We can see when S_n becomes high, turn-on delay are compensated, when S_n- becomes high, turn-off delay are eliminated. Figure 2.13 shows the efficiency of the rectifier with and without delay compensation under 1X mode. Without delay compensation, the recitfier efficiency will degrade about 3% over a wide input range.

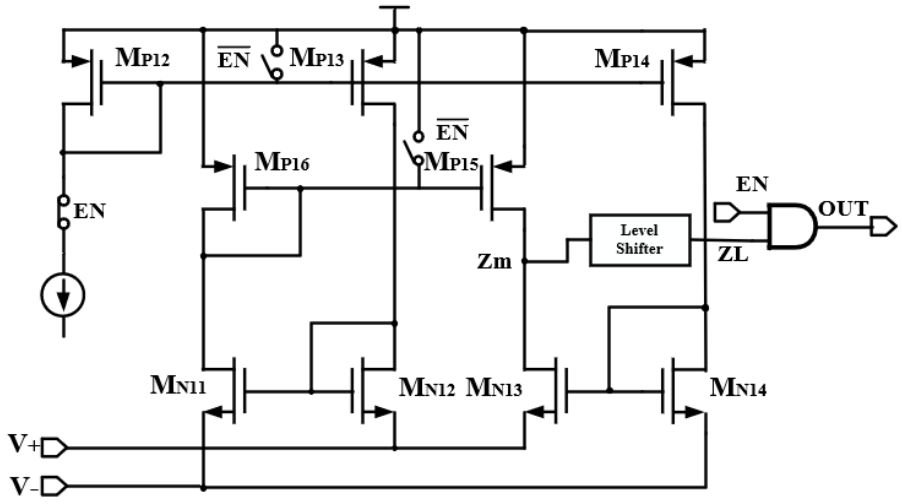


(a)

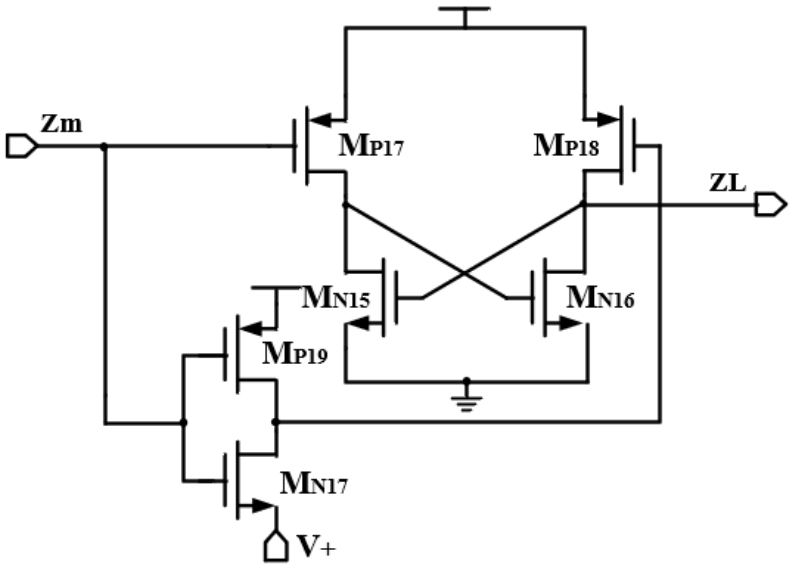


(b)

Figure 2.10: (a) Structure of CMP2 & CMP3. (b) Structure of CMP4.



(a)



(b)

Figure 2.11: (a) Structure of CMP5. (b) Level Shifter.

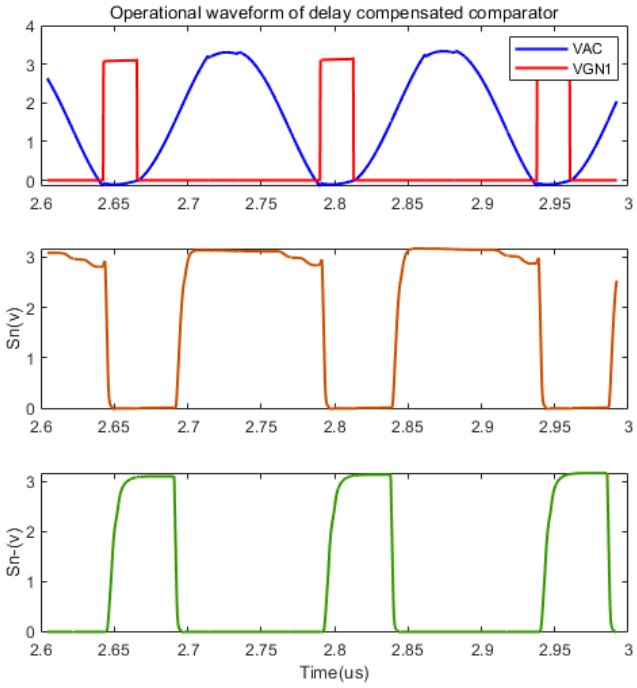


Figure 2.12: Operational waveform of delay compensated comparator

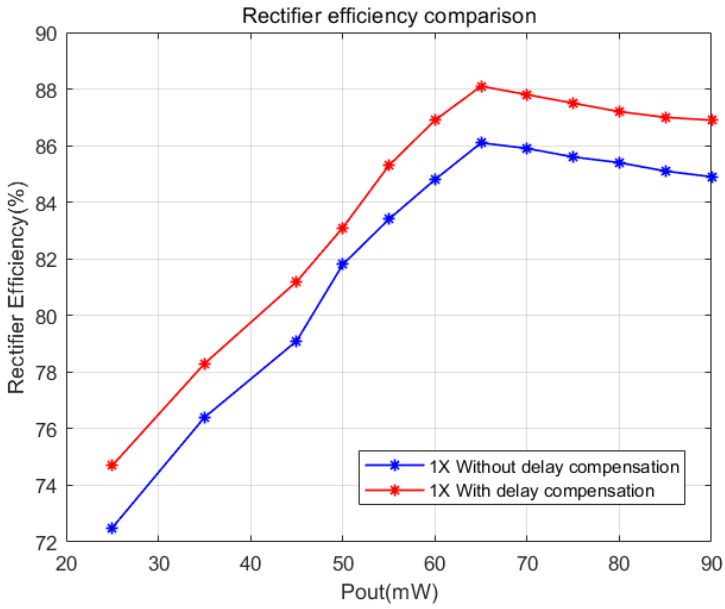


Figure 2.13: Rectifier efficiency with and without delay compensation

3 Analysis of resonance and proposed rectifier

3.1 Analysis of resonance

Figure 3.1 shows a pair of ideal coupled inductors with primary coil L_1 and secondary coil L_2 with mutual inductance M driving a load resistor R_L. The coil system can be described as:

$$V_1(t) = L_1 \frac{dI_1}{dt} + M \frac{dI_2}{dt} \tag{3.1}$$

$$V_2(t) = M \frac{dI_1}{dt} + L_2 \frac{dI_2}{dt} \tag{3.2}$$

The coupling factor k are used to describe the ratio of the open-circuit actual voltage ratio to the ratio that would be obtained if all the flux coupled from one magnetic circuit to the other. It can be defined as:

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{3.3}$$

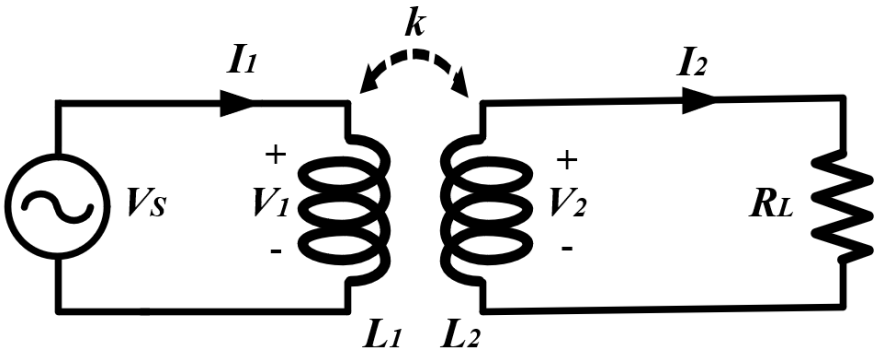


Figure 3.1: Ideal couple coils

For an WPT system for biomedical implants, the system power efficiency η_{sys} is very important. High system power efficiency can reduce the energy absorbed by human tissue(SAR). Besides, the system power gain A_{sys} is also important since it will affect the input voltage of the rectifier. Now, we will analyze the system power efficiency η_{sys} and the system power gain A_{sys} under different working modes and load conditions.

In IMD application, the weak coupling between primary coil and secondary coil is common due to skin and bones. Figure 3.3 is the resonant inductive coupling, capacitors are added to realize resonance circuits. There are two resonant ways, which is series resonant and parallel resonant. They can both be applied for the resonant wireless power transfer. Their advantages and disadvantages are discussed below.

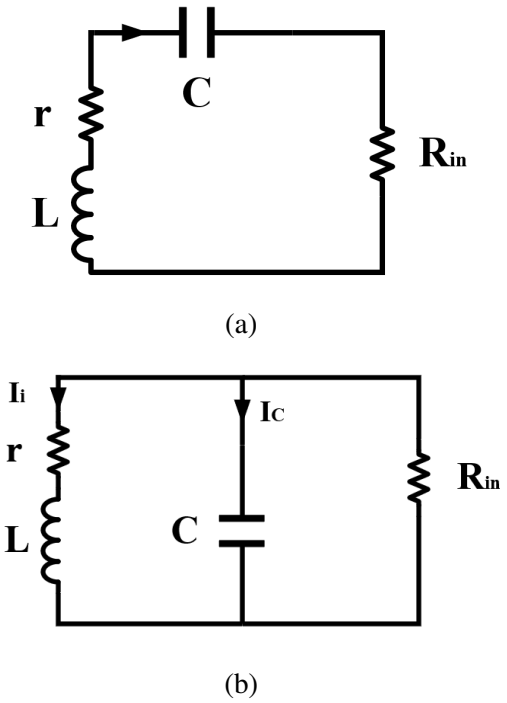


Figure 3.2: (a) Series resonant model (b) Parallel resonant model.

3.1.1 Series resonant

In most WPT cases, the primary coil applies series-resonance, the equation of the total impedance is shown below

$$Z = r + jX_L + jX_c \tag{3.4}$$

when the circuit is within series resonance, $wL = \frac{1}{wC}$ and X_L=X_c, the total impedance of the circuit will be minimized. The primary coil can increase AC current to get a larger magnetic field.

However, for the secondary coil, the series resonant may bring some problems. When the coil is driven with series capacitors, increasing the coil current can only be done by lowering the equivalent series resistances. The very large transistors need to be used to reduce the on-resistance, which will increase the gate driving loss. When we use the parallel resonant capacitor, the current that flow through the coil can be expressed as:

$$I_i = \frac{U}{\sqrt{r^2 + X_L^2}} = \frac{U}{\sqrt{r^2 + (wL)^2}} \tag{3.5}$$

The current that flow through capacitor can be expressed as:

$$I_c = \frac{U}{X_c} = wCU \tag{3.6}$$

3.1.2 Parallel resonant

For the secondary coil, in low-power application, parallel resonant is a better option. When the circuit is within parallel resonance, the relationship between both current can be expressed as:

$$I_i \sin\varphi = I_c \tag{3.7}$$

$$\sin\varphi = \frac{X_L}{\sqrt{r^2 + X_L^2}} \tag{3.8}$$

since the series resistance of the coil r is very small, so $\sin\varphi \approx 1$, which will minimize the total current of the current, the current handling capability of the active device will be smaller. Thus, the primary coil prefers series matching and the secondary coil prefers parallel matching. The primary coil has inductance L_{s1} and small series resistance R_{s1}. Wireless power driven by primary coil is coupled with secondary coil with inductance L_{s2} and small series resistance R_{s2}. Parallel-connected resonant capacitor C_{p2} is applied to match with the input impedance of rectifier R_{in}. The induction model of proposed system is shown in Figure 3.3.

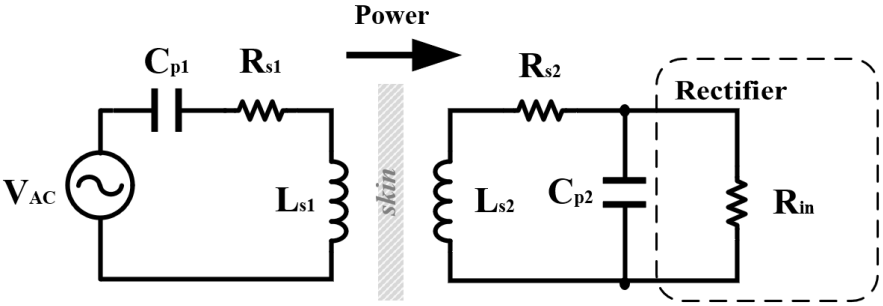


Figure 3.3: Induction Model of Proposed system

3.2 System voltage gain

We assume the equivalent quality factor of inductor L_{s1} and L_{s2} is Q_1 and Q_2 respectively. According to [14], If we assume R_{in} is large enough, $Q_\alpha \gg 1$, then the power-link gain A_{link}

can be approximately as

$$A_{link} = \frac{knQ_1Q_2}{k^2Q_1Q_2 + 1 + Q_2/Q_\alpha} \tag{3.9}$$

where $n = \sqrt{L_2/L_1}$. Combining equation (2.14) and (3.9), the system power gain A_{sys} under three working modes can be

$$A_{sys1X} = A_{link}(Q_{\alpha 1X}) \cdot M_{1X} \tag{3.10}$$

$$A_{sys2X} = A_{link}(Q_{\alpha 2X}) \cdot M_{2X} \tag{3.11}$$

$$A_{sys3X} = A_{link}(Q_{\alpha 3X}) \cdot M_{3X} \tag{3.12}$$

We can see that the system power gain is not only related to the voltage conversion gain M, but also to the system link gain A_{link}. If the received signal amplitude of 2X mode is significantly smaller than the received amplitude of 1X mode, even though the voltage conversion ratio of 2X mode is twice larger than 1X mode, the output signal amplitude in 2X mode may not be higher than that in 1X mode. The same thing applied to 3X mode. According to equation (3.9), for a reconfigurable rectifier, the change of Q_α has an impact on the system link gain A_{link}. Q_α is mainly affected by the input impedance of the reconfigurable rectifier. Therefore, the load condition can hugely affect the system voltage gain. Under different load condition, the voltage gain in 3X mode A_{sys3X} can be smaller than the gain in 2X modeA_{sys2X}. Thus, to analyze the performance of 3X mode, we need to deteremine the voltage-gain breakeven value of the load resistance, at which $A_{sys3X} = A_{sys2X}$. Combining the equation (3.9), (3.11), (3.12), the breakeven value between 2X mode and 3X mode R_{Lb} can be described as:

$$R_{Lb} = \frac{2Q_2}{\omega_0 C_{p2}(1 + k^2Q_1Q_2)} \cdot \frac{M_{2X}M_{3X}}{M_{3X} - M_{2X}} \tag{3.13}$$

According to [14], the the voltage-gain breakeven value of the load resistance between 1X mode and 2X mode R_{La} can be described as:

$$R_{La} = \frac{2Q_2}{\omega_0 C_{p2}(1 + k^2Q_1Q_2)} \cdot \frac{M_{1X}M_{2X}}{M_{2X} - M_{1X}} \tag{3.14}$$

When the load resistance is smaller than R_{La}, the 1X system voltage gain is larger than 2X system voltage gain, even though the VCR of 2X is larger than the VCR of 1X, the output of 1X mode can still be larger than that in 2X mode, since the input amplitude of 2X mode may be smaller. Thus, only when the load resistance is larger than R_{La}, the rectifier can switch from 1X mode to 2X mode to gain larger output. Similarly, when the load resistance is smaller than R_{Lb},

the 2X system voltage gain is larger than 3X system voltage gain. Thus, to make sure that the whole system can normally work, the load resistance of the system must be higher than R_{Lb}. Here we assume some data for the primary coil and secondary coil to demonstrate how the load condition will influence the system voltage gain A_{sys} and system power transfer efficiency η_{sys}. For the primary coil, $L_1 = 1.3\mu H$ and $Q_1 = 59$; For the secondary coil, $L_2 = 300nH$ and $Q_2 = 12$. The coupling factor is 0.06. The AC input frequency is 6.78MHz. Thus, the system voltage gain A_{sys} under different load conditions are shown in Figure 3.4. In Figure 3.4, We can see that in Region 1, when the load resistance is smaller than R_{La}, 1X gain is higher than 2X gain, both 2X mode and 3X mode cannot normally work. in Region 2, 3X gain is still smaller than 2X gain. Only when the load is higher than R_{Lb}, which is in Region 3, the whole system can work correctly.

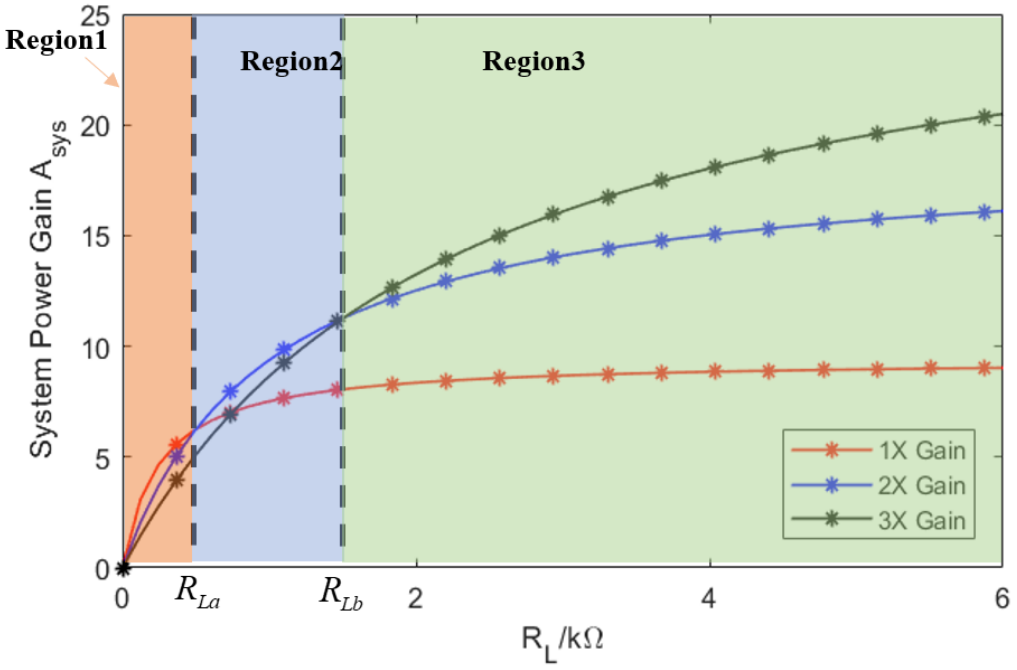


Figure 3.4: System power gain A_{sys} vs Load resistance R_L.

3.3 System voltage efficiency

The system voltage efficiency is important for our system, high efficiency can reduce the dissipated energy inside human body. According to [18], The primary link efficiency is defined as the ratio of the power P_{sec} that reaches the secondary circuit to the power P_{link} ffrom inductive link. It can also be calculated as the ratio of dissipated power in R_{eq} to the total dissipated power in R_{eq} and R_{s1}. The primary link efficiency can be described as:

$$\eta_{primary} \equiv \frac{P_{\sec}}{P_{link}} = \frac{R_{eq}}{R_{eq}+R_{s1}} = \frac{k^2 Q_1 Q_2}{1+\frac{Q_2}{Q_\alpha}+k^2 Q_1 Q_2} \tag{3.15}$$

The secondary link efficiency can be the useful energy P_{OUT} dissipated in the load to the accepted energy in the secondary circuit P_{sec}. The secondary link efficiency can be described as:

$$\eta_{\sec ondary} = \frac{Q_2}{Q_\alpha + Q_2} \tag{3.16}$$

The power-link efficiency η_{link} is then described as:

$$\eta_{link} = \eta_{prmiary} * \eta_{\sec ondary} = \frac{k^2 Q_1 Q_2^2}{(1+\frac{Q_2}{Q_\alpha}+k^2 Q_1 Q_2)(Q_\alpha + Q_2)} \tag{3.17}$$

where k is the coupling factor between primary and secondary coil, unloaded primary and secondary coil quality factors are $Q = \omega_0 L_{s1}/R_{s1}$, $Q = \omega_0 L_{s2}/R_{s2}$ respectively. $Q_\alpha = \omega_0 C_{p2} R_{in}$ is the secondary quality factor loaded by the rectifier. Then, the system power efficiency η_{sys} under three working modes can be given by:

$$\eta_{sys1X} = \eta_{link}(Q_{\alpha 1X}) \cdot M_{1X} \tag{3.18}$$

$$\eta_{sys2X} = \eta_{link}(Q_{\alpha 2X}) \cdot \frac{M_{2X}}{2} \tag{3.19}$$

$$\eta_{sys3X} = \eta_{link}(Q_{\alpha 3X}) \cdot \frac{M_{3X}}{3} \tag{3.20}$$

where $Q_{\alpha 1X} = \omega_0 C_{p2} R_{in1X}$, $Q_{\alpha 2X} = \omega_0 C_{p2} R_{in2X}$, $Q_{\alpha 3X} = \omega_0 C_{p2} R_{in3X}$.

The system power efficiency η_{sys} for different loading conditions are shown in Figure 3.5. We can see that 1X mode can achieve highest efficiency under heavy load. In Region 4, 1X mode efficiency is higher than both 2X efficiency and 3X efficiency. But with the increase of load resistance, the system power efficiency is gradually decreasing. Under light load condition, 2X mode and 3X mode efficiency is better. In Region 6, when the load resistance is higher than R_{Lm}, 3X mode system efficiency becomes the highest, but the output power will be smaller.

The proposed rectifier can be adaptively adjusted when the input AC amplitude changes due to coupling variation, which is realized with duty ratio detector and state control unit. Unbalanced comparator is used to reduce the conduction loss. The detail of circuit implementation is illustrated in Section IV.

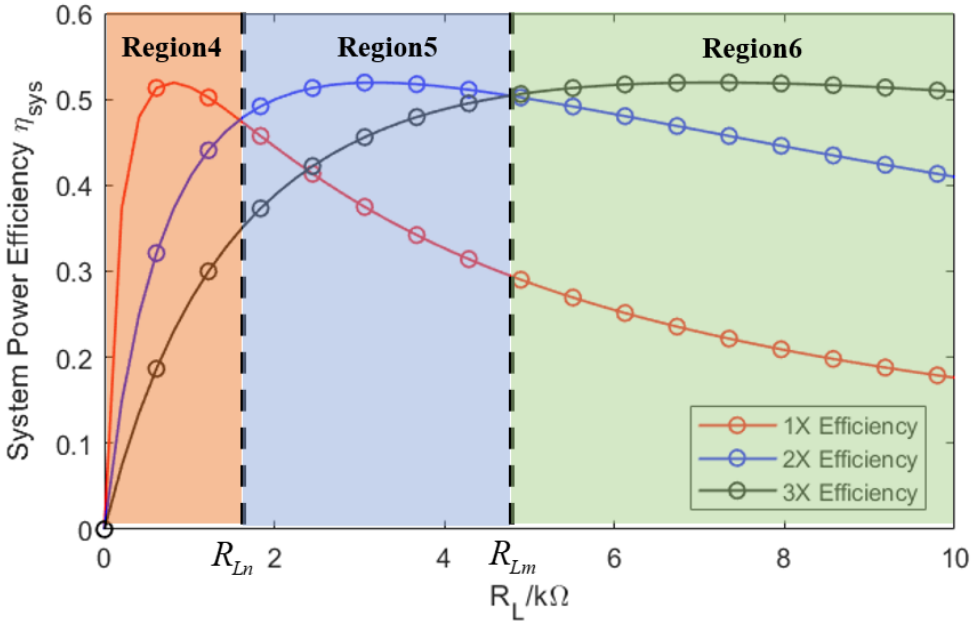


Figure 3.5: System power efficiency η_{sys} vs Load resistance R_L.

4 Circuit implementation

4.1 Duty ratio detector

Since there are three working modes in our reconfigurable rectifier, two switching periods are needed for the rectifier, which are $1x \sim 2x$ and $2x \sim 3x$. These three working mode are represented by two bit $MODE$ signal, which are '0,0', '0,1', '1,1'. To let the rectifier can adjust itself when the input amplitude changes, the local loop is required to detect the duty ratio of $MODE$ signal and reconfigure it to the correct working mode. Thus, a fast duty ratio detector is needed for our design. The structure of our duty ratio detector is shown in Figure 4.1. The duty ratio is detected by controlling the charging and discharging of the small capacitors in one cycle[19]. The switch is controlled by the $MODE$ signal, the charge from constant current source will flow to the smaller capacitors C_{d1} and C_{d2}. The top plate voltage of both capacitors are divided by a series of large resistance. If the duty ratio of $MODE$ signal is 100%, one percent top-plate voltage of capacitor C_{d1} can be higher than that on capacitor C_{d2}. The comparison result will be shown in P_{up}. Then the rectifier will change to the other switching period to realize larger output voltage. Similarly, if the duty ratio of $MODE$ signal is 0%, then the inverting signal $\overline{MODE}$ is 100%. one percent top-plate voltage of capacitor C_{d2} can also be higher than that on capacitor C_{d1}. P_{down} will become '1', the rectifier moves to the other switching period to get smaller output. After one cycle, all two capacitors C_{d1} and C_{d2} will be discharged by Rst signal. The detecting cycle is 16 times input AC signal period.

4.2 State control and window comparator

The other requirement for the change of mode-switching period is the comparison result of window comparator. Only when the output voltage is out of window formed by reference voltage, can the mode-switching period change to the other one. The structure of state control unit is shown in Figure 4.2. When the output voltage is out of window, Win_cmp will be '1'. P_{up} and P_{down} can pass to up/down counter to change $State$, which represents the mode-switching period. The sampling period of up/down counter is synchronized with duty ratio detector. Only the result of P_{up} and P_{down} at the highest top plate voltage will be sampled to change $State$.

4.3 Independent current source

A current source is needed for the comparator and duty ratio detector. Since we apply delay compensation technique for the comparator in the rectifier, the compensated delay is related

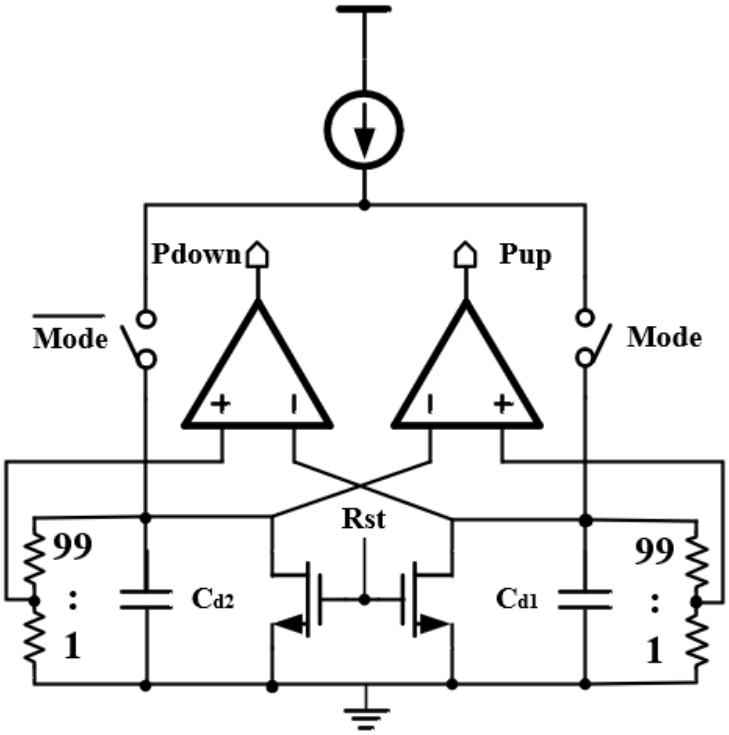


Figure 4.1: Duty ratio detector

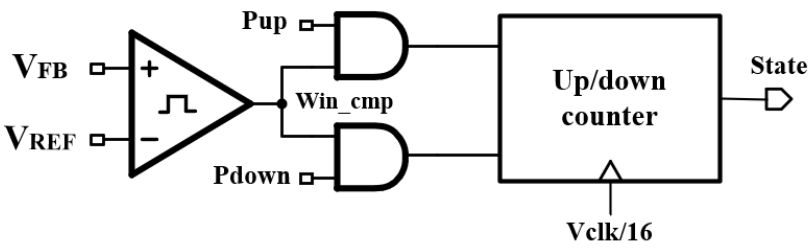
with the current level. If the current is larger, with the increase of current level, the compensated delay will be smaller[6], which will influence the PCE and VCR. Also, the consumed energy for the duty ratio detector and other comparator will be larger, which also degrades the efficiency. In order to provide a stable current for the delay-compensated comparator and other components, independent current source is used in this design[20]. It can provide a stable current at the branch no matter how the supply voltage changes. Here is how this independent current source works, M_{p1}, M_{p2}, M_{N1}, M_{N2} and R_3 forms a supply-independent current source, for M_{N1} and M_{N2}, if $KI_{REF} = I_{OUT}$, we can write $V_{GS1} = V_{GS2} + I_{D2}$ or

$$\sqrt{\frac{2I_{OUT}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{OUT}}{\mu_n C_{ox} K(W/L)_N}} + V_{TH2} + I_{OUT}R_3 \tag{4.1}$$

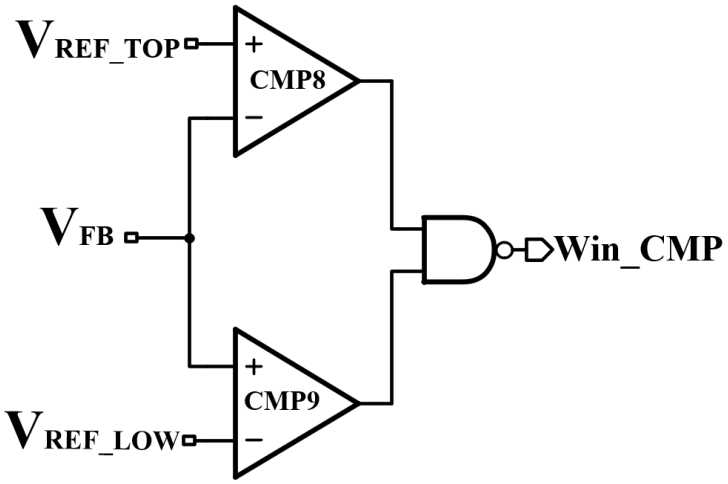
If we neglect the body effect, we can get

$$I_{OUT} = \frac{2}{\mu_n C_{ox} * (W/L)_N} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \tag{4.2}$$

we can see that the I_{OUT} is not related with the supply voltage. But this circuit needs a start-up mechanism, if all of the transistors carry zero current when the supply is turned on, they may



(a)



(b)

Figure 4.2: Schematic of (a)state control. (b) window comparator

remain off no matter how the supply voltage changes because the loop can support a zero current in both branches. This situation is not predicted in equation 4.2 since we assume $I_{OUT} \neq 0$. This problem is solved by adding a start-up circuit that can offer a biasing point when the supply is turned on. The schematic is shown in Figure 4.3. With the increase of supply voltage, the gate voltage of M_{N4} and M_{N3} are also increasing. The drain voltage of M_{N3} can offer a steer-up voltage for the loop. Then, the supply voltage will become high enough to turn on M_{N4}. The gate voltage of M_{N3} will then decrease to turn off. The loop will then become independent from the supply voltage. The waveform of independent current source has been shown in Figure 4.4. We can see that the current source is turned on when supply voltage reaches 1V, which is earlier than the start-up voltage 1.4V of the whole circuit. Then the current soonly increase to designed current. When the supply increase from 1.5V to 4.5V, the ripple current is only $3\mu A$, which is 20% of the designed current.

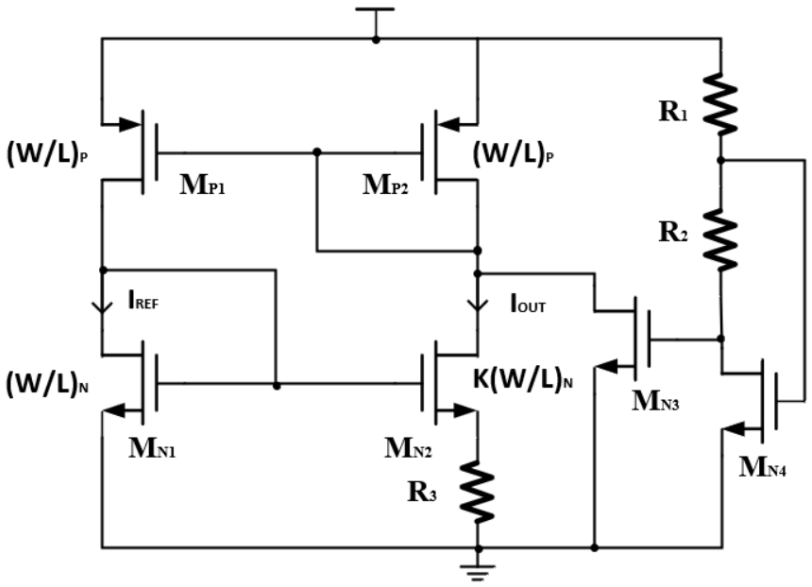


Figure 4.3: Independent current source

4.4 Frequency divider Design

The clock signal of our system is generated by the frequency divider unit. First, The AC signal V_{AC+} is harvested by an inverter. Then, we can get a square wave with the same frequency. But the required clock frequency is one sixteenth of AC frequency. Thus, a frequency divider is applied. It consists of four JK-flipflops. The structure is shown in Figure 4.5. The J and K inputs of each flip-flop are set to 1 to produce a toggle at each cycle of the clock input. For each

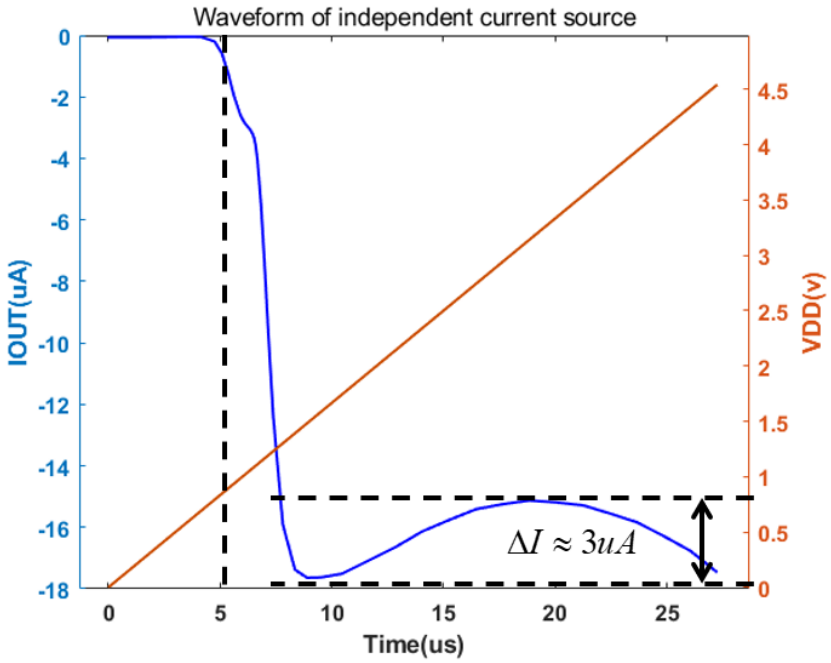


Figure 4.4: Waveform of current source

two toggles of the first cell, a toggle is produced in the second cell, and so on down to the fourth cell. This produces a binary number equal to the number of cycles of the input clock signal.

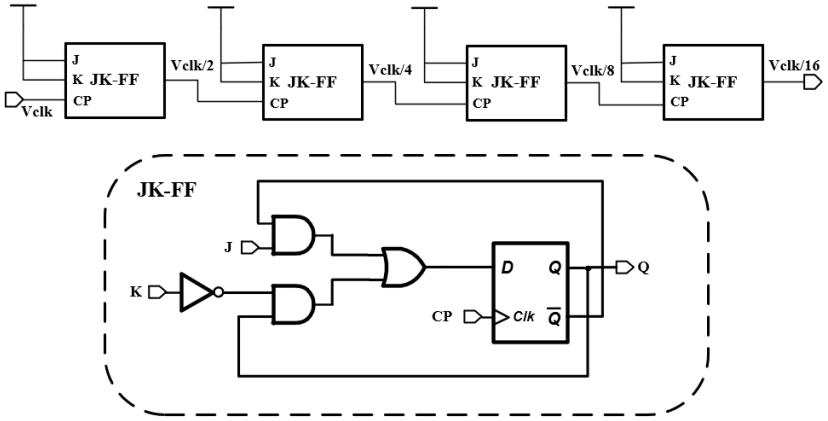
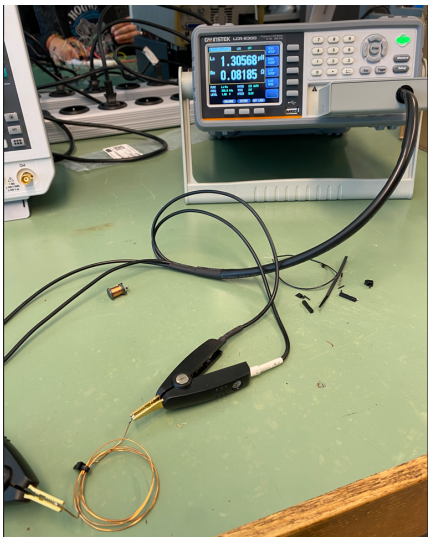


Figure 4.5: Schematic of frequency divider

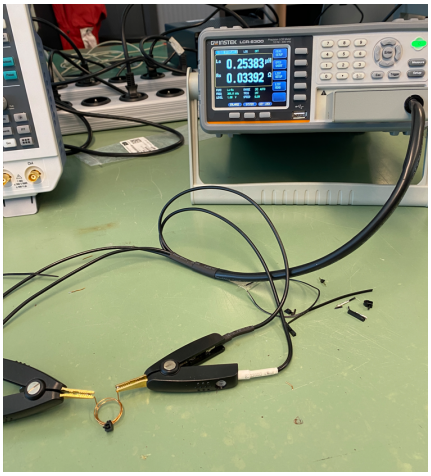
5 Results

5.1 Experiment setup

(a)



(b)



(c)

Figure 5.1: (a) Experiment setup (b) Primary coil (c) Secondary coil.

Table 3: Diameter for Coils

Coils	Diameter	Inductance	Quality factor@6.78Mhz
Primary coil	2.5cm	1.3μH	52
Secondary coil	1cm	250nH	17

The measurement are done in the measurement room LB.690 in the building of the Faculty of Electrical Engineering, Mathematics and Computer Science at Delft University of Technology. Primary coil and secondary coil are designed. Their data and photos are shown in Figure 5.1 and Table 3. The experiment setup includes pulse generator, oscilloscope, primary coil, secondary coil, PCB, DC signal generator. The coil are enamelled copper wire, the conduction area is $0.203mm^2$. The copper wire are covered with the dis-conductive material, which is very suitable for the wireless power transfer coils. The coil will be soldered to the circuit board to form resonant LC-meter are also used to measure the inductance and series resistance of the coils. According to the data measured by LC-meter, the inductance of primary coil is 1.3μH, the diameter of the coil is 3cm, and 4 turns. The inductance of secondary coil is 220nH, the diameter is 1cm and 3 turns. since the AC frequency is 6.78MHz, according to quality factor $Q = \omega L/R$, the quality factor is 52 and 15.

The pulse generator can generate AC signal with 6.78Mhz as transmitted signal, due to the mismatch of capacitors, the actual resonant frequency is Mhz. The transmitted signal amplitude is . When the distance between primary coil and secondary coil is 1cm, the received signal amplitude is V. Oscilloscope is used to monitor the signal waveform. The DC voltage source is responsible for generating ground signal rail. The bare die is bonded in PCB, which is used to connect off-chip devices like fly capacitors and load capacitors and resistors. A series of reference signal like REF_TOP, REF, REF_LOW are also generated from PCB.

5.2 Chip Packaging and die photo

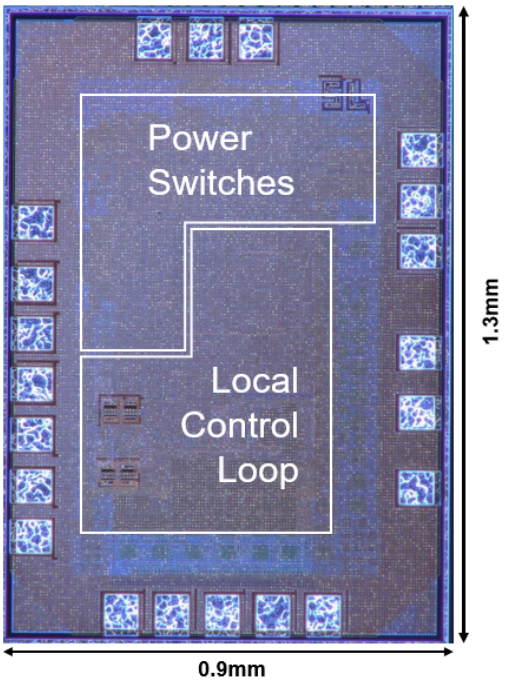


Figure 5.2: chip die photo

Figure 5.2 shows the tape-out layout of my design. This chip will be packaged and wire bonded with DIP24(Dual-in-line) by EI lab tudelft. The chip area is $1.3mm \times 0.9mm$. The number of pads are 21, including 4 power pads, 5 digital pads and 12 analog pads. There are only two input pads which is V_{AC+} and V_{AC-}. The rest of them are observation pads. More packaging information are added in Appendix.

The power receiver are fabricated in a 0.18 μm, The die photo is shown in Figure 5.2.

5.3 PCB Design

The PCB figure is shown in Figure 5.3. Four layers board are used in this design, the top layer and bottom layer are used as signal layer. The middle two layers are used as GND plane, which can help to isolate the different signal layer. The board area is $100mm \times 60mm$. The chip is plugged with DIL 24 socket. The observation pads are all connected with 2-headers. The resistors and capacitors use SMD 0805 packaging. Several vias are placed at the edge of board to reduce the GND path.

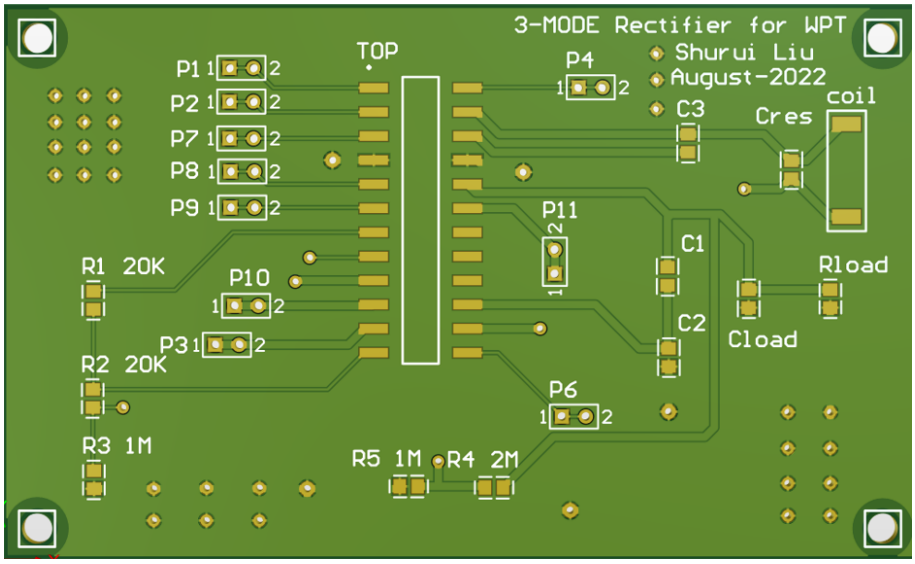


Figure 5.3: PCB photo

5.4 Operational waveform of proposed system

Fig. 5.4 shows the measured waveform of the proposed 3-mode rectifier with local loop control. The rectifier can switch between 1X and 2X mode, 2X and 3X mode, depending on the need of reference voltage. The output voltage can be regulated at 5V. At first, when the input voltage amplitude is larger than 2.5V, the rectifier can switch between 1X and 2X to maintain a stable output, the ripple is only 60mV, then with the decrease of received input AC amplitude, we can see when the duty ratio of $MODE\_1$ signal is becoming larger, the rectifier needs to work with 2X mode for longer time. When the duty ratio of $MODE\_1$ reaches 100%, the mode-switching period needs to change from 1X∼2X mode to 2X∼3X mode. *State* will become '1', V_{REC} changes about 76mV. The input AC signal amplitude also changes, although the VCR becomes higher, the input AC amplitude becomes smaller, that is due to the change of load condition, higher VCR means smaller input impedance of the rectifier, that is why 3X starts with a relatively large duty ratio. Then with the decrease of input signal V_{AC}, the duty ratio of $MODE\_0$ continues to be larger. The ripple of signal when the rectifier switches between 2X and 3X is about 100mV.

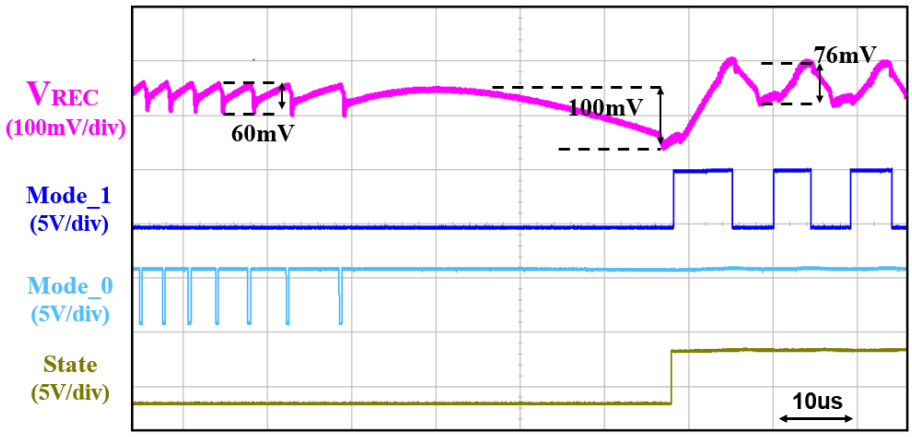
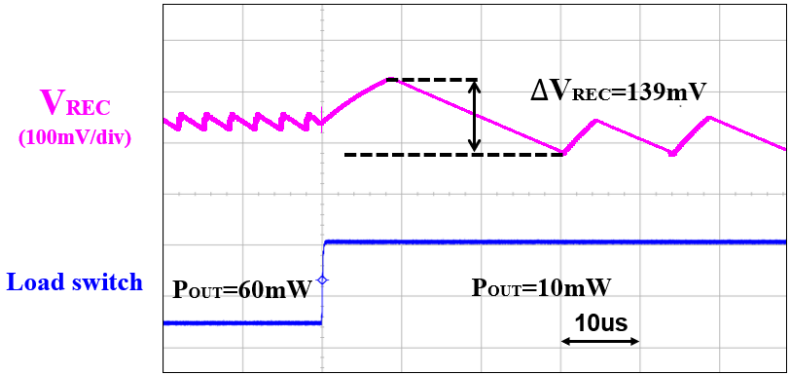
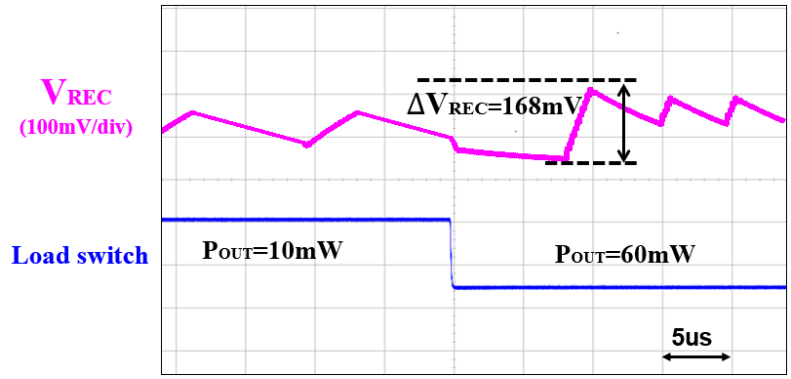


Figure 5.4: Operational waveform of proposed system

5.5 The waveform of load shift



(a)



(b)

Figure 5.5: Load shift transient (a)Heavy load to light load. (b) Light load to heavy load.

Fig. 5.5 show the transient response under load shift. the coil distance is cm. when the output

power changes from heavy load to light load, the output V_{REC} can be regulated at 5V. The figure is shown in Fig. 5.5(a). The overshoot voltage is 139mV. When the output power changes from light load to heavy load, the output V_{REC} can still be regulated at 5V. The coil distance is cm. The figure is shown in Fig. 5.5(b). The undershoot voltage is 168mV.

5.6 Rectifier efficiency vs P_{OUT}

The measured rectifier efficiency for different P_{OUT} ranging from 15mW to 110mW is shown in Figure 5.6. The power consumption of comparators and PWM controller are all included. In the light load, the switching loss of the active switch degrades the receiver efficiency, but the switching loss will not increase a lot with the output power. With the increase of output power, the conduction loss of the power path dominates in the heavy load. At $P_{OUT} = 65mW$, the receiver reaches its maximum efficiency 87.4%. At the coil distance of 0.3cm. The rectifier works with 1X and 2X mode.

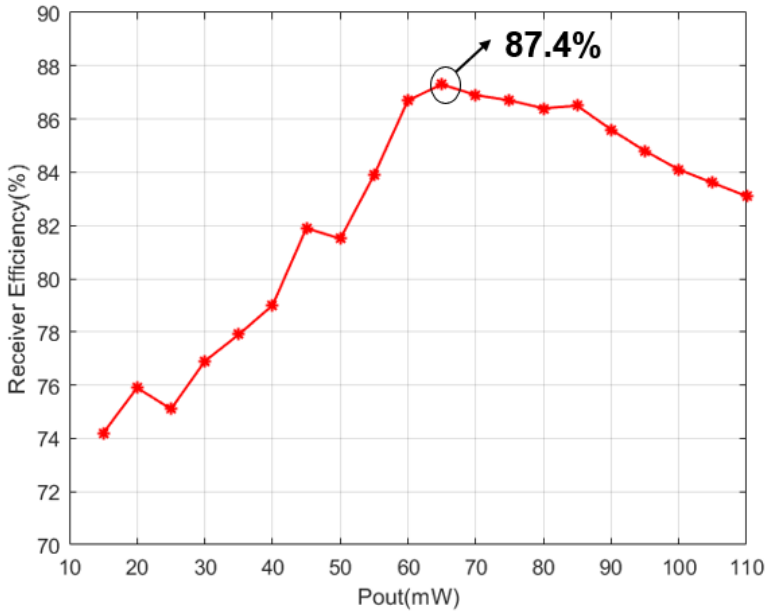


Figure 5.6: Measured receiver efficiency

5.7 Comparison with previous work

Table 4 summarizes a performance comparison with other state of the art designs. The result shows that our design has the smaller chip area, the widest VCRs and satisfied efficiency.

Table 4: PERFORMANCE COMPARISONS

	2013 JSSC[10]	2015 ISSCC[9]	2015 JSSC[21]	2017 JSSC [13]	2021 JSSC[22]	**This work**
Process	0.35 μm	0.13 μm	0.35 μm	0.35 μm	0.25 μm	**0.18 μm**
Resonant frequency	6.78MHz	6.78 MHz	2MHz	6.78 MHz	6.78 MHz	**6.78 MHz**
Rectifier Structure	3R Rectifier	Rectifier +Buck	Rectifier +LDO	3-Mode Rectifier	0X/1X Rectifier	**1X/2X/3X Rectifier**
Chip Area(RX)	5.52mm^2	4.8mm^2	14.44mm^2	4.8mm^2	2.07mm^2	**1.17mm^2**
Off-chip Components	5 diodes, 3 capacitors	1 inductors, 2 capacitors	3 capacitors	1 capacitors	1 capacitors	**4 capacitors**
V_{OUT}	5 V	5 V	3 V	5 V	5 V	**5 V**
Peak receiver efficiency	86%	84.6%	76%	92.2%	92.9%	**87.4%**
VCR	$<$1	2.5	N/A	$<$1	$<$1	**0.95$\sim$2.68**

6 Conclusion

6.1 Summary of Main Contributions

A 6.78Mhz 3-mode operational reconfigurable rectifier for wireless power transfer system is presented. The proposed system can adaptively configure with 1X/2X/3X modes to gain a stable output, which shows the widest VCR range among the state-of-the-art designs. Thus, this system can work in wider input range to get required output voltage with local loop control, which can realize better performance in weak coupling condition. The mode-switching is achieved by detecting the duty ratio of mode signal and the comparison result with reference voltage. Delay compensation technique are applied to reduce the comparator delay caused by large transistor size for higher power efficiency and voltage conversion efficiency.The measured VCR range is 0.95$\sim$2.67. The measured maximum power and receiver efficiency is 120mW and 87.4%, respectively. For the state switching, the maximum ripple is 100mV. The undershoot when the load shifts are under 170mV.

6.2 Future Work

6.2.1 Adaptive delay compensation comparator

In the proposed system, the delay compensated comparator are applied to reduce the comparator delay caused by large gate capacitance and internal delay. The comparator utilize unbalanced biasing structure to offer turn-on delay and turn-off delay for delay compensation. But the unbalanced structure size ratio is fixed, which means the current structure can only offer fixed delay compensation for the comparator. The switch offset current can only be optimized for a particular condition. However, if the current can adaptively change according to the working conditions, the on-delay and off-delay can be well compensated under PVT variation and potential mismatch. A negative feedback loop can be added to the current push-pull comparator structure. In this way, the offset current can be adaptively adjusted depending on the delay condition, the comparator delay can be eliminated under various conditions. The operational principle can be as follows. V_{AC} voltage will be sampled and held by sampling circuit. Then the sampled voltage $V_{AC\_on/off}$ will be compared with ground by feedback amplifier OTA. which generates $V_{ea\_on/off}$ to adjust the value of on-delay offset current and off-delay offset current. Then the turn-on/off delay will be reduced compared with previous cycle and finally eliminated.

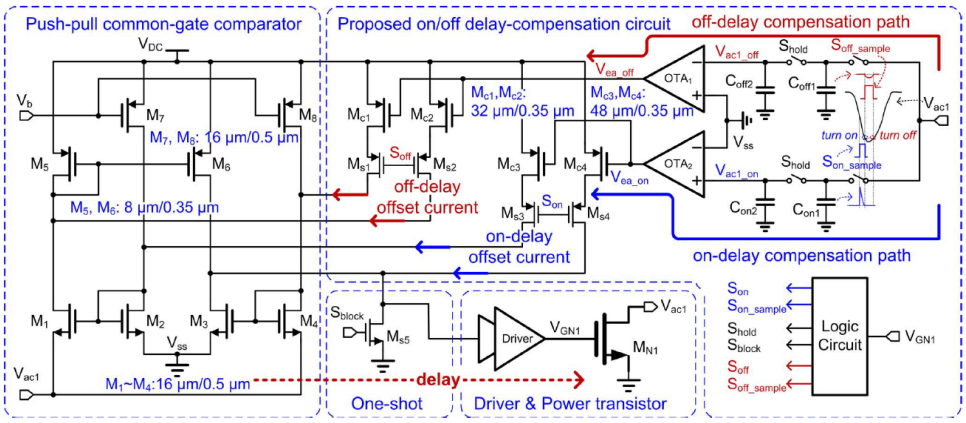


Figure 6.1: Adaptive delay compensation technique

6.2.2 Adaptive sizing of active diodes

The active diodes with their gate switching introduces switching loss driven by their drivers. The larger the transistor size is, the smaller the conduction loss but the larger the switching loss. The optimized transistor size for balancing the conduction loss and switching loss is changing under different load condition and PVT variation. Thus, adaptive sizing can be adopted into rectifier design to optimize the PCE efficiency. When the circuit is in light load, we can choose smaller transistor size to reduce dominated switching loss. When the circuit is in heavy load, conduction loss dominates, then we can switch to larger transistor size to maintain a high power efficiency. Although the change of transistor size might influence the comparator delay, resulting in the limit of size change, the combination of adaptive delay compensation techniques can help to optimized the transistor size without limits.

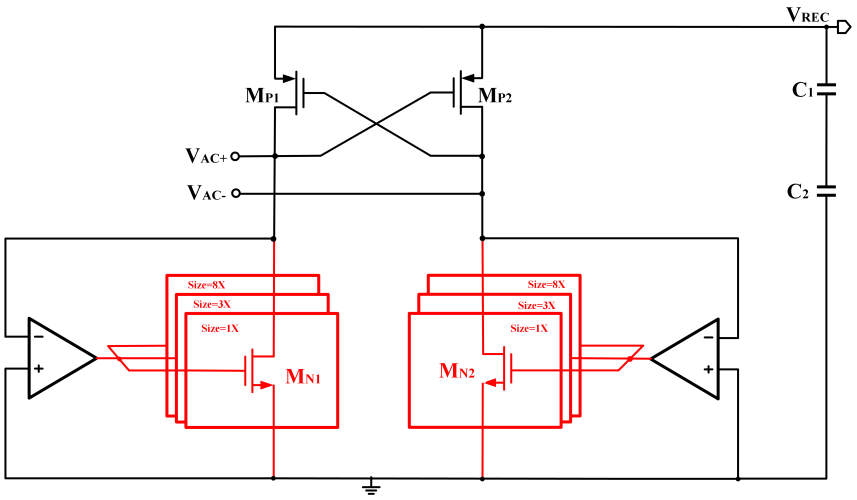


Figure 6.2: Adaptive sizing technique

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8 Publication

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