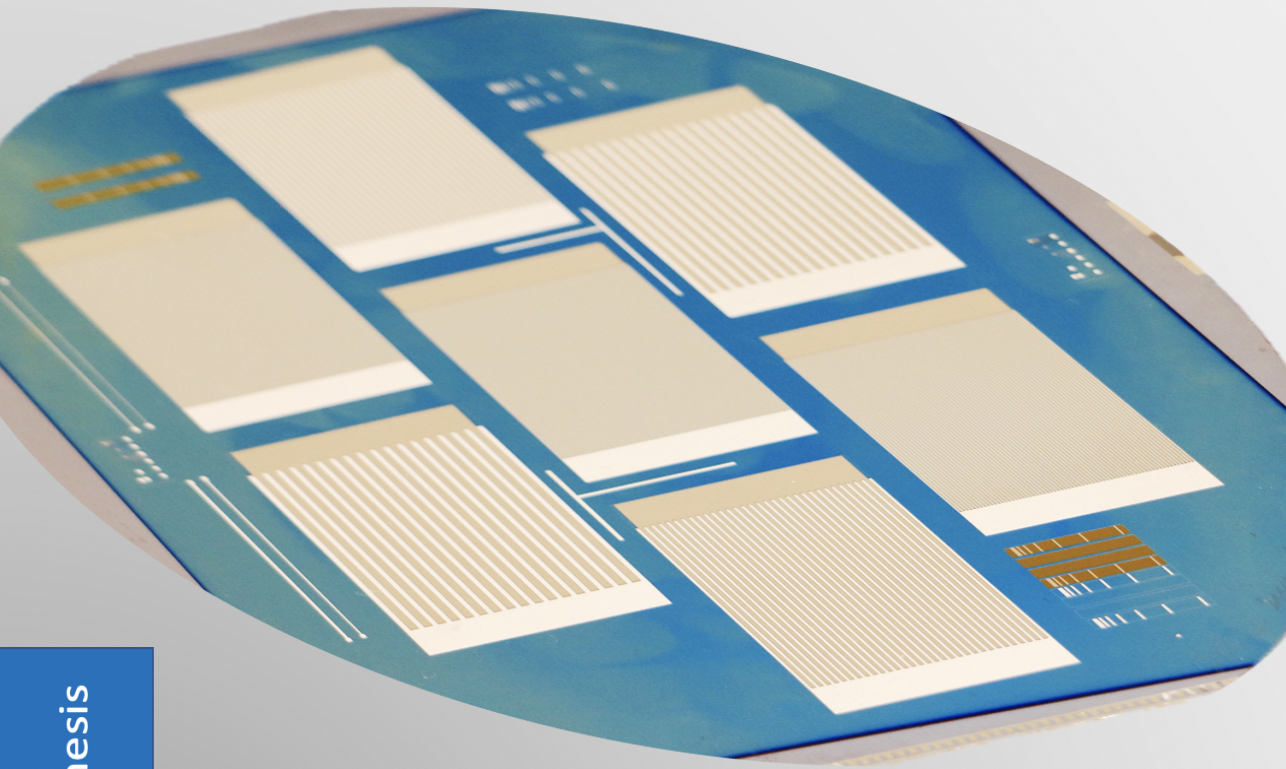
Experimental demonstration of poly-Si/SHJ hybrid tunnel-IBC c-Si cells

Chaofeng Li



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by

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ABSTRACT

Interdigitated back-contacted solar cell (IBC) is a successful high-efficiency solar cell concept. Without a metal grid at the front side, the metal shading loss is eliminated. However, the fabrication process of an IBC cell is much more complicated than that of a FBC cell. Within the PVMD group, two poly-Si carrier-selective passivating contacts (CSPCs) IBC cell fabrication methods were developed, namely Self-aligned and Etch-back method. These two methods require respectively to pattern the IBC rear side twice and three times to define the emitter and BSF area. In this project, a novel poly-Si/SHJ hybrid IBC solar cell design using tunneling recombination junction (TRJ) is proposed, which only requires one pattern step to define the emitter and BSF area, thus, significantly simplifies the flowcharts of IBC cells.

The main objective of this thesis is to demonstrate the novel poly-Si/SHJ hybrid TRJ IBC cell concept by fabricating such high-efficiency hybrid IBC cells. With the proposed hybrid IBC cell design, the BSF layers are deposited on the full rear side after the emitter patterning. Thus, a TRJ is introduced at the emitter ((p^+)poly-Si). The carrier tunneling efficiency across the TRJ layers should be guaranteed. The BSF layers passivation quality is also crucial for hybrid IBC cell performance, and the shunting due to the full area deposited BSF layers should be limited as well.

The TRJ proof-of-concept was firstly demonstrated in FBC cells due to their easier fabrication processes. And different materials combinations of (i)a-Si:H, (n)a-Si:H and (n)nc-Si:H were used to form TRJ with (p^+)poly-SiO_x. Firstly, it was found that the existence of (i)a-Si:H is detrimental to the device performance, especially for the cell FF. Secondly, for cells without (i)a-Si:H layer, the cell performance was improved by replacing (n)a-Si:H with more conductive and low activation energy (n)nc-Si:H layer. At last, the TRJ with dual-n-layer, (p^+)poly-SiO_x/(n)a-Si:H/(n)nc-Si:H, was found to be most promising. And the cell FF decreases with (n)a-Si:H layer thickness. However, instead of only depositing (n)nc-Si:H, the (n)a-Si:H was kept for its better passivation ability than (n)nc-Si:H, as it is directly deposited on the c-Si surface at BSF in hybrid IBC cells.

Then the hybrid design with dual-n-layer was demonstrated and optimized regarding the passivation quality, TRJ efficiency and the R_{shunt} in IBC cells. We firstly demonstrated that poly-Si delivers better performance than poly-SiO_x due to its lower resistivity. With 18 nm(at textured BSF)(n)n-Si:H, the (n)a-Si:H layer thickness optimizes at 3 nm in poly-Si/SHJ hybrid cells. The pitch width was also found to have an influence on cell external parameters as the number of fingers decreases with pitch width. The cell FF increases and the J_{sc} decreases with pitch widening. The best cell obtained in this project has 3/18 nm (n)a-Si:H/(n)nc-Si:H and a medium pitch width (650 µm). It has a V_{oc} of 665 mV, a J_{sc} of 39.36 mA/cm^2, a FF of 74.33% and an efficiency of 19.45%.

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NOMENCLATURE

η	Conversion efficiency
$\Psi_{\mathbf{ph},\lambda}$	Spectral Photon Flow
$\sigma_{\mathbf{d}}$	Dark conductivity
$\tau_{\mathbf{eff}}$	Effective carrier lifetime
a–Si : H	Hydrogenated amorphous silicon
ALD	Atomic layer deposition
ARC	Anti-reflective coating
BSF	Back surface field
CSPCs	Carrier selective passivating contacts
CVD	Chemical vapour deposition
$\mathbf{D_{n,p}}$	Electrons/holes diffusion coefficient
DI water	Deionized water
$\mathbf{E_c}$	The Lowest Energy of Conduction Band
$\mathbf{E_v}$	The Highest Energy of Valence Band
EQE	External Quantum Efficiency
FBC	Front/back contacted cell
FF	Fill factor
FGA	Forming gas annealing
FSF	Front surface field
FZ	Float-Zone
$\mathbf{I_{ph}}$	Photocurrent
IBC	Interdigitated back contacted cell
$\mathbf{iV_{oc}}$	Implied open-circuit voltage
$\mathbf{J_0}$	Saturation current density

J_{sc} Short-Circuit current density

$L_{n,p}$ Electrons/holes diffusion length(μm)

LPCVD Low-pressure chemical vapour deposition

$N_{A,D}$ Acceptor,donor concentration

NAOS Nitric acid oxidation of silicon

nc–Si : H Hydrogenated nanocrystalline silicon

nc–SiO_x : H Hydrogenated Nanocrystalline Silicon Oxide

PCD Photoconductance Decay

PECVD Plasma enhanced chemical vapour deposition

POLO Polycrystalline on oxide

poly–SiO_x Polycrystalline silicon oxide

poly–Si Polycrystalline silicon

PVD Physical vapour deposition

QSSPC Quasi-steady-state photo conductance

R_{series} Series resistance

R_{sheet} Sheet resistance

R_{shunt} Shunt resistance

SHJ Silicon hetero-junction

SRH Shockley-Read-Hall

STC Standard test condition

TCO Transparent conductive oxide

TOPCon Tunnel oxide passivating contacts

TRJ Tunneling recombination junction

V_{oc} Open-circuit voltage

1

INTRODUCTION

Solar energy, an essential source of renewable energy would certainly play a vital role in the future energy supply and solar cells are be the major form of application. In this chapter, poly-Si IBC solar cell will be introduced and then the motivation and research goals as well as the outline of this thesis will be presented.

1.1. Solar energy: the key to the renewable future

With the growth of the world's population and the improvement of people's living standards, human energy consumption will continue to increase. Climate and environmental issues caused by fossil energy consumption are also receiving more attention and many countries have set clear carbon neutral targets[1]. Renewable energy technologies play a key role in solving the contradiction. Among them, solar energy is the most promising option. As it can be seen in Figure 1.1, solar energy has the largest potential comparing to other renewable and finite energy forms[2].

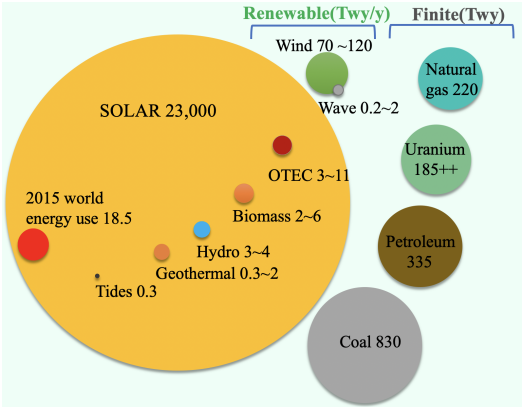

Figure 1.1: Renewable and finite energy sources potential estimate in 2015. Adapted from [2]

In 2018, the annual installation of solar power crossed the threshold of 100GW and a total cumulative capacity over 0.5 TW[3].In 2019, the annual installation increased by 13% and reached 116.9 GW, however, its share of the global power generation was merely 2.6%[4]. It is expected that in 2023, the total cumulative capacity would be more than 1.2 TW[4]. For a long time, the solar energy industry in various countries has developed largely with the support from preferential policies. The development of technology pushed solar electricity generation cost to decrease steeply over the last decade as shown in Figure 1.2 which makes it more competitive in the electricity market[4]. With the support from society as well as its increasing cost-competitiveness, solar energy is the one of keys to the 100% renewable future.

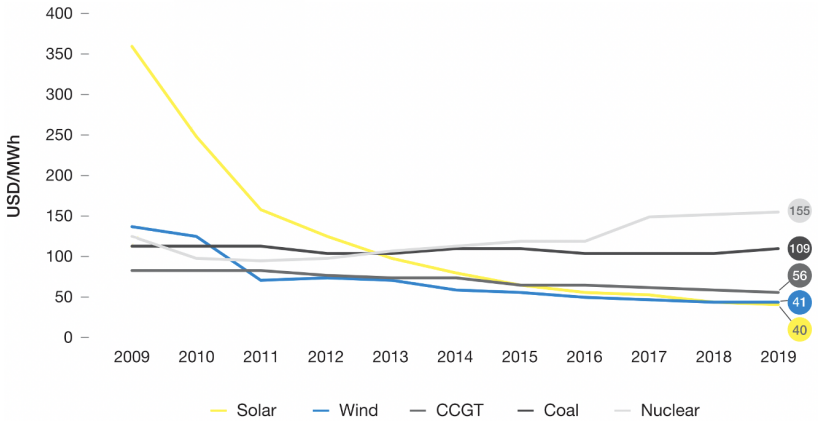

Figure 1.2: Different power sources generation cost comparison[4].

1.2. Interdigitated back contact solar cell

Poly-Si CSPCs (carrier selective passivating contacts) interdigitated back contact (IBC) cell is the IBC cell with tunnel oxide/polysilicon passivating contacts (also called POLO or TOPCon). An efficiency of 26.1% was obtained in 2018 with this concept[5]. In this section, the working principle of a solar cell will be briefly introduced first and then poly-Si CSPCs IBC cells will be discussed.

1.2.1. Solar cell working principle

The working principle of a solar cell is based on the photovoltaic effect. The whole process can be briefly separated into four steps as shown in Figure 1.3. (1) Firstly, Photons are absorbed by the semiconductor material and electron-hole pairs are generated. (2) Secondly, the pairs would recombine which is undesired and will be explained more in detail in section2.1.1. (3) Or the pairs would get separated by n-type and p-type material on different sides of the bulk. Thirdly, the charge carriers are extracted from the cell and flow to the external circuit. This is also the collection step. (4) Only successfully collected carriers can contribute to power generation. (5) At last, the electrons which came

out from one terminal and traveled through the external circuit will recombine at the other terminal with holes.

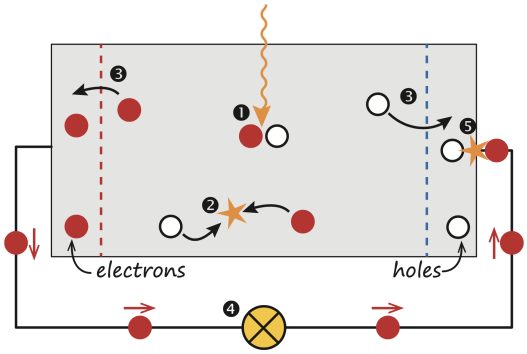

Figure 1.3: Schematic representation of solar cell working principle[6].

1.2.2. Poly-Si FBC and IBC comparison

Figure 1.4 shows a basic poly-poly front/back contacted (FBC) cell and a poly-Si interdigitated back contact cell structure[7]. Generated electrons would flow to the n^+ poly-Si layer and holes to p^+ poly-Si layer. The front side is textured which can increase the amount of light coupled into the bulk[6]. An anti-reflective coating (ARC) layer is deposited on the front surface to further decrease light reflection. The ARC layer thickness is determined based on light interference theory[6]. Layers other than the absorber would cause parasitic absorption losses as they would also absorb light, especially the layers at the front side. Finally the electrons would be collected at the metal electrodes on the n^+ poly-c-Si layer and flow to the external circuit.

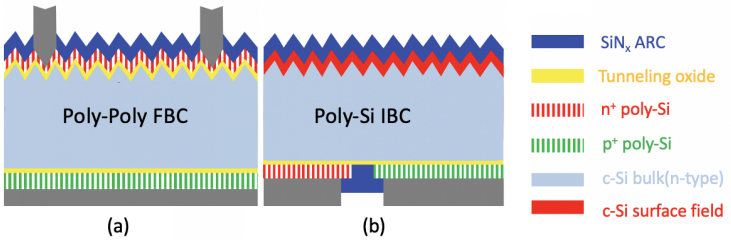

Figure 1.4: Schematic drawing of(a) Poly-Poly FBC cell and (b) Poly-Si IBC cell. Adapted from [7]

The FBC cell has a metal grid on the front side which obviously would introduce shading losses. This is a relatively simple design, and achieved an efficiency of 19.6% within PVMD group[7]. IBC cell is a successful high-efficiency concept and Figure 1.4 (b) shows a Poly-Si IBC structure with an efficiency of 23%[7] thanks to the unshaded illuminated side. A higher current density of 42.2mA/cm^2 was obtained comparing to 38.1mA/cm^2 of the poly-poly FBC cell. Besides, due to the relaxed optical restrictions on the rear side,

larger metal contact coverage for IBC cells can be applied. Thus, the poly-Si IBC has a FF up to 77.8% which is higher than that of the FBC (75.2%). As both electron collector and hole collector are positioned at the rear side, the fabrication process of an IBC solar cell is much more complicated than that of a FBC cell. In this thesis project, cell precursor with p-type poly-Si (and poly-SiO_x) emitter will be used in this thesis project and for back surface field (BSF) materials in silicon heterojunction (SHJ) cells such as n-type amorphous and nanocrystalline silicon will be used, and the cell design is based on the poly-Si CSPCs IBC solar cell shown in Figure 1.4.

1.2.3. Poly-Si CSPCs IBC solar cell fabrication

Combining different process methods such as photolithography, wet etching, chemical vapour deposition and ion-implantation etc., the pattern structure design and process steps of a poly-Si CSPCs IBC cell is of large freedom. Figure 1.5 (a) shows the so called POLO-IBC cell developed by group ISFH with an efficiency of 25%[8]. The rear side poly-Si layer is boron-doped in advance and then a photoresist mask is applied for phosphorous ion-implantation to obtain n-type area (doping compensation). After this, another patterning step with photoresist and KOH ecthing are applied to separate the n^+ and p^+ regions. Figure 1.5 (b) shows another design developed by the same group which enables an efficiency of 26.1%[9][10]. Photolithography with special designed masks and ion-implantation were used to pattern the rear doping layer structure. To protect the undoped region (grey) which separates the n-type doped and p-type doped region, at least two pattern steps are required. With this structure the chemical etching induced degradation is avoided, and the optimized undoped region width is 30 µm to sufficiently reduce lateral cross recombination[10].

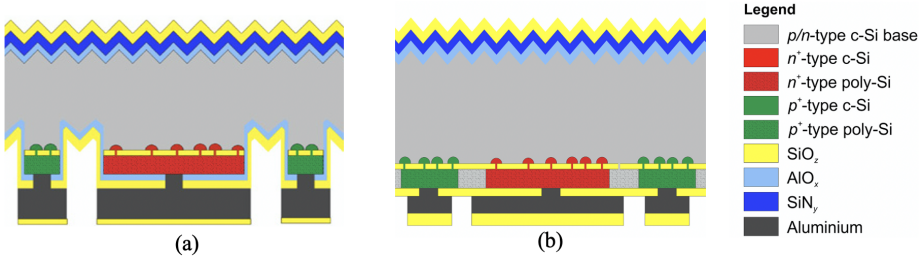

Figure 1.5: Schematic drawing of POLO-IBC cell with (a) etched gaps [8](b)undoped gap regions [9]

PVMD group also gained a lot of experience in fabricating poly-Si CSPCs IBC solar cell. Two approaches are presented in Figure 1.6 and Figure 1.7: Self-aligned and etched-back[11]. For both methods, the ultra-thin tunneling SiO_2 is grown wet-chemically on both sides and then an intrinsic amorphous silicon layer is also deposited on both sides by low-pressure chemical vapour deposition (LPCVD). (a2) For self-aligned method[12], the full rear side intrinsic layer is phosphorous doped using P-implantation (phosphorous implantation) followed by SiN_x deposition. (a3) Then the first pattern step using photoresist and photo lithography is applied to pattern the SiN_x layer which allows to chemically remove the SiN_x and n-type doped layer in the region dedicated for p-type

region. In the meanwhile, alignment markers will also appear on the wafer due to the etching process. (a4) After this etching step, the tunneling SiO_2 growth is repeated followed by an another intrinsic amorphous layer deposition. (a5) Then the layer would be boron-doped using B-implantation (boron implantation) and a SiN_x layer is also deposited. (a6) With the marker on the wafer, another similar photolithography step with opposite opening areas and another similar chemical etching step are applied to pattern the SiN_x layer and etch the SiN_x and undoped amorphous layer. Till this step, as shown in Figure1.6 (a6) at the rear side separated regions with different polarities are formed[12].

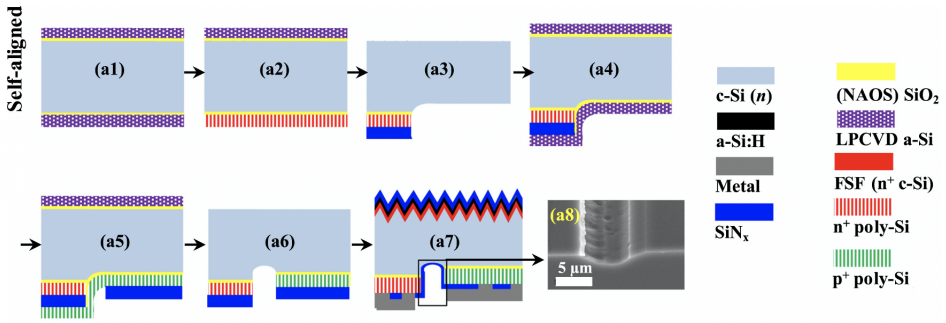

Figure 1.6: Schematic representation of PVMD self-aligned process for IBC solar cells. Adapted from[12].

In etch-back method, as shown in Figure 1.7, (b2) the rear side is implanted twice with two different photomasks to fabricate the n-type (BSF) and p-type (emitter) doped regions separated by an undoped region[11]. (b3) This region will be chemically etched away with another photolithography pattern. So in total three pattern steps are required to pattern the rear side n and p fingers as shown in Figure 1.7(b3). But it is worth noting that with this method less chemical etching steps are required and the initially deposited intrinsic layer by LPCVD on the polished bulk surface is kept. Unlike that in self-aligned method, the boron ion is implanted into the intrinsic layer deposited on a chemically etched surface. For this reason a better passivation quality could be obtained[11]. After the formation of BSF and emitter, for both methods the wafer will undergo other processes steps such as texturing, front surface field implantation ARC layer deposition and metallization to complete the IBC cell (a7,b4)[12][11].

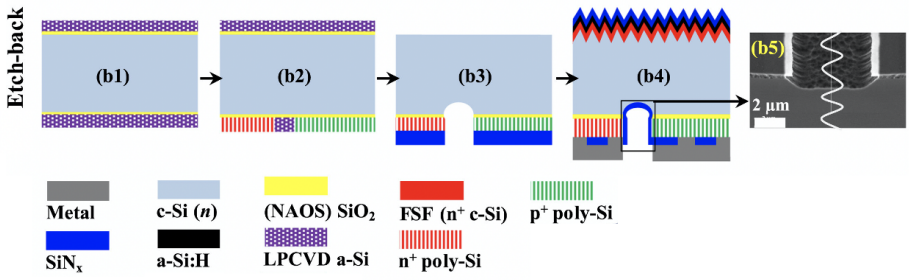

Figure 1.7: Schematic representation of PVMD etch-back process for IBC solar cells[11]. Adapted from [11]

1.3. Motivation and research goals

In this project, a new poly-Si(O_x)/SHJ hybrid IBC cell is proposed. In this section, the motivation, research goals as well as the thesis outline are presented.

1.3.1. Motivation

As discussed in the previous section, at least two steps pattern is required to fabricate the poly-Si IBC cell emitter and BSF. A new hybrid poly-SiO_x/SHJ IBC cell structure is proposed as shown in Figure 1.8. Similar to the self-aligned[12] method introduced in section1.2, part of the poly-Si layer is chemically etched away after patterning SiN_x using photolithography. Then, a full area i/n a-Si:H deposition is applied. In total only one step pattern is required to finish the formation of emitter and BSF. This will significantly simplify the fabrication process. At the emitter, an tunneling recombination junction (TRJ) (P^+)poly-SiO_X/(i)a-Si:H/(n)a-Si:H is formed and it will be discussed in Section 2.5.

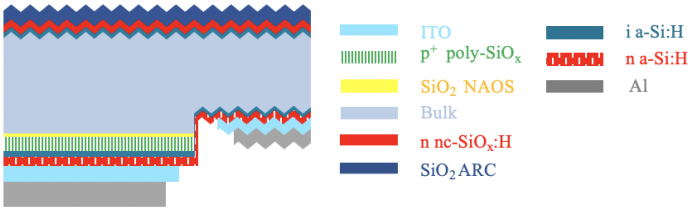

Figure 1.8: Hybrid Poly-SiO_x/SHJ IBC solar cell

1.3.2. Research goals

The band diagram of the proposed IBC cell emitter is shown in Figure 1.9. The band diagram starts from the part of the bulk that is nearest to the p^+poly-SiO_x layer. At the part the bulk would also be boron-doped due to the ion penetration during ion-implantation and high-temperature annealing[12].

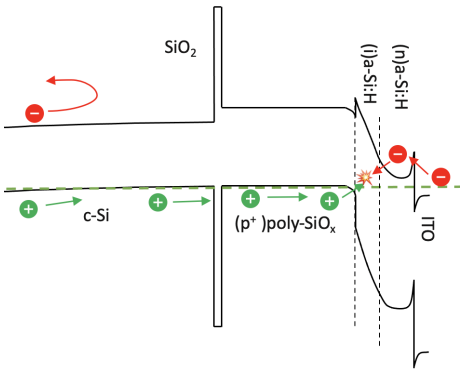

Figure 1.9: Emitter side band diagram

The cell shown in Figure 1.8 can be divided into three parts: the emitter, the BSF and the gap in between.

1. At the emitter side, it can be found that another pn junction is introduced. The device should be working only if the carriers can transport through the junction efficiently. This is tunnel recombination junction(TRJ). The electrons should be able to tunnel through the amorphous layer and recombine with the holes.

2. At the BSF side, in this part the c-Si surface is not passivated by the chemically grown silicon oxide like in the emitter. And the c-Si bulk surface is exposed after emitter pattering. So, the passivation quality at the BSF area should also be guaranteed.

3. At the gap, as the conductive n-type layer connects the emitter and the BSF, the gap is actually a path for shunting, which has to be minimised for high-efficiency device.

Therefore, according to the analysis above, the first main research goal is the emitter TRJ proof-of-concept demonstration. The proof-of-concept would be done in poly-poly FBC solar cells as its fabrication process is much shorter than that of an IBC cell.

- Is the TRJ structure P^+)poly-SiO_X/(i)a-Si:H/(n)a-Si:H shown in Figure 1.8 feasible? And what is the optimal intrinsic layer thickness?

- If it is not working with (i)a-Si:H/(n)a-Si:H, what layers should be deposited?

The second main research goal is the demonstration of hybrid SHJ/Poly-Si IBC solar cell using the optimised TRJ.

- What is the influence of the TRJ layer thickness on passivation and shunt resistance?

- Whats is the influence of the pitch size (total width of an emitter, an BSF and a gap) on IBC cell performance?

1.3.3. Outline

In the first chapter, background, motivation as well as the research goals are given. The second chapter mainly consists of the literature review. In this chapter, the fundamentals about the basic semiconductor physics, material properties as well as the TRJ are discussed. All these would support the experiment design and results analysis. In chapter three, the equipment used for cell fabrication as well as the equipment used for characterization are introduced. In chapter four, the proof-of-concept of the introduced TRJ at the emitter is demonstrated. After having a proved working TRJ, the structure is demonstrated in the proposed hybrid IBC cell. And the layer thickness as well as the pitch size influence is discussed in chapter five. Lastly, in chapter six, the results are summarised and the outlooks are also given for potential further improvement.

2

FUNDAMENTALS

In this chapter, the recombination mechanism is explained first. And then literature about the different materials used in this projects are reviewed. At last the interband tunnel recombination junction is discussed.

2.1. Recombination mechanism and carrier lifetime

When a piece of semiconductor is under illumination, the thermal equilibrium will be disturbed and carrier pairs are generated.The generation process involves the absorption of photons with equal or higher energy than the material bandgap and the excitation of electrons from valence band to the conduction band. In a solar cell, the absorber absorbs the incident photons and generate excess electron-hole pairs. Those electrons and holes should be seperately and effectively collected at different terminals before they recombined. The average time before a minority carrier recombines with a corresponding majority carrier is defined as the carrier lifetime. The content in this part is based on two books respectively written by A. Smets et al.[6] and D.A.Neamen et al.[13].

2.1.1. Recombination mechanism

Opposite of the generation process, the recombination process involves the process that an electron losses its energy and stabilizes back to the valence band. In the meanwhile, heat or light is produced. There are four main recombination mechanisms: Direct recombination, Auger recombination, Shockley-Read-Hall recombination, Surface recombination. In different materials the dominant recombination mechanism differs.

Direct recombination The direct recombination mechanism, also called radiative or band to band recombination, dominates in direct band semiconductor materials such as gallium arsenide. Electrons directly recombine with holes in the conduction band while releasing photons with similar energy to the bandgap as shown in Figure 2.1. The recombination rate is assumed to be proportional to the electrons and holes concentration in conduction band and valence band respectively.

Auger recombination In indirect bandgap materials such as c-Si, Auger recombination is more important which involves three particles. Unlike direct recombination, the released energy and momentum from a recombined electron-hole pair is transferred to another electron or hole. Two process types are possible: electron-electron-hole (eeh) and electron-hole-hole (ehh). Obviously, the recombination rate depends on the charge carrier densities. Figure 2.1 shows the eeh case, in which another electron receives the energy and is pushed higher into the conduction band. Gradually, the energy is released thermally and the electron goes back to the band edge. The higher the doping level is, the higher the Auger recombination rate would be. This makes auger recombination an important limiting factor of silicon-based solar cell efficiency[14].

Shockley-Read-hall recombination Unlike the previous mentioned two mechanisms, Shockley-Read-Hall recombination is trap-assisted. Atom impurities or lattice defects would introduce allowed energy states within the forbidden gap and act as recombination centres. Two kinds of traps are available, donor-type and acceptor-type traps. SRH recombination consists of two steps. Firstly, an electron or a hole is trapped in a such a defect. Secondly, before it is re-emitted back to the conduction band or valence band, it could recombine with a hole or an electron that is also moving to the defect. The energy released is transferred to the lattice and dissipated in the form of heat.

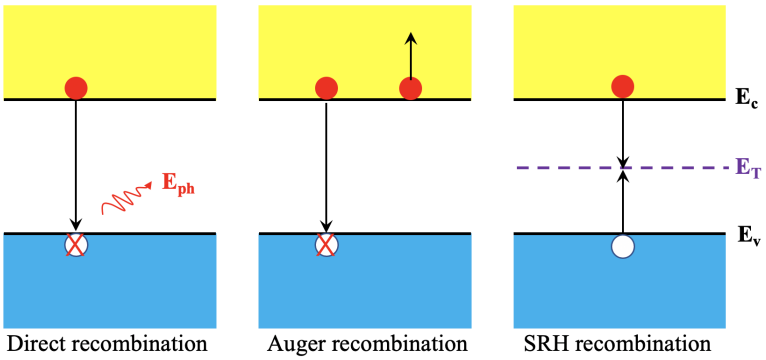

Figure 2.1: Schematic representation of Direct recombination, Auger recombination (eeh), SRH recombination mechanisms schematics. Adapted from[6]

Surface recombination Above mentioned three mechanisms are all bulk recombination mechanisms. In semiconductors with high purity, the surface recombination will dominate. On the bulk surface of a c-Si-based solar cell, due to the disruption of the crystal lattice, there are many silicon atoms that can not form four bonds with adjacent atoms. This results in the formation of dangling bonds which are considered as surface defects and would also introduce trap states within the forbidden gap as shown in Figure 2.2. Those defects would act as SRH recombination centers and degrade the cell performance. Three parties are required for surface recombination: a minority carrier, a majority carrier and a surface defect. Thus, it is possible to suppress the surface recombi-

nation by reducing the defects density or decreasing the minority carrier concentration. These two methods correspond to the so-called chemical passivation and field-effect passivation which will be discussed in specific cases in the following sections.

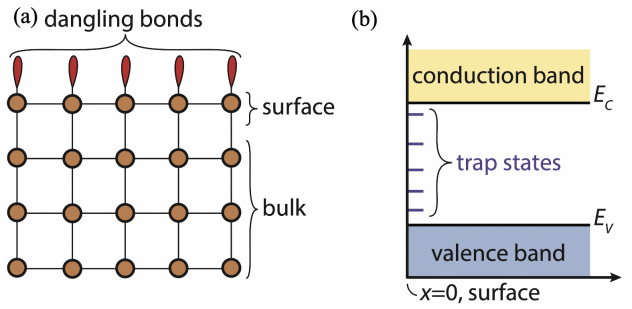

Figure 2.2: (a) Surface dangling bonds (b) Surface defects induced trap states. Adapted from [6]

2.1.2. Minority carrier lifetime

Minority carrier lifetime that relates to the electrons and holes recombination rate, is an important parameter of photovoltaic semiconductor materials The ability to accurately obtain this parameter is of great significance to the design and manufacture of semiconductor devices. For solar cells, carrier lifetime in cell precursors is an important parameter used to predict the cell open-circuit voltage. A long enough minority carrier lifetime is important for obtaining high-efficiency solar cell.

The overall carrier lifetime is related to the lifetime determined by each of the recombination processes, and can be expressed as follow:

$$\frac{1}{\tau_{tot}} = \frac{1}{\tau_1} + \frac{1}{\tau_2} + \frac{1}{\tau_3} + ... \tag{2.1}$$

Considering the recombination mechanism discussed above, the equation becomes:

$$\frac{1}{\tau_{tot}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{aug}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_s} \tag{2.2}$$

The bulk recombination rate is very low for a Float-Zone (FZ) c-Si wafer comparing to the surface recombination, and the lifetime is determined by the carrier lifetime determined by surface recombination which is the lowest.

Minority carrier diffusion length is the distance that a minority carrier travels before recombination and is related to the charge carrier collection probability. The probability describes the chance of a charge carrier generated under illumination to be collected by the P-N junction. The diffuse length is determined by carrier lifetime and diffusing coefficient D_n and D_p.

$$L_n = \sqrt{D_n \tau_n} \quad \text{in p-type semiconductor} \tag{2.3}$$

$$L_p = \sqrt{D_p \tau_p} \quad \text{in n-type semiconductor} \tag{2.4}$$

With diffusion length, the saturation current density also known as dark current density can be calculated by the equation:

$$J_o = q n_i^2 \left(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D} \right) \tag{2.5}$$

N_A and N_D are the doping concentration. J_0 is closely related to the diffusion length and thus related to carrier lifetime. With saturation current density, the open circuit voltage can be estimated by the following equation:

$$V_{oc} = \frac{K_B T}{q} ln(\frac{J_{ph}}{J_o} + 1) \tag{2.6}$$

K_B is Boltzmann constant and T is temperature. According to equation 2.6, to have a high V_{oc}, it is necessary to have a low J_0. Therefor, for a solar cell, it is important to have a low recombination rate and a high carrier lifetime.

2.2. Poly-Si/tunnel oxide CSPCs

Poly-Si passivating contacts can provide excellent surface passivation quality, and as mentioned above, poly-Si passivating contacts IBC cell has reached an efficiency up to 26%[5]. To obtain a high-performance silicon solar cell, it is necessary to to have an excellent surface passivation quality that minimises the recombination losses. The tunnel oxide layer introduces surface passivation and the hydrogenation process further improves the chemical passivation quality. The field passivation effect is introduced by the heavily doped poly-Si layer. To ensure the surface passivation quality, it is vital to optimize multiple parameters during the process such as annealing temperature, oxide layer thickness, process method doping level and doping profile etc.

2.2.1. Carrier transport through the oxide layer

In SiO_2/Poly-Si passivating contact, carriers need to travel through the oxide layer. At the bulk interface, ultrathin thin (around 1.5nm[15]) silicon oxide layer introduces chemical passivation and forms a tunnel junction. The transport mechanism is quantum tunneling and the tunneling probability is described by (Wentzel-Kramers-Brillouin)WKB approximation[16]. Here, the barrier height, the carriers energy, and the free and occupied states on both side of the barrier are vital parameters that have significant impacts on the tunnel transport efficiency [17]. Among them, thickness has an exponential effect on carrier tunneling possibility. It would be harder for carriers to tunnel through with a thicker layer, but a too-thin layer will not ensure good passivation quality. It was found that for poly-Si CSPCs IBC cells the efficiency drops sharply at thickness higher than 1.6nm[17].

In fact, the transport through the oxide layer is not straight forward. Besides tunneling, it could also be transported via pinholes [18][19], or the combination of both[20]. The pinholes can be formed by the thermal process of the poly-Si junction[18], and it

was verified by selective etching which could magnifier the pinholes in the oxide using 15% tetramethylammonium hydroxide (TMAH) solution at 80°C[21]. It is found that the major part of current would localize at the points where the oxide layer is thinner than its surroundings and thus the carrier transport by pinholes can be depicted by Figure [20]. And the current through pinholes becomes more dominant when the oxide layer is thicker as the tunneling is less efficient[20]. With high pinhole densities, the recombination losses increase which is dominated by the recombination in pinholes[20]. A higher implied open-circuit voltage can be obtained when the oxide layer has a high intact integrity and increasing annealing temperature would decrease oxide integrity[22].

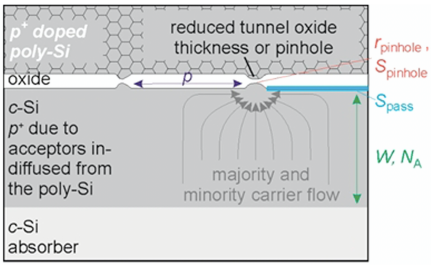

Figure 2.3: Schematic representation of pinholes in poly-Si/c-Si junction[20]

2.2.2. Chemical passivation effect

Chemical passivation improves the device performance by reducing the interface defect density. In SiO_2/Poly-Si stack the chemical passivation comes from the oxygen in the oxide layer and hydrogen from the hydrogenation step by applying a capping layer or forming gas annealing.

Chemical passivation by SiO_2 Figure2.4 (a) shows the comparison of different materials' passivation quality as a function of fix-charge density[23]. Thermally grown SiO_2 shows high chemical passivation ability and a moderate-field effect passivation ability. Silicon oxide passivates the surface by saturating the dangling bonds with silicon-oxygen bond. Further chemical passivation can be achieved by hydrogenation with the application of capping layers such as Al_2O_3 and SiN_x[24][25] or by forming gas annealing. Hydrogenation passivates the surface defects by hydrogen diffused to the interface and saturates defects with hydrogen as shown in Figure 2.4 (b).

The oxide layer can be grown by several methods: thermal oxidation, NAOS (nitric acid oxidation of Si)[26], or ozone based techniques DIO_3 (wet-chemical oxidation) and UV/O_3 (photo oxidation)[27].Thermal oxidation is widely used in semiconductor device industry but it is hard to obtain a good thickness uniformity and has a large leakage current density[26]. Another method, the NAOS method is an effective way to form an ultrathin silicon oxide layer on Si layer with low leakage current density[26]. With this method, the wafers are cleaned and native oxide is etched first and then immerged in 68wt%HNO_3 aqueous solution. A uniform oxide layer can be obtained which gives a uniform electri-

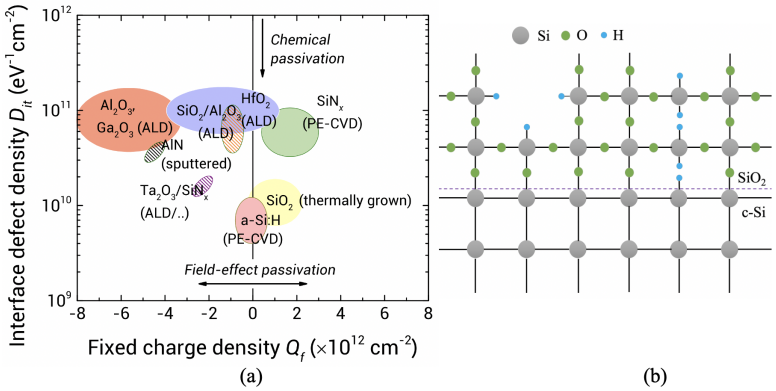

Figure 2.4: (a)Different materials passivation comparison[23] (b) SiO_2 chemical passivation at c-Si bulk surface

cal field at the interface[26]. The oxide layer can also be formed by ozone-based methods: using DIO_3 or UV/O_3[28][27]. With DIO_3 method, the wafers are first immersed in ozonized DI-water with a constant ozone concentration and temperature[27]. The oxide layer could also be dry grown with UV/O_3 with which the SiO_2 is grown by photon-oxidation with a UV excimer[28]. With different methods, the oxide density, thickness uniformity, defect density and thermal stability may vary[26][27][29].

After the growth of SiO_2, doped amorphous Si layer is deposited on the oxide surface followed by an annealing step. Annealing at certain temperature allows the crystallization of the amorphous layer, dopant activation and diffusion. The annealing temperature has a major influence on the passivation quality. It is clearly shown in Figure 2.5 that with the tunnel oxide layer, the temperature optimizes at a certain value (850°C).

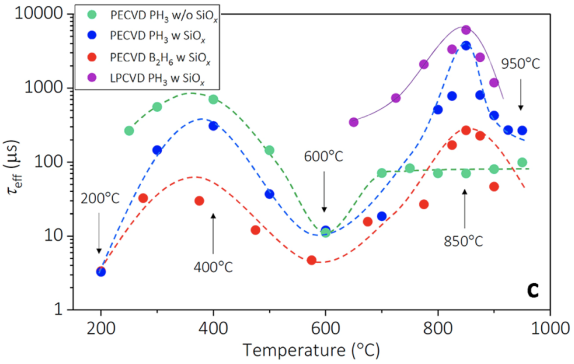

Figure 2.5: Annealing temperature influence on NAOS/poly-Si passivation contacts passivation quality[30]

However, the passivation decreases rapidly if the annealing temperature exceeds the temperature (850°C) as shown in Figure 2.5[30]. A related simulation was also conducted

and the result showed that when poly – Si/SiO_x layer is annealed at temperature higher than 850°C, the current by pinholes would dominate, and when the annealing temperature is around 850°Cthe carrier transport is dominated by tunneling mechanism[30]. This could be explained as excessive high temperature process causes the breakup or balling-up of the thin oxide layer. SiO_2 reacts with Si and produces gaseous SiO[31]. At the break-up region the oxide layer is non-continuous and large pinhole density with big size is expected[32]. Those phenomena would lead to the direct contact of c-Si bulk and the defect-rich doped poly silicon layer which would significantly reduce the passivation quality[32].

Hydrogenation To further enhance the passivation quality, the hydrogenation process is necessary. This can be done by apply capping layers which are hydrogen-rich such as Al_2O_3[24], SiN_x[25][33] followed by annealing in forming gas. When SiNx is applied to the front surface or the rear surface of a bifacial solar cell, the SiN_x layer can also serve as an ARC layer[33]. Van de loo et al[25]. applied an Al_2O_3 layer by ALD (Atomic layer deposition) and analyzed the H concentration with secondary ion-mass spectrometry measurements. Figure 2.6(a) shows the measured results.

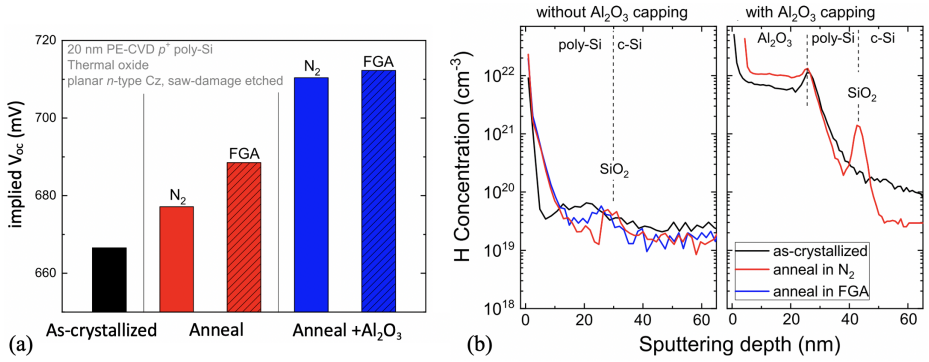

Figure 2.6: (a)Passivation quality (iVoc) and (b)hydrogen concentration distribution comparison between samples with or without Al_2O_3 capping layer[25]

As shown in Figure 2.6, with Al_2O_3 capping the H concentration increases largely and a peak is observed at the SiO_2/c-Si interface. This could explain the large improvement (32mv gain) of the iVoc by applying Al_2O_3 cap as shown in Figure 2.6(b). Not only the hydrogenation step can reduce the defect density at the interface, but also can passivate the defects within the material bulk as it can be seen in Figure 2.6(b) the hydrogen concentration in the poly-Si layer is also increased with a capping layer[25]. When amorphous silicon crystallize to polysilicon after annealing, dangling bonds are formed at the crystal grain boundary due to discontinuity and they can be passivated by the hydrogenation process. Therefore, it is vital to have hydrogenation step for high-performance poly-Si CSPCs solar cell.

2.2.3. Field-effect passivation

Field-effect passivation passivates the surface by introducing an internal electrical field at the interface and suppresse the minority carrier concentration there. This could be achieved by increasing the doping level and improving the doping profile, which results in enhanced bending at the interface. Heavily phosphorous doped poly-Si layer shifts the Fermi level as shown in Figure 2.7. Holes at the interface would be repelled. The SRH recombination requires three parties: majority carrier, defect states and minority carrier. Thus, the recombination rate is decreased at the interface and in the defective poly-Si layer[34].

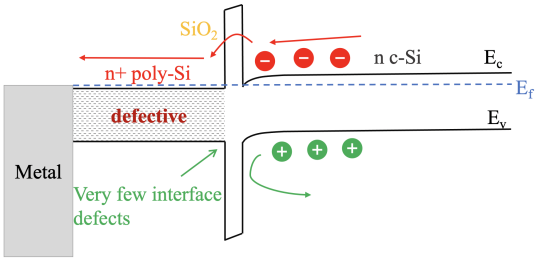

Figure 2.7: Band diagram of c-Si/SiO_2/(n^+)poly-Si. Adapted from [34]

As the Fermi level is affected by the dopant concentration, the doping level also has an influence on the field-effect passivation. Generally, it is beneficial to heavily dope the poly-Si layer which introduces a larger Fermi level shift and results in a stronger internal electrical field. But it should be pointed out that if the dopants diffuse into the bulk the field-effect passivation would be weakened. The oxide layer could block the dopant diffusion to the bulk to a certain extent. But still, some dopants could succeed diffusing to the c-Si layer during annealing[12]. To obtain a good field passivation quality, as shown in Figure 2.8, it is necessary to confine most of the dopants within the poly layer and have a sharp decrease at the interface with shallow diffusion to the bulk[12][35].

2.3. Hydrogenated amorphous silicon

Amorphous silicon as a semiconductor material has been studied for more than a half century. It was already found in 1978 that hydrogenated amorphous silicon could provide remarkable passivation quality on crystalline silicon surface[36]. The turning point of its application in solar cells could be marked by the introduction of an ultrathin intrinsic hydrogenated amorphous silicon layer between the doped hydrogenated amorphous silicon layer and the crystalline silicon bulk. In 1992, Sanyo introduced this concept and fabricated solar cells with an efficiency of 18.1% at low process temperature (<200°C)[37]. With further improvement, an efficiency of 20.1% was obtained in 2000 on an area larger than 100cm^2 in fron/back contacted cells[38]. The concept can also be applied in interdigitated back contacted cell and a high conversion efficiency of 26.6% was reported in 2017 by KANEKA corporation[39].

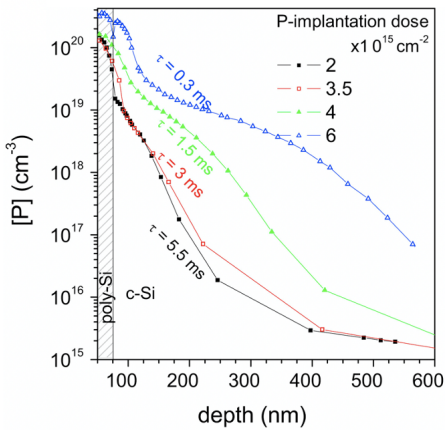

Figure 2.8: Doping profile influence on carrier lifetime in P-implanted poly-Si CSPCs [12]

2.3.1. Atomic structure and energy states

In crystalline silicon, one silicon atom is bonded to four adjacent silicon atoms with tetrahedral structure[6]. A well ordered lattice means less defects in the bulk. However it is different in hydrogenated amorphous silicon.

Atomic structure Pure amorphous silicon, the material itself is defect rich. The defect density is higher than 10^{19}cm^{-3}[40]. The defects inside a-Si come from the disorder of the amorphous lattice, which results in numerous unsaturated dangling bonds. Amorphous silicon (a-Si) and hydrogenated amorphous silicon (a-Si:H) can be deposited using plasma enhanced chemical vapor deposition (PECVD). By adding certain hydrogen dilution during deposition, a-Si:H can be obtained, and the defect density could be largely reduced to around $10^{16}/\text{cm}^3$[6]. In a-Si:H, the atoms still tend to keep the tetrahedral structure, however the Si-Si bands are stretched or compressed as illustrated in Figure 2.9(a)[41].

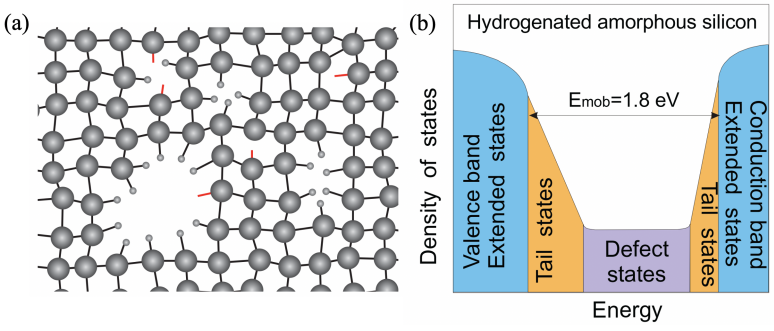

Figure 2.9: (a)a-Si:H atomic structure illustration (b)energy states distribution of a-Si:H [41]

When the strain in the atomic net is too high, the bond would break. In this case, not

all Si atoms can form four bonds with adjacent atoms and leave unsaturated dangling Si bonds[42]. The defective dangling bonds within the material act as the recombination centers. With hydrogen added during the deposition, those defects can be largely passivated by forming Si-H bonds. The defect density in the film varies with the hydrogen dilution during deposition. It was found that when monohydrides have the largest concentration the defect density has the lowest value and the film has the best quality[43].

Energy states The distorted silicon-silicon bond lengths and angles would affect the atomic structure and lead to tails states in conduction and valence band[41]. Unlike c-Si, the edges of the conduction band and the valence band are not sharply defined due to the amorphous atomic structure. The tail states and defect states within the extended states are called the localized states. The states in the extended states are called delocalized states as the charge carrier has higher mobility in such states. Similar to the definition of bandgap in c-Si, the energy barrier between the delocalized states in the different two sides as shown in Figure2.9(b)is defined as the mobility gap E_{mob} which is around 1.8eV[41].

2.3.2. Intrinsic/doped a-Si:H contact passivation mechanism

Intrinsic and doped hydrogenated amorphous silicon stack is widely used in heterojunction solar cells. This is owing to its excellent surface passivation quality on c-Si surface, thus enabling a high V_{oc} value. The passivation mechanism can also be explained by two aspects: chemical passivation and field-effect passivation.

Chemical passivation At the c-Si/a-Si:H interface, the dangling bonds on the c-Si surface could be passivated by forming Si-Si bond with the Si atoms from the a-Si:H layer during deposition. However, as mentioned above, not like in c-Si, the atomic structure is disordered in a-Si:H. This results in that some dangling bond cannot have a suitable Si atom from the growing layer side to form silicon-silicon. The left dangling bonds could be further passivated by hydrogen atoms added during the deposition, which would penetrate the growing film and reach the c-Si surface to passivate the c-Si surface defects. This leads to further surface defect density reduction as shown in Figure2.10[42].

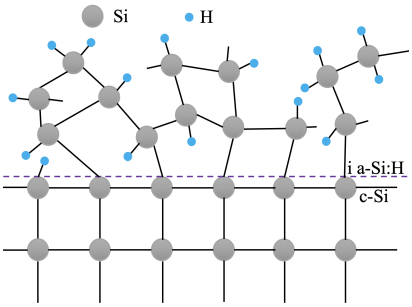

Figure 2.10: c-Si surface chemical passivation by (i)a-Si:H

It is also proved that by adding hydrogen plasma treatments during deposition the passivation quality increases even though this process will make the a-Si:H bulk atomic structure more disordered[44]. The hydrogen dilution optimizes at a certain value and a too-high dilution leads to epitaxial growth which is defect-rich[43]. The condition of the substrate also has an influence on the passivation quality. It is necessary to keep it contamination-free which can be achieved by hydrofluoric acid etching[45] after cleaning with nitrid acid (oxidation). Low temperature post annealing is also beneficial for the passivation quality if there is no epitaxial growth of c-Si at the initial deposition stage, which means an abrupt transition from c-Si to a-Si:H[46]. The passivation enhancement by low-temperature annealing can be explained by the increased amount of monohydride at the c-Si/a-Si:H interface detected by using Fourier transform infrared (FTIR) spectrometry[47]. The monohydrides come from the dihydride or higher hydride-state at the growing surface of a-Si:H, which are restructured and form bonds with the c-Si surface[47][48]. Thus, the surface defect density is further reduced and post-annealing passivation gain can be obtained.

Field effect passivation Similar to the case in poly-Si passivating contacts, the doped layer introduces band bending at the interface. And the formed internal electrical field could reduce the minority carrier density. This field effect is clearly shown in Figure 2.11. The electrons flowing to the p+ a-Si:H/c-Si side and the holes flowing to the n+ a-Si:H/c-Si are repelled back to the c-Si bulk[49].

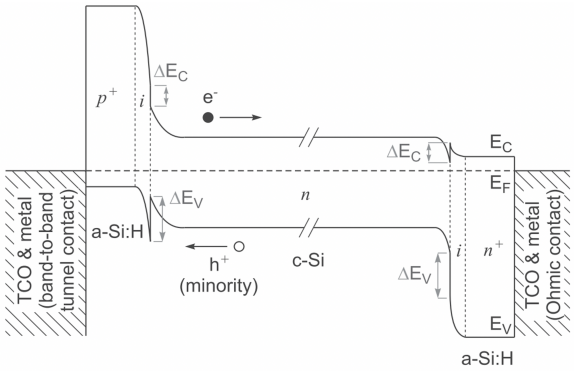

Figure 2.11: Band diagram of an amorphous silicon heterojunction solar cell [49]

Another feature that can be easily noticed from Figure 2.11 is the unsymmetrical band offset which is due to the band gap difference of c-Si and a-Si:H [50]. The offset increases largely the barrier height for electrons at the p-side and holes at the n-side to transport over the barrier and reach the contacts. The carriers can only pass through the doped layer by tunneling or thermionic emission[15]. Therefore, the band offset reduces the recombination rate at the interface. Therefore, the revers saturation current density is decreased and the V_{oc} is increased[42]. This could also be interpreted as the defects are shielded from the electrons or holes at the interface with p-type layer and n-type layer respectively.

2.3.3. Passivation by doped a-Si:H directly

Doped a-Si:H layer can also be deposited directly to passivate the c-Si surface, but this gain in passivation quality is much lower than that with an (i)a-Si:H as the buffer layer. This is due to the lack of sufficient surface chemical passivation. The defect density at the c-Si surface was found to be more than an order of magnitude higher than the case with 10nm (i)a-Si:H buffer layer, and this passivation loss cannot be fully compensated by tuning doping concentration[51]. Logically, in order to get high open-circuit voltage, it is better to have the Fermi level in the doped layer as close to the conduction/valence band as possible. This could be done by increasing the doping concentration. Therefore, larger band bending and better field effect passivation are expected. However, it was found that enhancing doping to high levels leads to an increase of bulk defect density in both n and p-type layer[52][53] and in the n-type a-Si:H layer the defect density is proportional to the square root of the doping level[52].

When doped a-Si:H layer is deposited directly on the c-Si bulk, τ_{eff} and V_{oc} are much lower than that with (i)a-Si:H as buffer layer due to insufficient chemical passivation. This would set limit to the cell's V_{oc} and efficiency. A heterojunction solar cell with the structure (p)a-Si:H/c-Si/(n)a-Si:H reached an iV_{oc} of 631mV and an efficiency of 17.6% in 2006[54], Which is much lower than that with an intrinsic a-Si:H buffer layer fabricated by Sanyo in 2005 (efficiency:21.5%, V_{oc}: 712mV)[55]. It is worth noting that a fill factor of 74.3% was obtained without (i)a-Si:H. Even though the cell performance is worse than that with an intrinsic buffer layer, but it is possible to be further improved by controlling the deposition condition[54].

2.4. Hydrogenated nonocrystalline silicon

Hydrogenated nanocrystalline silicon (nc-Si:H), also referred as hydrogenated microcrystalline silicon shows good electrical and optical properties in SHJ cells[56].This material can also be deposited by using PECVD but with a higher hydrogen dilution comparing to a-Si:H deposition[57]. By adding oxygen to nc-Si:H deposition, nc-SiOx:H can be obtained which is optelectrical tunnable[58]. In this section, the growth mechanism of nc-Si:H and its electrical and optical properties will be introduced.

2.4.1. Growth mechanism

The atomic structure of nc-Si:H is similar to that of a-Si:H, which lacks long range ordering. In nc-Si:H the ordered crystalline phase in the grain or nanocrystals are embedded in an disorder amorphous phase[59]. Thus, like that of the a-Si:H, nc-Si:H would also contain dangling-bonds within the material, especially at the grain boundaries or the amorphous phase. These defects could be passivated by adding hydrogen during the film deposition[60]. Different from a-Si:H, nc-Si:H has a bandgap of around 1.12eV which is close to that of c-Si[6]. The deposition of nc-Si:H on i a-Si:H substrate experiences an evolution from completely amorphous structure to a highly crystalline structure as shown in Figure 2.12[61].

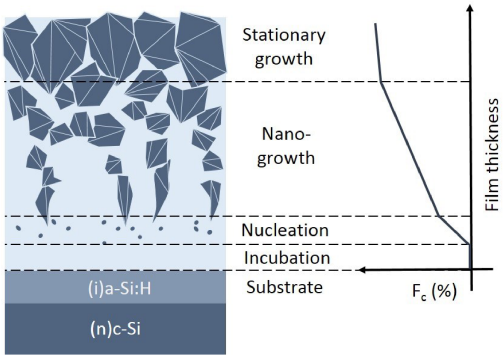

Figure 2.12: Schematic representation of nanocrystalline silicon growth [61]

Briefly, the growth starts with an amorphous layer and then the nucleation starts after which the deposited layer becomes more and more crystallized[61].This evolution is affected by several important factors: deposition parameters, substrate selectivity, film thickness. The fully amorphous layer, which is critical for the entire film properties, is called the incubation layer and highly depends on the hydrogen dilution and substrate material. As it is fully amorphous, the doping efficiency is low and results in a lower carrier mobility[61]. The incubation layer thickness could be reduced by adding CO_2 plasma treatment[62] to the substrate surface or increasing H_2 dilution ratio of the deposition gas flow[61].

2.4.2. Electrical and optical properties

As mentioned above, nc-Si:H has a structure of nanocrystals embedded in an amorphous matrix and has a much higher crystallinity than a-Si:H. The dark conductivity of nc-Si:H is a few orders higher than that of a-Si:H[63]. By increasing the thickness of the nc-Si:H film, the crystallinity would increase and therefore a higher dark conductivity can be obtained[61][64]. Different doping type also has an influence on the conductivity. For both a-Si:H and nc-Si:H, n-type doped films have higher conductivity than p-type doped films. This is because that the formed B-H-Si complex is electrically inactive[65]. Nc-Si:H also shows a higher doping efficiency than a-Si:H as the dopants is preferentially located in the embedded crystals[61]. By adding pre-HPT, corresponding doped nc-Si:H seed, VHF (i) nc-Si:H buffer layer, post-HPT or the combination of some of those treatments allows to further increase the dark conductivity and reduce the activation energy[58].With higher material conductivity and lower contact resistance, in some literature, SHJ solar cells fabricated with doped nc-Si:H films has a higher FF comparing to doped a-Si:H[62]. Besides the better electrical properties, nc-Si:H, especially nc-SiO_x:H also has a better optical property with a lower absorption coefficient as shown in Figure2.13[61].

By adding oxygen in the material, both the electrical and optical properties would vary as shown in Figure 2.14 [66]. For both n-type and p-type nc-Si:H, the refractive index n de-

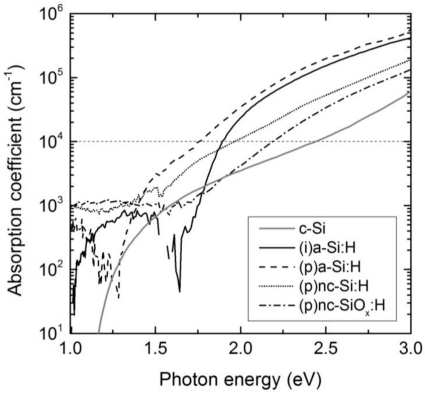

Figure 2.13: Absorption coefficient as function of photon energy for different Si material[61]

creases and the absorption coefficient also decreases with adding oxygen alloy. However, the conductivity also decreases which can be explained by the decreased crystallinity or the decreased doping efficiency[61]. For the comparable refractive index, n-type film has a higher conductivity and for the similar conductivity n-type film has a lower refractive index, which makes phosphorous doped nc-SiO$_x$:H a better choice in the trade-off between electrical and optical properties[66].

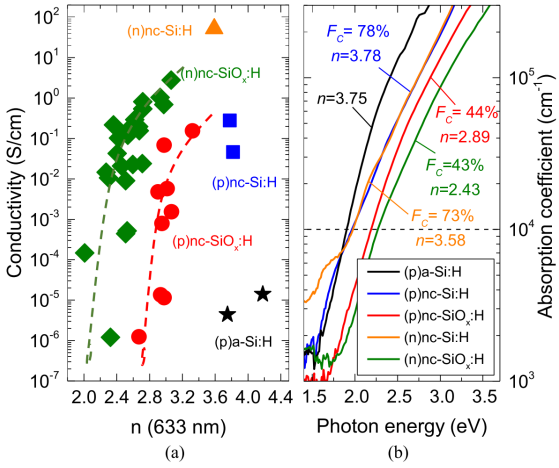

Figure 2.14: Nanocrystalline material (a)conductivity as a function of refractive index (b)absorption coefficient as function of photon energy [66]

2.5. Interband tunneling recombination junction

Multi-junction or tandem solar cell is a high conversion efficiency concept[67][68][69] and tunnel junctions are usually embedded between adjacent sub-cells. It is essential to have efficient tunneling junctions between the absorbers to avoid large voltage drop due to reverse-biased junctions . Figure 2.15 shows the band diagram of a a III-V triple-junction cell[6]. The junction is very thin with a narrow depletion region and this results in a steep the slope of the conduction band valence band. As shown in Figure 2.15, such steep slope allows the the electrons (red) to tunnel through the small barrier and reach the p-layer side where they recombine with the holes (white).[6]. It is also called tunneling recombination junction (TRJ) and the current density of the whole cell is limited by the recombination current[6].

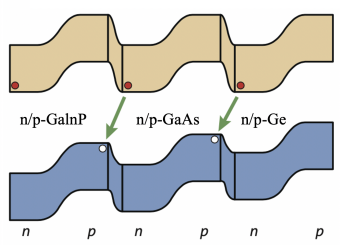

Figure 2.15: Band diagram of a III-V triple junction cell[6]

Figure 2.16(a) shows the structure of a Si-based tandem (micromorph) solar cell and its corresponding band diagram in Figure 2.16(a)[70]. A tunnel junction is inserted between the p s-Si:H layer an the emitter of the bottom cell. Three cases were examined with this structure based on both experiment and simulation: without TRJ layer, using p-type nc-Si as TRJ layer and using p and n-type nc-Si as double TRJ layers.

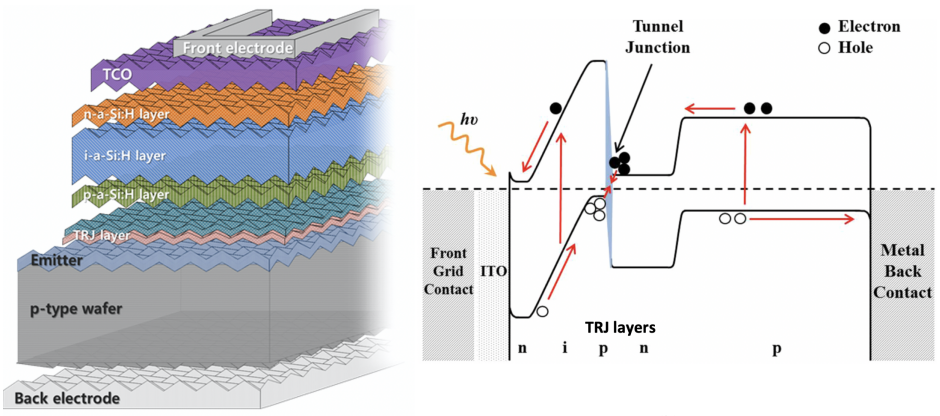

Figure 2.16: Schematic illustration of (a) a micromorph tandem cell and (b) corresponding band diagram [70]

The result shows that the cell with (p)nc-Si/(n)nc-Si double TRJ layers has the best performance with the highest FF(66.16%) and the cell without TRJ layer has the worst performance with an FF equals to 57.86%. The FF increase benefits from a lower series resistance[70]. When double nc-Si layer are inserted at the tunnel junction, the depletion region width would decrease due to the higher doping level and local electric filed, which is much higher than the other two cases[70]. It can be imagined that the higher the doping layer level is, the steeper the valence and conduction band would be. And it would facilitate the electron tunneling.

This concept was also applied in IBC solar cells. Andrea Tomasi et al.[71] developed a simple processing method of so-called tunnel IBC, which relies on the interband tunneling transport. The rear bulk surface is passivated by intrinsic a-SI:H. The n nc-Si:H was patterned using a shadow mask and the p nc-Si:H is deposited on the full rear area. In total only one pattern step is required to process the rear BSF and emitter. At the electron collector contact an interband tunnel recombination junction is formed as shown in Figure 2.17 (b). The tunnel junction should have a low resistance to minimize resistive losses. The TJ is also required to have good electron transport selectivity which means high field effect passivation quality. These two requirements can be achieved by increase doping concentration to a high level. Another requirement for the TJ is that the lateral conductance of the (p)nc-Si:H layer should be low[71] to obtain a high enough shunt resistance. The nanocrystalline layers were optimized by varying doping gas concentrations during deposition to get different crytallinity[72]. The optimized TJ-IBC has an efficiency up to 23.9%[72].

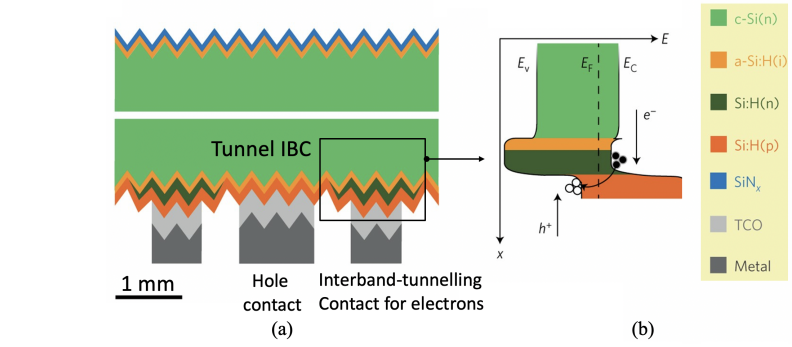

Figure 2.17: (a)Tunnel-IBC structure and (b)tunnel recombination junction band diagram. Adapted from[71]

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3

PROCESS TECHNIQUES

In this chapter, the main process and characterization equipment are introduced. This includes the principles of the used equipment as well as processing details. This chapter starts with wafer preparation and then intrinsic/doped layer deposition, ITO and metal deposition as well as photolithography are also introduced. At last, several characterisation methods are presented.

3.1. Process techniques

In this section the techniques used to deposit the different layers are introduced.

3.1.1. Wafer preparation

In this project, high-quality n-type Float-Zone (FZ) wafers are used. The main parameters are given in table3.1.

Table 3.1: Polished FZ wafer parameters

Doping	Orientation	thickness	Resistivity	Diameter
n-type	<1 0 0>	$280 \pm 20 \mu$m	$1-5\Omega$cm	100 ± 2mm

Cleaning Wafers are cleaned using nitric acid. The standard cleaning line in *EKL* consists of two main steps. Firstly, the wafers are immersed in 99% HNO_3 solution for 10 minutes at room temperature to remove organic contamination on the surface followed by 5 minutes DI water rinsing. And then the wafers are immersed in 69.5% HNO_3 at 110°Cto remove inorganic contamination for another 10 minutes followed by 5 minutes DI water rinsing and drying. During cleaning steps, a chemically grown oxide layer is formed on the surface. Usually before deposition or growth of any other layers, the above mentioned chemically grown oxide or native oxide layer is removed first. This is achieved by 0.55% HF etching for 4 minutes followed again by DI water rinsing and the silicon

surface would become hydrophobic. A special setup named *Marangoni* which uses isopropyl alcohol (IPA) allows to etch and dry the wafers without transferring wafers.

Texturing Random texture on the front side of a solar cell would facilitate light scattering. As more light is coupled into the cell as shown in Figure 3.1, textured surface allows obtaining a higher short circuit current (J_{sc})[6]. This can be achieved using Tetramethylammonium hydroxide (TMAH)[73]. When a <1 0 0> wafer is etched, the <1 0 0> surface reacts much faster and will be etched away. The <1 1 1> surface facets react much slower and will remain on the surface. Therefore, wafers with a random pyramid structure consisting of <1 1 1> facets are obtained. In this thesis project, for texturing, the wafers are immersed in preheated mixed solution of 1 L TMAH and 4 L DI water with 120 ml ALKA-TEX.8 as additive at 80°C[11].

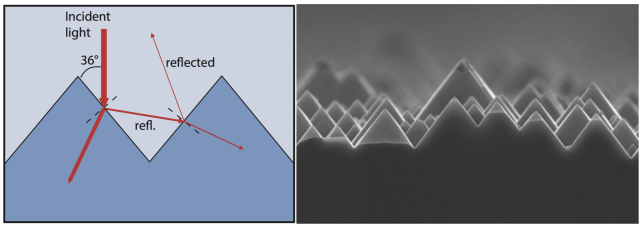

Figure 3.1: Schematic representation of textured surface[6]

NAOS growth As discussed in Section 2.2.2, NAOS tunnel oxide together with heavily doped poly-Si enables excellent passivation quality[74]. In this thesis project, NAOS layer will be applied to passivate the c-Si surface. The wafers are immersed in 69.5% HNO_3 at room temperature for an hour. This does not require any special designed equipment unlike thermal oxide or oxide grown by UV/O_3[27]. The obtained oxide thickness after 1 hour is around 1.5 nm[35]. If the layer gets too thick, the tunneling efficiency across the oxide layer would decrease drastically[17].

3.1.2. Intrinsic and doped layer deposition

Si-based materials are all deposited by chemical vapour deposition (CVD) in this thesis project. Both LPCVD (Low-pressure chemical vapour deposition) and PECVD (Plasma enhanced chemical vapour deposition) are used for intrinsic layer deposition whereas the doped layer is uniquely deposited by PECVD.

Low-pressure chemical vapour deposition The LPCVD system used is textitTempress Systems Inc's LPCVD furnace[75] and the furnace system is shown in Figure 3.2. It can be used to deposit various films such as a-Si:H and nc-Si:H. The chemical reaction in the reactor is thermal driven. With five heaters the temperature is precisely controlled. In this thesis project, the LPCVD furnace is used to deposit intrinsic amorphous silicon layer. The temperature is set at 580°C and pressure at 150mTorr. The recipe used has a deposition rate of around 2 nm/min. In the furnace, the layer is deposited on both sides

of the wafers. After deposition, the wafers are annealed at 600°C for an hour to release the stress.

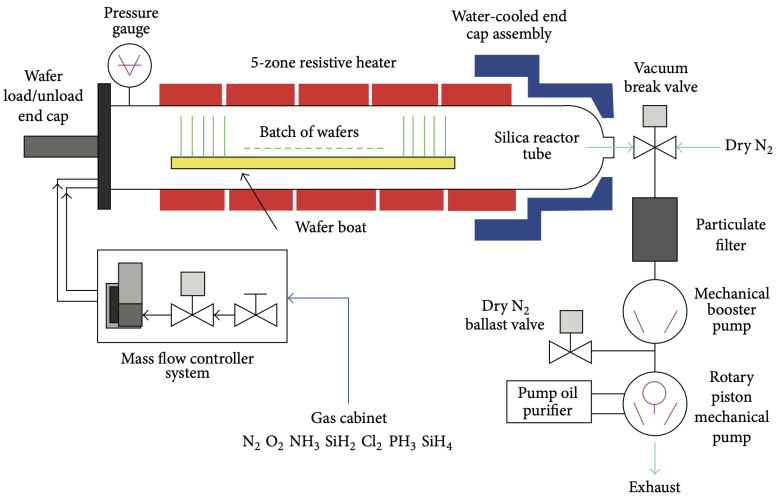

Figure 3.2: Schematic representation of LPCVD furnace system [76]

Plasma enhanced chemical vapour deposition As mentioned in Section 2.3 and Section 2.4, a-Si:H and nc-Si:H can be deposited using PECVD system. The reactor is shown in Figure 3.3. Two PECVD systems are used which respectively named *AMOR* and *AMIGO* (Elettorava, S.p.A.) Both systems have separated chambers for n-type, p-type layer and intrinsic layer deposition as well as other chambers for other functions.

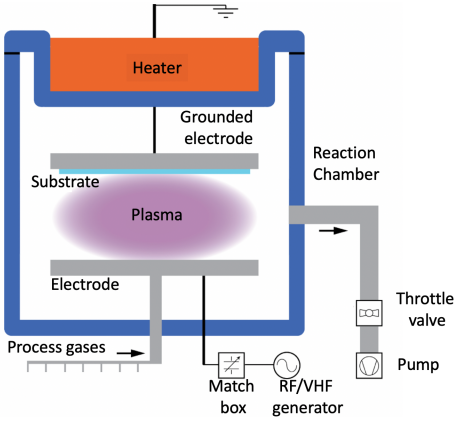

Figure 3.3: Schematic representation of PECVD system [76]

Unlike LPCVD furnace, PECVD works at a lower temperature and a rapidly alternating electrical field is applied between the two electrodes shown in Figure 3.3 to ignite the plasma. The frequency generator is set at radio frequency (RF:13.56HZ) for a-Si:H and nc-Si:H deposition. With plasma presented, the energetic electrons and ions could provide energy to the reaction. Before deposition, the wafers are preheated for 40 minutes to reach a stable temperature at around 180°C. Different gas precursors are available in these systems and mainly silane (SiH4), carbon dioxide (CO2), hydrogen (H2), phosphine (PH3) and diborane (B2H6) are used in this thesis project. *AMOR* is used to deposit n and p type doped a-SiO_x : H layer which is followed by annealing for crystallization. *AMIGO* is mainly used to deposited high quality (i/n)a-Si:H, (n)nc-Si:H and (n)nc-SiO_x : H.

Two other PECVD systems are also used in this thesis project. The *Oxford instruments Plasmalab System 100* in *Kavli nanolab* and *Novellus* in *EKL*. They both are used to deposit SiN_x at 400°C for the purpose of hydrogenation or acting as a protective layer.

Ion-implantation Ion-implantation can also be used to fabricate doped poly-Si layers. *Varian EP500 implanter* is available in *EKL* and the system principle is shown in Figure3.4. During implantation, the dopant species, dose and implantation energy are well-controlled to obtain the expected doping profile. Ions are available in the plasma. They are directed using magnets and accelerated by voltage gradient. At last, an ion-beam with certain energy is directed to the substrate and penetrates the surface.

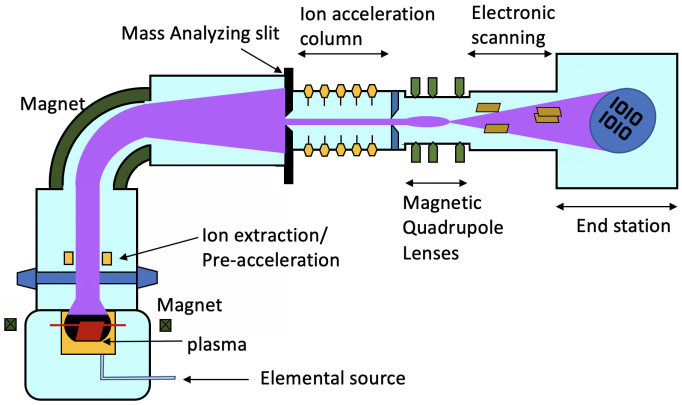

Figure 3.4: Schematic representation of ion-implantation

High-temperature annealing An annealing step is necessary after ion-implantation or PECVD doped amorphous layer deposition to crystallize the a-Si(O_x:H) into poly-Si(O_x:H). The annealing process in N_2 activates the dopants and in the meantime the dopants would diffuse[30][77]. If a large amount of dopants diffuse into the bulk the passivation quality would degrade as explained in Section 2.2. So it is important to optimize the annealing parameters. Another Tempress furnace like the one in Figure 3.2

is used for annealing. In this thesis project, the a-SiO_x : H deposited in *AMOR* was annealed at 850°Cfor 45minutes, and dopants implanted a-Si was annealed at 950°Cfor 3minutes. Another annealing step is applied after hydrogenation by SiN_x capping layer namely forming gas annealing. The wafers are annealed in atmosphere of 10% H_2 in N_2 for 30 minutes at 400°C. This is also the temperature at which the SiN_x layer is deposited.

3.1.3. Electrode material deposition

Two physical vapour deposition (PVD) methods are introduced in this section: sputtering and evaporation. Different from CVD process, no chemical reaction is involved.

ITO sputtering The equipment *ZORRO* (Polyteknic AS) is used for transparent conductive oxide (TCO) sputtering and the working principle is briefly shown in Figure 3.5. The target material is heated in vacuum. Radio frequency is applied to ionize the argon gas. During the deposition a magnetic field is applied to increase the ion-current density, and thus, it is called magnetron sputtering. The generated argon ions are accelerated towards and bombard the target material. The species are sputtered from the target and then deposited on the substrate. The electronic passivation quality would degrade due to sputtering damage caused by energetic ion bombardment.

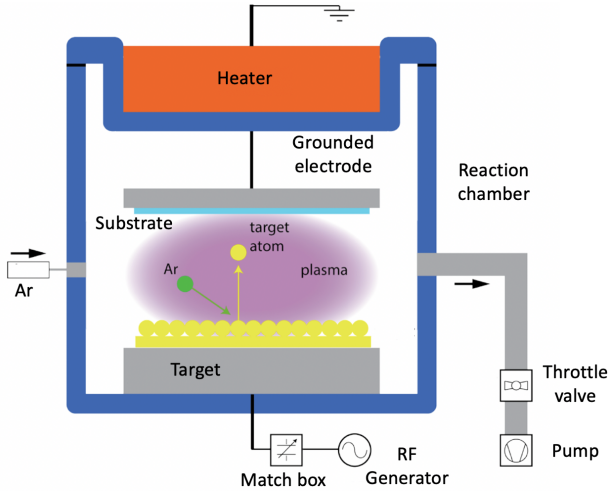

Figure 3.5: Schematic representation of TCO sputtering system [76]

TCO layer is usually coated at the front side of FBC solar cell to improve lateral conductivity[78] as it facilitates the transport of charge carriers to metal grid terminals. In this thesis project, indium tin oxide (ITO) is used which consists of 90% indium oxide (In_2O_3) and 10% tin oxide (SnO_2)[6]. At the front side of FBC cells 75 nm ITO is deposited which can also serve as ARC layer. At the rear side, ITO layer can improve infrared light response[79].

Metallization Evaporation technique is applied for metallization. This is done using*PROVAC PRO500s*. The react chamber is illustrated schematically in Figure 3.6. The metal can be heated up and melt thermally or by e-beam. The melt source material would evaporate and condense on the substrate surface.

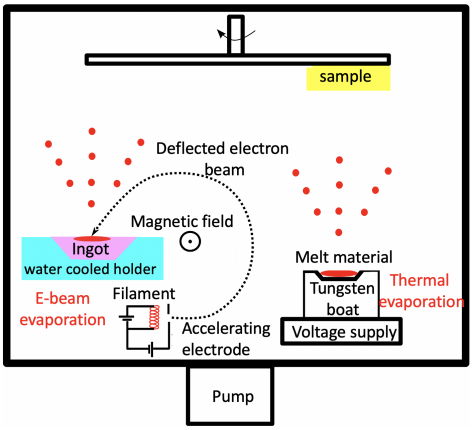

Figure 3.6: Schematic representation of evaporation system [80]

The heat for thermal evaporation comes from the resistor under high voltage. A tungsten boat is used to hold source material with lower melt point than the boat itself such as Ag. For e-beam evaporation, the energy comes from the accelerated electrons which would strike into the source material. E-beam evaporation is used for material with high melt point or material that can alloy or react with tungsten. In this thesis, this system is used to deposit aluminum and silicon oxide layer. The deposition process is conducted in high vacuum environment to minimize collisions of source atoms with background species.

3.1.4. Photolithography and wet etching

In this subsection, photolithography as well as the necessary etch chemicals are introduced. This step is vital for IBC rear structure patterning.

Photolithography As shown in Figure 3.7 the photolithography consists of three main steps: coating, exposure and development. The whole process takes place in the polymer lab of *EKL*. The *Brewer science manual spinner* is used for photoresist coating. Both positive (AZ ECI3027) and negative (nLOF^{TM}2020) photoresist are used. *SUSS MicroTec MA/BA8 mask aligner* is used for mask alignment and exposure. The exposure time depends on the photoresist type and thickness. The development step is done manually using the MF322 solution. Exposed positive photoresist would dissolve in development solution. For negative photoresist, the unexposed photoresist would dissolve. To use nLOF^{TM}2020 photoresist, the wafers need HMDS (hexa-methylenedi-siloxane) treatment first to ensure good adhesion of photoresist to the wafer. This is fullfilled by leaving wafers in HMDS vapour for 10 minutes at room temperature. Then the wafer is coated with photoresist, baked, exposed, baked again and developed. In this thesis,

photolithography with positive photoresist is used to pattern the front metal grid of FBC cells and rear surface of IBC cells for metallization followed by lift-off.

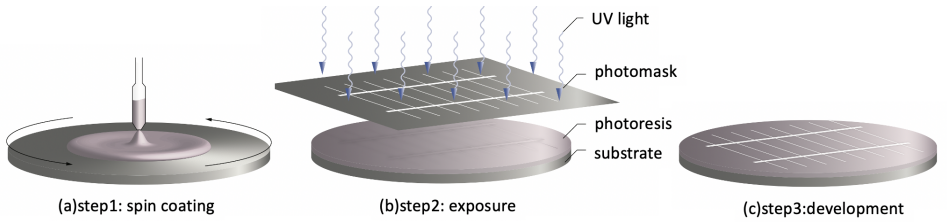

Figure 3.7: Schematic representation of photolithograpgy. Adapted from [81]

Wet chemical etch Following the photolithography steps, usually wet etching steps are needed to pattern the structure. Different etchants are used to etch different materials on the surface. And the etching time should be well-controlled to avoid over-etch or under-etch. Table 3.2 shows the etching processes for patterning the rear side of IBC cells.

Table 3.2: Chemicals used for etching and other processes

Substrate Material	SiN_x		poly-Si	ITO
Etchant	1.BHF1:7	2.0.55%HF	$40\%HF + 69.5\%HNO_3\,1:40$	30%HCL

3.2. Characterisation method

In this section, several characterization methods used in this thesis are introduced: Photoconductance lifetime tester, Dark conductivity and Activation energy measurement, Current-voltage measurement, Reflection and External quantum efficiency measurement.

3.2.1. Photoconductance Lifetime Tester

Photonconductance lifetime tester is an important tool used for multiple times throughout the cell fabrication. It provides valuable information of τ_{eff}, J_0) and iV_{oc} for process control and device optimization. The minority carrier lifetime is the characteristic time for the minority charge carriers to decay back to thermal equilibrium concentration after excitation. Different recombination mechanisms as explained in Section 2.1.1 would facilitate the decay process and reduce the carrier lifetime. The measure principle is illustrated in Figure 3.8.

In this thesis, Sinton WCT-120 lifetime tester is used. The required inputs are wafer doping type, thickness, resistivity and optical constant. The samples are placed above a coil on the stage at a constant temperature. The flash lamp gives a very short light pulse to

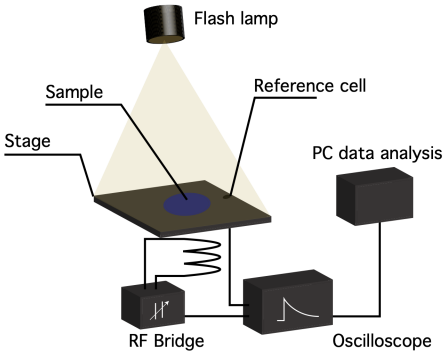

Figure 3.8: Schematic representation of Sinton WCT-120[82].

the sample. Due to the illumination, the photoconductance of the wafer will increase. The coil located underneath the wafer sends electromagnetic waves into the wafer above and it will also sense the change of conductance in the sample which leads to a change in impedance of the coil. This signal is sent to and measured by an RF bridge circuit connected to the coil. Before returning to thermal equilibrium and while excess carriers are presented, for n-type wafer the excess photoconductance σ_L can be calculated by the following equation[83]:

$$\sigma_L = q(\Delta n \mu_n + \Delta p \mu_p) W = q \Delta p (\mu_n + \mu_p) W \tag{3.1}$$

where μ_n and μ_p are respectively electron and hole mobility. Δn and Δp are excess electrons and holes concentration, respectively. And W is the wafer thickness. Generally two modes are available for analysis depending on the range of carrier lifetime: transient photoconductance decay mode (PCD) and quasi-steady-photoconductance mode (QSSPC). Transient PCD mode which has a shorter light pulse is recommended for samples with higher carrier lifetime and QSSPC mode with much longer light pulse is for samples with shorter lifetime. The carrier effective lifetime can be calculated by the following equation:

$$\tau_{eff} = \frac{\sigma_L}{J_{ph}(\mu_n + \mu_p)} \tag{3.2}$$

where $J_{ph}$is the photocurrent. For low-level injection, the recombination rate of minority carriers can be considered equal to the excess electron concentration divided by the effective τ_{eff}, so lifetime can be expressed using the following equation[6]:

$$\tau_{eff} = \frac{\Delta_p}{G - \frac{\partial \Delta p}{\partial t}} \tag{3.3}$$

where G is the calculated carrier generation rate calculated. For transient PCD mode G is considered to be zero and for QSSPC mode $\frac{\partial \Delta p}{\partial t}$ is considered zero. The carrier lifetime in this thesis is read at a minority carrier density(MCD) of 10^{15}cm^{-3} which is close to the injection level under one sun illumination. Carrier lifetime τ_{eff} is a function of

MCD[61]. At higher injection level (MCD > 10^{15}cm^{-3}) the recombination mechanism is more influenced by Auger recombination as the excess carrier density is high. At lower injection level (MCD < 10^{15}cm^{-3}) the recombination mechanism is more dominant by SRH recombination and the measure τ_{eff} can reflect the defect density level. Different from measure device level V_{oc}, iVoc is calculated with minority carrier density using following equation:

$$iV_{oc} = \frac{K_B T}{q} ln(\frac{\Delta p(N_D + \Delta p)}{n_i^2}) \tag{3.4}$$

where N_D represents the donor doping concentration. Except implied circuit voltage, sheet resistance and saturation current density can also be obtained.

3.2.2. Dark Conductivity and Activation Energy Measurement

Activation energy(E_{act}) is the energy gap between the Fermi level and the conduction band or valence band as schematically shown in Figure 3.9. For same materials, a lower activation energy means higher doping level. In interband tunnel recombination junctions, it is necessary to have high doping level to reduce junction space charge region which would improve the tunnelling efficiency.

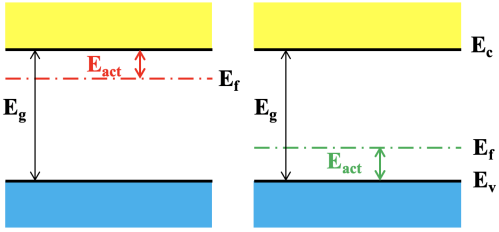

Figure 3.9: Activation energy definition for n-type and p-type material.

The dark conductivity is firstly measured, and it can be expressed as:

$$\sigma_d = q(n\mu_n + p\mu_p) \tag{3.5}$$

where n and p, μ_n and μ_p are respectively carrier density and mobility for electrons and holes. Considering a n-type wafer, the electrons concentration is related to the Fermi level as shown in the equation below:

$$n = N_c exp(\frac{E_F - E_C}{K_B T}) \tag{3.6}$$

where N_C is conduction band effective density. The dark conductivity is also related to the activation energy as shown in equation below:

$$\sigma_d(T) = \sigma_0 exp(-\frac{E_{act}}{K_B T}) \tag{3.7}$$

The measurement is conducted in dark environment. The current I and applied voltage V are measured. The dark conductivity at a certain temperature is determined by the

following equation:

$$\sigma_d(T) = \frac{dI}{tlV} \tag{3.8}$$

where l and d are respectively electrodes length and the distance between two electrodes, and t is the measured layer thickness. The measurement of σ_d is conducted at a series of substrate temperature. A linear function can be obtained by fitting $ln(1/\sigma_d(T))$ over $1/K_B T$ and the slope is the activation energy.

3.2.3. Current-Voltage Measurement

AAA class Wacom WXS-90S-L2 solar simulator is used in to measure solar cell external parameters, most importantly, the J-V curve. The measurement setup is shown in Figure 3.10 (a). The measurement is conducted at standard test condition (STC). The stage is controlled at 25°C by a water cooling system. The light from the light source which consists of a Xe-lamp and a halogen lamp is characterized by an AM1.5 spectrum and an irradiance of 1000W/m^2. Before measurement, the lamps are warmed up first and the system is calibrated with two reference cells. The J-V curve is obtained by a 4 point probe measurement with high accuracy, which means that two separate sets of probing wires are used for voltage supply and current collection. With 4-probe measurement, the voltage supply and sourcemeter are attached to the solar cell with two separate pairs of wires. This makes it possible to apply the voltage very accurately, since there will not be any current flowing through these wires. All the current will flow through the sourcemeter and thus, the voltage drop across wires in 2-probe measurement is avoided.

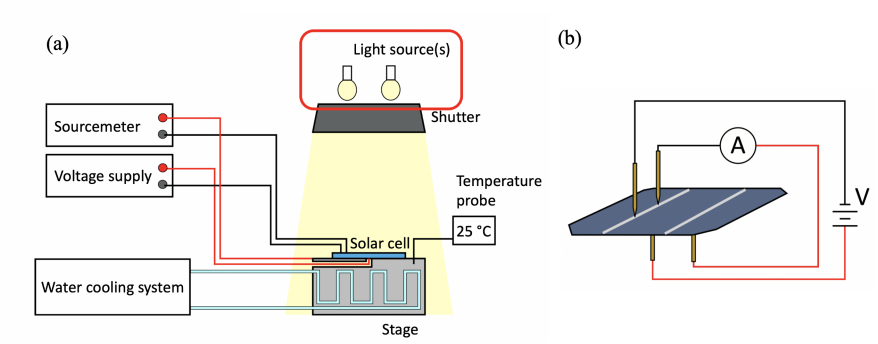

Figure 3.10: Schematic representation of (a) Wacom measurement setup and (b) four-probe measurement. Adapted from *EE4377 PV Technologies course material*

Figure 3.11 (a) shows a typical p-n junction J-V curve. This is also the main output of Wacom. V_{mpp} and I_{mpp} are the voltage and current at the maximum power point. From the J-V curve some other parameters can be calculated. The slope of the more vertical part of the J-V curve represents the series resistance and the effect on J-V characteristics is shown in Figure 3.11 (b). The slope of the more horizontal part of the J-V curve represents the shunt resistance and the effect on J-V characteristics is shown in Figure 3.11 (c). For a high-performance solar cell, always low series resistance and high shunt resistance are expected. Besides the resistance, solar cell FF and efficiency (η) can also

be calculated using the following equations:

$$FF = \frac{V_{mpp} \times J_{MPP}}{V_{oc} \times J_{sc}} \tag{3.9}$$

$$\eta = \frac{V_{mpp} \times J_{mpp}}{I_{in}} = \frac{V_{ov} \times J_{sc} \times FF}{I_{in}} \tag{3.10}$$

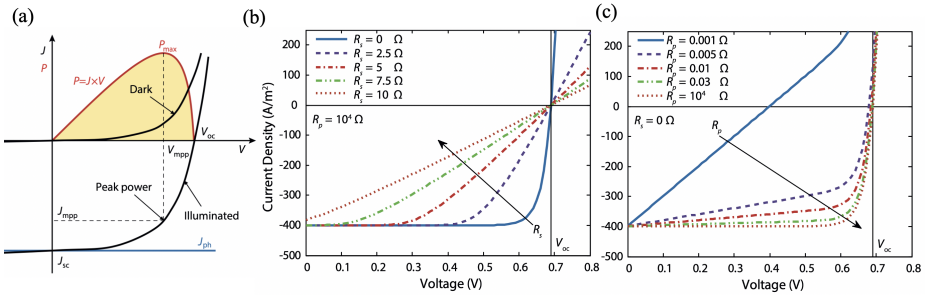

Figure 3.11: (a)J-V characteristics of a p-n junction and the effect of (b) series resistance R_s and (b) parallel resistanceR_p (shunt resistance) [6].

3.2.4. Reflectance measurement

In this thesis a *PerkinElmer Lambda 950 UV/VIS spectrometer* is used to measure the reflectance. Figure 3.12 shows the measurement setup overview. The optical system generates two monochromatic beams with high resolution which are the reference beam and the sample beam. The beam is directed into the integrating sphere which is coated with a highly reflective and scattering material called Spectralon. the light entered the sphere would be reflected for many times and scattered in all direction and generates a homogeneous electromagnetic field inside the sphere. The two detectors (green) at the bottom of the sphere can measure the light density over a large range of wavelength. The port plug can be used to remove the specular reflection and thus only the diffuse reflection is measured. The reference beam is used to determine and correct the chamber reflection.

3.2.5. External quantum efficiency measurement

The external quantum efficiency(EQE) represents the ratio of successfully collected electron and hole pairs to the total incident photons on the solar cell surface. EQE is a function of wavelength and is calculated by the following equation:

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{q\Psi_{ph,\lambda}} \tag{3.11}$$

where $\Psi_{ph,\lambda}$ is the spectral photon flow on the solar cell[6] and $I_{ph,\lambda}$ is photocurrent. Various optical and electrical losses could bring the value lower than 100%, such as parasitic absorption, reflective loss and recombination losses. The EQE-setup which is also

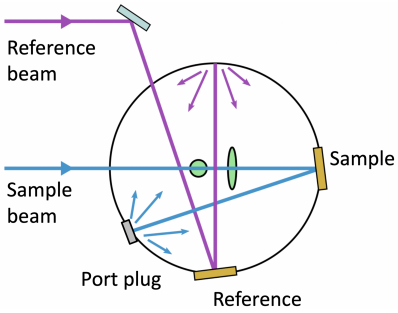

Figure 3.12: Reflectance measurement setup. Adapted from *EE4377 PV Technologies course material.*

called spectral response setup is shown in Figure3.13. A xenon lamp with very even spectral distribution is used to provide a light source with a continuous spectrum. The light is first chopped by the chopper wheel to have an on-off frequency. And then it passes through the monochromator which selects a very narrow wavelength band from the incoming light spectrum. Then the chopped monochromatic light is focused on the solar cell by lens system. The current is then measured and the current signal is sent to and processed by the lock-in Amplifier. The lock-in amplifier is also capable of filtering the solar cell's response from the environmental noise as the solar cell is a light-sensitive device.

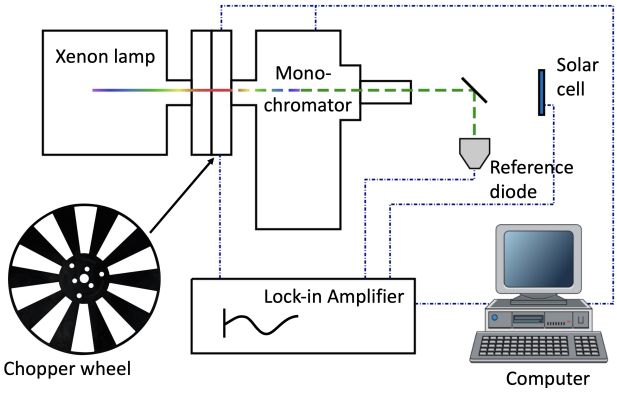

Figure 3.13: Schematic of EQE measurement setup. Adapted from *EE4377 PV Technologies course material.*

$\Psi_{ph,\lambda}$ is determined by using a reference diode with known EQE curve. And it is calculated using the following equation:

$$\Psi_{ph,\lambda} = \frac{I_{ph}^{ref}(\lambda)}{qEQE^{ref}(\lambda)} \tag{3.12}$$

With $I_{ph,\lambda}$which can be measured directly using an Ampere meter, the EQE curve can be obtained by combining the above two equations 3.11 and 3.12:

$$EQE(\lambda) = EQE^{ref}(\lambda)\frac{I_{ph}(\lambda)}{I_{ph}^{ref}(\lambda)} \tag{3.13}$$

EQE measurement is also an accurate way to measure the short circuit current density by performing the measurement under short circuit conditions. That's because the J_sc determined in this way is independent of the light source spectral and the light source simulator used in J-V curve measurement can not fit the AM1.5 spectral 100%. Besides, shading masks are used in EQE measurement to avoid contact area influence. The measured wavelength-dependent photon flow is integrated over the whole AM1.5 spectral photon flux to obtain the short circuit current density and multiplied by elementary charge constant using the following equation:

$$J_{sc} = -q\int_{\lambda_1}^{\lambda_2} EQE(\lambda)\Phi_{ph,\lambda}^{AM1.5}d\lambda \tag{3.14}$$

It is possible to obtain the internal quantum efficiency(IQE) by extracting reflective loss from the EQE measurement. In this way only absorbed photons are considered and this really reflects the solar cell internal problem. the IQE can be determined by:

$$IQE(\lambda) = \frac{EQE(\lambda)}{1 - R(\lambda)} \tag{3.15}$$

where $R(\lambda)$ is the wavelength-dependent reflectance.

4

TRJ PROOF-OF-CONCEPT IN HYBRID FBC SOLAR CELLS

Before making poly-Si/SHJ hybrid IBC solar cells, the TRJ proof-of-concept was demonstrated in FBC solar cells first. Different materials combinations were tested:(i)a-Si:H/(n)a-Si:H, (i)a-Si:H/(n)nc-Si:H and (n)a-Si:H/(n)nc-Si:H. It was found that the TRJ was not working with an (i)a-Si:H and the dual-n-layer structure was proved feasible.

4.1. FBC cell fabrication process

In this section, the major process steps of FBC solar cells is explained as shown in Figure 4.1. (1) N-type FZ <1 0 0> c-Si wafers were used. SiN_X was first deposited on one side of the wafer as a protective layer. (2) Then the wafer was textured using TMAH and the side with SiN_X was protected from texturing. After texturing and cleaning the wafer was immersed in poly-etch solution ($69.5\%HNO_3 : 40\%HF = 40 : 1$)for 2 minutes. This is because a poly-etch step is necessary for the IBC cell fabrication and will be explained in Section 5.2.1. (3) And then protective SiN_X layer was etched in BHF7 : 1 solution followed by standard cleaning.

(4) The wafer was etched using *Marangoni* first and then immersed in $69.5\%HNO_3$ for one hour at room temperature to grow a silicon oxide layer of around 1.5 nm thick[35]. (5~6) Next, the wafer was loaded in PECVD *AMOR*. An (i)a-SiO_x : H layer was deposited first and then a n-type or p-type a-SiO_x : H layer was deposited on the intrinsic layer. An (i)a-Si can also be deposited using LPCVD to replace the (i)a-SiO_x : H deposition. (7) As shown in Figure 4.1, the wafer was annealed at 850°C for 45 minutes. After annealing the amorphous layer would crystallize into doped poly-SiO_x. Then on both sides, 120 nm SiN_X was deposited using PECVD system *Oxford Instruments PlasmaPro80* in *Kavli nanolab* at 400°C for hydrogenation. (8) After that the wafer was annealed in forming gas for 30 minutes at 400°C. At this point, all high-temperature processes were finished.

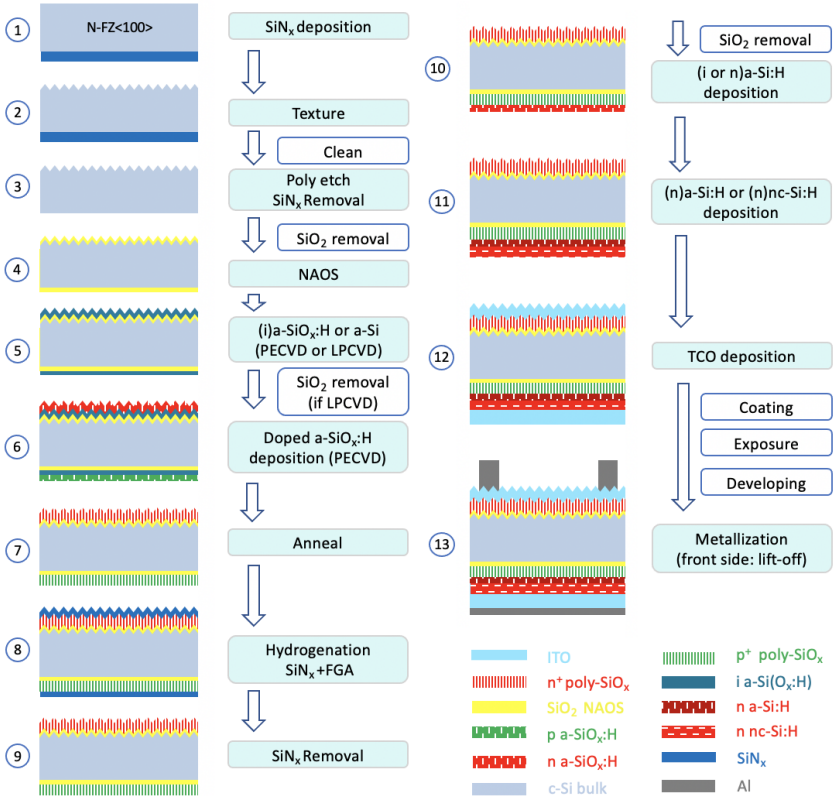

Figure 4.1: Schematic presentation of FBC cells fabrication process

(9) The SiN_X layer was etched fast using BHF7:1 followed by slow etching in 0.55% HF. It is crucial to control the etching time in BHF7:1 to avoid over-etch the poly layer. (10~11) After SiN_X removal, the wafer was ready for high-quality SHJ solar cell films deposition in another PECVD system *AMIGO*. Right before loading in the equipment, the oxide(chemically grown after cleaning) on the wafers was removed first using 0.55%HF.

(12) In step 12, 75 nm and 150 nm ITO were sputtered respectively on the front and the rear side. A metal mask was attached on the surface to define the dies on the wafer. (13) Then, the cells were metalized using e-beam system *PROVAC*. Before metallization, the front side was firstly coated with a thick photoresist layer (12 µm) and then, exposed and developed to define metal pattern. Secondly, Al was deposited on both sides. At last, part of the Al together with the photoresist on the front side were removed by a lift-off process in acetone and the metal grid remained. On the rear side, the dies were fully covered by Al using a metal mask with the same design as the one used in step 12.

4.2. TRJ with (i)a-Si:H/(n)a-Si:H in FBC cells

In this section, a preliminary test was conducted to find out the (i)a-Si:H buffer layer influence on the TRJ. The cell structure will be presented first and then the measured device results are discussed.

4.2.1. Cells design with (i)a-Si:H/(n)a-Si:H

The fabrication steps of FBC cells is introduced in detail in section4.1. Cells with different structures were fabricated to study the influence of the (i)a-Si:H/(n)a-Si:H presence as shown in Figure 4.2. Three cells were made: (a)without any extra layer as the reference cell, (b)with only a 20 nm (n)a-Si:H layer and the (c) has both 4 nm (i)a-Si:H and 20 nm (n)a-Si:H layers.

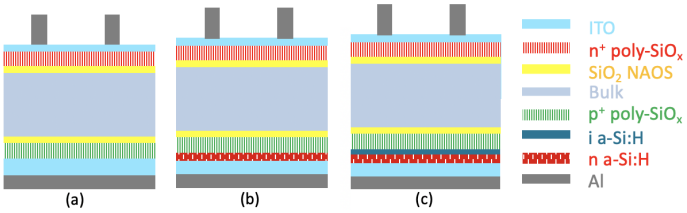

Figure 4.2: Solar cell sketches for (a)reference cell without TRJ (b)with only (n)a-Si:H (c)with both (i)a-Si:H/(n)a-Si:H

Figure 4.1 describes most of the fabrication process. But in this experiment, double sides flat wafers were used. And only PECVD *AMOR* was used for amorphous layer deposition before annealing as shown in Figure 4.1 step 5 and 6. The poly-SiO_x layer after annealing had a thickness of around 20 nm. It should be pointed out here that these three precursors were only hydrogenated by FGA without SiN_x as capping layer hydrogenation. After ITO sputtering, the cell was metalized. On the front side, the metal grid has a thickness of 2 µm and on the rear side, the cell is fully covered by 1 µm Al. The 75 nm ITO at the front side also served as the ARC layer. The mask consisting of 15 dies of different sizes was used to define the die area and a corresponding 15-die photomask of different metal coverage was used. A picture of a finished wafer is shown in Figure 4.3

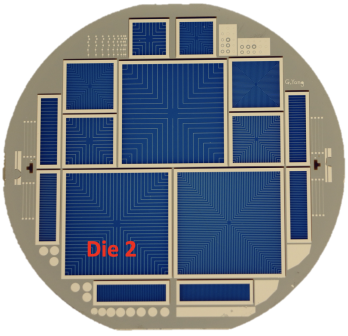

Figure 4.3: The front side layout design of the FBC cells with 15 solar cell dies

After depositing the (i)a-Si:H/(n)a-Si:H layer on the (p^+)poly-SiO_x surface, an interband tunneling recombination junction was introduced. Figure 4.4 shows again the rear side band diagram. The holes are transported to the (p^+)poly-SiO_x and recombine with the electrons tunneled from the a-Si:H layer. The main goal of these three cells was to study the influence on the FF to support further improvement of the TRJ.

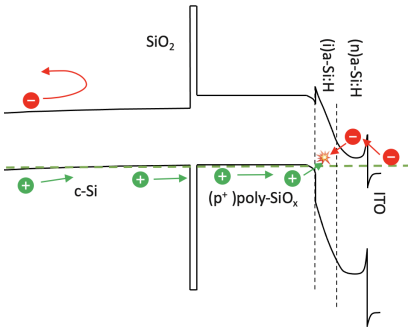

Figure 4.4: Emitter side band diagram

4.2.2. FBC cells with (i)a-Si:H/(n)a-Si:H performance comparison

The cell precursors iV_{oc} were measured after annealing, FGA and ITO sputtering which respectively correspond to the step 7,8 and 12 shown in Figure 4.1.

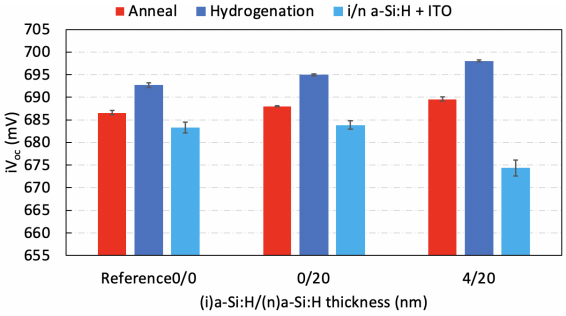

Figure 4.5: Preliminary test cell precursor passivation quality

As masks consisting of 15 different dies were used, in total 15 measured results were available. After metallization, the cell external parameters were measured using *WA-COM*. After eliminating very strange values, the results are plotted in a box plot in Figure 4.6. The reference cell and the one with only 20 nm (n)a-Si:H layer have comparable V_{oc}, but, the one with both 4/20 nm (i)a-Si:H/(n)a-Si:H has a much lower V_{oc}. As for the FF, the drop is even more obvious. The average FF of the three largest dies dropped from 65.56%(reference cell) to 51.61% after adding only (n)a-Si:H. However, the cell with both 4/20 nm (i)a-Si:H/(n)a-Si:H layers have extremely low FF of less than 23%. Obviously, the carriers are not able to tunnel through the TRJ efficiently.

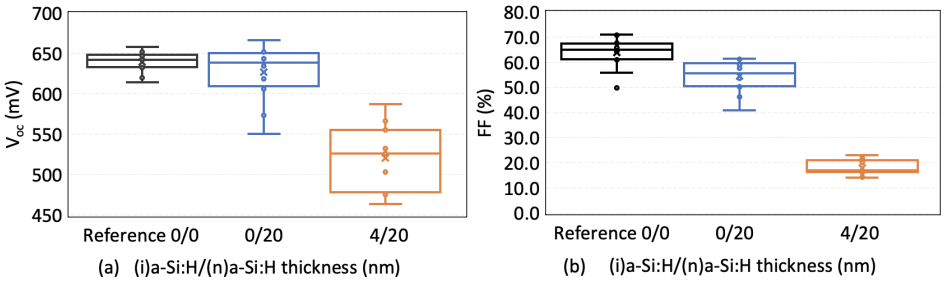

Figure 4.6: (a)V_{oc} and (b) FF comparison of cell without TRJ, with (n)a-Si:H and with i/n a-Si:H

The J-V curves of die2 on each wafer are plotted in Figure 4.7. Die2 has a cell area of 8.97 cm^2 and a metal coverage of 2.96%. The reference cell, the cell with only (n)a-Si:H layer and the cell with both layers respectively have an efficiency of 13.37%, 10.28% and 1.03%. The cell with both (i)a-Si:H/(n)a-Si:H layers is not working. As it can also be seen Figure 4.7 that its J-V curve shape is abnormal. And the J-V curve of the cell with (n)a-Si:H also deviates from the reference cell without TRJ. From the curve it can be seen that the deviation is caused by its higher R_{series}. Nevertheless, when only a (n)a-Si:H is deposited directly the TRJ is still working, even though, the FF drops 15.76% in die2 as compared to the reference cell without TRJ.

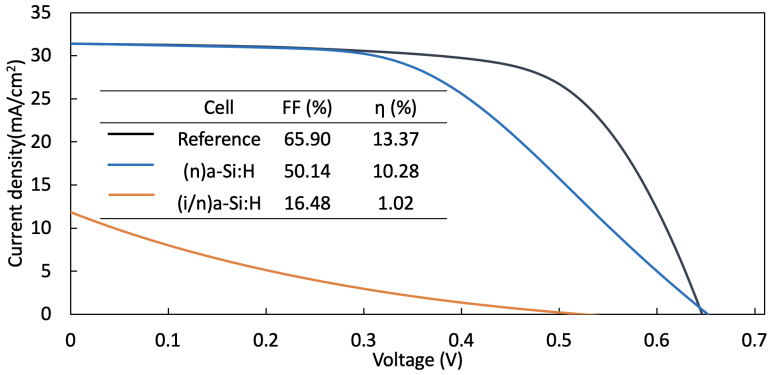

Figure 4.7: J-V curves of reference cell without TRJ, cell with (n)a-Si:H and cell with i/n a-Si:H(Die2)

To conclude, adding a 4 nm thick (i)a-Si:H between the p^+poly-SiO_x layer and the (n)a-Si:H layer decreases significantly the tunneling efficiency of the TRJ. As discussed in section2.5 that the doping level (Fermi level) at both sides of the TRJ and depletion width affect the tunneling efficiency. The reason for the low FF in the cell with both (i)a-Si:H/(n)a-Si:H layers could be that the 4 nm (i)a-Si:H is too thick. The TRJ performance can be improved by decreasing the intrinsic layer thickness or replacing (n)a-Si:H with a more conductive material such as (n)nc-Si:H. As (n)nc-Si:H has a smaller E_{act}, the depletion region width should be thinner and the conduction band slope at the TRJ would be steeper[6].

4.3. TRJ with (i)a-Si:H/(n)nc-Si:H in FBC cells

It was proved that inserting a 4 nm (i)a-Si:H would decrease the FF to a very low level and the device is no longer considered working. Another two sets of FBC cells were made to investigate the influence of the (i)a-Si:H layer thickness. This time, the (n)a-Si:H is replaced with (n)nc-Si:H, and in these two sets of FBC cells, the (n)nc-Si:H layers have two different doping levels.

4.3.1. Cell design with (i)a-Si:H/(n)nc-Si:H

Cell structure Figure 4.8 shows the structure of the cells. Unlike the cells for in previous preliminary test, front side textured wafers were used here and the precursors were also hydrogenated by SiN_x. Still, both (i)a-SiO_x : H/(n or p)a-SiO_x : H layers before annealing as shown in Figure 4.1 step 5 and 6 were deposited using PECVD *AMOR* only. (n)nc-Si:H layers with two different doping levels were deposited. In total, 12 cells were made as shown in Figure 4.8. They are (a) two reference cells, (b) two cells with only 30 nm (n)nc-Si:H at two different doping levels, and (c)8 cells with 1, 2, 3 and 4 nm (i)a-Si:H and 30 nm (n)nc-Si:H at two different doping levels.

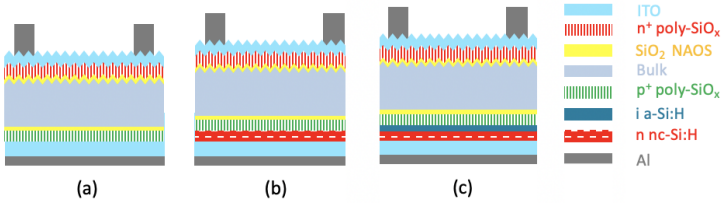

Figure 4.8: Solar cell sketches for (a)Reference cell without TRJ (b) with only (n)nc-Si:H (c) with (i)a-Si:H/(n)nc-Si:H

E_a of (n)nc-Si:H As mentioned above, (n)nc-Si:H with two different doping levels were used. Nc-Si:H has a lower E_{act} because it has a higher doping efficiency[84]. It is possible to get different doping level by adjusting the doping gas PH_3 flow during deposition of (n)nc-Si:H. The measured E_{act} is shown in table 4.1. Lower E_{act} was obtained by reducing the doping gas flow rate. A low E_{act} and highest dark conductivity were obtained at 0.2 sccm flow rate. By applying this flow rate, it is expected that the tunneling efficiency would increase and the cell FF would also increase. This could be that the crystalline phase increases by decreasing PH_3 flow rate[85].

Table 4.1: Electrical properties of(n)nc-Si:H deposited under different PH_3 flow rates

	(n)nc-Si:H				(n)a-Si:H
PH3 flow rate(sccm)	0.2	0.7	1.2	1.7	11
Thickness(nm)	20.8	20.7	20.2	20.8	20.3
E_{act}(meV)	39.84	39.23	48.18	63.01	236.02
Dark conductivity(@25°C,S/cm)	6.01E+0	4.27E+0	2.04E+0	7.25E-1	0.59E-2

Cell precursor passivation quality Two groups of cells with (n)nc-Si:H at different doping levels and 0~4 nm of (i)a-Si:H variations were made. Each group also has a reference cell and all cells in each group were processed in the same run. In Figure 4.9, numbers without (group1) and with (group2) an apostrophe indicate the (n)nc-Si:H deposited under 1.2 and 0.2 sccm respectively. The precursor iV_{oc} was measured several times along the fabrication process. The measured results are shown in Figure 4.9. All precursors had iV_{oc} within the range 668~690 mV after annealing and the passivation uniformity between different precursors is low. But after hydrogenation the passivation uniformity both among the precursors and on one precursor(see the error bar) were largely improved. All wafers had an average iV_{oc} larger than 710 mV after hydrogenation. After the deposition of (i)a-Si:H and (n)nc-Si:H, the iV_{oc} dropped and the difference between wafers was still small. The (n)nc-Si:H doping level does not have an obvious influence on the FBC cell precursor passivation. However, iV_{ov} dropped more than 30 mV after ITO deposition. This will be discussed more in detail in Section 4.4.2.

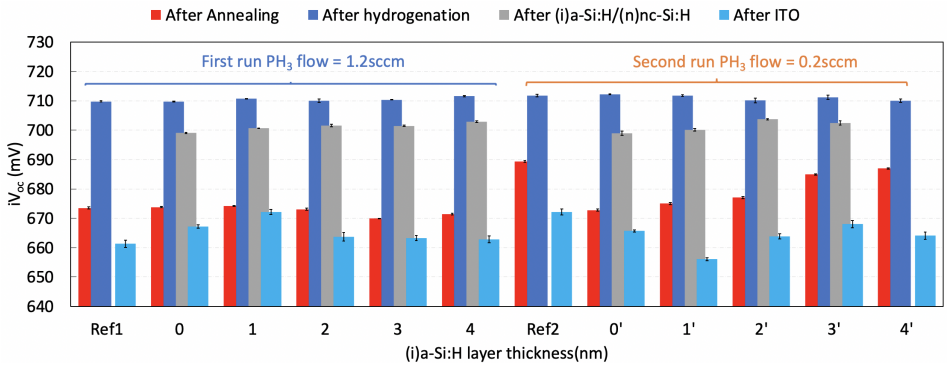

Figure 4.9: Precursor passivation quality of cells with different (i)a-Si:H layer thickness and (n)nc-Si:H deposition PH_3 flow rate

4.3.2. FBC cells with with (i)a-Si:H/(n)nc-Si:H performance comparison

The cells were also metalized using *Provac* and lift-off process as introduced in previous section. The measured cell external parameters are shown in Figure 4.10. The blue and orange line respectively represent the cells with (n)nc-Si:H deposited with PH_3 flow rate of 1.2 sccm and 0.2 sccm as well as their corresponding reference cell. The J_{sc} decreases with (i)a-Si:H layer thickness. The cell with 1 nm (i)a-Si:H in group 2 has much lower V_{oc} than that in group 1. This is considered caused by equipment reproducibility or other factors during the process. The FF drops to a very low level even with only 1nm (i)a-Si:H and it keeps decreasing with the (i)a-Si:H thickness. The efficiency measured results show a similar trend as FF. Comparing to the corresponding reference cell, the FF drop in cell with 0 nm (n)a-Si:H is 0.30% in the case with 0.2 sccm PH_3 flow rate, which is smaller than in the case with 1.2 sccm (1.41%). This benefits from the lower E_{act} and higher conductivity of the (n)nc-Si:H layer.

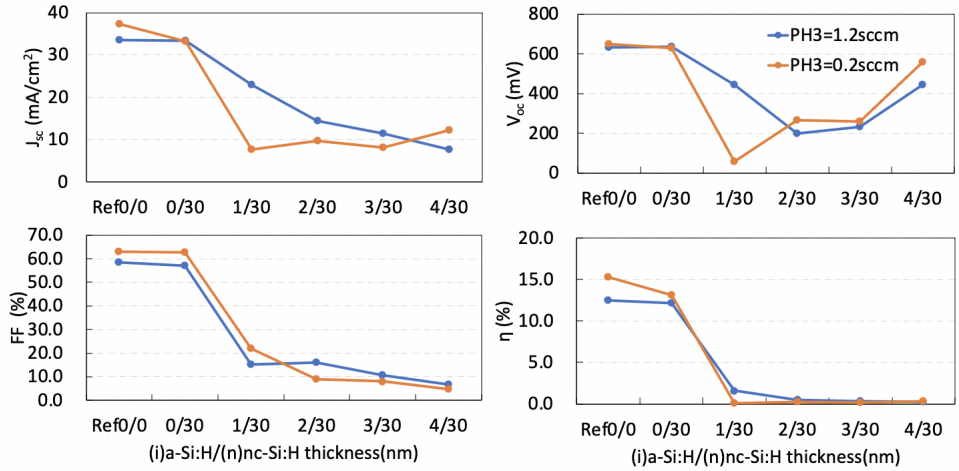

Figure 4.10: External parameters comparison of cells with varied (i)a-Si:H layer thickness (0, 1, 2, 3 ,4 nm) and 30 nm (n)nc-Si:H

Figure 4.11 shows the J-V curves of cells (die2) in group1. It can be seen that the J-V curve of the cell with 30 nm (n)nc-Si:H only deviates slightly from the reference. It can be concluded that an (i)a-Si:H layer can not be inserted here in the proposed hybrid structure even with 1 nm thickness. However the (i)a-Si:H is important for the IBC precursor passivation as this layer is partially deposited directly on the c-Si bulk surface as shown in Figure 1.8. As the TRJ is working with only (n)nc-Si:H, the passivation would be largely degraded in IBC cells due to the lack of (i)a-Si:H buffer layer. During the deposition of (n)nc-Si:H a larger power of 11W (for (i)a-Si:H power=3 W) is applied which means more bombardment damage to the bulk surface. So it is necessary to find an alternative material to replace the (i)a-Si:H which can ensure the tunnel efficiency and not degrade the passivation quality severely.

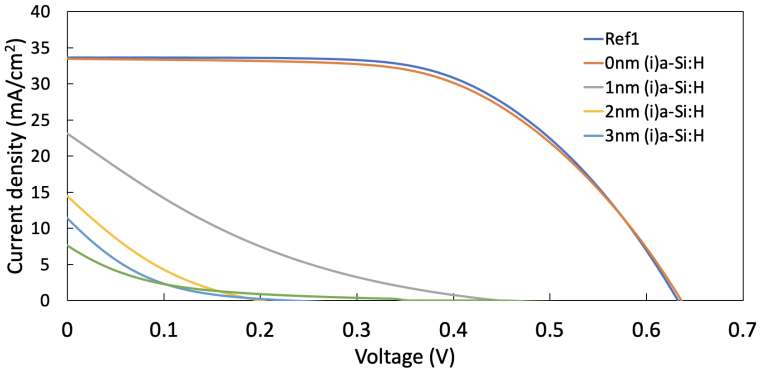

Figure 4.11: J-V curves of cells with varied (i)a-Si:H layer thickness(0, 1, 2, 3 ,4 nm) and 30 nm (n)nc-Si:H

4.4. Fabrication of blister-free (p^+)poly-SiO_x layer

In the previous section, blistering after annealing and large iV_{oc} drop after ITO sputtering were observed in Figure 4.9. And these two phenomena could be related. In this section, the blistering is discussed and a solution that using both LPCVD and PECVD instead of using PECVD only for amorphous layer deposition before annealing is introduced.

4.4.1. Blistering and passivation degradation

Severe blistering was observed at the boron-doped flat side of the wafers shown in Figure 4.8. As shown in Figure 4.12, it characterizes as discontinuity of the poly-SiO_X layer and has a featured diameter of around 35µm. The blistering can still be observed even after ITO sputtering and metallization.

Blistering is formed due to the high hydrogen incorporation during amorphous layer deposition using PECVD system[77]. It can be observed both in the as-deposited layer(not observed in samples in this project) and after annealing[77]. It is assumed that this happens at the tunnel oxide/(i)a-SiO_x : H interface. During a-Si:H deposition in PECVD a large amount hydrogen is incorporated in the deposited layer. This would lead to the formation of H_2 molecules which would accumulate at the interface. Thus the a-Si:H adhesion ability to the SiO_x surface is reduced[77][86]. Obviously, in the blister region, the as-deposited a-SiO_x:H is not well bonded with the tunnel oxide layer. During the annealing at 850°CH would effuse thermally and as a result, these parts would fall off[86].

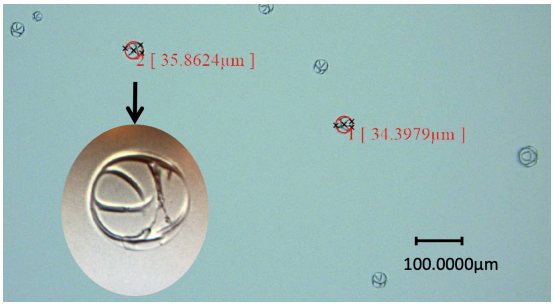

Figure 4.12: Blistering phenomena observed on the FBC precursor flat rear side(p^+)poly-SiO_x after annealing

In the FBC cells shown in Figure 4.8, the ITO layer is in contact with (n^+)poly-SiO_x on the front side and with (p^+)poly-SiO_x/(n)nc-Si:H on the rear side. In the front side textured precursors, the iV_{oc} dropped drastically (30 ~40 mV drop) after ITO sputtering as shown in 4.9. It was reported that the passivation degradation is larger when ITO is as-deposited on a thinner (10 nm comparing to 14 and 24 nm) poly-Si layer[87]. However, if we increase the thickness of poly-SiO_x,he blistering phenomena becomes worse. This is because a thicker deposited layer would enhance the blistering effect[88]. Normally, passivation degradation due to ITO sputtering damage can be recovered by annealing or curing[89]. For the tunnel oxide/poly-Si passivating contacts, a relatively high post-annealing temperature (250°C~350°C[89]) is required. However, this rather high annealing temperature is detrimental for the amorphous or nonocrystalline silicon layer[90]

as well as the c-Si:H/(i)a-Si:H passivation[78](not in the previous introduced FBC cells). Large density of defects can already start to form within a-Si:H if annealed at low temperature of 200°C[78][90]. The annealing process would break the Si-H bond and leads to H effusion and thus degrades the passivation quality[91].

It was also found that when ITO is sputtered either only on the front side or on the rear side, the passivation degrades significantly(textured front side:(n^+)poly-SiO_x, flat rear side: (p^+)poly-SiO_x/(i)a-Si:H/(n)nc-Si:H). So, the precursor iV_{oc} drop is not caused by the material difference of the layer in contact with ITO. Thus, post-annealing at high temperature above 200°Cobviously is not applicable here in this thesis as amorphous or nanocrystalline silicon layers are also deposited. And it is believed that the main passivation degradation is caused by the inhomogeneous surface due to blistering effect. At the blistering region where the surface is ruptured, a path is created for ITO or metal to diffuse into the poly-SiO_x layer and introduce recombination centers[92]. As mentioned above the blistering can still be observed after metallization(1µm). It is reasonable to consider that at the blistering region ITO is sputtered on a much thinner layer or even in contact with the c-Si bulk. Thus, the sputtering damage is much more severe.

4.4.2. Blistering elimination

It is possible to reduce blistering by increasing the H_2 to SiH_4 ratio[77]. When a higher ratio is applied, the deposition rate decreases and the slow deposition rate allows the hydrogen to diffuse away from the interface during deposition[77]. It is also possible to reduce the hydrogen incorporation during deposition by increasing substrate temperature[86][93]. At higher deposition temperature, a-Si:H with lower hydrogen concentration can be obtained[93]. Another possible solution is to decrease the temperature ramping rate during annealing and use a lower initial temperature[86][93].

The intrinsic and doped a-SiO_x : H layers (before annealing) in all the cells presented in the previous section were only deposited in the PECVD system *AMOR* using a two steps method. The details of the recipe are listed in table 4.2. First, a 10 nm intrinsic layer is deposited on the tunneling oxide and secondly another 10 nm doped layer is deposited bwith additional B_2H_6. The H_2 to SiH_4 ratio is around 12.5. The annealing step starts from an initial temperature of 600°C and has a ramp rate of 10°C/min.

Table 4.2: Recipe of boron-doped a-SiO_x : H layer deposition on flat surface using PECVD *AMOR*

	System parameters			**Gas flow rate(sccm)**				
Step	Temperature (°C)	Pressure (mbar)	Power (W)	SiH_4	CO_2	B_2H_6 ($2\%H_2$)	H_2	Deposition rate (nm/min)
1	180	2	5	8	2	0	100	8
2	180	2	5	8	2	5	100	8

Another feasible solution is to replace the first step deposition of (i)a-SiO_x : H in PECVD by (i)a-Si deposition in LPCVD. Using LPCVD the hydrogen incorporation at the interface could be avoided[88][93]. The deposition conditions are listed in table 4.3. Clearly,

the deposition temperature is much higher than that using PECVD and only silane gas is supplied. The only hydrogen source is the silane decomposition. The deposition rate is also about 4 times slower comparing to that using PECVD. All these factors would facilitate hydrogen effusion during the slow deposition and avoid hydrogen incorporation.

Table 4.3: Deposition condition of a-Si on flat surface using LPCVD furnace

Temperature °C	Pressure mTorr	SiH_4 sccm	Deposition rate nm/min
570	150(0.2mbar)	45	~2

The wafers were loaded in the LPCVD furnace right after tunnel oxide growth (NAOS). Before loading in the PECVD *Amor* for another 20nm doped layer deposition the oxide layer on the wafers was removed using *Marangoni* as shown in Figure 4.1 step 4-7. The oxide layer was formed in air, especially when unloading from the LPCVD furnace. The dopants would diffuse into the intrinsic layer during annealing. In total, 30 nm (n^+)poly-SiO_x was obtained on the rear flat side and around 28 nm (p^+) poly-SiO_x on the front textured side after annealing. The precursor structure is also shown in the inset of Figure 4.13 (a). Two whole wafers (wafer1 and 2) were cut into four quarters separately to test annealing time length, while another two whole wafers (wafer3 and 4) were used to test passivation after hydrogenation and ITO sputtering. The result is shown in Figure 4.13. The optimized annealing time at 850°C is 45 minutes. Even though the deposition process is more complicated, but no blistering was found on the flat rear side. Instead of losing more than 30 mV before, here the iV_{oc} drop after ITO sputtering is limited within around 2~8 mV.

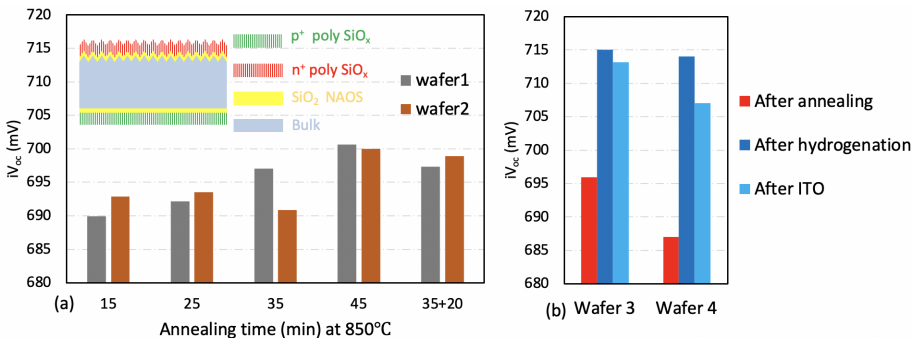

Figure 4.13: Passivation test(using both LPCVD and PECVD)(a) at different annealing time and (b) after hydrogenation and ITO sputtering (annealed for 45 minutes, at 850°C)

4.5. TRJ with (n)a-Si:H/(n)nc-Si:H in FBC cells

In the previous section, experiments proved that even adding 1nm (i)a-Si:H layer is not feasible for TRJ. In this section, hybrid FBC cells with only n-type layers (dual-n-layer (n)a-Si:H/(n)nc-Si:H) will be introduced. The cell design will be explained first and then the cell results with different (n)a-Si:H layer thickness will be presented and discussed.

4.5.1. Experiment design

Cell design The (i)a-Si:H was found not feasible in the TRJ. However, in the hybrid IBC cell, the (n)nc-Si:H should not be deposited directly on the bulk for passivation consideration. As introduced in Section 2.3.3, it is also possible to passivate the surface by (n)a-Si:H directly[51]. In this case, the precursor iV_{oc} would be lower than that with an (i)a-Si:H buffer layer, but a high FF can still be expected[54]. In the FBC cells, the (n)a-Si:H was deposited on the p^+ SiO_x : H. So unlike in IBC cells, such V_{oc} drop would not be observed clearly in FBC cells.

The fabrication process of a dual-n-layers FBC cell is shown in Figure 4.1.In total 5 FBC cells were made to find out the influence of (n)a-Si:H thickness on cell performance. As shown in Figure 4.14, there was one reference cell without any extra layers and four cells with varying (n)a-Si:H layer thickness.

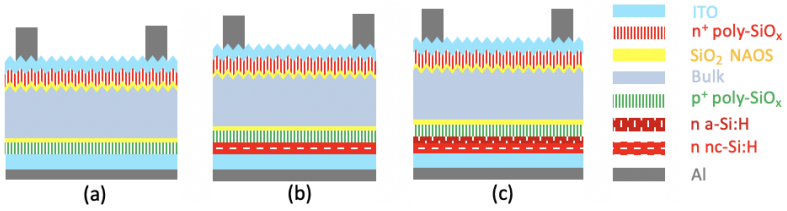

Figure 4.14: Solar cell sketches for (a)Reference cell (b) with only (n)nc-Si:H (c) with (n)a-Si:H/(n)nc-Si:H

The amorphous layers before annealing were deposited using both LPCVD and PECVD as introduced in Section 4.4.2 and had a total thickness of 30 nm. The thicknesses of all the layers in the FBC cells are listed in table 4.4.

Table 4.4: Thickness values of the layers in FBC cells with dual-n-layer

	Front side(textured)			Rear side(flat)		
n a-Si:H	Al	ITO	(n^+)poly-SiO_x	(p^+)poly-SiO_x	ITO	Al
0,3,4,5nm	1.8µm	75nm	28nm	30nm	150nm	1µm

Another set of masks was used in this experiment and a finished wafer is shown in Figure 4.15. These masks consist of six dies of same area, among which three have the same metal coverage. Comparing to the previous introduced 15-die mask, the advantage is to have three identical cells (die1,2,3) on one wafer which is beneficial for result analysis. But results were obtained on a smaller die (3.937cm^2).

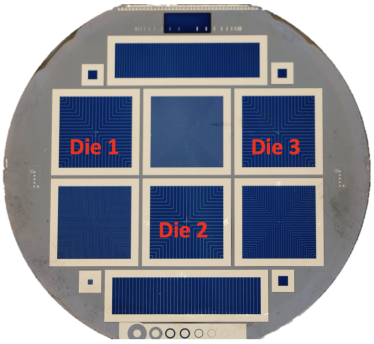

Figure 4.15: The front side layout design of the FBC cells with 6 solar cell dies

Metal finger height limitation A reference cell as shown in figure 4.14 (a) was fabricated with an Al metal grid height of 1.2 µm. Figure 4.16 shows the FF variation versus front side metal coverage. It can be seen that with 1.2 µm thick Al, the FF obviously increases a lot with the metal coverage.This means that the metal grid height is limiting the FF.

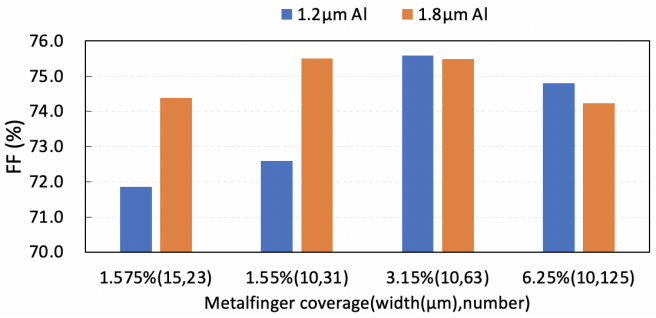

Figure 4.16: Influence of metal finger size on the cell fill factor

To minimise the influence from metal grid height, the metal grid height was increased to 1.8 µm (corresponding to 3 µm on flat surface). And as shown in figure 4.16, with 1.8 µm Al the FF still varies between different die but much less than that with 1.2 µm Al. It is possible to further reduce the influence from the grid height, however a too thick Al layer would cause problems to the lift-off step of metallization. Because a very thick photoresist coating would be required and it would be more difficult to have an unbroken metal grid. For all the FBC cells introduced later, the front grid Al thickness is 1.8 µm.

Cell precursor passivation quality It was found that using PH_3 flow rate of 0.2sccm a higher FF can be obtained, but still the PH_3 flow rate was set at 1.2sccm during (n)nc-Si:H deposition in this experiment. This is because the group has more experience of (n)nc-Si:H deposited at 1.2 sccm PH_3 flow rate. The precursor passivation quality was

checked at several fabrication steps during the fabrication and the iV_{oc} values are shown in Figure 4.17. The measured iV_{oc} of all precursors after annealing were around 695mV which is much higher than that shown in Figure 4.9 (around 676mV). And a much better uniformity between different wafers was obtained. The passivation degradation after ITO sputtering was also much smaller. The increased passivation quality mainly benefits from a thicker poly-SiO_x layer and the elimination of blistering as discussed in Section 4.4.2.

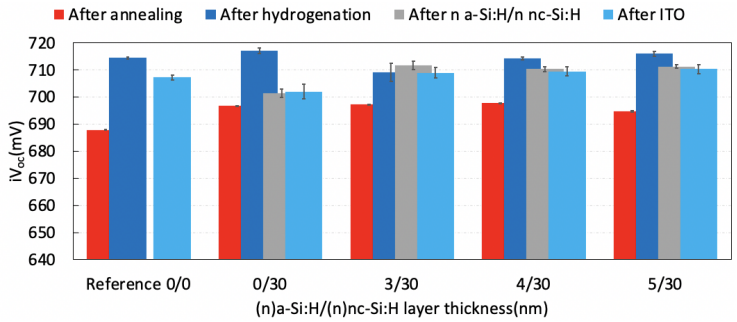

Figure 4.17: FBC cell precursors passivation quality with dual-n-layer

4.5.2. FBC cells with with (n)a-Si:H/(n)nc-Si:H performance comparison

Figure 4.18 shows the band diagram with TRJ (p^+)poly-SiO_x/(n)a-Si:H/(n)nc-Si:H. The tunnel barrier at the TRJ should be smaller than that with (i)a-Si:H. It was already proved that the cell would still work if only a (n)a-Si:H or (n)nc-Si:H layer is deposited in FBC cells, even though the FF would decrease as compared to the reference cell without TRJ. The FF decrease in the case with (n)a-Si:H was large and in the case with (n)nc-Si:H was quiet small. Based on those results, it can be predicted that the (p^+)poly-SiO_x/(n)a-Si:H/(n)nc-Si:H TRJ would be working and the (n)a-Si:H layer thickness should have an influence.

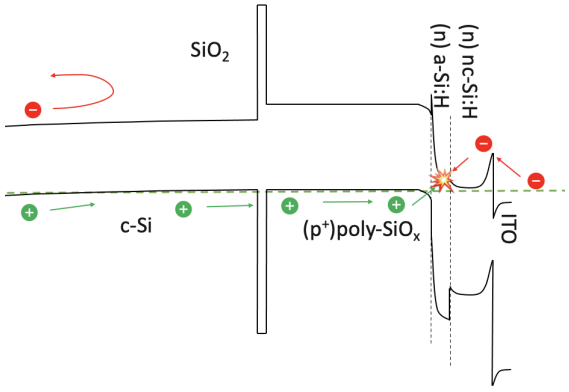

Figure 4.18: FBC cell rear side band diagram with dual-n-layer

As shown in Figure 4.19, the FF decreases with the buffer layer (n)a-Si:H thickness as shown in Figure 4.19. For cell with 3 nm (n)a-Si:H, the average FF of the die 1,3,5 is only 0.72% smaller than the reference without TRJ. However, the average FF drop is 3.6% when the (n)a-i:H layer is 5nm thick. A thinner (n)a-Si:H layer implies better tunneling efficiency as the (n)nc-Si:H layer is more close to the (p^+)poly-SiO_x layer.

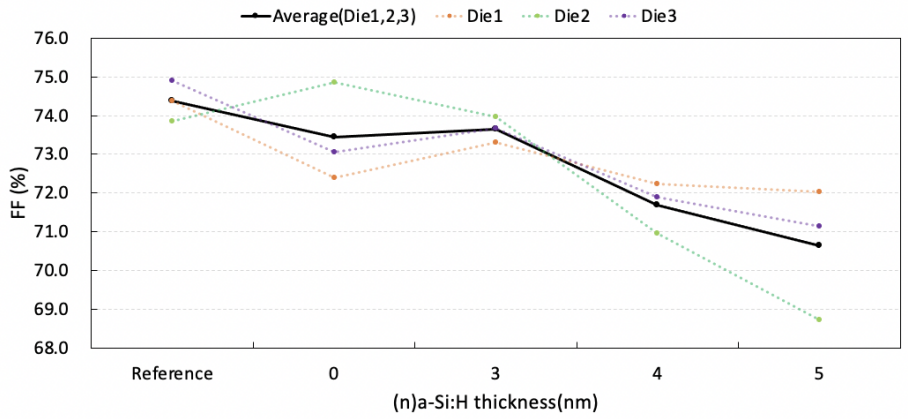

Figure 4.19: Fill factor as a function of (n)a-Si:H thickness in FBC cell with dual-n-layer

Figure 4.20 shows the V_{oc} variance of the cells. As already mentioned, as the dual-n-layer were deposited on the poly-SiO_x, the expected passivation degradation in IBC cells due to the change of (i)a-Si:H to (n)a-si:H would not be observed. The cells with 3, 4 and 5 nm (n)a-Si:H have higher V_{oc} than the reference cell without TRJ, this could be explained by the shielding of TCO influence[94] as theses cells have a thicker n layer under the ITO layer. With thinner (n)a-Si:H the TRJ depletion region width should be smaller. The V_{oc} variation has similar trend as the precursor iV_{oc} variation after ITO sputtering.

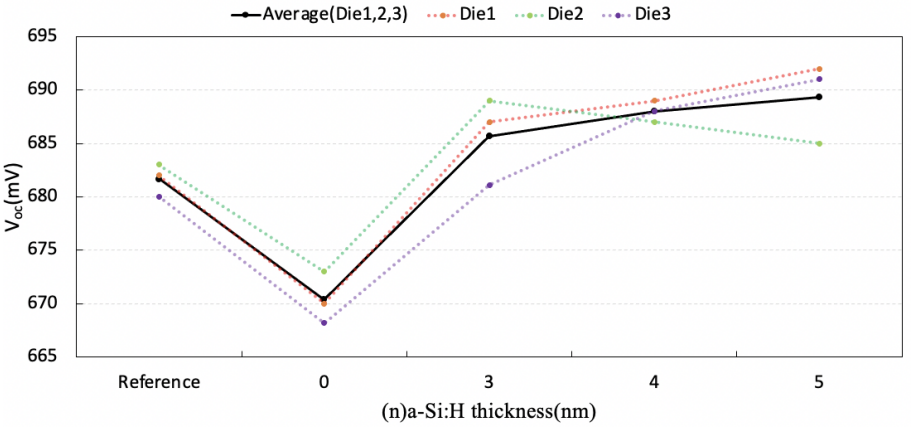

Figure 4.20: Open-circuit voltage as a function of (n)a-Si:H thickness in FBC cell with dual-n-layer

As all the dies have the same front metal coverage and ARC layer. The J_{sc} of different cell in die1,3,5 should be close. As shown in figure 4.21, the J_{sc} of all the dies are within the range 37~38.6 mA/cm^2

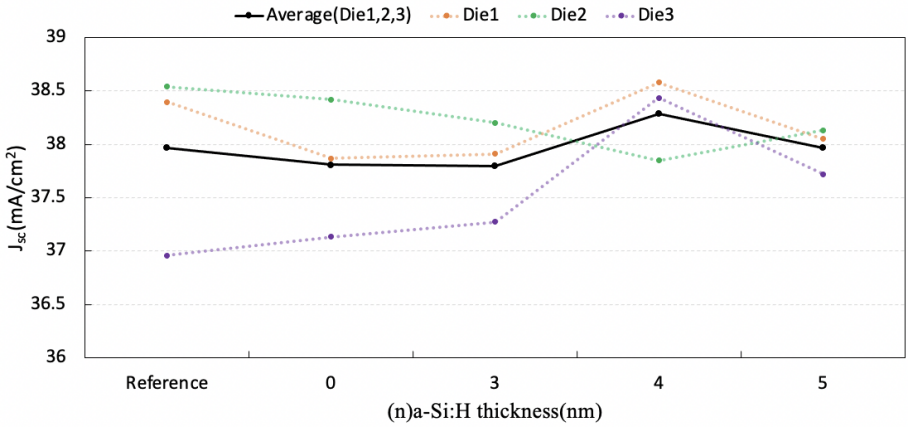

Figure 4.21: Short-circuit current density as a function of (n)a-Si:H thickness in FBC cell with dual-n-layer

Figure 4.22 shows the comparison of the J-V curves of die3 with different (n)a-Si:H layer thicknesses. It can be seen that the J-V curve of the the cell with 0 nm (n)a-Si:H, is more vertical than the others at the part more close to the V_{oc}. And the slope of this part becomes smaller with the increase of (n)a-Si:H layer thickness. This indicates that the $_{\text{series}}$ increases with the (n)a-Si:H layer thickness, which can explain the decrease of FF[6]. Such increase of R_s is due to the decrease of the tunneling efficiency at the TRJ.

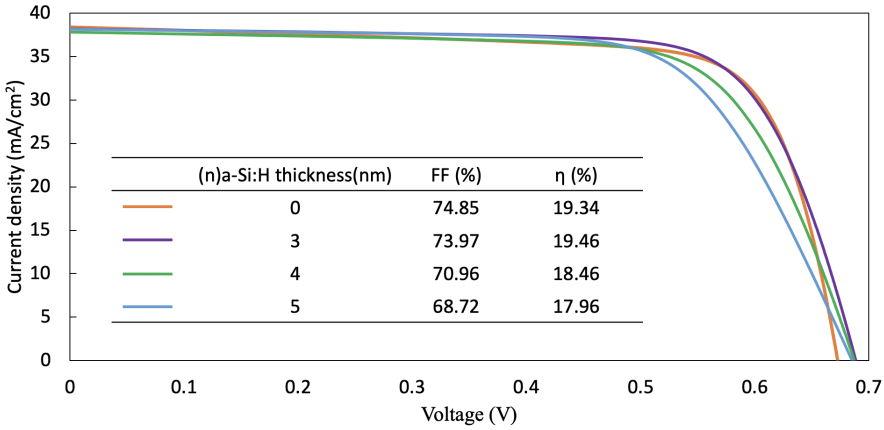

Figure 4.22: J-V curves comparison of cells with varied (n)a-Si:H layer thickness(0, 1, 2, 3, 4 nm) and 30 nm (n)nc-Si:H(Die3)

5

HYBRID IBC SOLAR CELLS DEMONSTRATION

The TRJ was proved working with the (n)a-Si:H/(n)nc-Si:H layers in the Chapter 4. In this chapter, firstly the dual-n-layer passivation quality was tested with the symmetrical passivation structure. And then the structure was applied to the IBC cells. Two different emitter materials, (p^+)poly-SiO_x and (p^+)poly-Si, were compared on device level. Besides, IBC cells with different (n)a-Si:H and (n)nc-Si:H layer thickness will also be compared. At last the influence of pitch width of IBC cells will be discussed.

5.1. Dual-n-layer BSF passivation test

As in the BSF area, the c-Si surface is passivated by the dual-n-layer directly, its passivation quality should be tested first. In Section 2.3.3, the passivation quality of doped a-Si:H layer is discussed[51]. The passivation test was conducted on both textured and flat symmetrical samples shown in Figure 5.1

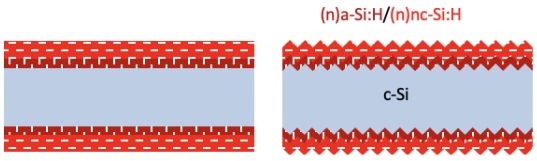

Figure 5.1: Dual-n-layer symmetrical samples

The passivation test result is shown in Figure 5.2. With the increase of (n)a-Si:H layer thickness, the measured iV_{oc} decreases on textured surface and increases on flat surface. More importantly, the iV_{oc} is higher for thin (n)a-Si:H (1~8 nm) for textured surface as compared to that for flat surface. Generally, the textured <1 1 1> surface is easier to passivate than <1 0 0> surface. Because at the <1 1 1> surface, each Silicon atom only has one dangling bond instead of two at <1 0 0> surface[95]. The observed decrease of

passivation quality for textured surface could be that the better field-effect passivation of (n)nc-Si:H is more shielded by the increased (n)a-Si:H thickness. For the flat surface, such decrease could be compensated by the improved chemical passivation with thicker (n)a-Si:H, and results in an increased passivation quality.

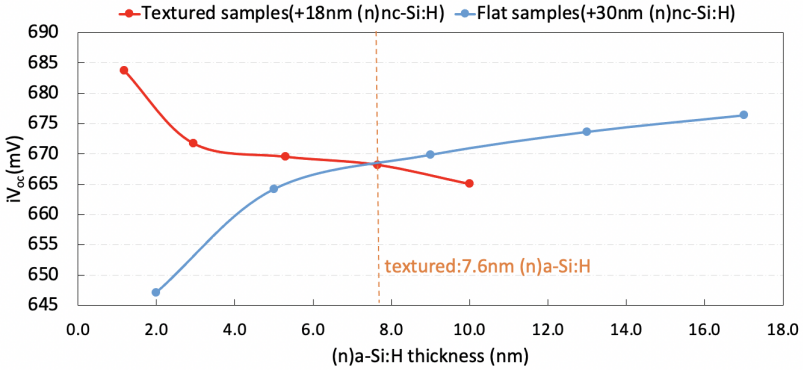

Figure 5.2: Dual-n-layer passivation quality with varied (n)a-Si:H thickness

It was proved in Section 4.5.2 that the R_{series} would increase with (n)a-Si:H thickness and leads to FF decrease. Therefore, in the IBC cells, the BSF side would be textured and the (n)a-Si:H layer thickness was picked from the range 1~8 nm (corresponding to 2~13 nm on flat surface). It was expected to have both high FF and V_{oc} with a thin (n)a-Si:H layer.

Hydrogen plasma treatment (HPT) before (n)nc-Si:H deposition was reported to be beneficial for passivation as the hydrogen can diffuse into the film and saturate the dangling bonds.[96][97]. During HPT, the a-Si:H layer is being etched[98][99]. The active hydrogen atoms in plasma would react with the material and replace it with volatile hydrogen compounds[98]. Then the film would be etched. Figure 5.3 shows the HPT influence. The HPT was applied between (n)a-Si:H and (n)nc-Si:H deposition. HPT also facilitates (n)nc-Si:H crystalline phase growth[58]. The passivation was optimized at 60s in symmetrical samples with 1.2/18 nm (n)a-Si:H/(n)nc-Si:H.Figure 5.3 (a) shows that with 1.2/18 nm (n)a-Si:H/(n)nc-Si:H the passivation optimizes at 60s HPT.

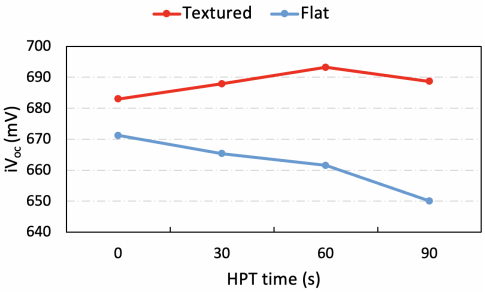

Figure 5.3: Dual-n-layer passivation test with varied HPT time (1.2/18 nm (n)a-Si:H/ (n)nc-Si:H)

5.2. IBC cell fabrication process and rear side layout

In this section, the fabrication process of a poly-Si/SHJ hybrid IBC cell is explained. All the dual-n-layer thickness in the following sections means the thickness on textured BSF.

5.2.1. Hybrid IBC cells fabrication flowchart

The fabrication flowchart is briefly shown in Figure 5.4.

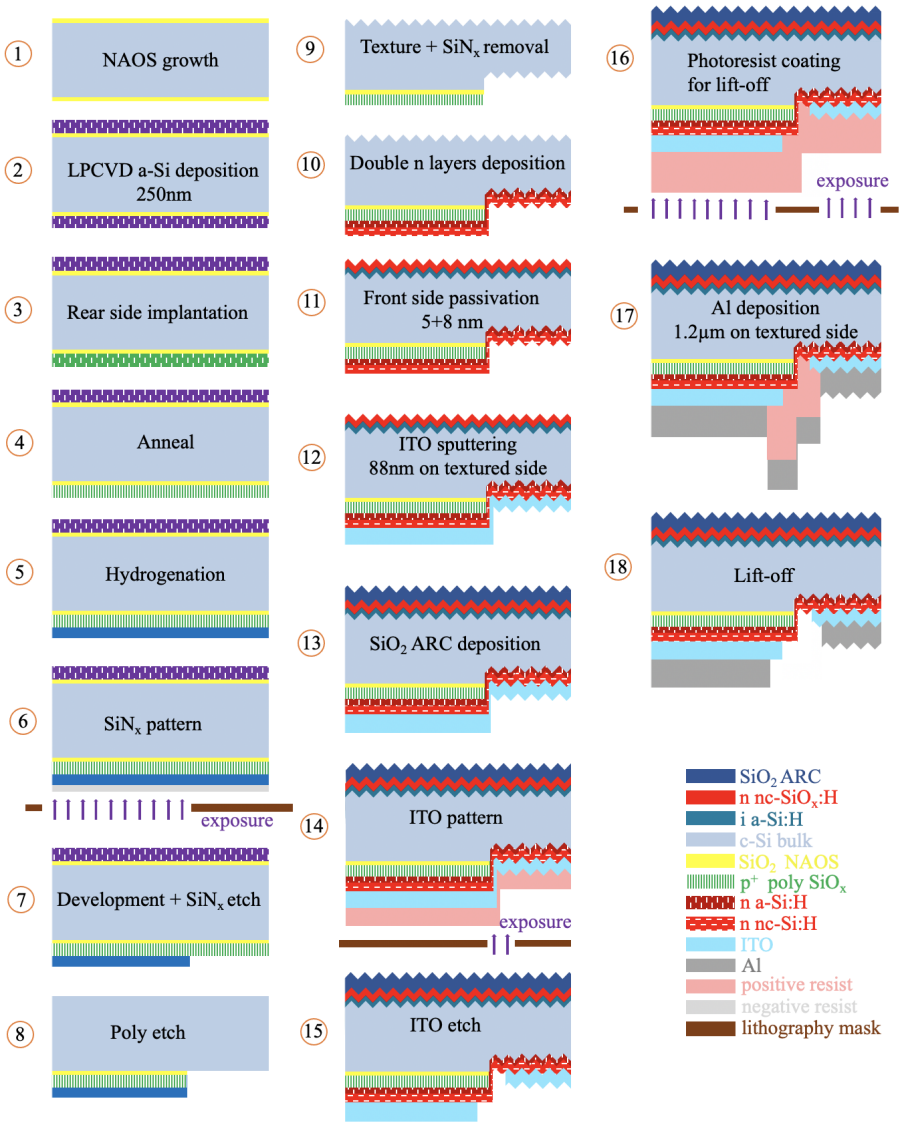

Figure 5.4: Poly-Si/SHJ hybrid IBC cell fabrication process flow chart

Starting with a n-type wafer, the native oxide was first removed using *Marangoni*. (1) And then the wafer was immediately submerged in 69% HNO_3 for an hour at room temperature to grow the tunnel oxide layer (NAOS). Right after the NAOS step, the wafer was rinsed, dried and loaded in the LPCVD furnace for 250 nm a-Si deposition. (2) The deposition was on both sides. Then the rear side was boron-implanted and annealed at 950°C. After annealing the implanted layer would crystallize to (p^+)poly-Si as shown in Figure 5.4 step 3~4.

Then the wafer was loaded in PECVD *Nouvellus* system for SiN_x deposition. The SiN_x served as a capping layer for hydrogenation as well as a mask layer for poly-Si etch in later steps. The hydrogenation step (5) also included 30 minutes forming gas annealing at 400°C after SiN_x deposition. (6~7) In order to etch away the (p^+)poly-Si in the dedicated BSF region, the SiN_x was patterned. A 2 µm negative photoresist nLOF^{TM}2020 was coated on the rear side. The mask is opened in emitter region. After exposure and development the photoresist in the the emitter region was kept. Then the uncovered SiN_x in the BSF region would be etched away in BHF1:7. And then the remaining photoresist was removed by plasma using *Tepla*. After that the front side a-Si and the rear side uncovered (p^+)poly-Si were etched away in poly-etch solution (40%HF:69%HNO_3=1:40) as shown in step 8.

After the poly-etch step, the front side and the BSF area were textured. The wafer was immersed in a preheated mixed solution (80°C) of 1 L TMAH and 4L DI water with 120 ml ALKA-TEX.8 as additive. (9) After texturing, the wafer was cleaned and the rest SiN_x was etched away. After that the wafer was cleaned twice with 4 minutes 0.55%HF etch in-between. Right before loading in the PECVD system *Amigo*, the oxide layer (chemically grown after cleaning) was removed using *Marongoni*. The dual-n-layer were first deposited on the rear side as shown in step 10. And then the wafer was flipped. (11) Then the 5/8 nm (i)a-Si:H/(n)nc-SiO_x layers were deposited on the front side to passivate the c-Si front surface. (12) After deposition in *Amigo*, a 150 nm (on flat emitter:150 nm, on textured BSF: 88 nm) ITO layer was sputtered on the rear side at room temperature. Then the wafer was annealed at 180°C in air for around 10 minutes to recover the sputtering introduced passivation loss. (13) And then 110nm SiO_2 was deposited using e-beam system *Provac* as ARC layer.

In step 14~15, the ITO layer was patterned. A 4 µm AZ ECI3027 positive resist was coated on the rear side. The ITO pattern mask is opened at the finger gap. After development, the ITO at the gap was etched away in 37% HCl. Then the resist was removed in acetone. (16) After that, 3 layers of 4µm AZ ECI3027 positive resist were coated at the rear side. A photomask which is opened at the area dedicated for metal finger was used for exposure. After development, the wafer was loaded in *Provac* for Aluminum deposition (2 µm on flat emitter and 1.2 µm on textured BSF). At last, the undesired aluminum was lifted off in acetone.

5.2.2. IBC cell rear layout

The Figure 5.5 shows the rear side of a finished IBC cell. Masks with 7 dies were used which are respectively named as A1, A2, A3, B1,B2, C1, C2.

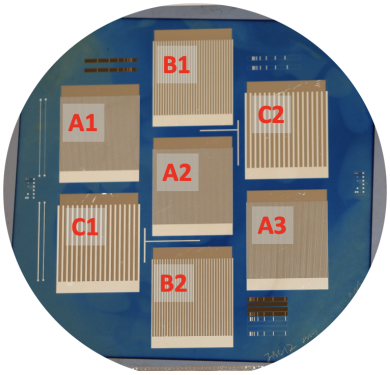

Figure 5.5: The rear side layout design of the IBC cells

Figure 5.6 shows the picture of the fingers under microscope. The gap between the adjacent emitter and BSF metal finger is about 40 µm. On each side 10 µm width is covered with ITO. On the left of the flat and textured area dividing line, it is (p^+)poly-Si/(n)a-Si:H/(n)nc-Si:H and on the right side it is only the dual-n-layer.

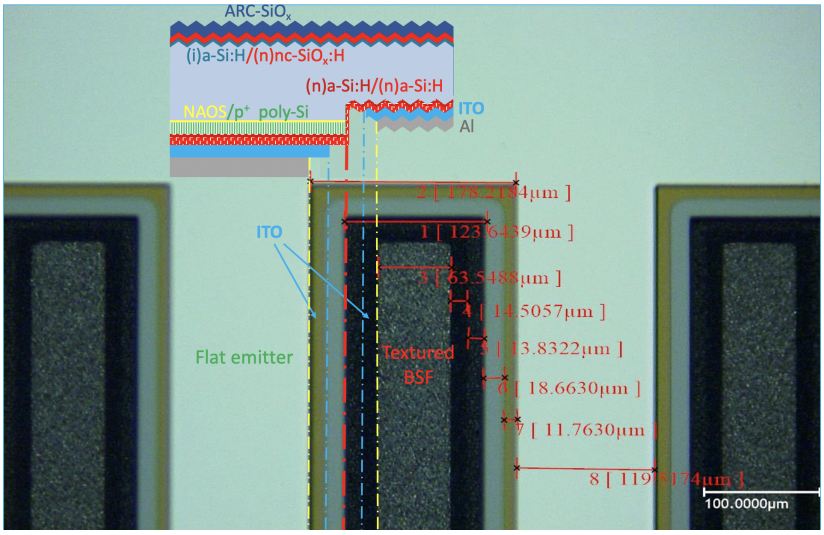

Figure 5.6: IBC cell finger structure under microscope (Die A2)

The dies' geometrical parameters are listed in Table 5.1. Dies with the same letter in the name are identical but located at different position on the wafer. Dies with different letter in name have different pitch width (A < B < C). But the emitter to the pitch width ratio is kept at around 60% in all dies.

Table 5.1: Different dies finger size

Die	A	B	C
Pitch (µm)	300	650	1200
Emitter width (µm)	160	370	700
BSF width (µm)	100	240	460
Emitter finger number	67	31	17
Cell area (cm^2)	4.04	4.09	4.18

5.3. (p^+)poly-SiO_x and (p^+)poly-Si comparison

The passivation quality and the sheet resistance R_{sheet} of (p^+)poly-SiO_x and (p^+)poly-Si were measured. The τ_{eff} and iV_{oc} were measured with symmetrical samples (after hydrogenation, and the τ_{eff} was measured at minority carrier density of $10^{15}/cm^{-3}$). Results shows that poly-SiO_x has a better passivation quality but a much higher R_{sheet}.

Table 5.2: (p^+)poly-SiO_x and (p^+)poly-Si material proprieties comparison

	thickness (nm)	carrier lifetime (ms)	iV_{oc} (mV)	sheet resistance (Ω/sqr)
(p^+)poly-SiO_x	30	3.2	708	790
(p^+)poly-Si	250	2.5	701	137

Two IBC cells with 1.2/18 nm (n)a-Si:H/(n)nc-Si:H and different emitter p-type layer materials were made. Figure 5.7 shows that the cell with poly-Si has both higher V_{oc} and FF. It should be pointed out that the process flow in Figure 5.4 is for IBC with poly-Si. And the cell precursors were all fabricated in *EKL CR100* where the contamination is better controlled. Instead, the poly-SiO_x precursor was fabricated in *EKL CR10000*. When it involves chemical process, such as steps 7 and 8 in Figure 5.4, contaminated containers were used. This could result in the low V_{oc} of poly-SiO_x hybrid IBC cell.

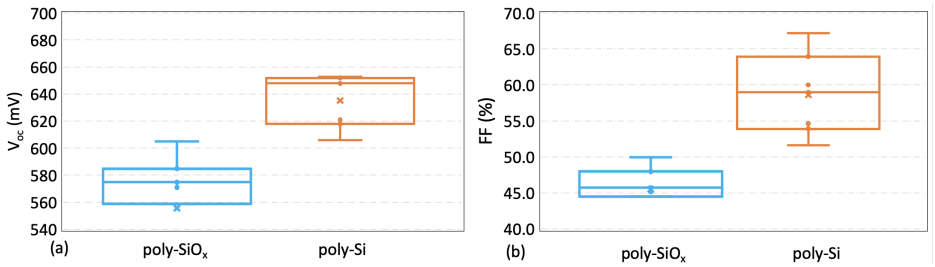

Figure 5.7: Poly-SiO_x and poly-Si hybrid IBC cell (a)V_{oc} and (b)FF comparison(cell with 1.2/18 nm (n)a-Si:H/(n)nc-Si:H)

The (p^+)poly-Si/SHJ hybrid also has a much higher FF than that with (p^+)poly-SiO_x as shown in Figure 5.7(b). This is because (p^+)poly-Si is more conductive than (p^+)poly-

SiO_x. The R_{sheet} of (p^+)poly-SiO_x is about as 5.6 times large as that of (p^+)poly-Si. By comparing the part more close to V_{oc} in Figure 5.8, it can also be found that the cell with poly-Si emitter has a lower R_{series}. The J_{sc} difference is small and the poly-Si/SHJ hybrid IBC has a much higher efficiency.

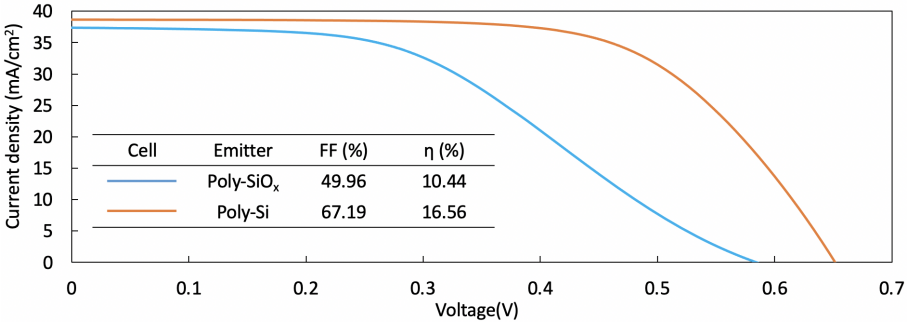

Figure 5.8: Poly-SiO_x and poly-Si/SHJ hybrid IBC cells JV curves comparison (Die C1)

Since IBC cell with poly-Si emitter has a better performance, only poly-Si/SHJ hybrid IBC cells would be fabricated for further experiments.

5.4. Dual-n-layer thickness influence

In this section, the measured external parameters (mainly V_{oc} and FF) of poly-Si/SHJ hybrid IBC cells with different (n)a-Si:H/(n)nc-Si:H layer thickness are presented and discussed.

5.4.1. (n)a-Si:H layer thickness influence

As shown in Figure 5.2, the dual-n-layer passivation quality for textured surface is better than that for flat surface in the (n)a-Si:H thickness range 1~8 nm. The performance of the poly-Si/SHJ hybrid cell with respectively 0, 1.2, 3, 5.3, 7.6 nm (n)a-Si:H and 18 nm (n)nc-Si:H were compared. Figure 5.9 shows the measured V_{oc} and FF. In the figure it is divided into two parts with (n)a-Si:H thinner and thicker than 3 nm.

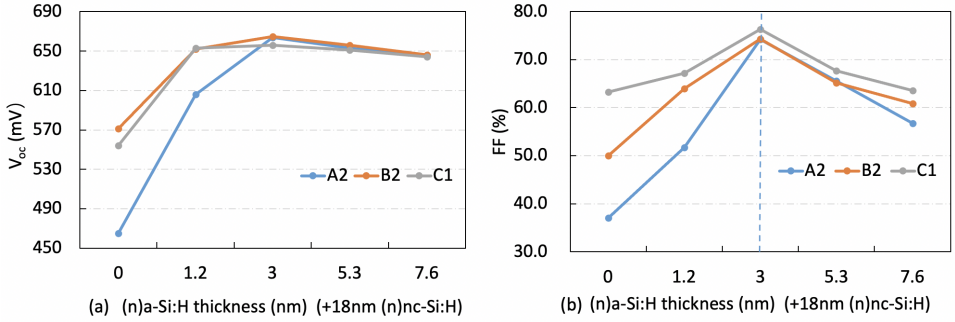

Figure 5.9: Poly-Si/SHJ hybrid IBC cell (a)V_{oc} and (b)FF as a function of (n)a-Si:H thickness

(n)a-Si:H thickness range 0~3 nm Figure 5.9 (a) shows that the V_{oc} increases rapidly with (n)a-Si:H from 0 to 3 nm and then decreases slowly. In this (n)a-Si:H thickness range, the FF also increases. The analysis of V_{oc} and FF change versus (n)a-Si:H thickness is supported by comparing the JV curves. Figure 5.10 shows the measured JV curves of cell with respectively 0, 1.2 and 3 nm (Die C1).

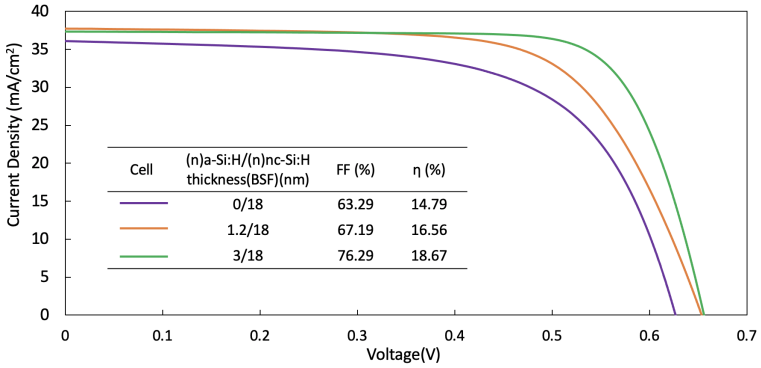

Figure 5.10: Poly-Si/SHJ hybrid IBC cell JV curves with varied (n)a-Si:H thickness (0, 1.2, 3 nm) and 18 nm (n)nc-Si:H (Die C1)

The cell with only (n)nc-Si:H has a much lower V_{oc}. This is due to the poor passivation quality and the severe shunting loss. It can be seen very clearly from the curves that the slope of the part close to J_{sc}inclines more with the decrease of (n)a-Si:H, which means that the R_{shunt} decreases. Low R_{shunt} would provide the current an alternate flow path, which leads to drop of FF and V_{oc}[6]. This could explain the increases of the V_{oc} and FF with (n)a-Si:H thickness from 0 to 3nm. It can also be seen in Figure 5.9(a)that the increase of V_{oc} in die A2 is largest. This is because this die has more shunting paths, and thus the shunt influence is more significant. The performance in different die will be discussed more in Section 5.5. So, from the hybrid IBC cell device level analysis, a (n)a-Si:H with a certain thickness is necessary.

(n)a-Si:H thickness range 3~7.6 nm However, a thicker (n)a-Si:H is not necessarily the better. As it can be seen in Figure 5.9 (b)when the (n)a-Si:H layer thickness is higher than 3 nm, the FF decreases. And the V_{oc} decreases slightly. The V_{oc} change in this (n)a-Si:H thickness range corresponds to the decrease of dual-n-layer passivation quality as shown in Figure 5.2. The JV curves in Figure 5.11 shows that the three cells all have sufficient R_{shunt}. But the R_{series} increases clearly with the (n)a-Si:H thickness. This corresponds to the results in Section 4.5.2. Increasing (n)a-Si:H thickness would lead to the decrease of TRJ tunnel efficiency.

In conclusion, when (n)nc-Si:H thickness is fixed (18 nm in this section), it is necessary to have a (n)a-Si:H layer to ensure a high R_{shunt}. But a too thick (n)a-Si:H layer would decrease the FF largely due to R_{series} increase, and also decreases the V_{oc} slightly. The dual-n-layer can be considered that several nanometers of the (n)nc-Si:H is replaced by (n)a-Si:H for better passivation quality and higher R_{shunt}.

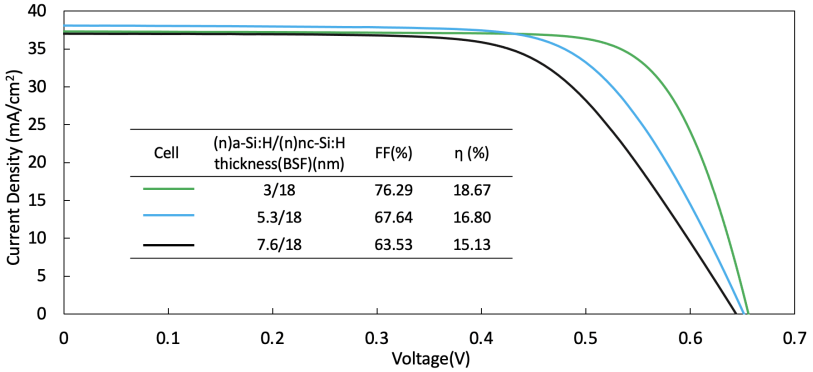

Figure 5.11: Poly-Si/SHJ hybrid IBC cell JV curves with varied (n)a-Si:H thickness(3, 5.3, 7.6nm) and 18nm (n)nc-Si:H(Die C1)

5.4.2. (n)nc-Si:H thickness influence

Cells showing low R_{shunt} In cells with low R_{shunt}, the FF is lower than expected, such as in Cell with 1.2/18 nm (n)a-Si:H/(n)nc-Si:H. Comparing to (n)a-Si:H, (n)nc-Si:H is more conductive as shown in Table 4.1. And the (n)nc-Si:H layer connects the emitter and BSF which makes it the major shunting path. As discussed in Section 2.4, the (n)nc-Si:H layer conductivity increases with its thickness because of the increasing crystallinity[17]. So, it is logical to reduce the (n)nc-Si:H layer thickness if the R_{shunt} is too low. As shown in Figure 5.3, 1.2 nm(n)a-Si:H/60s HPT/18 nm (n)nc-Si:H provides the best passivation quality. And the (n) a-Si:H is also thin which means the TRJ is also efficient. Figure 5.12 shows the JV curves of hybrid IBC cell with 1.2 nm (n)a-Si:H/60s HPT and varied thickness of (n)nc-Si:H (6, 12, 18 nm). The difference comparing to previous introduced IBC cells here is that the HPT was applied.

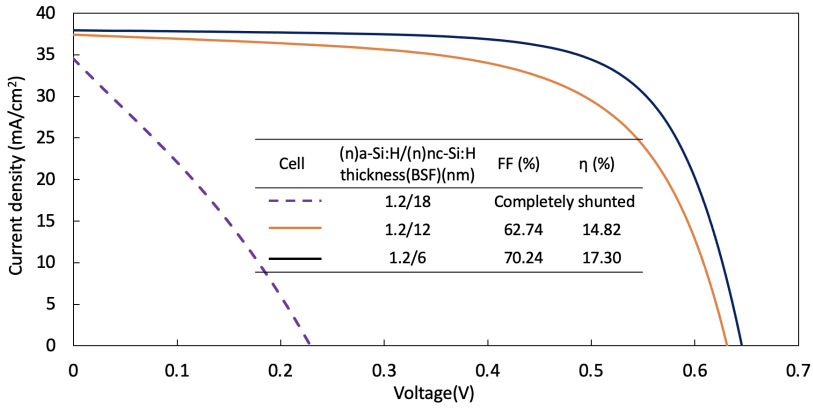

Figure 5.12: Poly-Si/SHJ hybrid IBC cell JV curves with 1.2 nm (n)a-Si:H/60s HPT and varied (n)nc-Si:H thickness (6, 12, 18 nm)(Die C1)

In Figure 5.10, the cell with 1.2/18 nm has a FF of 67.19. However, if HPT was applied, the cell with 1.2 nm (n)a-Si:H/60s HPT/18 nm (n)nc-Si:H is completely shunted in Figure 5.12. During the hydrogen plasma treatment, the (n)a-Si:H is being etched. And HPT would also facilitate the crystalline phase growth of (n)nc-Si:H[58]. So, here the (n)a-Si:H layer is thinner than 1.2 nm and the 18 nm (n)nc-Si:H should be more conductive than that without HPT. By decreasing the (n)nc-Si:H thickness to 12 nm, the cell is working. But still, it can be seen from the JV curve the R_{shunt} is low. Further, decrease of (n)nc-Si:H thickness to 6 nm leads to further increase of R_{shunt} and the FF increases.

Cells showing high R_{shunt} In cells with high R_{shunt}, the FF limitation form shunting is small. And thus, the effect of decreasing (n)nc-Si:H thickness on R_{shunt} should be limited. Figure 5.13shows the J-V curves of poly-Si/hybrid IBC cells with 5.3 nm (a)-Si:H and two different (n)nc-Si:H thickness (18, 12 nm). By reducing the (n)nc-Si:H thickness, the contributed R_{series} of the (n)nc-Si:H layer itself in the cell could decrease if the layer crystallinity is not decreased too much.

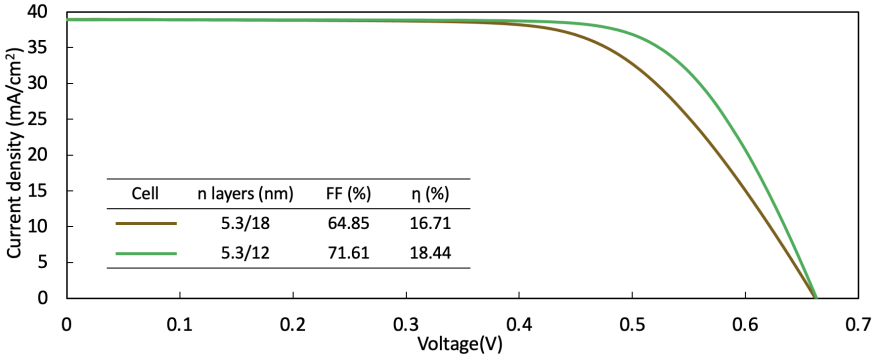

Figure 5.13: Poly-Si/SHJ hybrid IBC cell JV curves with 5.3nm (n)a-Si:H and varied (n)nc-Si:H thickness (18, 12 nm)(Die C1)

Figure 5.13 shows that the cell (5.3 nm (a)a-Si:H) R_{series} decreases by reducing the (n)nc-Si:H thickness from 18 to 12 nm. But the thickness should not be overly reduced. Because when the (n)nc-Si:H is too thin, the doping efficiency would be low and the layer electrical property would be largely degraded. And also when the (n)nc-Si:H layer is too thin, the TCO effect due to work function mismatch should be more severe and the FF would decrease[94].

To conclude, it is possible to improve the cell performance by optimising the (n)nc-Si:H layer thickness.

5.4.3. Necessity of (n)nc-Si:H

From the previous section, it was found that it is beneficial to decrease the (n)nc-Si:H layer thickness. It is logical to question the necessity of depositing (n)nc-Si:H. In the Chapter 4, it was already found that the FF deviates a lot from the reference cell if a

pure (n)a-Si:H layer is deposited(figure 4.6). In this experiment, three cells were made to investigate (n)nc-Si:H layer's necessity in hybrid IBC cells: a reference IBC cell with only 10nm(n)a-Si:H, a cell with extra 18nm (n)nc-Si:H and the third one with extra 18nm (n)a-Si:H. As shown in Figure 5.14, by comparing the reference cell and the other two cells, the reference cell has lower FF. The cell with 10/18nm (n)a-Si:H/(n)nc-Si:H has the highest FF as shown in Figure 5.14.

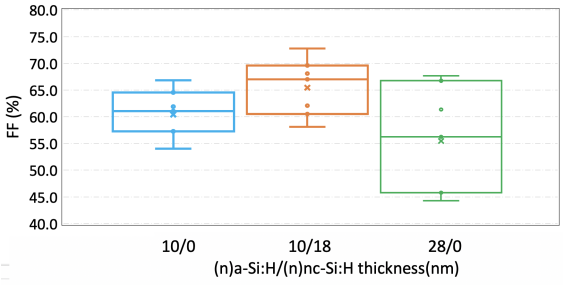

Figure 5.14: FF comparison of cells with 10 nm (n)a-Si:H + 0, 18 nm (n)nc-Si:H and 18 nm (n)a-Si:H

By adding an extra (n)a-Si:H or (n)nc-Si:H layer, the TCO effect would be better shielded, and thus a higher FF could be obtained[94]. As (n)nc-Si:H has a lower activation energy, comparing to adding (n)a-Si:H, the band bending is larger and the cell R_{series} is smaller. It can be concluded that to have a good electrical property, it is necessary to keep this dual-n-layer structure. The comparison in this subsection provides another perspective to understand the dual-n-layer. It can also be considered that a large part of the (n)a-Si:H is replaced by the (n)nc-Si:H to obtain a higher FF.

5.5. Pitch width influence

From die A to B to C, the pitch width increases. As a result, the number of fingers and gaps decreases. It was found that the die pitch width also influences the external parameters especially the FF and J_{sc}.

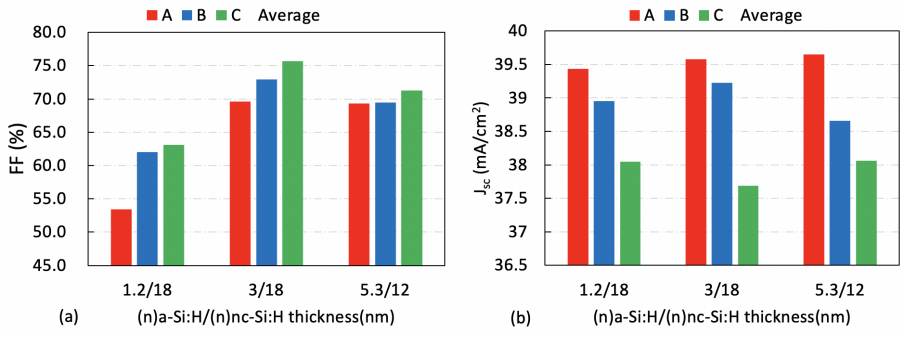

Figure 5.15: The influence of IBC cell rear pitch width design, see Table 5.1, on the cell (a)FF (b)J_{sc}. The values of each bar are the average of the identical dies with the same letter.

5.5.1. Pitch width influence on FF

From Figure 5.15 (a), it can be seen that the FF increases with the pitch width. This is because that the die with a larger pitch width has fewer finger gaps, that is, less shunting paths. It was shown in Figure 5.9, the FF difference between dies decreases with (n)a-Si:H thickness. And when the R_{shunt} is high (in Figure 5.15(a), in cell with 5.3/12 nm (n)a-Si:H/(n)nc-Si:H) the FF variation between different dies is rather small. J-V curves in Figure 5.16 shows that die A3 clearly has a lower R_{shunt}. From die A3 to die C1, the FF has increased by 5.4%. The die C1 with 3/18 nm (n)a-Si:H/(n)nc-Si:H is the highest FF obtained among all the cells made in this project.

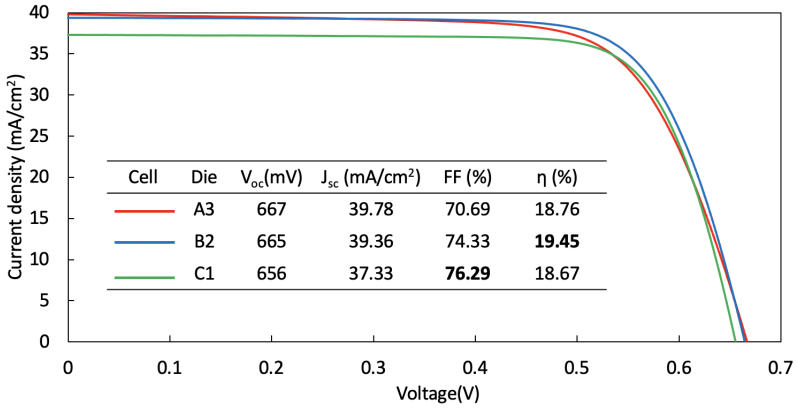

Figure 5.16: IBC Cell J-V curves comparison between different dies (3/18 nm (n)a-Si:H/ (n)nc-Si:H)

5.5.2. Pitch width influence on short-circuit current density

The finger numbers also have an influence on J_{sc}. The J_{sc} decreases with pitch width as shown in Figure 5.15(b). It should be pointed out that the reflectance varies between different dies. This is because the offset between the wafers loaded in *Provac* and the e-beam source in the vertical direction. The ARC layer thickness increases from one side to another side (depends on the loading direction). In the wafer shown in Figure 5.5, the SiO_2 ARC layer thickness at the front side increases from the left to right (C1 < B2 < A3). From the Figure 5.17, it can be seen that the reflectance decreases from A3 to B2 to C1 in wavelength range 400 ~500 nm. And it is the opposite in the range 700 ~1000 nm. The IQE curves were calculated and plotted in Figure 3.13(b) and it decreases with pitch width.

The IQE decrease with pitch width is due to the increased electrical shading loss[100][101]. In die A, the finger density is higher as it has more fingers in a similar large die. The electrons and holes need to be transported laterally and vertically to be collected at the BSF and the emitter respectively before being recombined[101]. Otherwise, the carrier collection efficiency would be reduced. So, it can be imagined that comparing to die A, in die C the holes need to diffuse a longer path on average to be collected at the emitter. So the carrier collection efficiency would decrease with pitch width and results in lower J_{sc}.

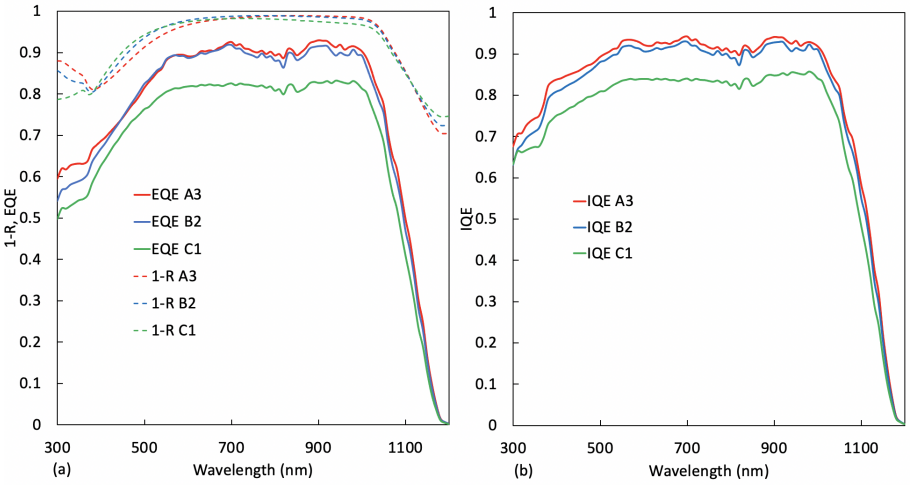

Figure 5.17: (a)1-R and EQE, (b) IQE of die A3, B2 and C1 in IBC cell with 3/18 nm (n)a-Si::H/(n)nc-Si:H

In conclusion, the FF increases (in Figure 5.15 a) with IBC cell pitch width and on the contrary the J_{sc} decreases (in Figure 5.15 b). Thus, there is a trade-off between these two external parameters versus pitch width. The best cell obtained in this thesis project is the die B2 with 3/18 nm (n)a-Si:H/(n)nc-Si:H. The cell external parameters are respectively: V_{oc} of 665 mV, J_{sc} of 39.36 mA/cm^2, FF of 74.33% and efficiency of 19.45%. The efficiencies of die A3 and C1 are lower respectively due to lower FF and lower J_{sc} as compared to die B2.

6

CONCLUSIONS AND OUTLOOKS

This thesis project is focused on the demonstration of a novel poly-Si/SHJ hybrid IBC solar cell concept, which aims to minimize the patterning steps during the cell processes, by using the tunneling recombination junction (TRJ) approach. Firstly, the TRJ concept was evaluated in an easily fabricated front-back contacted (FBC) cell, then the proof-of concept poly-Si/SHJ hybrid TRJ IBC cells were fabricated to study the influences of TRJ on the cell electrical performances. The analyses are, therefore, mainly on the cell FF and V_{oc}. With the gained understanding on the fabrication processes and the cell structure, especially, the TRJ, outlooks are given for further performance improvements of the poly-Si/SHJ hybrid IBC cell .

6.1. Conclusion

Following the goal of evaluating the TRJ for fabricating a high-efficiency poly-Si/SHJ IBC solar cell, experiments were based first on TRJ FBC cells. Different combinations of (i)a-Si:H, (n)a-Si:H and (n)nc-Si:H were used to form the TRJ with FBC cell rear emitter (p^+)poly-SiO_x. The (i)a-Si:H layer was kept in the TRJ structure for the purpose of maintaining the highest possible passivation quality of the back surface field region of the hybrid IBC solar cells. However, the dual-n-layer structure, (n)a-Si:H/(n)nc-Si:H, was proved to be the most promising TRJ structure from the carrier transport point of view, which was finally applied in the IBC cells. The detailed conclusions are given as follows.

6.1.1. TRJ proof-of concept in FBC cells

The proof-of-concept of the TRJ was conducted in FBC cells, due to the their easier fabrication processes. In this session, two parameters were evaluated: (I)The thickness of (i)a-Si:H layer in the (p^+)poly-SiO_x/(i)a-Si:H/(n)Si:H(or (n)nc-Si:H) TRJ structure; (II)The thickness of (n)a-Si:H layer in the (p^+)poly-SiO_x/(n)a-Si:H/(n)nc-Si:H TRJ structure;

First, on the thickness of (i)a-Si:H layer: TRJ structure of (p^+)poly-SiO_x/4 nm (i)a-Si:H/20 nm (n)a-Si:H was tested firstly, with which as emitter, the (i)a-Si:H/(n)a-Si:H will act as

back surface field for the potential hybrid TRJ IBC cell. It was found that the 4 nm (i)a-Si:H layer would decrease the cell FF significantly to 16.48%. Comparing to the reference cell without TRJ, in FBC cell with 0/20 nm (i)a-Si:H/(n)a-Si:H, the average FF dropped by more than 13% due to high R_{series}, which can be seen from the S-shaped J-V curve.

To improve the TRJ tunnel efficiency, the (i)a-Si:H layer thickness was reduced and the (n)a-Si:H layer was replaced by low activation energy and more conductive (n)nc-Si:H material. In addition, (n)nc-Si:H with two different doping levels were also evaluated. It was found that it is indeed beneficial to deposit (n)nc-Si:H with a lower activation energy, as the TRJ depletion region width would be smaller. Thus, it enhances the tunneling probability across the TRJ layers. However, the cell FF still keeps at a very low value (<23%) if an (i)a-Si:H layer is deposited, even for 1 nm (i)a-Si:H layer case. Obviously, the existence of (i)a-Si:H is detrimental to the device performance regarding the FF, therefore, in the second part of this section, we removed this layer.

Second, on the thickness of (n)a-Si:H layer: another combination ((n)a-Si:H/(n)nc- Si:H-dual-n-layer), as back surface field for the potential hybrid TRJ IBC cells, with different (n)a-Si:H layer thickness was also tested in the FBC structure. It was found that the TRJ (p^+)poly-SiO_x/(n)a-Si:H/(n)nc-Si:H structure works much better than the TRJ with (i)a-Si:H. on the other hand, the cell FF decreases with increasing the (n)a-Si:H thickness, which is mainly attributed to its influences on the carriers' tunneling probability. A negligible difference (0.72%) was found on the cell FFs between the reference FBC cell without TRJ and the cell with TRJ structure of (p^+)poly-SiO_x/3 nm (n)a-Si:H/30 nm (n)nc-Si:H. It proved a high-efficient carrier tunneling recombination transport at used TRJ in the FBC cell.

6.2. Proof-of-concept hybrid IBC cells

After the passivation optimization of the IBC cell's BSF region, with the optimized high-efficiency TRJ layers, the poly-Si/SHJ concept is then demonstrated in IBC cells. As the dual-n-layer was directly deposited on the c-Si surface as BSF, therefore, its passivation quality to the c-Si surface is crucial. The passivation quality is currently lower compared to the structure having an (i)a-Si:H passivation layer. It was found that the passivation quality of the dual-n-layer structure is better for textured c-Si surface than that for flat c-Si surface with 0~7.6 nm (n)a-Si:H/18 nm (n)nc-Si:H. For textured surfaces, the measured iV_{oc} decreases with increasing the (n)a-Si:H thickness. The influence of the hydrogen plasma treatment(HPT) before (n)nc-Si:H deposition was evaluated. The optimized treatment time is found to be around 60s for textured symmetrical samples with 1.2 nm (n)a-Si:H/18 nm (n)nc-Si:H as passivation layers. On the IBC cells' electrical performances: A series of conclusions can be drawn from the IBC cells results:

I. IBC cells with emitter material (p^+)poly-Si was found to have better performance than that with (p^+)poly-SiO_x because of the higher conductivity of (p^+)poly-Si.

II. In the IBC cell with dual-n-layer BSF, the R_{shunt} and R_{series} are the main impact factors on cell's performance. The conductive n-layer connects the emitter and BSF

across the finger gaps, which makes them the shunting paths. The main impact factor on R_{series} is the (n)a-Si:H thickness, which influences the TRJ tunneling probability. Therefore, the dual-n-layer influences the cell FF and V_{oc}.

III. For IBC cells with (p^+)poly-Si/dual-n-layer as emitter, because the TRJ tunneling efficiency and its passivation quality to the textured BSF region both decreases with increasing (n)a-Si:H thickness, it was expected that the IBC cell would have an excellent performance when only 1.2 nm (n)a-Si:H is deposited on the textured BSF region. However, the highest FF was obtained with 3 nm (n)a-Si:H inter layer. This is because when the (n)a-Si:H is too thin the R_{shunt} becomes too small, and thus decrease the cell FF. However, when the (n)a-Si:H is too thick, due to the increasing R_{series}(lower tunneling efficiency TRJ) the cell FF also decreases .

IV. The (n)nc-S:H layer thickness also influences the FF. The conductivity of the (n)nc-Si:H layer increases with its thickness. So, when the cells shows low R_{shunt}, it is beneficial to reduce the (n)nc-Si:H thickness to increase R_{shunt}. And when the cells shows high R_{shunt}, in order to further enhance the cell FF, it is possible to reduce the R_{series} by adjusting (n)nc-Si:H thickness. In this project, by reducing the (n)nc-Si:H thickness from 18 nm to 12 nm a lower R_{series} was obtained in an IBC cell with 5.3 nm(n)a-Si:H/(n)nc-Si:H as BSF, which induces the FF increases from 71.61% to 64.85%.

V. At last the influence of pitch size design on the IBC cell performances were also studied. The FF increases with pitch widening as there is fewer shunting paths. This increase is less obvious in cells with higher R_{shunt}. To the opposite, the J_{sc} decreases with pitch widening as the carrier collection efficiency decreases. The best cell obtained in this project has a BSF with dual-n-layer thickness combination of 3/18 nm, and a medium pitch width of 650 µm. It has a V_{oc} of 665 mV, a J_{sc} of 39.36 mA/cm^2, a FF of 74.33% and an efficiency of 19.45%.

6.3. Outlooks

Further optimization of the dual-n-layer BSF. In this project, the best cell has 3/18 nm (n)a-Si/(n)nc-Si:H as BSF. It was found that the cell with 5.3/12 nm (n)a-Si/(n)nc-Si:H has a higher FF than that with 18 nm (n)nc-Si:H thanks to the lower R_{series}. So, it is also possible to improve the obtained best cell by reducing the (n)nc-Si:H layer thickness. If the (n)nc-Si:H layer is thinner, then the R_{shunt} would increase. This would allow to reduce the (n)a-Si:H layer thickness to have a more efficient TRJ at the emitter side. 3 nm (n)a-Si:H at textured BSF side corresponds to 5nm at flat emitter side. And it was found in FBC cells that with 5 nm (n)a-Si:H, the average FF dropped by around 3.7% compared to the reference cell and the decrease is only 0.72% with 3 nm (n)a-Si:H (1.8 nm on texture surface). So, based on the obtained best cell, it is possible to increases the FF by reducing the dual-n-layer thickness to a more optimized thickness.

Introducing HPT Hydrogen plasma treatment(HPT) is beneficial for crystalline phase growth of (n)nc-Si:H[61] and its passivation quality[96].By controlling the HPT process, it is possible to obtain a thinner but more conductive (n)nc-Si:H layer. However, the HPT

process should be optimized along with the (n)a-Si:H/(n)nc-Si:H thickness to prevent R_{shunt} from being reduced. The 1.2 nm(at textured BSF side) used in this project is too thin. During the HPT process, the (n)a-Si:H is actually being etched away[98]. The iV_{oc} gain from HPT can be reflected in V_{oc} only when the R_{shunt} is high. With an optimized (n)a-Si:H/HPT/(n)nc-Si:H layers stack, a higher V_{oc} can be expected.

Fully textured rear side In this project, the rear side of the IBC cell is partly textured. This is because the optimization of (p^+)poly-Si/tunnel oxide passivation for textured surface is still ongoing within the group. Once it is optimized, double sides textured wafers can be used and the fabrication process can be largely simplified. In addition, the thickness of (n)a-Si:H layer on the emitter side would be 1.7 times thinner comparing to the current IBC cells with flat emitter side. This thickness decrease would facilitate the electrons tunneling at the TRJ. Or from another perspective, it would allow more freedom of the dual-n-layer thickness optimization. In this project, the ITO thickness at the IBC rear side is 150 nm on the flat emitter side and only around 88 nm on the BSF side. If double sides textured wafers are used, a full area 150 nm ITO can be deposited. Thus, a better infrared-response can be expected[79].

Double ARC layers The ARC layer SiO_2 was deposited using e-beam system and the uniformity was not good. The uniformity can be improved by using PECVD system for low-temperature SiO_2 deposition. It also possible to reduce reflection by applying double layers ARC[102]. A combination of 40 nm SiN_x and 140 nm SiO_2 allows to reduce the reflectance in a wider wavelength range[102]. Thus, a higher J_sc can be expected.

Applying Front surface field As discussed in Section 5.5.2, the electrical shading loss would decrease carrier collection probability and thus, reduce the cell J_{sc}, especially in cell with large pitch width. For cell with large pitch width, the lateral carrier transport resistance can be reduced by applying a Front surface field (FSF) and the cell performance can be improved[103]. In this project, if FSF is applied, a higher J_{sc} can be expected for die C which has the highest FF among the dies in the hybrid IBC cells. The FSF can be applied by ion-implantation[12].

Metal finger thickness In this project, the Al thickness is only 1.2 µm at BSF and 2 µm at emitter side. This is limited by the metal evaporation and lift-off processes. From the results in Section 4.5, it can be seen that the thin metal finger's resistance is limiting the FF in FBC cells. The metallization using e-beam Al could be replaced by Cu-plating. Then a much thicker metal layer (>20 µm) could be obtained and a higher FF can be expected[104].

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Delft, 26th August 2021

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