MMIC packaging using Flip-Chip technology at G band

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by

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Preface

The thesis you are about to read is about MMIC packaging using flip-chip technology at G band. I have written this report to obtain the degree of Master of Science in Electrical Engineering: wireless communications and sensing program at the Delft University of Technology. The work presented in this thesis is part of the 'Fly's Eye Lens Antenna System for Future Tbps Wireless Communications' project at the Terahertz Sensing group in collaboration with Huawei.

Since I started my internship in the group, I have learned a lot of new things both about my topic and also from others in the group on their work. Also, I enjoyed the group activities, group runs, group lunches, and 3 pm coffee breaks with people of the group, helping me to stay motivated to complete this thesis. For this, I would like to thank them.

I would like to thank dr. Marco Spirito, prof. dr. Nuria Llombart, and dr. Maria Alonso-delPino for our weekly meetings which helped me to work through the main challenges I came across. Specifically, I would like to thank Marco for giving me the opportunity to do the preliminary TRL measurements, and for the support in designing the TRL test structures. Also, I would like to thank Nuria for her support in understanding the transmission line transitions and CST simulations. Next, I would like to thank Maria for introducing me to the project and the discussions whenever I had doubts. Lastly, a special thanks to Nick van Rooijen, whom I could always bother with questions and discussion at any moment.

I would like to thank my family, friends, and girlfriend for supporting me. To the reader: I hope you enjoy reading this thesis.

Rik Bokhorst
Delft, September 2022

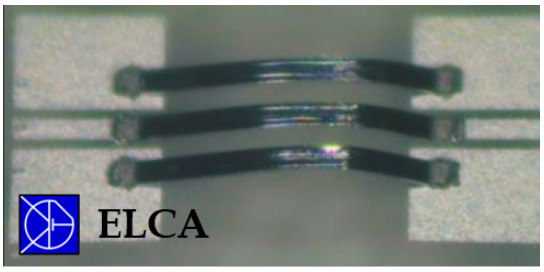
Abstract

Front-end Monolithic Microwave Integrated Circuits (MMICs) have recently become commercially available for frequencies above 100 GHz. However, achieving low-loss and broadband interconnections between the antenna and MMICs is challenging for integrated front ends at these frequencies. This thesis presents the characterization of a flip-chip interconnection used for an integrated front end at 150 GHz (G-band) with an on-package leaky-wave dual lens antenna. Two paths for the front-end integration have been proposed. The first path adopts CPW transmission lines on 500 μm-thick fused silica and provides easy assembly and seamless flip-chip capabilities. The second uses microstrip transmission lines on 50 μm-thick fused silica and provides lower transmission line loss but a challenging assembly and flip-chip interconnection. In this thesis, a path toward microstrip and CPW flip-chip interconnections has been outlined at the high millimeter-wave frequencies. Two-port test structures using CPW transmission lines were developed, adopting a double Thru-Reflect-Line calibration and allowing for accurate extracting of the interconnection response. The final interconnection to the MMICs has been realized using a via-less CPW to microstrip transition with high impedance transmission line S11 matching compensation. The simulated S11 and S22 are below -12 dB, Ohmic loss below 0.6 dB, radiation loss below 0.4 dB, and transmission line losses around 0.15 dB/mm.

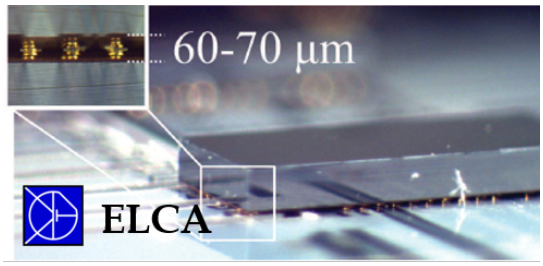
Contents

1 Introduction

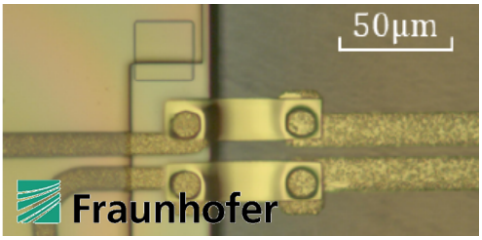
Front-end Monolithic Microwave Integrated Circuits (MMICs) have recently become commercially available for frequencies above 100 GHz. However, achieving low-loss and broadband interconnections between the antenna and MMICs is challenging for integrating front ends at submillimeter frequencies. At these frequencies, there are integrated solutions where antennas and electronics are integrated within the same package, for example by employing IC to waveguide interfaces [1], adopting an antenna-on-chip [2] or utilizing a near system-on-chip solution using EM-coupling [3]. At frequencies above 100 GHz and below 300 GHz, the MMICs that are commercially available are sold separately from the antenna. The packaging and integration of these chips are in the hands of the front-end integration designer. The packaging technology that is currently available typically uses one of these three MMIC interconnection technologies (see Fig. 1.1): wire bonding or flip-chip bonding in the low millimeter band or beam-lead bonding in the higher millimeter band (above 300 GHz).



(a) Wire-bonding [4]



(b) Flip-chip bonding [5]



(c) Beam-lead bonding [6]

Figure 1.1: MMIC interconnection technologies

At frequencies above 60 GHz, high inductance effects of wire-bonding lead to an S11 mismatch. Furthermore, high radiation losses are associated with the bond-wires at mm-wave frequencies [7]. The distance between the MMIC and the carrier as well as from the pads to the edge of the MMIC/carrier restricts the minimum length of the wire-bonds to around 100 μm [8]. The parasitic inductance associated with these wire-bonds may be compensated for, but this results in a narrowband behavior.

Beam-lead bonding results in lower losses at mm-wave frequencies. Arias Campo *et al.* [6] mention losses of 0.2 dB per interconnect over the H-band, using a differential air-bridge interconnect, from GaAs to Quartz. However, beam-lead bonding is unsuitable for integration using commercial MMICs because the lengths of the beam leads are limited. Furthermore, beam-lead bonding is significantly more costly than other interconnection methods and not widely available, in contrast to flip-chip and wire-bonding.

Flip-chip technology is very suitable for commercial applications because it is well established for use at microwave and millimeter-wave frequencies [8]–[10]. The height of the flip-chip studs is much shorter than the wire-bonds, reducing the inductance and losses. Furthermore, radiation effects are critical for the performance of flip-chip interconnections above 100 GHz and should thus be reduced. Lastly, parallel plate line (PPL) modes should be suppressed [11].

Sinha *et al.* [11] present a broadband interconnection using the flip-chip approach for frequencies up to 500 GHz using a BCB stack. At 500 GHz, they report a total loss of 0.9 dB and reflection below -18 dB. Although their approach does not use commercial MMICs, the design principles hold, and the potential of the flip-chip technology at high frequencies has been proven. By shrinking the dimensions of the flip-chip studs, the parasitics are reduced. Yet, the effect of the carrier on the MMIC circuitry should also be considered for commercial MMICs. Flip-chip interconnections up to 100 GHz are typically modeled by an equivalent π-circuit, consisting of a few lumped elements [12]. If dimensions scale linearly with frequency, this description can be extended to higher frequencies [11]. Nonetheless, due to fabrication limitations, this is not the case.

The impact of the parasitic effects in the interconnection plays a very important role in the system performance at high mm-wave frequencies. However, the packaging using commercial MMICs using a flip-chip interconnection has not been studied in detail at frequencies above 100 GHz. Thus, there is a need to study the parasitic effects of the flip-chip interconnection at the G band frequency range and suppress them to realize a low-loss broadband interconnection to commercial MMICs.

1.1. Background and project context

The rapid growth of cellular data and smartphones creates challenges for providers of wireless services in terms of the available bandwidth [13]. Millimeter-wave frequencies in the range of 30-300 GHz provide the bandwidths required for mobile broadband applications [14]. Wireless links will support data rates towards 100 Gbps for point-to-point mobile applications at these frequencies [15].

The fifth-generation mobile technology standard for broadband cellular networks (5G) facilitates high-speed communications. 5G builds upon existing technology platforms while integrating new radio concepts such as phased-arrays, massive MIMO, and ultra-dense networks to increase the network capacity. However, the most demanding situations with high connection density reflect challenges not properly addressed by the current technologies implemented in 5G [16].

The scenario that is the most demanding in terms of simultaneous user connections and has high bandwidth requirements is a stadium hosting an audience of several people. Similar scenarios include other congested locations like shopping malls, festivals in the open air, and conference halls. The Fly's Eye concept [17] proposes to combine quasi-optical beam forming with a mm-wave broadband operation to enable a single base station providing more than Tbit/sec overall (front-end) capacity to a dense environment with tens of thousands of users. A complete base station will contain an array of thousands of directive lenses covering a bandwidth of over 20%. The developed technology can be potentially exploited for future 6G use cases [18].

The final goal of the Fly's Eye project is to demonstrate the concept and performance by developing an integrated front-end prototype. Scalable lens arrays are realized in the form of modular planar panels, each generating multiple simultaneous beams, as depicted in Fig. 1.2. The antenna architecture consists of a core and shell lens and a fused silica wafer, on which the antenna feed is placed. The antenna design and single-pixel architecture are developed by Nick van Rooijen, a Ph.D. candidate at the Terahertz Sensing group.

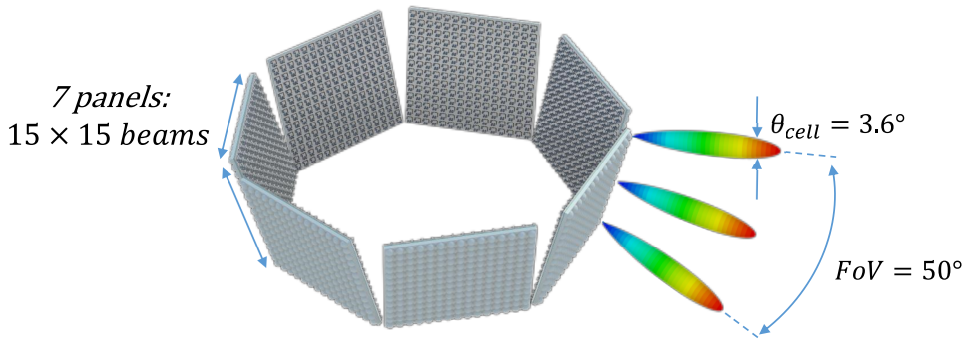
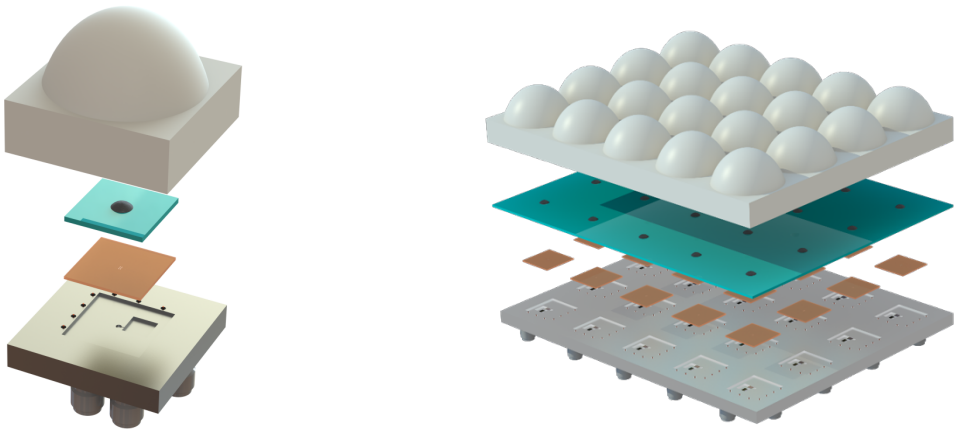


Figure 1.2: Sketch exemplifying the multi-beam base station synthesis for the link demo using N lens array panels. The example shows M=7 panels with a 16x16 lens array per panel (N=256).

This thesis presents the characterization of a flip-chip interconnection used for an integrated front end at 150 GHz (G band) with a leaky-wave on-package dual lens antenna using commercial MMICs. The work presented in this thesis is part of the development of a single-pixel prototype, as depicted in Fig. 1.3a. This prototype will demonstrate the front-end integration, after which the single module will be scaled by placing the elements in an array of desired size, as depicted in Fig. 1.3b.



(a) Single-pixel architecture

(b) 3D view of a packaged multi-pixel lens antenna array element

Figure 1.3: Fly's Eye demonstration at 150 GHz

For the single-pixel prototype, two commercially available MMICs and a feeding antenna are integrated on a single fused silica wafer, as shown in Fig. 1.4. The first MMIC provides a multiplication (x6) stage, followed by a subharmonic IQ mixer acting as a frequency doubler to end up at the G band. As indicated in Fig. 1.4 by the red dotted lines, three flip-chip interconnections are required. A transmission line on the fused silica connecting the mixer MMIC and the multiplier MMIC requires two flip-chip interconnections, whereas the final connection from the mixer to the transmission line for the antenna feed on the fused silica requires another flip-chip interconnection.

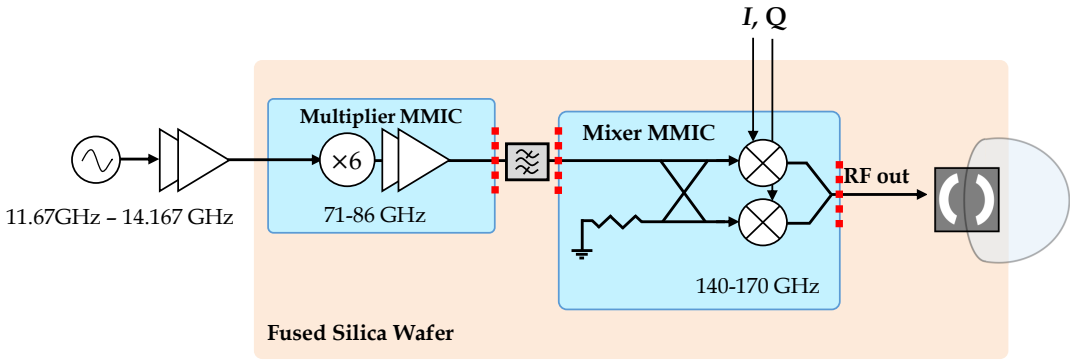


Figure 1.4: Circuit diagram of the MMIC integration. The red dotted lines indicate the locations of the interconnections.

1.2. Study of the acquired MMICs

Advances in technology for high electron mobility transistors (HEMTs) and low-noise amplifiers (LNAs) have led to the development of MMICs above 100 GHz [19], [20]. However, very few companies sell MMICs or packaged components above 100 GHz. Virginia Diodes produces MMICs based on Schottky diode technology and Goteborg Microwave Integrated Circuits (Gotmic) AB, a spinoff company from Chalmers University, provides GaAs MMICs technology. The latter offers a performance oriented for communications applications, possible to be implemented for applications with a high number of array elements.

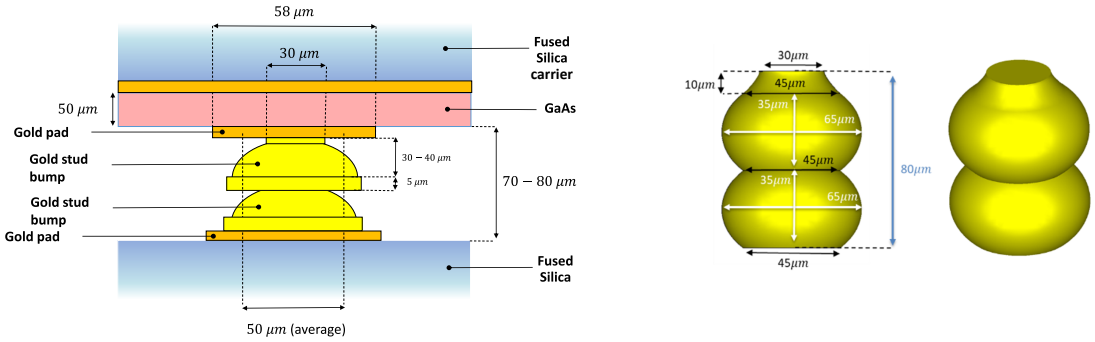
The MMICs acquired for this project are the gMDR0035 subharmonic IQ mixer [21] and the gXSB0025 ×6 frequency multiplier [22] from Gotmic. The MMICs consist of a gold metalization on a 50 μm-thick Gallium Arsenide (GaAs, $\varepsilon_r = 12.9$) substrate. They feature a 100 μm pitch connector P2 with an RF pad and two GND pads. The datasheets provided ([21], [22]) report a 50 Ω transmission line connected to P2. After visual inspection of the chips, it was concluded that the 50 Ω transmission line is of the microstrip type. The DFX-file of the mixer provided by Gotmic indicates a width of 33 μm for the microstrip transmission line. This microstrip geometry possesses a 53 Ω characteristic impedance, according to verification using the Characterization of Printed Transmission Line tool (TL tool) [23], which is discussed in detail in Section 1.4. Furthermore, the tool confirms that the line does not introduce any radiation losses and that the Ohmic/dielectric losses are around 0.58-0.64 dB/mm in the frequency band 140-170 GHz.

1.3. Flip-Chip bonding

Flip-chip technology is used for interconnecting dies such as semiconductor devices, IC chips, integrated passive devices and microelectromechanical systems (MEMS) to external circuitry [24]. The flip-chip method uses studs (conductive bumps or balls) that are deposited on the pads of (MM)ICs on a chip. The chip is then flipped and connected to the circuitry on an external wafer. This process is automatized and suitable for mass-production commercial applications. Due to mechanical stress on the interconnections, the MMICs should be stabilized by adding extra flip-chip studs or an underfill, ensuring structural support [8].

For this project, the flip-chip technology process will be provided through a collaboration with CITC (Chip Integration Technology Center, in The Netherlands). CITC employs flip-chip bonding technology using gold ball stud bumps. One gold stud bump realizes a separation of 30-40 μm, whereas for two stud bumps 70-80 μm is achieved.

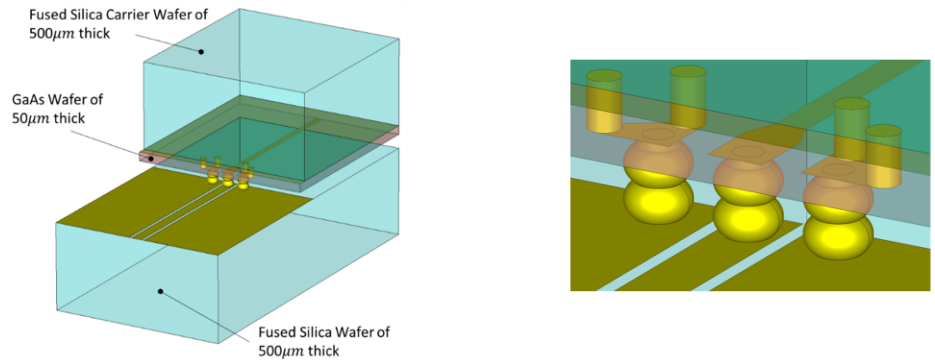
Since the two chips are bonded through thermo-compression forces and the MMICs are 50 μm thick, the MMICs will be bonded to a thicker carrier of 500 μm to increase the robustness of the bond. After several discussions with CITC, a 3D model of the bumps was outlined, shown in Fig. 1.5 and Fig. 1.6. This model will be used for full-wave simulations of the designs throughout the thesis.



(a) Sketch of the transition based on discussions with CITC

(b) CST model of the bumps used for 3D simulations

Figure 1.5: Physical model of the two Au stud bumps placed on top of each other



(a) 3D model of the flip-chip interconnection between the MMICs and transmission line in fused silica

(b) Zoomed 3D view of the flip-chip interconnection from the MMICs to the fused silica

Figure 1.6: 3D physical model of the flip-chip transition for two Au stud bumps placed on top of each other

1.4. Characterization of transmission lines for front-end integration

The on-package integration of the antenna and the RF front end, as presented in Section 1.1, is deemed viable in the case of a low-loss RF front end. Accordingly, this section covers the characterization of various transmission line geometries, considering Ohmic, dielectric, and radiation losses. Two transmission line types are considered: coplanar waveguides (CPW) and microstrip transmission lines. These transmission lines are implemented into two front-end integration topologies, discussed in more detail in the next subsection.

Calculations in this section are done using a MATLAB tool, which was previously developed in the THz Sensing Group for the characterization of transmission lines [23]. The tool implements the spectral Green's function of an infinite transmission line, computing the propagation constant and attenuation constant from the complex poles of the Green's function.

The antenna and the front end are integrated on a low-loss fused silica wafer with a gold metalization, adopting thin-film technology manufactured by Applied Thin-film Productions (ATP). ATP fabricates conductors with trace widths and gaps of at least 0.0004" or 10.16 μm, with a tolerance of ±0.0002" or 5.08 μm. For simulations and calculations throughout the thesis, the assumed material properties are listed in Table 1.1.

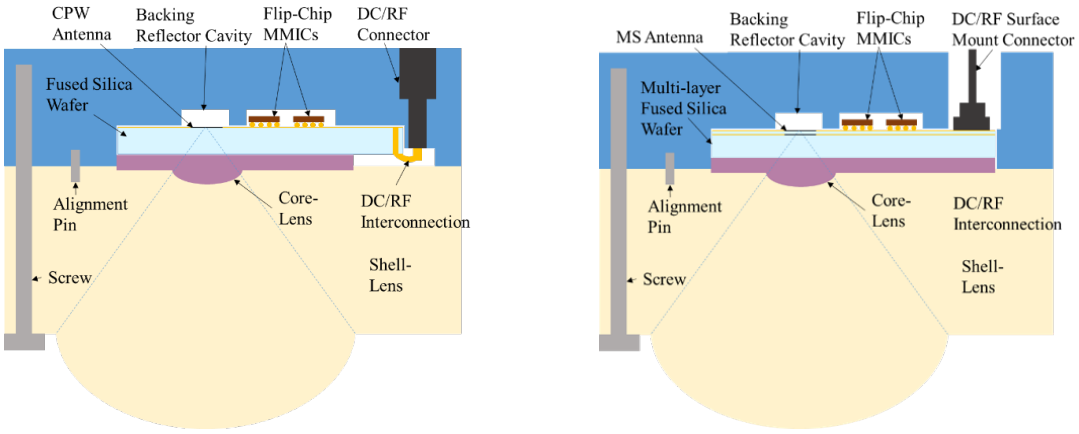
Table 1.1: Assumed material properties at 155GHz

Material	Permittivity	Conductivity [S/m]	Tangent Delta
Fused silica	3.9		0.0006
Gold		$4.3 \cdot 10^7$	

1.4.1. Front-end integration paths

Two front-end integration paths are considered, as depicted in Fig. 1.7. The CPW topology is the most straightforward to fabricate because only a single layer printed on a thick silica wafer is required, resulting in a more robust integration. For this configuration, the front end

could be integrated onto a single wafer including the antenna, the RF circuitry, the MMICs, and the DC interconnections. A sketch of this front-end integration is provided in Fig. 1.7a. A CPW-fed double slot antenna will be present at the backside of a thick 500 μm silica wafer. The antenna will be connected to the RF MMIC mixer via CPW transmission lines and flip-chip bonding. The DC/RF connections are present on the same substrate.



(a) Front end integration scheme using CPW interconnection on 500μm-thick fused silica

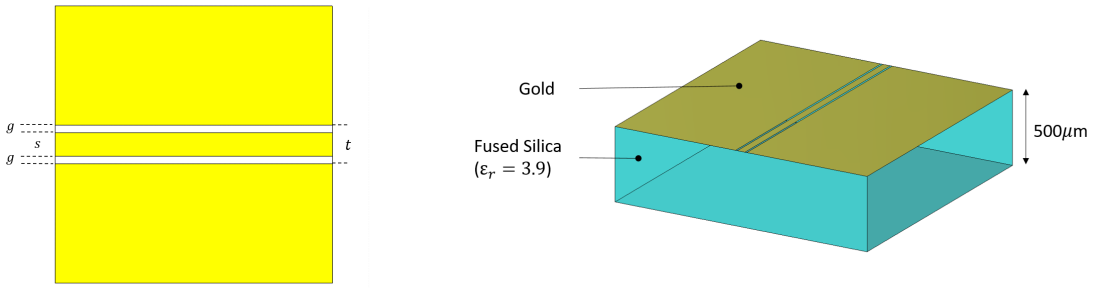
(b) Front end integration scheme using microstrip interconnection on 50μm-thick fused silica

Figure 1.7: Front end integration between MMICs and antenna

A second route for the front-end integration is also proposed using a microstrip-fed double slot antenna. For this configuration, two silica wafers are required: a thick 500 μm wafer for the leaky wave resonant cavity and a thin 50 μm wafer for the microstrip feeding network. Both of these wafer thicknesses are available at ATP thin-films. The thin 50 μm wafer can be fabricated with a double-side pattering. In this case, the wafers can be bonded using a thin 1-2 μm glue via the CITC processing capabilities. The RF interconnection between the antenna and the RF flip-chipped mixer will be done via a microstrip on this thin layer. A sketch of this front-end integration is provided in Fig. 1.7b.

1.4.2. CPW transmission line for Front end integration

CPW transmission lines allow for a single metal layer configuration, simplifying the fabrication process. The CPW is printed on a 500 μm-thick fused silica wafer, as indicated in Fig. 1.8b, allowing placement of a leaky wave antenna in the same layer, as presented in Fig. 1.7a.

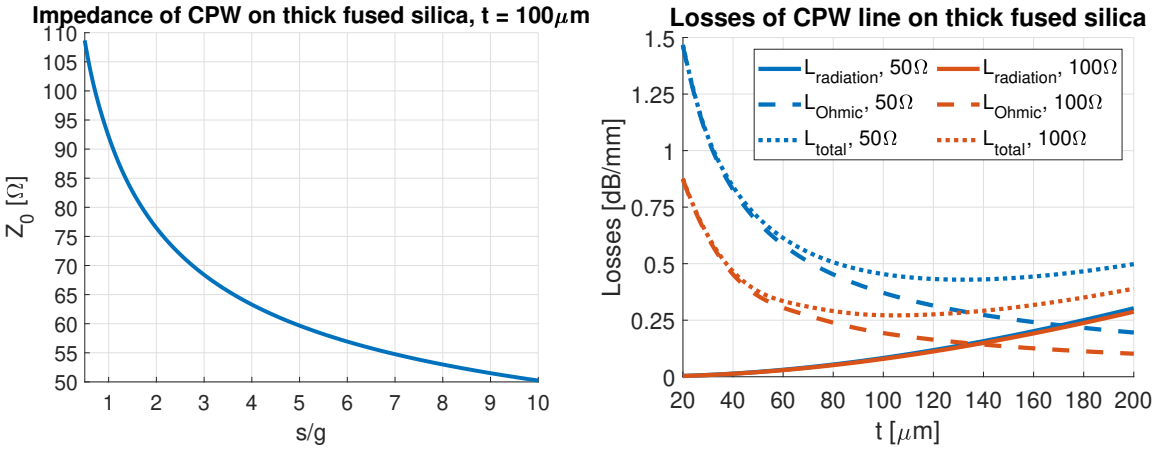


(a) Top view

(b) 3D view

Figure 1.8: Coplanar waveguide (CPW) transmission line on 500 μm thick fused silica

The characteristic impedance of a CPW is determined by the ratio of the width s of the central metal strip to the gap g between the strip and one of the grounds. In Fig. 1.9a, the characteristic impedance of a CPW printed on 500 μm-thick fused silica is plotted for different s/g, while maintaining $t = s + 2g$ constant at 100 μm. The characteristic impedance is around 100 Ω for a ratio s/g of around 0.7 and drops to around 50 Ω when s/g is around 10. Subsequently, the radiation losses, Ohmic/dielectric losses, and the total losses are plotted for both 50 Ω and 100 Ω in Fig. 1.9b. There is a trade-off between Ohmic losses and radiation losses: wider CPWs suffer from radiation introduced by the excitation of the surface wave mode, but narrowing the CPW will increase the Ohmic losses.



(a) Characteristic impedance of the CPW for $t = 100\mu m$

(b) Losses of the CPW, for 50Ω and 100Ω

Figure 1.9: Characteristic impedance and losses of a CPW transmission line on thick fused silica dielectric, found using the TL Tool [23]

Concluding, the CPW width $t = s + 2g$ should be in the order of 100 μm accomplishing <0.5 dB/mm of total loss.

1.4.3. Microstrip transmission lines for Front end integration

The second option is to realize the front-end integration using microstrip transmission lines, as depicted in Fig. 1.7b. For this geometry, a strip of width s is printed on a 50 μm-thick fused silica wafer and a ground plane is located on the opposite side of the wafer, as indicated in Fig. 1.10. Bonding of this wafer to the thicker wafer presented before is required to form a leaky wave cavity for the antenna. The characteristic impedance and losses are again calculated using the TL tool [23] and plotted in Fig. 1.11. When increasing the width of strip s to around 100 μm, the losses are reduced to below 0.15 dB/mm, yielding a characteristic impedance of around 50 Ω. The losses are significantly lower than for the CPW case, which results from the fact that there is no surface wave radiation present for this configuration. In conclusion, this option is preferred, as the loss reduction facilitates good antenna performance. However, as discussed before, the microstrip front-end integration is more challenging to fabricate compared to the CPW front-end integration.

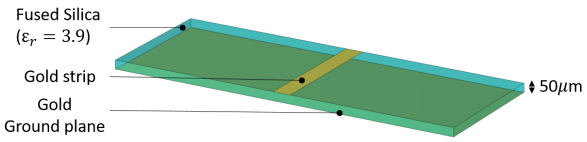


Figure 1.10: 3D view of a 50 Ω microstrip transmission line on fused silica of thickness 50μm

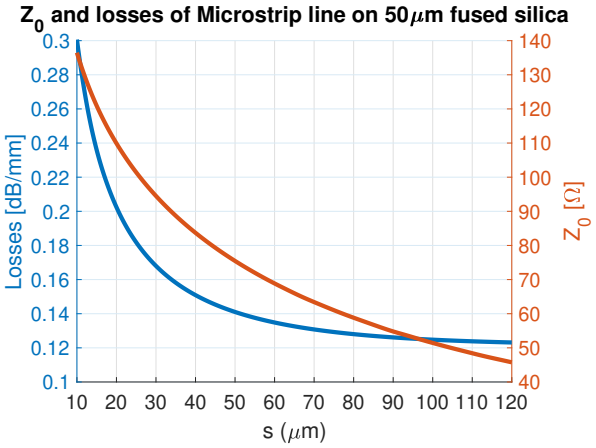


Figure 1.11: Characteristic impedance and losses of a microstrip line on 50μm fused silica wafer.

1.5. Thesis outline

The main part of this thesis contains four chapters. In Chapter 2, several transmission line interconnections on fused silica are studied using full-wave simulations. The transitions are subdivided into flip-chip interconnections and probe landing transitions. For both, CPW and microstrip transitions are considered. The transitions are optimized in terms of the S12, reducing radiation losses and improving S11/S22 matching.

Chapter 3 covers the design of double TRL test structures to accurately extract the interconnection response. The test structures are based on the optimized transmission line interconnections from Chapter 2. The first two sections cover the design of the test structures, implementation of the two TRLs, and verification of the code and the design. In the last two sections of Chapter 3, two mask designs based on the test structure designs are presented.

In Chapter 4, the optimized interconnection from Chapter 2 are incorporated into the design of the flip-chip interconnection to the MMICs. Both CPW and microstrip interconnections are considered.

Finally, Chapter 5 includes some preliminary TRL measurements verifying the TRL code and supporting the full-wave simulations of the designed TRL structures.

2

Optimization of Transmission Line Transitions for Flip-Chip test structures

In this chapter, the design of the test structures to evaluate the flip-chip interconnection and the thin-film technologies will be presented. The flip-chip interconnection will be tested using solely transmission lines in fused silica, reducing the materials and simplifying the mask fabrication.

The design has been realized based on the minimization of the radiation losses from the flip-chip interconnection, the transmission lines, and the transitions between different transmission line geometries. Since radiation losses are not de-embedded by the TRL calibration method, their reduction will ensure proper calibration of the test structures and improve the performance of the final design.

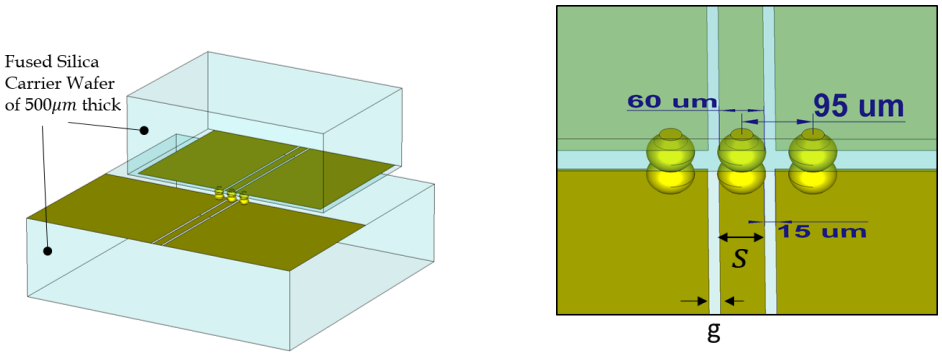
This Chapter is divided into two parts. In Section 2.1, three symmetric flip-chip interconnections are examined: a CPW interconnection, a microstrip interconnection using vias, and a via-less microstrip interconnection. Subsequently, Section 2.2 covers two transitions required to land the RF probes on the test structures.

2.1. Flip-Chip Transmission Line Interconnections

The flip-chip interconnections considered in this chapter are based on the transmission line geometries used for the front-end integration of the MMICs, as discussed in Section 1.4. The 3D ellipsoidal stud model from Fig. 1.5b is used to model the studs. The separation between the studs will be 95 μm, corresponding to the distance set by the dimensions of the MMICs, as shown in Fig. 1.6b.

2.1.1. Flip-Chip CPW interconnection

The flip-chip interconnection using CPW transmission lines has the smoothest field transition, as the field distribution of a CPW transmission line matches best to the field in between the studs. The flip-chip CPW interconnection is depicted in Fig. 2.1.



(a) 3D model used for CST simulations **(b)** Stud placement and dimensions

Figure 2.1: Flip-Chip interconnection using CPW transmission lines.

Verification of the radiation loss reduction

The CPW transmission lines suffer from radiation loss, as explained in Section 1.4. Therefore, the dimensions of the CPWs on both wafers are reduced. The width of the central strip s (indicated in Fig. 2.1b) is reduced to 60 μm in order to leave sufficient space for the flip-chip bumps. The gap g (see Fig. 2.1b) between the conductors is reduced to 15 μm, taking into account the minimum dimensions and tolerances of the fabrication, as discussed in Section 1.4. The model displayed in Fig. 2.1a was simulated for varying s (Fig. 2.1b) to verify the reduction of the radiation loss. The losses were extracted using the approach discussed in Appendix A.1. The result is plotted in Fig. 2.2, confirming the reduction.

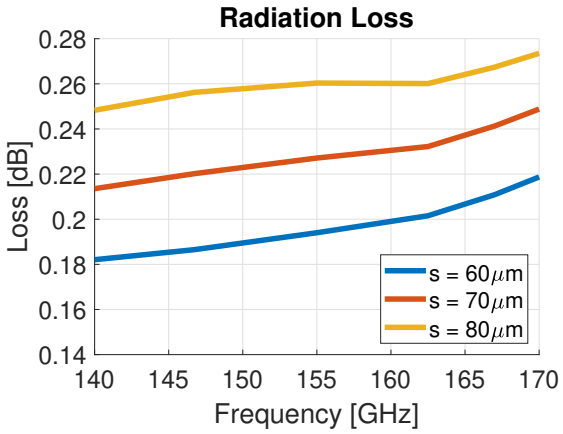
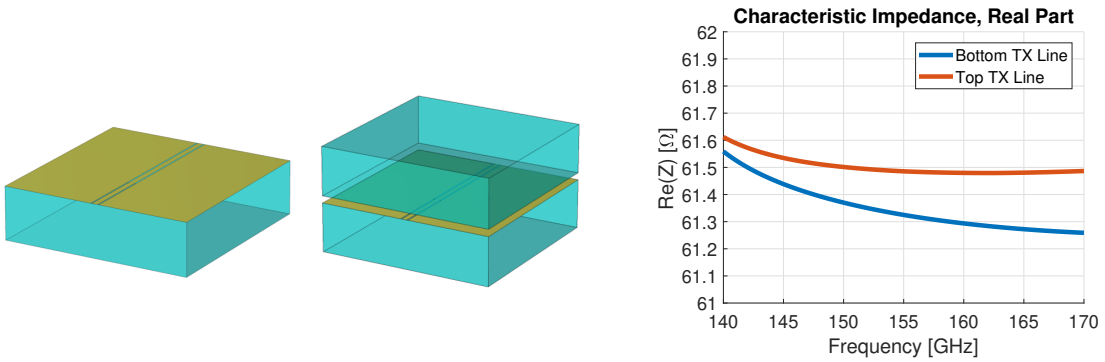


Figure 2.2: Radiation loss for varying CPW width for the flip-chip interconnection using CPW transmission lines

Study of the CPW impedances

Subsequently, the impedance matching in the transition is studied. Therefore, two transmission line structures were simulated in CST: one representing the bottom wafer (Fig. 2.3a) and another representing the top wafer (Fig. 2.3b), in the presence of the other fused silica wafer. These simulations verify that the MMIC performance does not vary in the presence of the fused silica wafer close to the interface (up to 80 μm). The characteristic impedance of both transmission lines is computed from the S-parameter results from CST simulations and depicted in Fig. 2.3c. Concluding, there is practically no mismatch between the CPWs and the effect of the bottom wafer is negligible.



(a) CPW transmission line on bottom wafer

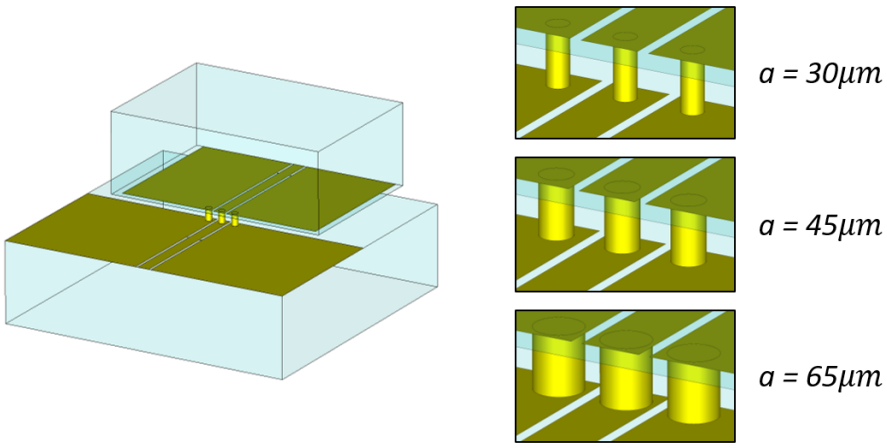
(b) CPW transmission line on the top wafer at 80μm from the bottom fused silica wafer

(c) Real part of the characteristic impedance, from full-wave CST simulations

Figure 2.3: CPW transmission lines for the flip-chip interconnection.

Effect of the bump size/shape on S11/S22

Consequently, the effect of adding the studs between the two transmission lines is studied by replacing the ellipsoidal studs with cylinders of varying diameter: 30 μm, 45 μm, and 60 μm, as displayed in Fig. 2.4.

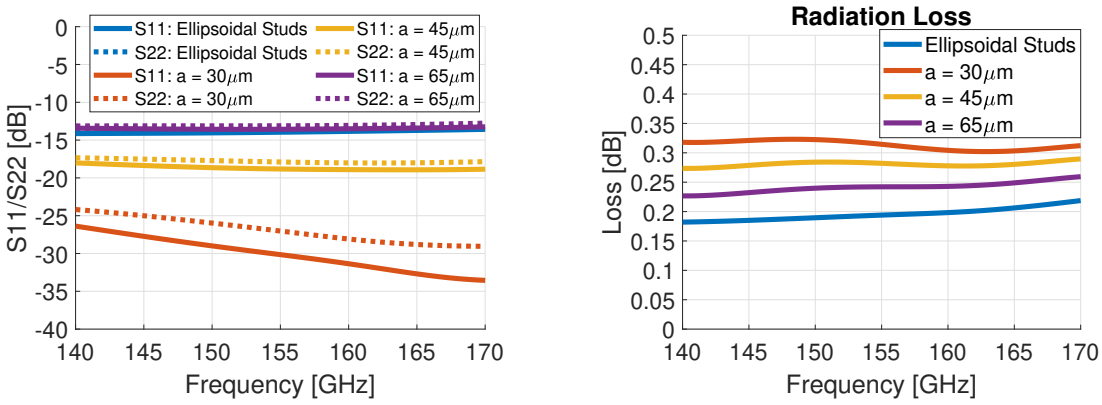


(a) 3D model of the CPW transition using cylinders to represent the studs

(b) Drawings of cylinders of diameter $a = 30$ μm, $a = 45$ μm, and $a = 65$ μm, connecting the two CPW transmission lines

Figure 2.4: 3D models of the flip-chip CPW interconnection for varying cylindrical studs.

The S11 and S22 of the flip-chip CPW interconnection for the cylindrical studs of varying diameters are plotted in Fig. 2.5a to assess the effect of the shape and size of the studs. The S11/S22 matching improves significantly when the cylinder diameter is reduced and resembles the performance of the ellipsoidal studs for cylinders of diameter 65 μm. The observation that small diameter studs improve the performance was also made in literature [10]. The radiation loss is increased by 0.1 dB when the cylinder diameter increases, as is plotted in Fig. 2.5b.



(a) S11 (solid lines) and S22 (dotted lines)

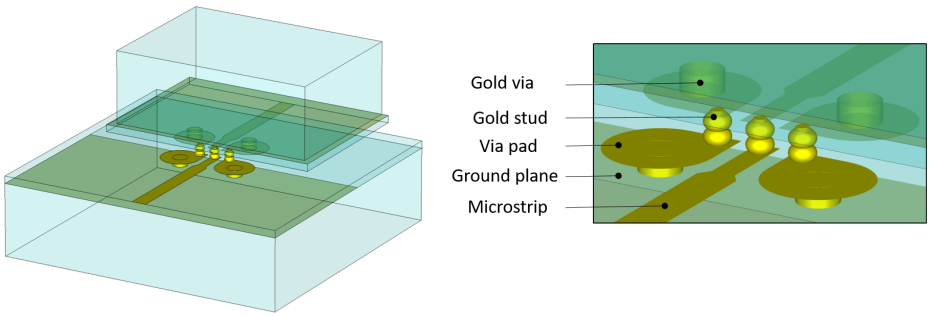
(b) Radiation loss

Figure 2.5: Results from full-wave simulations of the flip-chip CPW interconnection using cylindrical studs from Fig. 2.4, and ellipsoidal studs from Fig. 1.6b.

It is concluded that the shape and size of the studs have a major impact on the matching of the interconnection at 150 GHz. Due to the sensitivity of the stud dimensions, further investigation of the process variation is required. This study will be done by several flip-chip measurements, for which the mask will be discussed in Section 3.4. Accordingly, this interconnection is not optimized further to compensate for the mismatch (for example, by adding matching stubs).

2.1.2. Flip-Chip microstrip interconnection using vias

As demonstrated in Section 1.4, the transmission line losses are significantly reduced when replacing CPW transmission lines with microstrip transmission lines because there is no surface wave radiation in the latter case. Therefore, this option is preferred for the final MMIC integration. The first attempt to design a flip-chip transition using microstrip lines uses vias for the interconnection of the ground plane of the microstrips. In this case, the dimensions of the vias offered by ATP are used. A 50 Ω microstrip transmission line with a width of 100 μm is selected to minimize the Ohmic losses, as explained in Section 1.4. The two ground studs on either side are placed on pads, which on both wafers typically are connected to the ground plane using vias, as depicted in Fig. 2.6a.



(a) 3D model of the Flip-Chip microstrip interconnection using vias

(b) Indication of the different parts of the symmetric transition

Figure 2.6: 3D models of the flip-chip microstrip interconnection using vias.

Modeling of the vias and design of the via pads

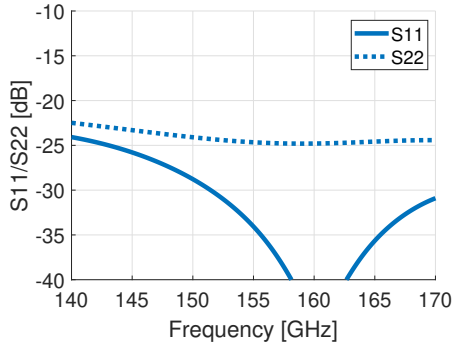
The ATP technology initially provided the capacity to fabricate Au plated through vias of 0.8 times the substrate height. However, because of the very thin (50 μm-thick) wafer selected, the vias had to be replaced by hollow plated throughs (HTPs) with a larger diameter, as requested by ATP. The resulting diameter is 4 mils (101.6 μm), as is listed in Table 2.1. Furthermore, circular pads are designed on which the vias are placed on one side and the studs on the other, as shown in Fig. 2.6b. The diameter of the pads was first determined as 8 mils (203.2 μm) to leave a 2 mils (50.8 μm) ring around the vias, accounting for tolerances in size and location of the vias. Subsequently, another 60 μm was added to the pad diameter to avoid placing the studs on the taper of the via holes. The microstrip is tapered near the pads to improve the matching.

Table 2.1: Via dimensions and tolerances: Au plated through from ATP

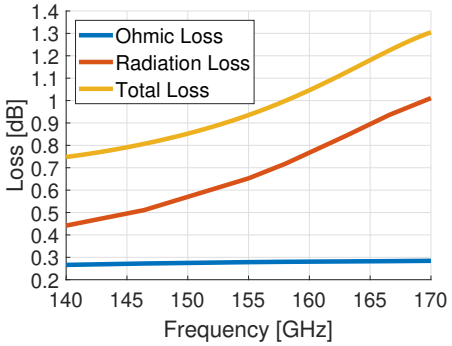
Diameter	± 0.004" (101.6 μm)
Size tolerance	± 0.001" (25.4 μm)
Location tolerance	± 0.001" (25.4 μm)
Hole taper	± 0.001" (25.4 μm)

Performance of the flip-chip microstrip interconnection

The performance of the flip-chip interconnection for the geometry as shown in Fig. 2.6a is depicted in Fig. 2.7. Although good S11/S22 matching over the bandwidth was achieved, the radiation loss is increasing to 1 dB at 170 GHz, as depicted in Fig. 2.7b. In Chapter 3, the design of back-to-back test structures using CPW transmission lines will be explained, which has also been attempted using the microstrip design using vias. However, the TRL calibration of the microstrip structures using vias, which was simulated using CST, shows significant calibration errors compared to reference simulations. It was concluded that these errors are due to the coupling of the radiation loss to the transmission lines. An attempt to reduce this coupling by increasing the length of the transmission lines was unsuccessful. The fabrication constraints lead to very large pads and vias, increasing the radiation losses to levels at which the correct operation of this architecture becomes nonviable. The design using vias cannot be further improved for the reduction of radiation loss and therefore a via-less design has to be considered.



(a) S11 and S22 matching

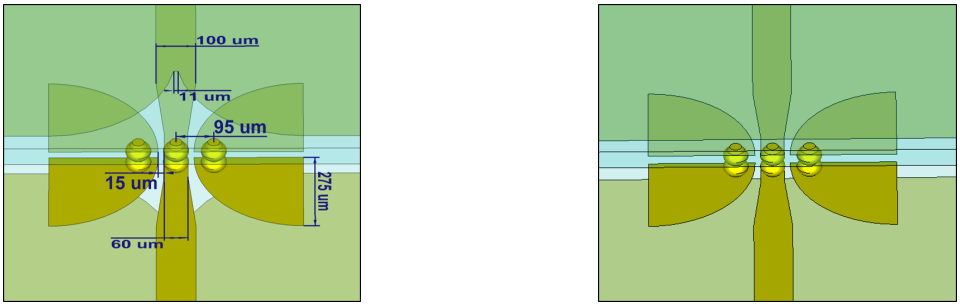


(b) Losses: Ohmic Loss, Radiation Loss, Total Loss

Figure 2.7: Simulated performance of Flip-Chip microstrip interconnection using vias.

2.1.3. Via-less Flip-Chip microstrip interconnection

Subsequently, a via-less 50 Ω microstrip interconnection was endeavored. As a starting point, the studs are placed on a CPW-like configuration, with the same dimensions as the CPWs in Section 2.1.1 ($s = 60$ μm, $g = 15$ μm). However, the CPW ground conductors on both sides are truncated in a quarter circular shape, in order to facilitate the transition from a CPW to a microstrip field distribution. Furthermore, for the microstrip transmission line, a ground plane metallization is required, located below the 50 μm-thick fused silica. However, extending the ground plane below the CPW will excite the grounded CPW (CPWG/CBCPW) mode, introducing a mismatch (S11/S22). Therefore, the ground plane is tapered in a quarter circular shape as well, as illustrated in Figure 2.8a. The microstrip transmission lines on both sides are designed and verified at 50 Ω using 3D CST simulations.



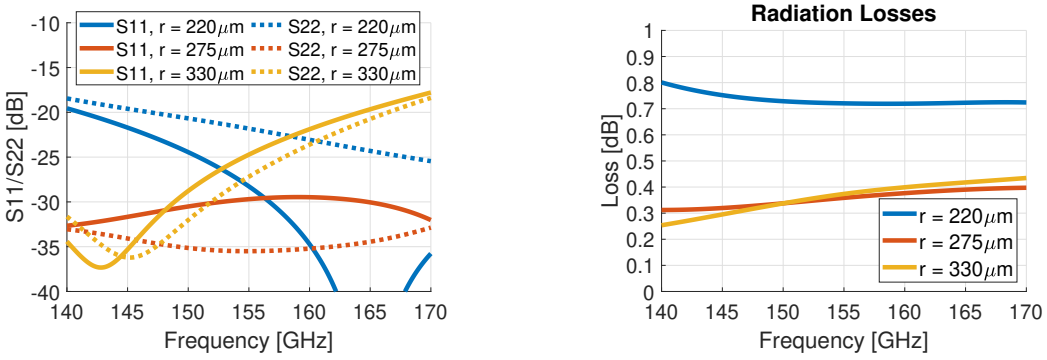
(a) Truncated ground plane

(b) Non-truncated ground plane

Figure 2.8: 3D model of the via-less Flip-Chip microstrip interconnection

Optimization of the quarter circle radius

Both quarter circular shapes are optimized for the reduction of radiation loss from the excitation of surface waves in the dielectric. The radius of the quarter circle was found to be optimal at around 275 μm, as depicted in Fig. 2.9. This is approximately $\lambda/4$ at the center frequency, where λ (wavelength) was found using the effective permittivity of the simulated microstrip transmission line. When increasing or decreasing the radius of the quarter circles, the S11/S22 matching is deteriorated, as displayed in Fig. 2.9a. Furthermore, decreasing the radius leads to an increase in radiation losses, as shown in Fig. 2.9b.



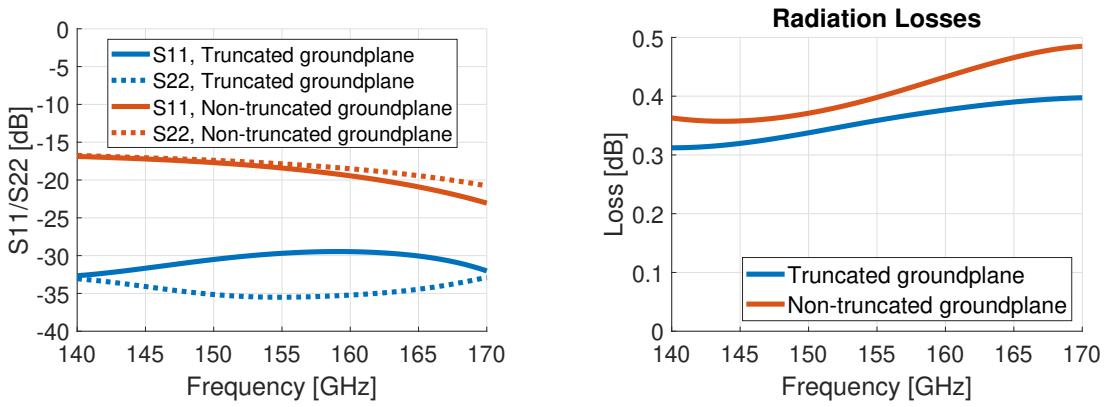
(a) S11 and S22 matching

(b) Radiation Loss

Figure 2.9: Simulated performance of via-less flip-chip microstrip interconnection for varying quarter-circle radius r of 220 μm, 275 μm, and 330 μm.

Verification of the effect of the ground plane truncation

As depicted in Fig. 2.8a, the ground planes are truncated using quarter circular shapes to avoid exciting the CPWG mode. The effect of this truncation was verified using CST full-wave simulations of the interconnection with (see Fig. 2.8a) and without (see Fig. 2.8b) truncation of the ground plane. In the latter case, the ground plane is extended to the ending on the microstrip. The resulting comparison is presented in Fig. 2.10. The S11/S22 matching has been improved from below -15 dB to below -25 dB.



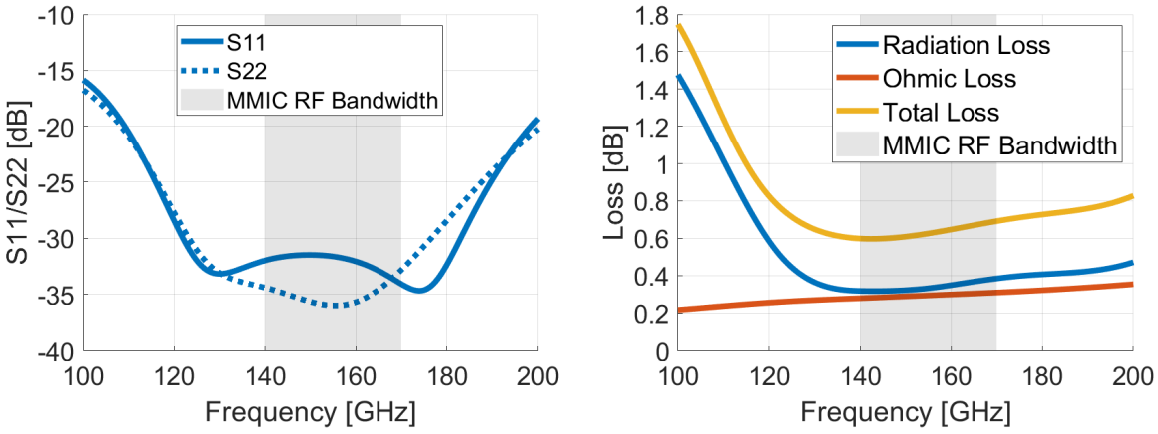
(a) S11 and S22 matching

(b) Radiation Loss

Figure 2.10: Simulated performance of via-less flip-chip microstrip interconnection for truncated and non-truncated ground plane.

Performance and bandwidth

The interconnection model as presented in Fig. 2.8a was simulated using CST to assess the performance and bandwidth of the transition. A matching below -20 dB and loss below -1 dB is to be expected over a limited bandwidth only, as presented in Fig. 2.11.



(a) S11 and S22 matching

(b) Losses: Ohmic Loss, Radiation Loss, Total Loss

Figure 2.11: Simulated performance of via-less flip-chip microstrip interconnection. The frequency range is extended to 100-200 GHz to demonstrate the limited bandwidth.

Visualization of the 2D electric field

The 2D electric field was obtained from CST simulations, to visualize the change of the electric

field over the interconnection. Xy-cuts A, B, and C are indicated in Fig. 2.12, and the electric field is plotted using contour plots and vector plots in Fig. 2.13.

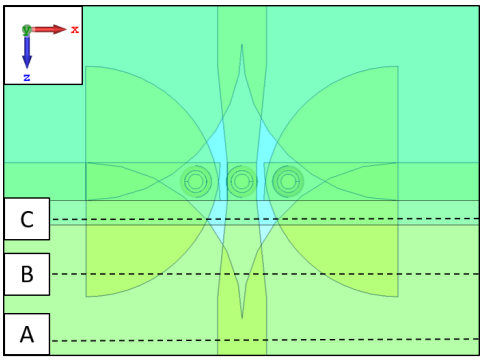
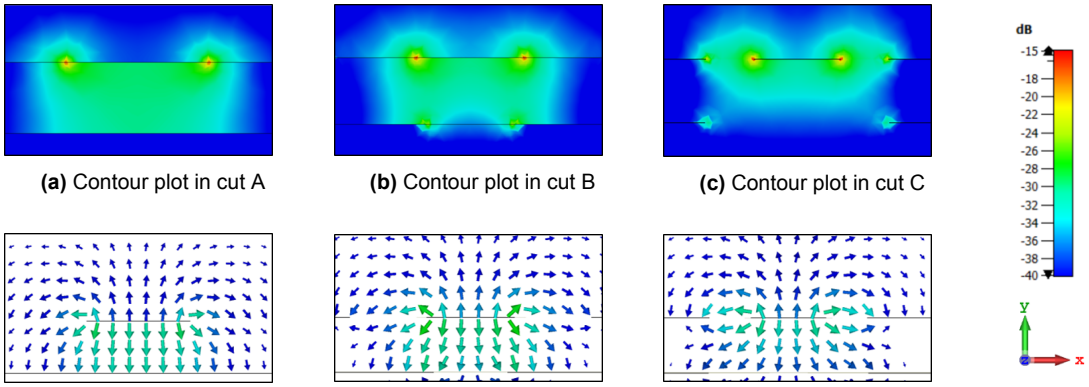


Figure 2.12: Top view (xz-plane) of the via-less Flip-Chip microstrip interconnection, with A, B, and C indicating different xy-cuts.

In cut A, the field distribution is identified as corresponding to a microstrip, where the field is concentrated between the strip and the ground plane along y. Subsequently, in cut B, the ground plane is truncated in the center part, bending the field in the positive and negative x-direction on both sides. Furthermore, bringing in the CPW ground conductors from both sides also aids in bending the field horizontally. Finally, considering cut C, a CPW field distribution is recognized, as it is concentrated between the center strip and the two ground conductors on the side along x.



(a) Contour plot in cut A **(b)** Contour plot in cut B **(c)** Contour plot in cut C

(d) Vector plot in cut A **(e)** Vector plot in cut B **(f)** Vector plot in cut C **(g)** Color bar, axis

Figure 2.13: 2D Electric field relative to the maximum in xy-cuts A, B, and C, as indicated in Fig. 2.12.

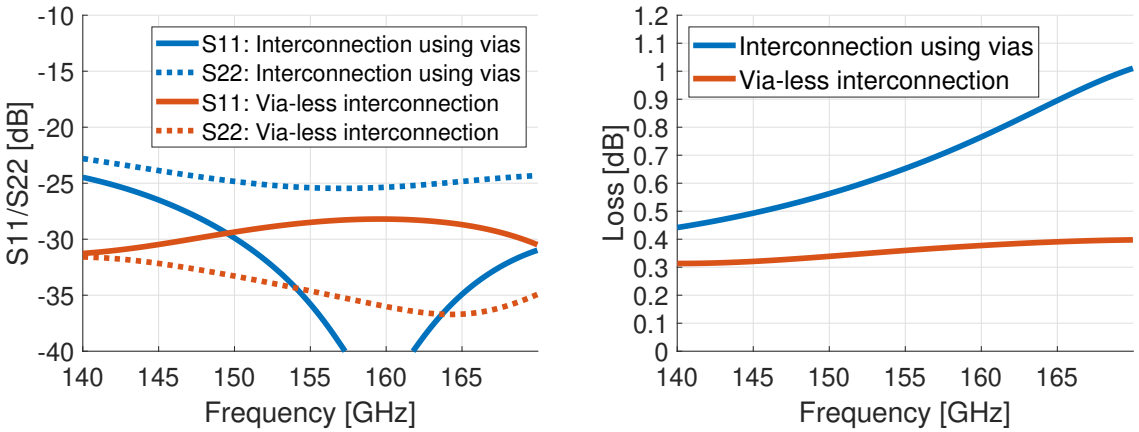
The CPW field pattern in cut B is very similar to the field pattern between the studs. The latter resembles the CPW equivalence of a twin line (or two-wire), as depicted in Fig. 2.14.

(a) Contour plot **(b)** Vector plot

Figure 2.14: 2D Electric field relative to the maximum in the xy-plane of the studs for $y = d/2$, where d is the separation between the two transmission lines or the total height of the studs.

Comparison with interconnection using vias

The comparison of the performance in terms of S11/S22 and radiation loss between the microstrip interconnection using vias and the via-less interconnection is depicted in Fig. 2.15. The matching has slightly improved, while the radiation loss is significantly reduced, from above 1 dB to below 0.5 dB.



(a) S11 and S22 matching

(b) Radiation loss

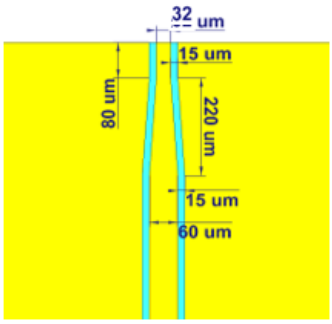
Figure 2.15: Comparison of S11/S22 matching and radiation loss between the flip-chip microstrip interconnection using vias and the via-less interconnection.

The microstrip transmission lines do not add additional radiation to this, unlike in the case of the CPW transmission lines. Furthermore, there is no need for complementary transitions to the microstrip-fed antenna. The via-less microstrip interconnection is therefore considered in the next phase examining the design of the flip-chip interconnection to the MMICs.

2.2. Probe landing transitions

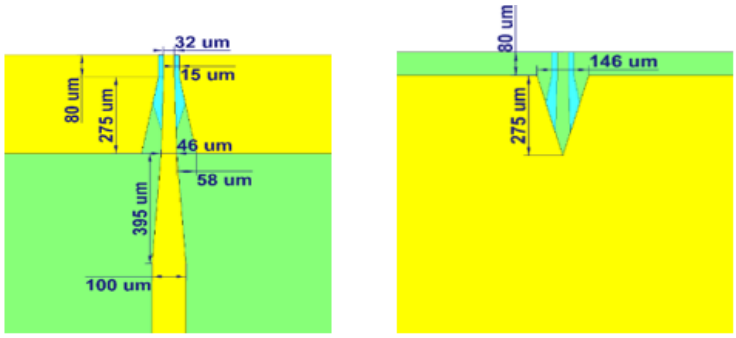
The flip-chip transmission line interconnections discussed in the previous section are implemented in the design of back-to-back test structures that are measured using 50 Ω RF probes with 100 μm pitch. Therefore, transitions from both CPW and microstrip transmission lines to RF probe landing pads are examined.

The landing pads are defined by the RF probes, which excite a CPW mode. The dimensions of the landing pads are reduced to avoid the excitation of the common mode. Firstly, the width of the center strip is reduced to 32 μm, which is the minimal width on which the RF probes are ensured to land successfully. Secondly, the gap between the conductors is reduced to 15 μm, in accordance with the fabrication limitations. Lastly, the CPW transmission line is tapered from 60 μm to 32 μm for landing the RF probes, as depicted in Fig. 2.16. The length of the pads is 80 μm to leave sufficient space for landing the probe. However, in the case of the microstrip transmission line, a transition to a CPW transmission line is required to be designed. The resulting probe landing transition, including the dimensions, is depicted in Fig. 2.17.



(a) Top view

Figure 2.16: CPW probe landing transition

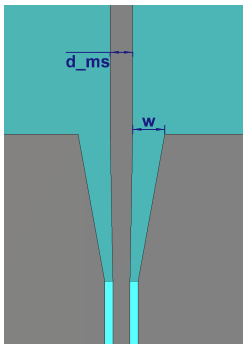


(b) Bottom view

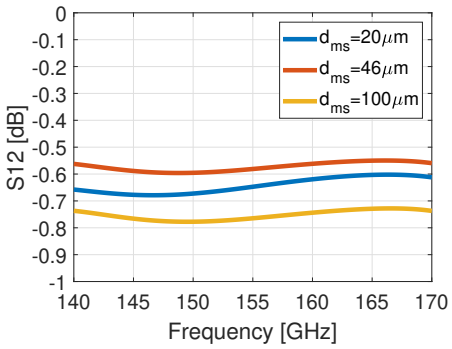
Figure 2.17: Microstrip probe landing transition

Optimization of microstrip to CPW transition

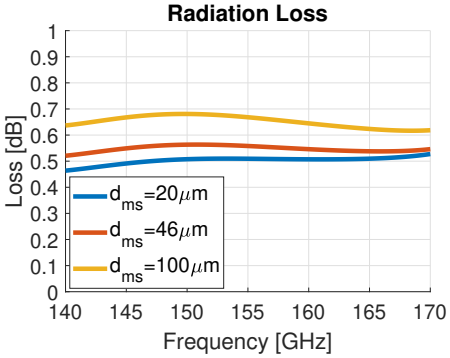
Before arriving at the final design, the transition from microstrip to CPW was optimized in terms of the S12, minimizing both radiation and mismatch. Therefore, the geometry depicted in Fig. 2.18a was simulated in CST. The CPW central strip is tapered to a width d_{ms} at the beginning of the microstrip. As shown in Fig. 2.18b, the S12 is optimal for $d_{ms} = 46$ μm. The radiation loss increases when d_{ms} is incremented in the first place, as displayed in Fig. 2.18c. Increasing d_{ms} widens the CPW over the transition, leading to the excitation of more surface waves.



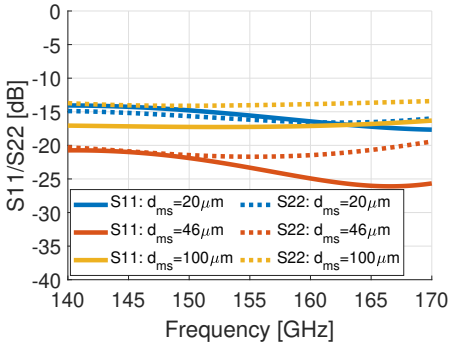
(a) Drawing



(b) S12



(c) Radiation losses



(d) S11/S22 matching

Figure 2.18: Optimization of d_{ms} of the microstrip to CPW transition for probe landing.

In the second place, both increasing and decreasing d_{ms} from its optimal value causes S11/S22 mismatch, as presented in Fig. 2.18d. This mismatch is due to the change in the characteristic impedance of the microstrip. The characteristic impedance is around 80 Ω for $d_{ms} = 46$ μm, which matches the characteristic impedance of the CPW in the taper.

Furthermore, the distance w between the CPW ground and the central strip at the end of the taper (indicated in Fig. 2.18a) was also optimized in terms of the S12, as depicted in Fig. 2.19. Although decreasing w reduces the radiation losses (Fig. 2.20a), a mismatch in S11 and S22 (Fig. 2.20b) is introduced for small w. Thus, there is a trade-off between radiation loss and S11/S22 matching. The optimal value of w, 58 μm was selected.

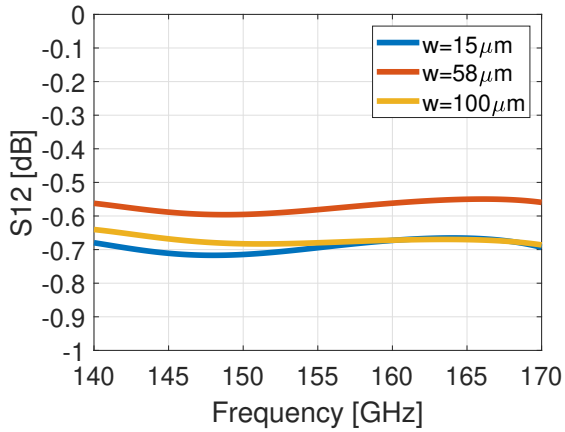
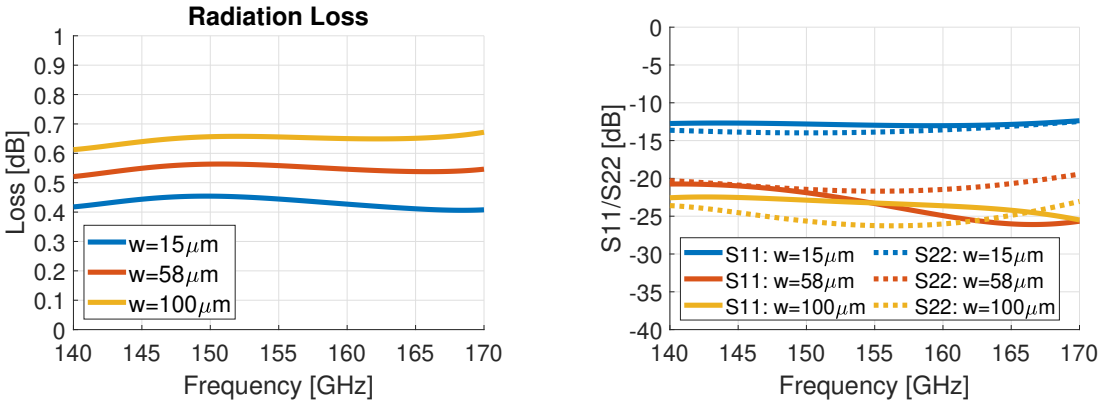


Figure 2.19: Optimization of w of the microstrip to CPW transition for probe landing: S12.

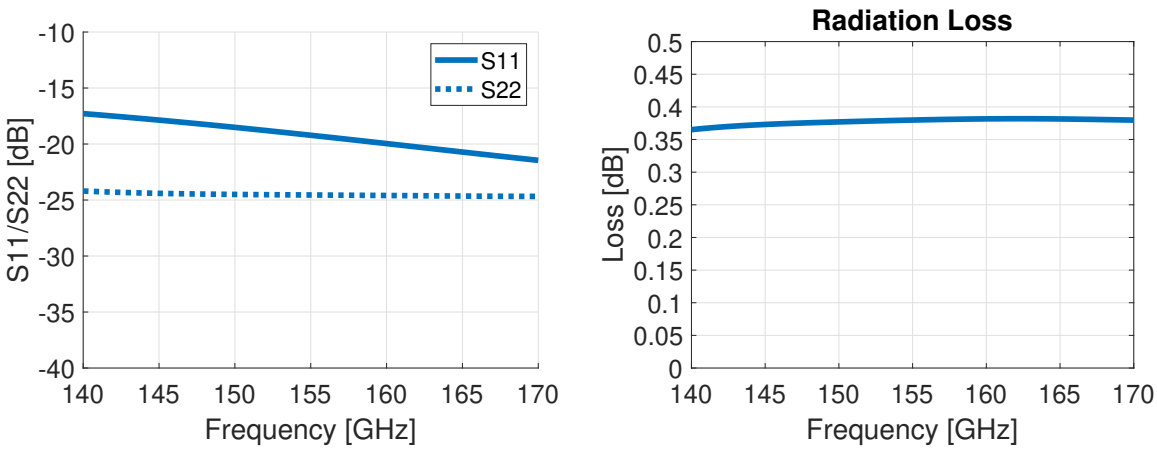


(a) Radiation losses

(b) S11/S22 matching

Figure 2.20: Optimization of w of the microstrip to CPW transition for probe landing.

Subsequently, the microstrip is tapered to a 100 μm wide strip of 50 Ω, used for the antenna feeding. The ground plane is tapered simultaneously, further reducing the radiation. The final resulting geometry was displayed in Fig. 2.17 and the final CST simulation results are shown in Fig. 2.21. The S11/S22 matching is below -15 dB, and the radiation loss is reduced to below 0.4 dB over the frequency range 140-170 GHz.



(a) S11 and S22 matching

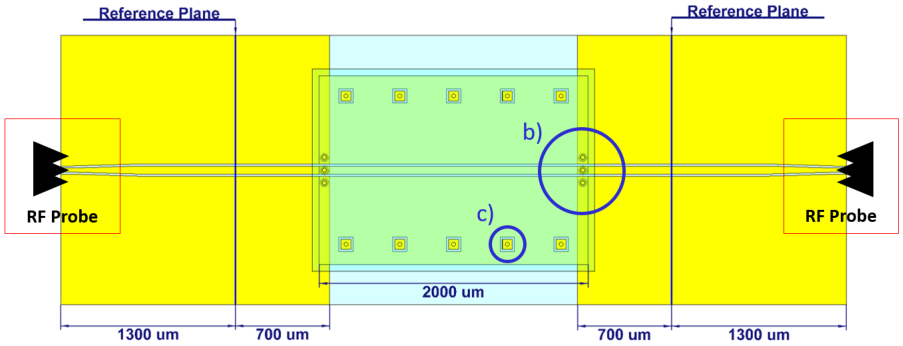
(b) Radiation loss

Figure 2.21: S11/S22 matching and radiation loss of the microstrip probe landing transition

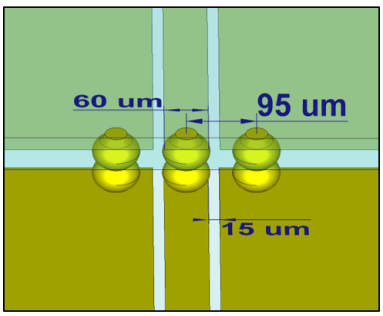
3

Design of Double TRL Test Structures for Flip-Chip Characterization >100 GHz

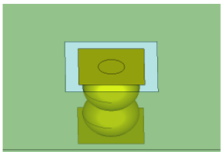
In this chapter, the CPW flip-chip interconnection and probe landing transition analyzed in the previous chapter are implemented in two-port structure configurations, allowing for a calibration de-embedding and accurate extracting of the interconnection response. A small die containing a CPW transmission line is flip-chipped onto a wafer on which the probes are landed, as depicted in Fig. 3.1.



(a) Back-to-back test structure



(b) Flip-chip CPW interconnection



(c) Flip-chip stud for mechanical support

Figure 3.1: Back-to-back CPW test structure for measuring the electrical performance of the flip-chip CPW interconnection.

The extraction of the interconnection response for the developed test structures is realized using a double Thru-Reflect-Line calibration. In Section 3.1, the calibration procedure is explained, and the motivation for using the TRL procedure is provided.

The first TRL (TRL1) is required to de-embed the S-parameters between the error boxes. TRL1 is covered in Section 3.2 in two parts. In the first part, the TRL1 design is presented together with the derivation of the necessary equations for the TRL. In the second part of Section 3.2, the implementation of the equations and design is verified using full-wave simulations of the designed structures.

Next, a second TRL (TRL2) is developed to determine the S-parameters of a single flip-chip interconnection from the measurement of the back-to-back structure. In Section 3.3, TRL2 is discussed in four parts. In the first part, the motivation for using TRL2 is provided by demonstrating that the S-parameter bisection is insufficient to determine the S-parameters of one interconnection from the back-to-back structure. The second part of Section 3.3 presents the design of the TRL2 structures, whereas, in the third part, the TRL equations for symmetric error boxes are derived. Finally, in the last part of Section 3.3, the TRL2 implementation of the equations and the design is verified using full-wave simulations.

The last two sections of this chapter cover mask designs, including the TRL1 and TRL2 designs presented in the preceding sections. Section 3.4 contains the design of a large 4-inch wafer of 500 μm-thick fused silica with one metal layer, whereas the design in Section 3.5 features a smaller 1/4-inch wafer of 50 μm-thick and with two metal layers.

3.1. The TRL calibration procedure

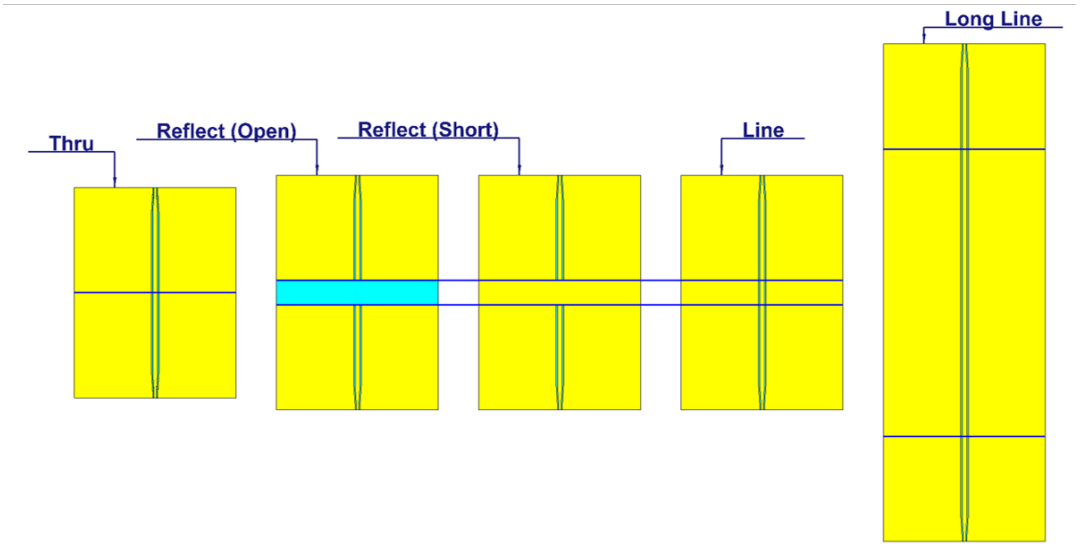
The RF probes are connected to a vector network analyzer (VNA) with frequency multiplier transmit/receive modules, capable of computing the 2-port scattering parameters (or S-parameters), describing reflections and transmission in the network from the VNA's source to load. These include all reflections in the cables and probes, which are not part of the device-under-test (DUT) that is to be measured. The artifacts of the measurement setup are removed, de-embedding the S-parameters of the DUT, using a procedure called calibration, where all the errors are included in the so-called error boxes.

Several calibration procedures were developed for this purpose. A detailed overview of these procedures was presented by Rumiantsev [25]. The first explicit solution for calibrating a two-port VNA by an eight-term model was introduced by Kruppa and Sodomsky [26]. The solution was further modified to yield the ten-term solution, known as short-open-load-thru (SOLT) or thru-open-short-match (TOSM), which is today a well-established technique. Engen and Hoer [27] introduced the thru-reflect-line (TRL) calibration technique, which was the first method not requiring all standards to be ideal or fully known. Line-Reflect-Match (LRM) was developed to improve the bandwidth of the calibration [28]. However, SOLT and Line-Reflect-Match (LRM) are lumped-standard based calibration methods, which give difficulties to achieve reliable measurement results at mm-wave frequencies [25]. After the introduction of the TRL, numerous other self-calibration methods were developed, optimized for different applications.

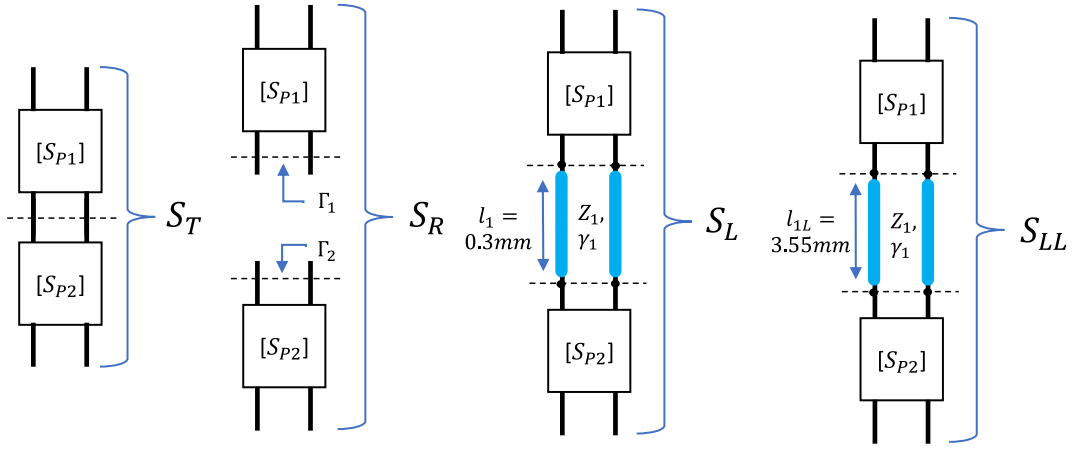
The TRL calibration procedure provides the ability to determine the propagation constant of the line standard. This enables the characterization of fabricated transmission lines required to integrate MMICs. Finally, the TRL calibration method is chosen since it has the least requirement of standards and it does not need lumped standards, like LRM or SOLT.

3.2. TRL to de-embed the S-parameters in between the error boxes (TRL1)

TRL1 consists of 5 structures: a thru, an open and short for the reflect standard, a line, and a long line to characterize the losses, as depicted in Fig. 3.2a. The measured S-parameters for the structures of the TRL are S_T, S_R, S_L, and S_{LL}, corresponding to the thru, reflect, line, and long line, respectively, as indicated in Fig. 3.2b. The error boxes of the TRL are modeled as S-matrix blocks S_{P1} and S_{P2}.



(a) 2D model



(b) Schematic

Figure 3.2: TRL1 structures

For the Thru standard, the error boxes are directly connected, and the reference planes coin-

cide, while for the Reflect and Line standards, the reference planes are separated by a certain length l_1. In the case of the Reflect open (or short), the transmission lines are terminated with an open circuit (or short circuit) at the reference planes. On both sides, a reflection coefficient (Γ_1,Γ_2) defines the Reflect standard. The Line standard has a section of transmission line of length l_1 with characteristic impedance Z_1 and propagation constant $\gamma_1 = \alpha_1 + j\beta_1$, where α_1 is the attenuation constant (losses) and β_1 the phase constant. The long line only differs from the Line standard in length l_{1L}. The length of the Line standard l_1 has to be $\lambda/4$ (or 90 degrees) at the center frequency of the bandwidth of interest. This length is required to distinguish the Line standard from the Thru in terms of phase constant β over the entire bandwidth of interest. Therefore, a length $l_1 = 300\mu$m was selected, which is around $\lambda/4$ at the center frequency. Furthermore, the reflection coefficients Γ_1 and Γ_2 have to be known within $\pm 90°$. However, the exact values are determined by the TRL.

3.2.1. TRL procedure used for TRL1

The TRL derivations and equations given in this section were first introduced by Engen and Hoer [27]. The equations are written in this section as they were implemented in MATLAB, relating them to the designed TRL1 structures.

The S-parameters of two-ports relate the reflected wave amplitudes b_1 and b_2 to the the incident wave amplitudes a_1 and a_2, by

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{3.1a}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{3.1b}$$

At this point, it is convenient to convert to either transmission matrices (ABCD-parameters) or scattering transfer parameters (T-parameters). The advantage of both over S-parameters is the property to achieve the network parameters of two cascaded two-ports by computing the matrix product of the individual network parameter matrices. However, T-parameters, like S-parameters, relate incident and reflected waves, while ABCD-parameters relate voltages and currents. Therefore, to convert from S-parameters to ABCD-parameters, the complex frequency-dependent source and load impedances are required to be known, unlike T-parameters [29]. Therefore, T-parameters are used at this point.

S-parameters to T-parameters conversion

The T-parameters are found from the S-parameters by rewriting Equation (3.1a) and Equation (3.1b) for b_1 and a_1 as a function of a_2 and b_2, as

$$b_1 = -\frac{\det(S)}{S_{21}}a_2 + \frac{S_{11}}{S_{21}}b_2 = T_{11}a_2 + T_{12}b_2 \tag{3.2a}$$

$$a_1 = -\frac{S_{22}}{S_{21}}a_2 + \frac{1}{S_{21}}b_2 = T_{21}a_2 + T_{22}b_2 \tag{3.2b}$$

where $\det(S)$ indicates the determinant of S. The T-parameters T_T, T_R, T_L, T_{LL}, T_{P1}, and T_{P2} are obtained from the S-parameters S_T, S_R, S_L, S_{LL}, S_{P1}, and S_{P2} respectively, using Equation (3.2a) and Equation (3.2b).

T-parameters representation of the Thru and Line connections

Then, the Thru and Line connections as depicted in Fig. 3.2b are written by cascading the T-matrices as

$$T_T = T_{P1} T_{P2} \tag{3.3}$$

$$T_L = T_{P1} \begin{bmatrix} e^{-\gamma_1 l_1} & 0 \\ 0 & e^{\gamma_1 l_1} \end{bmatrix} T_{P2} \tag{3.4}$$

where the transmission line between the error boxes of the Line standard is assumed to be non-reflecting. T_{P2} is eliminated by solving Equation (3.3) for T_{P2} and substituting it into Equation (3.4), yielding

$$T_C T_{P1} = T_{P1} \begin{bmatrix} e^{-\gamma_1 l_1} & 0 \\ 0 & e^{\gamma_1 l_1} \end{bmatrix} \tag{3.5}$$

where

$$T_C = T_L T_T^{-1} \tag{3.6}$$

T_C is computed from the known T_L and T_T (computed from S_L and S_T obtained from the measurements), while T_{P1} and γ_1 remain unknown. Expanding Equation (3.5), where the elements of T_C and T_{P1} are represented as $t_{C,ij}$ and $t_{P1,ij}$ respectively gives

$$t_{C,11} t_{P1,11} + t_{C,12} t_{P1,21} = t_{P1,11} e^{-\gamma_1 l_1} \tag{3.7a}$$

$$t_{C,21} t_{P1,11} + t_{C,22} t_{P1,21} = t_{P1,21} e^{-\gamma_1 l_1} \tag{3.7b}$$

$$t_{C,11} t_{P1,12} + t_{C,12} t_{P1,22} = t_{P1,12} e^{\gamma_1 l_1} \tag{3.7c}$$

$$t_{C,21} t_{P1,12} + t_{C,22} t_{P1,22} = t_{P1,22} e^{\gamma_1 l_1} \tag{3.7d}$$

Equation (3.7a) is solved for $e^{-\gamma_1 l_1}$ and then substituted into Equation (3.7b), while Equation (3.7c) is solved for $e^{\gamma_1 l_1}$ and substituted into Equation (3.7d). This gives the following quadratic equations

$$t_{C,21} \left(\frac{t_{P1,11}}{t_{P1,21}} \right)^2 + (t_{C,22} - t_{C,11}) \frac{t_{P1,11}}{t_{P1,21}} - t_{C,12} = 0 \tag{3.8a}$$

$$t_{C,21} \left(\frac{t_{P1,12}}{t_{P1,22}} \right)^2 + (t_{C,22} - t_{C,11}) \frac{t_{P1,12}}{t_{P1,21}} - t_{C,12} = 0 \tag{3.8b}$$

Root choice and solution of γ_1

It is noted that Equation (3.8a) and Equation (3.8b) have the same known coefficients and therefore yield two of the same solutions. Engen and Hoer [27] argue that in any case

$$\left| \frac{t_{P1,12}}{t_{P1,22}} \right| < \left| \frac{t_{P1,11}}{t_{P1,21}} \right| \tag{3.9}$$

has to hold for practical measurement systems. Therefore, the smallest solution of the quadratic equation is selected for $\frac{t_{P1,12}}{t_{P1,22}}$, and the largest for $\frac{t_{P1,11}}{t_{P1,21}}$. All four Equations (3.7a)-(3.7d) may be solved for γ_1, expressed in terms of the elements of T_C and the ratios $\frac{t_{P1,12}}{t_{P1,22}}$ or $\frac{t_{P1,11}}{t_{P1,21}}$. Equation

3.7c was implemented to find β_1 as

$$\beta_1 = \Im\left(\ln\left(t_{C,11} + \frac{t_{P1,22}}{t_{P1,21}} t_{C,12}\right)\right) \tag{3.10}$$

α_1 is obtained by replacing T_L by T_{LL} in Equation (3.6). This gives

$$T_C^* = T_{LL} T_T^{-1} \tag{3.11}$$

Then α_1 is found by

$$\alpha_1 = \Re\left(\ln\left(t_{C,11}^* + \frac{t_{P1,22}}{t_{P1,21}} t_{C,12}^*\right)\right) \tag{3.12}$$

Solution of de-embedded T-parameters in between the error boxes

Any measured device-under-test (DUT) may be modeled using S-parameter boxes, as depicted in Fig. 3.3, where the error boxes are denoted by S_{P1} and S_{P2}. Using the TRL, S_x is de-embedded from S_M, the latter denoting the measured S-parameters.

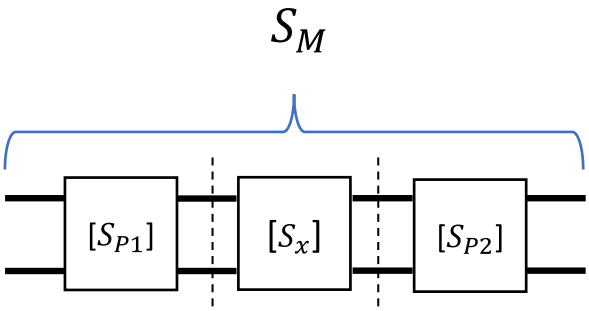


Figure 3.3: Schematic of a measured DUT structure

S_M and S_X are converted to scattering transfer parameters T_M and T_X using Equation (3.2a) and Equation (3.2b). T_M is decomposed into the cascaded elements as

$$T_M = T_{P1} T_X T_{P2} \tag{3.13}$$

T_{P1} and T_{P2} are rewritten in terms of the elements, as

$$T_M = t_{P1,22} t_{P2,22} \begin{bmatrix} \frac{t_{P1,11}}{t_{P1,22}} & \frac{t_{P1,12}}{t_{P1,22}} \\ \frac{t_{P1,21}}{t_{P1,22}} & 1 \end{bmatrix} T_X \begin{bmatrix} \frac{t_{P2,11}}{t_{P2,22}} & \frac{t_{P2,12}}{t_{P2,22}} \\ \frac{t_{P2,21}}{t_{P2,22}} & 1 \end{bmatrix} \tag{3.14}$$

And then after solving for T_X and inverting the matrices,

$$T_X = \frac{1}{t_{P1,22} t_{P2,22}} \frac{1}{\frac{t_{P1,11}}{t_{P1,22}} - \frac{t_{P1,12}}{t_{P1,22}} \frac{t_{P1,21}}{t_{P1,22}}} \frac{1}{\frac{t_{P2,11}}{t_{P2,22}} - \frac{t_{P2,12}}{t_{P2,22}} \frac{t_{P2,21}}{t_{P2,22}}} \begin{bmatrix} 1 & -\frac{t_{P1,12}}{t_{P1,22}} \\ -\frac{t_{P1,21}}{t_{P1,22}} & \frac{t_{P1,11}}{t_{P1,22}} \end{bmatrix} T_M \begin{bmatrix} 1 & -\frac{t_{P2,12}}{t_{P2,22}} \\ -\frac{t_{P2,21}}{t_{P2,22}} & \frac{t_{P2,11}}{t_{P2,22}} \end{bmatrix} \tag{3.15}$$

Equation (3.3), is also written in a similar way as Equation (3.14), as

$$t_{T,22} \begin{bmatrix} \frac{t_{T,11}}{t_{T,22}} & \frac{t_{T,12}}{t_{T,22}} \\ \frac{t_{T,21}}{t_{T,22}} & 1 \end{bmatrix} = t_{P1,22} t_{P2,22} \begin{bmatrix} \frac{t_{P1,11}}{t_{P1,22}} & \frac{t_{P1,12}}{t_{P1,22}} \\ \frac{t_{P1,21}}{t_{P1,22}} & 1 \end{bmatrix} \begin{bmatrix} \frac{t_{P2,11}}{t_{P2,22}} & \frac{t_{P2,12}}{t_{P2,22}} \\ \frac{t_{P2,21}}{t_{P2,22}} & 1 \end{bmatrix} \tag{3.16}$$

which is rewritten as

$$t_{P1,22}t_{P2,22}I = t_{T,22}\frac{1}{\frac{t_{P1,11}}{t_{P1,22}} - \frac{t_{P1,12}}{t_{P1,22}}\frac{t_{P1,21}}{t_{P1,22}}}\frac{1}{\frac{t_{P2,11}}{t_{P2,22}} - \frac{t_{P2,12}}{t_{P2,22}}\frac{t_{P2,21}}{t_{P2,22}}}\begin{bmatrix} 1 & -\frac{t_{P1,12}}{t_{P1,22}} \\ -\frac{t_{P1,21}}{t_{P1,22}} & \frac{t_{P1,11}}{t_{P1,22}} \end{bmatrix}\begin{bmatrix} \frac{t_{T,11}}{t_{T,22}} & \frac{t_{T,12}}{t_{T,22}} \\ \frac{t_{T,21}}{t_{T,22}} & 1 \end{bmatrix}\begin{bmatrix} 1 & -\frac{t_{P2,12}}{t_{P2,22}} \\ -\frac{t_{P2,21}}{t_{P2,22}} & \frac{t_{P2,11}}{t_{P2,22}} \end{bmatrix} \tag{3.17}$$

This means only the 6 ratios are required to be determined: $\frac{t_{P1,11}}{t_{P1,22}}$, $\frac{t_{P1,12}}{t_{P1,22}}$, $\frac{t_{P1,21}}{t_{P1,22}}$, $\frac{t_{P2,11}}{t_{P2,22}}$, $\frac{t_{P2,12}}{t_{P2,22}}$, and $\frac{t_{P2,21}}{t_{P2,22}}$. Then, Equation 3.17 gives the product $t_{P1,22}t_{P2,22}$, which value is required to find T_X from Equation 3.15.

Rewriting the T-parameters expansion of the Thru to find the 6 unknown ratios

Equation (3.16) is premultiplied by T_{P1}^{-1}, as

$$t_{T,22}\frac{1}{\frac{t_{P1,11}}{t_{P1,22}} - \frac{t_{P1,12}}{t_{P1,22}}\frac{t_{P1,21}}{t_{P1,22}}}\begin{bmatrix} 1 & -\frac{t_{P1,12}}{t_{P1,22}} \\ -\frac{t_{P1,21}}{t_{P1,22}} & \frac{t_{P1,11}}{t_{P1,22}} \end{bmatrix}\begin{bmatrix} \frac{t_{T,11}}{t_{T,22}} & \frac{t_{T,12}}{t_{T,22}} \\ \frac{t_{T,21}}{t_{T,22}} & 1 \end{bmatrix} = t_{P2,22}\begin{bmatrix} \frac{t_{P2,11}}{t_{P2,22}} & \frac{t_{P2,12}}{t_{P2,22}} \\ \frac{t_{P2,21}}{t_{P2,22}} & 1 \end{bmatrix} \tag{3.18}$$

Then matrix multiplication on the left-hand side is performed, and $t_{P2,22}$ is placed on the left-hand side, yielding

$$\frac{t_{T,22}}{t_{P2,22}}\frac{1}{\frac{t_{P1,11}}{t_{P1,22}} - \frac{t_{P1,12}}{t_{P1,22}}\frac{t_{P1,21}}{t_{P1,22}}}\begin{bmatrix} \frac{t_{T,11}}{t_{T,22}} - \frac{t_{P1,12}}{t_{P1,22}}\frac{t_{T,21}}{t_{T,22}} & \frac{t_{T,12}}{t_{T,22}} - \frac{t_{P1,12}}{t_{P1,22}} \\ -\frac{t_{P1,21}}{t_{P1,22}}\frac{t_{T,11}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,22}}\frac{t_{T,21}}{t_{T,22}} & -\frac{t_{P1,21}}{t_{P1,22}}\frac{t_{T,12}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,22}} \end{bmatrix} = \begin{bmatrix} \frac{t_{P2,11}}{t_{P2,22}} & \frac{t_{P2,12}}{t_{P2,22}} \\ \frac{t_{P2,21}}{t_{P2,22}} & 1 \end{bmatrix} \tag{3.19}$$

The matrix elements are equated, giving

$$\frac{t_{P2,11}}{t_{P2,22}} = k\left(\frac{t_{T,11}}{t_{T,22}} - \frac{t_{P1,12}}{t_{P1,22}}\frac{t_{T,21}}{t_{T,22}}\right) \tag{3.20a}$$

$$\frac{t_{P2,12}}{t_{P2,22}} = k\left(\frac{t_{T,12}}{t_{T,22}} - \frac{t_{P1,12}}{t_{P1,22}}\right) \tag{3.20b}$$

$$\frac{t_{P2,21}}{t_{P2,22}} = k\left(-\frac{t_{P1,21}}{t_{P1,22}}\frac{t_{T,11}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,22}}\frac{t_{T,21}}{t_{T,22}}\right) \tag{3.20c}$$

$$1 = k\left(-\frac{t_{P1,21}}{t_{P1,22}}\frac{t_{T,12}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,22}}\right) \tag{3.20d}$$

where

$$k = \frac{t_{T,22}}{t_{P2,22}}\frac{1}{\frac{t_{P1,11}}{t_{P1,22}} - \frac{t_{P1,12}}{t_{P1,22}}\frac{t_{P1,21}}{t_{P1,22}}} \tag{3.21}$$

To eliminate k and therefore $t_{P2,22}$ from the right-hand side of Equations (3.20a), (3.20b), and (3.20c), Equation (3.20d) is solved for k and then substituted into Equations (3.20a), (3.20b), and (3.20c), yielding

$$\frac{t_{P2,11}}{t_{P2,22}} = \frac{\frac{t_{T,11}}{t_{T,22}} - \frac{t_{P1,12}}{t_{P1,22}}\frac{t_{T,21}}{t_{T,22}}}{-\frac{t_{P1,21}}{t_{P1,22}}\frac{t_{T,12}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,22}}} \tag{3.22a}$$

$$\frac{t_{P2,12}}{t_{P2,22}} = \frac{\frac{t_{T,12}}{t_{T,22}} - \frac{t_{P1,12}}{t_{P1,22}}}{-\frac{t_{P1,21}}{t_{P1,22}}\frac{t_{T,12}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,22}}} \tag{3.22b}$$

$$\frac{t_{P2,21}}{t_{P2,22}} = \frac{-\frac{t_{P1,21}}{t_{P1,22}}\frac{t_{T,11}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,22}}\frac{t_{T,21}}{t_{T,22}}}{-\frac{t_{P1,21}}{t_{P1,22}}\frac{t_{T,12}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,22}}} \tag{3.22c}$$

$\frac{t_{P1,11}}{t_{P1,21}}$ and $\frac{t_{P1,12}}{t_{P1,22}}$ have been determined by solving Equation (3.8a) and Equation (3.8b) respectively, while the elements $t_{T,ij}$ of T_T have been derived from the measured thru matrix S_T. Therefore, it is useful to rewrite Equations (3.22a), (3.22b), and (3.22c) with only known variables on the right hand side, giving

$$\frac{t_{P2,11}}{t_{P2,22}}\frac{t_{P1,21}}{t_{P1,22}} = \frac{\frac{t_{T,11}}{t_{T,22}} - \frac{t_{P1,12}}{t_{P1,22}}\frac{t_{T,21}}{t_{T,22}}}{-\frac{t_{T,12}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,21}}} \tag{3.23a}$$

$$\frac{t_{P2,12}}{t_{P2,22}}\frac{t_{P1,21}}{t_{P1,22}} = \frac{\frac{t_{T,12}}{t_{T,22}} - \frac{t_{P1,12}}{t_{P1,22}}}{-\frac{t_{T,12}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,21}}} \tag{3.23b}$$

$$\frac{t_{P2,21}}{t_{P2,22}} = \frac{-\frac{t_{T,11}}{t_{T,22}} + \frac{t_{T,21}}{t_{T,22}}}{-\frac{t_{T,12}}{t_{T,22}} + \frac{t_{P1,11}}{t_{P1,21}}} \tag{3.23c}$$

Relating reflection coefficients of the Reflect standard to determine $\frac{t_{P1,21}}{t_{P1,22}}$

The other ratios on the left-hand side may be computed when the ratio of $\frac{t_{P1,21}}{t_{P1,22}}$ is known. For this, the Reflect standard is considered, relating the input reflection coefficient $s_{R,11}$ to Γ_1 and $s_{R,22}$ to Γ_2, as indicated in Fig. 3.2b. For error box P1, the incident wave amplitudes are $a_{P1,1}$ and $a_{P1,2}$, while the reflected wave amplitudes are $b_{P1,1}$ and $b_{P1,2}$. Then the reflection coefficient at the load is given by:

$$\Gamma_1 = \frac{a_{P1,2}}{b_{P1,2}} \tag{3.24}$$

The wave amplitudes are related to the T-parameters by Equation (3.2a) and Equation (3.2b). Using these equations and Equation (3.24), the input reflection coefficient of the Reflect standard is written as:

$$\begin{aligned} s_{R,11} &= \frac{b_{P1,1}}{a_{P1,1}} \\ &= \frac{t_{P1,11}a_{P1,2} + t_{P1,12}b_{P1,2}}{t_{P1,21}a_{P1,2} + t_{P1,22}b_{P1,2}} \\ &= \frac{t_{P1,11}\Gamma_1 + t_{P1,12}}{t_{P1,21}\Gamma_1 + t_{P1,22}} \end{aligned} \tag{3.25}$$

Solving Equation (3.25) for Γ_1 gives

$$\Gamma_1 = \frac{s_{R,11} - \frac{t_{P1,12}}{t_{P1,22}}}{-\frac{t_{P1,21}}{t_{P1,22}}s_{R,11} + \frac{t_{P1,11}}{t_{P1,22}}} \tag{3.26}$$

And equivalently, for error box P2,

$$\Gamma_2 = \frac{a_{P2,1}}{b_{P2,1}} \tag{3.27}$$

$$\begin{aligned} s_{R,22} &= \frac{b_{P2,2}}{a_{P2,2}} \\ &= \frac{\frac{t_{P2,11}}{\det(T_{P2})} a_{P2,1} - \frac{t_{P2,21}}{\det(T_{P2})} b_{P2,1}}{-\frac{t_{P2,12}}{\det(T_{P2})} a_{P2,1} + \frac{t_{P2,22}}{\det(T_{P2})} b_{P2,1}} \\ &= \frac{t_{P2,11}\Gamma_2 - t_{P2,21}}{-t_{P2,12}\Gamma_2 + t_{P2,22}} \end{aligned} \tag{3.28}$$

$$\Gamma_2 = \frac{s_{R,22} + \frac{t_{P2,21}}{t_{P2,22}}}{-\frac{t_{P2,12}}{t_{P2,22}} s_{R,22} + \frac{t_{P2,11}}{t_{P2,22}}} \tag{3.29}$$

Since Γ_1 and Γ_2 are unknown but equal, they are eliminated by equating Equation (3.26) and Equation (3.29), giving

$$\frac{t_{P1,21}}{t_{P1,22}} = \pm \sqrt{\frac{\left(s_{R,11} - \frac{t_{P1,12}}{t_{P1,22}}\right)\left(\frac{t_{P2,11}}{t_{P2,22}}\frac{t_{P1,21}}{t_{P1,22}} - \frac{t_{P2,12}}{t_{P2,22}}\frac{t_{P1,21}}{t_{P1,22}} s_{R,22}\right)}{\left(s_{R,22} + \frac{t_{P2,21}}{t_{P2,22}}\right)\left(\frac{t_{P1,11}}{t_{P1,21}} - s_{R,11}\right)}} \tag{3.30}$$

The magnitude of Equation (3.30) has been expressed in terms of the measured reflection coefficients $s_{R,11}$ and $s_{R,22}$, the ratios $\frac{t_{P1,12}}{t_{P1,22}}$ and $\frac{t_{P1,11}}{t_{P1,21}}$ previously computed from Equation (3.8a) and Equation (3.8b), and the expressions from Equations (3.23a)-(3.23c). After computing the magnitude of $\frac{t_{P1,21}}{t_{P1,22}}$, Equation (3.26) is used to check whether the sign of $\frac{t_{P1,21}}{t_{P1,22}}$ is correct, by computing the angle of Γ_1. If the angle is smaller than 90° for the short, or bigger than 90° for the open, the sign has to be changed. $\frac{t_{P2,11}}{t_{P1,22}}$ is computed by multiplying the result of Equation (3.30) by $\frac{t_{P1,11}}{t_{P1,21}}$ previously computed from Equation (3.8a) and Equation (3.8b). $\frac{t_{P2,11}}{t_{P2,22}}$ and $\frac{t_{P2,12}}{t_{P2,22}}$ are found from Equation (3.23a) and (3.23b) using the result of Equation (3.30). Equation (3.17) gives the product $t_{P1,22}t_{P2,22}$ expressed in terms of all ratios that were previously computed. Finally, T_X is computed from Equation (3.15) and S_X is found by using Equation (3.2a) and Equation (3.2b), which finalizes the TRL procedure.

3.2.2. Verification of TRL1 procedure and design

In order to verify the TRL procedure and design, the structures presented in Fig. 3.2a are modeled and simulated in CST, using waveguide ports placed on both ends of the transmission lines. The resulting S-parameters are saved and imported in MATLAB and assigned to variables S_T, S_R, S_L, and S_{LL} for the thru, reflect, line, and long line respectively. The equations from the previous subsection are implemented.

Verification of the propagation constant

The phase constant β_1 is found using Equation (3.10) and the attenuation constant α_1 from Equation (3.12). For comparison, the section of uniform transmission line between the reference planes of the Line standard is simulated in CST as well.

The S-parameters are first converted to ABCD-parameters, using

$$A = \frac{\left(Z_{01}^{*} + S_{11}Z_{01}\right)\left(1 - S_{22}\right) + S_{12}S_{21}Z_{01}}{2S_{21}\left(R_{01}R_{02}\right)^{1/2}} \tag{3.31a}$$

$$B = \frac{\left(Z_{01}^{*} + S_{11}Z_{01}\right)\left(Z_{02}^{*} + S_{22}Z_{02}\right) - S_{12}S_{21}Z_{01}Z_{02}}{2S_{21}\left(R_{01}R_{02}\right)^{1/2}} \tag{3.31b}$$

$$C = \frac{\left(1 - S_{11}\right)\left(1 - S_{22}\right) - S_{12}S_{21}}{2S_{21}\left(R_{01}R_{02}\right)^{1/2}} \tag{3.31c}$$

$$D = \frac{\left(1 - S_{11}\right)\left(Z_{02}^{*} + S_{22}Z_{02}\right) + S_{12}S_{21}Z_{02}}{2S_{21}\left(R_{01}R_{02}\right)^{1/2}} \tag{3.31d}$$

taken from [29]. The asterisks indicate complex conjugate, and $R = \Re(Z_{0i})$. Z_{01} and Z_{02} are the port impedances from CST. The propagation constant γ is then given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh\gamma l & Z\sinh\gamma l \\ \frac{1}{Z}\sinh\gamma l & \cosh\gamma l \end{bmatrix} \tag{3.32}$$

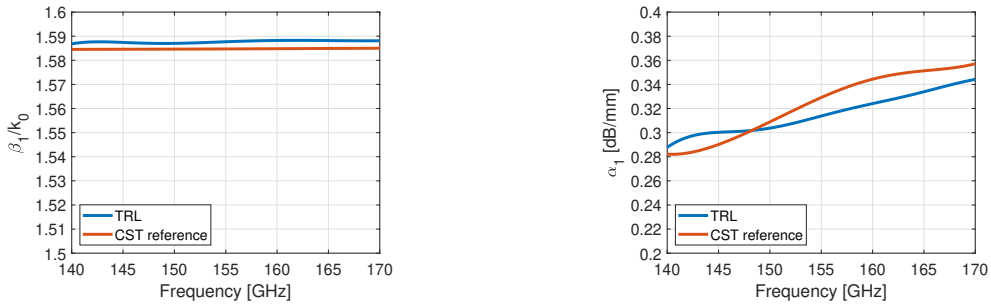
were l is the length of the simulated transmission line [30]. The complex characteristic impedance Z of the simulated transmission line is also found using Equation (3.32). Solving Equation (3.32) for γ and taking the imaginary part gives

$$\beta_{1,REF} = \Im\left(\operatorname{arccosh}(D_{REF})/l\right) \tag{3.33}$$

where D_{REF} corresponds to the 2,2-th element of the ABCD matrix associated with the S-parameters obtained from the reference CST simulation of the uniform line. The attenuation constant is directly found from the S-parameter of a long line simulated in CST, as

$$\alpha_{1,REF} = 10\log_{10}\left(\left|S_{REF,11}\right|^2 + \left|S_{REF,12}\right|^2\right)/l \tag{3.34}$$

The attenuation constant obtained using the TRL is also converted to dB/m by multiplying by $20/\ln(10)$ (≈ 8.686). The results are depicted in Figure 3.4, showing excellent agreement between the results obtained from the implemented equations and CST simulations of the TRL structures and the reference simulation of the uniform transmission line.



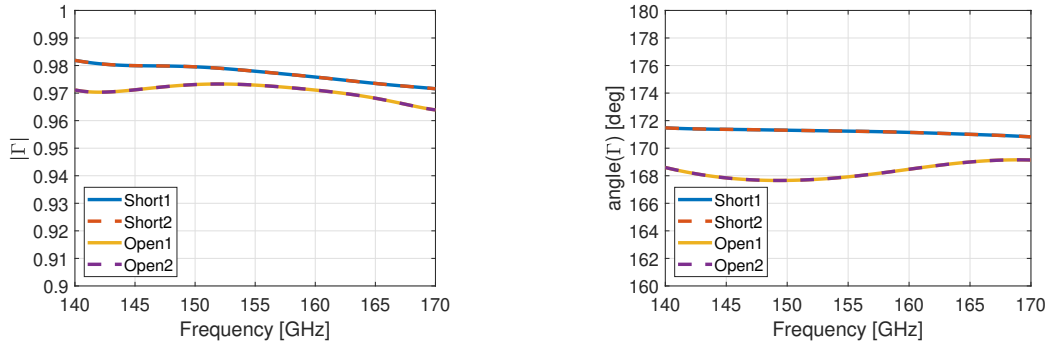
(a) Phase constant over free space wavenumber

(b) Attenuation constant in dB per mm

Figure 3.4: Propagation constant results: using TRL1 equations from simulated TRL1 structures (blue) and simulation of a uniform reference line (red).

Verification of the reflection coefficients and performance of the Reflect standards

The reflection coefficients Γ_1 and Γ_2 are calculated as part of the TRL using Equation (3.26) and Equation (3.29) and indicated in Figure 3.2b. The results for both the Reflect: open circuit and Reflect: short circuit (as indicated in Fig. 3.2a) are presented in Fig. 3.5. Γ_1 and Γ_2 are identical because the structures are perfectly symmetric in the simulated case. An ideal reflect standard means that the magnitude of the reflection coefficient equals 1. Furthermore, for the open circuit, the angle of the reflection coefficient is ideally 0 degrees. Thus, there is 0 degrees phase angle between the incident and reflected waves. On the contrary, for the short circuit, there is 180 degrees phase difference. However, both short and open are non-ideal and the short is performing slightly better than the open. The magnitude and angle of the resulting Γ_1 and Γ_2 are plotted in Fig. 3.5. Short1 and open1 are the reflection coefficient Γ_1 at port 1 for the short and open, whereas short2 and open2 are the reflection coefficient Γ_2 at port 2 for the short and open circuit. For comparison to the short, 180 degrees were added to the angle of the open circuit plotted in Fig. 3.5b.



(a) Magnitude of the reflection coefficients

(b) Angle of the reflection coefficients in degrees, plotted in the range 0-180 deg.

Figure 3.5: Reflection coefficient results obtained using the TRL for both Reflect: short and Reflect: open. 1 and 2 as indicated in Fig. 3.2b. Short1 and open1 are the Γ_1 (reflection coefficient at port 1) for the short and open circuit, whereas short2 and open2 are the Γ_2 (reflection coefficient at port 2) for the short and open circuit.

Verification of the de-embedded S-parameters in between the error boxes

The back-to-back structure designed is represented by S-parameter boxes as shown in Fig. 3.3. The de-embedded subpart of the back-to-back structure is depicted in Fig. 3.6.

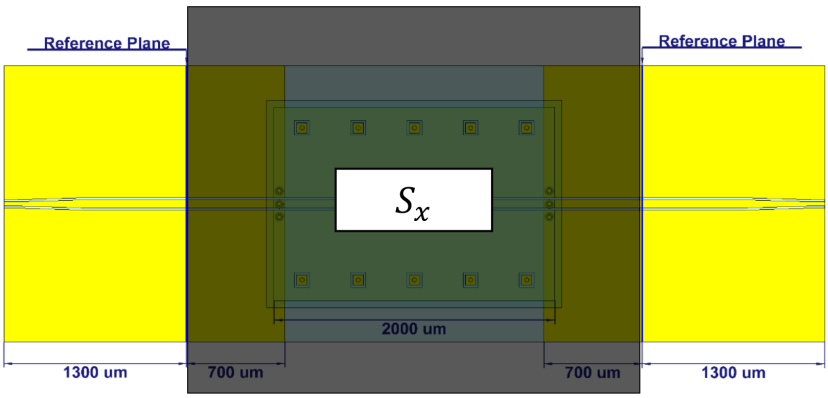


Figure 3.6: Back-to-back test structure with the de-embedded subpart indicated in black

The S-parameters S_X of the highlighted part are obtained using the TRL code and the simulated TRL1 structures. First, the structure was simulated in CST, obtaining S-parameters S_M. Subsequently, S_M was converted to T-parameters T_M using Equation (3.2a) and Equation (3.2b), and T_X was found using Equation (3.15) and converted to S_X. The highlighted part in Fig. 3.6 was also simulated in CST, placing the ports directly on the reference plane locations, and obtaining the CST reference S-parameters. The comparison is depicted in Fig. 3.7 and shows excellent agreement. This agreement verifies the TRL de-embedding code and the designed TRL1 structures.

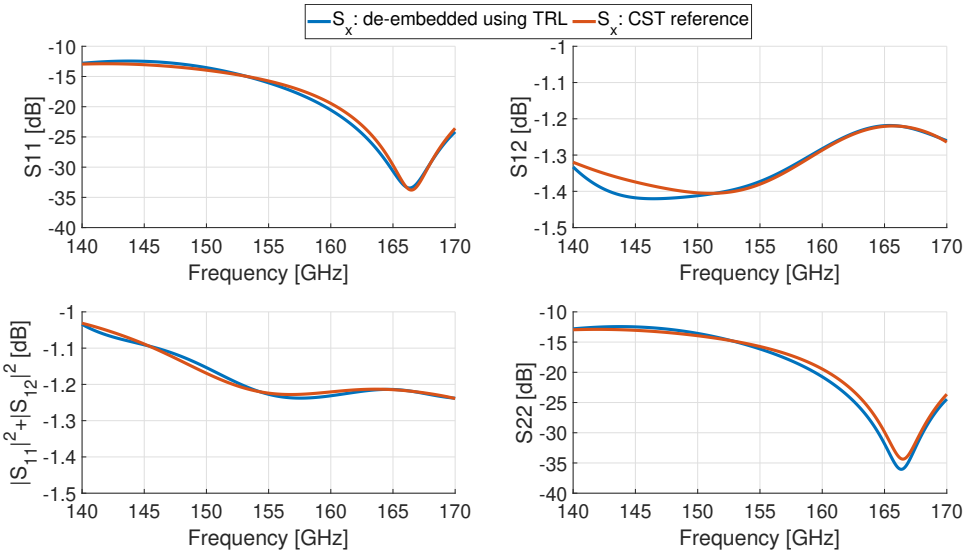
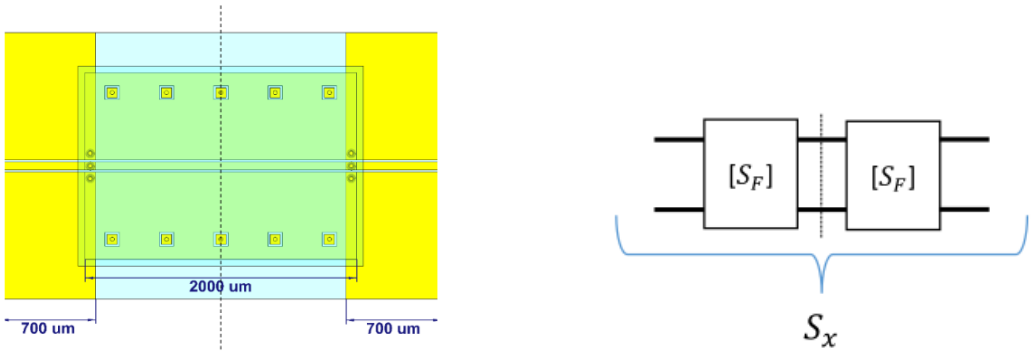


Figure 3.7: Comparison between the de-embedded S-parameters in between the error boxes using TRL1 vs CST reference simulation

3.3. TRL to obtain the S-parameters of a single transition (TRL2)

In the previous section, the S-parameters S_X were de-embedded using TRL1. However, the corresponding subpart (see Fig. 3.8a) contains two flip-chip CPW interconnections. The goal is to obtain the S-parameters of a single interconnection. As denoted in Fig. 3.8, the subpart is symmetric and each half is represented by an S-parameter block S_F.



(a) 2D drawing of the subpart

(b) Schematic of S_X

Figure 3.8: Subpart of back-to-back CPW test structure corresponding to S_X

3.3.1. S-parameter bisection

The first approach is to solve for S_F analytically, by using the method of S-parameter bisection. First, S_X is written as a product using T-parameters as

$$\begin{bmatrix} t_{X,11} & t_{X,12} \\ t_{X,21} & t_{X,22} \end{bmatrix} = \begin{bmatrix} t_{F,11} & t_{F,12} \\ t_{F,21} & t_{F,22} \end{bmatrix} \begin{bmatrix} t_{F,11} & -t_{F,21} \\ -t_{F,12} & t_{F,22} \end{bmatrix} = \begin{bmatrix} t_{F,11}^2 - t_{F,12}^2 & -t_{F,11}t_{F,21} + t_{F,12}t_{F,22} \\ t_{F,11}t_{F,21} - t_{F,12}t_{F,22} & t_{F,22}^2 - t_{F,21}^2 \end{bmatrix} \tag{3.35}$$

where $t_{X,ij}$ are the elements of the T-parameters T_X corresponding to S_X and $t_{F,ij}$ of T_F corresponding to S_F (conversion using Equation (3.2a) and Equation (3.2b)). Since S_X and S_F are reciprocal ($S_{12} = S_{21}$), the determinant of T_X and T_F should be equal to 1. Additionally, S_X is symmetric ($S_{X,11}$ = $S_{X,22}$) and therefore $t_{X,12} = -t_{X,21}$. This gives the following set of nonlinear equations:

$$t_{X,11} = t_{F,11}^2 - t_{F,12}^2 \tag{3.36a}$$

$$t_{X,12} = -t_{F,11}t_{F,21} + t_{F,12}t_{F,22} \tag{3.36b}$$

$$t_{X,21} = t_{F,11}t_{F,21} - t_{F,12}t_{F,22} \tag{3.36c}$$

$$t_{X,22} = t_{F,22}^2 - t_{F,21}^2 \tag{3.36d}$$

It is useful to convert these equations back to S-parameters, giving

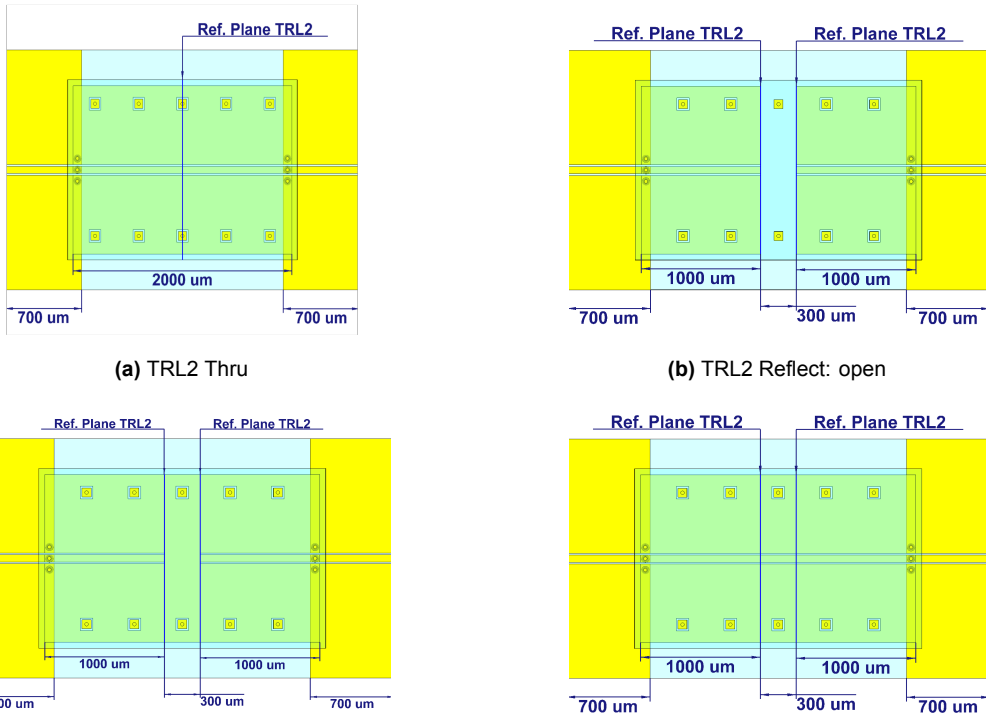
$$S_{X,11} = S_{X,22} = S_{F,11} + \frac{S_{F,22} + S_{F,12}^2}{1 - S_{F,22}^2} \tag{3.37a}$$

$$S_{X,12} = S_{X,21} = \frac{S_{F,12}^2}{1 - S_{F,22}^2} \tag{3.37b}$$

S_X is both symmetric (Equation (3.37a)) and reciprocal (Equation (3.37b)), meaning there are two equations only. However, these equations have multiple physical and passive solutions ($0 < |S_{F,ij}| < 1$) when solved for S_F. This would be sufficient only if S_F itself would be symmetric ($S_{F,11} = S_{F,22}$), which is not the case. Thus, additional structures have to be included, providing another set of equations that allow solving for S_F.

3.3.2. TRL2 design

Designing another TRL does provide one solution for S_F. For this TRL, referred to as TRL2, the reference planes are located on the top structures of the back-to-back design, as indicated in Fig. 3.9 by ”Ref. Plane TRL2”. Four back-to-back test structures are required, which are all de-embedded using the procedure of TRL1 explained in the previous subsection.



(a) TRL2 Thru

(b) TRL2 Reflect: open

(c) TRL2 Reflect: short

(d) TRL2 Line

Figure 3.9: 2D models of the TRL2 structures.

The TRL2 Thru (Fig. 3.9a), Reflect open/short (Fig. 3.9b/Fig. 3.9c), and Line (Fig. 3.9d) are represented by S_{XT}, S_{XR}, and S_{XL} respectively in Fig. 3.10. The error boxes are in this case S_F because the cable and probes have been already de-embedded using TRL1.

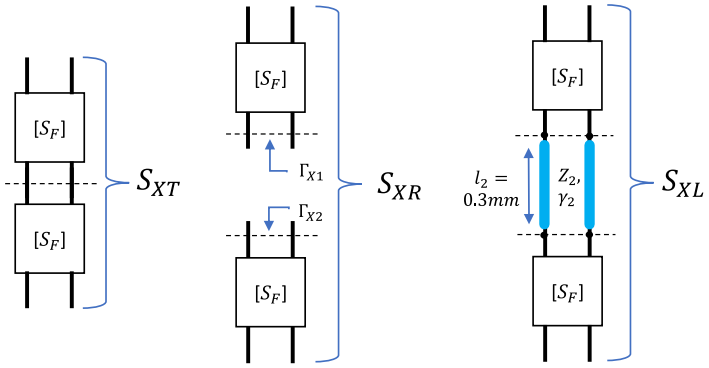


Figure 3.10: Schematic of TRL2 using S-parameter boxes

3.3.3. TRL procedure used for TRL2

The procedure introduced for TRL1 has the advantage that the error boxes do not have to be identical, and it is not required to calculate the S-parameters of the error boxes, only to remove their effect. In the case of TRL2, the S-parameters of the error boxes are of interest. Therefore, the approach is slightly different. S_{XT}, S_{XR} and S_{XL} are first converted to T-parameters T_{XT}, T_{XR}, and T_{XL} respectively, using Equation (3.2a) and Equation (3.2b). T_{XT} and T_{XL} are

written using cascading T-matrices as depicted in Fig. 3.8b, as

$$T_{XT} = \begin{bmatrix} t_{F,11} & t_{F,12} \\ t_{F,21} & t_{F,22} \end{bmatrix} \begin{bmatrix} t_{F,11} & -t_{F,21} \\ -t_{F,12} & t_{F,22} \end{bmatrix} \tag{3.38}$$

$$T_{XL} = \begin{bmatrix} t_{F,11} & t_{F,12} \\ t_{F,21} & t_{F,22} \end{bmatrix} \begin{bmatrix} e^{-\gamma_2 l_2} & 0 \\ 0 & e^{\gamma_2 l_2} \end{bmatrix} \begin{bmatrix} t_{F,11} & -t_{F,21} \\ -t_{F,12} & t_{F,22} \end{bmatrix} \tag{3.39}$$

where $t_{F,ij}$ are the elements of scattering transfer parameters T_F, corresponding to S_F. For Equation (3.38) and Equation (3.39), the second T_F has been written differently, because this S_F is mirrored.

$$t_{XT,11} = t_{F,11}^2 - t_{F,12}^2 \tag{3.40a}$$

$$t_{XT,12} = -t_{F,11}t_{F,21} + t_{F,12}t_{F,22} \tag{3.40b}$$

$$t_{XT,22} = -t_{F,21}^2 + t_{F,22}^2 \tag{3.40c}$$

where by symmetry $t_{XT,12} = -t_{XT,21}$ and by reciprocity $\det(T_{XT}) = 1$. Expanding Equation (3.39) into its elements gives

$$t_{XL,11} = e^{-\gamma_2 l_2} t_{F,11}^2 - e^{\gamma_2 l_2} t_{F,12}^2 \tag{3.41a}$$

$$t_{XL,12} = -e^{-\gamma_2 l_2} t_{F,11} t_{F,21} + e^{\gamma_2 l_2} t_{F,12} t_{F,22} \tag{3.41b}$$

$$t_{XL,22} = -e^{-\gamma_2 l_2} t_{F,21}^2 + e^{\gamma_2 l_2} t_{F,22}^2 \tag{3.41c}$$

When converting back to S-parameters, due to reciprocity ($S_{XT,12} = S_{XT,21}$ and $S_{XL,12} = S_{XL,21}$) and symmetry ($S_{XT,11} = S_{XT,22}$ and $S_{XL,11} = S_{XL,22}$), the resulting equations are

$$S_{XT,11} = S_{F,11} + \frac{S_{F,22} S_{F,12}^2}{1 - S_{F,22}^2} \tag{3.42a}$$

$$S_{XT,12} = \frac{S_{F,12}^2}{1 - S_{F,22}^2} \tag{3.42b}$$

$$S_{XL,11} = S_{F,11} + \frac{S_{F,22} S_{F,12}^2 e^{-2\gamma_2 l_2}}{1 - S_{F,22}^2 e^{-2\gamma_2 l_2}} \tag{3.43a}$$

$$S_{XL,12} = \frac{S_{F,12}^2 e^{-2\gamma_2 l_2}}{1 - S_{F,22}^2 e^{-\gamma_2 l_2}} \tag{3.43b}$$

These four equations are equivalent to ones given by Pozar [30]. The following steps are given by Pozar as well. Equation (3.42b) is solved for $S_{F,12}^2$ and substituted into Equation (3.42a) and Equations (3.43a,b), giving

$$S_{XT,11} = S_{F,11} + \frac{S_{F,22}(1 - S_{F,22}^2) S_{XT,12}}{1 - S_{F,22}^2} \tag{3.44a}$$

$$S_{XL,11} = S_{F,11} + \frac{S_{F,22}(1 - S_{F,22}^2) S_{XT,12} e^{-2\gamma_2 l_2}}{1 - S_{F,22}^2 e^{-2\gamma_2 l_2}} \tag{3.44b}$$

$$S_{XL,12} = \frac{(1 - S_{F,22}^2) S_{XT,12} e^{-2\gamma_2 l_2}}{1 - S_{F,22}^2 e^{-\gamma_2 l_2}} \tag{3.44c}$$

$S_{F,11}$ is eliminated by subtracting Equation (3.44b) from Equation (3.44a), arriving to

$$S_{XT,11} - S_{XL,11} = S_{F,22} S_{XT,12} - \frac{S_{F,22}(1 - S_{F,22}^2) S_{XT,12} e^{-2\gamma_2 l_2}}{1 - S_{F,22}^2 e^{-2\gamma_2 l_2}} \tag{3.45}$$

Solving Equation (3.44c) for $S_{F,22}$ and substituting into Equation (3.45) gives a quadratic equation for $e^{\gamma_2 l_2}$, which solution is given by:

$$e^{\gamma_2 l_2} = \frac{S_{XL,12}^2 + S_{XT,12}^2 - (S_{XT,11}^2 + S_{XL,11}) \pm K}{2 S_{XL,12} S_{XT,12}} \tag{3.46a}$$

$$K = \sqrt{\left[S_{XL,12}^2 + S_{XT,12}^2 - (S_{XT,11} - S_{XL,11})^2\right]^2 - 4 S_{XL,12}^2 S_{XT,12}^2} \tag{3.46b}$$

The choice of the square root is made in the same way as explained for TRL1, using the reflect standard. Equation (3.42b) and Equation (3.42a) are each multiplied by S_{F22} and subtracted from Equation (3.43b) and Equation (3.43a) respectively, giving

$$S_{XT,11} = S_{F,11} + S_{F,22} S_{XT,12} \tag{3.47}$$

$$S_{XL,11} = S_{F,11} + S_{F,22} S_{XL,12} e^{\gamma_2 l_2} \tag{3.48}$$

These results are subtracted from each other, eliminating $S_{F,11}$, and solved for $S_{F,22}$, yielding

$$S_{F,22} = \frac{S_{XT,11} - S_{XL,11}}{S_{XT,12} - S_{XL,12} e^{\gamma_2 l_2}} \tag{3.49}$$

Then Equation (3.47) is solved for $S_{F,11}$, giving

$$S_{F,11} = S_{XT,11} - S_{F,22} S_{XT,12} \tag{3.50}$$

Lastly, Equation (3.42b) is solved for $S_{F,12}^2$, as

$$S_{F,12}^2 = S_{XT,12}(1 - S_{F,22}^2) \tag{3.51}$$

S_F has been fully characterized in terms of S_{XT} and S_{XL}.

3.3.4. Verification of TRL2 MATLAB function and design

The S-parameters of the structures presented in Fig. 3.9 were de-embedded using TRL1 from CST simulations of the full back-to-back structures including the probe landing transitions. Equations (3.46), (3.49), (3.50), and (3.51) were implemented in a MATLAB function to output S_F from input S-parameters S_{XT}, S_{XR}, and S_{XL}. A CST reference simulation, placing one port on the top structure at the dotted line indicated in Fig. 3.8a, was done to evaluate the TRL2 code and designed structures. The result is depicted in Fig. 3.11 and shows good agreement between the simulated results of TRL2 and the reference simulation.

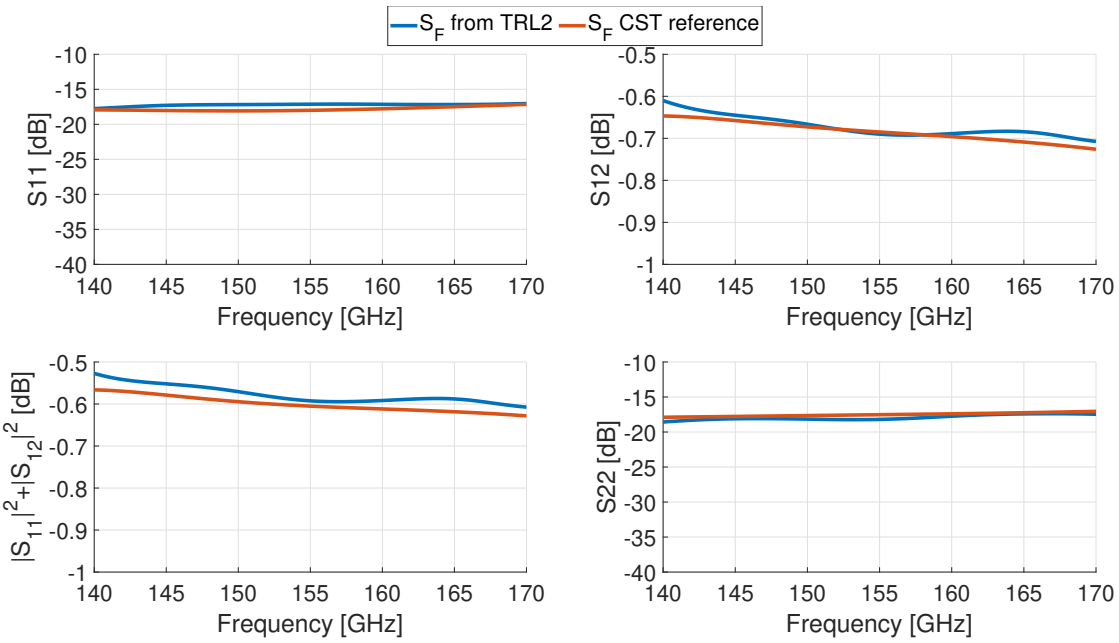
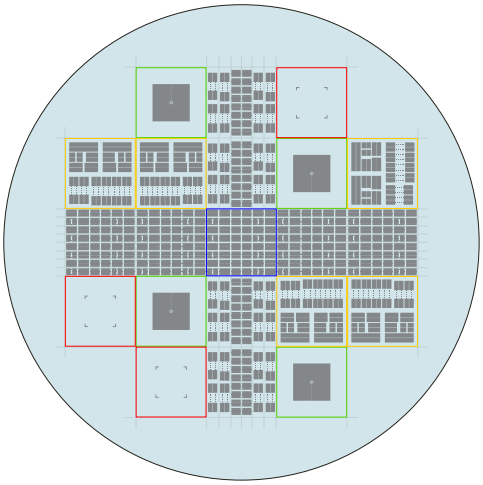


Figure 3.11: Comparison between the resulting S_F found from simulation of the TRL2 back-to-back test structures and the TRL2 MATLAB code vs CST reference simulation.

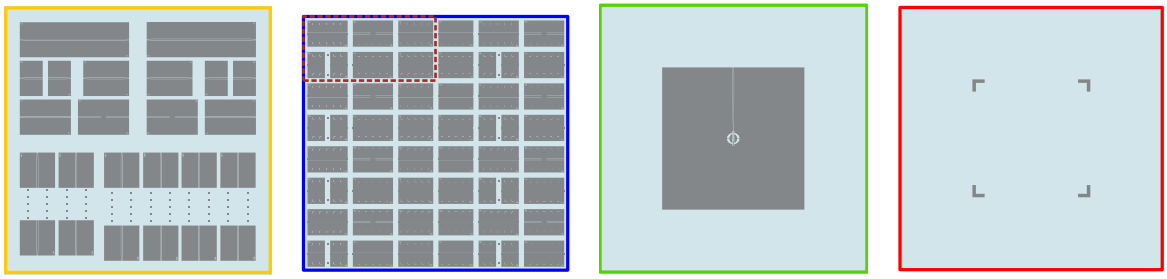
3.4. Mask design on a 4 inch 500 micron-thick fused silica wafer

The test structures for the characterization of the CPW flip-chip transition are fabricated using the capabilities of CITC and Else Kooi Laboratory (EKL), the latter located at the Delft University of Technology. The first step is to design a mask featuring all CPW transmission line structures, placed in one metal layer, which is deposited on a 4-inch (10.21 cm) fused silica wafer of 500 μm-thick. EKL will realize both the aluminum metallization and the dicing of the features. Subsequently, CITC will flip-chip the TRL2 top features onto the TRL2 bottom dies. In Fig. 3.12, the complete mask is depicted, with the components indicated in colored boxes, containing:

- **5$\times$ 15$\times$15 mm^2 die** (Fig. 3.12b, yellow). Top part contains 2$\times$ TRL1 structures: Thru (*T1*), Reflect: open (*O1*), Reflect: short (*S1*), Line (*L1*), and Extra long line (*E1*). Bottom part contains TRL2 bottom: 2$\times$ Thru (*T2B*), 2$\times$ Line ((*L2B*)), Reflect: short (*S2B*), and Reflect: open (*O2B*).
- **32$\times$ 2.4$\times$1.6 mm^2 die containing TRL2 top line/open/short + 16$\times$ 2.1$\times$1.6 mm^2 die containing TRL2 top thru** (Fig. 3.12c, blue). 8 repetitions of TRL2 top structures: 2$\times$ Thru (*T2*), 2$\times$ Line (*L2*), Reflect: short (*S2*), and Reflect: open (*O2*).
- **4$\times$ 15$\times$15 mm^2 die** (Fig. 3.12d, green). CPW antenna design with 8$\times$8 mm^2 ground plane, and transition for probe landing for de-embedding using TRL1.
- **3$\times$ 15$\times$15 mm^2 die** (Fig. 3.12e, red). Alignment marks at 0.25 inch, for placing the microstrip antenna fabricated in ATP.



(a) Total mask overview



(b) TRL1 + TRL2 bottom **(c)** TRL2 top **(d)** CPW antenna **(e)** Carrier microstrip antenna

Figure 3.12: CPW mask design on 4 inch 500μm-thick fused silica wafer using aluminum metallization.

Flip-chip bonding

The features included in the mask indicated in Fig. 3.12c will be diced into 48 small dies and flip-chipped by CITC onto the structure in the bottom part of Fig. 3.12b, as illustrated in Fig. 3.13.

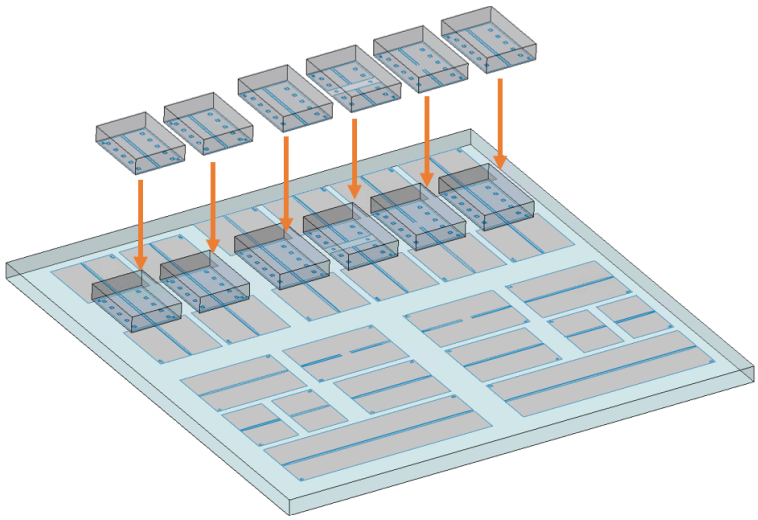
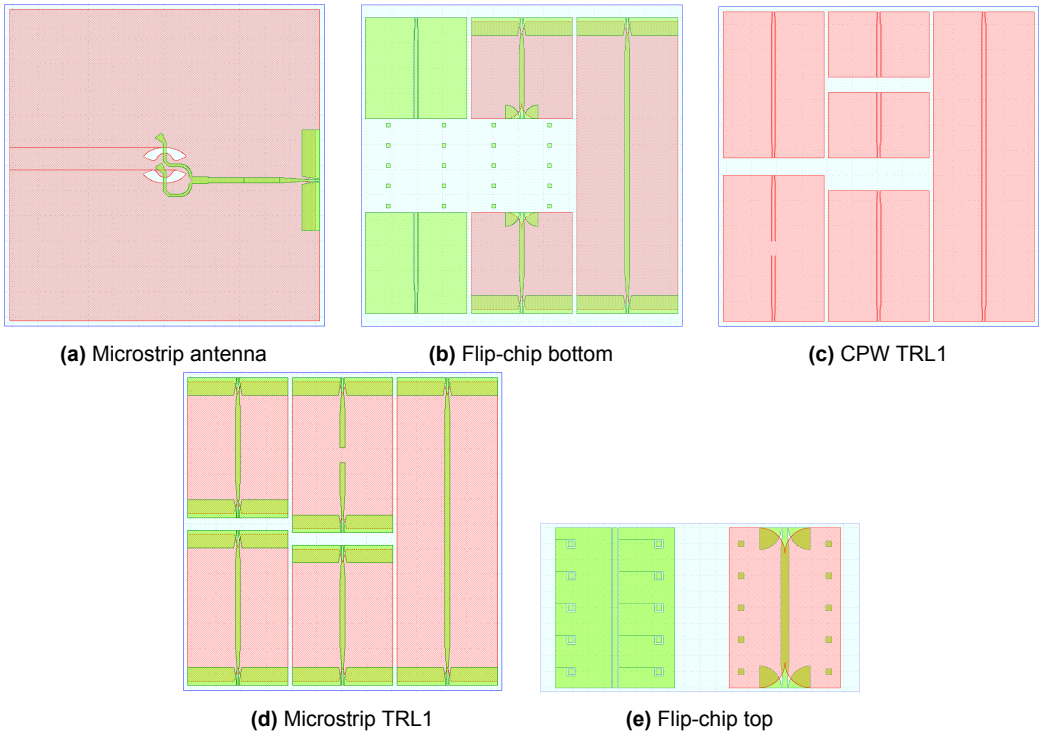


Figure 3.13: Illustration of the flip-chip process for the fabricated features included in the mask

3.5. Mask design on 1/4 inch 50 micron-thick fused silica wafers

A second mask was designed to realize test structures for both via-less microstrip and CPW flip-chip interconnections, discussed in Chapter 2, on a 50 μm-thick fused silica substrate. The microstrip transmission lines require a ground metallization below the 50 μm fused silica layer and the CPW transmission lines require the substrate to be bonded to a 500 μm-thick fused silica carrier, which will also provide structural support.

ATP is capable of delivering 50 μm wafers, although with maximum dimensions of 6.35$\times$6.35 mm^2 per design. This limitation means the CPW and microstrip designs have to be distributed over multiple wafers, as depicted in Fig. 3.14. These designs include the probe landing transitions as presented in Chapter 2. The flip-chip top structures in Fig. 3.14e are intended to be flip-chipped onto the left-most structures in Fig. 3.14b. The S-parameters of these structures and the microstrip antenna in Fig. 3.14a between the error boxes (probe landing transition, probes, cables, etc.), are de-embedded using the TRL1 structures presented in Fig. 3.14c and Fig. 3.14d. However, one disadvantage of this mask design is that it does not feature a TRL2 design. Thus, the S-parameters of a single transition are not obtained using this design. The CPW flip-chip test structures are best suited for the characterization of the flip-chip studs since the CPW mode resembles more the fields between the studs compared to a microstrip mode. Furthermore, the CPW flip-chip test structures are already included in the mask previously presented. Therefore, only the microstrip antenna (Fig. 3.14a) and microstrip TRL1 (Fig. 3.14d) are fabricated for the mask in depicted in Fig. 3.14, reducing costs significantly.



(a) Microstrip antenna **(b)** Flip-chip bottom **(c)** CPW TRL1

(d) Microstrip TRL1 **(e)** Flip-chip top

Figure 3.14: Mask designs on the 50μm-thick fused silica wafer.

4

Flip-Chip Interconnection to commercial MMICs >100 GHz

After studying several symmetric flip-chip interconnections using fused silica wafers in Chapter 2, this chapter extends this work to the flip-chip interconnection between the MMICs and the fused silica wafer. The symmetric flip-chip CPW interconnection and via-less flip-chip microstrip interconnection, derived in Chapter 2, provide a good starting point for the interconnections to the MMICs. Furthermore, the studs are represented by cylinders of diameter 30 μm to reduce the effect of the studs on the S11/S22 mismatch. As discussed in Section 1.2, the chips feature a 33 μm-thick 50 Ω microstrip transmission line on a 50 μm-thick GaAs substrate. The flip-chip studs are placed on the RF connector P2, imported from the DXF-file provided by Gotmic [21].

In Section 4.1, the symmetric CPW interconnection is modified by placing the top wafer to represent the MMIC, and the effect on the S11/S22 matching and losses is studied. Then, the S11/S22 matching is improved by designing a high impedance transmission line section using the Smith Chart. Furthermore, the effect is verified using full-wave simulations. In Section 4.2, the same steps are repeated for the via-less microstrip interconnection. Finally, the final simulated performance is compared to the CPW interconnection to the MMIC.

4.1. Flip-chip interconnection to MMICs using CPW on fused silica

The symmetric flip-chip CPW interconnection introduced in Chapter 2 has been already optimized in terms of radiation losses. The top fused silica wafer in Fig. 2.4a is replaced by a GaAs wafer representing the MMICs, as depicted in Fig. 4.1. The MMIC features a 50 Ω microstrip with pads in a CPW configuration, connected to the ground plane using vias on both sides. Although a CPW transmission line has higher radiation loss per unit length compared to a microstrip, the pads of the MMIC still give an increase in overall radiation loss. As a result, the total radiation is similar to the symmetric CPW case, as depicted in Fig. 4.2b.

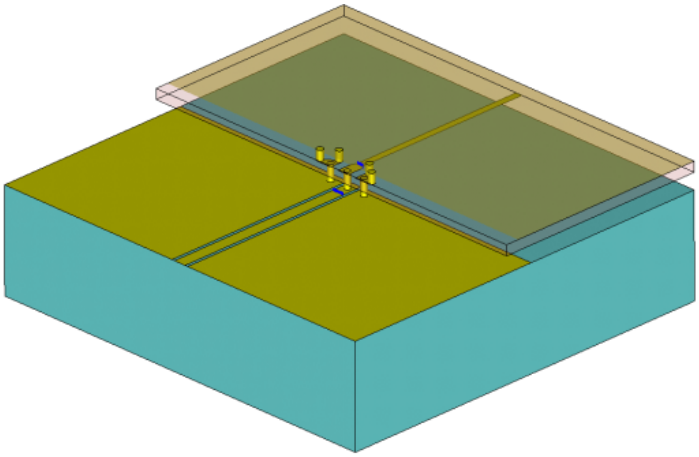
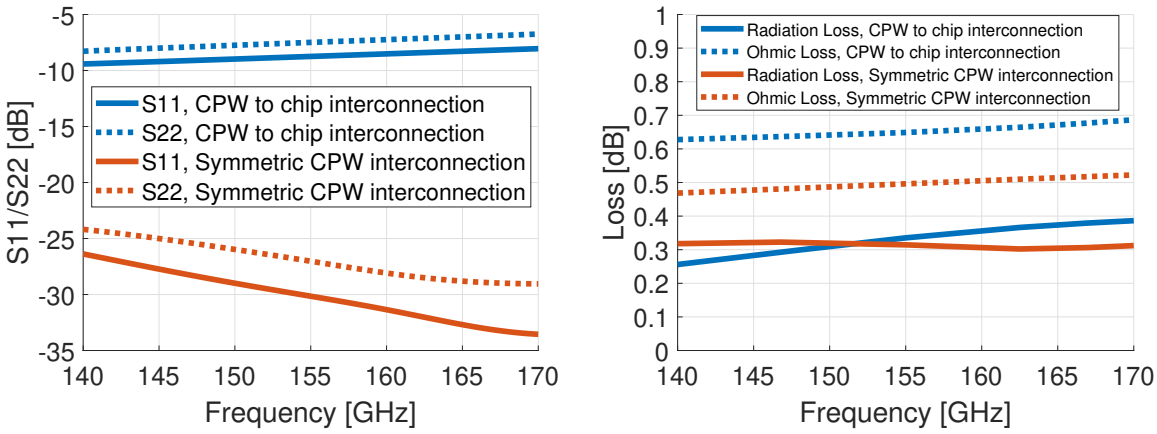


Figure 4.1: 3D model of the flip-chip interconnection to the MMICs using CPW transmission lines on the fused silica and representing the studs by cylinders with a radius of 30 μm. The blue lines indicate the reference planes used for de-embedding the S-parameters of the interconnection.

For the symmetric CPW interconnection considered in Chapter 2, the S11/S22 matching improved to below -20 dB when decreasing the diameter of the studs to 30 μm. When this procedure is repeated for the CPW interconnection to the chip, the S11/S22 matching could not be improved to below -10 dB, as depicted in Fig. 4.2a. Therefore, it is concluded that the S11/S22 mismatch is introduced by the capacitive effect of the pads on the MMICs.



(a) S11 and S22 matching

(b) Radiation loss and Ohmic loss

Figure 4.2: Comparison of the simulated performance in CST between the flip-chip CPW interconnection to the MMICs from Fig. 4.1 and the symmetric CPW interconnection from Fig. 2.4a for cylinder diameter of 30 μm.

S11/S22 mismatch compensation using series high impedance transmission lines

Since the design of the MMICs is fixed, the S11/S22 matching is improved by designing a matching network on the fused silica wafer. The matching network is realized by placing a section of high impedance transmission line in series with the CPW in the fused silica. The length of the high impedance transmission line and its placement relative to the studs are adjusted, optimizing the S11 and S22 matching over the frequency band of interest (140-170 GHz).

De-embedding the flip-chip interconnection

The S-parameters S_{tot} obtained from CST simulations of the 3D model presented in Fig. 4.1 describe the flip-chip CPW interconnection including 1 mm of transmission line on both sides of the transition. Both transmission lines are excited using waveguide ports placed at the endings ensuring virtually perfect matching. Since the transmission lines are both uniform up to the transition, there are practically no reflections up to the blue curves indicated in Fig. 4.1. Both blue lines are separated from the ports by 900 μm, as shown in the corresponding schematic in Fig. 4.3.

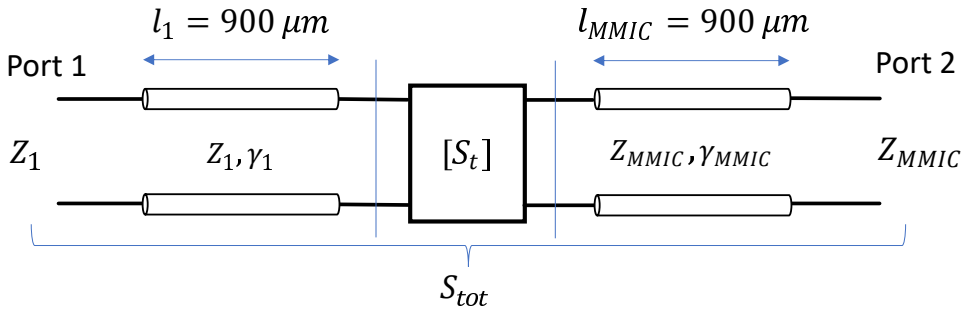


Figure 4.3: Schematic of the simulated flip-chip CPW interconnection to the MMICs. The transmission lines on both sides are de-embedded to obtain the S-parameters of the transition S_t.

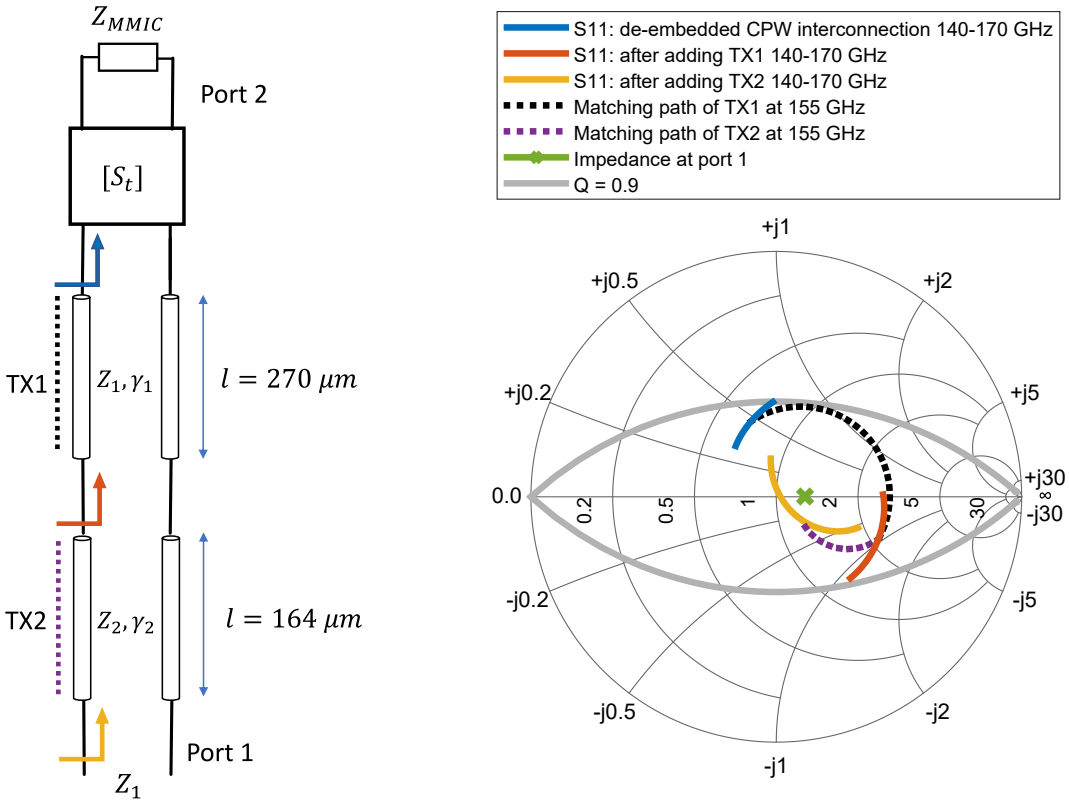
Separate CST simulations of the CPW on the fused silica wafer and the microstrip on the GaAs MMIC were done to obtain Z_1, γ_1, Z_{MMIC}, and γ_{MMIC}. The S-parameters obtained from these simulations were converted to ABCD-parameters using Equations (3.31a-d), preceding the computation of the complex propagation constants and characteristic impedances by Equation (3.32). Subsequently, the same equations are used to obtain the ABCD-parameters $ABCD_{tot}$ corresponding to S_{tot}, representing the full structure in Fig. 4.3. Since the ABCD-parameters of cascaded two-ports are by definition written as a matrix product of the ABCD-parameters of the individual two-ports, $ABCD_t$ is obtained by:

$$ABCD_t = ABCD_1^{-1} ABCD_{tot} ABCD_{MMIC}^{-1} \tag{4.1}$$

and after converting back to S-parameters, S_t has been successfully de-embedded.

Design of the compensation section using the Smith Chart

The S11 of S_t as indicated by the blue arrow in the schematic in Fig. 4.4a is plotted in blue in the 50 Ω Smith Chart in Fig. 4.4b over the frequency range 140-170 GHz. First, adding a section of transmission line (TX1) with the same characteristic impedance Z_1 (around 63 Ω) and propagation constant γ_1 rotates the points on the Smith Chart on a circle with the impedance Z_1 in the center. This matching path is illustrated at 155 GHz in the Smith Chart (Fig. 4.4b) by the black dotted line. The S11 after adding this transmission line is indicated by the red arrow in the schematic and plotted from 140 to 170 GHz in red in the Smith Chart. Thereafter, a transmission line section TX2 with a high impedance Z_2 (around 95 Ω) is added, rotating in the Smith Chart towards the impedance at port 1 of around 63 Ω (indicated by the green cross). The matching path at the center frequency of 155 GHz is indicated by the purple dotted line. Finally, the yellow line indicates the final S11, which is the closest to the Port 1 impedance as achievable over the frequency band of interest.



(a) Schematic **(b)** 50 Ω Smith Chart

Figure 4.4: CPW interconnection to the MMICs including high impedance transmission line compensation.

The lengths of both TX1 and TX2 are optimized to achieve the best S11 matching over 140-170 GHz. ABCD-parameters $ABCD_{TX1}$ and $ABCD_{TX2}$ are found using Equation (3.32). Cascading S_t and both transmission lines as indicated in Fig. 4.4a gives

$$ABCD_c = ABCD_2 ABCD_1 ABCD_t \tag{4.2}$$

Thereafter, S_c is found by converting back to S-parameters, normalizing to $Z_1 \approx 65\ \Omega$ at Port 1 and to $Z_{MMIC} \approx 50\ \Omega$ at Port 2. Since the lengths of both lines are the only unknowns, they are adjusted, optimizing $S_{c,11}$. The resulting lengths are 270 μm and 164 μm for TX1 and TX2, respectively.

Implementation and performance of the compensation transmission line section in the 3D model

The high impedance transmission line compensation section is implemented by decreasing the width of the CPW center strip and thereby increasing the CPW gap, retaining the total dimensions of the CPW, as listed in Table 4.1. This conservation ensures the radiation losses associated with the CPW transmission line are unchanged. The resulting 3D model is depicted in Fig. 4.5.

Table 4.1: Characteristic impedance and dimensions of the compensation section for the flip-chip interconnection to the MMICs using CPW transmission lines on the fused silica.

Transmission line section	Characteristic Impedance [Ω]	Central strip width s [μm]	Gap width g [μm]	Total dimensions $t = s + 2g$ [μm]
TX1	65	60	15	90
TX2	95	30	30	90

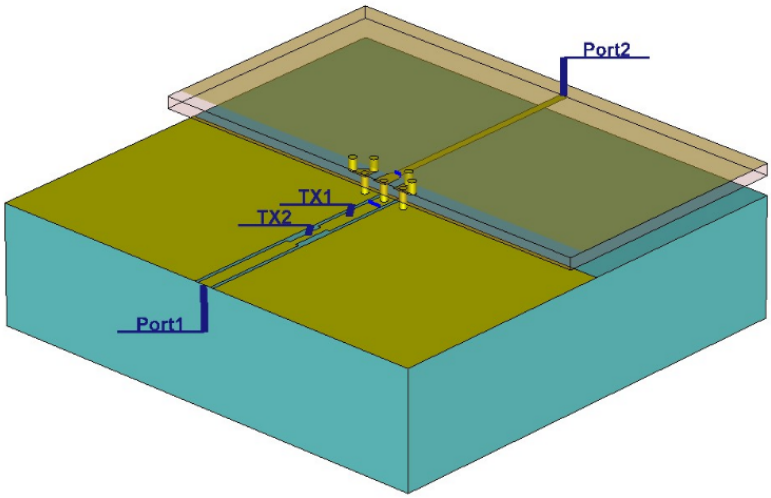
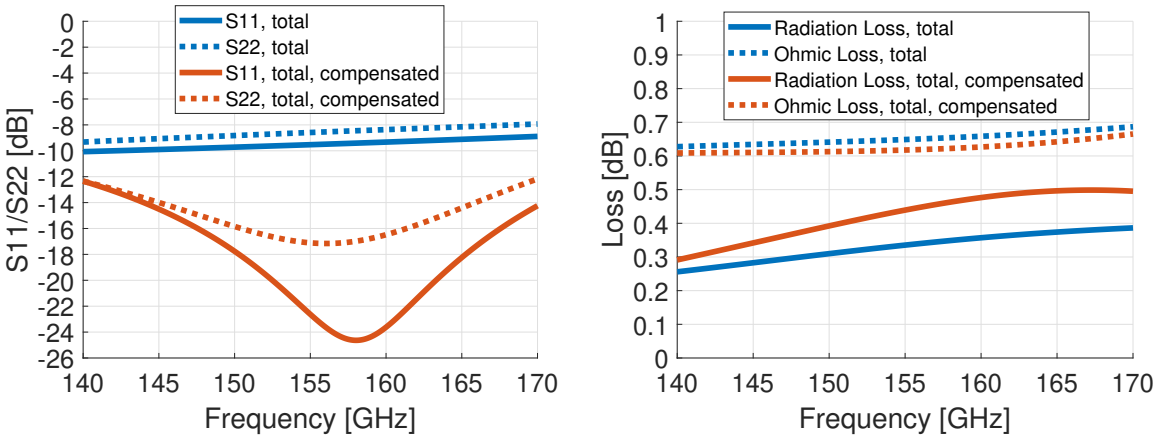


Figure 4.5: 3D model of the flip-chip interconnection to the MMICs using CPW transmission lines on the fused silica including a compensation series transmission line.

The 3D model of the compensated interconnection is simulated using CST. The resulting performance is plotted in Fig. 4.6 in red and, for comparison, the results from the simulation of the model in Fig. 4.2 are included in blue. The transmission lines on both sides are not de-embedded to compare the losses. The S11/S22 matching has been improved to below -12 dB over the bandwidth. The radiation loss has increased by only 0.1 dB at the highest frequencies in the band due to the discontinuities between the high impedance sections and the surrounding lower impedance transmission lines.



(a) S11 and S22 matching

(b) Radiation loss and Ohmic loss

Figure 4.6: Comparison of the simulated performance in CST between the flip-chip CPW interconnection to the MMICs from Fig. 4.1 and the interconnection including the high impedance section compensation from Fig. 4.5.

4.2. Flip-chip transition to MMICs using microstrip on fused silica

As discussed in the introduction, the integration using microstrip transmission lines is preferred, because the losses are significantly lower than in the case CPWs are used, due to the absence of radiation losses associated with the CPWs. One way to transition to a microstrip transmission line is to use the probe landing transition from Section 2.2 and connect it to the compensated CPW interconnection to the MMIC as presented in the previous section. However, this approach has two disadvantages. First, the transition used for probe landing adds around 0.5 dB of radiation to the radiation introduced by the interconnection and the compensation section, resulting in over 1 dB of radiation. Second, this transition will cover substantial space (over 1 mm) on the fused silica wafer together with the compensation section, which has to be repeated at every flip-chip interconnection on the wafer. A better approach is to transition to microstrip directly at the flip-chip interconnection, as endeavored in Subsection 2.1.3. Therefore, the symmetric via-less flip-chip microstrip interconnection has been modified by replacing the top wafer with the GaAs layer representing the chip. The 3D model for this interconnection is depicted in Fig. 4.1.

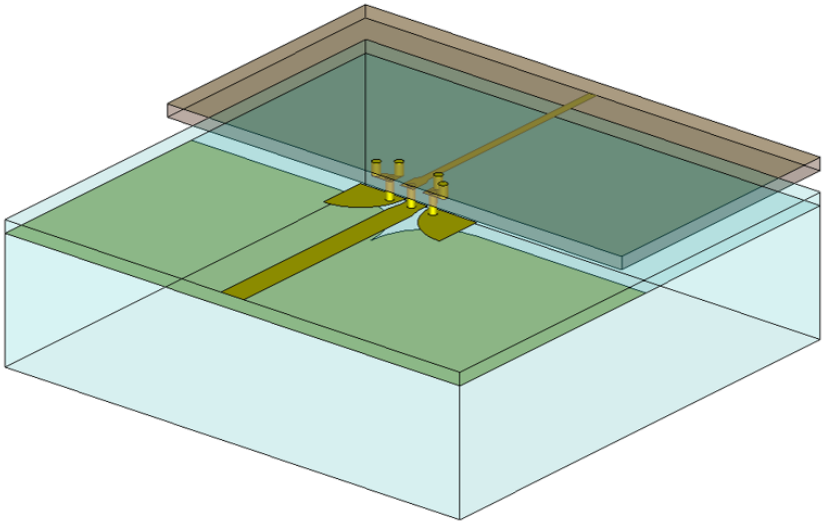
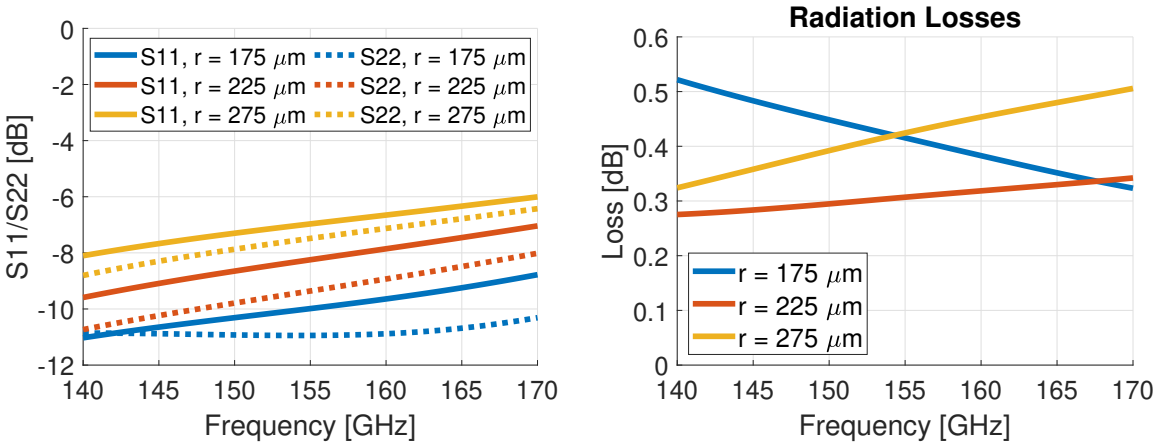


Figure 4.7: 3D model of the flip-chip interconnection to the MMICs using microstrip transmission lines on the fused silica.

Optimization of the quarter-circular pads

In Section 2.1.3, quarter-circular pads have been optimized for the symmetric via-less microstrip interconnection, minimizing the radiation loss and realizing a smooth transition from a CPW to a microstrip field distribution. The selected radius r of the quarter of 275 μm in the symmetric case, gives rise to an increase in radiation loss for increasing frequency over the bandwidth of interest in the case of the interconnection to the MMIC, as plotted in Fig. 4.8b. r is reduced to the optimal value of 225 μm because the envelope of the radiation loss over frequency is then flattened. Reducing r further would lead to an increase at the higher frequencies. However, the length of the taper of the microstrip in fused silica was also optimized, by shortening it to 50 μm (as depicted in Fig. 4.7). Although the radiation loss has been reduced below 0.35 dB, the S11/S22 matching is only below -7 dB. Therefore, this optimization did not lead to significant improvement of the S11/S22 matching.



(a) S11 and S22 matching

(b) Radiation Loss

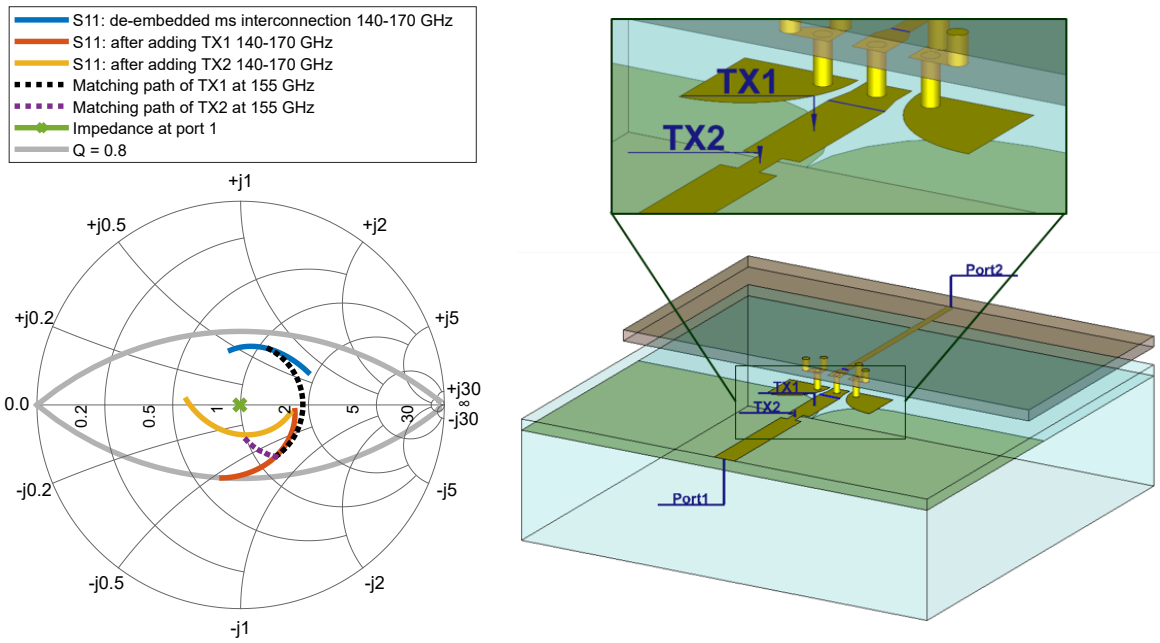
Figure 4.8: Simulated performance (from full-wave CST simulation) of the via-less flip-chip microstrip interconnection to the MMIC for varying quarter-circle radius r of 175 μm, 225 μm, and 275 μm.

Compensating for the S11/S22 mismatch by a high impedance transmission line section
The S11/S22 is improved using the same procedure as introduced in the previous section, using a high impedance microstrip transmission line. The transmission line dimensions and characteristic impedances are listed in Table 4.2. The characteristic impedances were verified using CST full-wave simulations of the uniform section, where the ports are placed directly on the ends of the section.

Table 4.2: Characteristic impedance and dimensions of the compensation section for the flip-chip interconnection to the MMICs using microstrip transmission lines on the fused silica.

Transmission line section	Characteristic Impedance [Ω]	Strip width s [μm]
TX1	50	100
TX2	85	30

Before adding the transmission line sections, the S-parameters were de-embedded up to the beginning of the microstrip taper, as indicated by the blue curve in Fig. 4.9b. The lengths of the transmission line section were chosen as 270 μm and 70 μm for TX1 and TX2, respectively, optimizing the S11 and S22 matching using the Smith Chart. The S11 matching paths are depicted in the Smith Chart in Fig. 4.9a, whereas the 3D model used for full-wave CST simulations is presented in Fig. 4.9b. Together with the microstrip taper and pad, the total length of the microstrip transmission line on the fused silica is 440 μm. In the case of the CPW transmission lines, the total length is 531 μm. Therefore, the CPW geometry does not offer an advantage in terms of the total space occupied compared to the microstrip geometry.



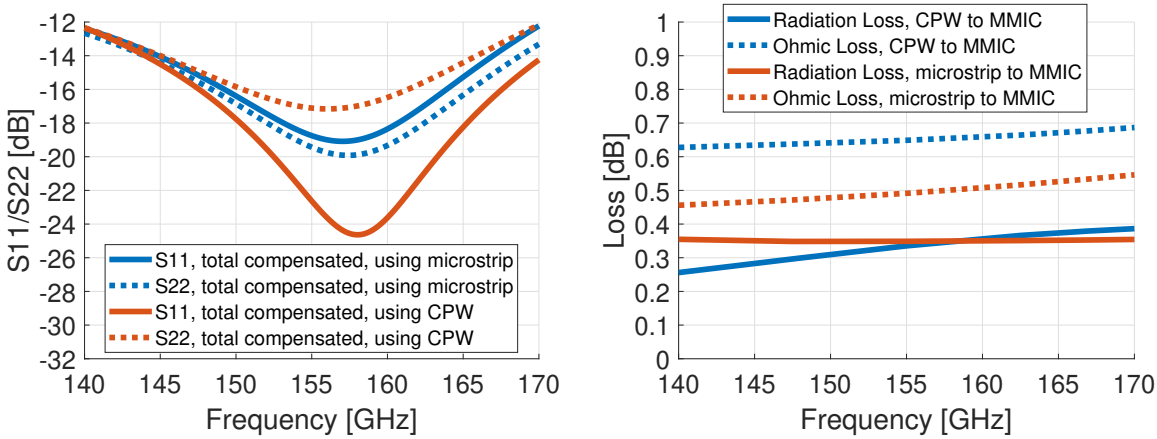
(a) 50 Ω Smith Chart

(b) 3D model for full-wave simulations

Figure 4.9: Flip-chip interconnection to the MMICs using microstrip transmission lines on the fused silica including a compensation series transmission line.

Comparison of the microstrip interconnection to the MMIC to the CPW interconnection, after adding S11/S22 matching compensation

The resulting model, depicted in Fig. 4.9b, is simulated in CST and the resulting performance is depicted in Fig. 4.10. The transmission lines of 1 mm on both sides are not de-embedded in order to compare the losses to the CPW case. As shown in Fig. 4.10a, the S11/S22 matching has been improved to below -12 dB over the frequency band of interest, similar to the performance using CPWs. The S11 and S22 are very similar for the microstrip case. When comparing in terms of losses, the Ohmic loss is around 0.1 dB improved compared to the CPW case, while the amount of radiation loss is below 0.4 dB for both cases.



(a) S11 and S22 matching

(b) Radiation and Ohmic Loss

Figure 4.10: Simulated performance (from full-wave CST simulation) of the via-less flip-chip microstrip interconnection to the MMIC after adding a high impedance series transmission line (from Fig. 4.9b) in blue versus the CPW interconnection to the MMIC after adding compensation (from Fig. 4.5), plotted in red.

Q-factor and bandwidth comparison and discussion

In the Smith Chart, arcs may be plotted for points with a ratio X/R, where X is a reactance and R is a resistance. This ratio is known as the quality factor (Q-factor) of a resonant circuit. To achieve a certain Q-factor, the matching paths in the Smith Chart have to stay within the arcs. As depicted in Fig. 4.4b and Fig. 4.9a, for the two matching circuits considered in this chapter, the matching paths stay within the arcs for $Q = 1$. This low Q indicates a relatively broadband impedance matching. However, Fig. 4.10a indicates the bandwidth is limited. This bandwidth limitation is given by the usage of transmission lines, which present impedance variations with frequency at a phase velocity given by the electrical length of the transmission lines. Therefore, matching will be only ensured at the center frequency at which the matching network was designed.

Further steps to improve the S11/S22 matching

The next step would be to adjust the flip-chip interconnection to improve the S11 matching over a wider bandwidth. One way would be to modify the transmission line on which the stud is landing, to reach a lower impedance. Another option would be to get a better understanding of where the S11 mismatch is coming from (for instance the pads on the MMIC or studs) and redesign the interconnection based on this knowledge.

5

Preliminary TRL Measurements

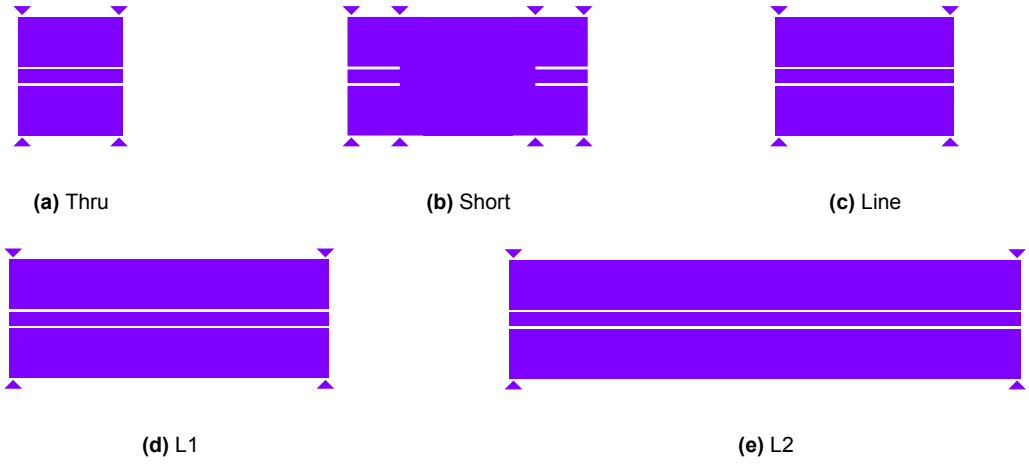
At the time of writing, the masks for the test structures introduced in Chapter 3 are under fabrication. However, the design and code developed though-out the thesis have been verified by simulation already. Nonetheless, some preliminary TRL measurements have been completed to substantiate the simulation results. The mask considered for these measurements contains structures similar to the mask presented in Section 3.4 in terms of the materials, the characteristic impedance, and the losses. Therefore, the preliminary TRL measurements will support the mask design from Section 3.4 and verify the implementation of TRL1 from Section 3.2.

Section 5.1 covers the dimensions and material properties of the measured structures. In Section 5.2, the resulting S-parameter are verified using corrected S-parameters from the calibration software. Finally, in Section 5.3, the measured results are compared to a simulated reference case in terms of the complex propagation constant, evaluating the phase and losses.

5.1. Mask for the preliminary measurements

A wafer made of fused silica, shown in Fig. A.1, was used to characterize the performance of the TRL algorithm. The measured features are indicated by red boxes. This mask design is not related to the work done in this thesis and was developed for a different purpose. However, this mask may still be used for testing the implementations discussed previously because of its similarities to the mask presented in Section 3.4.

The masks of the measured structures are repeated in Fig. 5.1. Two instances (T1 and T2) of lines L1 and L2 were measured for repeatability. The length difference between the Thru and the Line standard is 192 μm, which is around 1/6 wavelength or 60 degrees at the center frequency. The length of L1 and L2 is 556 μm and 1050 μm respectively, as the distance between the reference planes set by the Thru. The Thru has a length of 270 μm, whereas in the designed mask this length is 1 mm.



(a) Thru **(b)** Short **(c)** Line

(d) L1 **(e)** L2

Figure 5.1: Features measured during the preliminary TRL measurements. Indigo indicates aluminum.

The metal (aluminum) indicated in indigo in Fig. 5.1 has thickness 1.9 μm-2 μm and conductivity around $2.9 \cdot 10^7$ S/m. The metal lies on top of 300 μm-thick fused silica die. The CPW transmission lines have a width of the central strip of 35 μm and a gap on both sides of 7.5 μm. Referring to Fig. 1.9, according to the TL tool [23], a characteristic impedance of around 60 Ω is expected, and losses around 0.5 dB/mm. Three experiments are done:

1. Die on a metal chuck
2. Die on ferrite (absorbing material)
3. Die on 500 μm silicon wafer with low resistivity (around 2.5 Ω/cm).

The measurements are done from 140 to 220 GHz (WR5 band), visually aligning the RF probes.

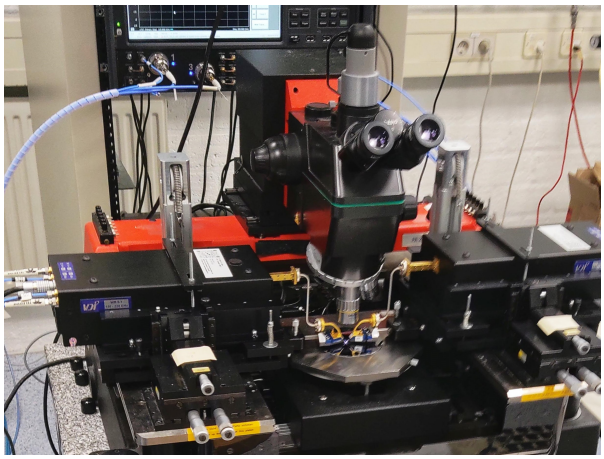
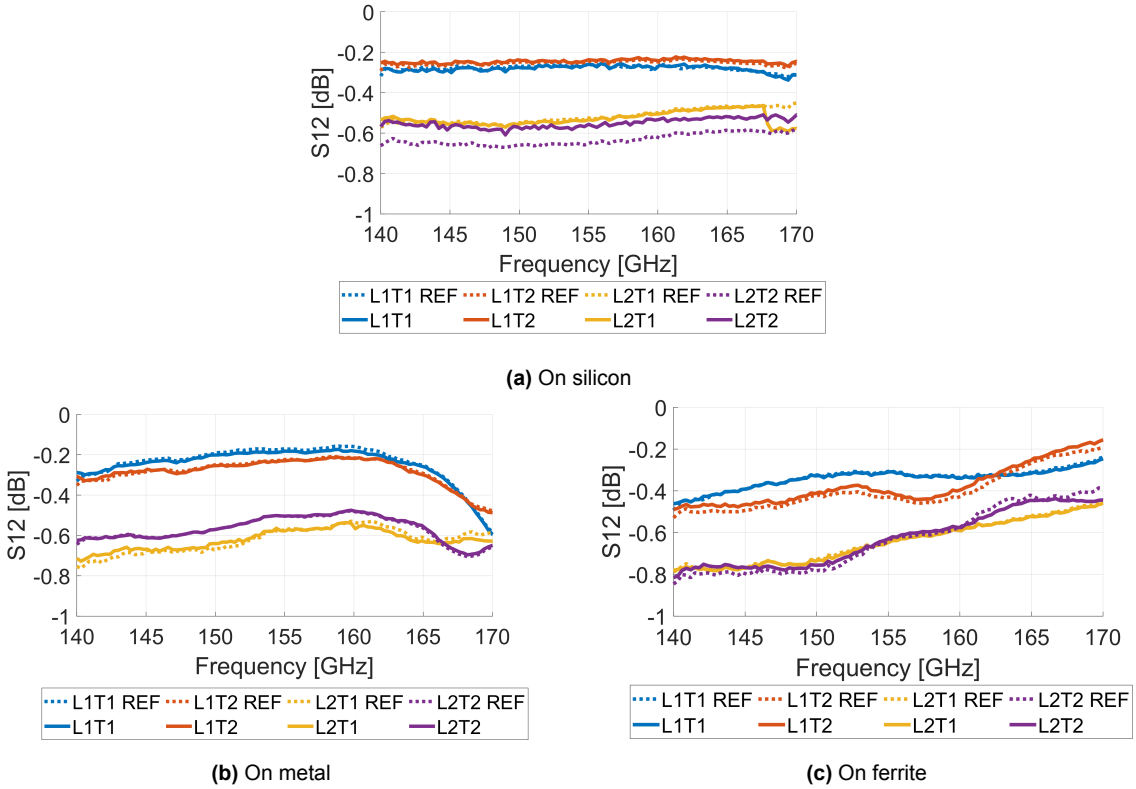


Figure 5.2: Measurement set-up for the preliminary measurements

5.2. TRL calibration verification

The S-parameters obtained from the measurement are corrected for the switch-terms (see Appendix A.3). Thereafter, the TRL1 code presented in Section 3.2 is used to de-embed the S-parameters between the error boxes for the lines L1 and L2. The resulting S12 was compared to results obtained from WinCal calibration software of the VNA, which has a TRL and the switch-term correction implemented as well (see Fig. 5.3). The obtained S-parameters show good agreement with the results obtained through the WinCal calibration tool, verifying the TRL.



(a) On silicon

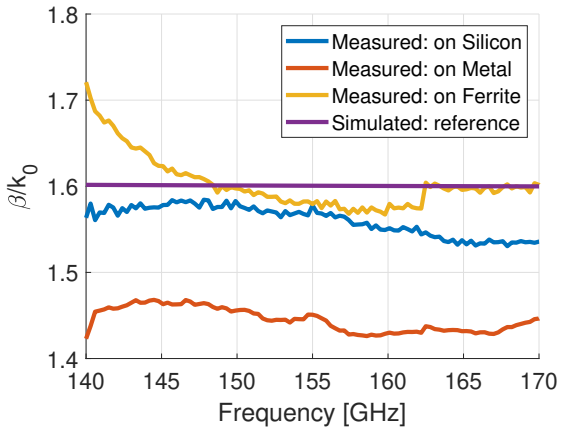
(b) On metal

(c) On ferrite

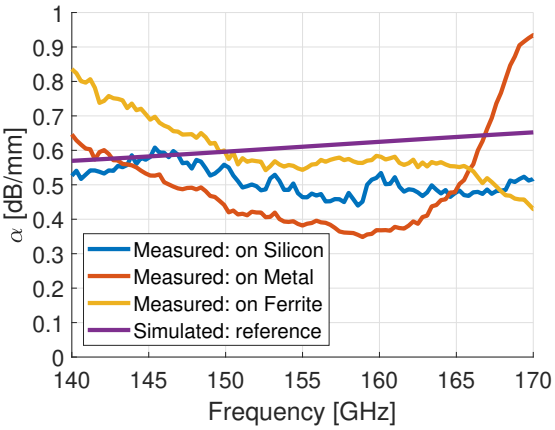
Figure 5.3: Verification of the TRL and Switch-term correction implementation in MATLAB against the WinCal TRL reference.

5.3. Propagation constant measurement results

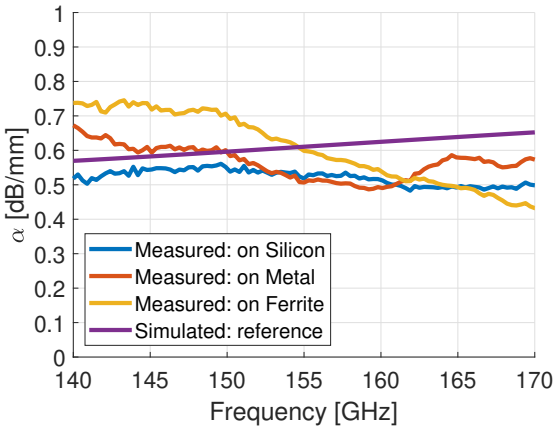
The TRL returns the complex propagation constant, quantifying the phase constant and the attenuation constant (losses). The CST simulation of the same geometry on semi-infinite fused silica (open boundary below the fused silica) serves as a reference, where the propagation constant is determined using the approach discussed in Section 3.2.2. Accordingly, the results are presented in Fig. 5.4 for placing the die on the three different materials. The longer line L2 is performing better than the shorter line for the determination of the losses in terms of the attenuation constant. This is likely due to the decreasing cross-talk between the probes over distance. Furthermore, placing the die on a silicon wafer with low resistivity was demonstrated to result in the flattest behavior over frequency, close to the simulated results.



(a) Phase constant



(b) Attenuation constant L1 (556 μm)



(c) Attenuation constant L2 (1050 μm)

Figure 5.4: Propagation constant obtained from measurement using TRL1, compared to a reference CST simulation of the same line on semi-infinite fused silica.

Concluding, the preliminary measurements have been successfully completed. The MATLAB code implemented for TRL1 and the switch-term correction has shown to match results obtained using a commercial calibration tool. Furthermore, the TRL1 code has been used to find the phase constant from the Line standard and attenuation constants using the longer transmission lines. The measurement results for the die placed on a silicon carrier show the best agreement with the result of a CST simulation assuming semi-infinite fused silica. From the measurements it is concluded that an error below 2% is expected for the phase constant and below 4% for the attenuation constant. The designed mask is expected to give even better accuracy due to the longer transmission lines used for the Thru standard, which reduces the effect of the probes on the transmission lines.

Due to the similarity between the mask used for the preliminary measurements and the mask presented in Section 3.4 in terms of materials, characteristic impedance, and losses, it is expected that the TRL1 calibration for the measurement of the designed mask will have at least around the same accuracy and the calibration will be successful.

6

Conclusion and Future work

This thesis has explored the flip-chip bonding technology for frequencies at 150 GHz (G band). Designs and a characterization approach have been defined and some preliminary measurements have been performed.

At higher mm-wave frequencies, more bandwidth is available, allowing data rates toward 100 Gbps. Current technology platforms for broadband cellular networks (5G) have not been able to properly address the most demanding situations with high connection density. Therefore, the Fly's Eye concept has been proposed, combining quasi-optical beam forming with an mm-wave broadband operation to enable a single base station providing more than Tbit/sec overall (front-end) capacity to a dense environment with tens of thousands of users. The final goal of the Fly's Eye project is to demonstrate the concept and performance by developing an integrated front-end prototype. This thesis has presented the characterization of a flip-chip interconnection used for the integrated front-end prototype at 150 GHz (G band) with a leaky-wave on-package dual lens antenna. The goal of the project was to develop the front end with two commercially available MMICs and a feeding antenna integrated on a single fused silica wafer. Flip-chip bonding has been selected because it has significantly lower radiation loss than wire-bonding at mm-wave frequencies and it is very suitable for mass production applications.

In Chapter 1, two paths for the front-end integration have been proposed. The first path adopts CPW transmission lines on 500 μm-thick fused silica, and the second uses microstrip transmission lines on 50 μm-thick fused silica, bonded to a 500 μm-thick wafer to create the leaky wave resonant cavity. For the CPWs, the total dimensions have been decreased to 100 μm to minimize radiation loss due to the excitation of the surface wave mode. Total losses have been estimated to decrease to below 0.5 dB/mm. For the microstrip on fused silica, the strip width has been increased to around 100 μm to decrease losses to below 0.15 dB/mm. The microstrip does not support the surface wave mode and therefore does not radiate. However, front-end integration using microstrip transmission lines is more challenging to fabricate and manufacture than the CPW front-end integration.

In Chapter 2, several symmetric flip-chip interconnections in fused silica have been studied

and optimized to minimize radiation loss, to be later implemented in test structures. While radiation losses are bound by the fabrication technology (minimizing the CPW dimensions), matching networks have been designed to optimize the matching of the flip-chip bonding interconnection. The flip-chip CPW interconnection has been considered first because the flip-chip stud may be placed directly on the CPW lines, leading to a smooth field transition. The decrease of radiation loss to below 0.22 dB has been verified using full-wave simulations, when decreasing the central strip width s to 60 μm and the gap width g to 15 μm. It was demonstrated that the size and shape of the studs have a major impact on the S11/S22 matching. Smaller diameter studs were found to significantly improve S11/S22 matching performance. Analysis of the electric field distribution indicated a good similarity between the CPW mode and the fields at the flip-chip interconnection. Therefore, it has been decided to fabricate the CPW interconnection using uniform lines to determine the impact of the studs on the electrical performance. A flip-chip microstrip interconnection using vias has been designed, which indicated an increase in radiation loss to around 1 dB at 170 GHz, causing the design to be unviable. Therefore, a via-less microstrip interconnection has been endeavored, using circularly tapered pads and ground plane, facilitating the transition from microstrip to CPW and reducing radiation loss. The dimensions of these quarter-circles have been optimized to a radius of about a quarter wavelength, reducing radiation. S11/S22 matching below -30 dB and total loss below 0.8 dB has been achieved over a limited bandwidth of 38%, but wider than the bandwidth of interest (140-170 GHz). The via-less microstrip interconnection has led to a significant reduction of radiation loss as has been expected because the optimized microstrip transmission lines are less lossy than the CPW transmission lines. Two RF probe landing transitions have been designed, for microstrip and CPW transmission lines. The transmission lines are tapered to a width of the metal of 32 μm to avoid excitation of the common mode. The microstrip is transitioned to CPW for landing the probes, optimizing the dimensions to minimize the radiation loss to below 0.4 dB.

In Chapter 3, back-to-back test structures have been developed using the CPW designs from Chapter 2. A double Thru-Reflect-Line calibration has been designed to first de-embed the S-parameters between the error boxes (TRL1) and then determine the S-parameters of one interconnection (TRL2). The derivation resulting in analytical expressions of the reflection coefficient, propagation constant, and S-parameters between the error boxes have been presented. Subsequently, for TRL2, the error boxes have been assumed to be equal, which allows one to obtain an analytical expression for the S-parameters of the error boxes, which in this case describe the flip-chip interconnection. The TRL structures (TRL1 and TRL2) have been modeled in CST for full-wave simulations. The equations have been implemented in MATLAB, resulting in excellent agreement with CST reference simulations. Finally, two mask designs have been presented: the design of a large 4-inch wafer of 500 μm-thick fused silica with one metal layer and a smaller 1/4-inch wafer of 50 μm-thick and with two metal layers. The larger mask has been already sent for fabrication at the TU Delft clean room and will be used to characterize the electrical performance of the flip-chip studs and the CPW antenna integration. The second smaller mask will be used to test the microstrip antenna integration.

In Chapter 4, the symmetric flip-chip CPW interconnection and the symmetric via-less microstrip interconnection have been revised to study the interconnection to commercially avail-

able MMICs. In the 3D CST model, the top wafer has been replaced by a wafer representing the MMICs. For the CPW interconnection, a high impedance transmission line section has been placed in series on the fused silica wafer. The length of the section and the placement have been optimized using the Smith Chart, improving the S11/S22 matching to below -12 dB over the frequency bandwidth 140-170 GHz. Total radiation loss amounts to below 0.5 dB and Ohmic loss below 0.7 dB. Thereafter, the via-less microstrip interconnection has been adopted. Again, the S11/S22 has been improved to below -12 dB over the bandwidth, radiation loss is below 0.4 dB, and Ohmic loss below 0.6 dB. From the Smith Chart, it has been concluded that the Q-factor is below 1 and, therefore, a broadband matching would be expected. However, the S11/S22 matching shows a narrow band frequency behavior due to the usage of transmission lines, which present impedance variations with frequency at a phase velocity given by the electrical length of the transmission lines. Therefore, matching will be only ensured at the center frequency at which the matching network was designed.

In Chapter 5, preliminary TRL measurements have been done for a wafer with transmission lines possessing a characteristic impedance, losses, and material properties similar to these on the mask considered in Section 3.4. The implemented TRL1 MATLAB code from Chapter 3 showed good agreement with a commercially available software tool and simulations. From the preliminary measurements, accuracy of 98% is expected for the phase constant and 96% for the attenuation constant for TRL measurements of the designed mask considered in Section 3.4.

Based on this work, several recommendations can be made for further improvement of flip-chip interconnections above 100 GHz. The shape and size of the flip-chip studs have been shown to impact the electrical performance, and specifically the S11/S22 matching, significantly. Therefore, stud diameters should be decreased to improve the performance of the interconnection at mm-wave frequencies. Due to the sensitivity of the stud dimensions, further investigation of the process variation is required. This study will be done by several flip-chip measurements of the CPW mask presented in Section 3.4.

Furthermore, it has to be determined whether the procedure of TRL2 gives measurement results that agree with simulations, showing that the effect of the radiation coupling between parts of the back-to-back structures has been sufficiently reduced. The final via-less microstrip flip-chip interconnection presented in Section 4.2 has to be re-optimized after the electrical performance of the studs has been measured.

Further improvement of the S11/S22 matching of this interconnection may include changing the height of the studs or further decreasing the gap between the ground pads and the center strip on the fused silica wafer to decrease the characteristic impedance. Another option would be to get a better understanding of where the S11 mismatch is coming from (for instance the pads on the MMIC or studs) and redesign the interconnection based on this knowledge.

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A

Appendix

A.1. Computing the losses using CST simulations

The full-wave simulations in this thesis are done using the frequency domain solver in CST. CST gives the loss in metals and dielectric P_{ohmic} expressed in Watt. Furthermore, it gives the power accepted into the structure at each port, denoted by $P_{accepted}$. The Ohmic loss in dB is then computed as

$$L_{ohmic}\,[\text{dB}] = 10\log_{10}\left(\frac{P_{accepted} - P_{ohmic}}{P_{accepted}}\right) \tag{A.1}$$

An equivalent expression is used to determine the dielectric loss as

$$L_{dielectic}\,[\text{dB}] = 10\log_{10}\left(\frac{P_{accepted} - P_{dielectric}}{P_{accepted}}\right) \tag{A.2}$$

The total loss is computed as

$$L_{tot}\,[\text{dB}] = 10\log_{10}\left(|S_{11}|^2 + |S_{12})^2\right) \tag{A.3}$$

or by taking the S-parameter balance from CST and then taking 20 times the 10-log. The radiation loss may then be determined by:

$$L_{rad} = L_{tot} - L_{ohmic} - L_{dielectric} \tag{A.4}$$

where all losses are expressed in dB. Note that for this simulation it is required that all boundaries are open boundaries, assuming the simulated structures are infinitely extended.

Another approach to find the radiation loss is by replacing the lossy materials with lossless materials, replacing Gold/Aluminium with PEC, and setting the loss tangent of the dielectric to zero. It has been verified that this approach gives the same radiation loss as the method previously discussed. Furthermore, the losses have to be verified by calculations using the transmission line tool [23].

A.2. Mask used for the preliminary measurements

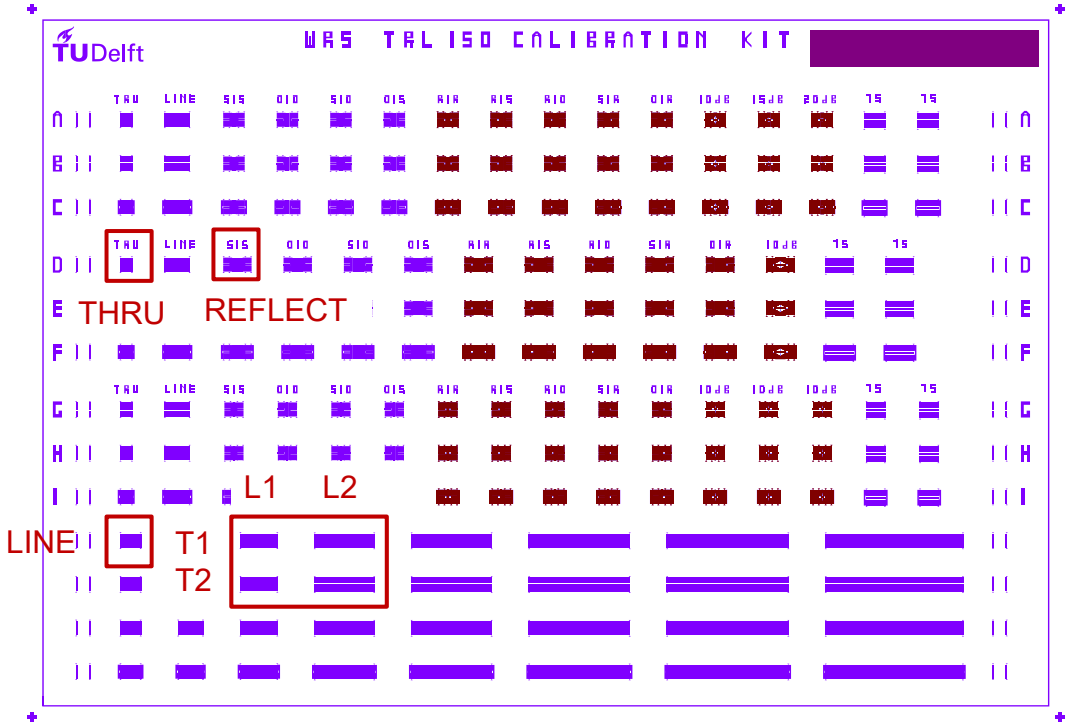

Figure A.1: Total mask used for preliminary TRL measurements. Blue indicates aluminum and red is a resistive layer, not relevant for the measurements. Red boxes indicate the measured features.

A.3. Switch-term correction

Switch-term correction is a technique to remove the effects of an imperfect switch inside the VNA due to the non-ideal load impedances terminating the unstimulated port. The reflection coefficients Γ_F and Γ_R are referred to as switch-terms and determined once during measurement of the Thru. Γ_F is the ratio of forward-traveling waves measured at port 2 when port 1 is excited, while Γ_R is the ratio between waves traveling in the reverse direction at port 1 when the source is switched to port 2. The switch-term model was introduced by Marks [31] and the corrected S-parameters are given by

$$S_{11} = \frac{S_{11}^F - S_{12}^R S_{21}^F \Gamma_F}{1 - S_{12}^R S_{21}^F \Gamma_R \Gamma_F} \tag{A.5}$$

$$S_{21} = \frac{S_{21}^F - S_{22}^R S_{21}^F \Gamma_F}{1 - S_{12}^R S_{21}^F \Gamma_R \Gamma_F} \tag{A.6}$$

$$S_{12} = \frac{S_{12}^R - S_{11}^F S_{12}^R \Gamma_R}{1 - S_{12}^R S_{21}^F \Gamma_R \Gamma_F} \tag{A.7}$$

$$S_{22} = \frac{S_{22}^R - S_{12}^R S_{21}^F \Gamma_R}{1 - S_{12}^R S_{21}^F \Gamma_R \Gamma_F} \tag{A.8}$$

The equations were implemented in a MATLAB function to obtain the corrected S-parameters from the uncorrected S-parameters and the measured switch-terms.