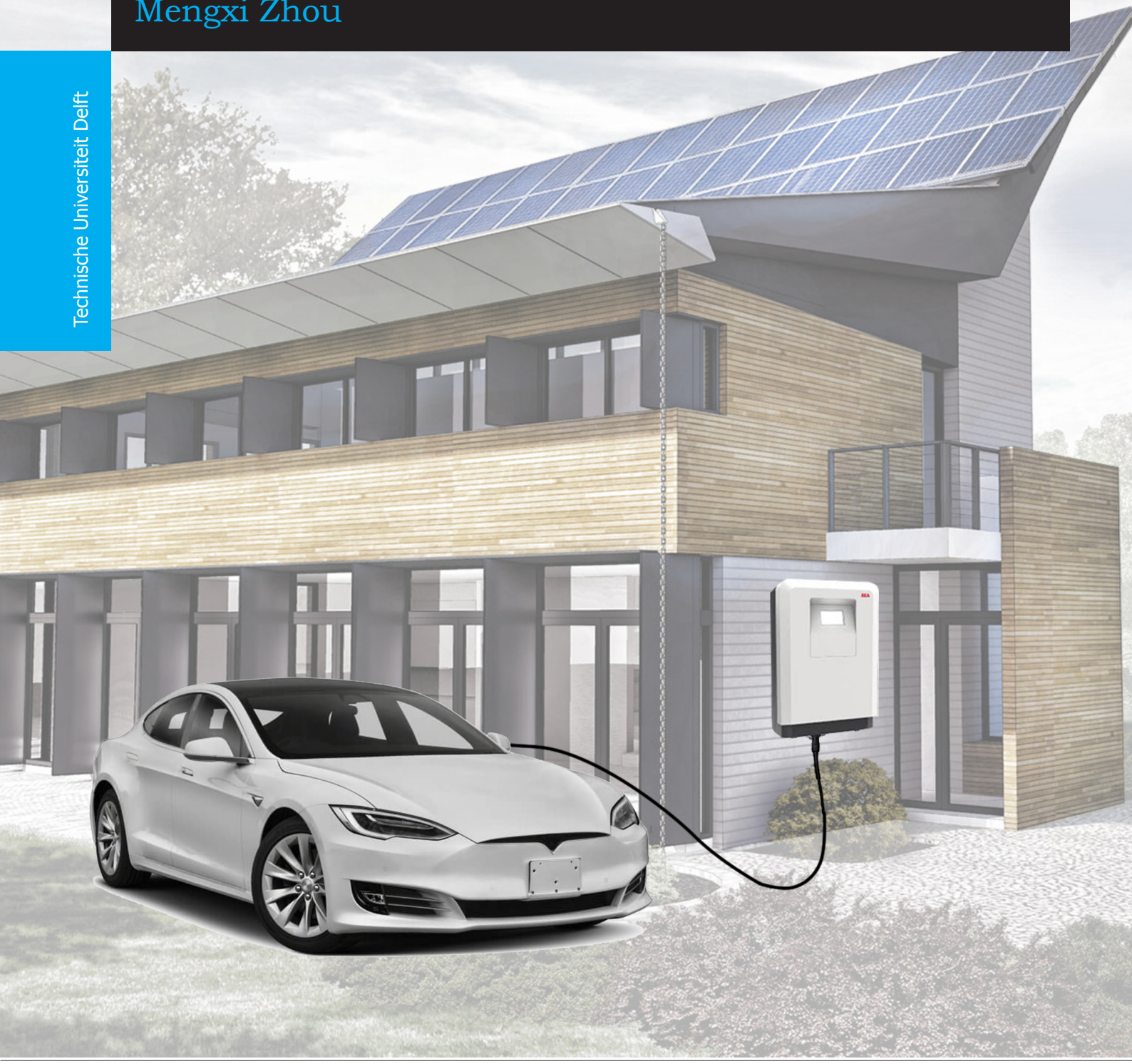
Investigation into the DC-DC Converter for the PV Integrated Bidirectional EV Charging System

Mengxi Zhou

Technische Universiteit Delft



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Challenge the future

Investigation into the DC-DC Converter for the PV Integrated Bidirectional EV Charging System

by

Mengxi Zhou

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University Supervisor:	Prof. dr. ir. Pavol Bauer,	TU Delft
	Dr. ir. Zian Qin,	TU Delft
Company Supervisor:	Ir. Stefan Raaijmakers,	ABB
Thesis committee:	Prof. dr. ir. Pavol Bauer,	TU Delft
	Dr. ir. Zian Qin,	TU Delft
	Dr. ir. Jose Rueda Torres,	TU Delft

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Abstract

With the rapid development of the economy and the continuous innovation of technology, the automobile industry is developing at a high speed. While providing convenient transportation and improving the efficiency of production and living, it has also caused a series of problems such as the energy shortage and environmental pollution. Electric vehicles (EVs) are getting more and more attention and support because of their unique advantages such as the energy saving and zero emission. Once the electric vehicle can charge from the clean and sustainable energy source such as the solar and wind energy, it can be an environment-friendly mode of transportation. Therefore, the photovoltaic (PV) integrated EV charging system appears in recent years. In the meanwhile, ABB is also interested in finding a way to combine their PV products and the EV chargers to make a more compact and efficient PV integrated EV charging system.

A possible solution of making a more compact PV integrated EV charging system is to use the multiport converter which can integrate the separated DC-DC converters. However, the traditional multiport converter needs a large number of active switches and the control of the whole converter is complex. Moreover, the zero voltage switching (ZVS) operation cannot be achieved easily in the traditional multiport converter. Therefore, a dual boost integrated dual active bridge (DAB) converter used for the PV integrated bidirectional EV charging system is investigated in this master thesis project.

This master thesis is the first step to investigate the dual boost integrated DAB converter working with a large output voltage range, which can be compatible with the new CHAdeMO standard (CHAdeMO 2.0) regarding the charging voltage range and make the whole PV integrated EV charging system more compact and efficient. The investigation is divided into three parts which are: the working principle and control analysis, the power loss modeling and analysis and the experimental verification tests.

First of all, the specifications of the converter are clarified, the circuit structure, the working principle of the two interleaved boost converters in the primary side and the working principle of the whole converter are analyzed. Secondly, the parameters of the converter are calculated according to the specifications and all the equations in terms of the voltage, the current and the output power are deduced. The power modes and the control structure of the converter are also introduced.

Afterwards, the soft switching characteristics of the switches and the circulating power in the dual boost integrated DAB converter are investigated by considering the DC bus voltage, PV voltage, and the EV battery voltage, and then the ZVS region is enlarged by applying the DC blocking capacitor voltage control. Besides, the transistor candidates are chosen and the power loss model and the thermal model of the candidates are built. The loss breakdown, the loss ratio and the thermal performance of the switches are analyzed and evaluated.

An analysis tool which can analyze the voltage and current at different points, the output power, the soft switching region and the circulating power of the dual boost integrated DAB converter is developed in Mathcad. This analysis tool is not only suitable for this project but also can be used to do other customized designs, which helps to decrease the time and cost for the development. The simulation model including the control loop and the thermal model of this converter is built in PLECS to check the feasibility of the design. Finally, a test bench is built and the experimental tests are implemented to verify the analysis and the simulation results.

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Introduction

1.1. Background

With the rapid development of the economy and the continuous innovation of technology, the automobile industry is developing at a high speed. While providing convenient transportation and improving the efficiency of production and living, it has also caused a series of problems such as the energy shortage and environmental pollution.

Electric vehicles (EVs) are getting more and more attention and support because of their unique advantages such as the energy saving and zero emission. The prediction of the vehicle sales in the next 30 years is shown in the Figure 1.1, it can be seen that the battery electric vehicle has the largest sale ratio in the future.

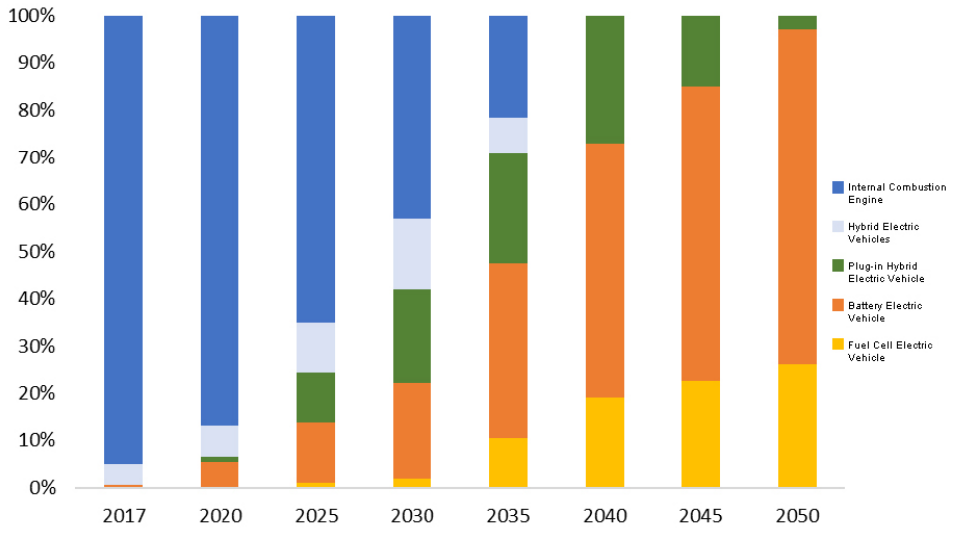


Figure 1.1: The prediction of the vehicle sales [1]

If the electric vehicle can charge from the clean and sustainable energy source such as the solar and wind energy, it can be an environment-friendly mode of transportation. Therefore, the photovoltaic (PV) integrated EV charging system appears in recent years.

1.2. Motivation

The system structure of the existing PV integrated EV charging system is shown in the Figure 1.2. There are three DC-DC converters (the DC-DC converter between the DC bus and the PV panels, the DC-DC converter between the energy storage system and the DC bus and the DC-DC converter between the DC bus and the battery of the EV) in the whole system, which results in problems such as high

cost, low efficiency and low power density due to the large number of components and the several power conversion stages.

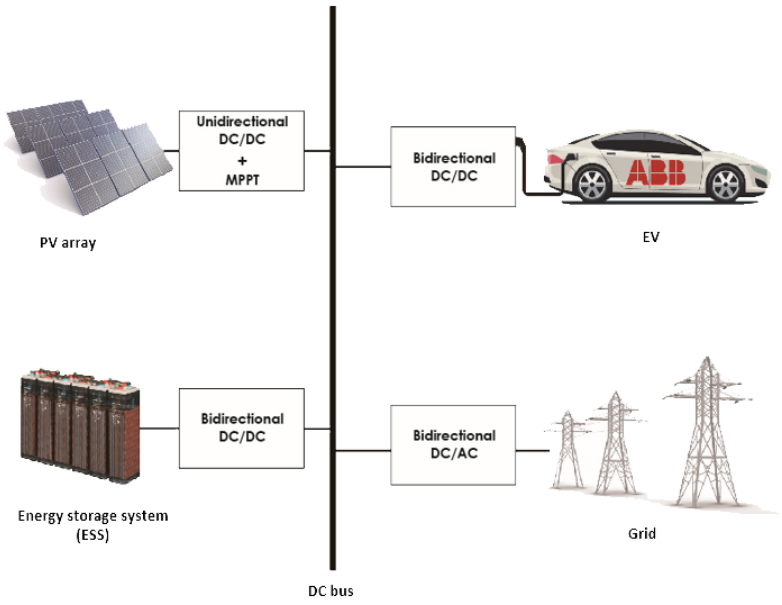


Figure 1.2: The system structure of the existing PV integrated EV charging system

The multiport converter can integrate the separated DC-DC converters and may have the advantages in terms of the efficiency, the cost and the power density due to the reduced power conversion stage and the smaller number of components in the whole system [3]. The new system structure which combines the DC-DC converter between the DC bus and the PV panels and the DC-DC converter between the DC bus and the battery of the EV by using the three-port DC-DC converter is shown in the Figure 1.3. The three-port bidirectional DC-DC converter which is in the red dash line is the research object of this master thesis project.

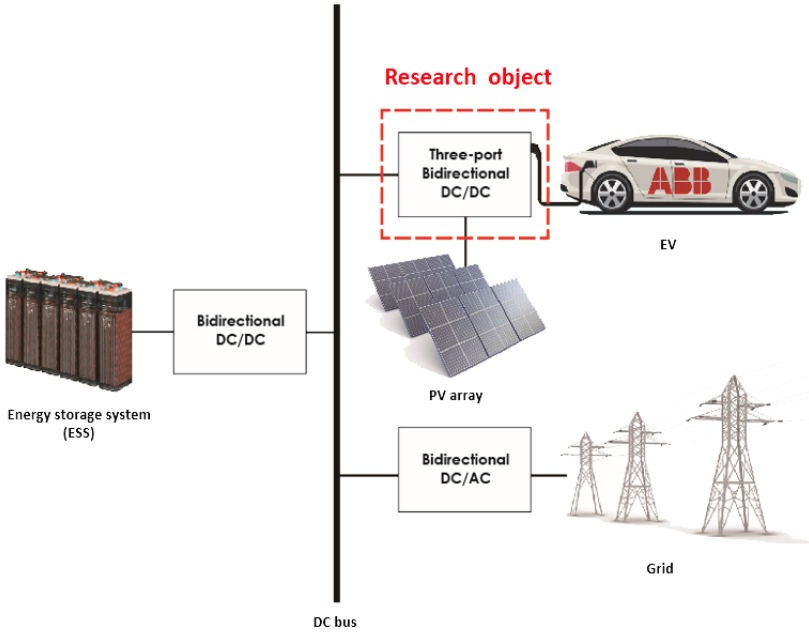


Figure 1.3: The new system structure of the PV integrated EV charging system

1.3. Research objectives and research questions

This master thesis project is the first step to investigate the isolated DC-DC converter for the PV integrated bidirectional EV charging system to make the whole system more compact and more efficient. The investigated converter should be able to work with a large output voltage range so that it can support both the existing $500V$ battery EVs and the next generation high voltage EVs. These research objectives can be translated into the following research questions:

- What is the best topology of the DC-DC converter to make the PV integrated bidirectional EV charging system more compact and more efficient?
- What are the best control and modulation methods for the converter to operate in a large voltage range?
- How will the converter perform at different operation points and operation modes of the system?

1.4. Research methodology

The research methodology of this master thesis project is indicated by a flowchart which is shown in the Figure 1.4.

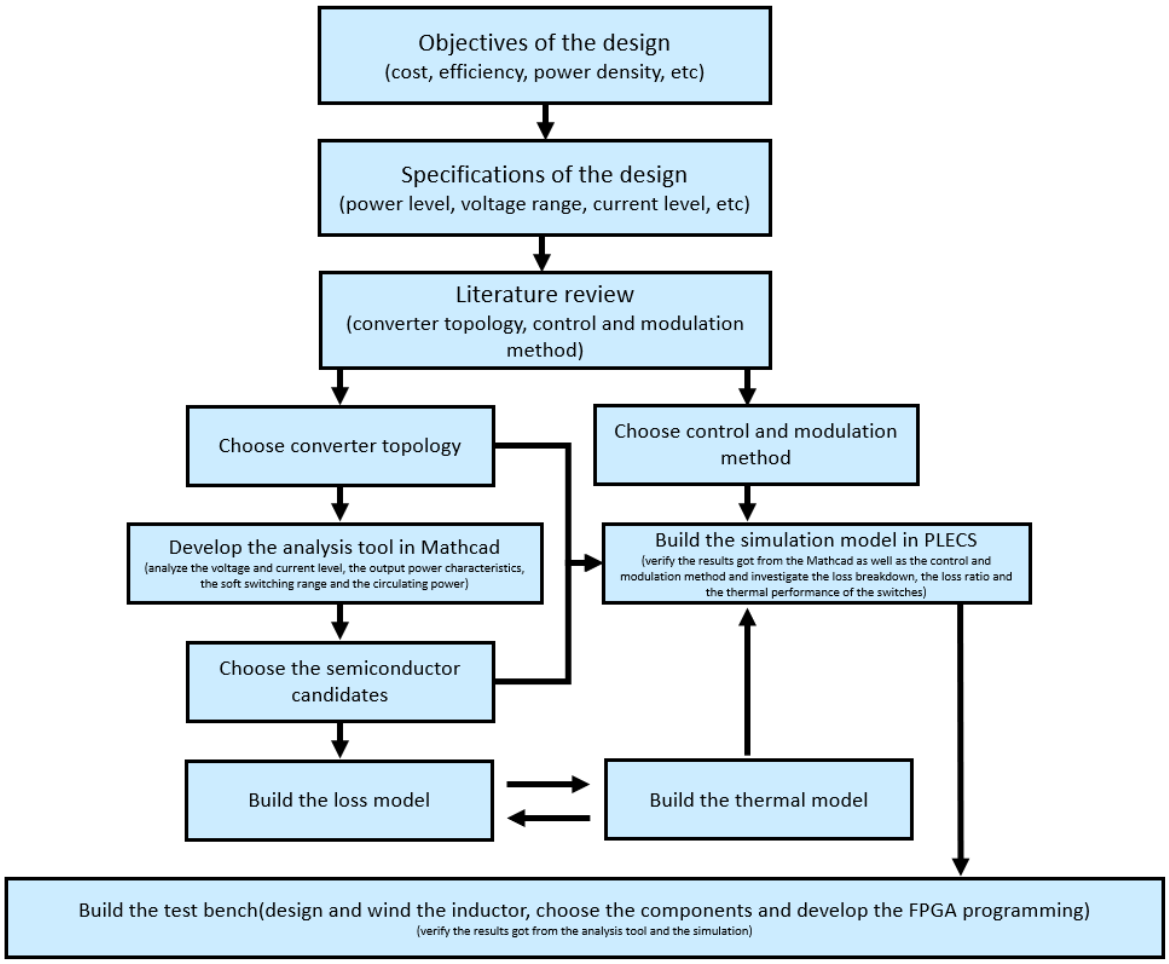


Figure 1.4: The flowchart of the methodology

In order to design a novel isolated DC-DC converter for the PV integrated bidirectional EV charging system, the first thing needs to be done is to clarify the objectives and the specifications of the design. The second step is to find the suitable topology and the suitable control and modulation method according to the objectives and specifications by doing the literature review. Afterwards, the working

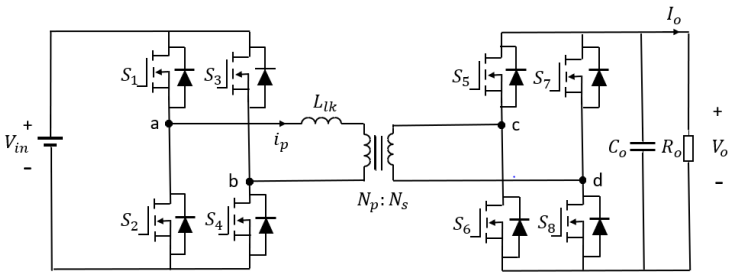
principle, the voltage and current level, the output power characteristics, the soft switching range and the circulating power of the investigated converter should be analyzed. According to the analyzed results, several semiconductor candidates should be proposed and the loss model of the semiconductor should be developed. Then, the simulation model including the control loop and the thermal model should be built to verify the previous analysis and evaluate the loss breakdown, the loss ratio and the thermal performance of the switches. The last step is to build a test bench to do the experiment test to verify the analysis and simulation results.

1.5. Literature review

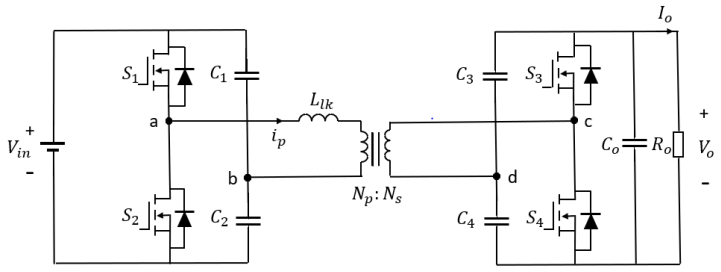
1.5.1. Review of the converter topologies

The EV chargers are classified into two types: unidirectional EV chargers and bidirectional EV chargers. The latter type can realize the vehicle to grid (V2G) function since it can support the power flow from the EV battery to the grid. Hence, the load of the grid can be reduced during the peak load hours [4]. That is why the bidirectional DC-DC converter is more preferable for the EV charging application. And the bidirectional DC-DC converters are divided into non-isolated and isolated bidirectional DC-DC converters. The isolated DC-DC converter is preferred over the non-isolated type because of the high gain and galvanic isolation [5]. With the galvanic isolation, the shock hazard can be mitigated and the common mode noise can be reduced. The main types of the isolated bidirectional DC-DC converters which can realize the buck-boost purpose are bidirectional flyback converters, dual active bridge (DAB) converters and CLLC resonant converters. In [6–8], different kinds of bidirectional flyback converters are designed and analyzed. The main drawback of the bidirectional flyback converter is that it is only suitable for low power level. In [9], the interleaved flyback structure is used to increase the power level. However, the number of the components, the cost and the complexity of the whole converter are increased due to the interleaved structure. The DAB and CLLC resonant converters are the most popular DC-DC converters for bidirectional EV chargers because of their high efficiency, buck-boost capability, high power density and the controllable bidirectional power transfer [10–14].

The main types of the DAB converters and CLLC resonant converters are full bridge DAB, half bridge DAB, full bridge CLLC and half bridge CLLC, which are shown in the Figure 1.5 and Figure 1.6 [15]. Different topologies are suitable for different applications and need different design methods.

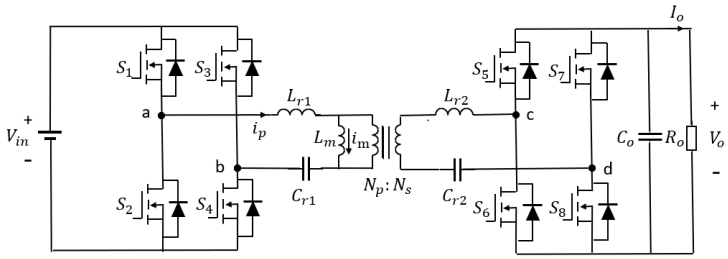


(a) Full bridge DAB converter

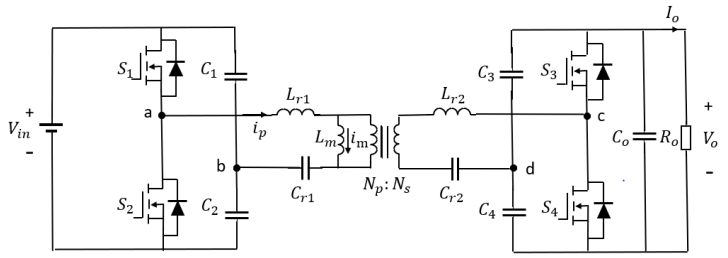


(b) Half bridge DAB converter

Figure 1.5: The full bridge and half bridge DAB converter topologies



(a) Full bridge CLLC resonant converter



(b) Half bridge CLLC resonant converter

Figure 1.6: The full bridge and half bridge bidirectional CLLC resonant converter topologies

A $5kW$ full bridge DAB for a 380V input and 20V-28V output battery charger is designed, built and tested in [16], the highest efficiency is more than 96%. In [17], a 600W half bridge DAB for EV charger is built and tested, which verifies the theoretical analysis. A $5kW$ full bridge CLLC converter for a 380V DC power distribution system is built and tested in [18] and the highest efficiency is 97.8%. The $1kW$ half bridge CLLC converter with the 300-600V input voltage and 200V-400V output voltage, which is used for the bidirectional EV charging system, is built and tested in [19]. The highest efficiency is 96.5% for the charging mode and 97.4% for the discharging mode.

The four topologies are analyzed and compared in [15] and [20], from which the following conclusions can be got:

- CLLC resonant converters have a higher efficiency than the DAB converters in the narrow load range conditions.
- The highest efficiency of the CLLC resonant converter can be achieved when it operates around the resonant frequency. When the operating frequency is far from the resonant frequency, the efficiency will be reduced due to the increased circulating losses. And the DAB converter may lose the soft switching of the switches at the light load condition.
- The soft switching region of the CLLC resonant converters is larger than the DAB converters especially at the light load condition.
- The half bridge structure has a higher efficiency than the full bridge structure in low power application due to the reason that there are fewer switches and corresponding driving circuits in the whole converter, but the full bridge is more suitable for high power (higher than $1kW$) application.
- Another advantage of the half bridge CLLC resonant converter is that the two capacitors in each side can reduce the flux imbalance of the transformer.
- If the converter needs to operate with a large voltage range, the design and control complexity of the CLLC resonant converter is larger than that of the DAB converter due to the larger number of design considerations and the nonlinearity relationship between the gains and the loads.

- The output current of the CLLC resonant converter is similar to the sinusoidal waveform and has less high-order harmonic ripples compared with that of the DAB converter. Therefore, the current filter is not needed for the CLLC resonant converter, whereas it may be needed for the DAB converter.
- Both the primary side and secondary side current of the half bridge structure are much larger than those of the full bridge structure. Hence, the current stress on the components of the half bridge converter is larger than that of the full bridge converter.
- The half bridge structure has the advantages in terms of the size and weight since the reduced number of switches and the corresponding driving and cooling systems.

To integrate the PV panels to the EV charging systems, a lot of researches focus on how to do this by using the three-port converters. Compared with the separated two-port converters, the three-port converter has a more compact structure, higher efficiency, lower cost and more flexible power flow control due to the reduced number of components and the reduced power conversion stage in the whole system [21]. And the complicated communication between the different two-port converters can be eliminated in the three-port converter.

The conventional isolated three-port bidirectional DC-DC converters use the multi-winding transformer to get the galvanic isolation between the source and the load and three bridges are connected to the three-winding transformer [22]. The structure of the conventional full bridge and half bridge three-port converters are shown in the Figure 1.7 [23–25], from which it can be seen that the advantages of the three-port converter compared with the different two-port converters in terms of the number of components and the design and control complexity are not so obvious due to the additional bridge. In [26] and [27], the resonant tanks are added to the conventional three-port converters to improve their performance.

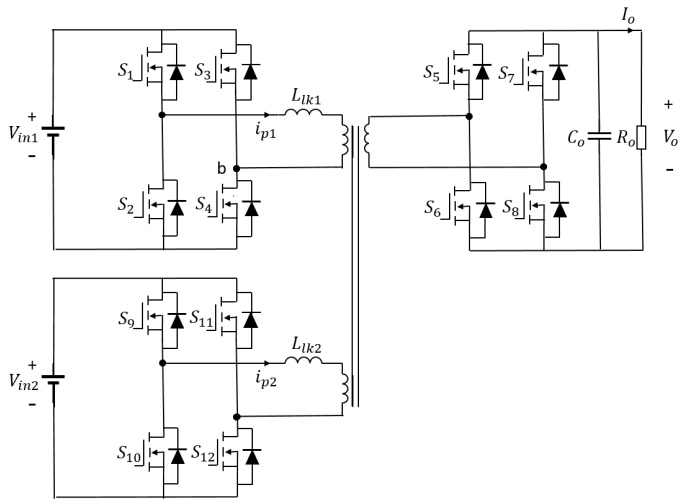
A novel LLC integrated partly isolated three-port DC-DC converter is proposed in [21], which integrates two interleaved buck-boost converters with a full bridge LLC converter. The structure of this two buck-boost integrated LLC converter is redrawn and shown in the Figure 1.8. A $500W$ prototype, in which the PV voltage is $65V - 115V$, the input voltage is $165V - 200V$ and the output voltage is $360V$, is built and tested. This structure is helpful to the ripple sensitive energy sources such as solar and fuel cell since the two interleaved buck-boost converters can have a phase shift which can reduce the current ripple. Moreover, the switches in the two buck/boost converters can be reused as the primary side switches of the full bridge LLC converter, which reduces the number of the components in the whole converter. However, this structure cannot realize the bidirectional power flow due to the uncontrolled rectifier in the secondary side. Fortunately, this topology can be evolved into the one which integrates the two interleaved bidirectional buck/boost converters with a DAB converter or a bidirectional CLLC resonant converter which has the capability of bidirectional power flow.

A $300W$ dual buck/boost integrated three-port bidirectional DC-DC converter which integrates two buck/boost converters with the DAB converter and has a half bridge secondary side is built and tested in [3]. The schematic of this converter is shown in the Figure 1.9. The voltage at the PV port is $60V$, the voltage at the battery port is $24V$ and the output voltage is $102V$. The power transfer between the two input ports and the input and output ports, the performance characteristic and the soft switching of all the switches are verified. A full bridge three-port bidirectional DC-DC converter which integrates two boost converters and the full bridge DAB converter is proposed in [28]. The power rating of this converter is $250kW$ and the output voltage is $7000V$. The functionality and the characteristic of this converter are verified in simulation.

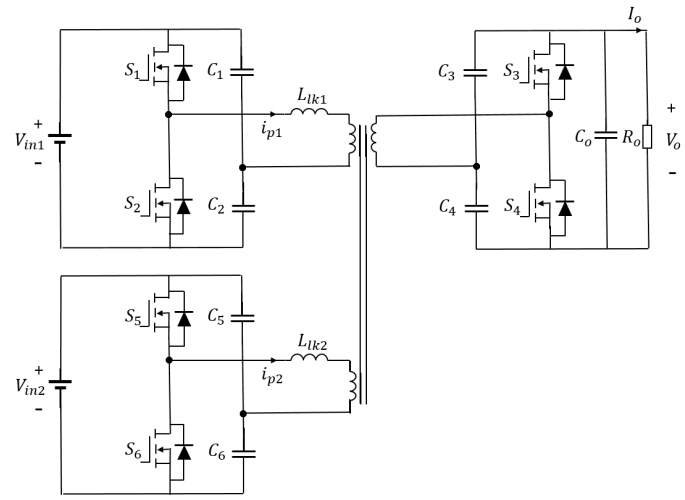
In the above studies, all the existing designs do not consider the applications which require the high power (equal or larger than $10kW$) and also the large output voltage range ($200V - 950V$) which are the specifications of the converter in this master thesis project.

1.5.2. Review of the modulation strategies

For the three-port DC-DC converter integrating two buck/boost converters with the full bridge converter, the phase-shift plus the pulse width modulation (PWM) is proposed in [29] and [30]. This modulation strategy can realize the power flow control among the three ports and also regulate the output voltage. The control is performed by using two control variables: the duty cycles of the primary side switches and the phase shift between the two switch legs in the primary side. This primary-side



(a) Conventional bidirectional full bridge three-port converter



(b) Conventional bidirectional half bridge three-port converter

Figure 1.7: Conventional bidirectional full bridge and half bridge three-port converter topologies

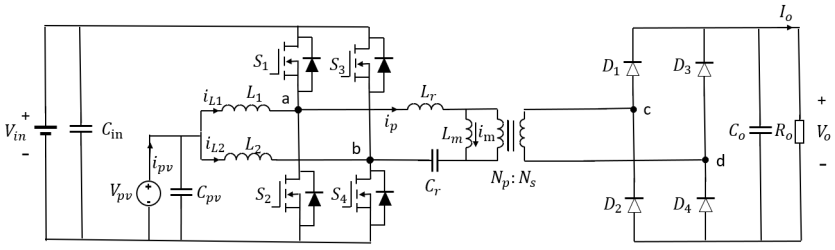


Figure 1.8: The two buck/boost integrated LLC converter

phase-shift (PSPS) plus PWM modulation increases the design flexibility of the multiport converters. However, the main drawback of this modulation strategy is that the soft switching range is very limited and the power flow between the primary side and secondary side cannot be bidirectional. Moreover, the conduction losses are relatively high in the PSPS plus PWM modulated multiport converter because of the circulating current at the freewheeling stage. The secondary-side phase-shift (SSPS) plus PWM modulation is proposed in [31–33], which can widen the soft switching range of the switches and also reduce the circulating current to get less conduction losses. This modulation strategy is used in a full

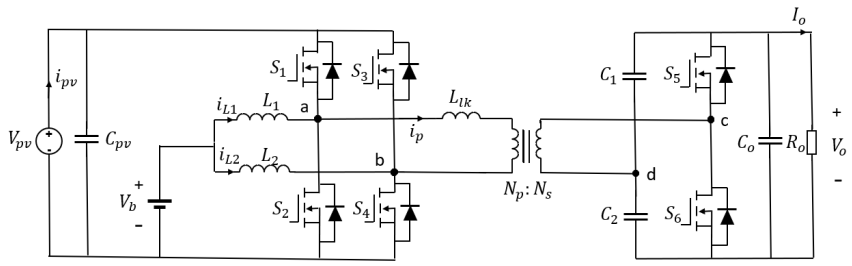


Figure 1.9: The two buck/boost integrated DAB converter with half bridge secondary side

bridge three-port converter where the two lower diodes in the secondary side of the full bridge are replaced by two switches. The phase shift between the two legs in the primary side is $180°$ to get the minimal current ripple. There are still two control freedoms left, the phase shift between the gate signals of the primary side switches and the secondary side switches and the duty cycle of the primary side switches. However, this kind of converter cannot realize the bidirectional power flow between the primary side and secondary side either.

Generally, the resonant converter is modulated by using the pulse frequency modulation (PFM). The main drawback of this modulation is that the input and output voltage range is very narrow since the voltage gain is only regulated by the switching frequency. The switching frequency needs to be varied in a large range if the input voltage range or the load variation range is wide, which is a big challenge for the magnetic components. The hybrid modulation of PWM and PFM used in the LLC resonant converter is proposed in [34–36]. The hybrid modulation can effectively increase the input voltage range and the load variation range. The hybrid modulation of PWM and PFM is also used in the three-port bidirectional CLLC resonant converter in [37] which uses the PFM to achieve higher voltage gain and uses the PWM to achieve the lower voltage gain. A $1kW$ prototype is designed and implemented to charge a $150V$ to $250V$ battery pack, the switching frequency range is $60.2kHz - 99.7kHz$ and the maximum efficiency is 96.14% with $390V$ input voltage at rated $1kW$. It can be seen from this case that the buck/boost integrated CLLC resonant converter is not suitable for the application with a very large output voltage range since the output voltage variation from $150V$ to $250V$ has already resulted in a frequency variation from $60.2kHz$ to $99.7kHz$.

1.5.3. Summary of the literature review

Based on the above studies, several conclusions need to be emphasized:

- The novel two buck-boost integrated three-port DC-DC converter is a very good choice to realize the more compact and more efficient PV integrated EV charging system since the interleaved structure in the primary side is suitable for the PV array which is a current sensitive energy source. Besides, the reuse of the switches in the primary side can reduce the cost of the whole system.

- The half bridge structure is more suitable for the low power application and the full bridge structure is more suitable for the high power application because the current stress on the components of the half bridge structure is much larger than that of the full bridge structure.

- The CLLC resonant converter has a higher efficiency than the DAB converter but it is more suitable for the application with a narrow output voltage range since the efficiency will be reduced once the operating frequency is far from the resonant frequency. Besides, the design and control complexity of the CLLC resonant converter is larger than that of the DAB converter when it operates with a large output voltage range due to the larger number of design considerations.

A dual boost integrated DAB converter with the full bridge secondary side is investigated and the SSPS plus PWM modulation is used in this master thesis project according to these conclusions.

1.6. Project contributions

This master thesis project is the first step to investigate the novel isolated DC-DC converter for the PV integrated bidirectional EV charging system to make the whole system more compact and more efficient. Besides, the investigated converter can be compatible with the new CHAdeMO standard (CHAdeMO 2.0) regarding the charging voltage range requirement. The main contributions of this project are:

- The feasibility to use the dual boost integrated DAB converter with a full bridge secondary side for the PV integrated bidirectional EV charging system with the $10kW$ power rating has been investigated in this thesis. The investigated converter can be compatible with the new CHAdeMO standard (CHAdeMO 2.0) regarding the charging voltage range requirement.
- The analysis tool which can analyze the voltage and current at different points, the output power, the soft switching region of the switches and the circulating power in the investigated converter is developed in Mathcad. All the key parameters of this converter such as the input voltage, the PV voltage, the output voltage, the switching frequency, the leakage inductance, the inductance of the boost inductors and the turn ratio of the transformer are the inputs of the analysis tool and all these parameters can be changed and the results in terms of the important voltage and current waveforms, the output power curve, the soft switching region map of the switches and the circulating power curve can be drawn immediately.
- The simulation model including the control loops of the dual boost integrated DAB converter is built in the PLECS. The feasibility of the SSPS plus PWM modulation method, the new modulation method which changes the full bridge secondary side to the half bridge one when the DC blocking capacitor voltage control is used and the analysis results got from the analysis tool are verified by the simulation results.
- The ZVS characteristic of the switches and the circulating power in the dual boost integrated DAB converter are investigated by considering the DC bus voltage, PV voltage, and the EV battery voltage, and then the ZVS region is enlarged by applying the DC blocking capacitor voltage control. The effect of the DC blocking capacitor voltage control on the soft switching region, the power losses of the switches and the circulating power in the converter when it is working with a large voltage range is analyzed and tested.
- The method which uses the thermal model to evaluate the power losses and the maximum junction temperature of the switches in a designed converter is proposed in this thesis. The proposed method and the built thermal model can be used to check the feasibility of the converter design and to estimate the efficiency of the designed converter.
- A test bench of the investigated converter is built by doing the modifications on a CLLC resonant converter and connecting the newly designed components to it. The analysis and simulation results got from the Mathcad and the PLECS as well as the implementability of the dual boost integrated DAB converter are verified by the experiment results.

1.7. Structure of the thesis

This thesis is composed of the following five chapters:

- Chapter 1 introduces the background, the motivation, the research objectives and research questions, the research methodology, the literature review and the contributions of this master thesis project.
- Chapter 2 clarifies the specifications of the converter and describes the circuit of the dual boost integrated DAB converter. The working principle of the two interleaved boost converters in the primary side and the working principle of the whole converter are analyzed in this chapter. Besides, the parameters of the investigated converter are calculated and all the equations in terms of the voltage, the current and the output power are deduced. The power modes and the control structure of the dual boost integrated DAB converter are also shown in this chapter.

- Chapter 3 mainly focuses on the power loss modeling and analysis of all the switches in the dual boost integrated DAB converter. The ZVS characteristic of the switches and the circulating power in the dual boost integrated DAB converter are investigated by considering the DC bus voltage, PV voltage, and the EV battery voltage, and then the ZVS region is enlarged by applying the DC blocking capacitor voltage control. All the equations related to the soft switching of the switches and the circulating power are deduced in this chapter. All the analysis is verified by the simulation results. Besides, the transistor candidates are chosen and the power loss model and the thermal model of the candidates are built. The loss breakdown, the loss ratio and the thermal performance of the switches are analyzed and evaluated.
- Chapter 4 presents the content of the experimental tests. First of all, the two boost inductors are designed. A comparison of gapped ferrite cores and powder cores is done and a summarized procedure about the design of the inductors with the powder core is introduced. Then, the FPGA programming is developed to do the open loop control of the converter. Afterwards, the test of the original board has been done to check the gate driver circuit and the dedicated power supply, so any error can then be identified at a much earlier stage of the experimental test. All the experimental test results are shown in this chapter, which can verify the previous analysis.
- Chapter 5 gives the conclusions summarized from the previous analysis and the experiment test and also points out the future work of this project.

2

Working principle and control

2.1. Specifications of the converter

The dual boost integrated DAB converter used for the PV integrated EV charging system, which consists of two non-isolated boost converters and an isolated DAB converter is the research object of this work. According to the data sheet of ABB's $10kW$ PV inverter, the full power maximum power point tracking (MPPT) voltage range is $220V - 470V$ [38]. Hence, the voltage range of the PV port of the three-port converter in this master thesis project is $220V - 470V$. The voltage at the DC bus port can be changed from $600V$ to $900V$ which is decided by the power factor correction module in the system. The maximum output voltage is $950V$ which can make sure that the converter can support both all the existing $500V$ battery EVs and the next generation high voltage EVs. The maximum output current is $30A$ which is decided by the design requirement of ABB's EV charger. All the specifications of the converter are summarized in the Table 2.1.

Table 2.1: Converter specifications

Parameters	Specifications
Voltage range at the DC bus port	$600V - 900V$
Voltage range at the PV port	$220V - 470V$
Voltage range at the output port	$200V - 950V$
Maximum output power	$10kW$
Maximum output current	$30A$

2.2. Working principle of the two interleaved boost converters

The schematic of the two interleaved boost converters is shown in the Figure 2.1. Two boost inductors (L_1 and L_2) are connected to the mid-points of the two switch legs. The two switch legs are shifted $180°$ in this master thesis project in order to get the minimum PV current ripple. The gate signals of the two switches in the same leg are complementary. The output voltage of the two interleaved boost converters is regulated by regulating the duty cycle D of the lower switches (S2 and S4) and can be matched with the input voltage of the DAB converter V_{in}.

The currents of the two boost inductors and the PV current can be calculated by equation 2.1 , equation 2.2 and equation 2.3.

$$i_{L1}(t) = \int_0^t \frac{V_{pv} - u_a(t)}{L_1} dt + i_{L1_0} \tag{2.1}$$

$$i_{L2}(t) = \int_0^t \frac{V_{pv} - u_b(t)}{L_2} dt + i_{L2_0} \tag{2.2}$$

$$i_{pv}(t) = i_{L1}(t) + i_{L2}(t) \tag{2.3}$$

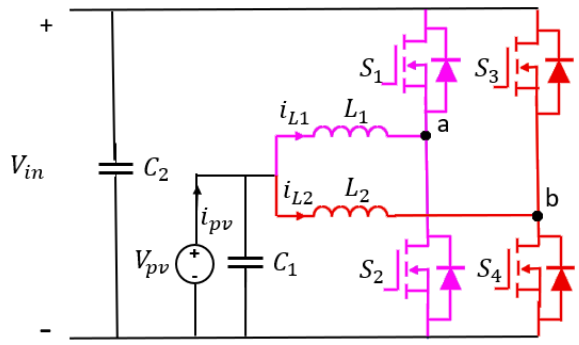


Figure 2.1: The schematic of the two interleaved boost converters

i_{L1_0} and i_{L2_0} are the initial values of i_{L1} and i_{L2} respectively.

The key waveforms of the two interleaved boost converters are shown in the Figure 2.2.

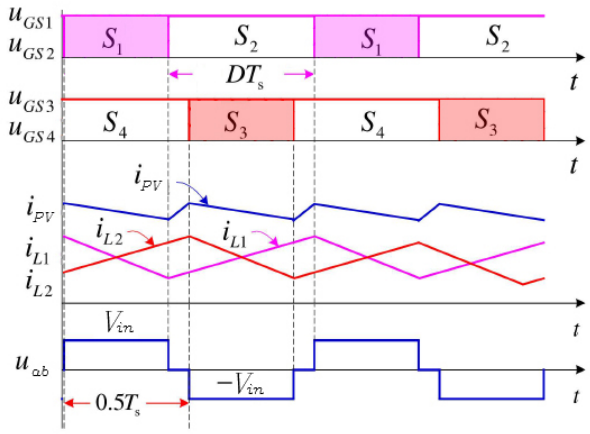


Figure 2.2: The key waveforms of the two interleaved boost converters

It can be seen from the Figure 2.2, there is a high frequency AC voltage u_{ab} between the mid-points of the two switch legs. The pulse width of the high frequency AC voltage will change when the duty cycles of the switches are changed. Hence, the two interleaved boost converters can be also took as a full bridge inverter and the AC voltage produced by this full bridge inverter can produce a stable DC voltage by connecting a rectifier to the inverter. The DC voltage can be the output of the third port, then the three-port converter is formed. The structure of the novel three-port converter is shown in the Figure 2.3.

In order to realize the galvanic isolation, the high frequency transformer can be added between the inverter and the rectifier.

The novel three-port converter has following advantages:

- The two ports in the primary side of the three-port converter are bidirectional and the partly isolated output port can be unidirectional or bidirectional, so the application of this novel three-port converter is flexible.
- The reduced power conversion stages between different ports can improve the conversion efficiency of the whole system.
- It is possible to realize the soft switching of all the switches in this converter.
- The two interleaved buck-boost converters can significantly reduce the current ripple, which is suitable for the current sensitive input source such as the PV panels.

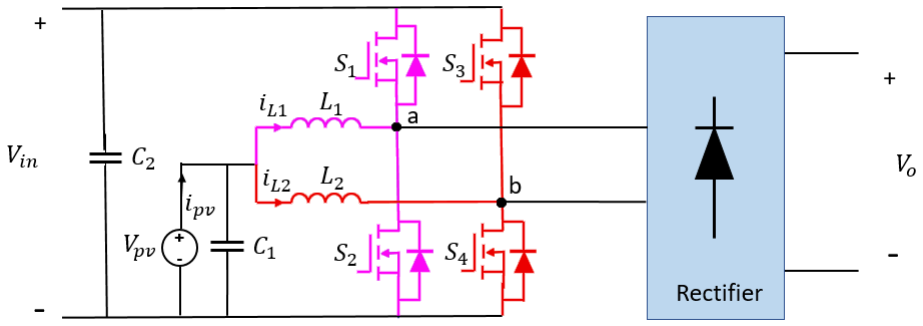


Figure 2.3: The structure of the novel three-port converter

- The primary side and the secondary side can use different control methods, so the decoupled control of the power ports can be realized.

2.3. Circuit description and parameter design

The schematic of the dual boost integrated DAB converter is shown in the Figure 2.4. The two input ports in the primary side are connected to the PV panels and the DC bus, respectively. The isolated output port is connected to the EV battery. From the PV port to the DC bus port, the converter works as a boost converter while from the DC bus port to the isolated output port, it works as a DAB converter. Hence, the active switches on the primary side are used as the interleaved boost converters and the primary side switches of the DAB converter simultaneously. L_{lk} is the leakage inductance of the transformer which determines how much power can be transferred from the primary side to the secondary side. And if this leakage inductance is not large enough to provide the power required, an extra inductor will be needed.

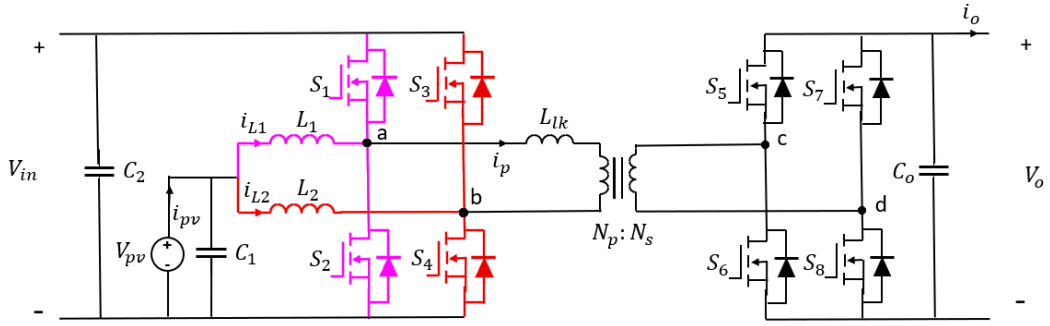


Figure 2.4: The schematic of the dual boost integrated DAB converter

The main parameters of this converter can be chosen and designed as follows:

- Switching frequency (f_{sw}): Consider the electromagnetic compatibility (EMC) requirement, the secondary harmonic frequency should be less than $150kHz$, so the suitable choice of the switching frequency can be $48kHz-65kHz$. In order to reduce the size of the whole converter, the switching frequency is set as $65kHz$.

- Inductance of the two boost inductors (L_1 and L_2): For the cost consideration, the current ripple of the inductor in the boost converter which is connected to the PV panels is generally set as 20% of the maximum average current. In this project, the worst situation of the current ripple will happen when the PV panel has the maximum power ($10kW$) and minimum voltage ($220V$) and the DC bus has the maximum voltage ($900V$). In this case, the average inductor current and the minimum and maximum value of the inductor current are:

$$I_{L1_{ave}} = \frac{P_{pv}}{2V_{pv}} = 22.727A \tag{2.4}$$

$$I_{L1_{min}} = I_{L1_{ave}} * (1 - 0.2) = 18.182A \tag{2.5}$$

$$I_{L1_{max}} = I_{L1_{ave}} * (1 + 0.2) = 27.273A \tag{2.6}$$

The duty cycle (D) of the boost converter is:

$$D = 1 - \frac{V_{pv}}{V_{in}} = 0.756 \tag{2.7}$$

The turn on time (T_{on}) of the boost converter is:

$$T_{on} = D * \frac{1}{f_{sw}} = 1.162 * 10^{-5}s \tag{2.8}$$

According to the Figure 2.2 and the equation 2.1, the inductance of L_1 is:

$$L_1 = \frac{T_{on}V_{pv}}{I_{L1_{max}} - I_{L1_{min}}} = 2.813 * 10^{-4}H \tag{2.9}$$

The inductance of L_2 uses the same value as that of L_1.

- Turn ratio of the transformer (n): For the $10kW$ EV charging system, the critical operating point is when the EV voltage is $333.3V$, simply set the turn ratio of the transformer (n) as 2 since the DC bus voltage can change from $600V$ to $900V$.
- Leakage inductance of the transformer (L_{lk}): According to the power equation of the conventional single phase shifted DAB converter, which is deduced in [39] and can be expressed as:

$$P_{out} = \frac{nV_{in}V_o\Phi(\pi - \Phi)}{2(\pi)^2 f_{sw}L_{lk}} \tag{2.10}$$

where Φ is the phase shift angle between u_{ab} and u_{cd}. When $\Phi = \frac{\pi}{2}$, the P_{out} is maximum. Since the maximum output power required in this project is $10kW$, the leakage inductance can be calculated by the equation 2.10 and the calculation result is $L_{lk} = 8.545 * 10^{-5}H$.

2.4. Working principle of the dual boost integrated DAB converter

In order to analyze the operation characteristics of the dual boost integrated DAB converter, the whole converter can be simplified to a structure which is shown in the Figure 2.5.

When the duty cycle D of S2 and S4 is equal or less than 0.5, the pulse width of u_{ab} is DT_s , where T_s is the period time. When the duty cycle D of S2 and S4 is larger than 0.5, the pulse width of u_{ab} is $(1 - D)T_s$. The gate signals and the two different cases of u_{ab} are shown in the Figure 2.6.

The current and the voltage of the leakage inductance have eight different cases which are defined according to the different D and the different δ which is the phase shift between the gate signals of S1 and S5. The turn-on time (T_{on}) and turn-off time (T_{off}) of S2 and S4 can be calculated by the equation 2.11 and equation 2.12. The different cases and the boundary conditions are shown in the Table 2.2.

$$T_{on} = DT_s \tag{2.11}$$

$$T_{off} = T_s - T_{on} \tag{2.12}$$

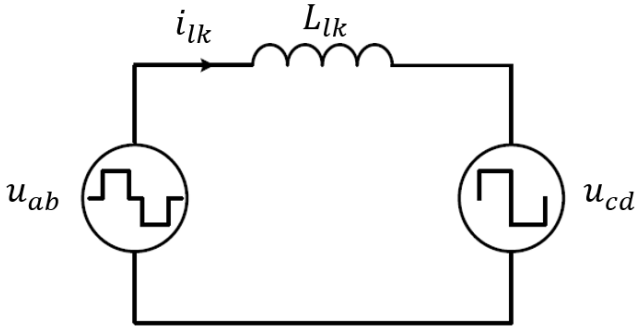
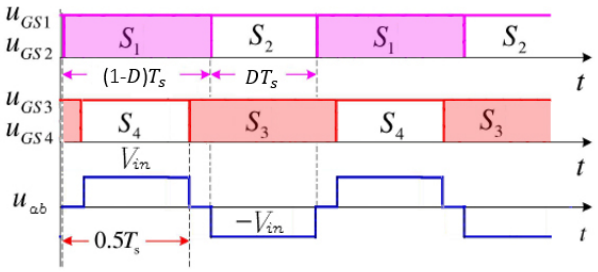
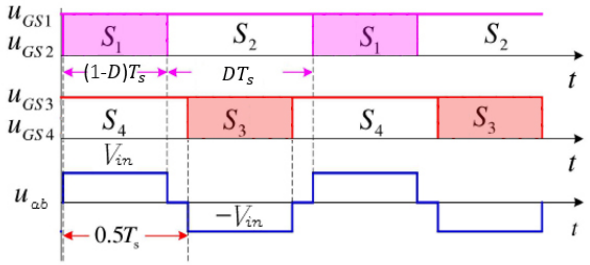


Figure 2.5: The equivalent circuit of the dual boost integrated DAB converter



(a) The gate signals and u_{ab} when D is equal or less than 0.5



(b) The gate signals and u_{ab} when D is larger than 0.5

Figure 2.6: The gate signals and the two different cases of u_{ab}

Table 2.2: The different cases of the current and voltage of the leakage inductance and the boundary conditions

Case	Boundary Condition ($D \leq 0.5$)	Case	Boundary Condition ($D > 0.5$)
I	$0 \leq \delta < (\frac{T_{off}}{T} - \frac{1}{2})$	V	$0 \leq \delta < (\frac{T_{off}}{T})$
II	$(\frac{T_{off}}{T} - \frac{1}{2}) \leq \delta < (\frac{1}{2})$	VI	$(\frac{T_{off}}{T}) \leq \delta < (\frac{1}{2})$
III	$(\frac{1}{2}) \leq \delta < (\frac{T_{off}}{T})$	VII	$(\frac{1}{2}) \leq \delta < (\frac{T_{off}}{T} + \frac{1}{2})$
IV	$(\frac{T_{off}}{T}) \leq \delta \leq 1$	VIII	$(\frac{T_{off}}{T} + \frac{1}{2}) \leq \delta \leq 1$

Every switching cycle of the dual boost integrated DAB converter can be divided into six stages. Take Case V as an example to analyze the operation principle of this converter. The gate signals and the key waveforms of Case V in steady state are shown in the Figure 2.7 and the equivalent circuit of each stage is shown in the Figure 2.8.

- Stage I $[t_0 - t_1]$[Figure 2.8a]:
  At t_0, switches S1, S4, S6 and S7 are on and the power is delivered from the primary side to the

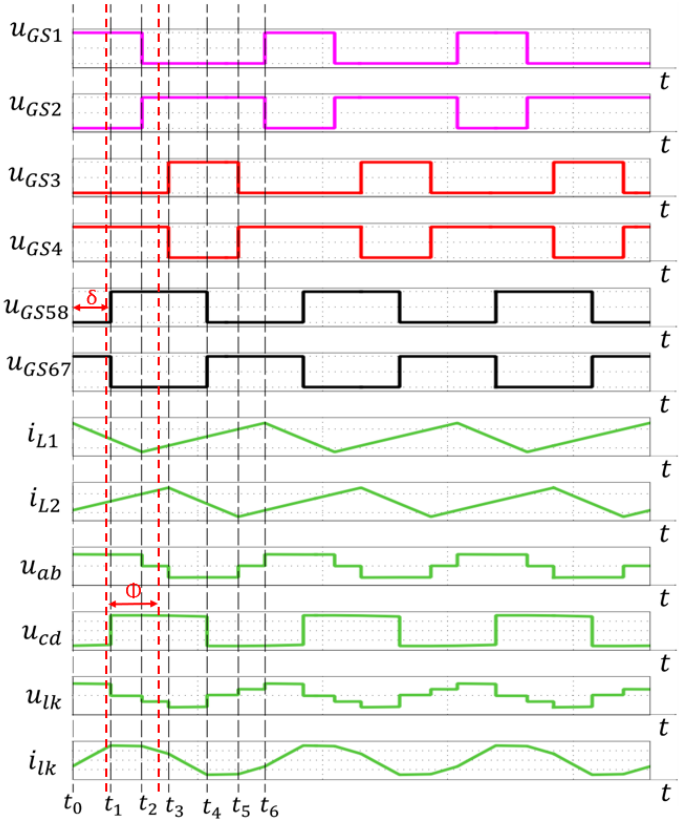


Figure 2.7: The gate signals and the key waveforms of Case V

secondary side. Once S6 and S7 are turned off and the i_{lk} reaches its maximum value, this stage ends. The output voltage of the primary side bridge (u_{ab}) is V_{in} during this stage. The voltage on the secondary side of the transformer (u_{cd}) is $-V_o$ during this stage. The voltage on the leakage inductance during this stage is $V_{in} + nV_o$, where $n = \frac{N_p}{N_s}$ is the turn ratio of the transformer. The current flowing through the leakage inductance i_{lk} can be expressed as:

$$i_{lk}(t) = \int_0^t \frac{V_{in} + nV_o}{L_{lk}} dt + i_{Llk_0} \tag{2.13}$$

Neglect all the losses in the converter, the output power in this stage can be expressed as:

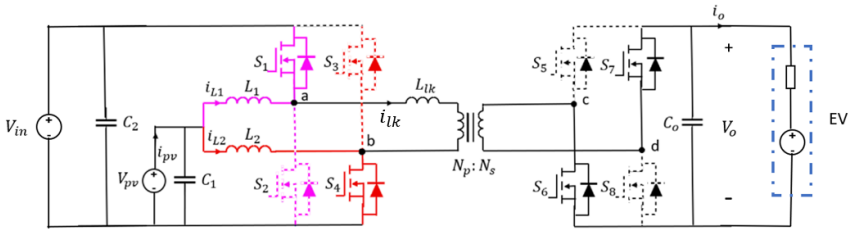
$$P_{out}(t) = \int_0^t (V_{in})(t * \frac{V_{in} + nV_o}{L_{lk}} + i_{Llk_0})dt \tag{2.14}$$

where i_{Llk_0} is the initial value of the leakage inductance current and $0 \leq t \leq t_1$. The initial value of the leakage inductance current will not influence the output power, so it can be neglected in the power calculation.

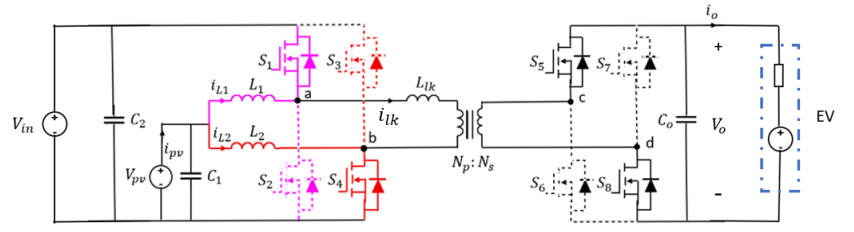
Since the phase shift δ is defined as the shift between the gate signals of S1 and S5, $t_1 = \delta * T_s$. The current flowing through the leakage inductance i_{lk} and the output power at the end of Stage I can be expressed as:

$$i_{lk}(t_1) = \frac{V_{in} + nV_o}{L_{lk}} * \delta T_s + i_{Llk_0} \tag{2.15}$$

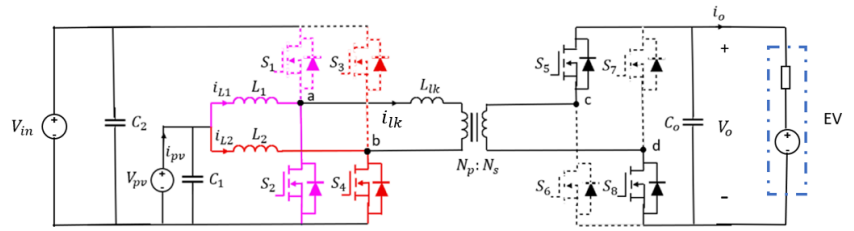
$$P_{out}(I) = \frac{T_s^2 \delta^2 V_{in}(V_{in} + nV_o)}{2L_{lk}} \tag{2.16}$$



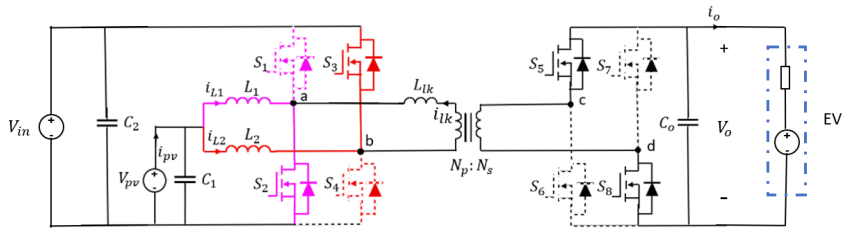
(a) The equivalent circuit of stage I



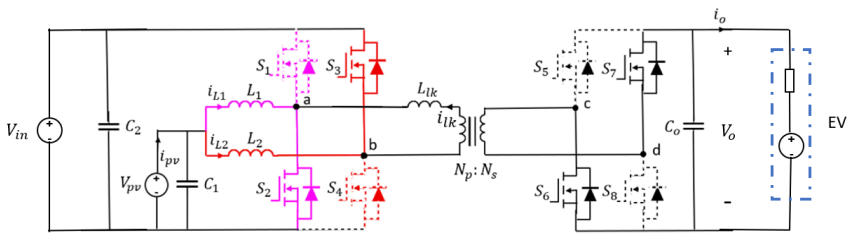
(b) The equivalent circuit of stage II



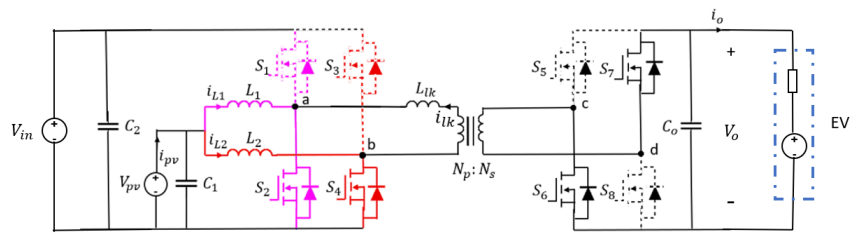
(c) The equivalent circuit of stage III



(d) The equivalent circuit of stage IV



(e) The equivalent circuit of stage V



(f) The equivalent circuit of stage VI

Figure 2.8: The equivalent circuit of each stage

- Stage II $[t_1 - t_2]$[Figure 2.8b]:

  At t_1, the secondary side switches S5 and S8 are turned on and this stage will end when the S1 is turned off. The output voltage of the primary side bridge (u_{ab}) is V_{in} during this stage. The voltage on the secondary side of the transformer (u_{cd}) is V_o. The voltage on the leakage inductance during this stage is $V_{in} - nV_o$. The current flowing through the leakage inductance i_{lk} and the output power P_{out} can be expressed as:

$$i_{lk}(t) = i_{lk}(t_1) + \int_{t_1}^{t} \frac{V_{in} - nV_o}{L_{lk}} dt \tag{2.17}$$

$$P_{out}(t) = \int_{t_1}^{t} V_{in}(i_{lk}(t_1) + (t - t_1) * \frac{V_{in} - nV_o}{L_{lk}})dt \tag{2.18}$$

  where $t_1 < t \leq t_2$.

  Since this stage ends when the S1 is turned off, $t_2 = T_{off}$. The current flowing through the leakage inductance i_{lk} and the output power at the end of Stage II can be expressed as:

$$i_{lk}(t_2) = i_{lk}(t_1) + \frac{V_{in} - nV_o}{L_{lk}} * (T_{off} - \delta T_s) \tag{2.19}$$

$$P_{out}(II) = \frac{V_{in}(T_{off} - \delta T_s)(T_{off}V_{in} + T_s\delta V_{in} - T_{off}nV_o + 3T_s\delta nV_o)}{2L_{lk}} \tag{2.20}$$

- Stage III $[t_2 - t_3]$[Figure 2.8c]:

  At t_2, the S2 is turned on. In this stage, both S2 and S4 are on, u_{ab} is 0 and the boost inductors (L_1 and L_2) are charged. This stage ends when S3 is turned on. The voltage on the secondary side of the transformer (u_{cd}) is V_o. The voltage on the leakage inductance during this stage is $-nV_o$. The current flowing through the leakage inductance i_{lk} and the output power P_{out} can be expressed as:

$$i_{lk}(t) = i_{lk}(t_2) + \int_{t_2}^{t} \frac{-nV_o}{L_{lk}} dt \tag{2.21}$$

$$P_{out}(t) = \int_{t_2}^{t} 0 * (i_{lk}(t_2) + (t - t_2) * \frac{-nV_o}{L_{lk}})dt \tag{2.22}$$

  where $t_2 < t \leq t_3$.

  Since this stage ends when the S3 is turned on, $t_3 = \frac{T_s}{2}$. The current flowing through the leakage inductance i_{lk} and the output power at the end of Stage III can be expressed as:

$$i_{lk}(t_3) = i_{lk}(t_2) + \frac{-nV_o}{L_{lk}} * (\frac{T_s}{2} - T_{off}) \tag{2.23}$$

$$P_{out}(III) = 0 \tag{2.24}$$

  Due to the symmetry of the current waveform,

$$i_{lk}(t_3) + i_{Llk_0} = 0 \tag{2.25}$$

$$i_{Llk_0} = -\frac{2T_{off}V_{in} - T_sV_on + 4T_sV_o\delta n}{4L_{lk}} \tag{2.26}$$

- Stage IV $[t_3 - t_4]$[Figure 2.8d]:

  At t_3, the S3 is turned on. In this stage, S2 and S3 are on, u_{ab} is $-V_{in}$. This stage ends when S5 and S8 are turned off. The voltage on the secondary side of the transformer (u_{cd}) is V_o. The voltage on the leakage inductance during this stage is $-V_{in} - nV_o$. The current flowing through the leakage inductance i_{lk} and the output power P_{out} can be expressed as:

$$i_{lk}(t) = i_{lk}(t_3) + \int_{t_3}^{t} \frac{-V_{in} - nV_o}{L_{lk}} dt \tag{2.27}$$

$$P_{out}(t) = \int_{t_3}^{t} (-V_{in})(i_{lk}(t_3) + (t - t_3) * \frac{-V_{in} - nV_o}{L_{lk}})dt \tag{2.28}$$

  where $t_3 < t \leq t_4$.

  Since this stage ends when the S5 and S8 are turned off, $t_4 = (\delta + \frac{1}{2}) * T_s$. The current flowing through the leakage inductance i_{lk} and the output power at the end of Stage IV can be expressed as:

$$i_{lk}(t_4) = i_{lk}(t_3) + \frac{-V_{in} - nV_o}{L_{lk}} * ((\delta + \frac{1}{2})T_s - \frac{T_s}{2}) \tag{2.29}$$

$$P_{out}(IV) = \frac{T_s\delta V_{in}(T_s\delta V_{in} - 2T_{off}V_{in} + T_s nV_o - 3T_s\delta nV_o)}{2L_{lk}} \tag{2.30}$$

- Stage V $[t_4 - t_5]$[Figure 2.8e]:

  At t_4, the S6 and S7 are turned on. In this stage, S2 and S3 are on, u_{ab} is $-V_{in}$. This stage ends when S3 is turned off. The voltage on the secondary side of the transformer (u_{cd}) is $-V_o$. The voltage on the leakage inductance during this stage is $-V_{in} + nV_o$. The current flowing through the leakage inductance i_{lk} and the output power P_{out} can be expressed as:

$$i_{lk}(t) = i_{lk}(t_4) + \int_{t_4}^{t} \frac{-V_{in} + nV_o}{L_{lk}} dt \tag{2.31}$$

$$P_{out}(t) = \int_{t_4}^{t} (-V_{in})(i_{lk}(t_4) + (t - t_4) * \frac{-V_{in} + nV_o}{L_{lk}})dt \tag{2.32}$$

  where $t_4 < t \leq t_5$.

  Since this stage ends when the S3 is turned off, $t_5 = \frac{T_s}{2} + T_{off}$. The current flowing through the leakage inductance i_{lk} and the output power at the end of Stage V can be expressed as:

$$i_{lk}(t_5) = i_{lk}(t_4) + \frac{-V_{in} + nV_o}{L_{lk}} * (\frac{T_s}{2} + T_{off} - (\delta + \frac{1}{2})T_s) \tag{2.33}$$

$$P_{out}(V) = -\frac{V_{in}(T_{off} - T_s\delta)(T_{off}V_{in} - T_s\delta V_{in} - T_s nV_o + T_{off}nV_o + T_s\delta nV_o)}{2L_{lk}} \tag{2.34}$$

- Stage VI $[t_5 - t_6]$[Figure 2.8f]:

  At t_5, the S4 is turned on. In this stage, both S2 and S4 are on, u_{ab} is 0 and the boost inductors (L_1 and L_2) are charged. This stage ends when S2 is turned off. The voltage on the secondary side of the transformer (u_{cd}) is $-V_o$. The voltage on the leakage inductance during this stage is nV_o. The current flowing through the leakage inductance i_{lk} and the output power P_{out} can be expressed as:

$$i_{lk}(t) = i_{lk}(t_5) + \int_{t_5}^{t} \frac{nV_o}{L_{lk}} dt \tag{2.35}$$

$$P_{out}(t) = \int_{t_5}^{t} 0 * (i_{lk}(t_5) + (t - t_5) * \frac{nV_o}{L_{lk}})dt \tag{2.36}$$

where $t_5 < t \leq t_6$.

The current flowing through the leakage inductance i_{lk} and the output power at the end of Stage VI can be expressed as:

$$i_{lk}(t_6) = i_{lk}(t_5) + \frac{nV_o}{L_{lk}} * (T_s - (\frac{T_s}{2} + T_{off})) \tag{2.37}$$

$$P_{out}(VI) = 0 \tag{2.38}$$

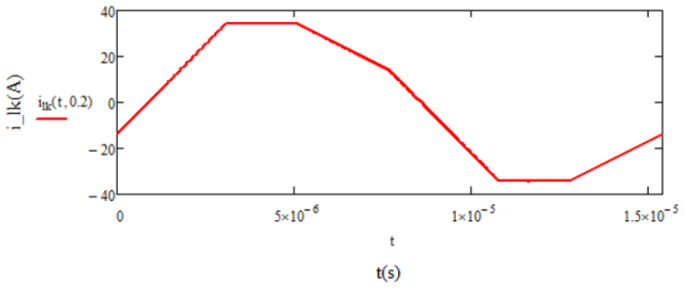
The average output power in the whole switching cycle can be calculated by:

$$P_{out} = \frac{P_{out}(I) + P_{out}(II) + P_{out}(III) + P_{out}(IV) + P_{out}(V) + P_{out}(VI)}{T_s} \tag{2.39}$$

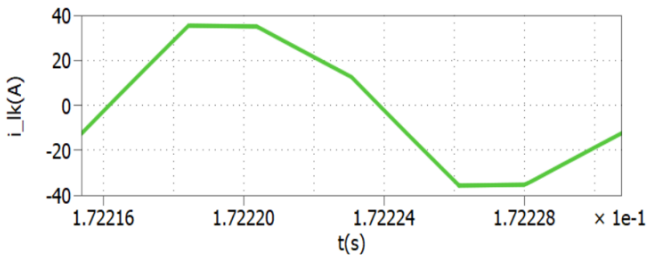
Hence,

$$P_{out}(\delta)(CaseV) = \frac{nV_{in}V_o(4T_sT_{off}\delta - 4T_s^2\delta^2 + T_sT_{off} - 2T_{off}^2)}{2L_{lk}T_s} \tag{2.40}$$

Using the Mathcad programming to plot the current waveform of the current flowing through the leakage inductance according to the deduced equations and compare this waveform to the one which is taken from the simulation in PLECS. The comparison result can prove the correctness of the equations. The waveforms of the leakage inductance current taken from Mathcad and PLECS when the DC bus voltage is $666.6V$, the PV voltage is $220V$, the EV battery voltage is $333.3V$ and the phase shift δ is 0.2 are shown in the Figure 2.9.



(a) The waveform taken from Mathcad



(b) The waveform taken from PLECS

Figure 2.9: The waveforms of the leakage inductance current taken from Mathcad and PLECS

By using the same methods, the values of the current flowing through the leakage inductance (i_{lk}) at time points t_0 - t_6 and the average output power in all the eight cases can be deduced.

- Case I:

  The current flowing through the leakage inductance (i_{lk}) at time points t_0 - t_6 is:

$$i_{lk}(t_0) = -\frac{2T_{on}V_{in} - T_sV_on + 4T_sV_o\delta n}{4L_{lk}} \tag{2.41}$$

$$i_{lk}(t_1) = i_{lk}(t_0) + \frac{T_sV_o\delta n}{L_{lk}} \tag{2.42}$$

$$i_{lk}(t_2) = i_{lk}(t_0) - \frac{T_sV_on}{2L_{lk}} + \frac{T_{on}V_on}{L_{lk}} + \frac{2T_sV_o\delta n}{L_{lk}} \tag{2.43}$$

$$i_{lk}(t_3) = i_{lk}(t_0) + \frac{T_{on}V_{in}}{L_{lk}} - \frac{T_sV_on}{2L_{lk}} + \frac{2T_sV_o\delta n}{L_{lk}} \tag{2.44}$$

$$i_{lk}(t_4) = i_{lk}(t_0) + \frac{T_{on}V_{in}}{L_{lk}} - \frac{T_sV_on}{2L_{lk}} + \frac{T_sV_o\delta n}{L_{lk}} \tag{2.45}$$

$$i_{lk}(t_5) = i_{lk}(t_0) + \frac{T_{on}V_{in}}{L_{lk}} - \frac{T_sV_on}{L_{lk}} + \frac{T_{off}V_on}{L_{lk}} \tag{2.46}$$

$$i_{lk}(t_6) = i_{lk}(t_0) \tag{2.47}$$

  The average output power in the whole switching cycle is:

$$P_{out}(\delta)(CaseI) = \frac{nV_{in}V_o(T_s - T_{off})(T_s - 2T_{off} + 4T_s\delta)}{2L_{lk}T_s} \tag{2.48}$$

- Case II:

  The current flowing through the leakage inductance (i_{lk}) at time points t_0 - t_6 is:

$$i_{lk}(t_0) = -\frac{2T_{on}V_{in} - T_sV_on + 4T_sV_o\delta n}{4L_{lk}} \tag{2.49}$$

$$i_{lk}(t_1) = i_{lk}(t_0) - \frac{T_sV_on}{2L_{lk}} + \frac{T_{off}V_on}{L_{lk}} \tag{2.50}$$

$$i_{lk}(t_2) = i_{lk}(t_0) + \frac{T_sV_{in} - 2T_{off}V_{in} + 2\delta T_sV_{in} + 2\delta T_snV_o}{2L_{lk}} \tag{2.51}$$

$$i_{lk}(t_3) = i_{lk}(t_0) + \frac{2T_sV_{in} - 2T_{off}V_{in} - T_sV_on + 4T_sV_o\delta n}{2L_{lk}} \tag{2.52}$$

$$i_{lk}(t_4) = i_{lk}(t_0) + \frac{T_sV_{in} - T_{off}V_{in} - T_{off}V_on + 2T_sV_o\delta n}{L_{lk}} \tag{2.53}$$

$$i_{lk}(t_5) = i_{lk}(t_0) + \frac{T_sV_{in} - 2T_s\delta V_{in} - T_sV_on + 2T_sV_o\delta n}{2L_{lk}} \tag{2.54}$$

$$i_{lk}(t_6) = i_{lk}(t_0) \tag{2.55}$$

  The average output power in the whole switching cycle is:

$$P_{out}(\delta)(CaseII) = \frac{nV_{in}V_o(4T_sT_{off}\delta - 4T_s^2\delta^2 + T_sT_{off} - 2T_{off}^2)}{2L_{lk}T_s} \tag{2.56}$$

- Case III:

  The current flowing through the leakage inductance (i_{lk}) at time points t_0 - t_6 is:

$$i_{lk}(t_0) = -\frac{2T_{on}V_{in} + 3T_sV_on - 4T_sV_o\delta n}{4L_{lk}} \tag{2.57}$$

$$i_{lk}(t_1) = i_{lk}(t_0) + \frac{T_sV_on}{2L_{lk}} - \frac{T_sV_o\delta n}{L_{lk}} \tag{2.58}$$

$$i_{lk}(t_2) = i_{lk}(t_0) + \frac{T_sV_on}{2L_{lk}} + \frac{T_{off}V_on}{L_{lk}} - \frac{2T_sV_o\delta n}{L_{lk}} \tag{2.59}$$

$$i_{lk}(t_3) = i_{lk}(t_0) + \frac{2T_sV_{in} - 2T_{off}V_{in} + 3T_sV_on - 4T_sV_o\delta n}{2L_{lk}} \tag{2.60}$$

$$i_{lk}(t_4) = i_{lk}(t_0) + \frac{T_sV_{in} - T_{off}V_{in} + T_sV_on - T_sV_o\delta n}{L_{lk}} \tag{2.61}$$

$$i_{lk}(t_5) = i_{lk}(t_0) + \frac{T_sV_{in} - T_{off}V_{in} + T_sV_on - T_{off}V_on}{L_{lk}} \tag{2.62}$$

$$i_{lk}(t_6) = i_{lk}(t_0) \tag{2.63}$$

  The average output power in the whole switching cycle is:

$$P_{out}(\delta)(CaseIII) = \frac{nV_{in}V_o(T_s - T_{off})(T_s + 2T_{off} - 4T_s\delta)}{2L_{lk}T_s} \tag{2.64}$$

- Case IV:

  The current flowing through the leakage inductance (i_{lk}) at time points t_0 - t_6 is:

$$i_{lk}(t_0) = -\frac{2T_{on}V_{in} + 3T_sV_on - 4T_sV_o\delta n}{4L_{lk}} \tag{2.65}$$

$$i_{lk}(t_1) = i_{lk}(t_0) + \frac{T_sV_on}{2L_{lk}} - \frac{T_{off}V_on}{L_{lk}} \tag{2.66}$$

$$i_{lk}(t_2) = i_{lk}(t_0) + \frac{-2T_{off}V_{in} + 2T_s\delta V_{in} + T_snV_o - 2\delta T_snV_o}{2L_{lk}} \tag{2.67}$$

$$i_{lk}(t_3) = i_{lk}(t_0) + \frac{2T_sV_{in} - 2T_{off}V_{in} + 3T_sV_on - 4T_sV_o\delta n}{2L_{lk}} \tag{2.68}$$

$$i_{lk}(t_4) = i_{lk}(t_0) + \frac{T_sV_{in} - T_{off}V_{in} + T_sV_on + T_{off}V_on - 2T_sV_o\delta n}{L_{lk}} \tag{2.69}$$

$$i_{lk}(t_5) = i_{lk}(t_0) + \frac{T_sV_{in} - T_s\delta V_{in} + T_sV_on - T_sV_o\delta n}{L_{lk}} \tag{2.70}$$

$$i_{lk}(t_6) = i_{lk}(t_0) \tag{2.71}$$

  The average output power in the whole switching cycle is:

$$P_{out}(\delta)(CaseIV) = \frac{nV_{in}V_o(4T_s^2\delta^2 - 4T_s^2\delta + T_s^2 - 4T_sT_{off}\delta + T_sT_{off} + 2T_{off}^2)}{2L_{lk}T_s} \tag{2.72}$$

- Case VI:

  The current flowing through the leakage inductance (i_{lk}) at time points t_0 - t_6 is:

$$i_{lk}(t_0) = -\frac{2T_{off}V_{in} - T_sV_on + 4T_sV_o\delta n}{4L_{lk}} \tag{2.73}$$

$$i_{lk}(t_1) = i_{lk}(t_0) + \frac{T_{off}(V_{in} + V_on)}{L_{lk}} \tag{2.74}$$

$$i_{lk}(t_2) = i_{lk}(t_0) + \frac{T_{off}V_{in} + T_sV_o\delta n}{L_{lk}} \tag{2.75}$$

$$i_{lk}(t_3) = i_{lk}(t_0) + \frac{2T_{off}V_{in} - T_sV_on + 4T_sV_o\delta n}{2L_{lk}} \tag{2.76}$$

$$i_{lk}(t_4) = i_{lk}(t_0) + \frac{-T_sV_on - 2T_{off}nV_o + 4T_sV_o\delta n}{2L_{lk}} \tag{2.77}$$

$$i_{lk}(t_5) = i_{lk}(t_0) + \frac{-T_sV_on + 2T_sV_o\delta n}{2L_{lk}} \tag{2.78}$$

$$i_{lk}(t_6) = i_{lk}(t_0) \tag{2.79}$$

  The average output power in the whole switching cycle is:

$$P_{out}(\delta)(CaseVI) = \frac{nV_{in}V_oT_{off}(T_s + 2T_{off} - 4T_s\delta)}{2L_{lk}T_s} \tag{2.80}$$

- Case VII:

  The current flowing through the leakage inductance (i_{lk}) at time points t_0 - t_6 is:

$$i_{lk}(t_0) = -\frac{2T_{off}V_{in} + 3T_sV_on - 4T_sV_o\delta n}{4L_{lk}} \tag{2.81}$$

$$i_{lk}(t_1) = i_{lk}(t_0) + \frac{-T_sV_{in} + 2\delta T_sV_{in} + T_sV_on - 2\delta T_snV_o}{2L_{lk}} \tag{2.82}$$

$$i_{lk}(t_2) = i_{lk}(t_0) + \frac{T_{off}V_{in} + T_sV_on + T_{off}V_on - 2\delta T_snV_o}{L_{lk}} \tag{2.83}$$

$$i_{lk}(t_3) = i_{lk}(t_0) + \frac{2T_{off}V_{in} + 3T_sV_on - 4T_sV_o\delta n}{2L_{lk}} \tag{2.84}$$

$$i_{lk}(t_4) = i_{lk}(t_0) + \frac{T_sV_{in} + 2T_{off}V_{in} - 2T_s\delta V_{in} + 2T_sV_on - 2T_sV_o\delta n}{2L_{lk}} \tag{2.85}$$

$$i_{lk}(t_5) = i_{lk}(t_0) + \frac{T_sV_on - 2T_{off}V_on}{2L_{lk}} \tag{2.86}$$

$$i_{lk}(t_6) = i_{lk}(t_0) \tag{2.87}$$

  The average output power in the whole switching cycle is:

$$P_{out}(\delta)(CaseVII) = \frac{nV_{in}V_o(4T_s^2\delta^2 - 4T_s^2\delta + T_s^2 - 4T_sT_{off}\delta + T_sT_{off} + 2T_{off}^2)}{2L_{lk}T_s} \tag{2.88}$$

- Case VIII:

  The current flowing through the leakage inductance (i_{lk}) at time points t_0 - t_6 is:

$$i_{lk}(t_0) = -\frac{2T_{off}V_{in} + 3T_sV_on - 4T_sV_o\delta n}{4L_{lk}} \tag{2.89}$$

$$i_{lk}(t_1) = i_{lk}(t_0) + \frac{T_{off}(V_{in} - V_on)}{L_{lk}} \tag{2.90}$$

$$i_{lk}(t_2) = i_{lk}(t_0) + \frac{2T_{off}V_{in} + T_sV_on - 2\delta T_snV_o}{2L_{lk}} \tag{2.91}$$

$$i_{lk}(t_3) = i_{lk}(t_0) + \frac{2T_{off}V_{in} + 3T_sV_on - 4T_sV_o\delta n}{2L_{lk}} \tag{2.92}$$

$$i_{lk}(t_4) = i_{lk}(t_0) + \frac{3T_sV_on + 2T_{off}V_on - 4\delta T_snV_o}{2L_{lk}} \tag{2.93}$$

$$i_{lk}(t_5) = i_{lk}(t_0) + \frac{T_sV_on - \delta T_snV_o}{L_{lk}} \tag{2.94}$$

$$i_{lk}(t_6) = i_{lk}(t_0) \tag{2.95}$$

  The average output power in the whole switching cycle is:

$$P_{out}(\delta)(CaseVIII) = -\frac{nV_{in}V_oT_{off}(3T_s + 2T_{off} - 4T_s\delta)}{2L_{lk}T_s} \tag{2.96}$$

According to the Figure 2.7, it can be seen that the relationship of the phase shift between the gate signals of S1 and S5 (δ) and the phase shift between the output voltages (u_{ab} and u_{cd}) of the primary and secondary side bridges (Φ) is:

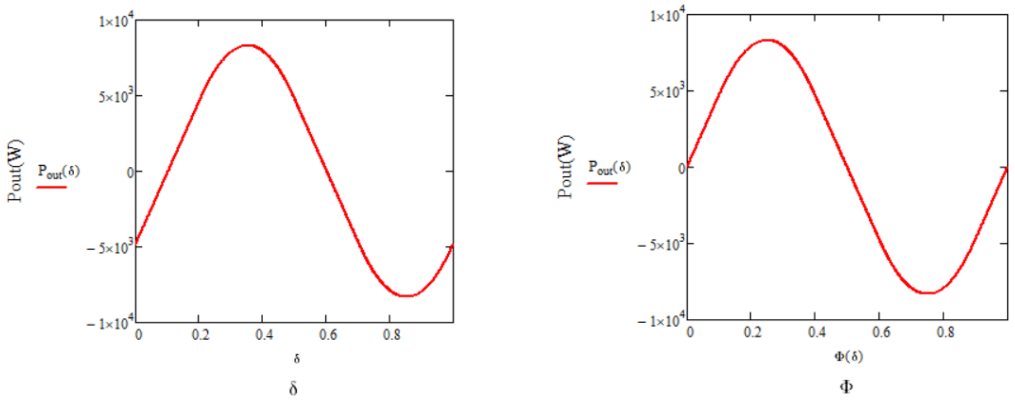
$$\Phi = \delta - \frac{1}{4} + \frac{1}{2}D \tag{2.97}$$

Using the Mathcad programming to plot the power curve of the dual boost integrated DAB converter according to the deduced equations. The results based on different phase shifts when $D < 0.5$ (Case I - Case IV) and when $D > 0.5$ (Case V - Case VIII) are shown in the Figure 2.10 and the Figure 2.11, separately.

The power curves when $D < 0.5$ are plotted when the DC bus voltage is $666.6V$, the PV voltage is $470V$ and the EV battery voltage is $333.3V$ and power curves when $D > 0.5$ are plotted when the DC bus voltage is $666.6V$, the PV voltage is $220V$ and the EV battery voltage is $333.3V$. When the duty cycle $D = 0.5$ (PV voltage is $333.3V$), the maximum output power can be reached. The power curves based on different phase shifts when $D = 0.5$ are shown in the Figure 2.12.

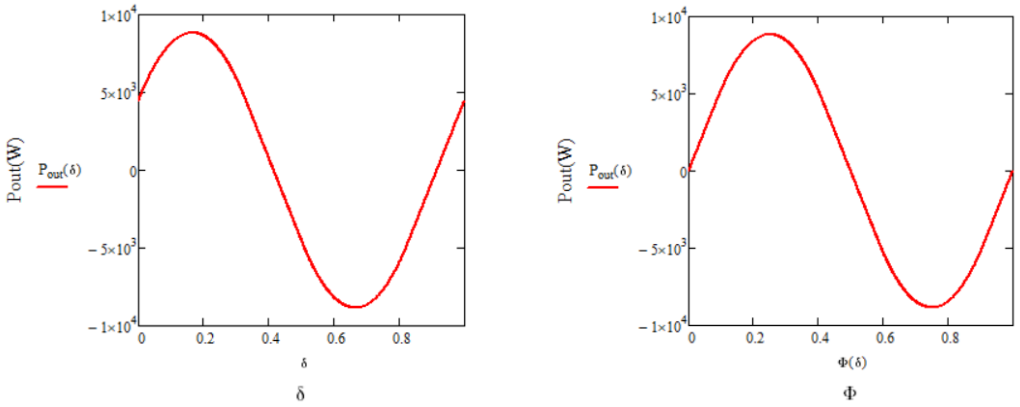
It can be seen from the output power curves that the output power is not only related to the input voltage, output voltage and phase shift but also related to the PV voltage since it will influence the duty cycle of the primary side switches. The maximum output power is in the Case II when $D \leq 0.5$ and in the Case V when $D > 0.5$. The maximum output power point can be found by calculating the derivative of the output power equations of Case II and Case V with respect to δ. The 3D plots of the maximum output power with different input and output voltages in several different cases in which the duty cycles of the S2 and S4 are different are shown in the Figure 2.13.

In the Figure 2.13, $P_{out-max}$ is the maximum output power with different input and output voltages and P_{out} (which is the blue plane) is the $10kW$ plane. It can be seen that the maximum output power increases when the absolute value of $D - 0.5$ decreases if the input and output voltages are the same.



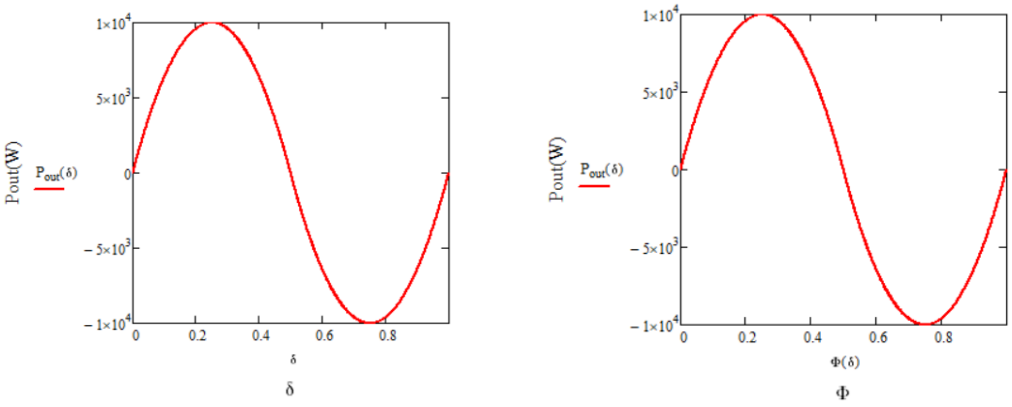
(a) The power curve based on phase shift δ when $D < 0.5$ **(b)** The power curve based on phase shift Φ when $D < 0.5$

Figure 2.10: The power curves based on different phase shifts when $D < 0.5$



(a) The power curve based on phase shift δ when $D > 0.5$ **(b)** The power curve based on phase shift Φ when $D > 0.5$

Figure 2.11: The power curves based on different phase shifts when $D > 0.5$



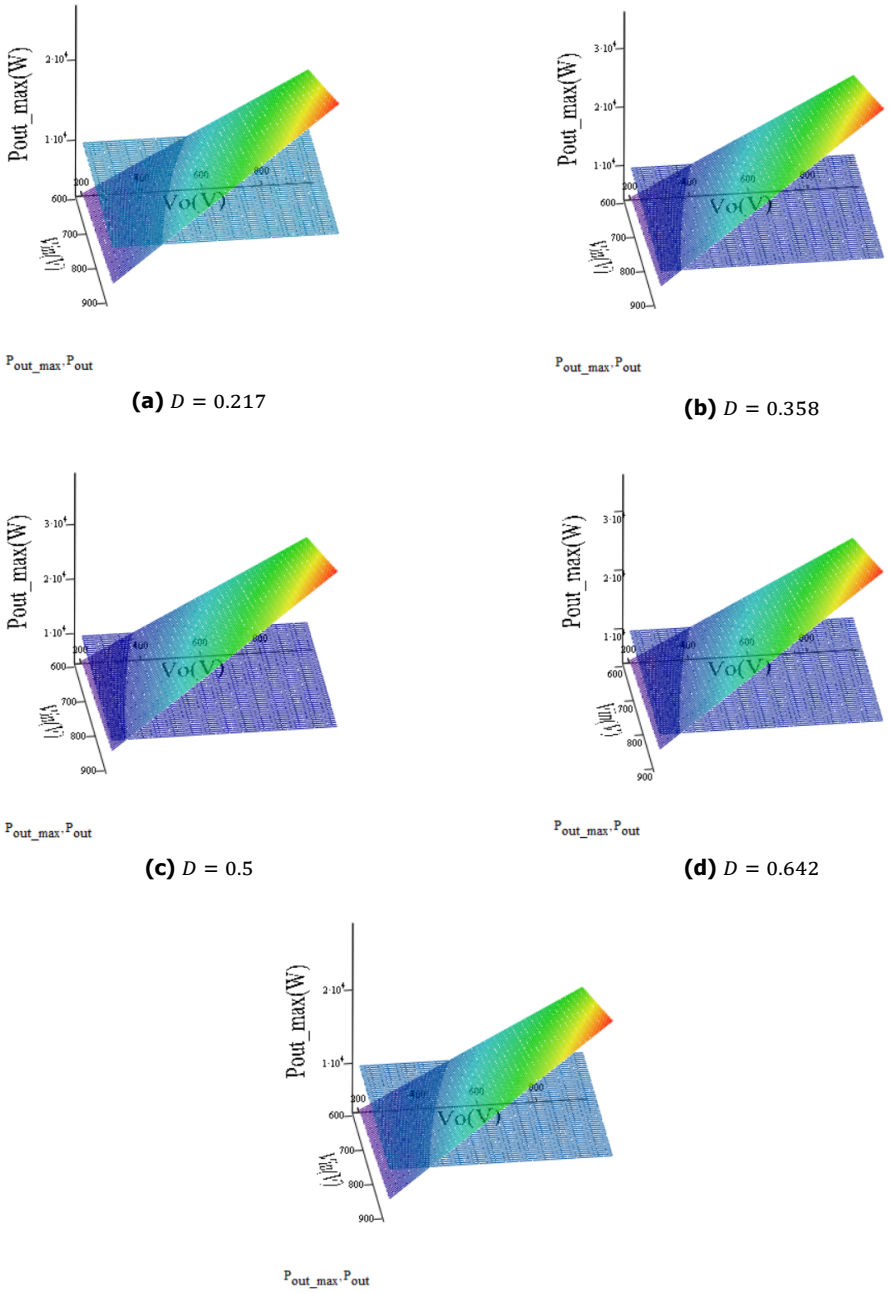
(a) The power curve based on phase shift δ when $D = 0.5$ **(b)** The power curve based on phase shift Φ when $D = 0.5$

Figure 2.12: The power curves based on different phase shifts when $D = 0.5$

2.5. Control strategy

2.5.1. Power modes

The dual boost integrated DAB converter has six power modes which are defined according to the power level at the different ports.



(a) $D = 0.217$ **(b)** $D = 0.358$

(c) $D = 0.5$ **(d)** $D = 0.642$

(e) $D = 0.756$

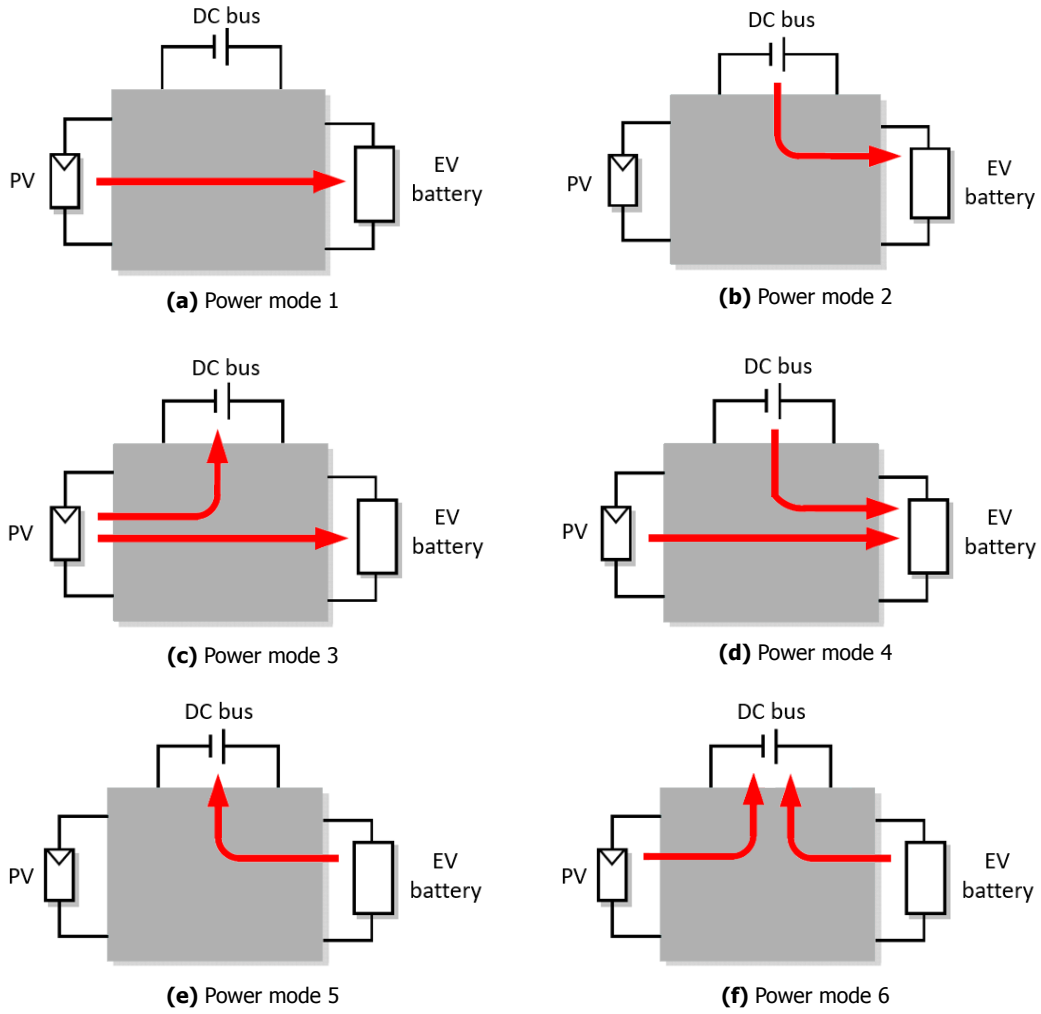
Figure 2.13: The 3D plots of the maximum output power with different input and output voltages

- Power mode 1: the power is transferred from the PV port to the output port when the illumination is strong enough to produce the same power which the EV battery required.
- Power mode 2: the power is transferred from the DC bus port to the output port when the power at the PV port is 0 since there is no illumination.
- Power mode 3: the power is transferred to both the DC bus port and the output port from the PV port when the power produced by the PV panel is larger than the power required by the EV battery.
- Power mode 4: the power is transferred from both the DC bus port and the PV port to the output

port when the power produced by the PV panel is not enough to supply the power required by the EV battery.

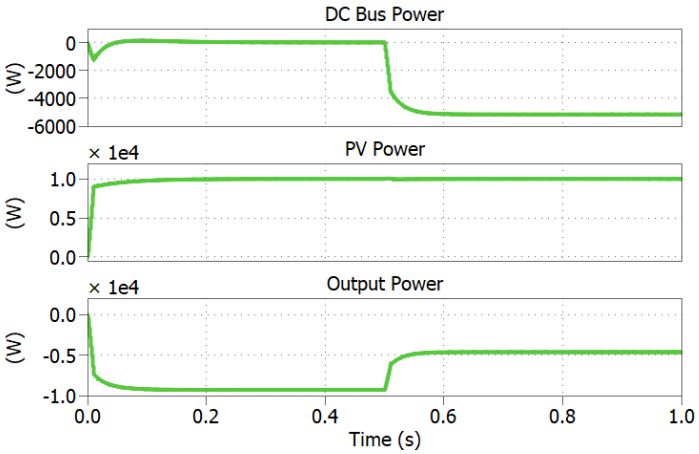
- Power mode 5: the power can also be transferred from the output port to the DC bus port when the EV battery has enough power or during the peak hours of the grid.
- Power mode 6: the power can be transferred from the output port and the PV port to the DC bus port when the grid needs more power.

The six power modes are demonstrated in the Figure 2.14. The simulation results of the switch between the different power modes are shown in the Figure 2.15. In the Figure 2.15, the positive average power means the power is transferred from this port and the negative average power means the power is transferred to this port. In the Figure 2.15a, the PV power is $10kW$, the load is also $10kW$ at the beginning, so the power is transferred from the PV port to the output port, which is power mode 1. The output power is a little bit less than $10kW$ since there is a small part of power is circulating in the circuit. The load is reduced to $5kW$ at $0.5s$, so the power is transferred from the PV port to both the output port and the DC bus port since the PV power is more than the power which is needed by the EV. In the Figure 2.15b, the PV power is $10kW$ at the beginning and the load is also $10kW$, so the power is transferred from the PV port to the output port. However, the PV power is reduced to $5kW$ at $0.5s$ due to the lack of illumination, so the EV battery is charged by both the PV power and the power from the grid, which is power mode 4. In the Figure 2.15c, the EV battery is charged by the PV power at the beginning and it starts to discharge after $0.5s$. The power discharged from the EV battery and produced by the PV panel is transferred to the grid during the peak hours.

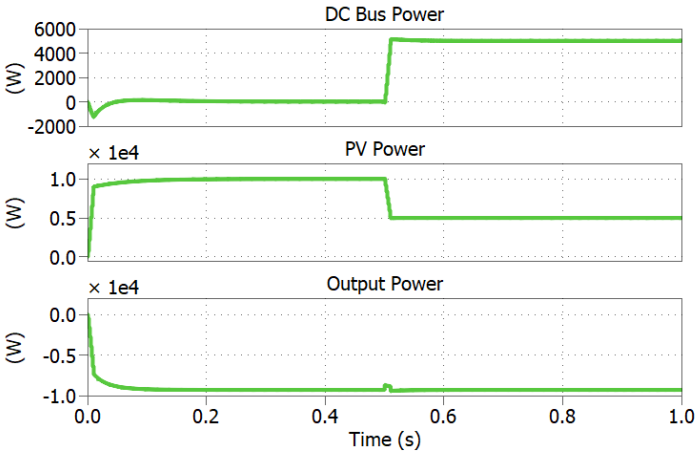


(a) Power mode 1 **(b)** Power mode 2 **(c)** Power mode 3 **(d)** Power mode 4 **(e)** Power mode 5 **(f)** Power mode 6

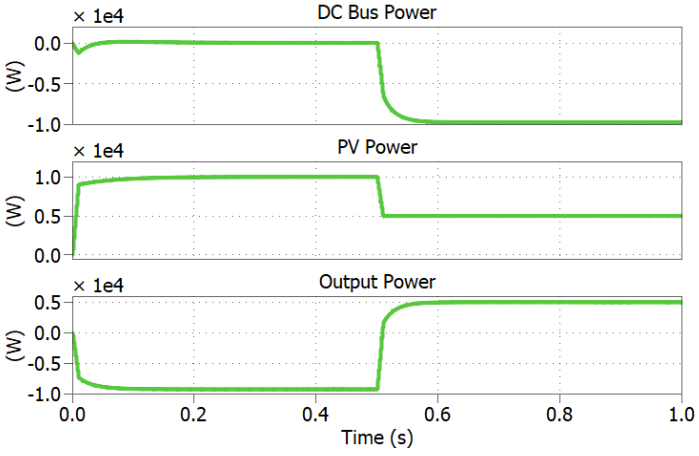
Figure 2.14: The power modes of the dual boost integrated DAB converter



(a) The switch from power mode 1 to power mode 3



(b) The switch from power mode 1 to power mode 4



(c) The switch from power mode 1 to power mode 6

Figure 2.15: The simulation results of the switch between the different power modes

2.5.2. Control structure

The charging curve of the EV battery is shown in the Figure 2.16. Generally, only the constant current charging stage (t_1 - t_2) will be used when charge the battery of the EV because of the following two reasons:

- Fully charge the battery will over stress the battery and reduce its life time.

- The EV battery can be charged to 80% of its capacity in a short time [40].

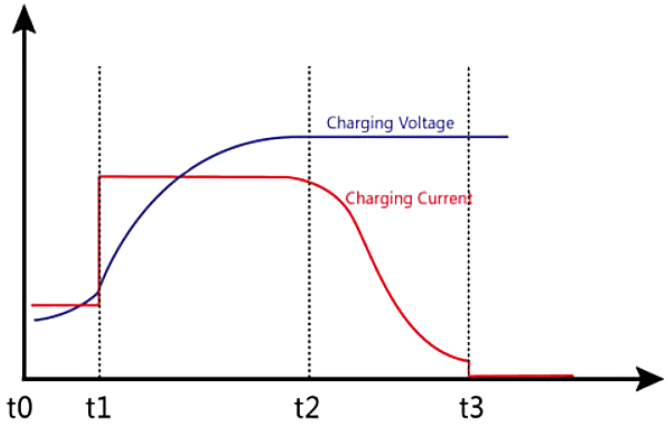


Figure 2.16: The charging curve of the EV battery

The control of the whole converter has two different cases:

- The first case is when there is some illumination from the sun so the PV power is not zero and the duty cycle of the primary side switches is controlled by the PV current which is the sum of the current flowing through the two boost inductors. The control structure of this case is shown in the Figure 2.17, which is aimed to manage the power flow between the three ports and regulate the output current and output voltage of the dual boost integrated DAB converter.
- The second case is when there is no illumination from the sun. The two interleaved boost converters have a start-up voltage, the start-up voltage is set as $200V$ according to the information in the data sheet of the ABB's $10kW$ PV inverter [38], the PV port of the dual boost integrated DAB converter will be disconnected from the whole converter when the PV voltage is less than $200V$ and the duty cycle of the primary side switches is kept as 0.5 in order to get the maximum transferred power in principle and the real power which is transferred to the secondary side is still decided by the phase shift between the primary side and secondary side, which is the same with the first case.

In the Figure 2.17, the PV current and PV voltage are sensed at the PV port to implement the MPPT of the PV panels. The duty cycle D of S2 and S4 in Figure 2.4 is decided by the voltage at the PV port and the input port and regulated by controlling the PV current which is the sum of the current flowing through the two boost inductors. And this duty cycle is produced by the PWM method. The power flow and the output current are controlled by the phase shift δ between the gate signals of S1 and S5 in the Figure 2.4. The duty cycles of the secondary side switches are always 0.5 while the S5 and S8 as well as the S6 and S7 are conducted as switch pairs. The maximum output current is $30A$ which is decided by the design requirement of ABB's EV charger, once the output current is larger than $30A$, the phase shift should be adjusted to limit the output current. Hence, when the voltage is less than $333.3V$, the output power cannot reach $10kW$ because of the current limitation.

The whole control loop in the simulation is composed of two subsystems which are shown in the Figure 2.18. It can be seen from the Figure 2.19a that there is another subsystem (PrimarySideControl) inside the primary side subsystem, which is used to realize the control of the duty cycle of the primary side switches in the first control case and the outside part is used to generate the PWM signals of the primary side switches in the second case. The structure of the PrimarySideControl block is shown in the Figure 2.19b and it adjusts the duty cycle of the primary side switches according to the error between the measured boost inductor current and the reference boost inductor current. And there are three subsystems in the secondary side subsystem which is shown in the Figure 2.20. The GeneratePhaseShift subsystem is a PID controller used to generate the phase shift between the primary and secondary side according to the error between the measured output current and the reference output current. The MaxMinδ including a C-Script block which is used to calculate the maximum and minimum phase shift

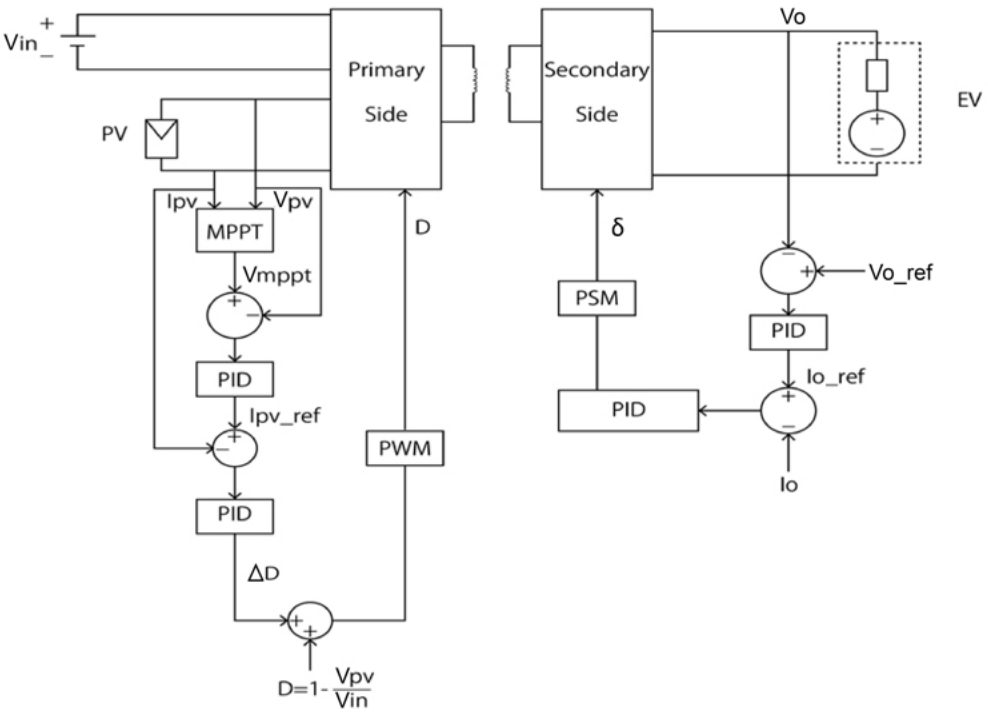


Figure 2.17: The control structure of the dual boost integrated DAB converter

according to the equations deduced in Mathcad to avoid that the converter works at the phase shift which is already out of the phase shift range with which the output power is from maximum negative value to the maximum positive value. The third subsystem (PhaseShiftModulation) is used to generate the PWM signals of the secondary side switches according to the phase shift got from the last step. Besides, the DC blocking capacitor voltage control is also included in this subsystem. The effectiveness of the built control loop in the simulation model can be verified by the simulation result which is shown in the Figure 2.21. It can be seen from the Figure 2.21 that the output current can reach the reference value in a short time.

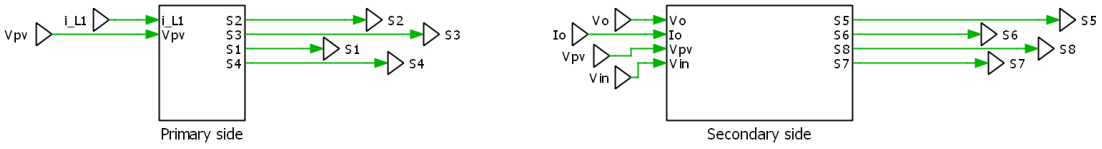
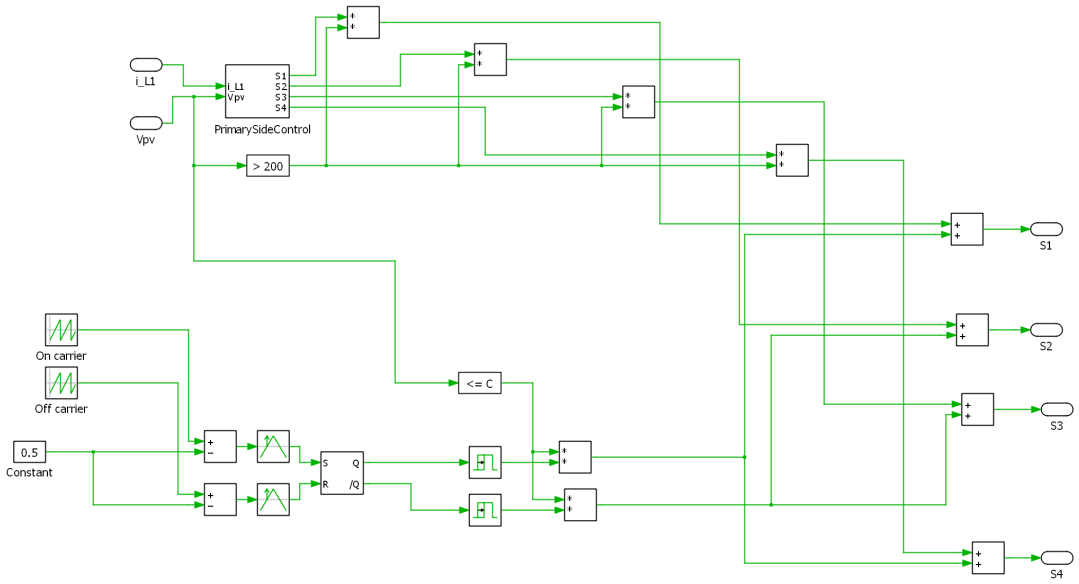


Figure 2.18: The whole control loop in the PLECS

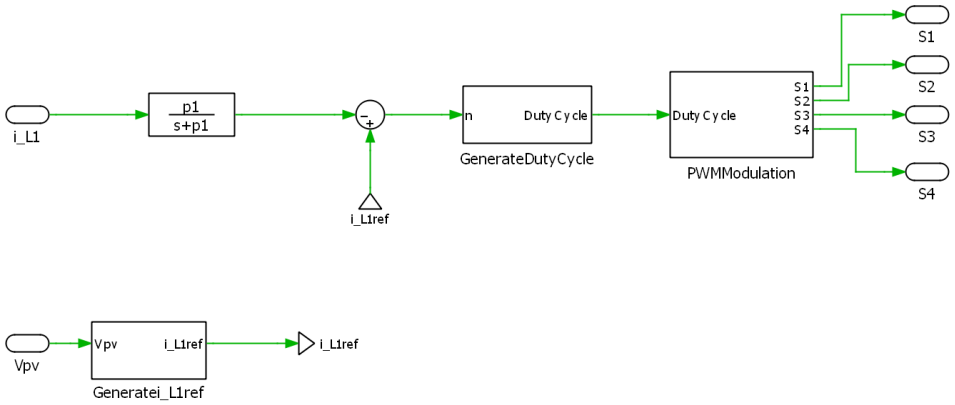
2.6. Summary

The contents about the specifications of the design, the parameter design of the dual boost integrated DAB converter, the working principle, the output power characteristic and the control strategy of this converter are presented in this chapter. Among all the contents presented in this chapter, the followings are important and need to be emphasized:

- The dual boost integrated DAB converter has the bidirectional capability and the interleaved structure in the primary side can significantly reduce the ripple of the PV current, which is suitable for the PV integrated bidirectional EV charging system.
- All the equations related to the working principle and the output power characteristics of the dual



(a) The primary side block



(b) The PrimarySideControl block

Figure 2.19: The primary side subsystem

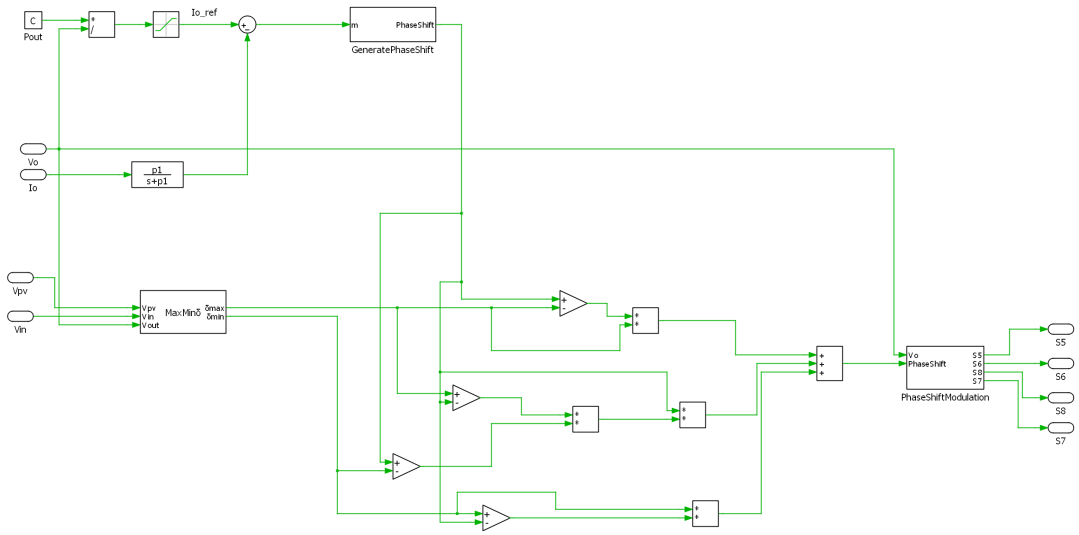


Figure 2.20: The secondary side subsystem

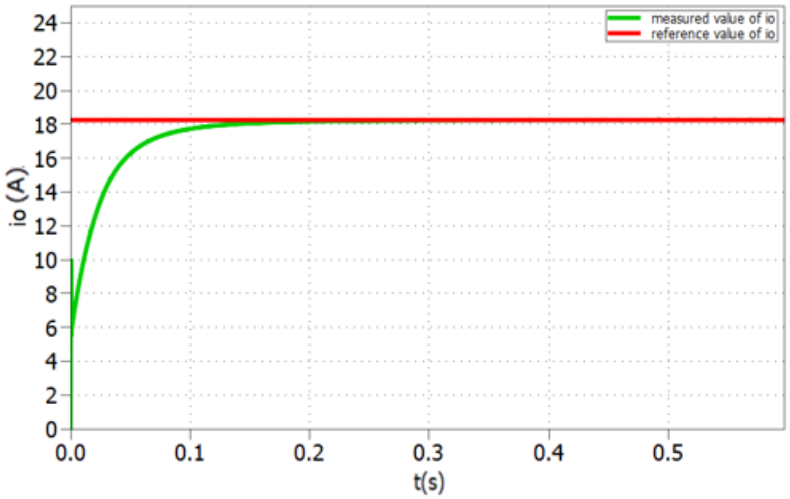


Figure 2.21: Verification of the control loop

boost integrated DAB converter are deduced in Mathcad. The deduced equations are verified by comparing the waveforms of the important current and voltage as well as the output power got from the Mathcad equations and the PLECS simulation. The built Mathcad programming is not only suitable for this master thesis project but can be also used for other design of the dual boost integrated DAB converter since all the key parameters (DC bus voltage, PV voltage, EV battery voltage, switching frequency, leakage inductance, turn ratio of the transformer and the inductance of the two boost inductors) are the input values of the programming. The customized design can be done by changing the input values in this programming.

- The power modes and the control strategy of the dual boost integrated DAB converter are also described in this chapter. The closed loop control is built in PLECS and the simulation results can verify that the effectiveness of the designed control loop.

After the basic working principle and the control strategy of the dual boost integrated DAB converter are studied in this chapter, the further analysis in terms of the soft switching region, the circulating power and the loss breakdown of it is proceeded in the next chapter to evaluate the performance of this converter.

3

Power loss modeling and analysis

3.1. Zero voltage switching characteristics

The dual boost integrated DAB converter in this project is a DAB converter from the DC bus port to the output port. One of the main disadvantages of the DAB converter is when the output voltage is not matched with the input voltage or when the load is too light, the zero voltage switching (ZVS) range of the switches will be very small. However, due to the interleaved boost converters at the primary side, the ZVS characteristics of this dual boost integrated DAB converter are different from the traditional DAB converter.

Generally, the prerequisite of the ZVS of the switches is that the antiparallel diode of the switch can conduct before the gate signal is given to the switch. The conducting of the antiparallel diode can clamp the voltage on the switch to zero to make sure that the switch has ZVS.

As for the dual boost integrated DAB converter with the PWM plus the phase shift modulation, the two switches on the same leg conduct complementarily. In order to realize the ZVS of the switch which is going to conduct, the current flowing through the switch which is on the same leg and going to be turned off should be larger than zero, so when this switch is turned off, the current on it starts to flow through the antiparallel diode of the switch which is going to be turned on. The current flowing through the switches on the secondary side of the dual boost integrated DAB converter is only related to the current flowing through the leakage inductance, so the analysis of the ZVS is relatively simple. The current flowing through the switches on the primary side is not only related to the current flowing through the leakage inductance but also related to the current flowing through the boost inductors (i_{L1} and i_{L2}), the analysis of the ZVS is more complex.

3.1.1. ZVS characteristics of the secondary side switches

Take Case V as an example to analysis the ZVS characteristics of the secondary side switches of the dual boost integrated DAB converter.

According to the gate signals and the key waveforms of Case V which are shown in the Figure 2.7, the ZVS conditions for the secondary side switches are:

- For S5 and S8:

$$i_{lk}(t_1) > 0 \tag{3.1}$$

- For S6 and S7:

$$i_{lk}(t_4) < 0 \tag{3.2}$$

Due to the symmetry of the waveform of i_{lk},

$$i_{lk}(t_4) = -i_{lk}(t_1) \tag{3.3}$$

Hence, the ZVS condition of the secondary side switches in Case V is:

$$i_{lk}(t_1) > 0 \tag{3.4}$$

$i_{lk}(t_1)$ can be calculated according to the equation 2.15 and equation 2.26, the final result of the ZVS condition of the secondary side switches in Case V is:

$$(4\delta + 2D + G - 2) > 0 \tag{3.5}$$

where δ is the phase shift between the gate signals of S1 and S5, D is the duty cycle of the switches S2 and S4 and G is the voltage gain which is equal to $\frac{nV_o}{V_{in}}$.

By using the same method, the ZVS conditions of the secondary side switches in all cases can be derived and the results are shown in the Table 3.1.

Table 3.1: The ZVS conditions of the secondary side switches in different cases

Case	ZVS Condition	Case	ZVS Condition
I	$(G - 2D) > 0$	V	$(4\delta + 2D + G - 2) > 0$
II	$(4\delta + 2D + G - 2) > 0$	VI	$(2 - 2D + G) > 0$
III	$(2D + G) > 0$	VII	$(4 - 4\delta + G - 2D) > 0$
IV	$(4 - 4\delta + G - 2D) > 0$	VIII	$(2D - 2 + G) > 0$

Since the range of the input voltage (V_{in}) is $600V - 900V$ and the range of the output voltage(V_o) is $200V - 950V$, the range of the voltage gain (G) is $0.667 - 2.111$. The ZVS conditions of the secondary side switches in all cases can be simplified according to the range of the duty cycle (D) and the range of the phase shift (δ) in different cases. The range of the duty cycle (D) and the range of the phase shift (δ) in different cases are shown in the Table 3.2. The simplified ZVS conditions of the secondary side switches in different cases are shown in the Table 3.3.

Table 3.2: The range of the duty cycle (D) and the range of the phase shift (δ) in different cases

Case	Range of D	Range of δ	Case	Range of D	Range of δ
I	$D \leq 0.5$	$0 \leq \delta < \frac{1}{2} - D$	V	$D > 0.5$	$0 \leq \delta < 1 - D$
II	$D \leq 0.5$	$\frac{1}{2} - D \leq \delta < \frac{1}{2}$	VI	$D > 0.5$	$1 - D \leq \delta < \frac{1}{2}$
III	$D \leq 0.5$	$\frac{1}{2} \leq \delta < 1 - D$	VII	$D > 0.5$	$\frac{1}{2} \leq \delta < \frac{3}{2} - D$
IV	$D \leq 0.5$	$1 - D \leq \delta \leq 1$	VIII	$D > 0.5$	$\frac{3}{2} - D \leq \delta \leq 1$

Table 3.3: The simplified ZVS conditions of the secondary side switches in different cases

Case	ZVS Condition	Case	ZVS Condition
I	$G > 1$	V	$G > 0$
II	$G > 1$	VI	$G > 0$
III	$G > 0$	VII	$G > 1$
IV	$G > 0$	VIII	$G > 1$

According to the Table 3.3, the summaries of the ZVS conditions of the secondary side switches are:

- When the duty cycle (D) of the switches S2 and S4 is less than 0.5 or equal to 0.5, the ZVS of the secondary side switches of the dual boost integrated DAB converter can be realized when the voltage gain G is larger than 1 when the phase shift δ is less than 0.5. When the phase shift δ is larger than 0.5 or equal to 0.5, the ZVS can be realized when the voltage gain G is larger than 0, which means the ZVS of the secondary side switches can be realized in the whole voltage gain range in this project when D is less than 0.5 or equal to 0.5 and the phase shift δ is larger than 0.5 or equal to 0.5.
- When the duty cycle (D) of the switches S2 and S4 is larger than 0.5, the ZVS of the secondary side switches of the dual boost integrated DAB converter can be realized in the whole voltage gain range when the phase shift δ is less than 0.5. When the phase shift δ is larger than 0.5 or equal to 0.5, the ZVS of the secondary side switches can be realized when the voltage gain G is larger than 1.

3.1.2. ZVS characteristics of the primary side switches

Take Case V as an example to analysis the ZVS characteristics of the primary side switches of the dual boost integrated DAB converter.

The current flowing through the switches in the primary side of the dual boost integrated DAB converter is not only related to the current flowing through the leakage inductance but also related to the current flowing through the boost inductors (i_{L1} and i_{L2}).

According to the gate signals and the key waveforms of Case V which are shown in the Figure 2.7, the ZVS conditions for the primary side switches are:

- For S1:

$$i_{L1}(t_0) - i_{lk}(t_0) > 0 \tag{3.6}$$

- For S2:

$$i_{L1}(t_2) - i_{lk}(t_2) < 0 \tag{3.7}$$

- For S3:

$$i_{L2}(t_3) + i_{lk}(t_3) > 0 \tag{3.8}$$

- For S4:

$$i_{L2}(t_5) + i_{lk}(t_5) < 0 \tag{3.9}$$

Due to the symmetry of the waveform of i_{lk},

$$i_{lk}(t_3) = -i_{lk}(t_0) \tag{3.10}$$

$$i_{lk}(t_5) = -i_{lk}(t_2) \tag{3.11}$$

Since the switches in the two boost converters in the primary side have the same duty cycle and the two boost inductors have the same inductance, $I_{L1_{max}} = I_{L2_{max}}$ and $I_{L1_{min}} = I_{L2_{min}}$. According to the waveforms of i_{L1} and i_{L2} in the Figure 2.7,

$$i_{L1}(t_0) = i_{L2}(t_3) = I_{L1_{max}} \tag{3.12}$$

$$i_{L1}(t_2) = i_{L2}(t_5) = I_{L1_{min}} \tag{3.13}$$

Hence, the ZVS condition of S3 is the same with that of the S1 and the ZVS condition of S4 is the same with that of the S2.

The average values of i_{L1} and i_{L2} are the same and equal to the half of the average value of the PV current. Hence, the maximum and minimum boost inductor current ($I_{L1_{max}}$ and $I_{L1_{min}}$) are:

$$I_{L1_{max}} = \frac{P_{pv}}{2V_{pv}} + \frac{1}{2} * \frac{V_{pv}}{L_1} * T_{on} \tag{3.14}$$

$$I_{L1_{min}} = \frac{P_{pv}}{2V_{pv}} - \frac{1}{2} * \frac{V_{pv}}{L_1} * T_{on} \tag{3.15}$$

The current flowing through the leakage inductance (i_{lk}) at different time point can be replaced by the equations deduced in the Section 2.4. Then, the ZVS conditions of the primary side switches can be represented as:

- For S1 and S3:

$$P_{pv} > 2V_{pv} i_{lk}(t_0) - V_{pv}^2 D * \frac{T_s}{L_1} \tag{3.16}$$

- For S2 and S4:

$$P_{pv} < -2V_{pv} i_{lk}(t_0) + V_{pv}^2 D * \frac{T_s}{L_1} + 2(-\frac{1}{2} + D) n V_{pv} V_o * \frac{T_s}{L_{lk}} \tag{3.17}$$

By using the same method, the ZVS conditions of the primary side switches of the dual boost integrated DAB converter in other cases can be represented as:

- Case I

  For S1 and S3:

$$P_{pv} > 2V_{pv}i_{lk}(t_0) - V_{pv}^2 D * \frac{T_s}{L_1} \tag{3.18}$$

  For S2 and S4:

$$P_{pv} < -2V_{pv}i_{lk}(t_0) + V_{pv}^2 D * \frac{T_s}{L_1} + (1 - 2D - 4\delta)nV_{pv}V_o * \frac{T_s}{L_{lk}} \tag{3.19}$$

- Case II

  For S1 and S3:

$$P_{pv} > 2V_{pv}i_{lk}(t_0) - V_{pv}^2 D * \frac{T_s}{L_1} \tag{3.20}$$

  For S2 and S4:

$$P_{pv} < -2V_{pv}i_{lk}(t_0) + V_{pv}^2 D * \frac{T_s}{L_1} + 2(-\frac{1}{2} + D)nV_{pv}V_o * \frac{T_s}{L_{lk}} \tag{3.21}$$

- Case III

  For S1 and S3:

$$P_{pv} > 2V_{pv}i_{lk}(t_0) - V_{pv}^2 D * \frac{T_s}{L_1} \tag{3.22}$$

  For S2 and S4:

$$P_{pv} < -2V_{pv}i_{lk}(t_0) + V_{pv}^2 D * \frac{T_s}{L_1} + (-3 + 2D + 4\delta)nV_{pv}V_o * \frac{T_s}{L_{lk}} \tag{3.23}$$

- Case IV

  For S1 and S3:

$$P_{pv} > 2V_{pv}i_{lk}(t_0) - V_{pv}^2 D * \frac{T_s}{L_1} \tag{3.24}$$

  For S2 and S4:

$$P_{pv} < -2V_{pv}i_{lk}(t_0) + V_{pv}^2 D * \frac{T_s}{L_1} + (1 - 2D)nV_{pv}V_o * \frac{T_s}{L_{lk}} \tag{3.25}$$

- Case VI

  For S1 and S3:

$$P_{pv} > 2V_{pv}i_{lk}(t_0) - V_{pv}^2 D * \frac{T_s}{L_1} \tag{3.26}$$

  For S2 and S4:

$$P_{pv} < 2V_{pv}i_{lk}(t_0) + V_{pv}^2 D * \frac{T_s}{L_1} - [2V_{pv}(D - 1)(V_{in} + n * V_o)] * \frac{T_s}{L_{lk}} \tag{3.27}$$

- Case VII

  For S1 and S3:

$$P_{pv} > 2V_{pv}i_{lk}(t_0) - V_{pv}^2 D * \frac{T_s}{L_1} \tag{3.28}$$

  For S2 and S4:

$$P_{pv} < -2V_{pv}i_{lk}(t_0) + V_{pv}^2 D * \frac{T_s}{L_1} + (1 - 2D)nV_{pv}V_o * \frac{T_s}{L_{lk}} \tag{3.29}$$

- Case VIII

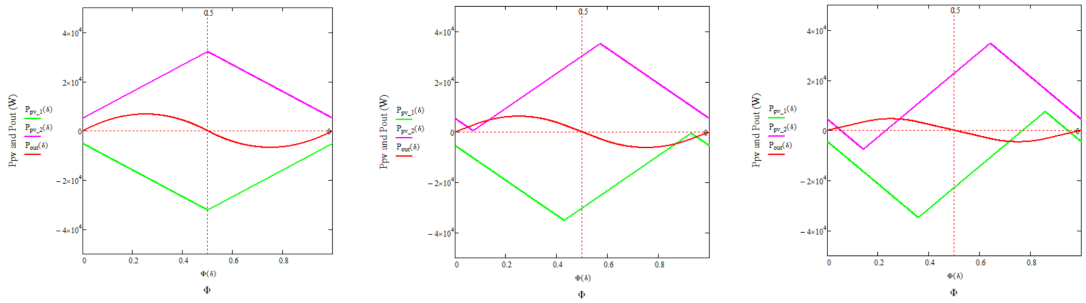
  For S1 and S3:

$$P_{pv} > 2V_{pv}i_{lk}(t_0) - V_{pv}^2 D * \frac{T_s}{L_1} \tag{3.30}$$

  For S2 and S4:

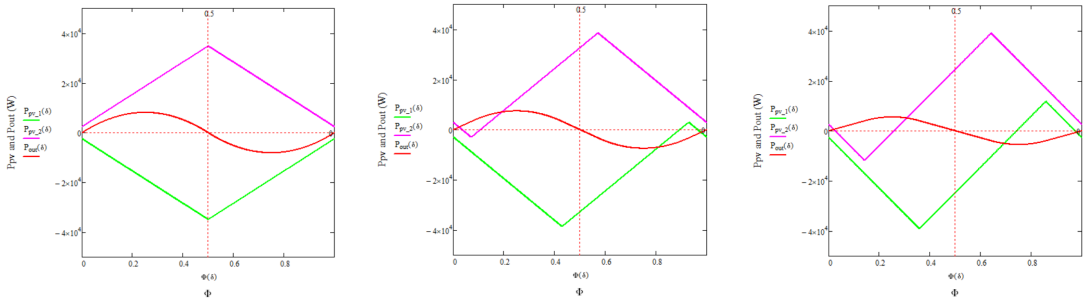
$$P_{pv} < 2V_{pv}i_{lk}(t_0) + V_{pv}^2 D * \frac{T_s}{L_1} - [2V_{pv}(D-1)(V_{in} - nV_o)] * \frac{T_s}{L_{lk}} \tag{3.31}$$

According to the ZVS regions of the primary side switches and the output power equations deduced in Section 2.4, the maps of the ZVS regions of the primary side switches of the dual boost integrated DAB converter with the output power can be obtained. The maps of Case I - Case IV ($D \leq 0.5$) when the voltage gain G is less than 1, equal to 1 and larger than 1 are shown in the Figure 3.1, Figure 3.2 and Figure 3.3, respectively. The three subfigures in each figure are plotted by changing the PV voltage, so the duty cycle D is changed.



(a) $D = 0.5$ **(b)** $D = 0.358$ **(c)** $D = 0.217$

Figure 3.1: The ZVS region with the output power when $G < 1$ ($D \leq 0.5$)



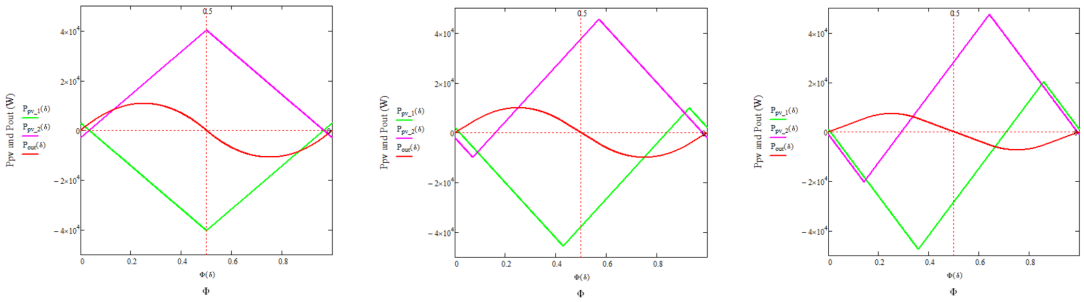
(a) $D = 0.5$ **(b)** $D = 0.358$ **(c)** $D = 0.217$

Figure 3.2: The ZVS region with the output power when $G = 1$ ($D \leq 0.5$)

The maps of Case V - Case VIII ($D > 0.5$) when the voltage gain G is less than 1, equal to 1 and larger than 1 are shown in the Figure 3.4, Figure 3.5 and Figure 3.6, respectively.

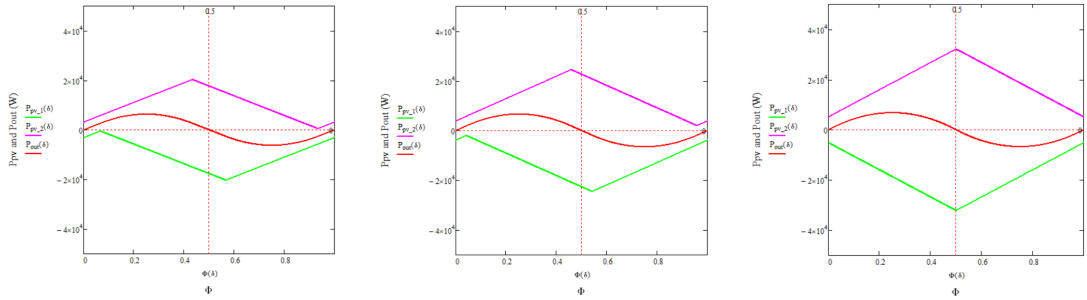
In the Figure 3.1 - Figure 3.6, the green line is the boundary of the ZVS region of S1 and S3, the purple line is the boundary of the ZVS region of S2 and S4 and the red line is the output power curve. The following conclusions can be summarized from the Figure 3.1 - Figure 3.6:

- The ZVS region of the primary side switches is increasing when the duty cycle D of S2 and S4 is approaching 0.5.



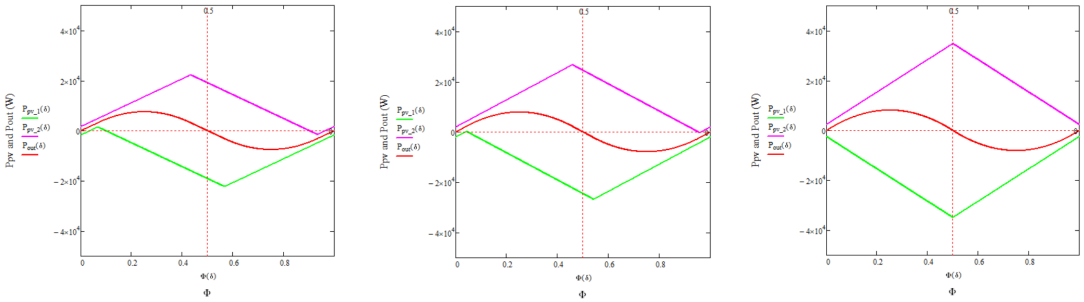
(a) $D = 0.5$ **(b)** $D = 0.358$ **(c)** $D = 0.217$

Figure 3.3: The ZVS region with the output power when $G > 1$ ($D \leq 0.5$)



(a) $D = 0.633$ **(b)** $D = 0.583$ **(c)** $D = 0.5$

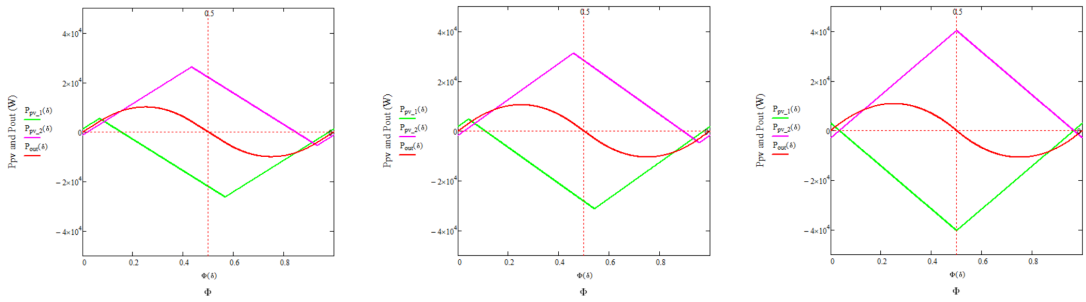
Figure 3.4: The ZVS region with the output power when $G < 1$ ($D > 0.5$)



(a) $D = 0.633$ **(b)** $D = 0.583$ **(c)** $D = 0.5$

Figure 3.5: The ZVS region with the output power when $G = 1$ ($D > 0.5$)

- The ZVS region of the primary side switches increases when the voltage gain G decreases. However, it can be seen from the Table 3.3, the ZVS of the secondary side switches will be more difficult to realize when G decreases.
- The ZVS of the primary side switches will be easier to realize when the phase shift Φ is approaching 0.5.
- In the charging mode ($\Phi \leq 0.5$), the ZVS of the S1 and S3 is easier to be realized compared with that of S2 and S4. In the discharging mode ($\Phi > 0.5$), the ZVS of the S2 and S4 is easier to be realized compared with that of S1 and S3.



(a) $D = 0.633$ **(b)** $D = 0.583$ **(c)** $D = 0.5$

Figure 3.6: The ZVS region with the output power when $G > 1$ ($D > 0.5$)

3.2. Circulating power analysis

When the power is transferred from the primary side to the secondary side of the dual boost integrated DAB converter, there may be a period when the direction of the current flowing through the leakage inductance (i_{lk}) and the direction of the primary side output voltage (u_{ab}) are opposite, as highlighted with orange in the Figure 3.7. Then the power is transferred to the opposite direction of the required direction. This power is called the circulating power. The circulating power is not useful to the output power and it will increase the current stress of the switches and the losses in the whole converter, so the efficiency will be decreased. When the output power of the dual boost integrated DAB converter is fixed, in order to compensate the circulating power, the converter needs to produce more power and the voltage is fixed, so the current needs to be increased. Hence, the conducting losses of the switches and the core losses of the transformer will be increased. The circulating power will also exist in the discharging period when the power is transferred from the secondary side to the primary side. It is very necessary to analyze the characteristics of the circulating power in the dual boost integrated DAB converter since it is one of the main factors which will influence the efficiency of this converter.

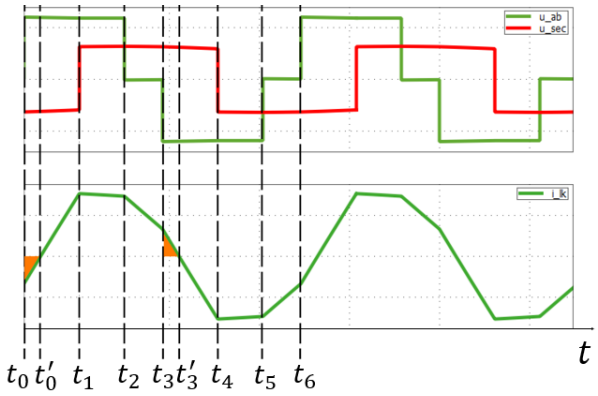


Figure 3.7: The circulating power of the dual boost integrated converter

Take Case V as an example to analyze the circulating power of the dual boost integrated DAB converter.

It can be seen from the Figure 3.7, in one switching period, there are two intervals which have the circulating power: $t_0 - t_0'$ and $t_3 - t_3'$. In these two time intervals, the signs of u_{ab} and i_{lk} are different. Due to the symmetries of the waveforms of u_{ab} and i_{lk}, the circulating power in these two intervals has the same amplitude. Hence, the average circulating power in one switching period can be expressed as:

$$P_{circulating}(\delta)(CaseV) = \frac{2\int_{t_0}^{t_0'} u_{ab}|i_{lk}(t)|dt}{T_s} \tag{3.32}$$

The point t_0' can be calculated by letting the equation 2.13 equal to zero and the result is:

$$t_0' = \frac{2T_{off}V_{in} - nT_sV_o + 4nT_s\delta V_o}{4(V_{in} + nV_o)} \tag{3.33}$$

In the interval $t = t_0 - t_0'$, the output voltage of the primary side bridge (u_{ab}) is V_{in}, so the average circulating power equation is:

$$P_{circulating}(\delta)(CaseV) = |\frac{V_{in}(2T_{off}V_{in} - nT_sV_o + 4nT_s\delta V_o)^2}{16L_{lk}T_s(V_{in} + nV_o)}| \tag{3.34}$$

By using the same methods, the average circulating power in different cases can be deduced:

$$P_{circulating}(\delta)(CaseI) = |\frac{V_{in}(2T_{on}V_{in} + nT_sV_o - 4nT_{on}V_o - 4nT_s\delta V_o)^2}{16L_{lk}T_s(V_{in} - nV_o)}| \tag{3.35}$$

$$P_{circulating}(\delta)(CaseII) = |\frac{V_{in}(2T_{on}V_{in} + nT_sV_o - 4nT_{off}V_o + 4nT_s\delta V_o)^2}{16L_{lk}T_s(V_{in} + nV_o)}| \tag{3.36}$$

$$P_{circulating}(\delta)(CaseIII) = |\frac{V_{in}(2T_{on}V_{in} + 3nT_sV_o - 4nT_s\delta V_o)^2}{16L_{lk}T_s(V_{in} + nV_o)}| \tag{3.37}$$

$$P_{circulating}(\delta)(CaseIV) = |\frac{V_{in}(2T_{on}V_{in} + 3nT_sV_o - 4nT_s\delta V_o)^2}{16L_{lk}T_s(V_{in} + nV_o)}| \tag{3.38}$$

$$P_{circulating}(\delta)(CaseVI) = |\frac{V_{in}(2T_{off}V_{in} - nT_sV_o + 4nT_s\delta V_o)^2}{16L_{lk}T_s(V_{in} + nV_o)}| \tag{3.39}$$

$$P_{circulating}(\delta)(CaseVII) = |\frac{V_{in}(2T_{off}V_{in} + nT_sV_o + 4nT_{off}V_o - 4nT_s\delta V_o)^2}{16L_{lk}T_s(V_{in} + nV_o)}| \tag{3.40}$$

$$P_{circulating}(\delta)(CaseVIII) = |\frac{V_{in}(2T_{off}V_{in} - 3nT_sV_o - 4nT_{off}V_o + 4nT_s\delta V_o)^2}{16L_{lk}T_s(V_{in} - nV_o)}| \tag{3.41}$$

According to the circulating power equations (equation 3.34 - equation 3.41), the circulating power curves when $G < 1$, $G = 1$ and $G > 1$ with different D can be plotted, as shown in the Figure 3.8. The red line in the Figure 3.8 is the case when $G < 1$, the blue line in the Figure 3.8 is the case when $G = 1$ and the green line in the Figure 3.8 is the case when $G > 1$. The output power curves are also plotted in the same figure with the same colors as their corresponding circulating power curves.

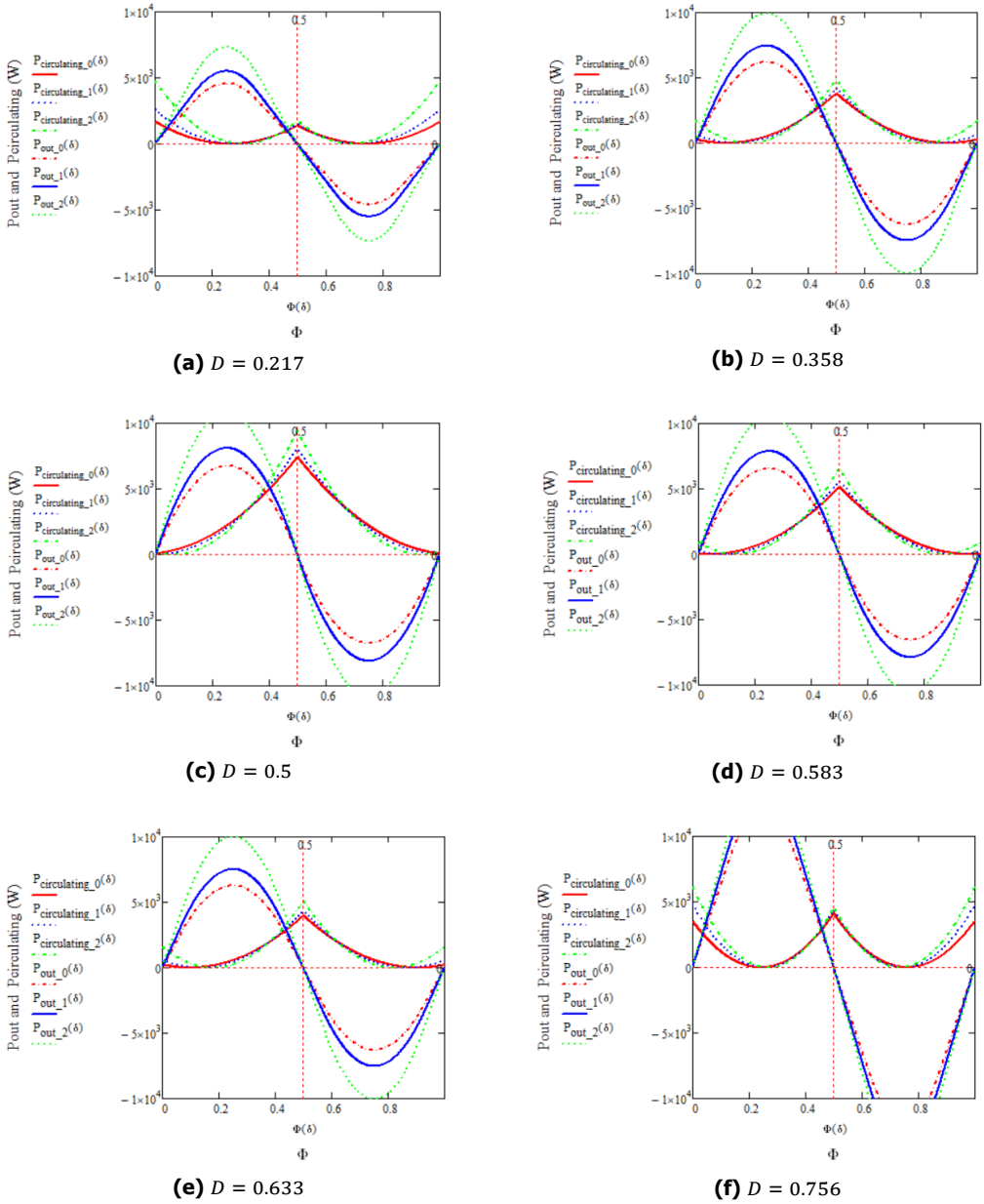
The circulating power ratio (Q) is the ratio between the circulating power and the output power, which can be calculated as:

$$Q = \frac{P_{circulating}(\delta)}{|P_{out}(\delta)|} \tag{3.42}$$

According to the circulating power equations (equation 3.34 - equation 3.41) and the output power equations deduced in the Section 2.4, the circulating power ratio curves when $G < 1$, $G = 1$ and $G > 1$ with different D can be plotted, as shown in the Figure 3.9. The red line in the Figure 3.9 is the case when $G < 1$, the blue line in the Figure 3.9 is the case when $G = 1$ and the green line in the Figure 3.9 is the case when $G > 1$.

The following conclusions can be summarized from the Figure 3.8 and Figure 3.9:

- At the maximum output power point, the difference of the circulating power ratio with different G is largest when D is 0.5. This difference will become smaller when the absolute value of $D - 0.5$ is increasing. However, there is a duty cycle with which the difference of the circulating power ratio with different G will be 0 at the maximum output power point and when the absolute value of $D - 0.5$ continuously increases, this rule will be changed to when the absolute value of $D - 0.5$ is increasing, the difference of the circulating power ratio with different G becomes larger.



(a) $D = 0.217$ **(b)** $D = 0.358$

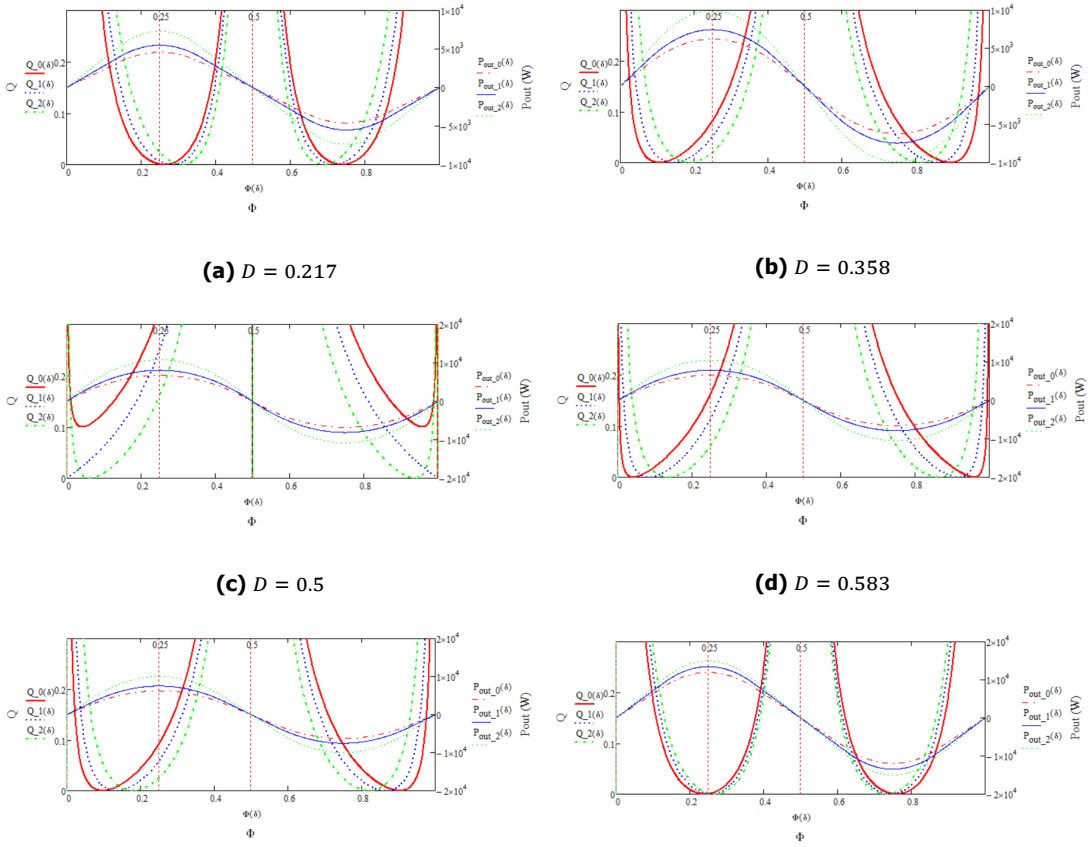
(c) $D = 0.5$ **(d)** $D = 0.583$

(e) $D = 0.633$ **(f)** $D = 0.756$

Figure 3.8: The circulating power curves

- The circulating power ratio Q is smaller when the voltage gain G increases before the point when the difference of the circulating power ratio with different G is 0 at the maximum output power point and after this point the circulating power ratio Q is larger when the voltage gain G increases.

Since the circulating power will increase the current stress and losses on the components of the dual boost integrated DAB converter, it is necessary to keep the circulating power as small as possible. However, according to the analysis of the ZVS characteristics and the circulating power, it can be seen that the condition of increasing the ZVS region of the secondary side switches and the condition of increasing the ZVS region of the primary side switches are contradictory since when the voltage gain G is increasing, the ZVS region of the secondary side switches will increase but the ZVS region of the primary side switches will decrease. Besides, when the absolute value of $D - 0.5$ is smaller than the boundary when the difference of the circulating power ratio with different G is 0, the condition of decreasing the circulating power at the maximum output power point is contradictory with the condition of increasing the ZVS region of the primary side switches and when the absolute value of $D - 0.5$ is



(a) $D = 0.217$ **(b)** $D = 0.358$

(c) $D = 0.5$ **(d)** $D = 0.583$

(e) $D = 0.633$ **(f)** $D = 0.756$

Figure 3.9: The circulating power ratio curves

larger than the boundary when the difference of the circulating power ratio with different G is 0, the condition of decreasing the circulating power at the maximum output power point is contradictory with the condition of increasing the ZVS region of the secondary side switches. Hence, it is necessary to find a method which can realize the ZVS of all the switches in a large voltage range while the circulating power can be kept as small as possible.

3.3. Optimization of the ZVS region and the circulating power

According to the analysis of the ZVS region and the circulating power of the dual boost integrated DAB converter, several important conclusions should be addressed again:

- Once $G > 1$, the ZVS of the secondary side switches can be realized in the whole power range in all the cases.
- For the primary side switches, the smaller the G, the larger the ZVS region.
- When $D \leq 0.5$, the larger the D, the larger the ZVS region of the primary side switches but when $D > 0.5$, the smaller the D, the larger the ZVS region of the primary side switches.
- There is a boundary of the absolute value of $D - 0.5$, the circulating power ratio decreases when the voltage gain increases when the absolute value of $D - 0.5$ is smaller than the boundary value and the circulating power ratio increases when the voltage gain increases when the absolute value of $D - 0.5$ is larger than the boundary value.

The specifications of the converter is clarified in Section 2.1: the input voltage of the DC bus port is $600V - 900V$, the PV voltage is $220V - 470V$ and the output voltage is $200V - 950V$. Hence, the range

of the duty cycle D is $0.217 - 0.756$ and the range of the voltage gain G is $0.667 - 2.111$. It can be seen that there is a large range where the voltage gain is far beyond 1 and the ZVS of the primary side switches is difficult to realize during this range. Besides, once the absolute value of $D - 0.5$ is larger than the boundary when the difference of the circulating power ratio with different G is 0, the large voltage gain will introduce a larger circulating power ratio.

The DC blocking capacitor voltage control which is proposed in [39] is aimed to increase the ZVS region and decrease the circulating power of the DAB converter with a large output voltage range. The same method can be used in this dual boost integrated DAB converter since it is a DAB converter from the input port to the output port.

3.3.1. DC blocking capacitor voltage control

The schematic of the proposed dual boost integrated DAB converter with the DC blocking capacitor is shown in the Figure 3.10.

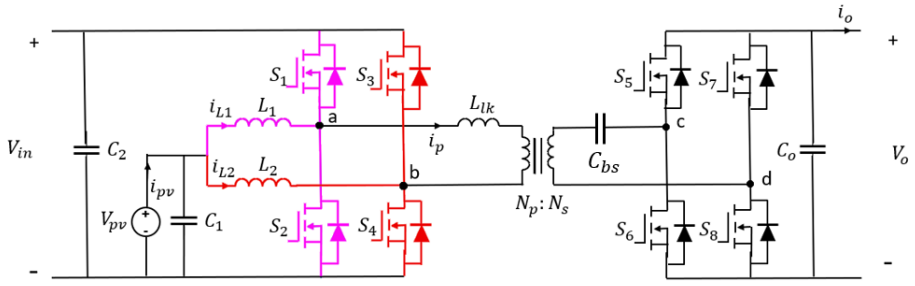


Figure 3.10: The schematic of the proposed dual boost integrated DAB converter with the DC blocking capacitor

The basic principle of the DC blocking capacitor voltage control is to introduce a voltage offset on the blocking capacitor (C_{bs}) when the voltage gain G is close to 2. A new modulation method is introduced to realize the DC blocking capacitor voltage control. Instead of pulse-width modulating S7 and S8, S7 is always off and S8 is always on in the new modulation when the voltage gain G is close to 2. The voltage at the point d in the Figure 3.10 will be clamped to 0, so the output voltage of the secondary side bridge (u_{cd}) will be changed from the pure AC voltage to the one with a DC component, as shown in the Figure 3.11. The DC component in u_{cd} is always $\frac{V_o}{2}$ since the duty cycle of the S5 and S6 is always 0.5. This DC component will drop on the blocking capacitor, so the voltage on the secondary side of the transformer will be an AC voltage whose amplitude is $\frac{V_o}{2}$ with no DC component.

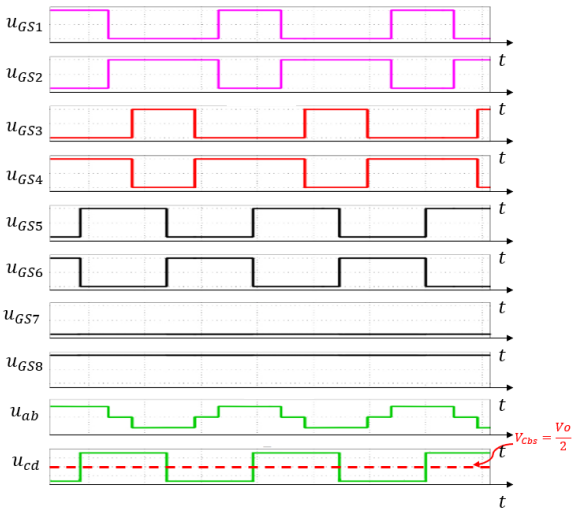


Figure 3.11: The gate signals and the key waveforms using DC blocking capacitor voltage control

By using the DC blocking capacitor voltage control, the voltage gain G can be always kept close to 1, which can widen the ZVS region and the low circulating power range to improve the efficiency of the dual boost integrated DAB converter with a large output voltage range.

3.3.2. Optimized working range

It can be seen from the Figure 3.1 - Figure 3.6 that the ZVS of the primary side switches is more difficult to realize when $D < 0.5$ compared with that when $D > 0.5$ and the most difficult points are when $D < 0.5$ and the phase shift Φ are $\frac{1}{4} - \frac{1}{2}D$ and $\frac{3}{4} + \frac{1}{2}D$, as shown in the Figure 3.12 which is the case when $D = 0.217$ and $G > 1$.

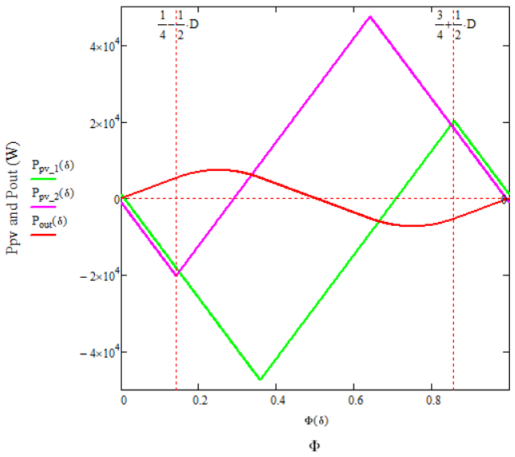


Figure 3.12: The most difficult points to realize the ZVS of the primary side switches when $D < 0.5$

Due to the symmetry of the ZVS region of the primary side switches, only consider one of the two worst points. Since when $D < 0.5$, the smaller the D, the smaller the ZVS region of the primary side switches and $D = 1 - \frac{V_{pv}}{V_{in}}$, so the worst case must happen when the input voltage is minimum ($V_{in} = 600V$). Use the ZVS boundary equations deduced in Section 3.1.2 and the output power equations deduced in Section 2.4, the cross point of the ZVS boundary of S2 and S4 and the output power when the phase shift $\Phi = \frac{1}{4} - \frac{1}{2}D$ can be calculated by solving the following equation which is got by using the equation 3.19 to subtract the equation 2.48:

$$P(D,G) = \frac{T_s V_{in}^2 (2DL_1 + 2DL_{lk} - GL_1 - 2D^2L_1 - 4D^2L_{lk} + 2D^3L_{lk} + 2D^2GL_1)}{2L_1L_{lk}} = 0 \qquad (3.43)$$

The solutions of equation 3.43 are shown in the Figure 3.13 which is drawn in Mathcad and P_1 is the zero plane. In Mathcad, all the solutions (different combinations of D and G) can be displayed. According to the ranges of D and G in this project, choose the minimum D when G is just larger than 1. Hence, this is the minimum D with which the converter is possible to realize the ZVS of both primary and secondary side switches. The minimum D is 0.465 and the corresponding G is 1.019, which is read from the results in the Mathcad. When V_{in} is $600V$, the output voltage V_o is $305.7V$. The ZVS region of the primary side switches when the input voltage is $600V$, the duty cycle D is 0.465 and the voltage gain G is 1.019 is shown in the Figure 3.14.

When the voltage gain is 1.019 and $V_{in} = 900V$, the corresponding output voltage V_o is $458.55V$. When $V_{in} = 900V$, according to the MPPT voltage range of the PV panel in this project, the minimum duty cycle D is 0.478. When $D = 0.478$, according to the solutions of the equation 3.43, $G = 1.065$, which means once the voltage gain is less than 1.065 ($Vo = 479.25V$), the ZVS of the primary side switches can be realized in the whole power range when $V_{in} = 900V$. The ZVS region of the primary side switches when the input voltage is $900V$, the duty cycle D is 0.478 and the voltage gain G is 1.065 and 1.019 are shown in the Figure 3.15. The maximum PV voltage is $470V$ in this project, which means the ZVS of both primary and secondary side switches can be realized in the whole PV voltage range when the input voltage is larger than $878.5V$. And when the input voltage is less than $878.5V$, the maximum PV voltage should be controlled to make sure the minimum duty cycle is 0.465 once the voltage gain

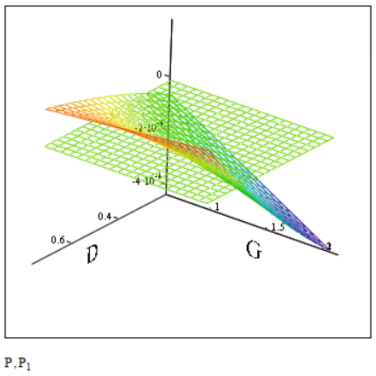


Figure 3.13: The solutions of equation 3.43

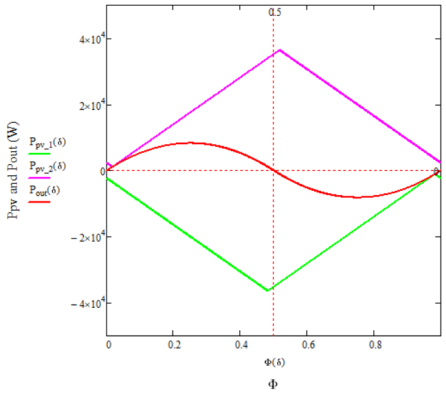
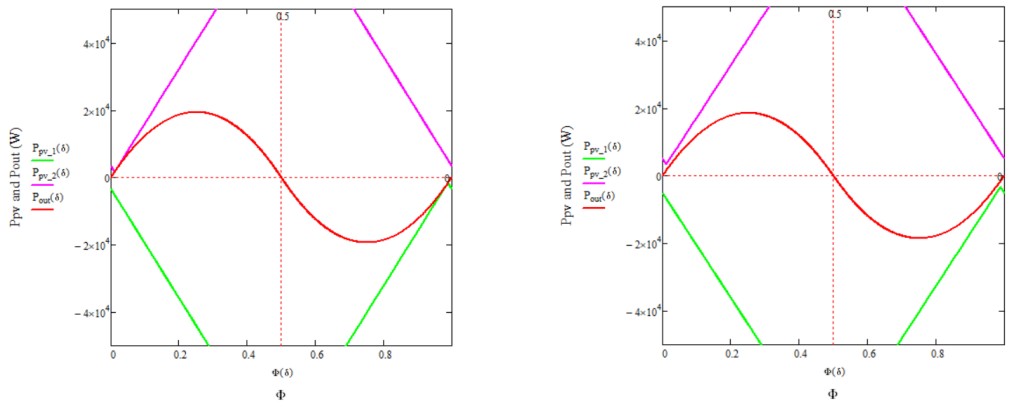


Figure 3.14: The ZVS region of the primary side switches when the input voltage is $600V$, the duty cycle D is 0.465 and the voltage gain G is 1.019

can be kept at 1.019. When the input voltage is larger than $878.5V$, the maximum voltage gain which can realize the ZVS of both primary and secondary side switches can be calculated by the equation 3.43. Calculate the duty cycle and replace the duty cycle in the equation to calculated the voltage gain. Once the input voltage is larger than $878.5V$, the minimum duty cycle is larger than 0.465, the maximum voltage gain can be larger than 1.019. Since the boundary of the absolute value of $D - 0.5$ is 0.25, which means once the duty cycle D is larger than 0.25 and smaller than 0.75, the circulating power ratio decreases when the voltage gain increases and most of the cases of this converter when the optimized duty cycle is implemented is inside this range, the circulating power is also optimized because the voltage gain is set as the maximum allowable value.

According to the analysis of the worst case, in order to realize the ZVS of both the primary and secondary side switches and get less circulating power of the dual boost integrated DAB converter with a large output voltage range, the following rules should be followed:

- When $200V \leq Vo \leq 300V$, keep $Vin = 600V$, the ZVS of primary side switches can be realized, but the ZVS of the secondary side switches cannot be realized in some cases.
- When $300V < Vo < 305.7V$, keep $Vin = 600V$, $1 < G < 1.019$, the ZVS of both primary and secondary side switches can be realized in the whole power range.
- When $305.7V \leq Vo \leq 458.55V$, adjust Vin to keep the $G = 1.019$, then the ZVS of both primary and secondary side switches can be realized in the whole power range and the circulating power is minimum when the output power is maximum.
- When $458.55V < Vo \leq 479.25V$, keep $Vin = 900V$, since $1.019 < G \leq 1.065$, the ZVS of both primary and secondary side switches can be realized in the whole power range.



(a) $G = 1.065$ **(b)** $G = 1.019$

Figure 3.15: The ZVS region of the primary side switches when the input voltage is $900V$ and the duty cycle D is 0.478

- When $479.25V < Vo \leq 600V$, keep $Vin = 900V$, $G > 1.065$, the ZVS of the primary side switches will be lost in some cases but the ZVS of the secondary side switches can always be realized.
- When $600V < Vo < 611.4V$, use the DC blocking capacitor voltage control and keep $Vin = 600V$, $1 < G < 1.019$, the ZVS of both primary and secondary side switches can be realized in the whole power range.
- When $611.4V \leq Vo \leq 917.1V$, use the DC blocking capacitor voltage control and adjust Vin to keep the $G = 1.019$, then the ZVS of both primary and secondary side switches can be realized in the whole power range and the circulating power is minimum when the output power is maximum.
- When $917.1V < Vo \leq 950V$, use the DC blocking capacitor voltage control and keep $Vin = 900V$, $1.019 < G < 1.065$, the ZVS of both primary and secondary side switches can be realized in the whole power range.

Hence, if all these rules are followed, except the output voltage range of $200V \leq Vo \leq 300V$ and $479.25V < Vo \leq 600V$, the ZVS of all the switches in this converter is possible to be realized in the whole power range once the output capacitance of the switches and the dead time are chosen properly if the minimum D is 0.465. Besides, since the voltage gain G is controlled as the maximum allowable value, the minimum circulating power is kept in a large range. The optimized working range of the PV voltage according to the different input voltage is shown in the Figure 3.16 and the optimized input voltage according to the different output voltage is shown in the Figure 3.17. It can be seen from the Figure 3.16 that once the input voltage is larger than $878.5V$, the whole MPPT voltage range ($220V - 470V$) of this project is satisfied with the optimized working range of the PV voltage. Besides, the minimum duty cycle of S2 and S4 can be lower than 0.465 when the output voltage is smaller than $305.7V$ since the voltage gain will be smaller than 1.019 in these cases. And the minimum duty cycle of the S2 and S4 in these cases can be calculated by the equation 3.43.

The ZVS conditions of the primary and secondary side switches analyzed before are the conditions with which the ZVS of the primary and secondary side switches is possible to be realized in the whole power range. However, the power rating of the EV charger in this project is $10kW$, once the output power of the converter cannot reach the $10kW$ due to the limitation of the maximum output current, the converter will always work at the maximum output power point during the steady state charging period. According to the analysis of the output power curves in the Section 2.4, the maximum output power point is when the phase shift Φ is 0.25 and it is always in the Case II when the duty cycle of S2 and S4 (D) is less than or equal to 0.5 or in the Case V when the duty cycle of S2 and S4 (D) is larger than 0.5. According to the ZVS conditions in the Table 3.1, the ZVS conditions of the secondary side switches of Case II and Case V are the same, which is:

$$(4\delta + 2D + G - 2) > 0 \tag{3.44}$$

where $\delta = \Phi - \frac{1}{2}D + \frac{1}{4}$ and Φ is 0.25 at the maximum output power point. So the ZVS condition of the secondary side switches at the maximum output power point is simplified to:

$$G > 0 \tag{3.45}$$

and this is always satisfied. Hence, the ZVS of all the switches in this converter can be realized at the maximum output power point when $200V \leq Vo \leq 300V$ and since the maximum output power cannot reach $10kW$ during this range because of the limitation of the maximum output current, so the converter will always work at the maximum output power point during the steady state charging period.

As for the output voltage range when $479.25V < Vo \leq 600V$, during which the ZVS of the primary side switches will be lost in some cases but the ZVS of the secondary side switches can always be realized according to previous optimized results. However, if the DC blocking capacitor voltage control is used during this range, the ZVS of the primary side switches is possible to be realized in the whole power range and the ZVS of the secondary side switches can always be realized at the maximum output power but the maximum output power cannot reach $10kW$ anymore. The average output power equations of Case II and Case V are the same, which is:

$$P_{out}(\delta) = \frac{nV_{in}V_o(4T_sT_{off}\delta - 4T_s^2\delta^2 + T_sT_{off} - 2T_{off}^2)}{2L_{lk}T_s} \tag{3.46}$$

where $T_{off} = (1-D)T_s$ and $\delta = \Phi - \frac{1}{2}D + \frac{1}{4}$. The voltage gain is $G = n\frac{\frac{V_o}{2}}{V_{in}}$ if the DC blocking capacitor voltage control is used. Therefore, the average output power equation of Case II and Case V can be written as:

$$P_{out} = -\frac{0.125GT_sV_{in}^2(4D^2 - 4D + 16\Phi^2 - 8\Phi + 1)}{L_{lk}} \tag{3.47}$$

If the DC blocking capacitor voltage control is used when $479.25V < V_o \leq 600V$, keep $V_{in} = 600V$. When $D = 0.5$ and $\Phi = 0.25$, the transferred power is maximum according to the analysis in the Section 2.4. Hence, the maximum output power curve which all the switches in the converter can realize ZVS at the maximum output power point is shown in the Figure 3.18.

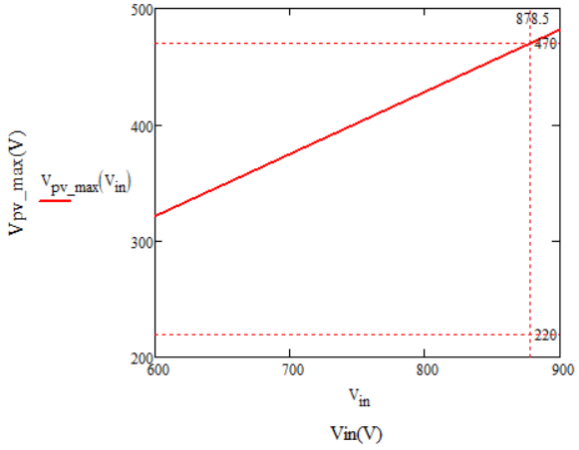


Figure 3.16: The optimized working range of the PV voltage according to different input voltage

Another method to realize the ZVS of the primary side switches in this converter when $479.25V < Vo \leq 600V$ is to reduce the PV power. The ZVS of the secondary side switches can always be realized but the ZVS of S2 and S4 will be lost is some cases during the charging mode and the ZVS of S1 and S3 will be lost in some cases during the discharging mode when $479.25V < Vo \leq 600V$. Due to the symmetry of both the output power curve and the ZVS region, once the ZVS of S2 and S4 can be realized in the charging mode, the ZVS of S1 and S3 will be also realized in the discharging mode.

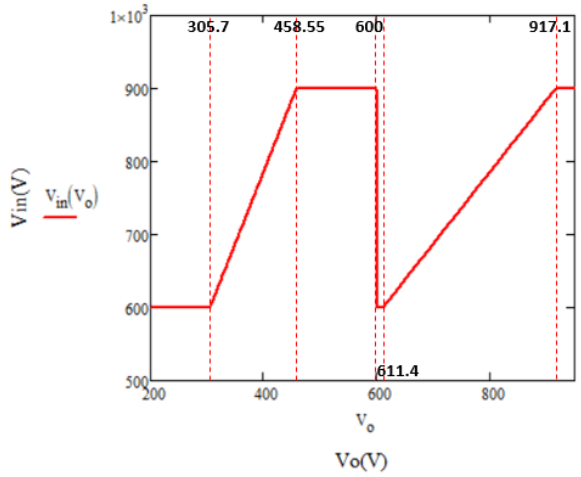


Figure 3.17: The optimized input voltage according to the different output voltage

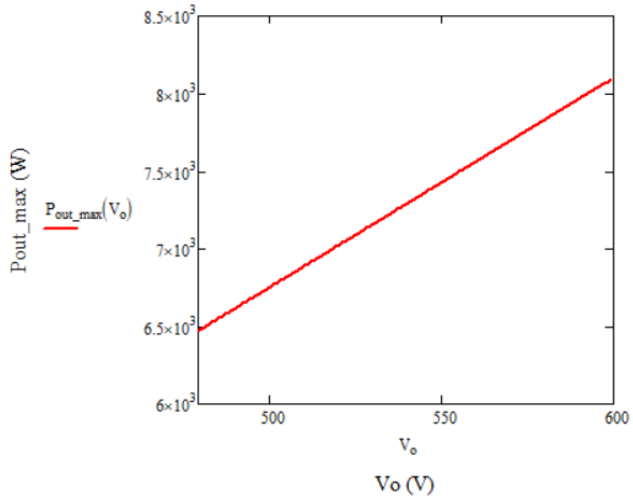


Figure 3.18: The maximum output power at which the ZVS of all the switches can be realized when $479.25V < V_o \leq 600V$

Therefore, only the ZVS of S2 and S4 in the charging mode when $479.25V < Vo \leq 600V$ is analyzed here. According to the ZVS boundary conditions of the S2 and S4 deduced in the Section 3.1.2, it can be seen that once the PV power is less than the boundary value, the ZVS of S2 and S4 can be realized at that point. The output power can reach 10kW when $479.25V < Vo \leq 600V$ if the DC blocking capacitor voltage control is not used. Hence, the converter is always transferring $10kW$ to the EV battery during the steady state charging period. The phase shift when the output power is $10kW$ can be calculated by the output power equations deduced in the Section 2.4 and the ZVS boundary of the S2 and S4 can be calculated by substituting the phase shift in the boundary equations to the one at which the output power is $10kW$. And make sure that the PV power is less than the boundary value then the ZVS of S2 and S4 during the charging mode and the ZVS of S1 and S3 during the discharging mode when $479.25V < Vo \leq 600V$ can be realized. Besides, the ZVS of the secondary side switches can be realized in the whole power range and the output power can reach $10kW$. This boundary PV power curve with which the ZVS of the primary side switches can be realized at $10kW$ output power point when $479.25V < Vo \leq 600V$ is shown in the Figure 3.19.

3.3.3. Simulation verification

In order to verify the optimized ZVS range, the simulations of the converter working at different output voltages are done in the PLECS. The simulation results are shown in the Figure 3.20. The green

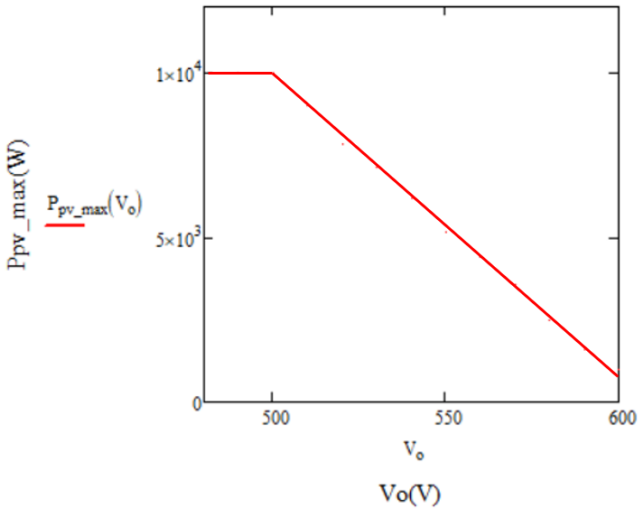


Figure 3.19: The boundary PV power curve

lines are the gate signals which are enlarged 20 times since the PLECS does not allow to use two different Y axes in one scope and the red lines are the drain source current of different switches. It can be seen from the Figure 3.20 that the ZVS of all the switches in the dual boost integrated DAB converter can be realized at the boundary points of the optimized working ranges. The reverse current is smallest when the output voltage (V_o) is $479.25V$ and voltage gain (G) is 1.065 since this is the boundary of the output voltage range when the ZVS of S2 and S4 can be realized in the charging mode and the DC blocking capacitor voltage control is not used.

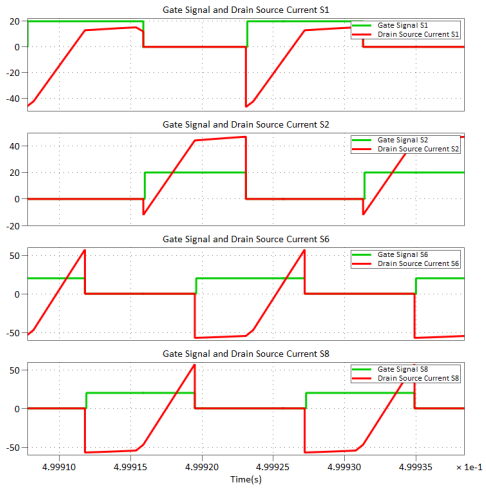
According to the conclusion got from the Section 3.3.2, the ZVS of all the switches can be realized at the maximum output power point when $200V \leq V_o \leq 300V$. The simulation results of $V_o = 200V$ and $V_o = 300V$ at the maximum output power points are shown in the Figure 3.21. The duty cycles in this figure are the minimum duty cycles corresponding to these cases, which are calculated by using the equation 3.43.

As for the output voltage range $479.25V < Vo \leq 600V$, the two methods (applying the DC blocking capacitor voltage control and reducing the PV power) to realize the ZVS of all the switches in the converter are verified by the simulation results shown in the Figure 3.22 and Figure 3.23,respectively. The duty cycles in the Figure 3.22 are the minimum duty cycles calculated by using the equation 3.43. Once the DC blocking capacitor voltage control is used when the output voltage is $479.25V - 600V$, the output power cannot reach $10kW$ but it can be seen from the Figure 3.22 that the ZVS of all the switches can be realized at the maximum output power points. The output power can reach $10kW$ if the method of reducing the PV power is used to realize the ZVS of all the switches when the output voltage is $479.25V - 600V$. The ZVS of all the switches in this converter can be realized at the $10kW$ output power point by limiting the maximum PV power. And it can be seen from the Figure 3.19 that once the output voltage is higher than $500V$, the maximum PV power should be lower than $10kW$ in order to realize the ZVS of all the switches at the $10kW$ output power point.

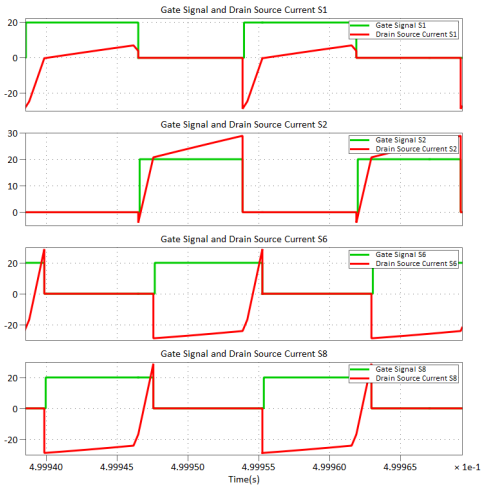
All the simulation results are consistent with the previous analysis, which can verify that the analysis is correct.

3.4. Loss breakdown of the switches

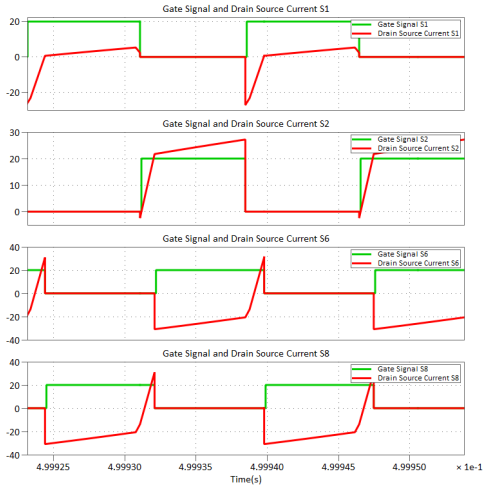
According to the loss breakdown analysis of the traditional DAB converter in [41–44], it can be seen that the conduction losses and the switching losses of the switches are the largest loss in this converter. Due to the introduction of the interleaved boost converters in the primary side, the loss distribution on the switches is not symmetric any more. The losses on the upper switch and lower switch in the same leg in the primary side are not the same. Besides, there is no loss on the switch S7 and only conduction loss on switch S8 when the DC blocking capacitor voltage control starts to work. Hence, it is meaningful to analyze the loss distribution of the switches in the dual boost integrated DAB converter.



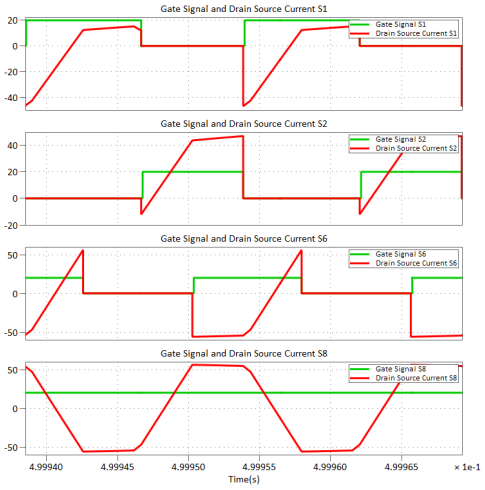
(a) $D = 0.465, G = 1.019, V_o = 305.7V$



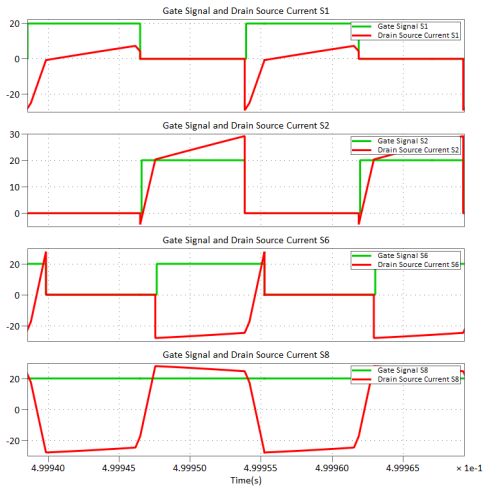
(b) $D = 0.478, G = 1.019, V_o = 458.55V$



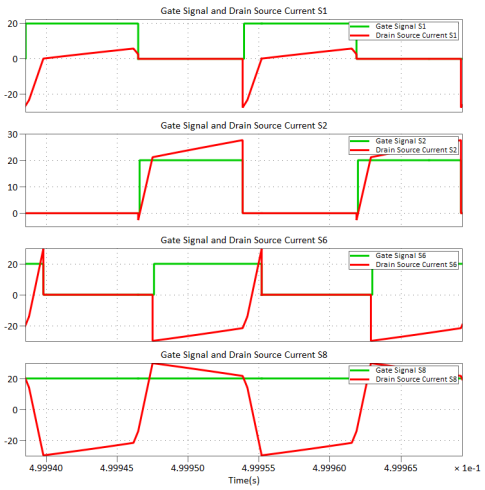
(c) $D = 0.478, G = 1.065, V_o = 479.25V$



(d) $D = 0.465, G = 1.019, V_o = 611.4V$



(e) $D = 0.478, G = 1.019, V_o = 917.1V$

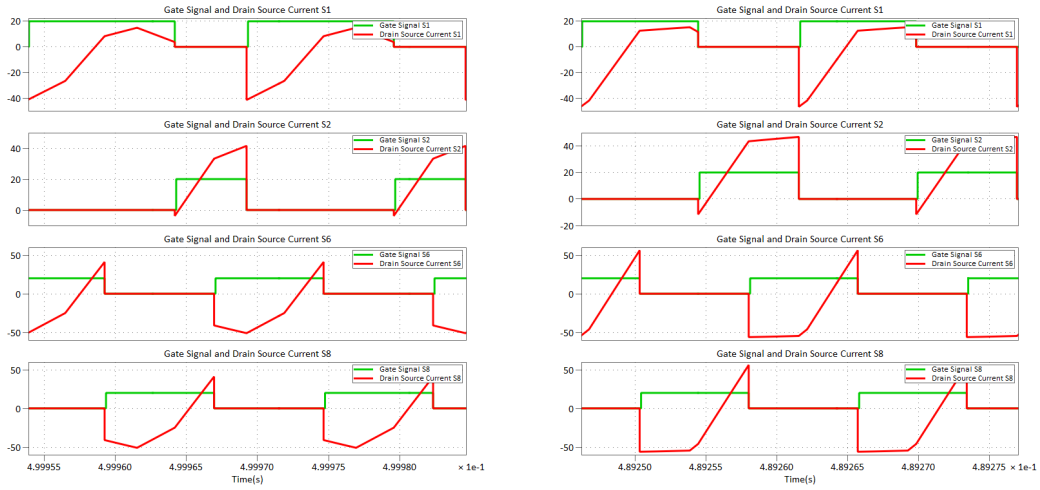


(f) $D = 0.478, G = 1.056, V_o = 950V$

Figure 3.20: The ZVS simulation verification

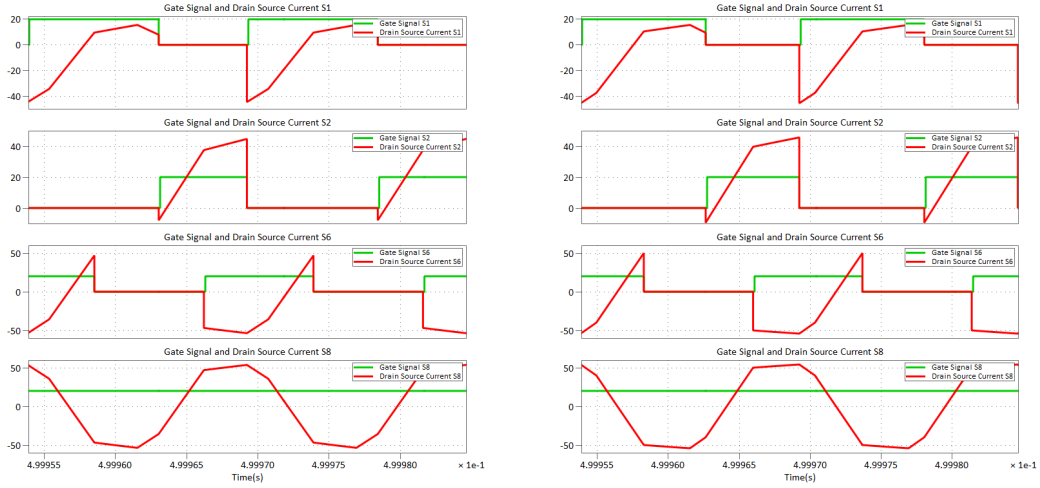
3.4.1. Selection of the transistors

According to the input and output voltage level which are specified in the Section 2.1, the $1200V$ SiC MOSFET is selected in this converter. According to the recorded data got from the simulation, the



(a) $D = 0.324, V_{in} = 600V, V_o = 200V$ **(b)** $D = 0.460, V_{in} = 600V, V_o = 300V$

Figure 3.21: The ZVS simulation verification of $V_o = 200V$ and $V_o = 300V$

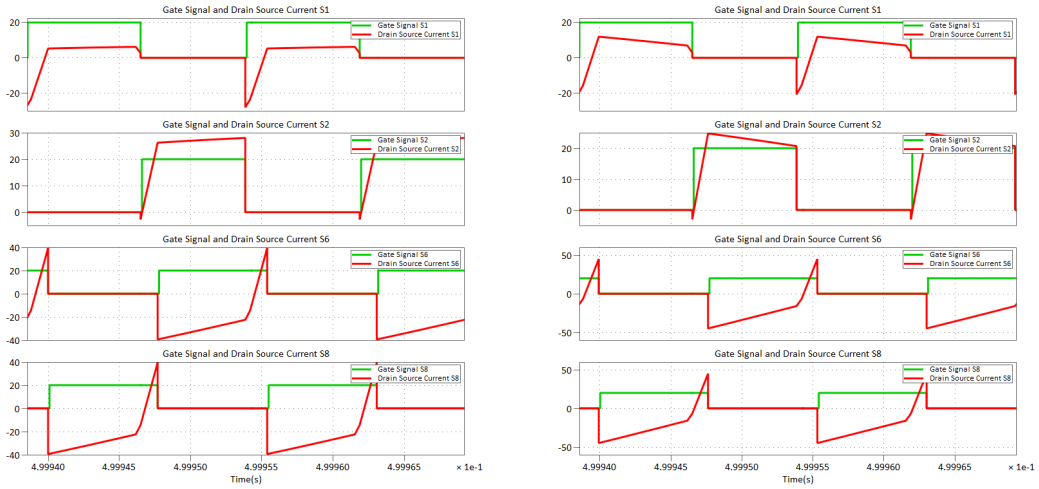


(a) $D = 0.400, V_{in} = 600V, V_o = 500V$ **(b)** $D = 0.426, V_{in} = 600V, V_o = 540V$

Figure 3.22: The ZVS simulation verification of $V_o = 500V$ and $V_o = 540V$ with DC blocking capacitor voltage control

maximum peak current of the switches will be higher than $86A$ and the maximum RMS current of the switches will be higher than $50A$ in this converter. The 10% margin should be set to the maximum peak current and maximum RMS current of the switches, which means the SiC MOSFET candidates should be able to stand a peak current as high as $94.6A$ and the RMS current as high as $55A$. The low on-resistance of the MOSFET is important for this converter due to the high RMS current. Besides, since the switches will be turned off at the peak current point, the switching off losses are also critical for the total losses of the switches. The continuous drain current of the existing commercial SiC MOSFETs is hard to meet the current requirement when the temperature is $100°C$ in this project. A solution to solve this problem is paralleling the SiC MOSFETs to get the higher current rating and also reduce the turn off losses and conduction losses. Three SiC MOSFET candidates are selected according to the voltage level, the current level, the on-resistance and the switching off energy. The information of the three candidates are shown in the Table 3.4 [45–47] and the schematics of the bridges with two parallel SiC MOSFETs and the bridges with three parallel SiC MOSFETs are shown in the Figure 3.24.

In order to evaluate which SiC MOSFET is more suitable for this topology and to decide whether two parallel MOSFETs or three parallel MOSFETs solution should be used, the power loss model and the

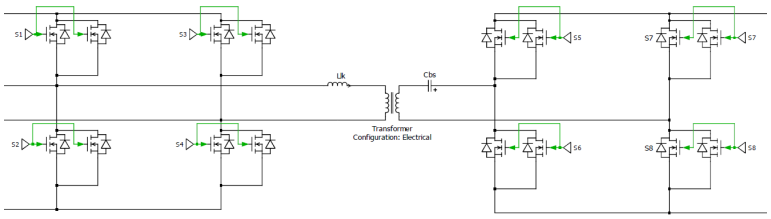


(a) $D = 0.478, V_o = 500V, P_{pv} = 10kW$ **(b)** $D = 0.478, V_o = 540V, P_{pv} = 6.179kW$

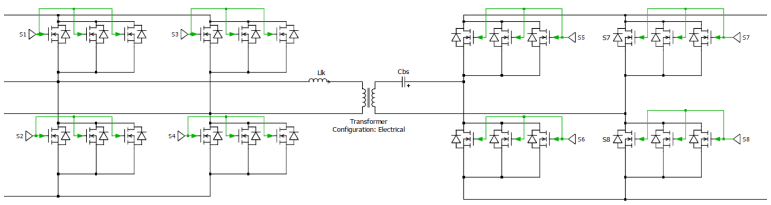
Figure 3.23: The ZVS simulation verification of $V_o = 500V$ and $V_o = 540V$ with reduced PV power

Table 3.4: Information of the SiC MOSFET candidates

Manufacturer	Type	Part No.	$I_{ds,max}(A)$ $(T_j = 25°C)$	$I_{ds,max}(A)$ $(T_j = 100°C)$	$T_{j,max}$ $(°C)$	$V_{ds,max}$ (V)	$R_{ds}(m\Omega)$ (typical)
Cree	SiC	C3M0075120K	30	19.7	150	1200	75
Cree	SiC	C2M0040120D	60	40	150	1200	40
Cree	SiC	C2M0025120D	90	60	150	1200	25



(a) The bridge with two parallel SiC MOSFETs



(b) The bridge with three parallel SiC MOSFETs

Figure 3.24: The schematics of the bridge with the parallel SiC MOSFETs

thermal model of the switches should be built.

3.4.2. Power loss model of the switches

The power losses of the MOSFET are composed of switching losses and conduction losses. The conduction losses include the conduction loss of the MOSFET and the conduction loss of the antiparallel diode.

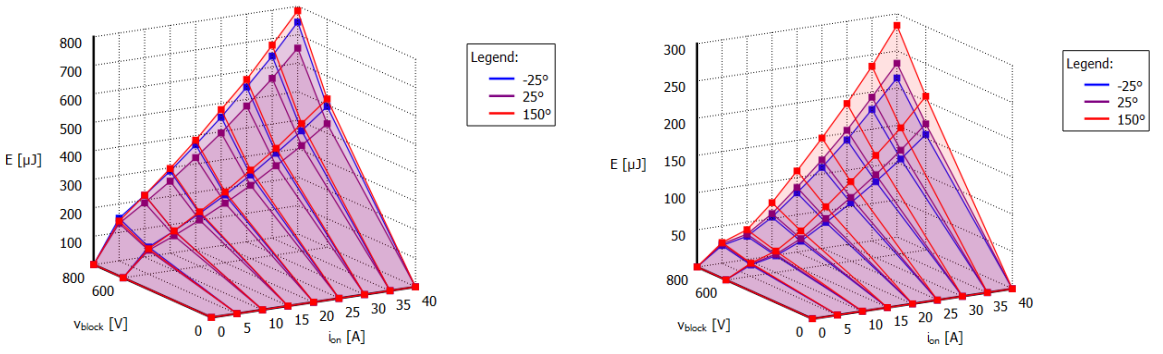
- Switching loss modelling:

  The switching losses exist because of the overlap of the drain-source current i_{ds} and the drain-source voltage v_{ds} during the turn-on and turn-off period. And the switching loss model can be represented as:

$$P_{sw} = f_{sw}[E_{on}(i_{on}, v_{block}, T_j) + E_{off}(i_{on}, v_{block}, T_j)] \tag{3.48}$$

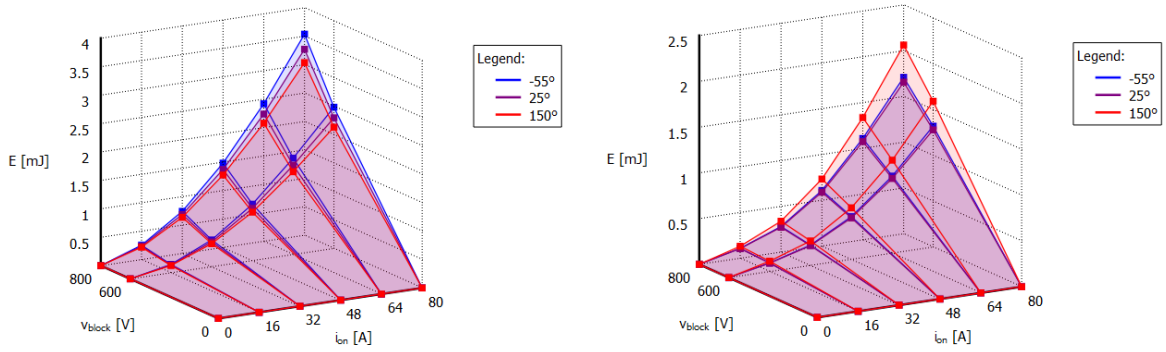
  where E_{on} and E_{off} are the turn-on and turn-off energy losses, separately. v_{block} is the block voltage on the switches and i_{on} is the conduction current at the turn-on or turn-off transition. T_j is the junction temperature of the switches.

  The turn-on and turn-off energy losses are provided in the datasheet [45–47] of the SiC MOSFET by the manufacturers. Assuming the switching loss is linearly related to the block voltage and the junction temperature, the 3D look-up tables of the E_{on} and E_{off} of the three SiC MOSFET candidates are shown in the Figure 3.25, Figure 3.26 and Figure 3.27, respectively. In these tables, the switching losses of the body diode due to the reverse recovery charge are also included.



(a) Switching on loss (E_{on}) **(b)** Switching off loss (E_{off})

Figure 3.25: 3D look-up tables of the switching losses of C3M0075120K

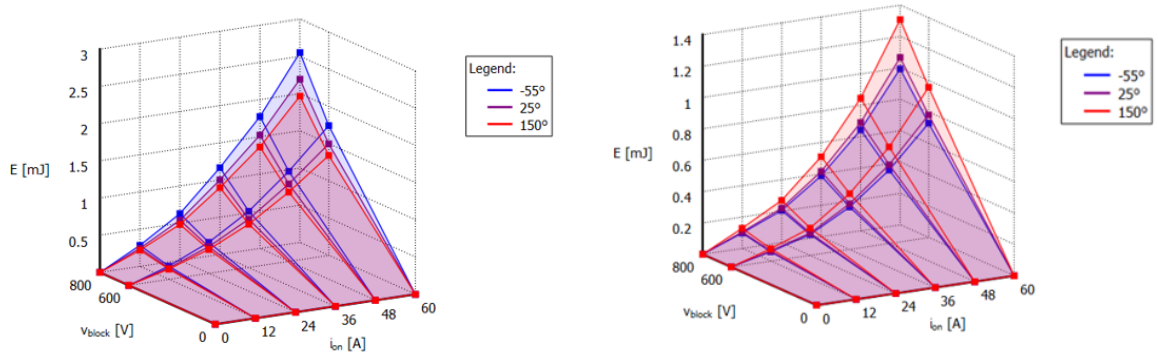


(a) Switching on loss (E_{on}) **(b)** Switching off loss (E_{off})

Figure 3.26: 3D look-up tables of the switching losses of C2M0040120D

- Conduction loss modelling:

  The conduction loss of the power MOSFET is decided by the conduction current (i_{on}) flowing through the MOSFET during the conduction phase and the equivalent on-state resistance ($R_{ds(on)}$) and the $R_{ds(on)}$ is influenced by the conduction current and the junction temperature of the MOSFET, so the conduction loss model is:

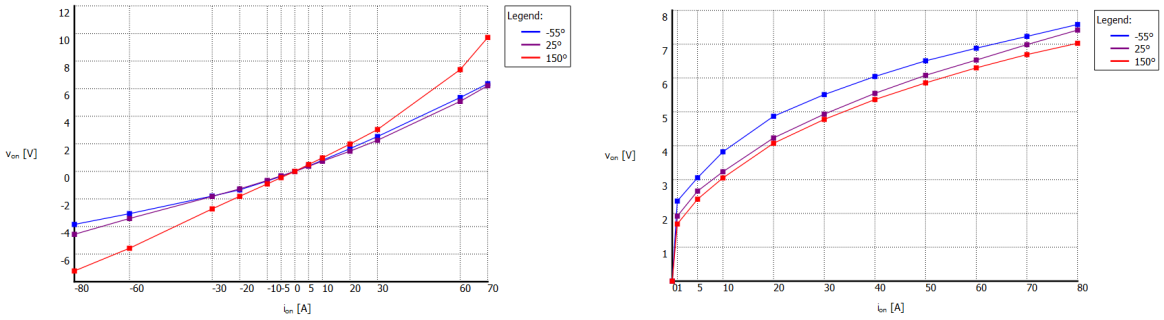


(a) Switching on loss (E_{on}) **(b)** Switching off loss (E_{off})

Figure 3.27: 3D look-up tables of the switching losses of C2M0025120D

$$P_{cond} = R_{ds(on)}(i_{on}, T_j) \cdot i_{on}(t)^2 = V_{on}(i_{on}, T_j) i_{on}(t) \tag{3.49}$$

Since the on-state resistance ($R_{ds(on)}$) is changed according to the i_{on} and T_j, the voltage dropped on the MOSFET during the on phase will also be changed. According to the datasheets [45–47], the 2D look-up tables of the $V_{on}(i_{on}, T_j)$ of the MOSFET and the body diode are shown in the Figure 3.28, Figure 3.29 and Figure 3.30. And the conduction losses of the MOSFET and the body diode can be estimated according to these look-up tables.



(a) $V_{on}(i_{on}, T_j)$ of the MOSFET **(b)** $V_{on}(i_{on}, T_j)$ of the body diode

Figure 3.28: 2D look-up tables of $V_{on}(i_{on}, T_j)$ in terms of different i_{on} and T_j of C3M0075120K

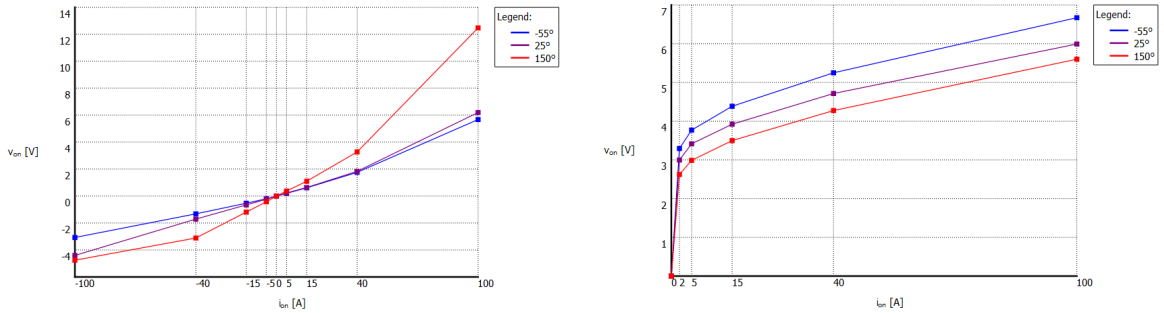
Hence, the power loss model of the single MOSFET is:

$$P_{loss} = \frac{1}{T_s} \int_0^{T_s} (P_{cond}(t) + P_{sw}(t)) dt \tag{3.50}$$

For the paralleling MOSFETs, the loss model is:

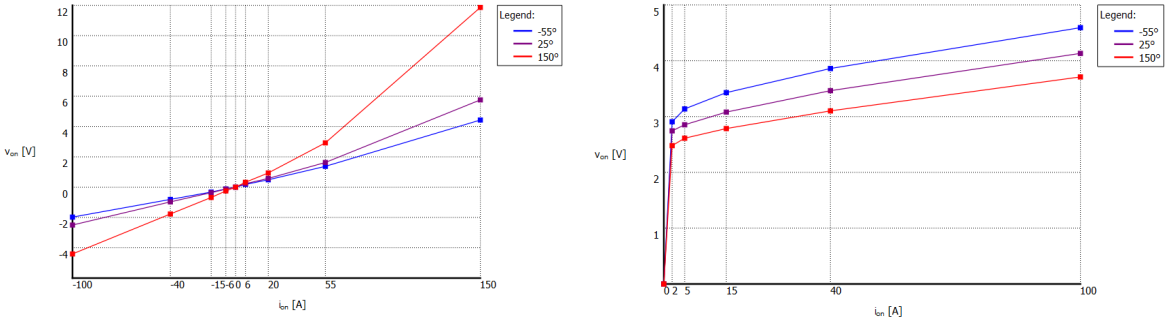
$$P_{loss} = N \frac{1}{T_s} \int_0^{T_s} (P_{cond}(t) + P_{sw}(t)) dt \tag{3.51}$$

where N is the number of the MOSFETs connected in parallel and T_s is the switching period.



(a) $V_{on}(i_{on}, T_j)$ of the MOSFET **(b)** $V_{on}(i_{on}, T_j)$ of the body diode

Figure 3.29: 2D look-up tables of $V_{on}(i_{on}, T_j)$ in terms of different i_{on} and T_j of C2M0040120D



(a) $V_{on}(i_{on}, T_j)$ of the MOSFET **(b)** $V_{on}(i_{on}, T_j)$ of the body diode

Figure 3.30: 2D look-up tables of $V_{on}(i_{on}, T_j)$ in terms of different i_{on} and T_j of C2M0025120D

3.4.3. Thermal model of the switches

The thermal model of the power MOSFET is actually a thermal circuit which the thermal parameters are represented by the electrical parameters. By neglecting the heat transfer in the horizontal direction and the convection as well as the radiation, the thermal model is simplified into one dimension, which is called 1D thermal model.

Two different thermal equivalent circuit models named continued-fraction circuit and partial-fraction circuit are introduced in [48]. The continued-fraction circuit reflects the physical layers of the semiconductor and the RC elements can be assigned to each layer while the partial-fraction circuit is just an mathematical equivalent model. The nodes in the partial-fraction circuit do not have any physical meaning. The inside thermal parameters of a power MOSFET are provided by the manufactures but the thermal parameters of the outside layers of the MOSFET can only be estimated according to the selected heatsink. Hence, the continued-fraction circuit is used in this project to do the thermal model because the physical significance of each layer.

The thermal circuit used for thermal modelling in this project is shown in the Figure 3.31. In the Figure 3.31, $R_{\theta jcn}$ and $C_{\theta n}$ are the thermal resistance and thermal capacitance of each layer inside the MOSFET and the $R_{\theta jc}$ is the total internal thermal resistance which is called junction-to-case thermal resistance. The case-to-heatsink thermal resistance $R_{\theta cs}$ and the heatsink-to-air thermal resistance $R_{\theta sa}$ are the external thermal resistance. $C_{\theta c}$ is the case thermal capacitance and $C_{\theta s}$ is the thermal capacitance of the heatsink.

The internal thermal parameters of the three SiC MOSFET candidates are shown in the Table 3.5. All the internal thermal parameters are provided by the datasheets [45–47]. The case thermal capacitance $C_{\theta c}$ is decided by the thermal interface material (TIM) and can be calculated by the equation [49]:

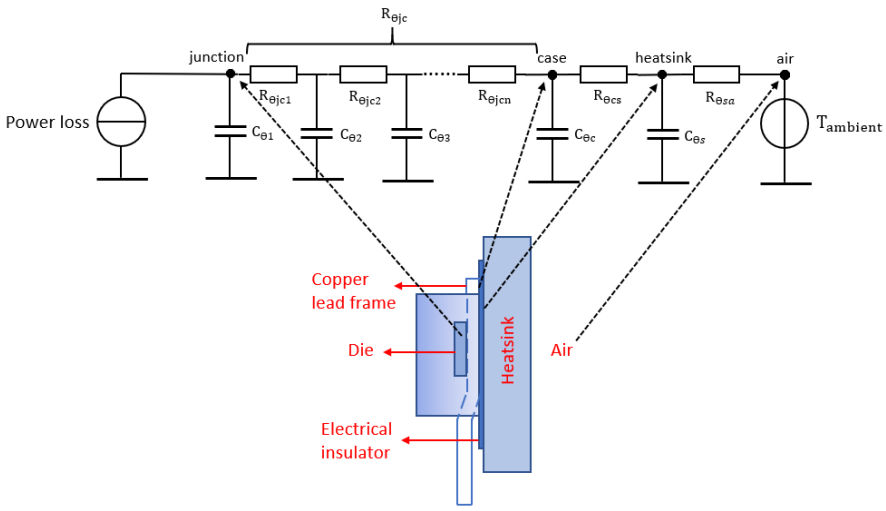


Figure 3.31: The thermal circuit used in this project

$$C_{\theta c} = mc_p \tag{3.52}$$

where the $m(kg)$ is the mass of the TIM and the $c_p(J/kg \cdot K)$ is the specific heat capacity of the TIM. The thermal resistance $R_{\theta cs}$ is influenced by the package and the typical value of TO-247 is provided in [50], which is $0.4K/W$. The thermal resistance of the heatsink can be read from the datasheet of the heatsink and the thermal capacitance can be calculated by using the equation 3.52. In all the simulations in this thesis, the $R_{\theta sa}$ is set as $0.6K/W$ when two MOSFETs connected in parallel and $0.4K/W$ when three MOSFETs connected in parallel.

Table 3.5: The internal thermal parameters of the three SiC MOSFET candidates

	Thermal resistance (K/W)				Thermal capacitance (J/K)			
	$R_{\theta jc1}$	$R_{\theta jc2}$	$R_{\theta jc3}$	$R_{\theta jc4}$	$C_{\theta 1}$	$C_{\theta 2}$	$C_{\theta 3}$	$C_{\theta 4}$
C3M0075120K	25e-3	59.2e-3	498e-3	469e-3	0.369e-3	1.22e-3	3.926e-3	355.2e-3
C2M0040120D	25.8e-3	85.72e-3	84.23e-3	182.4e-3	6.342e-3	16.45e-3	112e-3	358.6e-3
C2M0025120D	31.8e-3	74.1e-3	49.9e-3	113e-3	6.89e-3	19.3e-3	76.7e-3	235e-3

3.4.4. Performance evaluation of the MOSFET candidates

The relationship between the power loss and the junction temperature of the MOSFET is:

$$P_{loss} = \frac{T_j - T_a}{R_{\theta ja}} \tag{3.53}$$

where T_j is the junction temperature of the MOSFET, T_a is the ambient temperature and $R_{\theta ja}$ is the junction-to-ambient thermal resistance which is equal to the sum of $R_{\theta jc}$, $R_{\theta cs}$ and $R_{\theta sa}$.

Based on the built power loss model and the thermal model of the switches, the performance in terms of the power losses and the maximum junction temperature can be evaluated to check the feasibility of the design.

Due to the turn ratio of the transformer in this project is $2:1$, the current rating of the secondary side switches is much higher than the primary side switches, which means the conducting losses of the secondary side switches are much higher than the primary side switches. Besides, although the zero voltage turn-on of all the switches is realized, there are still turn-off losses. It can be seen from the equation 3.48 that the turn-off losses are not only related to the current but also related to the voltage on the MOSFETs. Hence, it is obvious that the worst case of the power loss will happen on the secondary side switches when the DC blocking capacitor voltage control is used since even the current level of the secondary side switches is almost the same with that when the DC blocking capacitor voltage control is not used but the voltage level is much higher. To evaluate which SiC MOSFET is more suitable for this project and to decide whether two-parallel-MOSFETs or three-parallel-MOSFETs

solution should be used, the power loss and temperature tests are done to the S6 and S8 in two cases (the first one is when the input voltage is $600V$, the PV voltage is $300V$ and the output voltage is $611.4V$, the second case is when the input voltage is $600V$, the PV voltage is $470V$ and the output voltage is $611.4V$) which are chosen according to the peak and RMS current got from the simulation results of the boundary cases. The test results of the two cases are shown in the Table 3.6 - Table 3.10 and the statistic histograms are drawn based on the data in these tables, which are shown in the Figure 3.32 and Figure 3.33. In order to distinguish the results of two parallel MOSFETs and three parallel MOSFETs, the additional subscript "d" is used to represent the two-parallel-MOSFETs case and the additional subscript "t" is used to represent the three-parallel-MOSFETs case. The total loss in the following tables means the total loss of the two or three paralleled MOSFETs and the maximum junction temperature is the maximum junction temperature of one of the paralleled MOSFETs.

Table 3.6: The test results of S6 in case 1

	Total loss(W)		Maximum junction temperature($^\circ C$)	
	$P_{total-d}$	$P_{total-t}$	$T_{j,max-d}$	$T_{j,max-t}$
C3M0075120K	60.65	39.92	104.90	59.95
C2M0040120D	66.27	48.38	90.34	56.75
C2M0025120D	37.88	28.57	60.26	42.71

Table 3.7: The test results of S6 in case 2

	Total loss(W)		Maximum junction temperature($^\circ C$)	
	$P_{total-d}$	$P_{total-t}$	$T_{j,max-d}$	$T_{j,max-t}$
C3M0075120K	49.64	34.83	90.00	55.30
C2M0040120D	65.27	54.49	89.26	60.75
C2M0025120D	44.50	31.09	66.42	44.26

Table 3.8: The test results of S8 in case 1

	Total loss(W)		Maximum junction temperature($^\circ C$)	
	$P_{total-d}$	$P_{total-t}$	$T_{j,max-d}$	$T_{j,max-t}$
C3M0075120K	95.64	52.86	151.98	71.78
C2M0040120D	61.04	32.81	85.46	46.65
C2M0025120D	31.76	19.84	54.68	37.36

Table 3.9: The test results of S8 in case 2

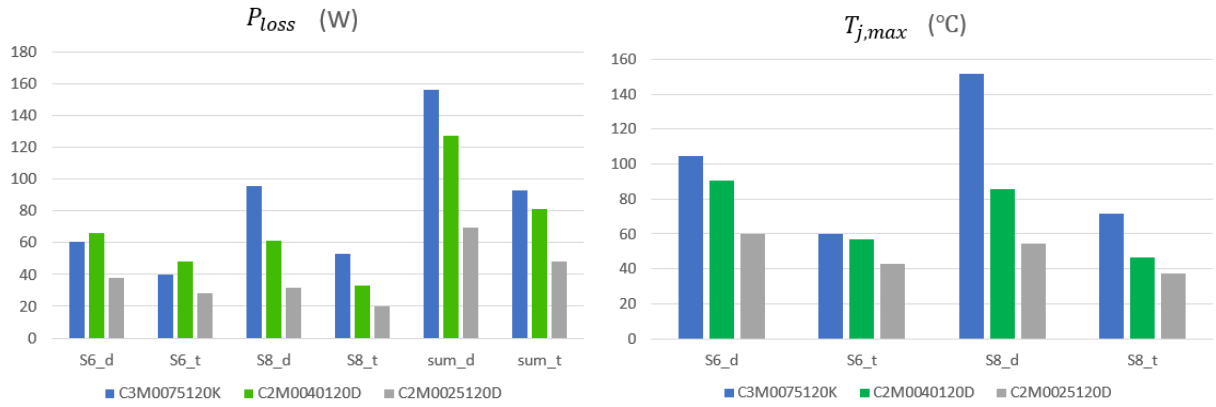
	Total loss(W)		Maximum junction temperature($^\circ C$)	
	$P_{total-d}$	$P_{total-t}$	$T_{j,max-d}$	$T_{j,max-t}$
C3M0075120K	56.54	40.05	100.10	60.40
C2M0040120D	44.73	29.17	69.29	44.25
C2M0025120D	28.45	16.49	51.59	35.28

Table 3.10: The sum of the total losses of S6 and S8

	Case 1		Case 2	
	P_{sum-d}	P_{sum-t}	P_{sum-d}	P_{sum-t}
C3M0075120K	156.29	92.78	106.18	74.88
C2M0040120D	127.31	81.19	110.00	83.66
C2M0025120D	69.64	48.41	72.95	47.58

According to the information in the Figure 3.32 and Figure 3.33, several conclusions can be got:

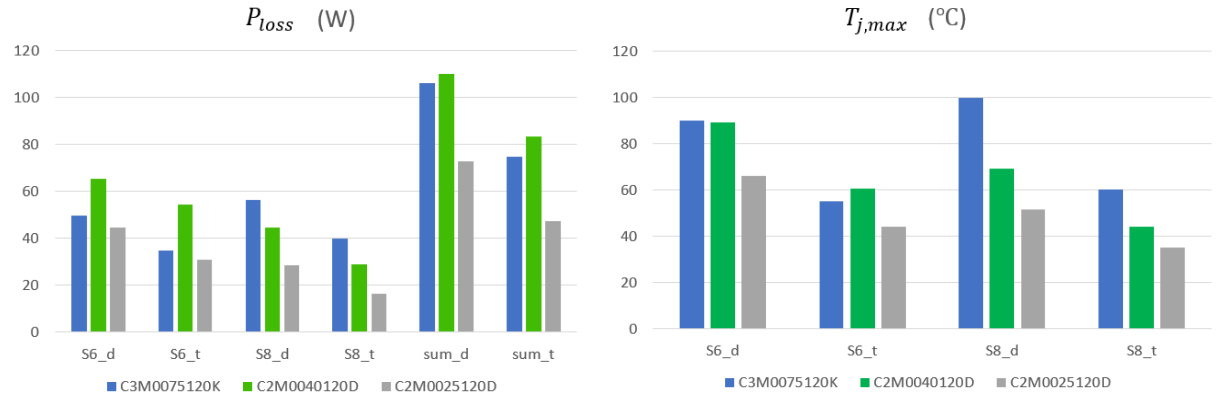
- Compare the simulation results of the two-parallel MOSFETs and the three-parallel MOSFETs, it can be seen that adding one more paralleled MOSFET can obviously reduce the total losses since the conduction losses are reduced by the reduced on-resistance and the switching losses are reduced by the reduced current. However, this does not mean that the more paralleled MOSFETs the better because the gate driver losses are ignored here, the gate driver losses will be increased by increasing the number of the paralleled MOSFETs. Besides, the design difficulty of the hardware part will become larger and larger with the increasing number of the paralleled MOSFETs since it is difficult to guarantee that all the paralleled MOSFETs can be switched simultaneously and have the balanced current sharing.



(a) Power loss results

(b) Temperature results

Figure 3.32: The statistic histogram of case 1



(a) Power loss results

(b) Temperature results

Figure 3.33: The statistic histogram of case 2

- According to the simulation results of the power losses of S6 and S8, it can be seen that the power losses of S8 are decreasing with the reduced on-resistance but the power losses of S6 are not always following this rule. This is because there is no turn-off loss in the losses of S8 since the DC blocking capacitor voltage control is used when the output voltage is larger than $600V$, so the power losses are only decided by the on-resistance. However, the total power losses of S6 are not only related to the on-resistance but also related to the turn-off energy and the turn-off energy of C2M0040120D is more than two times that of C3M0075120K which results in the larger total losses of S6 when the C2M0040120D is used even its on-resistance is smaller than that of the C3M0075120K.

- Another point is that it can be seen from the Figure 3.32a and Figure 3.32b that the maximum junction temperature of C2M0040120D is lower than that of the C3M0075120K even though the power loss of it is larger than that of C3M0075120K. This is because that the junction-to-case thermal resistance of C2M0040120D is smaller than that of the C3M0075120K.

- It can be seen from the Figure 3.32 that the maximum junction temperature of C3M0075120K will excess the maximum allowable value ($150°C$) when connecting two in parallel and the sum of the total power losses of S6 and S8 will be larger than $80W$ even when connecting three of them in parallel, which is too much from the efficiency point of view. As for the C2M0040120D, it can

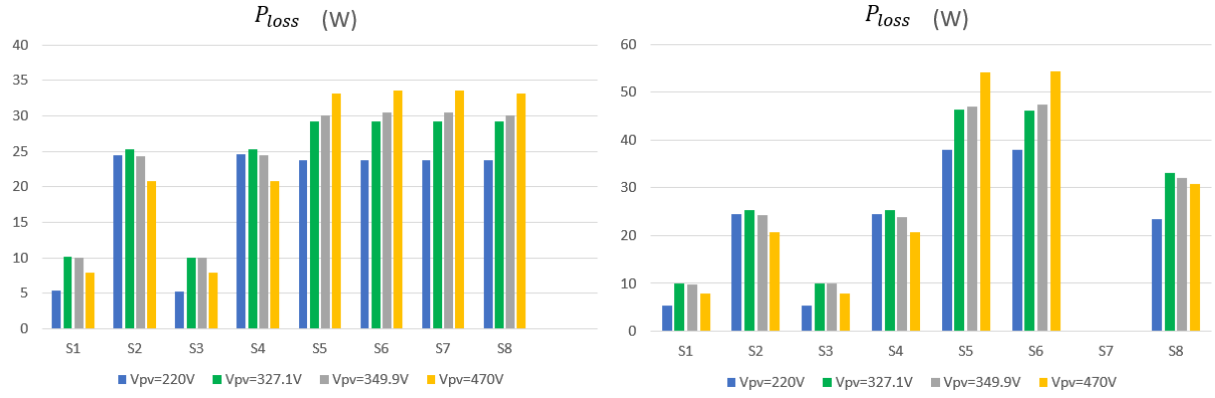
be seen from the Figure 3.32 and Figure 3.33 that the sum of the total losses of S6 and S8 will also be larger than $80W$ even connecting three in parallel. Hence, the most suitable SiC MOSFET for this project is C2M0025120D. From the efficiency point of view, the three-parallel-MOSFETs is the best solution for this project but from the cost and the difficulty of the hardware design points of view, the two-parallel-MOSFETs is the better solution. Hence, the SiC MOSFET C2M0025120D and the two-parallel-MOSFETs solution are chosen in this project.

3.4.5. Loss evaluation

In this dual boost integrated DAB converter, the losses on the different switches are different because of the following reasons:

- For the primary side switches, the losses are different among different switches because the duty cycle of the upper switches is different from that of the lower switches in the same leg since the duty cycle of the lower switches is decided by the PV voltage.
- For the secondary side switches, the losses are different among different switches when the DC blocking capacitor voltage control is used since the full bridge secondary side will be changed to the half bridge structure and there is no loss on the S7. S5 and S6 have both turn-off losses and conduction losses but S8 only has conduction losses.

The loss breakdown of all the switches in this converter with different power modes when the DC blocking capacitor voltage control is not used (the input voltage is 654.2V and the output voltage is 333.3V) and when it is used (the input voltage is 654.2V and the output voltage is 666.6V) are shown in the Figure 3.34 - Figure 3.37. The PV port is not used in the power mode 2 and power mode 5 due to the illumination is not enough. The loss ratios ($Q_{sw} = \frac{P_{total}}{P_{out}}$) of the total losses of all the switches in different cases are shown in the Table 3.11 in which the ratio is calculated by using the total losses of the switches to divide the power transferred to the EV port when the converter is working in the charging mode and to divide the power transferred to the DC bus port when it is working in the discharging mode. The PV voltage is $100V$ is the case when the PV port is not used since $100V$ is smaller than the start-up voltage ($200V$) of the PV port set in the control loop.



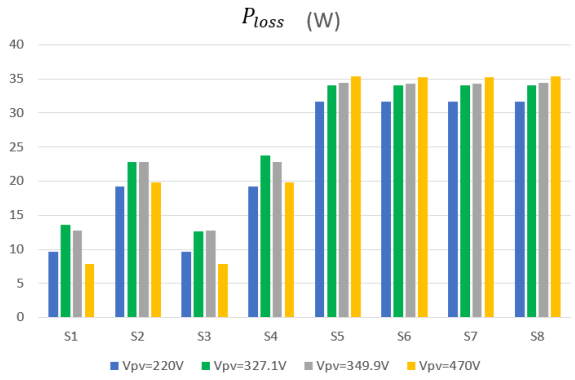
(a) Loss breakdown when the DC blocking capacitor voltage control is not used

(b) Loss breakdown when the DC blocking capacitor voltage control is used

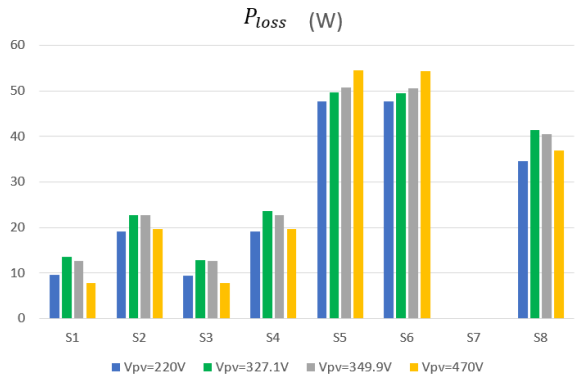
Figure 3.34: The loss breakdown of power mode 1 and 3

The following conclusions can be drawn according to the information in the Figure 3.34 - Figure 3.37 and the Table 3.11:

- It can be seen from the Figure 3.34 - Figure 3.37 that the losses on the primary side switches are almost the same when the DC blocking capacitor voltage control is used with that when the DC blocking capacitor voltage control is not used since the current and voltage of the primary side switches are mainly decided by the input voltage, PV voltage and the voltage gain ($\frac{nV_o}{V_{in}}$). The

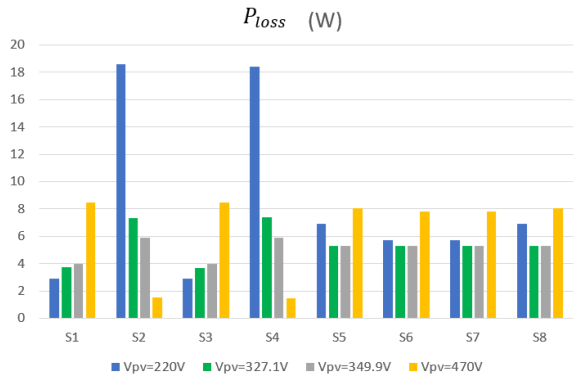


(a) Loss breakdown when the DC blocking capacitor voltage control is not used

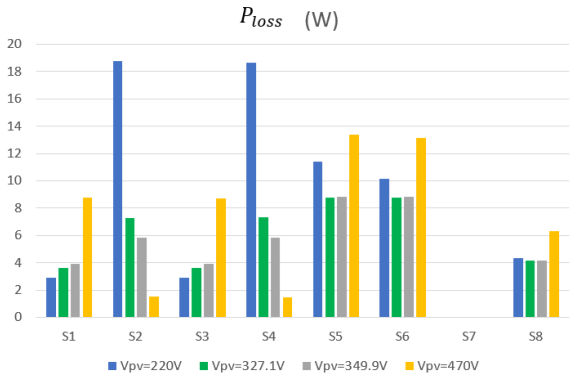


(b) Loss breakdown when the DC blocking capacitor voltage control is used

Figure 3.35: The loss breakdown of power mode 4

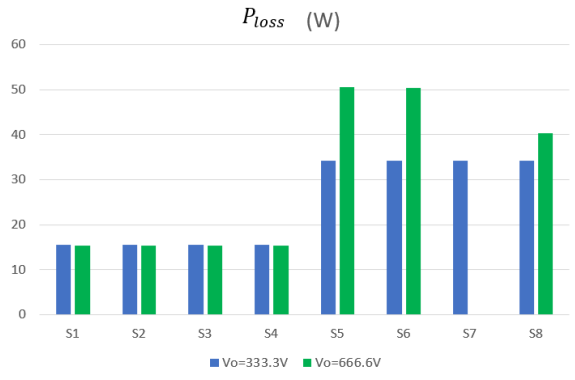


(a) Loss breakdown when the DC blocking capacitor voltage control is not used

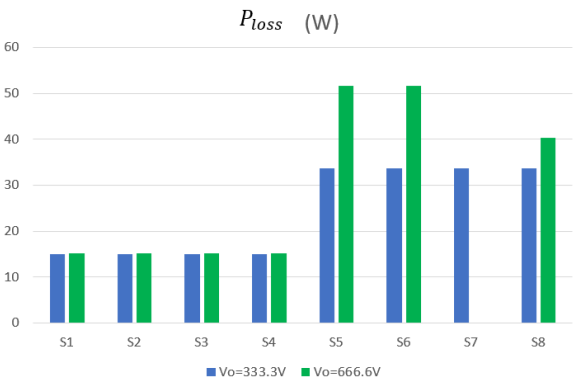


(b) Loss breakdown when the DC blocking capacitor voltage control is used

Figure 3.36: The loss breakdown of power mode 6



(a) Loss breakdown of power mode 2



(b) Loss breakdown of power mode 5

Figure 3.37: The loss breakdown of power mode 2 and 5

Table 3.11: The loss ratio of the different power modes

	Power mode 1 and 3		Power mode 2		Power mode 4		Power mode 5		Power mode 6	
	$333.3V$	$666.6V$	$333.3V$	$666.6V$	$333.3V$	$666.6V$	$333.3V$	$666.6V$	$333.3V$	$666.6V$
$V_{pv} = 100V$	-	-	2.03%	2.06%	-	-	2.03%	2.08%	-	-
$V_{pv} = 220V$	1.73%	1.76%	-	-	2.10%	2.14%	-	-	0.69%	0.70%
$V_{pv} = 327.1V$	1.89%	1.97%	-	-	2.13%	2.17%	-	-	0.44%	0.44%
$V_{pv} = 349.9V$	1.93%	1.98%	-	-	2.14%	2.18%	-	-	0.42%	0.42%
$V_{pv} = 470V$	2.71%	2.72%	-	-	2.52%	2.57%	-	-	0.53%	0.54%

voltage gain when the output voltage is $666.6V$ is the same with that when the output voltage is $333.3V$ due to the import of the DC blocking capacitor voltage control.

- Compare the loss breakdown in the Figure 3.34 with that in the Figure 3.35, it can be seen that the difference between the losses on S1 (S3) and S2 (S4) is smaller when the EV battery is charged by the PV power ($5kW$) and the power from the DC bus ($5kW$) than that when the EV battery is charged only by the PV power ($10kW$) since the difference of the RMS current and the difference of the peak current between S1 (S3) and S2 (S4) are smaller when the EV battery is charged by the PV power ($5kW$) and the power from the DC bus ($5kW$).

- It can be seen from the Figure 3.34 and the Figure 3.35 that the loss variation of S8 with different PV voltage is different with that of other secondary side switches when the DC blocking capacitor voltage control is used when the converter is working in the charging mode since the power loss of S8 when the DC blocking capacitor voltage control is used only includes the conduction loss. The current flowing through the secondary side switches is only related to the leakage current (i_{lk}) which can decide how much power can be transferred from the primary side to the secondary side. According to the conclusion got from the Section 2.4 (the output power increases when the absolute value of $D - 0.5$ decreases if the input and output voltages are the same), the RMS current of the secondary side switches increases when the absolute value of $D - 0.5$ decreases if the input and output voltages are the same, which means the conduction losses will also be increased when the absolute value of $D - 0.5$ decreases. Therefore, the conduction loss of the secondary side switches is the largest when the duty cycle of the primary side switches is 0.5. Hence, the power loss of S8 is the largest when the duty cycle of the primary side switches is 0.5 compared with that when the duty cycle of the primary side switches is not 0.5 when the DC blocking capacitor voltage control is used. The power loss of S8 when the PV voltage is $470V$ in the case when the DC blocking capacitor voltage control is used is larger than that when the PV voltage is $220V$ even though the output power of the latter case is larger than that of the former case since the circulating power is larger when the PV voltage is $470V$ than that when the PV voltage is $220V$. However, the power losses of other switches are composed of the conduction loss and the switching loss (the turn-off loss in this project). The turn-off losses of the switches are decided by the peak current when the switches are turned off if the voltage is the same. The peak current of the secondary side switches is increased with the increasing PV voltage when the output voltage is $333.3V$ and $666.6V$ according to the simulation results, which results in a larger turn-off loss when the PV voltage is increasing.

- The power losses on the switches are smallest in the Figure 3.36 compared with that in the other figures. The Figure 3.36 shows the loss breakdown of the switches when the converter is working in the discharging mode and the power is transferred from the EV port ($5kW$) and the PV port ($5kW$) to the DC bus port. In this case, only $5kW$ power is transferred from the secondary side to the primary side, the current stress of all the switches is much less than that in other cases (in which the power transferred between the primary and secondary sides is $10kW$), which means both the RMS current and the peak current of all the switches are less in this case. Therefore, the losses of all the switches are much less. This loss reduction is more obvious in the losses of the secondary side switches whose current is only decided by the leakage current which is determined by how much power is transferred between the primary and the secondary sides.

- The power losses of S2 and S4 are very large compared with the losses of other switches when the PV voltage is $220V$ in the Figure 3.36. This is because the zero voltage turn-on of S2 and S4 is lost in this case. The current flowing through S1 (S3) is negative when it is turned off

according to the simulation result, which means the sum of the current flowing through the boost inductors and the current flowing though the leakage inductance is positive. Therefore, there is no current flowing through the diode of the S2 (S4) before it is turned on, which means the ZVS is lost. As described in the last conclusion that the RMS current of all the switches are very small in this case, so the conduction losses of the switches are small. Besides, the turn-on energy of the C2M0025120D is larger than the turn-off energy which can be seen from the Figure 3.27. Hence, the power losses of S2 and S4 are much larger when the PV voltage is $220V$ compared with that of other switches.

- It can be seen from the Figure 3.37 that the power losses on the switches are almost the same when the converter is working in the charging mode with that when it is working in the discharging mode if the values of the DC bus voltage and the EV voltage are not changed in the two cases when the PV port is not used.
- It can be seen from the Table 3.11 that the loss ratio of the total losses on the switches when the output voltage is $666.6V$ has the same variation trend and almost the same value with that when the output voltage is $333.3V$ due to the import of the DC blocking capacitor voltage control. In most of the cases when the converter is working in the charging mode, charging the EV battery from both the PV port and the DC bus port has the largest loss ratio and charging the EV battery only from the PV port has the smallest loss ratio. The loss ratio of the power mode 6 (power is transferred from the EV battery and the PV port to the DC bus port) has the smallest loss ratio among all the cases.

To evaluate the losses on the switches of the dual boost integrated DAB converter with a large output voltage range, four loss ratio curves with different PV voltages when the converter is working in the power mode 1 and 3 are drawn, which are shown in the Figure 3.38. In the Figure 3.38, the case 1 is the case when the PV voltage is $220V$, the case 2 is the case of the PV voltage with which the duty cycle of all the primary side switches is 0.5, the case 3 is the boundary PV voltage which is got from the Figure 3.16 or calculated by the equation 3.43 and the case 4 is the case when the PV voltage is $470V$. When the output voltage is in the range of $479.25V - 600V$, the simulation test is done by reducing the PV power to realize the ZVS of all the switches in the converter.

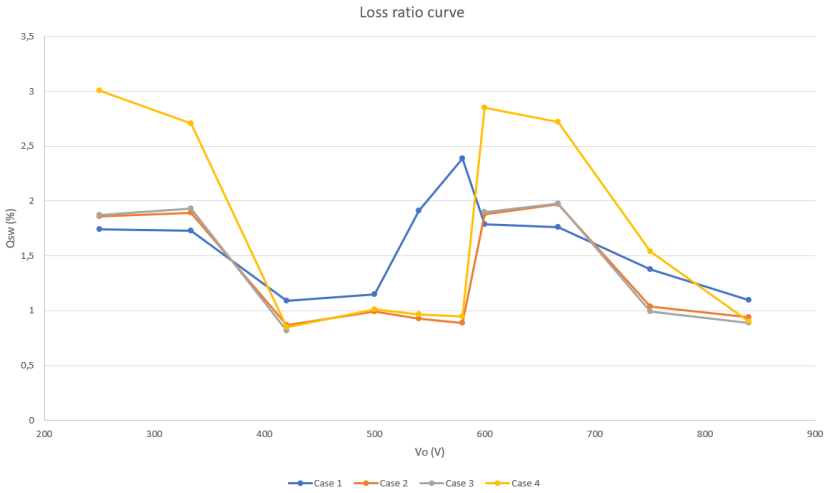


Figure 3.38: The loss ratio curves

According to the information in the Figure 3.38, the following conclusions can be drawn:

- The loss ratio curve of case 3 is very similar to that of case 2 since the boundary PV voltage is calculated to satisfy the requirement that the duty cycle of S2 and S4 is 0.465 once the voltage gain can be kept as 1.019, which is very close to 0.5.
- In most of the cases especially the critical working range (for the low voltage battery is $250V - 420V$ and for the high voltage battery is $666V - 840V$), the loss ratio is too high when the PV

voltage is $470V$ which is already out of the optimized working range in these cases. This result further verifies that the optimized working range deduced before is correct and meaningful. And there is a small period when the loss ratio is not so high in the mid of the loss ratio curve of case 4 since the input voltage is close to or already larger than $878.5V$, which means the PV voltage $470V$ is not out of the optimized working range.

- When the output voltage is increased from $333.3V$ to $420V$ or increased from $666.6V$ to $840V$, the decrease of the loss ratio of case 2 and case 3 is more drastic than that of the case 1 and this is because the decrease of both the RMS and peak current of all the switches of case 2 and case 3 when the output voltage is increased from $333.3V$ to $420V$ or increased from $666.6V$ to $840V$ is much larger than that of case 1.

- The peak loss ratio of case 1 is showing when the output voltage is $580V$ in the Figure 3.38 since the converter has the largest voltage gain at this case compared with other test points in this figure, which will result in a large leakage current. Therefore, the losses of the secondary side switches will be large. Besides, the PV power is reduced to $2499W$ in order to realize the ZVS of all the switches, which means a large amount of power needs to be drawn from the DC bus so the current stress on S1 and S3 will be larger. And the larger current stress will result in larger losses on S1 and S3.

- Last but not the least, it can be seen from the Figure 3.38 that the loss ratio is not continue rising with the increasing output voltage due to the introduce of the DC blocking capacitor voltage control.

3.5. Summary

In this chapter, the contents about the power loss modeling and analysis of the switches and the circulating power analysis of the dual boost integrated DAB converter are presented. Several important points need to be emphasized:

- The ZVS region of all the switches and the circulating power in the dual boost integrated DAB converter are calculated and programmed in the Mathcad. The developed programming is verified by the simulation results got from PLECS. The ZVS region and the circulating power of any customized design of the dual boost integrated DAB converter can also be checked by the developed Mathcad programming.

- It is hard to realize the ZVS of all the switches in the dual boost integrated DAB converter with a large voltage range which is required by this project and it can be seen from the analysis of the ZVS characteristics and the circulating power that the conditions to realize the ZVS of all the switches in this converter and the conditions to have the minimum circulating power are contrary in some cases. Therefore, the optimization method (DC blocking capacitor voltage control) is proposed and the optimized working range in terms of the DC bus voltage, PV voltage and the EV battery voltage is calculated to enlarge the ZVS region of the switches and reduce the circulating power. As a result, ZVS is able to be achieved in all the switches in the full operation range expect $200V \leq Vo \leq 300V$ and $479.25V < Vo \leq 600V$, and the circulating power is kept low.

- The power loss model and the thermal model of the SiC MOSFET candidates are built to evaluate the performance of different candidates and the most suitable one is chosen for this project according to the evaluation results. The simulation results might have some deviation even the PLECS simulation is used to make the modeling as precise as possible since the parasitic components of the PCB trace will also influence the losses on the switches.

- The losses on different switches are different in the dual boost integrated DAB converter, so the loss breakdown of different switches in different power modes is analyzed. Besides, the loss ratio curves are drawn according to the simulation results. It can be seen from the loss ratio curves that the performance of this converter with the large output voltage range is effectively improved by the optimization method and the calculated working range.

After all the principle analysis and the loss analysis of the dual boost integrated DAB converter are done, the experiment test is proceeded in the next chapter to verify the implementability of this converter and the previous analysis about this converter.

4

Experiment test

A test bench of the dual boost integrated DAB converter is built by modifying an existing CLLC converter in the lab. The CLLC resonant tank is removed and the third port which is connected to the PV panel is added by connecting the input capacitor (C_1 in the Figure 2.4) and the two boost inductors (L_1 and L_2 in the Figure 2.4). A new transformer and the additional inductor which is used to satisfy the leakage inductance requirement in this project as well as the DC blocking capacitors are also added. The Field Programmable Gate Array (FPGA) programming is developed to realize the open loop control of the converter.

4.1. Inductor design

The design of the two boost inductors in the primary side is critical for the achievement of the good performance of the whole converter. The specifications of the two boost inductors are shown in the Table 4.1.

Table 4.1: Boost inductor specifications

Parameters	Specifications
Maximum average current	$22.727A$
Maximum current ripple (p-p)	$9.091A$
Maximum peak current	$27.273A$
Switching frequency	$65kHz$
Required inductance	$0.2813mH$

To design an inductor, the first step is to choose the proper core material. There are two main commercial available core material for high power and high frequency application: gapped ferrite core and powder core. The powder core is selected in this project because of the following reasons:

- The gapped ferrite core often requires really low effective permeability to prevent saturation when the current is high. Since the initial permeability of ferrite is pretty high, it requires a relatively large air gap to get the low effective permeability. However, this large air gap results in a larger loss due to the fringing flux at the high switching frequency especially when the center gap is used. The powder core has the distributed air gap, so there is no fringing loss in the powder core.
- The powder core has the soft saturation characteristic which can be seen from the Figure 4.1.

  It can be seen from the Figure 4.1, the powder core has a gradual reduction in inductance when the current load is increasing. The gapped ferrite can keep the inductance almost unchanged before the saturation point. However, a sudden drop of the inductance can be seen once the saturation point is reached. Therefore, powder core is more suitable for the application with a high DC bias. The soft saturation characteristic also has advantages in terms of minimal temperature shift and natural fault tolerance, this makes the control and protection of the converter easier.

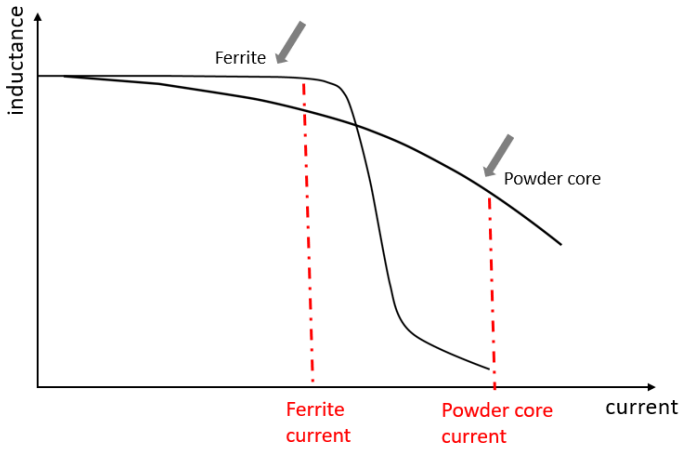


Figure 4.1: The soft saturation characteristic of the powder core

- The powder core has higher inherent saturation flux density compared with the ferrite core. And the elimination of the fringing flux makes it can work with higher switching frequency. The higher switching frequency, higher inherent saturation flux density and the soft saturation characteristics result in a large reduction of the inductor size.

The Kool Mμ E core "00K8020E040" is selected in this project and the powder core selection procedure is referred to the procedure in [2], which is summarized as:

- Calculate the product of LI^2, where L is the required inductance and I is the maximum average current.
- Choose the core based on the calculated value of LI^2 according to the Core Selection Chart which is shown in the Figure A.1. Choose the core which just lies above the diagonal permeability line at the calculated LI^2.
- Calculate the number of turns according to the following equation:

$$N = \sqrt{\frac{L * 10^6}{A_L}} \tag{4.1}$$

  where L is the required inductance (mH) and A_L is the inductance factor (nH/T^2) which can be read from the core data sheet. Considering the worst case, generally set a negative tolerance (-8%) to the value read from the data sheet. The calculated number of turns is the value needed to get the required inductance at no load.

- Calculate the DC bias according to the following equation:

$$H = \frac{NI}{l_e} \tag{4.2}$$

  where l_e is the path length which can also be read from the data sheet.

- Check the roll-off percentage of the initial permeability at the calculated DC bias according to the Permeability versus DC Bias Curves shown in the Figure A.2.
- Dividing the previously calculated number of turns by the roll-off percentage to get the required number of turns at the full load.
- Recalculate the inductance and the DC bias according to the required number of turns at the full load by using the equation 4.1 and equation 4.2, respectively.

- Calculate the inductance with the DC bias by computing the product of the calculated inductance and the roll-off percentage in the last step. This will result in an inductance which can satisfy the inductance requirement.
- Choose a proper wire based on the current level according to the Wire Table which is shown in the Figure A.3. In practical, it is better to keep the current density of the wire less than $600A/cm^2$.
- Check the winding factor by the equation:

$$F = \frac{NA_W}{W_A} \tag{4.3}$$

where A_W is the area of the wire which can be read from the Figure A.3 and W_A is the window area of the core which can be read from the core data sheet. A winding factor less than 60% means this is a manufacturable design.

After the basic design of the inductor is finished, there are still several parameters need to be checked: copper losses, core losses and the temperature rise of the inductor. The check process can be accelerated by using the inductor design tool provided by the company Magnetics. The test results of the designed boost inductor in this project are shown in the Figure 4.2.

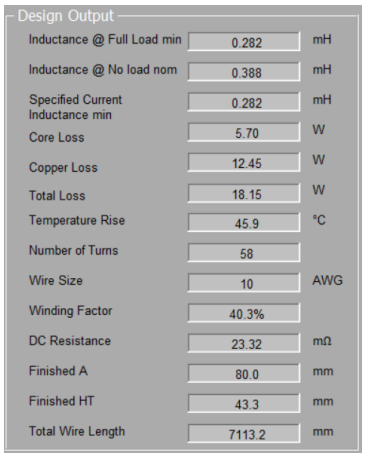


Figure 4.2: The check results of the designed boost inductor

4.2. FPGA programming

The open loop control (PWM generation) of the whole converter is implemented by the FPGA development board "Cora Z7-10", the programming language used is Verilog and the development software is Vivado. One of the simulation results (the duty cycle of the S1 and S3 should be 0.336, the duty cycle of S2 and S4 should be 0.664, the dead time should be $304ns$ and the phase shift between the S1 and S5 should be 0.1676) of the designed programming is shown in the Figure 4.3.

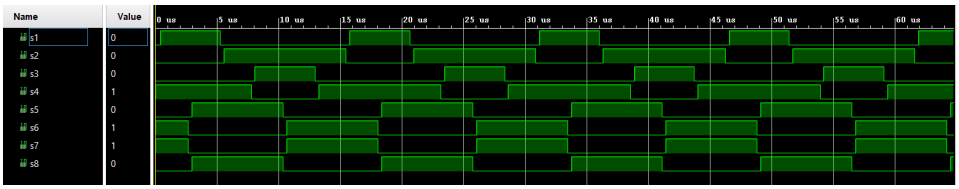
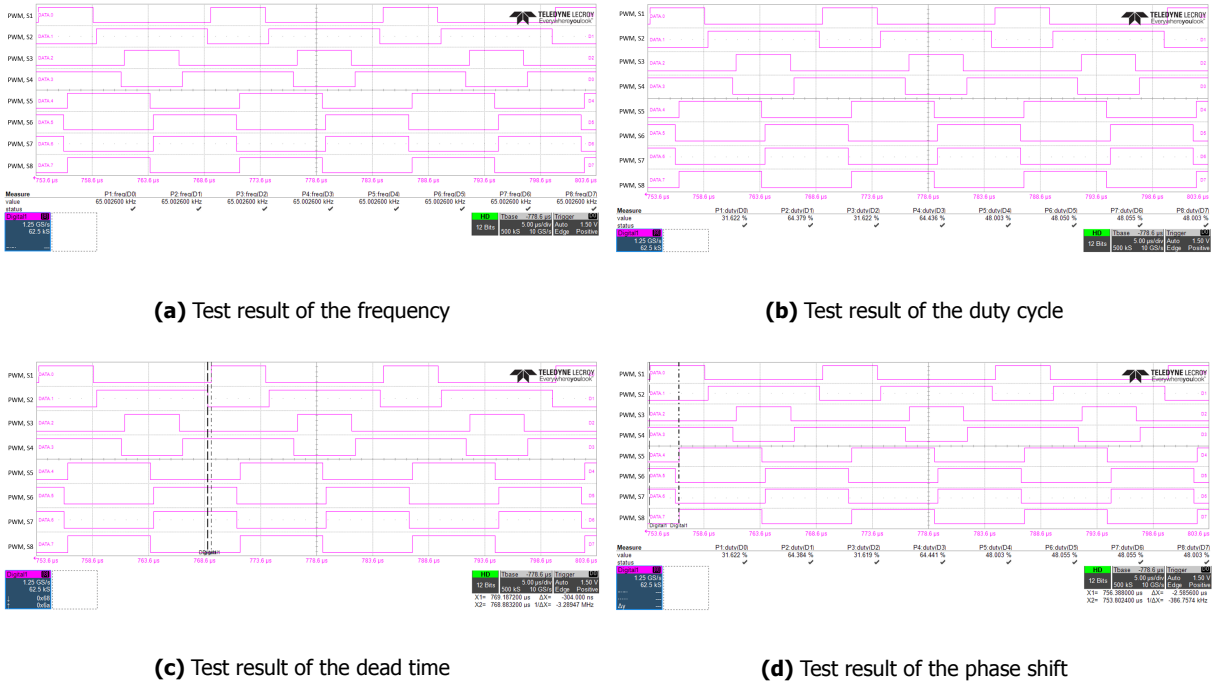


Figure 4.3: The Vivado simulation result of the designed programming

To further check the designed programming, the FPGA development board is connected to the oscilloscope to check the output signals. The test results are shown in the Figure 4.4.

It can be seen from the Figure 4.4a and Figure 4.4c that the test results of the switching frequency and the dead time are exactly the same as the supposed value. The phase shift between S1 and S5



(a) Test result of the frequency

(b) Test result of the duty cycle

(c) Test result of the dead time

(d) Test result of the phase shift

Figure 4.4: The test results of the FPGA signals

in the Figure 4.4d is $2.5856\mu s$ (which is $2.5856\mu s * 65kHz = 0.1681$) and the duty cycles of all the switches shown in the Figure 4.4b are 0.02 less than the expected values. The little difference of the phase shift and the duty cycle between the test values and the expected values is because of the import of the dead time.

4.3. Test of the original board

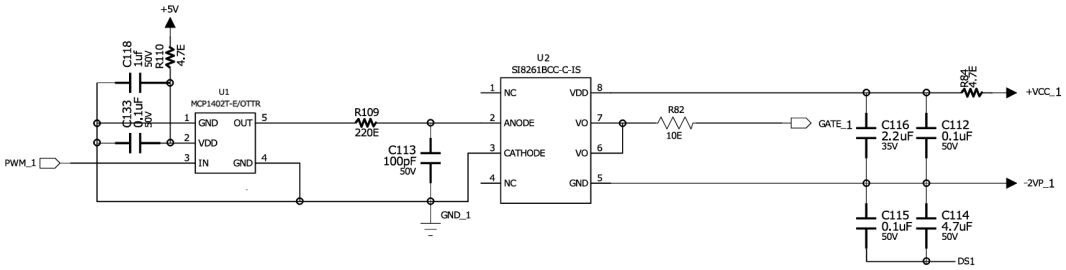
Before starting to do the modifications on the original board, it is prudential to perform the test of the board to verify the proper operation of the gate driver circuit and the dedicated power supply. Any error can then be identified at a much earlier stage of the experiment test.

The gate driver circuit in the original board is redrawn in the Figure 4.5. The MOSFETs are driven by an isolated gate driver (Si8261BCC-C-IS) which can support $4A$ peak output drive current with an input to output isolation of about $3.75kV$ [51]. The input current (I_F) flowing through the LED of the driver is followed by the output of the driver and it should be larger than $6mA$ to rise the output. A non-inverting buffer IC (MCP1402T-E/OTTR) is used to supply this current. The input of this buffer IC is connected to the FPGA development board. The output of the buffer IC is non-inverting and its maximum voltage is $5V$ [52]. The input current of the driver IC (Si8261BCC-C-IS) is limited by a current limiting resistor whose value can be calculated by the following equation:

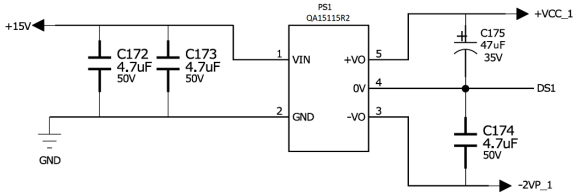
$$I_F = \frac{5 - V_F}{R_F} \tag{4.4}$$

where the I_F is the input current and V_F is the input forward voltage (ON) of the driver IC. The maximum value of V_F is $2.8V$ and the I_F should be larger than $6mA$. The current limiting resistor is selected as 220Ω which can limit the input current of the driver IC to $10mA$. The isolated dual polarity gate driver supplies generated by the isolated DC-DC converter module (QA15115R2) are used to prevent the unintentional turn-on of the MOSFETs. The QA15115R2 is powered by an external $15V$ power source and can generate a dual supply of $-2.5V$ and $+15V$ with a margin from -6% to 12% [53]. This dedicated power supply module also provides an isolation up to $3.5kV$.

The test setup for testing the gate driver circuit and the dedicated power supply of the original board is shown in the Figure 4.6. The PWM signals are generated by the FPGA board and sent to the input of the buffer IC (MCP1402T-E/OTTR). The test results are shown in the Figure 4.7 which shows the



(a) Gate driver ciruit



(b) Gate driver supply

Figure 4.5: The gate driver circuit

gate-source voltage of the S1, S2, S5 and S6. It can be seen that the switching frequency, duty cycle and the dead time are exactly the same with the digital signals shown in the Figure 4.4. The phase shift between the S1 and S5 is $2.5807\mu s$ (which is $2.5807\mu s * 65kHz = 0.1677$) which is very close to the expected value. The high-level voltage is around $15.8V$ and the low-level voltage is around $-2.8V$, which are within the range of the dual supply. The test results show that both the gate driver circuit and the dedicated power supply are working properly.

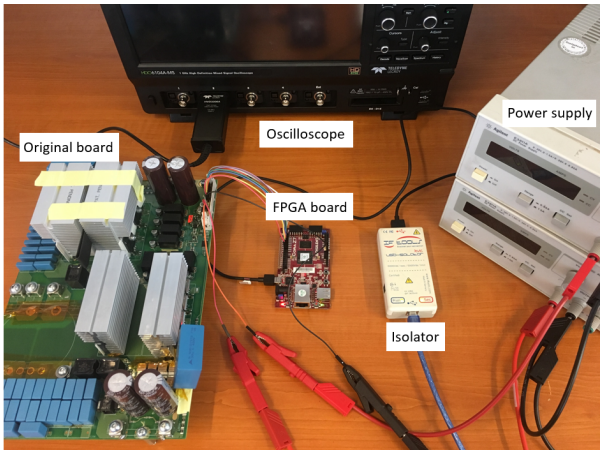
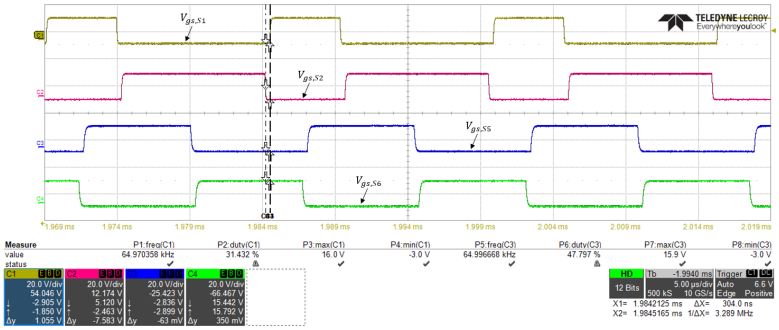


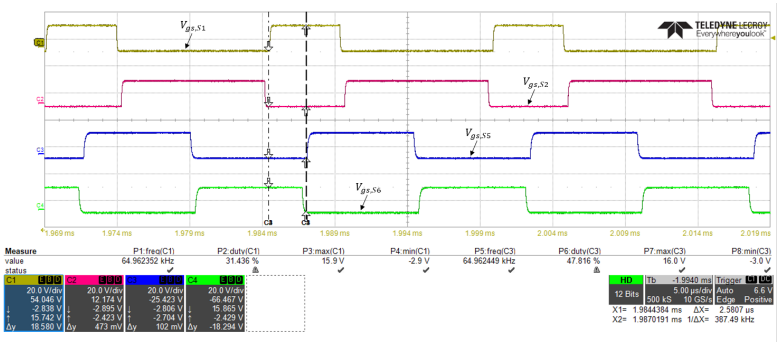
Figure 4.6: The test setup for testing the gate driver circuit and the dedicated power supply

4.4. Experimental results

Except the designed boost inductors whose parameters have been shown in the Section 4.1, the parameters of other main components used for the experiments are shown in the Table 4.2 and the test platform is shown in the Figure 4.8. The primary side DC blocking capacitor is not necessary if a control method is used to prevent the saturation of the transformer. All the tests are based on $2kW$ power.



(a) Dead time



(b) Phase shift between S1 and S5

Figure 4.7: Test results of the original board

Table 4.2: Parameters of the components used for the experiments

Parameters	Values
Turn ratio of the transformer	2:1
Leakage inductance	$86\mu H$
DC blocking capacitor primary side	$27.7\mu F$
DC blocking capacitor secondary side	$47\mu F$

4.4.1. Test results of the basic working principle

The waveforms of v_{ab}, v_{cd}, i_{lk} and i_{sec} which is the current flowing through the secondary side of the transformer in four different working cases are shown in the Figure 4.9.

The Figure 4.9a shows the waveforms when the duty cycle of the S2 and S4 is 0.5 and the phase shift δ is 0.05 ($V_{in} = 600V, V_{pv} = 300V$ and $V_o = 250V$), so $\frac{1}{2} - D \leq \delta < \frac{1}{2}$, which satisfies the condition of working case II shown in the Table 3.2. The Figure 4.9b shows the waveforms when the duty cycle of the S2 and S4 is 0.5 but the phase shift δ is 0.945 ($V_{in} = 600V$ and $V_o = 250V$), so $1 - D \leq \delta \leq 1$, which satisfies the condition of working case IV shown in the Table 3.2 and the power is transferred from the EV port to the DC bus port since the phase shift between the output voltages (v_{ab} and v_{cd}) of the primary and secondary side bridges (Φ) is $\Phi = \delta - \frac{1}{4} + \frac{1}{2}D = 0.945$ which is larger than 0.5. The Figure 4.9c shows the waveforms when the duty cycle of the S2 and S4 is 0.633 and the phase shift δ is 0.013 ($V_{in} = 600V, V_{pv} = 220V$ and $V_o = 250V$), so $0 \leq \delta < 1 - D$, which satisfies the condition of working case V shown in the Table 3.2. The Figure 4.9d shows the waveforms when the duty cycle of the S2 and S4 is 0.664 and the phase shift δ is 0.98 ($V_{in} = 654.2V, V_{pv} = 220V$ and $V_o = 333.3V$), so $\frac{3}{2} - D \leq \delta \leq 1$, which satisfies the condition of working case VIII shown in the Table 3.2. The phase shift between the S1 and S5 is 0.98 in the last case, which is actually the case when the phase shift δ is -0.02 but the phase shift between the output voltages (v_{ab} and v_{cd}) of the primary and secondary

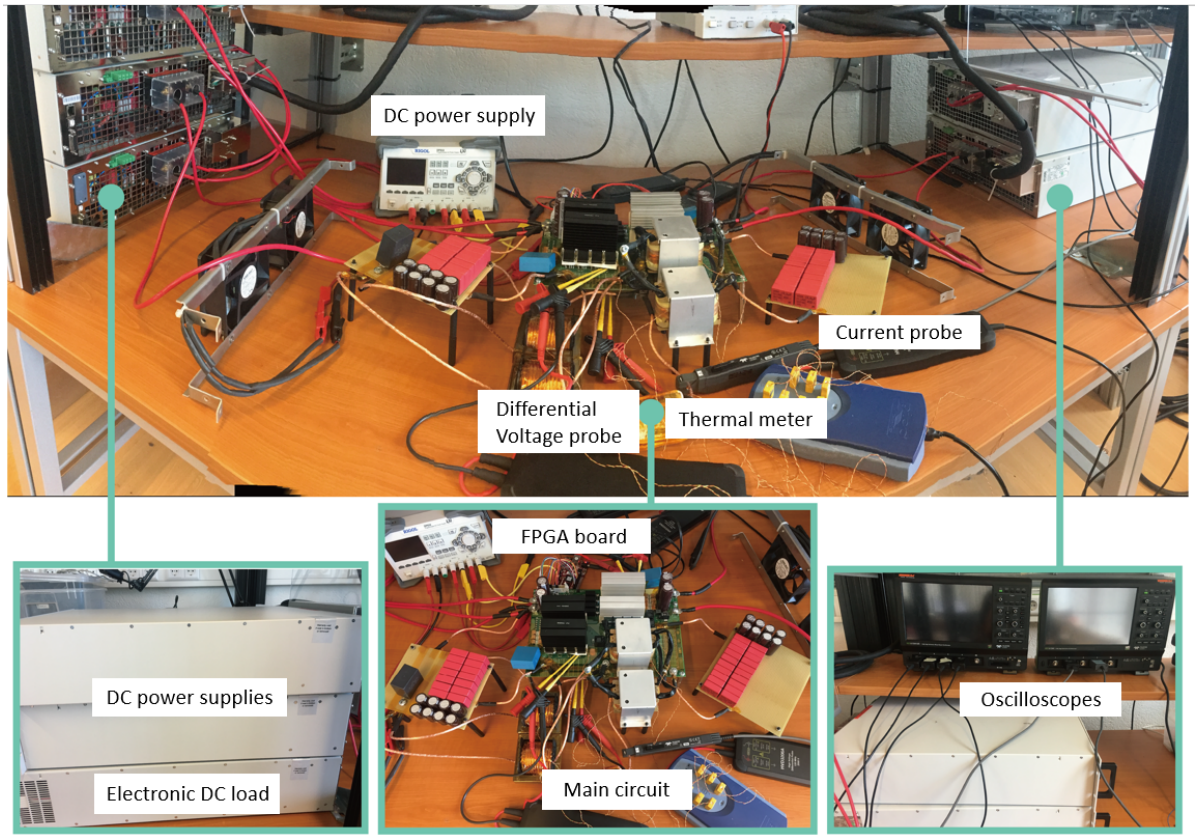


Figure 4.8: The test platform

side bridges (Φ) is $\Phi = \delta - \frac{1}{4} + \frac{1}{2}D = 0.062$ which is less than 0.5, so the power is still transferred from the primary side to the secondary side. It can be seen from the Figure 4.9 that the dual boost integrated DAB converter can work in different working cases according to the different duty cycle and phase shift. And the working waveforms are consistent with the previous analysis and the simulation results, which can verify the working principle analysis in the Chapter 2.

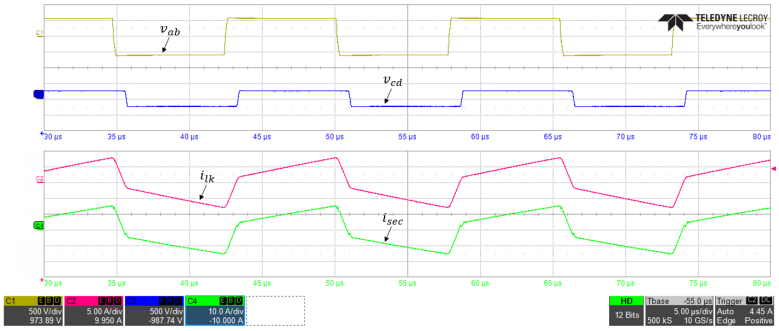
4.4.2. Test results of the effect of the interleaved structure

The test results of the waveforms of the current flowing through the two boost inductors and the total PV current with different duty cycles are shown in the Figure 4.10. It can be seen from the Figure 4.10 that the interleaved structure in the primary side of the dual boost integrated DAB converter can significantly reduce the ripple of the PV current. The closer the duty cycle is to 0.5, the smaller the PV current ripple and the PV current ripple is almost 0 when the duty cycle of the primary side switches is 0.5 since the phase shift between the two boost converters in the primary side of the dual boost integrated DAB converter is 50% (half switching cycle), which means i_{L1} is the maximum while the i_{L2} is minimum when the duty cycle of the primary side switches is 0.5. The test results are consistent with the analysis in the Chapter 2, which further verifies the conclusions got in the Chapter 2.

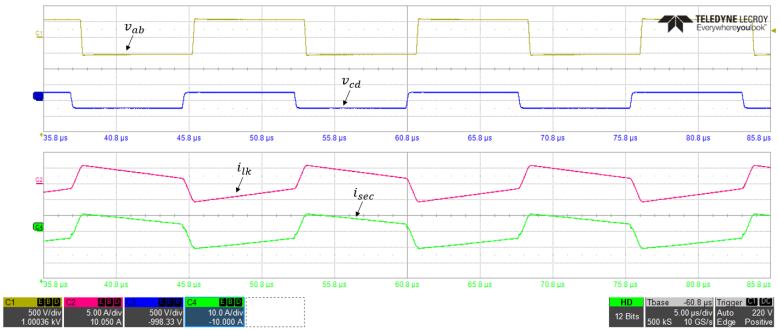
4.4.3. Test results of the DC blocking capacitor voltage control

In order to verify the optimization method (DC blocking capacitor voltage control) used to realize the ZVS of the switches in the dual boost integrated DAB converter with a large output voltage range, the waveforms of v_{ab}, v_{cd}, i_{lk} and i_{sec} as well as the gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) of S4 and S6 in the charging mode (S3 and S5 in the discharging mode) are measured. The reasons why the gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) of S4 and S6 in the charging mode (S3 and S5 in the discharging mode) are measured are:

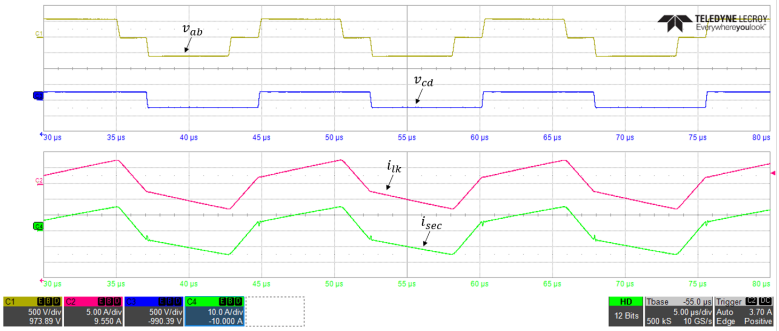
- It can be seen from the equation 3.1 to the equation 3.4 that the ZVS conditions of all the



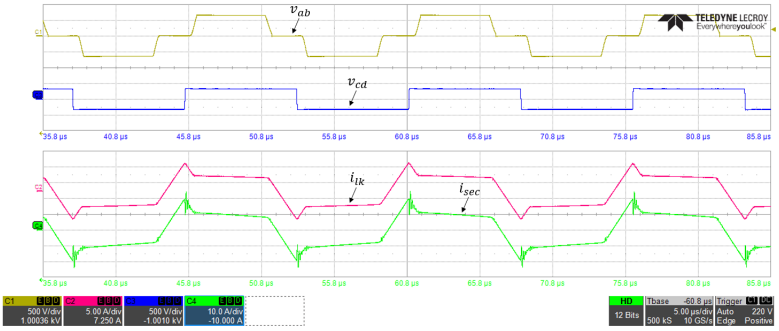
(a) Working case II



(b) Working case IV

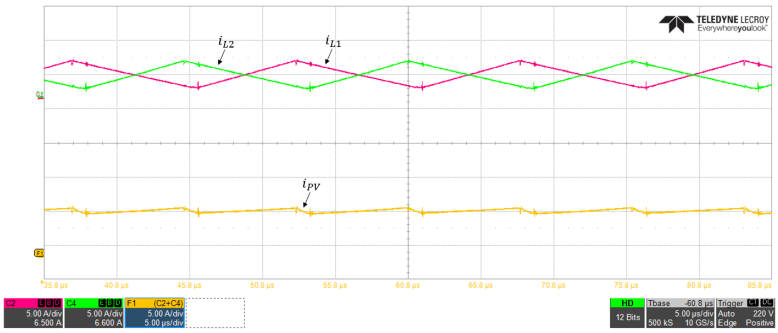


(c) Working case V

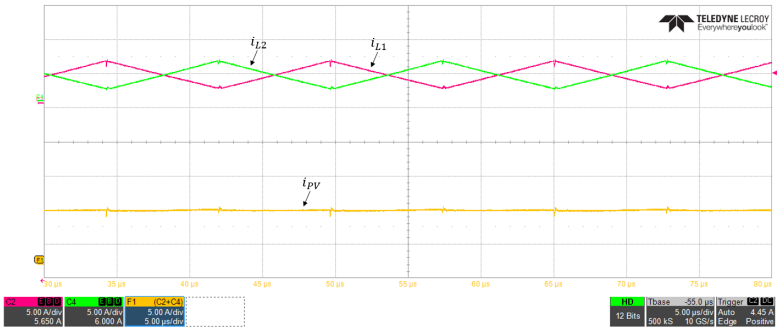


(d) Working case VIII

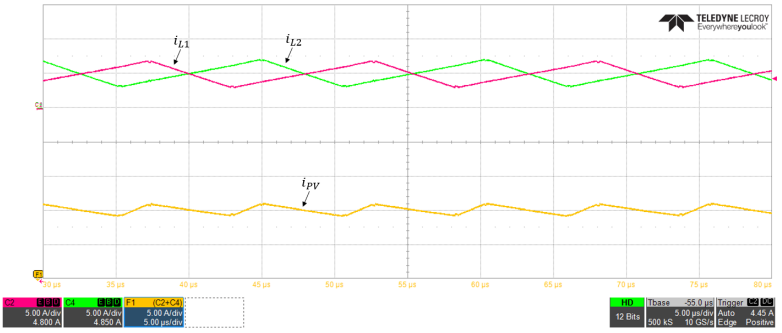
Figure 4.9: Experiment test results of different working cases



(a) $D = 0.465$



(b) $D = 0.5$



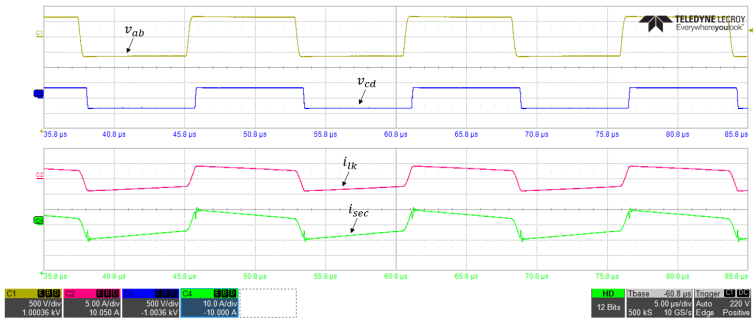
(c) $D = 0.633$

Figure 4.10: Experiment test results of the inductor current and the PV current with different D

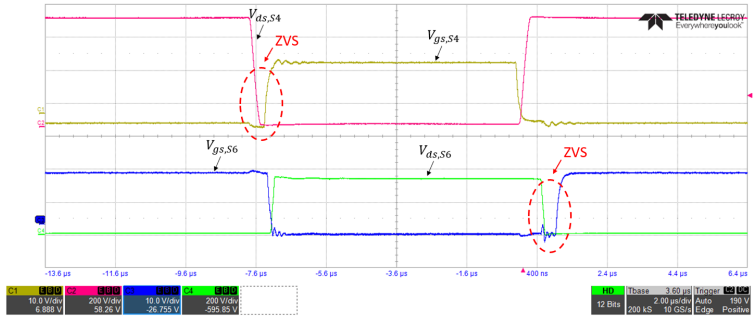
secondary side switches are the same, so once the ZVS of any one of the four switches in the secondary side is realized, the ZVS of all the secondary side switches of the dual boost integrated DAB converter can be realized.

- As for the primary side switches, according to the conclusion got in the Section 3.1.2 that the ZVS of the S1 and S3 is easier to be realized compared with that of S2 and S4 in the charging mode ($\Phi \leq 0.5$) and the ZVS of the S2 and S4 is easier to be realized compared with that of S1 and S3 in the discharging mode ($\Phi > 0.5$), so it is more necessary to test the ZVS of S2 and S4 in the charging mode and to test the ZVS of S1 and S3 in the discharging mode.

The test results when the DC blocking capacitor voltage control is not used ($V_{in} = 654.2V$ and $V_o = 333.3V$) and used ($V_{in} = 654.2V$ and $V_o = 666.6V$) in the charging mode (power is transferred from the DC bus port to the EV port) are shown in the Figure 4.11 and Figure 4.12, respectively. And the test results when the DC blocking capacitor voltage control is not used ($V_{in} = 654.2V$ and $V_o = 333.3V$)



(a) Waveforms of v_{ab}, v_{cd}, i_{lk} and i_{sec}



(b) Waveforms of V_{gs} and V_{ds} of S4 and S6

Figure 4.11: Test results when the DC blocking capacitor voltage control is not used in the charging mode

and used ($V_{in} = 654.2V$ and $V_o = 666.6V$) in the discharging mode (power is transferred from the EV port to the DC bus port) are shown in the Figure 4.13 and Figure 4.14, respectively.

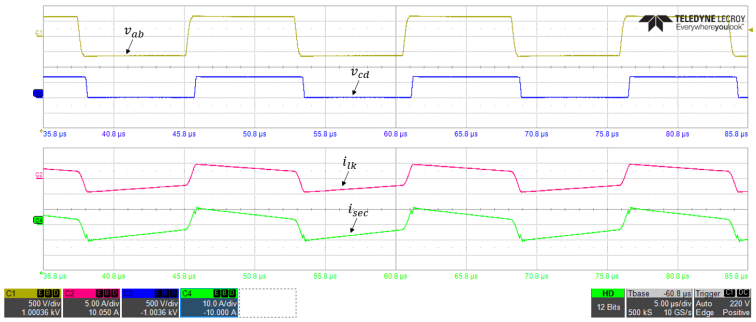
It can be seen that the primary side voltage of the case when the DC blocking capacitor voltage control is used is totally the same with that when the DC blocking capacitor voltage control is not used but the secondary side bridge voltage (v_{cd}) is changed from the pure AC voltage to the one with a DC component whose value is half of the output voltage according to the comparison of the Figure 4.11a and the Figure 4.12a. And the current flowing through the primary side and the secondary side of the transformer when the DC blocking capacitor voltage control is used is the same with that when the DC blocking capacitor voltage control is not used since the output voltage is doubled. Besides, it can be seen from the Figure 4.11b and the Figure 4.12b that the ZVS of all the switches can be realized in both cases (the voltage gain is around 1 and the voltage gain is around 2) due to the introduce of the DC blocking capacitor voltage control. It can be seen from the Figure 4.13 and the Figure 4.14 that the experiment results when the proposed converter works in the discharging mode have the same characteristic as that when it works in the charging mode. These results are consistent with the analysis in the Chapter 3, which can verify the conclusions got in the Chapter 3 are correct.

4.4.4. Test results of the ZVS region

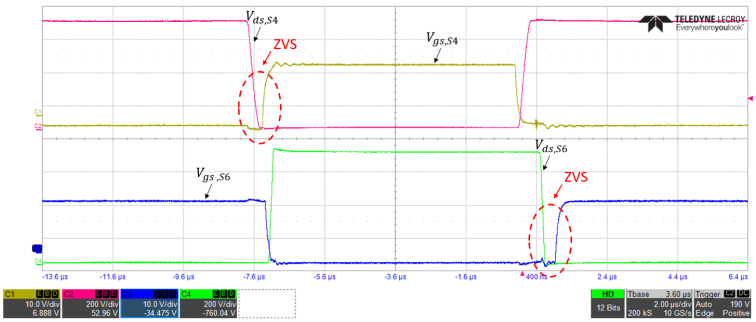
In order to verify the ZVS region and the optimized working range of the dual boost integrated DAB converter analyzed in the Chapter 3, the gate-source voltage (V_{gs}) and drain-source voltage (V_{ds}) of S4 and S6 in the charging mode (S3 and S5 in the discharging mode) with different input and output voltages in different power modes are measured.

The test results of the waveforms of V_{gs} and V_{ds} of S4 and S6 in power mode 1 (power is transferred from the PV port to the EV port) with the critical EV battery voltage range ($250V - 420V$) and higher EV battery voltage when the DC blocking capacitor voltage control is used are shown in the Figure 4.15 to the Figure 4.18.

According to the conclusions summarized in the Section 3.3.2 that When $200V \leq Vo \leq 300V$, the ZVS of primary side switches can be realized, but the ZVS of the secondary side switches cannot be



(a) Waveforms of v_{ab}, v_{cd}, i_{lk} and i_{sec}

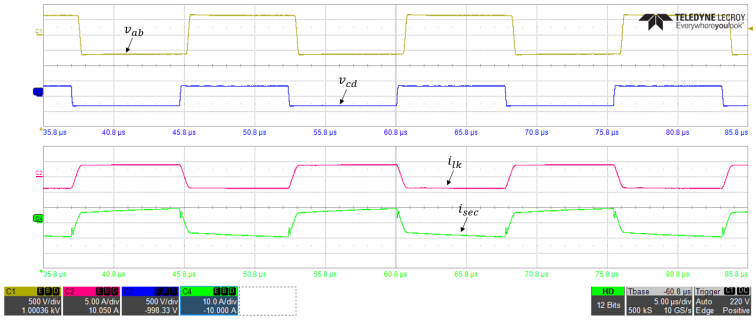


(b) Waveforms of V_{gs} and V_{ds} of S4 and S6

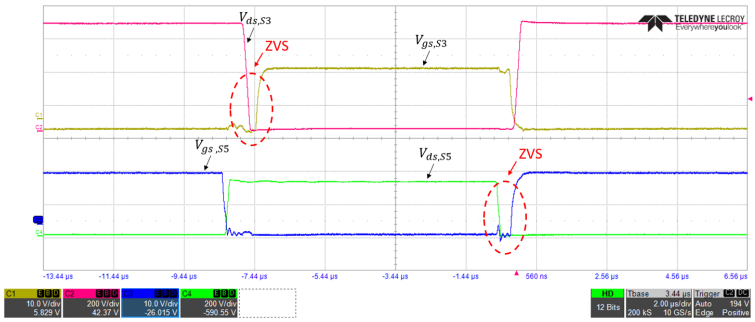
Figure 4.12: Test results when the DC blocking capacitor voltage control is used in the charging mode

realized in some cases once the duty cycle is larger than the minimum duty cycle calculated by the equation 3.43. The minimum D is 0.4 not 0.465 when $V_{in} = 600V$ and $V_o = 250V$ since the voltage gain is 0.833 not 1.019. The test results in the Figure 4.15 show that the ZVS of the primary side switches is realized when D is larger than 0.4 ($D = 0.633$ and $D = 0.5$) and it is lost when D is smaller than 0.4, which is consistent with the analysis. As for the secondary side switches, the phase shift δ is 0.013 when D is 0.633, which is working case V and the relationship between the phase shift and the duty cycle satisfies the ZVS condition of the secondary side switches in case V ($(4\delta + 2D + G - 2) > 0$), so the ZVS of the secondary side switches can also be realized as shown in the Figure 4.15a. The phase shift δ is 0.05 when D is 0.5, which is working case II and the relationship between the phase shift and the duty cycle satisfies the ZVS condition of the secondary side switches in case II ($(4\delta + 2D + G - 2) > 0$), so the ZVS of the secondary side switches can be realized as shown in the Figure 4.15b. The phase shift δ is 0.071 when D is 0.39, which is working case I and the relationship between the phase shift and the duty cycle satisfies the ZVS condition of the secondary side switches in case I ($(G - 2D) > 0$), so the ZVS of the secondary side switches can be realized as shown in the Figure 4.15c. The ZVS of both the primary and the secondary side switches can be realized when the EV battery voltage (V_o) is $333.3V$ or $420V$ once the duty cycle of S2 and S4 is larger than 0.465, which is the conclusion got in the Section 3.3.2. It can be seen from the Figure 4.16 and the Figure 4.17 that the ZVS of both the primary and the secondary side switches is realized when D is larger than 0.465 and the ZVS of the primary side switches is lost when D is less than 0.465, which is consistent with the analysis in the Section 3.3.2. When the EV battery voltage (V_o) is $840V$, the DC blocking capacitor voltage control is used, so ZVS condition of this case is totally the same with the case when the EV battery voltage is $420V$. It can be seen from the Figure 4.17 and the Figure 4.18 that the ZVS of the switches can also be realized even the voltage gain is doubled due to the introduce of the DC blocking capacitor voltage control.

The ZVS of the switches in the dual boost integrated DAB converter in other power modes is also verified by the experiment tests. The test results of the waveforms of V_{gs} and V_{ds} of S4 and S6 in power mode 2 (power is transferred from the DC bus port to the EV port and the duty cycle of the primary

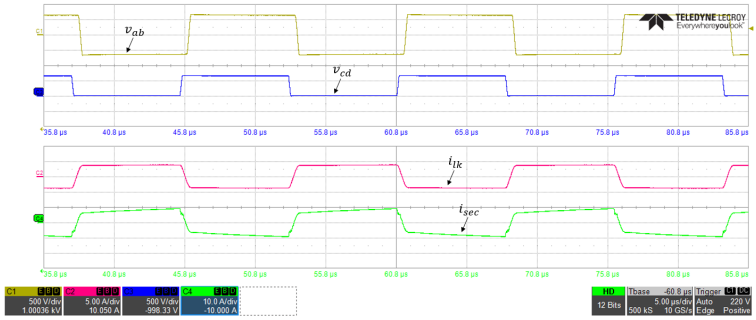


(a) Waveforms of v_{ab}, v_{cd}, i_{lk} and i_{sec}

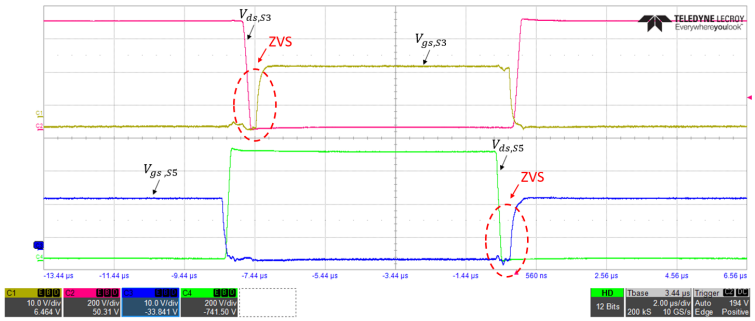


(b) Waveforms of V_{gs} and V_{ds} of S3 and S5

Figure 4.13: Test results when the DC blocking capacitor voltage control is not used in the discharging mode

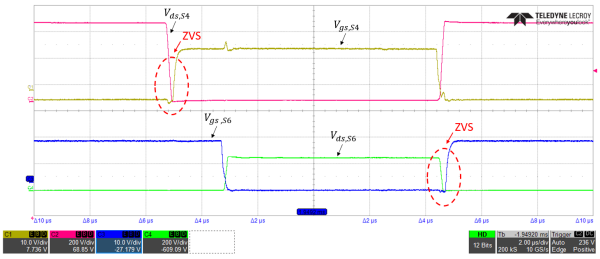


(a) Waveforms of v_{ab}, v_{cd}, i_{lk} and i_{sec}

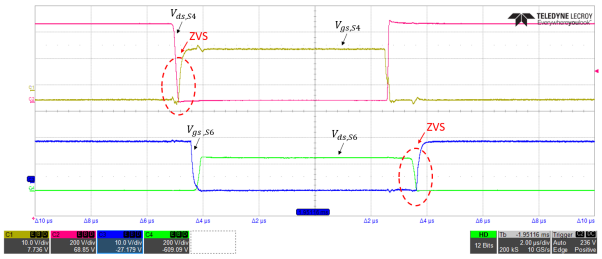


(b) Waveforms of V_{gs} and V_{ds} of S3 and S5

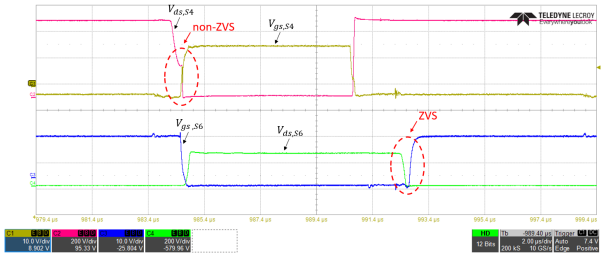
Figure 4.14: Test results when the DC blocking capacitor voltage control is used in the discharging mode



(a) $D = 0.633$ $(V_{pv} = 220V)$

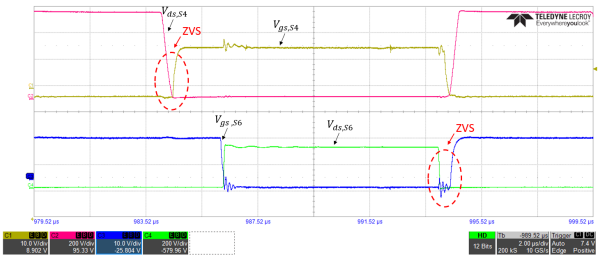


(b) $D = 0.5$ $(V_{pv} = 300V)$

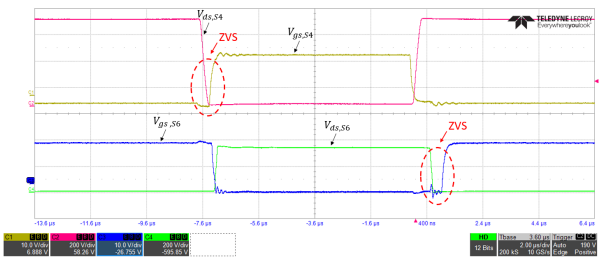


(c) $D = 0.39$ $(V_{pv} = 366V)$

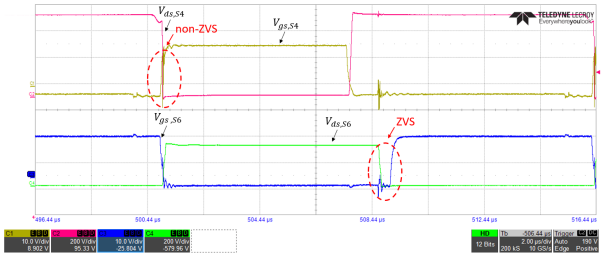
Figure 4.15: Test results of power mode 1 when $V_{in} = 600V$ and $V_o = 250V$



(a) $D = 0.664$ $(V_{pv} = 220V)$



(b) $D = 0.5$ $(V_{pv} = 327.1V)$

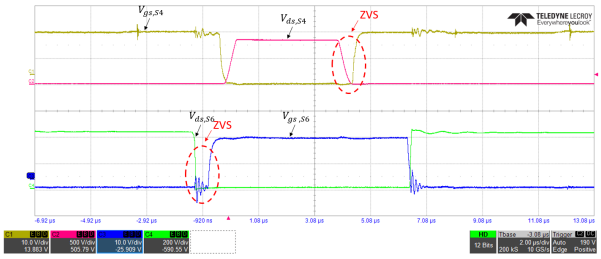


(c) $D = 0.45$ $(V_{pv} = 360V)$

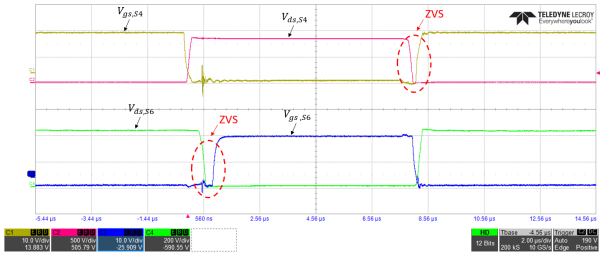
Figure 4.16: Test results of power mode 1 when $V_{in} = 654.2V$ and $V_o = 333.3V$

side switches is 0.5) are shown in the Figure 4.19. And the test results of the waveforms of V_{gs} and V_{ds} of S3 and S5 in power mode 5 (power is transferred from the EV port to the DC bus port and the duty cycle of the primary side switches is 0.5) are shown in the Figure 4.20.

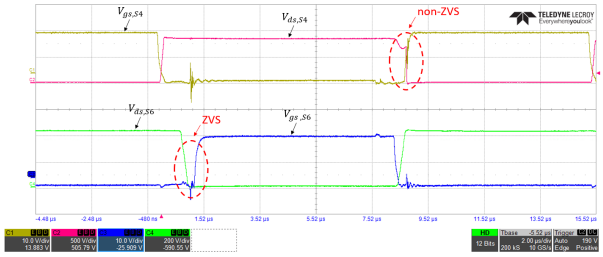
It can be seen from the Figure 4.19 and the Figure 4.20 that the ZVS of all the switches can also be realized when the dual boost integrated DAB converter is working in power mode 2 and power mode



(a) $D = 0.733$ $(V_{pv} = 220V)$

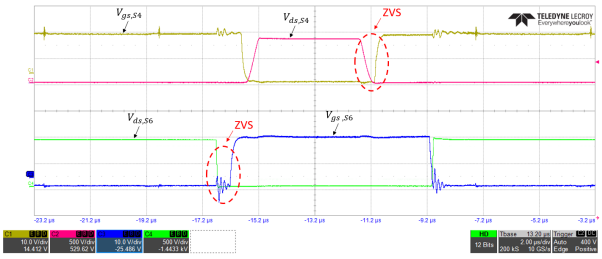


(b) $D = 0.5$ $(V_{pv} = 412.17V)$

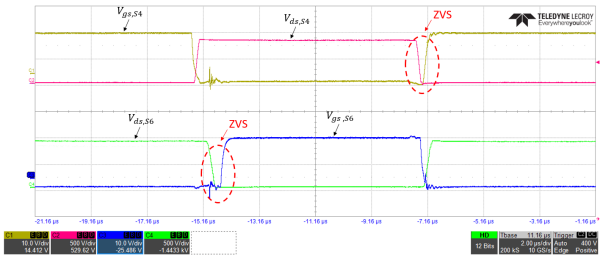


(c) $D = 0.45$ $(V_{pv} = 453.4V)$

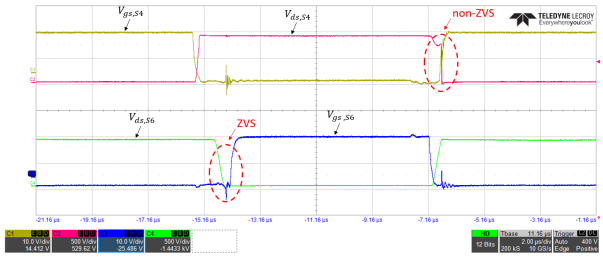
Figure 4.17: Test results of power mode 1 when $V_{in} = 824.34V$ and $V_o = 420V$



(a) $D = 0.733$ $(V_{pv} = 220V)$



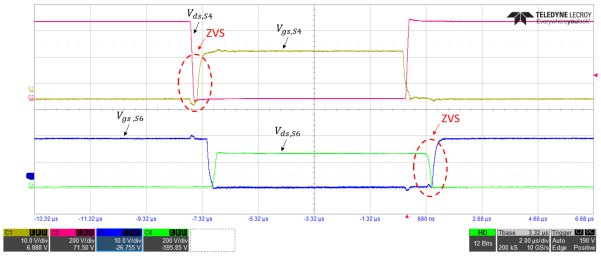
(b) $D = 0.5$ $(V_{pv} = 412.17V)$



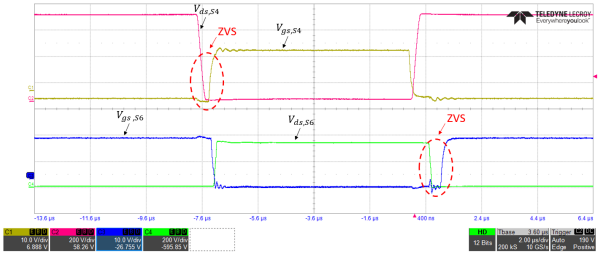
(c) $D = 0.45$ $(V_{pv} = 453.4V)$

Figure 4.18: Test results of power mode 1 when $V_{in} = 824.34V$ and $V_o = 840V$ with DC blocking capacitor voltage control

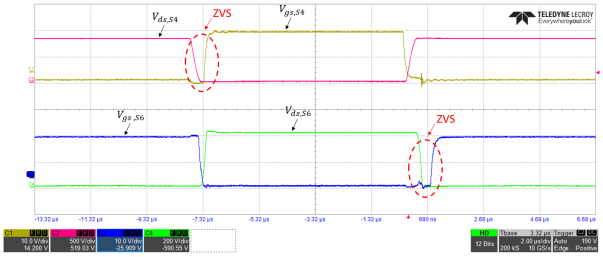
5 in the critical EV battery voltage range $(250V - 420V)$ even when the power is only $2kW$.



(a) $V_{in} = 600V$ and $V_o = 250V$

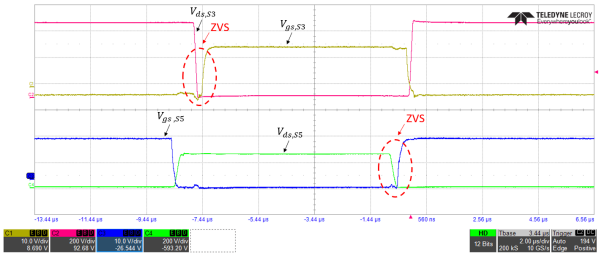


(b) $V_{in} = 654.2V$ and $V_o = 333.3V$

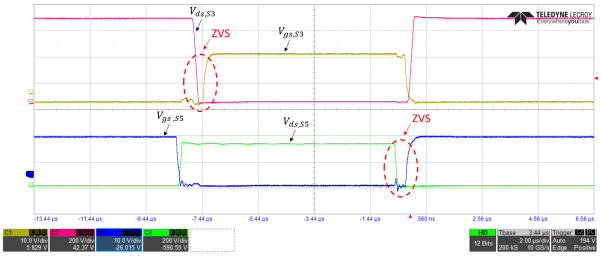


(c) $V_{in} = 824.34V$ and $V_o = 420V$

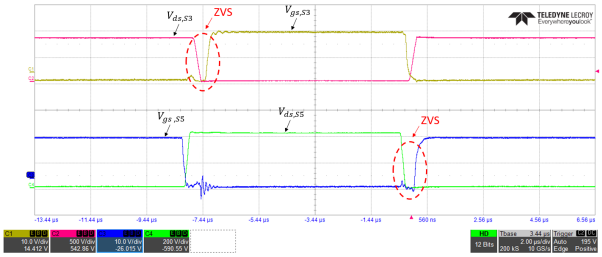
Figure 4.19: Test results of power mode 2



(a) $V_{in} = 600V$ and $V_o = 250V$



(b) $V_{in} = 654.2V$ and $V_o = 333.3V$



(c) $V_{in} = 824.34V$ and $V_o = 420V$

Figure 4.20: Test results of power mode 5

4.5. Summary

In this chapter, the contents about the experiment test in terms of the component design, the FPGA programming, the test of the gate driver circuit and all the test results about the basic working principle, the effect of the interleaved structure, the DC blocking capacitor voltage control and the ZVS region of the dual boost integrated DAB converter are presented. Several important conclusions need to be

emphasized:

- Compared with the gapped ferrite core, the powder core is more suitable for the application with a high DC bias due to its soft saturation characteristic. Besides, the elimination of the fringing flux makes the powder core can work with the higher switching frequency, which results in a reduction of the inductor size.
- The experiment test results in terms of the basic working principle, the effect of the interleaved structure, the DC blocking capacitor voltage control and the ZVS region of the dual boost integrated DAB converter are consistent with the previous analysis, which verifies all the analysis is correct. Besides, the design tool developed in Mathcad is also validated, so it can be used to do other customized designs and helps to decrease the time and cost for the development.
- Among all the test points, the highest efficiency in the charging mode is 97.5% which is the efficiency of the case when the power is transferred from the DC bus port to the EV port, the DC bus voltage is $600V$ and the EV battery voltage is $250V$. The lowest efficiency in the charging mode is 91.4% which is the efficiency of the case when the power is transferred from the PV port to the EV port, the DC bus voltage is $824.34V$, the PV voltage is $453.4V$ and the EV battery voltage is $840V$ since the ZVS of the primary side switches is already lost in this case. The efficiency of the case when the power is transferred from the PV port to the EV port is lower than that when the power is transferred from the DC bus port to the EV port if the DC bus voltage and the EV battery voltage are the same since there are additional losses on the two boost inductors when the power is transferred from the PV port. In the discharging mode, the highest efficiency among all the test points is 97.5% which is the efficiency of the case when the power is transferred from the EV port to the DC bus port, the EV battery voltage is $666.6V$ and the DC bus voltage is $654.2V$. And the lowest efficiency in the discharging mode is 95.4% which is the efficiency when the power is transferred from the EV port to the DC bus port, the EV battery voltage is $420V$ and the DC bus voltage is $824.34V$. All these efficiencies tested are based on the $2kW$ power. It should be noted that, the hardware is not a dedicated design for efficiency test. A better efficiency can be expected with an optimized hardware design.

5

Conclusion & Future work

5.1. Conclusion

In this master thesis project, the feasibility of the dual boost integrated DAB converter used for the PV integrated bidirectional EV charging system has been studied. The working principle and the loss analysis in terms of the ZVS characteristics and the loss breakdown of the switches, the circulating power and the optimized working range of this converter are investigated. A test bench is built to verify all the analysis and simulation results by doing the experimental test. There are some important conclusions got in this thesis need to be emphasized:

- The dual boost integrated DAB converter has the bidirectional capability and the interleaved structure in the primary side can significantly reduce the ripple of the PV current, which is a suitable topology for the PV integrated EV charging system since the PV panel is a current sensitive energy source and the bidirectional capability of the EV charger can realize the vehicle-to-grid (V2G) function which can reduce the load of the grid during the peak hours.

- The decoupled power control can be realized with the PWM plus SSPS control scheme used in this master thesis project. The boost inductor current (i_{L1} and i_{L2}) can be controlled by controlling the duty cycle of the primary side switches and further the power management between the two input ports can be realized by the controllable boost inductor current. The output current can be controlled by the phase shift between the primary side bridge and the secondary side bridge, which means the power transferred between the primary side and the secondary side can be controlled.

- It is hard to realize the ZVS of all the switches in the dual boost integrated DAB converter with a large voltage range which is required by this project and it can be seen from the analysis of the ZVS characteristics and the circulating power that the conditions to realize the ZVS of all the switches in this converter and the conditions to have the minimum circulating power are contrary in some cases. Therefore, the ZVS region of the switches and the circulating power are investigated by considering the DC bus voltage, PV voltage, and the EV battery voltage, and then the ZVS region is enlarged by applying the DC blocking capacitor voltage control. As a result, ZVS is able to be achieved in all the switches in the full operation range expect $200V \leq Vo \leq 300V$ and $479.25V < Vo \leq 600V$, and the circulating power is kept low.

- The losses on different switches are different in operation. For the primary side switches, this is because the duty cycle of the upper switches is different from that of the lower switches in the same leg. For the secondary side switches, this is because the full bridge secondary side will be changed to the half bridge structure and there is no loss on the S7. S5 and S6 have both switching losses and conduction losses but S8 only has conduction losses when the DC blocking capacitor voltage control is used. And the loss ratio of the total losses on the switches will not be continuously rising with the increasing output voltage due to the introduction of the DC blocking capacitor voltage control.

- Compared with the gapped ferrite core, the powder core is more suitable for the application with a high DC bias due to its soft saturation characteristic. Besides, the elimination of the fringing flux makes the powder core can work with the higher switching frequency, which results in a reduction of the inductor size.
- The experiment test results in terms of the basic working principle, the effect of the interleaved structure, the DC blocking capacitor voltage control and the ZVS region of the dual boost integrated DAB converter are consistent with the previous analysis, which verifies all the analysis is correct. Besides, the design tool developed in Mathcad is also validated, so it can be used to do other customized designs and helps to decrease the time and cost for the development.
- The highest efficiency among all the test points is 97.5% in both charging mode and discharging modes. It should be noted that, the hardware is not a dedicated design for efficiency test. A better efficiency can be expected with an optimized hardware design.

5.2. Future work

This master thesis project is the first step to investigate the dual boost integrated DAB converter for the PV integrated bidirectional EV charging system to make the whole system more compact and more efficient. There are several important things which are worth to be proceeded with:

- First of all, the hardware design of the converter can be done to further investigate this topology. In this master thesis, the experiment tests are implemented with a test bench which is built by removing the CLLC resonant tank of an existing CLLC resonant converter and connecting the two boost inductors, the additional leakage inductor and the DC blocking capacitors to it. Therefore, it is hard to verify the losses of the switches and to estimate the real efficiency of this converter.
- After the hardware design is finished and the prototype is constructed, the detailed switching losses, conduction losses and the loss breakdown as well as the loss ratio of the switches can be measured and compared with the simulation results, which is a good feedback to the power loss model and the thermal model built in the PLECS. Besides, the efficiency curves of this converter in different power modes can also be drawn according to the experiment results.
- Last but not the least, the closed loop control can be implemented after the prototype of the investigated converter is constructed to check the transient process when the converter is transferred from one power mode to another power mode.

A

Look-up charts from Magnetics

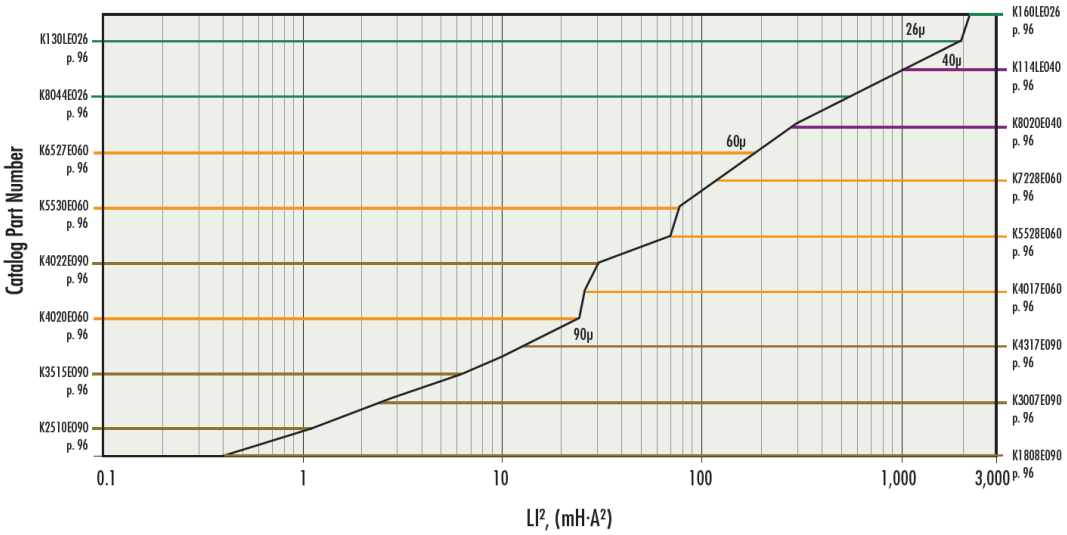


Figure A.1: The core selection chart of Kool Mμ E cores [2]

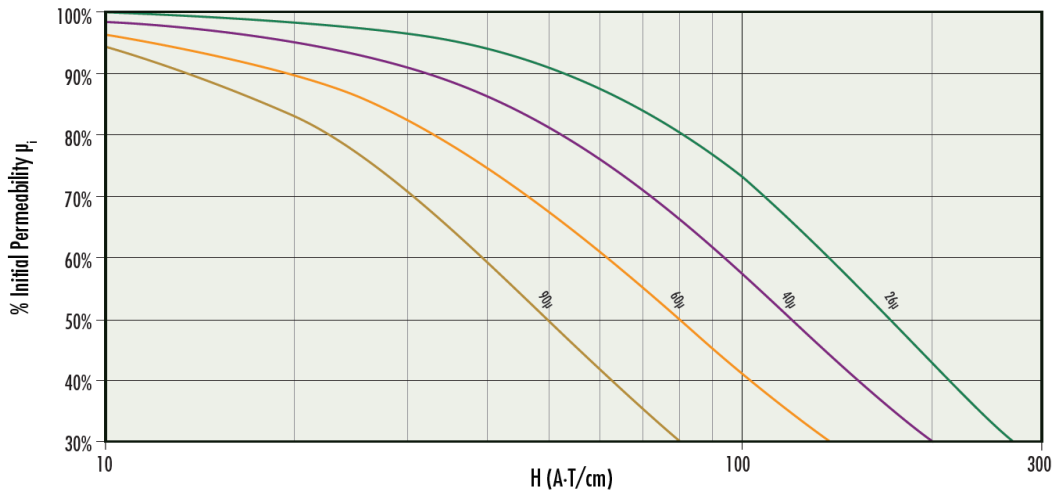


Figure A.2: The permeability versus DC bias curves of Kool Mμ E cores [2]

AWG Wire Size	Resistance Ω/meter	Wire O.D. (cm) Heavy Build	Wire Area cm^2	Current Capacity, Amps (listed by columns of Amps/cm^2)				
				200	400	500	600	800
6	.00130	.421	0.1392	26.6	53.2	66.5	79.8	106
7	.00163	.376	0.1110	21.1	42.2	52.8	63.3	84.4
8	.00206	.336	0.0887	16.7	33.5	41.8	50.2	66.9
9	.00260	.299	0.0702	13.3	26.5	33.2	39.8	53.1
10	.00328	.267	0.0560	10.5	21.0	26.3	31.6	42.1
11	.00414	.238	0.0445	8.34	16.7	20.8	25.0	33.3
12	.00521	.213	0.0356	6.62	13.2	16.5	19.8	26.5
13	.00656	.1902	0.0284	5.25	10.5	13.1	15.8	21.0
14	.00828	.1715	0.0231	4.16	8.33	10.4	12.5	16.7
15	.01044	.1529	0.01840	3.30	6.61	8.26	9.91	13.2
16	.01319	.1369	0.01472	2.62	5.23	6.54	7.85	10.5
17	.01658	.1224	0.01177	2.08	4.16	5.20	6.24	8.32
18	.02095	.1095	0.00942	1.65	3.29	4.11	4.94	6.58
19	.02640	.0980	0.00754	1.31	2.61	3.27	3.92	5.22
20	.03323	.0879	0.00607	1.04	2.08	2.59	3.11	4.15
21	.04190	.0785	0.00484	0.823	1.65	2.06	2.47	3.29
22	.05315	.0701	0.00386	0.649	1.30	1.62	1.95	2.59
23	.06663	.0632	0.00314	0.518	1.04	1.29	1.55	2.07
24	.08422	.0566	0.00252	0.409	0.819	1.0236	1.23	1.64
25	.10620	.0505	0.00200	0.325	0.649	0.812	0.974	1.30
26	.13458	.0452	0.00160	0.256	0.512	0.641	0.769	1.02
27	.16873	.0409	0.00131	0.204	0.409	0.511	0.613	0.817
28	0.214	.0366	0.00105	0.161	0.322	0.402	0.483	0.644
29	0.266	.0330	0.000855	0.129	0.259	0.324	0.388	0.518
30	0.340	.0295	0.000683	0.101	0.203	0.253	0.304	0.405
31	0.429	.0267	0.000560	0.0803	0.161	0.201	0.241	0.321
32	0.532	.0241	0.000456	0.0649	0.130	0.162	0.195	0.259
33	0.675	.0216	0.000366	0.0511	0.102	0.128	0.153	0.204
34	0.857	.01905	0.000285	0.0402	0.0804	0.101	0.121	0.161
35	1.085	.01702	0.000228	0.0318	0.0636	0.0795	0.0953	0.127
36	1.361	.01524	0.000182	0.0253	0.0507	0.0633	0.0760	0.101
37	1.680	.01397	0.000153	0.0205	0.0410	0.0513	0.0616	0.0821
38	2.13	.01245	0.000122	0.0162	0.0324	0.0405	0.0486	0.0649
39	2.78	.01092	0.000094	0.0124	0.0248	0.0310	0.0372	0.0497
40	3.54	.00965	0.000073	0.00974	0.0195	0.0243	0.0292	0.0390
41	4.34	.00864	0.000059	0.00795	0.0159	0.0199	0.0238	0.0318
42	5.44	.00762	0.000046	0.00633	0.0127	0.0158	0.0190	0.0253
43	7.03	.00686	0.000037	0.00490	0.00981	0.0123	0.0147	0.0196
44	8.51	.00635	0.000032	0.00405	0.00811	0.0101	0.0122	0.0162
45	10.98	.00546	0.000023	0.00314	0.00628	0.00785	0.00942	0.0126
46	13.80	.00498	0.000019	0.00250	0.00500	0.00624	0.00749	0.00999
47	17.36	.00452	0.000016	0.00199	0.00397	0.00497	0.00596	0.00795
48	22.10	.00394	0.000012	0.00156	0.00312	0.00390	0.00467	0.00623
49	27.60	.00353	0.000010	0.00125	0.00250	0.00312	0.00375	0.00499

Figure A.3: The wire selection table [2]

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