Design of A Readout System for a Low Leakage Soil Water-Content Sensor

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Abstract

Soil water-content sensors based on the measurement of soil impedance are widely used for the detection of rain-fall induced slope failure and other agriculture applications. In principle, low-leakage sensors can measure soil water content down to 4%, but they require readout systems capable of generating soil excitation signals at frequencies ranging from 1KHz to 1MHz. However, existing commercial products do not cover this frequency range. To solve this problem, a new readout system is proposed in this thesis. By using sinusoidal excitation, implemented by a pulse-width-modulated driver, and synchronous detection, the readout system achieves less than 1% measurement error from 1KHz to 1MHz.

Contents

Chapter 1 Introduction

1.1 Soil sensing application

Natural disasters like rainfall-induced slope failure cause tragic events. Therefore, it is vital to detect critical water content levels at a very early stage [1]. With the help of tilt sensors [2] and GPS units, detection is only possible after an accident has happened, which is often too late for an effective evacuation.

Figure 1-1 A landslide blocks the Kyushu Expressway [3]

Slope stability is determined by the driving and resisting forces present in a slope, where driving forces promote downslope movement while resisting forces deter the action [4]. When the driving forces overcome the opposing forces, the hill becomes unstable, and slope failure occurs. Besides constant factors like gravity, slope angle, and slope material, variables such as the water content in the slope play an important role. Water content can contribute to the driving force by increasing the load on a slope, or by removing its support by eroding the base of a ramp [4]. Therefore, real-time water content monitoring is necessary to predict slope failure.

Soil sensing also has other applications in the field of agriculture. Real-time monitoring of the analyte concentration in soil reflects water pollution, nutrient state of plants, and the health of domestic animals [5]. These parameters are crucial for the food safety and stability of food supply [5].

1.2 Soil sensor chip

Several types of sensors are available for conducting soil water-content measurements—namely, tensiometers [6], time-domain reflectometry (TDR) sensors [7], electrical conductivity (EC) sensors [8], and electrical impedance sensors. Tensiometers determine water content by measuring the suction forces. TDR sensors measure the time-of-travel of an electromagnetic wave passing through a waveguide, as the soil water content affects the wave velocity [9]. As the name suggests, EC sensors determine the water content by measuring the electrical conductivity of the soil sample, which is mainly a resistive measurement [5]. Compared with the other sensors, electrical impedance sensors have the advantages of long-term stability and a reduced need for maintenance [10].

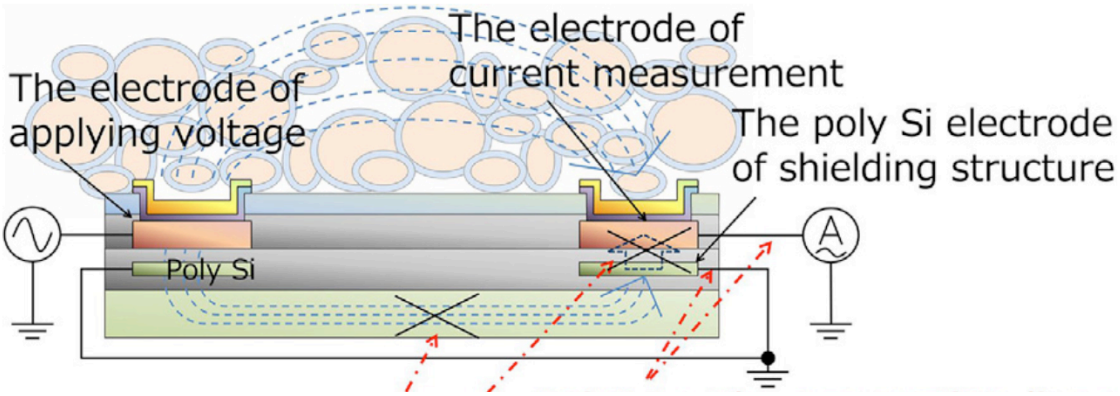

Figure 1-2 Cross-section of a low-leakage soil water content sensor [10]

In 2015, an electrical impedance sensor for real-time soil water content monitoring was introduced in [11]. Despite excellent performance in long-term mountain testing, the sensor struggled to measure low water content (<20%) due to considerable leakage current [10].

In 2017, a revised version of the soil sensor was proposed, which significantly reduces leakage current [10]. Figure 1-2 shows the working principles of the low-leakage soil sensor. The sensor uses a shielding electrode composed of a poly-Si structure under the current measurement electrode, which blocks the leakage current from interacting with the measurement signal [10]. This work made it possible to measure water content down to 4% [10].

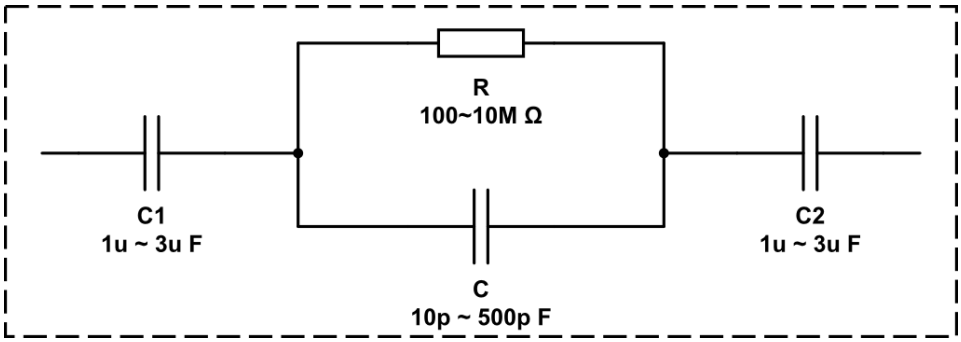

Figure 1-3 Electrical model of the proposed sensor

Figure 1-3 illustrates the equivalent electrical model of the soil sensor [10], wherein the resistance *R* varies both with the ion concentration in the water and the water content in the soil. The capacitor *C* depends solely on the soil water content. C_1 and C_2 represent the electrical double layer, which does not change with the soil water content but depends on the ion concentration. Depending on the soil environment, *R* ranges from 100 Ω to 10 MΩ, *C* varies from 10 pF to 500 pF, and C_1 and C_2 range from 1 μF to 3 μF. The electrical double layers are irrelevant in water content measurement.

By measuring the capacitance of *C*, the relative permittivity of the soil (ϵ_{soil}) can be calculated using Eq. (1):

$$\epsilon_{soil} = \frac{C \cdot D}{\epsilon_0 \cdot S} \tag{1}$$

where ϵ_0 is the permittivity of the vacuum, D is the distance between sensor electrodes, and S is the area of the electrode [10]. According to the dielectric mixing law [12], the water content of a soil sample can be calculated using Eq. (2):

$$\epsilon_{soil} = \left(V_{air}\sqrt{\epsilon_{air}} + V_{sand}\sqrt{\epsilon_{sand}} + V_{water}\sqrt{\epsilon_{water}}\right)^2 \tag{2}$$

where ϵ_{air}, ϵ_{sand}, and ϵ_{water} are the relative permittivity of air, sand, and water, respectively, and V_{air}, V_{sand}, and V_{water} are the ratios of volume density of air, sand, and water.

Figure 1-4 shows the absolute impedance of the electrical model over the frequencies for different *R*–*C* combinations. Because C_1 and C_2 do not affect water content measurement, a typical value of 1 μF for both is chosen to simplify the analysis. The

sensor needs to perform a frequency sweep up to the corner frequencies associated with each impedance range. So, the resistance and capacitance can be calculated from the relation of absolute impedance and frequency.

The resistance ranges from 100Ω to 10MΩ, and the capacitance varies from 10 pF to 500 pF; this indicates a frequency range of 31 Hz to 160 MHz. However, the combinations of high R/ high C and low R /low C are not realistic. For low water content, *C* is low, while *R* is high; for high water content, *C* is high while *R* is low. A realistic *R*–*C* combination gives a frequency range of 1 kHz–1 MHz [10], as shown in Figure 1-4. Therefore, the readout circuit needs only to cover this frequency range.

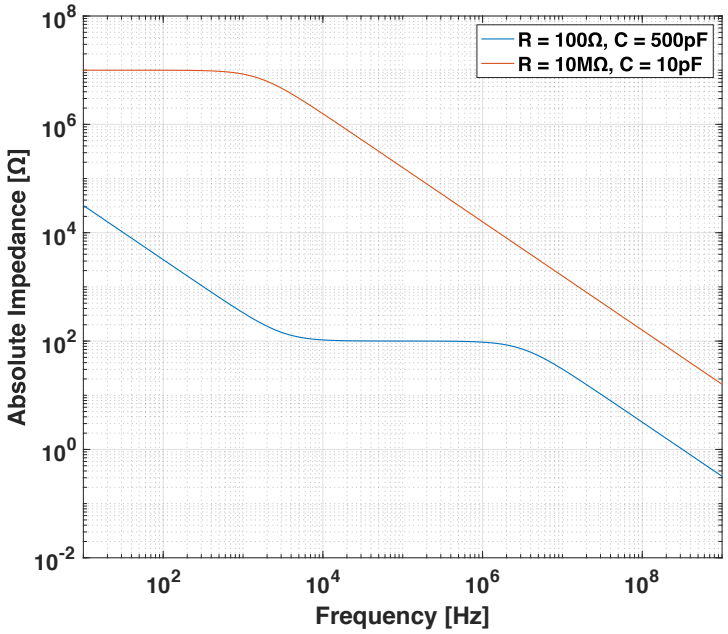

Figure 1-4 Absolute impedance of sensor network versus frequency

1.3 Soil sensor readout

In this thesis, a dedicated readout circuit is designed for the low leakage soil sensor [10]. Figure 1-5 illustrates the readout principle for the soil sensor. To measure the soil impedance, a sinusoidal voltage signal is applied to one electrode, and a sinusoidal current is measured at the other electrode. By varying the frequency of the input voltage signal and measuring the corresponding output current, an impedance profile is obtained. Then, the capacitance of *C* can be calculated to determine the water content in the soil.

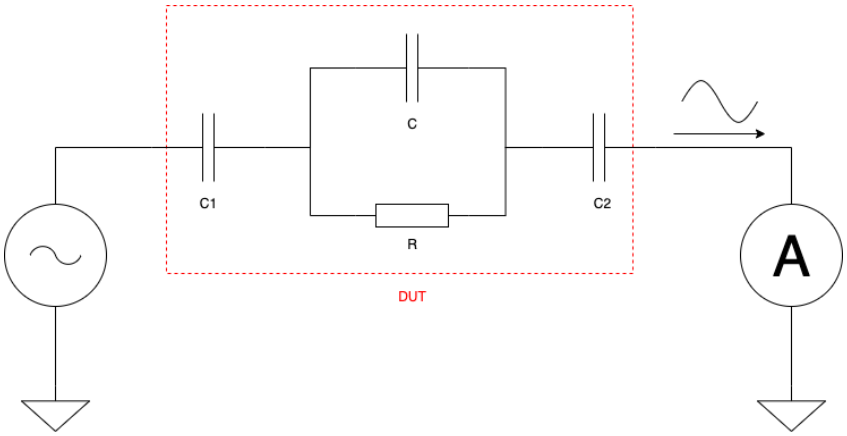

Figure 1-5 Operating principle of the readout circuit

First, the readout system needs to cover a high impedance dynamic range from |Z| ≈ 100 Ω to |Z| ≈ 8.6 MΩ. The bandwidth is from 1 kHz to 1 MHz, as explained in Section 1.2.

Second, the signal applied to the electrodes must be limited. This is because when an electrical current or a voltage signal is applied to the sensor electrode, oxidation-reduction (redox) reactions are stimulated [10]. If the signal level is beyond the redox reaction potential, it causes damage to the sensor electrode and reduces the sensor's lifetime. Our sensor [10] uses platinum electrodes, which limit the excitation voltage to 500 mV_{p-p} and current to 200 μA_{p-p}.

Finally, the accuracy specification for the readout scheme is 1%, which is chosen to be negligible compared to the error introduced by the sensor electrode (5% -7% [10]).

To summarize, the specifications of the sensor readout system are given in Table 1-1.

Table 1-1 Specifications of the sensor readout system

Impedance Range	100 Ω–10 MΩ
Frequency Range	1 kHz–1 MHz
Maximum Voltage	500 mV_{p-p}
Maximum Current	200 μA_{p-p}
Accuracy	1%

Commercial products, such as the AD5933 using a single-frequency DFT principle [13], can be used to readout soil sensors with a customized analog front end (AFE). Such a readout system has been implemented as a benchmark design in the present study and will be explained in detail in Chapter 2. A more accurate readout method based on PWM modulation is then proposed and described in Chapter 3, which also covers a broader frequency range.

1.4 Thesis structure

The thesis organized as follows:

- Chapter 2 explains the design of the benchmark system based on AD5933 and presents the measurement results.
- Chapter 3 presents the system-level design of the proposed readout and derives the specifications of each functional block.
- Chapter 4 focuses on the circuit design of the proposed readout.
- Chapter 5 presents the measurement results of the proposed readout.
- Chapter 6 draws conclusions and discusses future research.

Chapter 2 Benchmark system design

The benchmark system employs an existing commercial impedance converter, the Analog Devices AD5933 [13], to generate the soil sensor readout, which will be later compared to the proposed readout. The AD5933 is widely used for interfacing electrical impedance sensors (see, e.g., [14] [15] [16]).

The entire benchmark system, block-diagrammed in Figure 2-1, consists of the AD5933 and a dedicated analog front end (AFE). The AD5933 generates a sinusoidal voltage, which is then adjusted by the AFE to meet the soil sensor's input requirements. The soil sensor output is amplified by the AFE and then fed into the AD5933 for further impedance analysis.

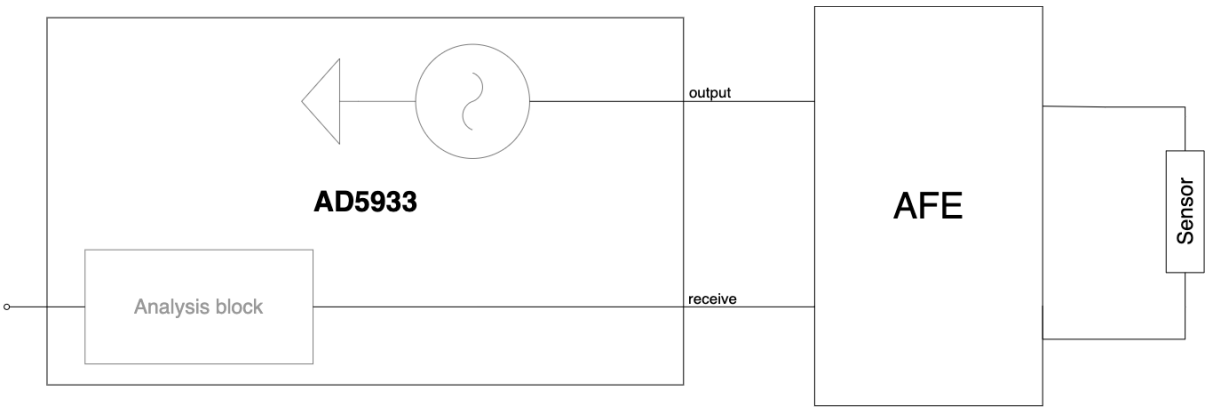

Figure 2-1 Block diagram of the benchmark system

The AD5933 will be described in more detail in Section 2.1; the AFE design will be discussed in Section 2.2. An issue due to spectral leakage of AD5933 is discussed in Section 2.3. The measurement results are shown in Section 2.4.

2.1 AD5933 analysis

Figure 2-2 shows the AD5933's functional block diagram, which comprises three major stages: the Transmit stage, the Receive stage, and the Discrete Fourier Transform (DFT) stage. The Transmit stage generates a sinusoidal voltage at the "output" node, using an onboard oscillator, a direct digital synthesizer (DDS), a digital-to-analog converter (DAC), and an output buffer. The Receive stage measures and digitizes the signal at the "receive" node, depending on the analog front end (AFE) configuration. There is also a gain stage and a low-pass filter (LPF) in the Receive stage. The 12-bit

ADC converts the analog signal into a digital signal. The single-frequency DFT stage extracts the digital signal at the excitation frequency.

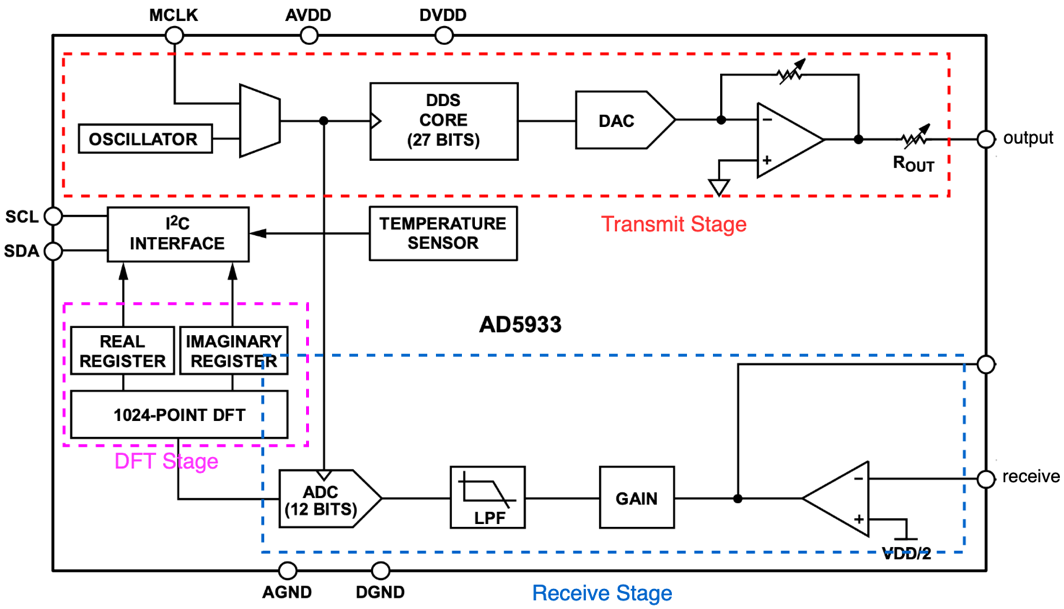

Figure 2-2 Block diagram of the AD5933

Although the AD5933 is designed for general impedance measurements, a dedicated AFE is required to interface our soil sensor [10] for the following reasons. Firstly, the Transmit stage of the AD5933 generates only fixed excitation signals (Table 2-1). The amplitudes of Sets 1, 2, and 3 are too high for the soil sensor (< 500 mV_{p-p}) due to redox reactions, as explained in Chapter 1, Section 1.2. Set 4 meets the soil sensor's maximum voltage requirement but does not make use of the full signal swing, and its output impedance is too high to interface with the soil sensor, whose impedance can be as low as 100 Ω. As a result, the AFE is designed to adjust the excitation signal amplitude, reduce the DC component at the "output" node, and minimize loading effects by providing a low output impedance.

Table 2-1 Four sets of excitation voltage in AD5933 [13]

Set	Amplitude	Common-mode voltage	R_{out}
Set 1	3 V_{p-p}	2.24 V	200 Ω
Set 2	1.47 V_{p-p}	1.15 V	2.4 kΩ
Set 3	0.58 V_{p-p}	0.47 V	1 kΩ
Set 4	0.3 V_{p-p}	0.26 V	600 Ω

The Receive stage feeds the response signal from the sensor into an onboard ADC. One major problem is that all the op-amps are hard-biased at $V_{DD}/2$ (common mode at 2.5 V), as in Figure 2-2. Since the sensor signal is AC-coupled (common mode at 0 V), there will be a common-mode difference of 2.5 V when the Receive stage interfaces with the sensor directly. So, the AFE should reset the common-mode voltage to match the Receive stage, in order to use the AD5933's full signal swing. Also, because of the common-mode difference, the op-amp in the Receive stage cannot interface with the soil sensor. Besides the common-mode issue, the datasheet [13] does not give detailed specifications of the op-amp in the Receive stage, which makes it difficult to estimate the transfer error and stability of this stage.

As for the DFT stage, the datasheet [13] does not provide the dynamic range of the ADC. [15] and [17] claim a dynamic range (DR) of 33 dB under matched common-mode conditions. The ADC's dynamic range ultimately limits the lowest signal level in the Receive stage. The lowest signal amplitude that the AFE should produce is $\frac{4.6\,V}{45\times5} \approx 20\,mV$, where 4.6 V is the full signal swing, 45 is the DR of the ADC, and 5 is the amplification provided by the gain stage of the AD5933.

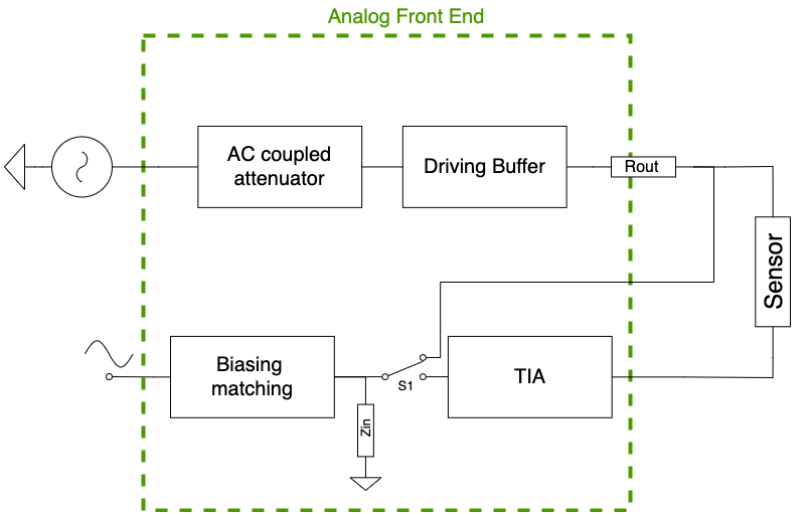

Figure 2-3 Block diagram of the analog front end

Figure 2-3 diagrams the AFE that interfaces the AD5933 with the soil sensor. Switch S1 limits the error due to loading effects by measuring the excitation voltage with sensor loading. Impedance Z_{in} also plays a role in this error. Figure 2-4 shows how the error varies with Z_{in} for different values of R_{out}. So, when R_{out} is below 10 Ω and Z_{in} above 50 KΩ, the error due to loading is less than 0.05%.

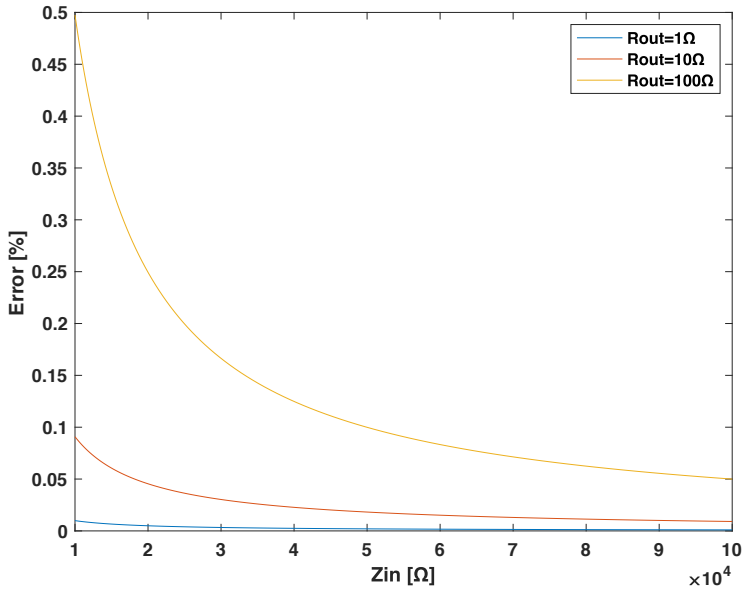

Figure 2-4 Error-dependence on Z_{in} for different R_{out}

In summary, the AFE must:

- Set the correct excitation amplitude where the maximum voltage is 500 mV_{p-p} and the maximum current is 200 μA_{p-p}
- Remove the DC component at the transmit stage output
- Provide a transimpedance block
- Reset the common-mode voltage to $V_{DD}/2$ at the Receive side

2.2 The analog front end design

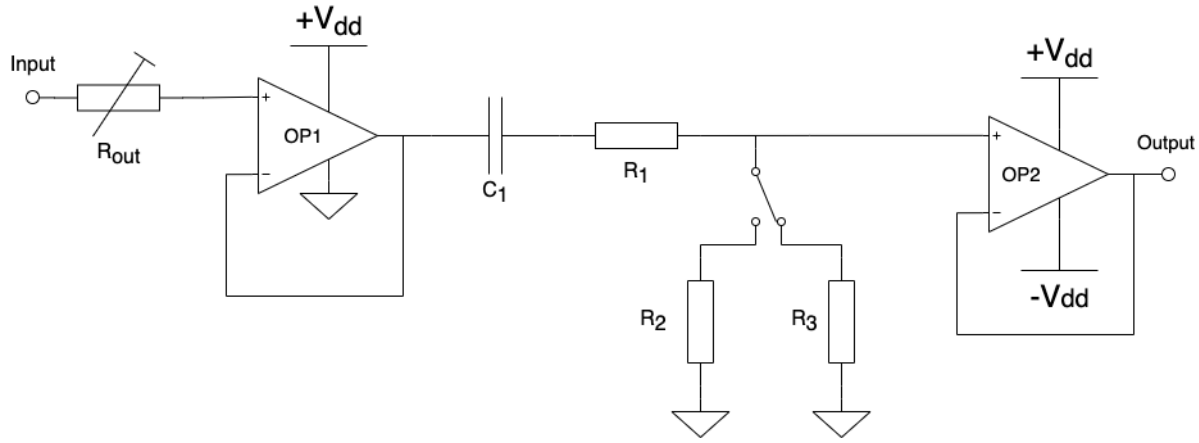

Figure 2-5 AC-coupled attenuator and driving buffer

Figure 2-5 shows the Transmit stage of the AFE. To get the desired signal amplitude, the Transmit stage uses Set 3 in Table 2-1, which needs the least attenuation to reach the 500 mV_{p-p} signal level. First, a unity-gain buffer, realized with an AD8606 op-amp

[18], is used to interface the AD5933 providing high input impedance and low output impedance. The datasheet [18] reports a closed-loop output impedance of 1.2 Ω up to 1 MHz.

C_1 removes the DC component. A resistive voltage divider (R_1, R_2, and R_3) is to generate the desired excitation voltages. As mentioned in the preceding chapter, the excitation signal should be smaller than 500 mV_{p-p} to prevent redox reactions. Therefore, 500 mV_{p-p} is chosen to maximize the SNR. However, in the presence of high water content, the soil sensor's impedance is at its lowest so, when operating with a 500 mV_{p-p} excitation voltage, the induced current exceeds the sensor limits (200 μA_{p-p}). Therefore, two excitation voltages (500 mV_{p-p} and 20 mV_{p-p}) are provided and can be selected using a SPDT switch. A low-amplitude "safe mode" covers the lower impedance range, and "normal mode" comes in when the signal is below the threshold. As shown in Figure 2-6, there are multiple choices for this threshold that can keep the current within limits. The AFE uses 2.5 kΩ as the threshold point for switching modes in order to maximize the high-excitation range, thereby optimizing the SNR.

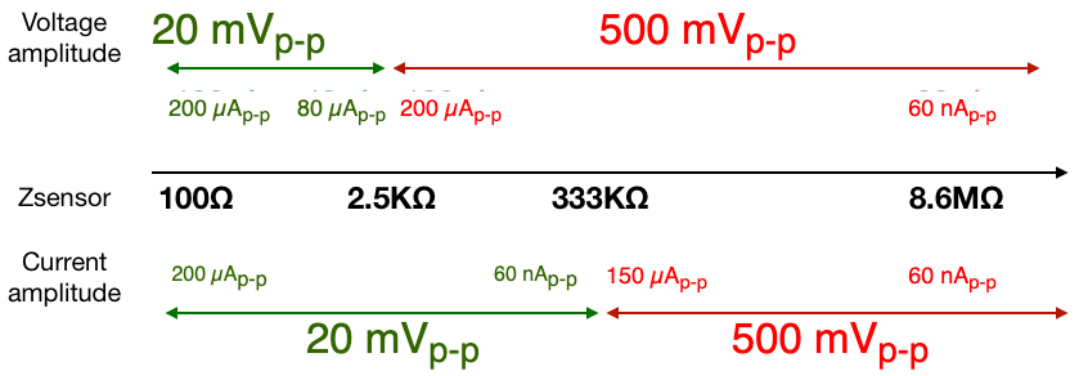

Figure 2-6 Excitation voltage for impedance range

The second unity gain buffer (Figure 2-5) drives the soil sensor. ADA4625 [19] is used as op-amp OP2 for its high capacitive drivability (1 nF) [19]. The sensor network starts acting like a high capacitive load (500 pF) from 1 kHz when R = 1 MΩ, C = 500 pF. In addition to having high capacitive drivability, the ADA4625 maintains a 2 Ω output impedance up to 1 MHz and suitability for working under a dual power supply [19].

Extra poles are not desirable in the transfer function, but the input capacitance of op-amp OP2 or the PCB traces creates a pole with the resistive voltage divider. So, the equivalent resistance of the voltage divider should be limited to avoid undesired

attenuation by this pole. The input capacitance of OP2 is around 20 pF [19]. Assuming the PCB trace contributes a further 5 pF, the positive input of OP2 would have 25 pF. To place the undesired pole in alignment with the AD5933's bandwidth (500 kHz), the equivalent impedance of a resistive divider should be smaller than 13 kΩ.

The equivalent impedance of the resistive divider equals R_1 in parallel with either R_2 or R_3, depending on the excitation voltage. The pole most likely limits the bandwidth in the high-gain régime. Therefore, the calculated resistances for the resistive divider is R_1 = 15 kΩ, R_2 = 94 kΩ, and R_3 = 535 Ω. For the value of C_1, the zero is designed at 10 Hz, two decades from the lowest signal frequency. This zero limits the bandwidth in the low-gain régime, which gives C_1>1 μF.

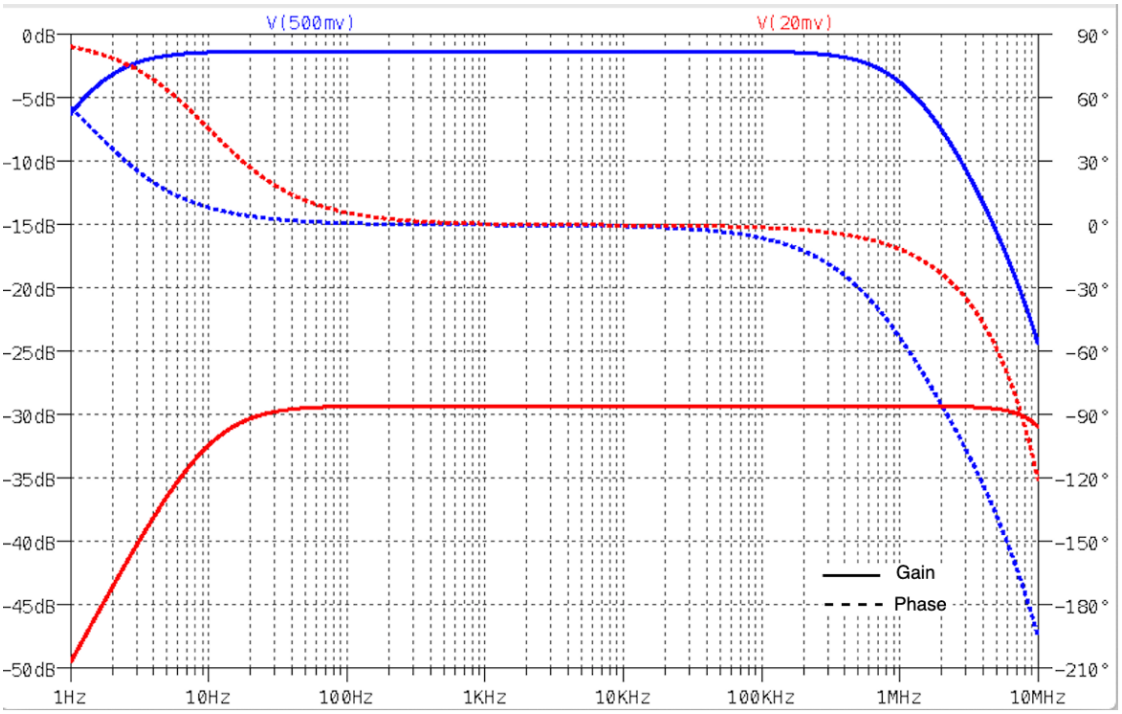

Figure 2-7 AC simulation of AFE at the Transmit stage

Figure 2-7 confirms the frequency responses from the "Input" node to the "Output" node, at two different gain settings. The zero locates at 10 Hz in a low-gain setting, while the pole is around 500 kHz at the high-gain setting.

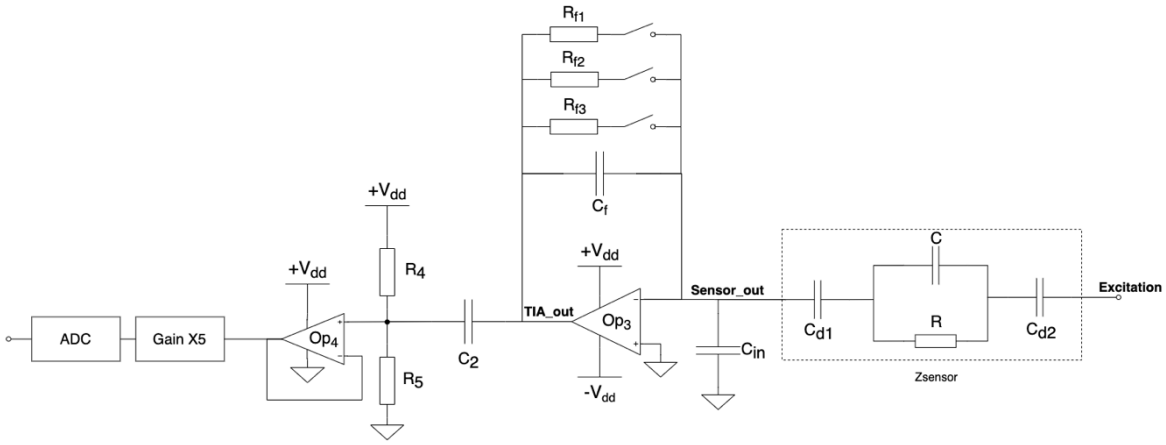

Figure 2-8 TIA and biasing matching design in the benchmark system

Figure 2-8 shows the AFE design on the Receive side. The transimpedance amplifier (TIA) should not saturate the ADC in the AD5933. So, the initial step is to determine the TIA's gain. The DR of the electric current signal at the "Sensor_out" node is 72 dB when using two excitation modes. Since the ADC has a dynamic range of 33 dB [17], the TIA needs to have three programmable gains to cover the full measurement. Table 2-2 displays the configurations for three impedance ranges, according to the ADC dynamic range. The exact TIA gain can be calculated using equation (3):

$$R_{\mathrm{f}} = \frac{Z_{\mathrm{mini}}\,(\frac{V_{DD}}{2} - \mathrm{headroom})}{\mathrm{Gain}\,(V_{\mathrm{pk}} + \frac{V_{DD}}{2} - V_{\mathrm{DC}})} \tag{3}$$

where Z_{mini} is the minimum impedance in the measurement range, which is in the first column of Table 2-2. The required headroom is 200 mV, according to the suggestions in the application note [17]. Gain is 5, from the programmable gain block in the AD5933 [13]. Voltage V_{pk} is the peak voltage of the selected output range, and V_{DC} is $V_{DD}/2$ assuming rebasing afterward. The TIA gains for each measurement range, calculated using Eq. (3), are shown in Table 2-2.

Table 2-2 impedance ranges for trans-impedance amplifier

Index	Impedance range [Ω]	Excitation Voltage [mV_{p-p}]	R_f [kΩ]	C_f [pF]
1	100–2.5 k	20	4.53	2.2
2	2.5 k–120 k	500	4.53	2.2
3	120 k–5.76 M	500	20.5	2.2
4	5.76 M–8.6 M	500	60.4	2.2

Once the feedback resistors are fixed, the next step is to select the Op3 for the TIA. The TIA transfer error is defined by Eq. (4):

$$\text{Error} = \frac{H - H_{\text{ideal}}}{H_{\text{ideal}}} \cdot 100\% \tag{4}$$

Where H is the transfer function of the TIA and H_{ideal} is the ideal transfer function, which equals to $H_{\text{ideal}} = I_{\text{sensorout}} * R_{\text{f}}$. By performing node analysis on the "Sensor_out" node, the error function can be rewritten as Eq. (5):

$$\text{Error}(s) = \left(\frac{Z_f(s)}{R_{\text{f}} + \frac{{R_{\text{f}}}^2}{A(s)Z_{\text{sensor}}} + \frac{R_{\text{f}}}{A(s)} + \frac{sC_{\text{in}}{R_{\text{f}}}^2}{A(s)}} - 1 \right) \cdot 100\% \tag{5}$$

Assuming no frequency dependence of Z_{f}, the error terms are $\frac{{R_{\text{f}}}^2}{A(s)Z_{\text{sensor}}} + \frac{R_{\text{f}}}{A(s)} + \frac{sC_{\text{in}}{R_{\text{f}}}^2}{A(s)}$. So, a higher op-amp gain can suppress the transfer error. This analysis also shows that a small sensor impedance, large input capacitors, and a large feedback resistance could lead to more significant errors. The target accuracy of the AFE is 0.5%, which agrees with the required system accuracy [13]. So, we can now find the required open-loop gain at 100 kHz for the calculated feedback resistance.

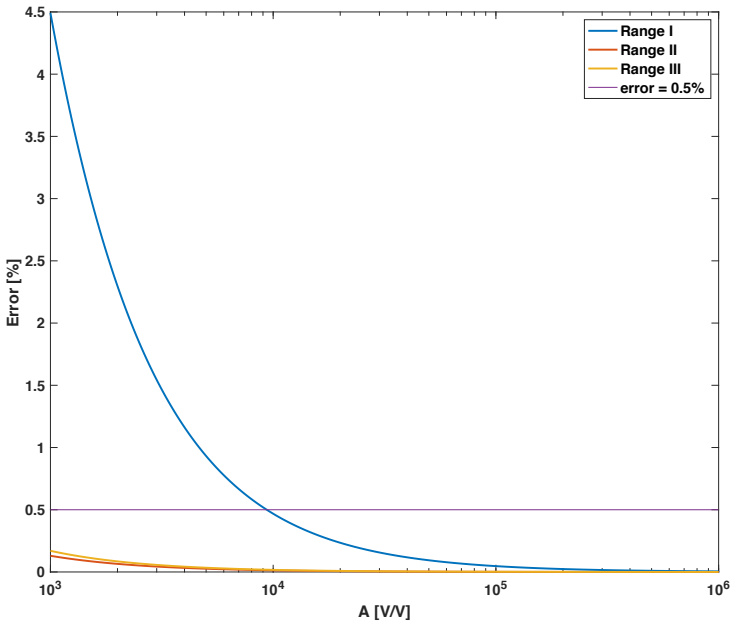

Figure 2-9 Transfer error versus op-amp gain for the benchmark system

Figure 2-9 shows the transfer error versus the op-amp open-loop gain. The figure suggests that transfer error in Range II and Range III is minimal compared with Range I, which can be explained by the higher sensor impedance. In Range I, the op-amp needs to have 89 dB gain at 100 kHz to keep the error below 0.5%. Besides the gain requirement, the op-amp needs to have a FET input stage to avoid the large input bias current, causing a voltage offset at the output. The BJT input stage has a more significant biasing current compared to a FET input stage, which could be tens of microamperes. The biasing current flows through the feedback resistor and creates a voltage offset of 0.64 V, assuming a biasing current of 10 µA. Additionally, the op-amp needs to work under a dual power supply due to the AC-coupled characteristic of the sensor. With these considerations in mind, the TIA uses an OPA818 op-amp [20] as the active device.

The last step is to examine the stability of the transimpedance amplifier. To stabilize the TIA, a feedback capacitor C_f (Figure 2-8) is employed, which compensates for a 45° phase margin at the frequency $\frac{1}{2\pi C_f R_f}$. If compensation is at the intercept point of the open-loop gain and uncompensated 1/β, the TIA could have a 45˚ phase margin.

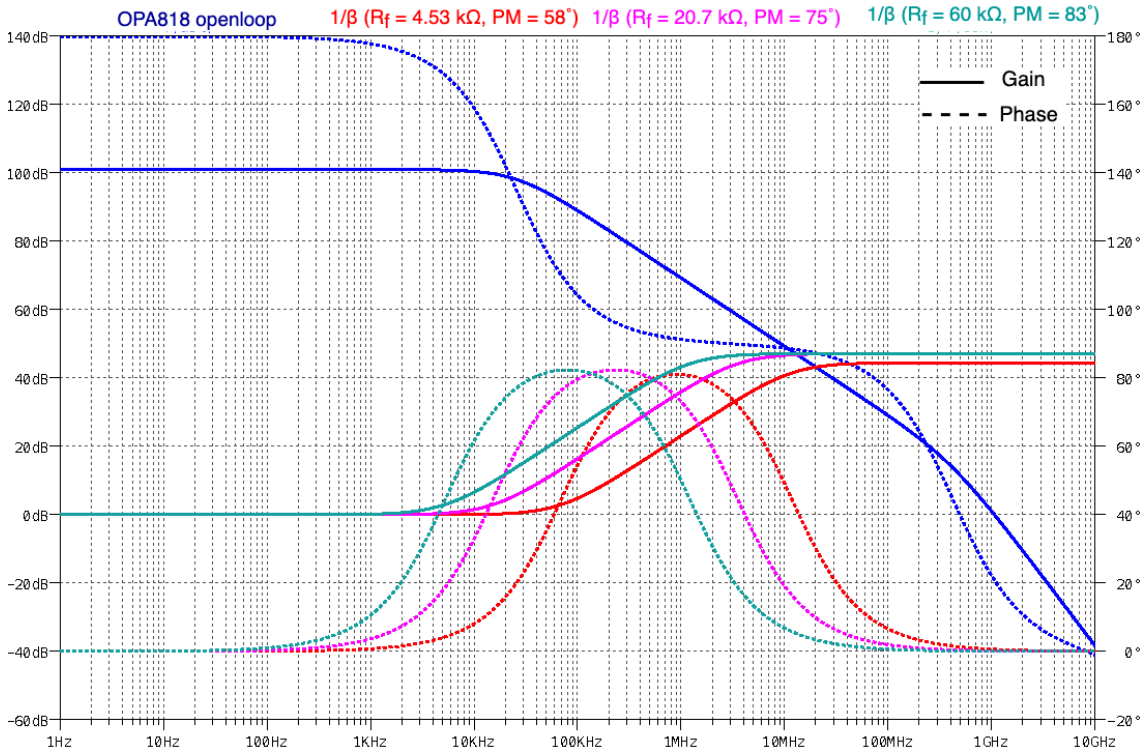

Figure 2-10 Compensated TIA at different feedback resistance

Figure 2-10 plots the OPA818 open-loop gain and 1/β at three different feedback resistances, at the worst-case stability (C = 500 pF and R = 10 MΩ). When C_f = 2.2 pF, the loop gain is critically compensated for R_f = 4.5 kΩ. For higher values of R_f, the loop gain is overcompensated. The bandwidth-limiting pole locates at 1.2 MHz, which is well above the signal bandwidth 100 kHz. Therefore, the same feedback capacitor is enough to compensate for all three feedback resistances.

The last block in the AFE is the biasing-matching block. The capacitance C_2 removes any offsets from the previous stage. Then, resistive division by R_4 and R_5 with equal weight add the $V_{DD}/2$ common-mode voltage to the signal. In this way, the bias voltage matches the AD5933 Receive stage. To obtain a high input impedance, R_4 and R_5 are 10 MΩ, which is in the same range of the input impedance of op-amp "Op4". The high-pass corner formed by resistive division and C_2 is chosen to be at 10 Hz, which gives C_2 =3.3 nF.

Circuit simulations were performed to verify the design of the AFE. Table 2-3 shows the simulation error at a different impedance corner. According to the Spice simulation, the AFE creates the worst-case 0.3% error at the lowest sensor impedance Z_{sensor} and at the highest frequency.

Table 2-3 Simulation results of AFE in the benchmark system

	1 kHz [%]	100 kHz [%]
500 pF,10 MΩ	0.051	0.125
10 pF,10 MΩ	0.061	0.051
500 pF,100 Ω	0.147	0.277
10 pF,100 Ω	0.187	0.197

2.3 Spectral leakage of the AD5933

The AD5933 impedance converter shows a significant offset at 1 kHz, even when no signal is present on the Receive stage, caused by the single-frequency DFT engine. Spectral leakage happens when the DFT window width is not an integer multiple of the input period [9]. According to [21], the spectral leakage produces a digital gain for both the real part and the imaginary part, as described by Eq. (6) and Eq. (7).

$$G_r = \frac{\sin(\frac{\pi}{N})^2 \sin(2\pi f N)}{4\sin(\pi(\frac{1}{N}+f))\sin(\pi(\frac{1}{N}-f))\tan(\pi f)} \quad (6)$$

$$G_i = \frac{\sin(\frac{\pi}{N})^2 \sin(2\pi f N)^2}{4\sin(\pi(\frac{1}{N}+f))\sin(\pi(\frac{1}{N}-f))\tan(\pi f)} \quad (7)$$

where *N* is the DFT length, and *f* is the normalized signal frequency. This gain depends on the signal frequency and reduces as the frequency increases. Figure 2-11 shows a plot of the real and imaginary parts of the gain versus frequency, where *k* = *f/N.* Singularities occur when *k* = 0 or *k* = 1, making the denominator zero. Besides these two singularities, the system should expect no spectral leakage when *k* is an integer. This condition ($k \in Z$ and $k \geq 2$) is called the *coherent detection condition*.

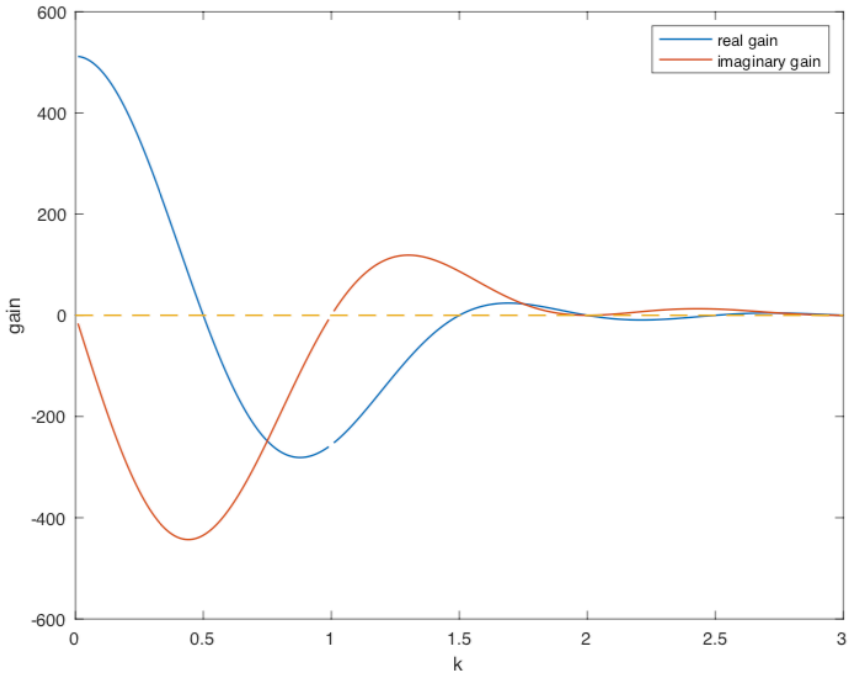

Figure 2-11 Theoretical predictions of spectral leakage

Measurement is done from *k* = 1 to *k* = 6 when no signal presents at the AD5933 Receive stage. Figure 2-12 confirms the theoretical prediction, where both the real-part gain and the imaginary-part gain touch zero at the coherent detection frequency. Also, the effect of spectral leakage fades away when the signal frequency increases.

As in Figure 2-12, the spectral leakage drops from a few thousand to below a hundred when *k* steps up from 1 to 6.

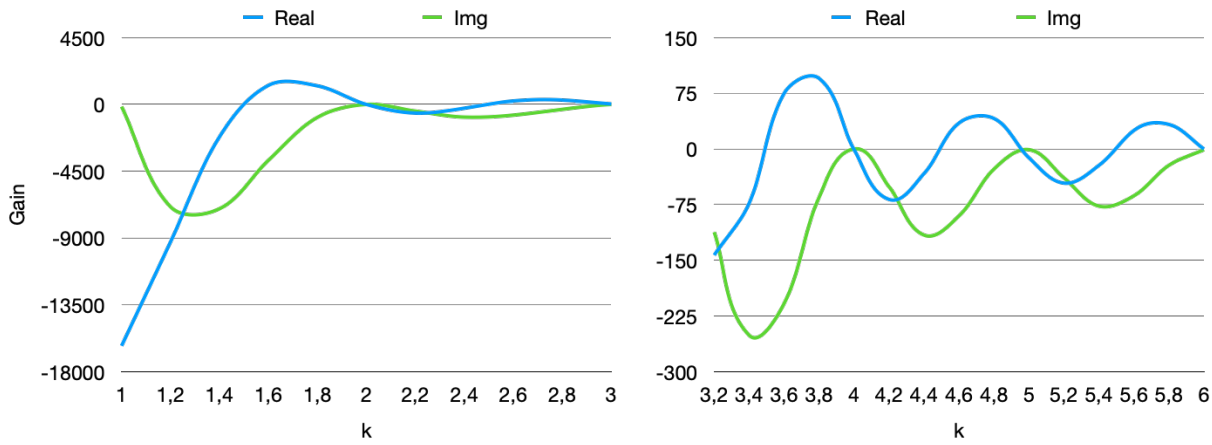

Figure 2-12 Measurement of spectral leakage of AD5933

Table 2-4 shows the coherent detection frequency and DDS code in hexadecimal for the AD5933. The DFT window is $T_{\mathrm{DFT}} = \frac{N}{F_{\mathrm{ADC}}}$, where F_{ADC} is the ADC throughput, and N is the DFT length. The excitation period for coherent detection is $T_{\mathrm{excitation}} = \frac{T_{\mathrm{DFT}}}{K}$.

Table 2-4 Coherent detection frequency for AD5933

k:	1	2	3	4	5	96	97
f [Hz]:	1024	2048	3072	4096	5120	9.8E+04	9.9E+04
DDS code [HEX]:	0x008000	0x010000	0x018000	0x020000	0x028000	0x300000	0x308000

2.4 Benchmark measurement

Figure 2-13 shows the accuracy of the AD5933 while measuring the equivalent sensor model. The measurement covers both ends of the frequency range, namely 2048 Hz and 100 kHz. 1 kHz is not tested because of the spectral leakage. When the sensor capacitor *C* = 470 pF (Figure 2-8), the worst-case error is around 1.2%. However, the errors go beyond 3% as the resistance *R* increases at the point of *C* = 10 pF and *f* = 100 kHz. Besides the error caused by the AFE, the main reason for the significant error at higher frequencies could be inherent limitations (nonlinearity or jitter) of the

ADC. The error is more pronounced when the signal is smaller, which is high absolute impedance.

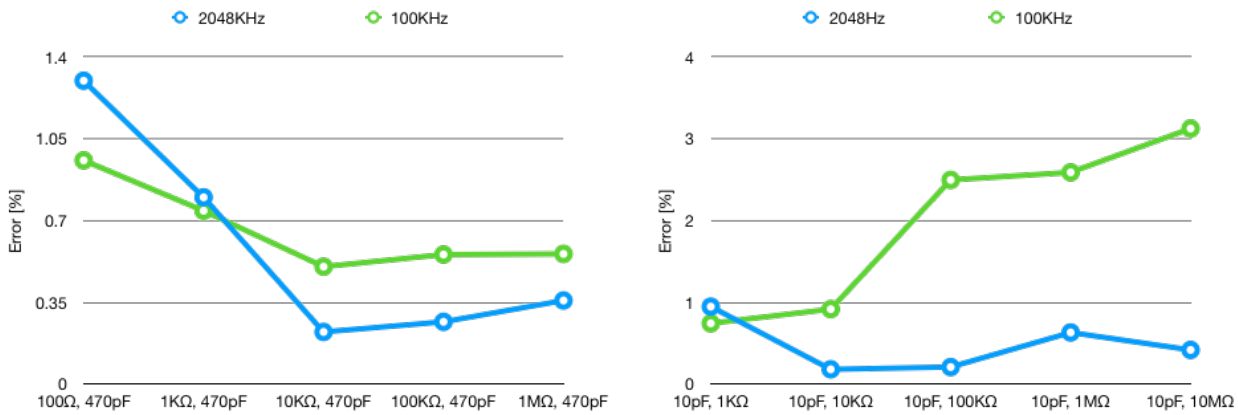

Figure 2-13 Impedance measurement error of AD5933

Table 2-5 shows the comparison of this benchmark board with other systems based on the AD5933. Similar techniques are used to avoid spectral leakage problems in order to achieve the stated performance. Therefore, the accuracy of the proposed benchmark system aligns with other existing cases.

To conclude, the AD5933 can work with the low-leakage soil sensor with the help of the customized AFE. However, the lowest system operating frequency range is limited by the spectral leakage of the DFT engine. As a result, the system can only measure from 2048 Hz to 100 kHz with a step of 1024 Hz. Moreover, the system shows poor performance when the impedance level is high, and when the frequency is high. The worst-case error is around 3%.

Table 2-5 Comparison with other systems based on AD5933

	Frequency Range	Impedance Range	Maximum Error
J. Ferreira [14]	5 kHz–450 kHz	Not mentioned	17%
Chabowski [15]	1 Hz–100 kHz	10 Ω–1 MΩ	3.5%
Bogónez-Franco [16]	100 Hz–200 kHz	10 Ω–1 kΩ	2.5%
This benchmark system	1 kHz–100 kHz	100 Ω–8.6 MΩ	3%

Chapter 3 System-level design

Based on the previous chapter, AD5933 evidently suffers from spectral leakage and poor SNR. Therefore, it cannot meet the accuracy requirement of our soil sensor. A new readout based on sinusoidal pulse width modulation (SPWM) is proposed. This chapter describes the system-level design, starting with the working principles, and then focusing on each sub-block.

3.1 Working principle of the proposed readout

3.1.1 Introduction to SPWM

As mentioned in Chapter 1, the soil sensor requires voltage excitation. The square-wave excitation has many in-band harmonics, and a pure sine wave excitation is challenging to generate.

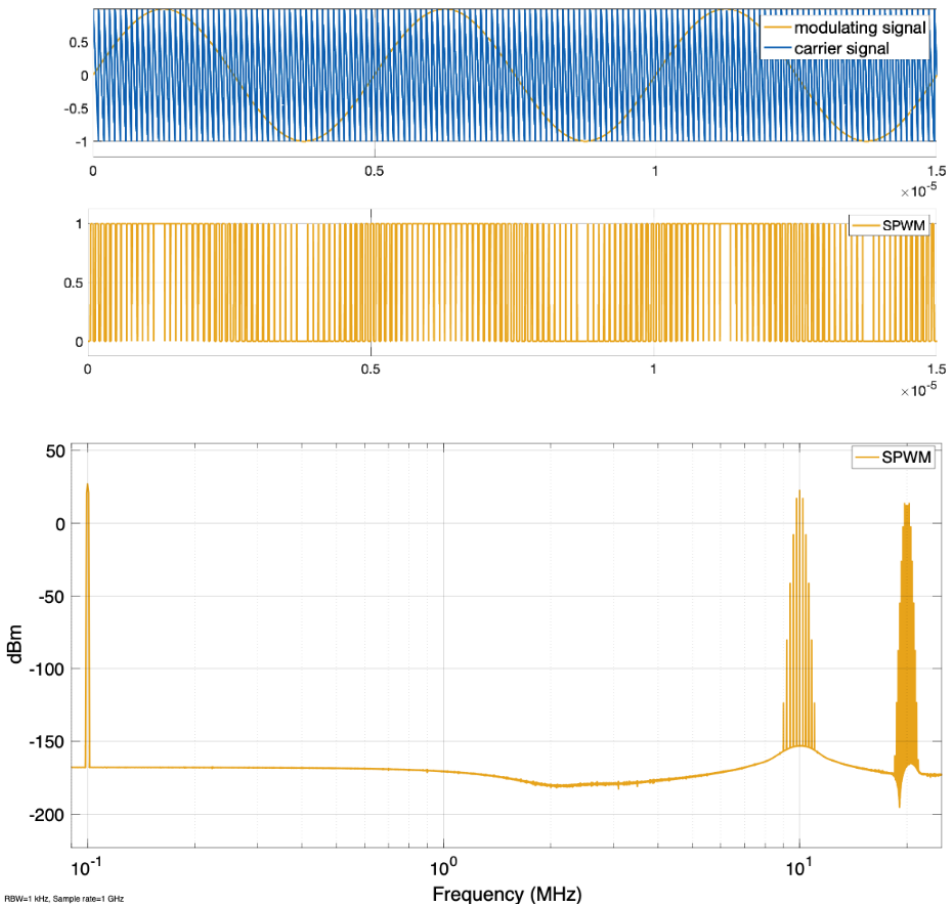

Figure 3-1 Time-domain SPWM signal and spectrum

Figure 3-1 shows a naturally sampled SPWM signal in the time domain and frequency spectrum. The naturally sampled SPWM compares the modulation signal with a carrier

signal, which has a high output when the modulation signal is larger than the carrier signal and vice versa. The figure shows the AD modulation scheme, where the SPWM signal has two levels. As in the figure, the SPWM does not produce additional in-band harmonics but instead generates high-frequency tones at the multiple of the carrier frequency. By filtering out the high-frequency PWM tones, a sinusoidal wave is recovered from the SPWM. This principle is widely used in class-D audio amplifiers [22]. Furthermore, the SPWM does not require a sophisticated DAC, can be driven by a digital inverter, and exhibits an excellent signal-to-noise ratio. Therefore, the SPWM-based system is expected to provide excellent performance intuitively. This work explores the SPWM excitation scheme.

3.1.2 Introduction to synchronous detection

Synchronous detection can extract an AC signal, which is widely used in communication systems and precision analog systems. It gives the system a very narrow measurement bandwidth so that it can collect signals in a high-noise or high-interference environment.

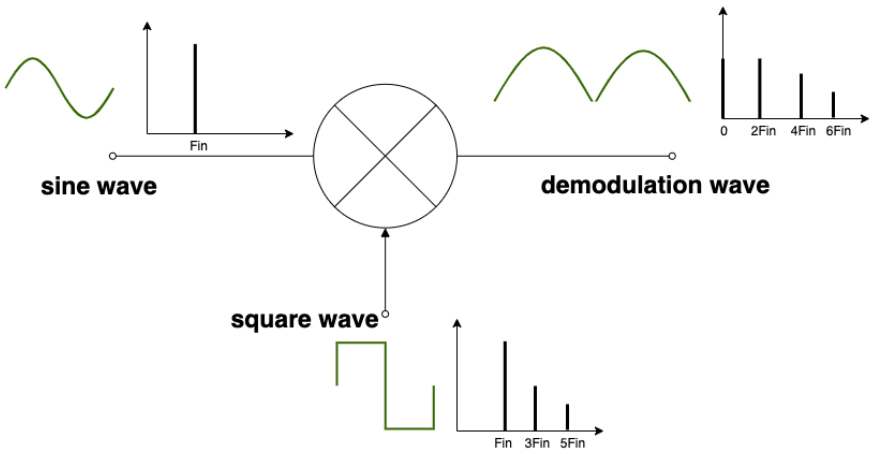

Figure 3-2 Working principles of synchronous detection

Figure 3-2 illustrates the working principles of synchronous detection. The system multiplies an AC signal ($A\sin(\omega t + \theta)$) with a synchronized clock ($\sin(\omega t)$). The products are a DC signal ($\cos(\theta)$) and doubled frequency signal ($\cos(2\omega t + \theta)$), which is described as the product-to-sum rule in Eq. (8).

$$A\sin(\omega t + \theta)\cdot\sin(\omega t) = \frac{A}{2}(-\cos(2\omega t + \theta) + \cos(\theta)) \qquad (8)$$

The equation shows that the DC signal depends both on the amplitude (A) and phase difference (θ). Consequently, phase shifts in the readout due to non-idealities cause measurement errors. To avoid these errors, a second measurement is performed with a 90° phase-shifted demodulation clock.

$$A\sin(\omega t + \theta)\cdot\sin\left(\omega t + \frac{\pi}{2}\right) = \frac{A}{2}\left(-\cos\left(2\omega t + \theta + \frac{\pi}{2}\right) - \sin(\theta)\right), \qquad (9)$$

After some mathematics, the phase shift (θ) and absolute amplitude (A) can be found:

$$\theta = \frac{Img}{Real} = \tan^{-1}\left(\frac{-\frac{A}{2}\sin(\theta)}{\frac{A}{2}\cos(\theta)}\right) \qquad (10)$$

$$A = 2\cdot\sqrt{Real^2 + Img^2} = 2\cdot\sqrt{\left(-\frac{A}{2}\sin(\theta)\right)^2 + \left(\frac{A}{2}\cos(\theta)\right)^2} \qquad (11)$$
$$= A\sqrt{\sin(\theta)^2 + \cos(\theta)^2}$$

where $Real$ is the DC signal when demodulated with an in-phase clock and Img is the DC signal when demodulated with a 90˚ phase-shifted clock.

3.1.3 The influence of harmonic distortion

Synchronous detection produces a measurement error when the demodulation clock and the modulation signal have overlapping harmonics. The overlapping harmonics also fold back to the baseband. As in Eq. (8), the error depends not only on the harmonic amplitude but the harmonic phase. Although the pulse width modulation does not produce additional in-band harmonics, the modulation signal contains harmonic distortion. Thus, it is necessary to exam the harmonic phase property.

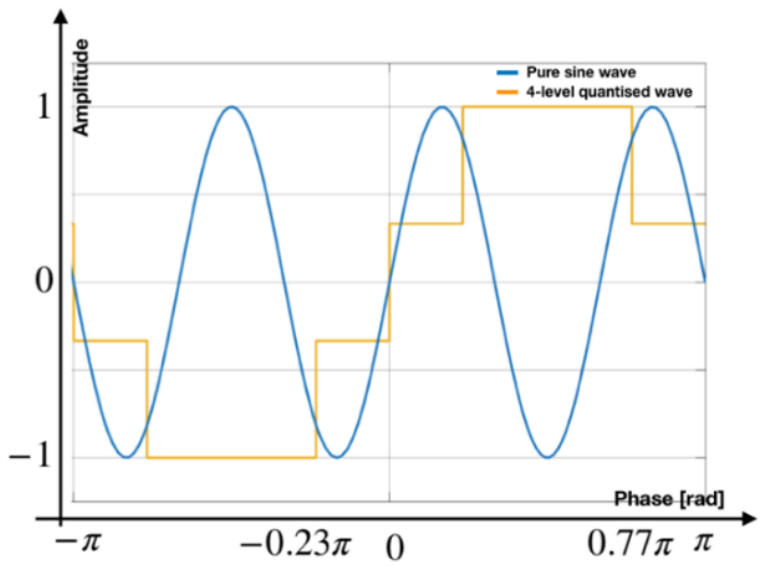

Figure 3-3 Four-level quantized sinusoidal wave used in the simulation

The calculation of harmonic power density distribution has been frequently described in the literature [23] [24], but no study has taken the harmonic phase shift into account. To understand the phase property of the signal harmonics, simulations and mathematical deviations are performed.

Take the four-level sine wave in Figure 3-3 as an example; the harmonics are calculated by deriving the Fourier series, as in Eq. (12). The first seven calculated harmonics are plotted in Figure 3-5 as the red series. The even harmonics are zero because of the signal symmetry. The negative harmonics have a 180° phase shift, which occurs at the third, fifth, and 13th harmonic order.

$$
\begin{aligned}
b_n = \frac{1}{\pi}\Bigg[& \int_{-\pi}^{-0.77\pi} -0.67\sin(nt)dt \\
& + \int_{-0.77\pi}^{-0.23\pi} -2\sin(nt)dt + \int_{-0.23\pi}^{0} -0.67\sin(nt)dt \\
& + \int_{0}^{0.23\pi} 0.67\sin(nt)dt + \int_{0.23\pi}^{0.77\pi} 2\sin(nt)dt \\
& + \int_{0.77\pi}^{\pi} 0.67\sin(nt)dt \Bigg] \\
= & \frac{1}{-n\pi}\left[2.67\cos(0.77\pi n) + 1.33\cos(\pi n)\right. \\
& \left. - \ 2.67\ \cos(0.23\pi n) - \ 1.3\ \cos(0)\right]
\end{aligned}
\tag{12}
$$

The testbench in Figure 3-4 could simulate the phase of the harmonics.

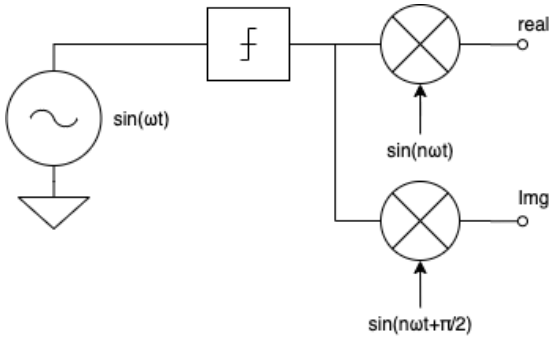

Figure 3-4 Simulation of harmonic phase properties

Because of the properties of the tangent function, Eq. (10) cannot distinguish between 0˚ and 180˚. Instead, Eq. (13) is used to compute the phase of the harmonics in the simulation.

$$\theta = \cos^{-1}\left(\frac{Real}{\sqrt[2]{Real^2 + Img^2}}\right) \tag{13}$$

The blue series in Figure 3-5 shows the simulated phase for the same waveform, which leads to the same results as in the mathematical model. Thus, the four-level sine wave has harmonics with a 180° phase shift.

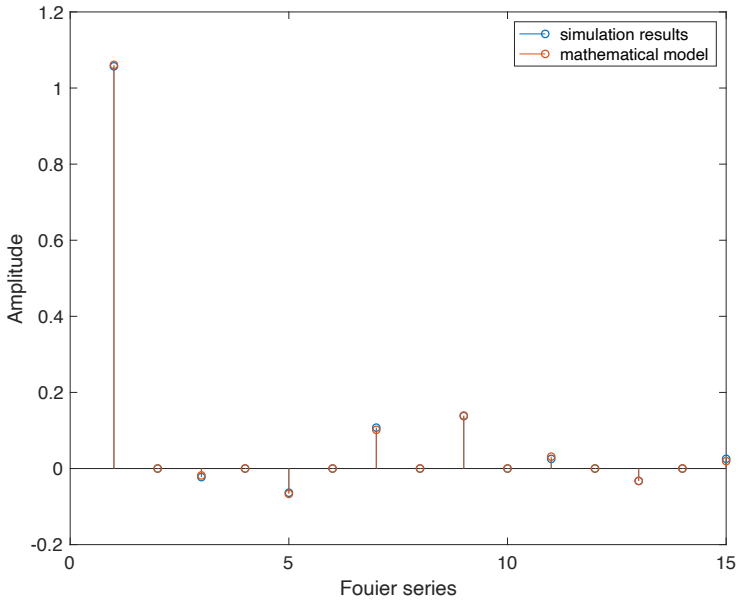

Figure 3-5 Harmonics of the four-level quantized sine wave

Then, the simulations are performed for different quantization levels, as in Figure 3-6. All of the quantization levels except the two-level quantized sine wave have harmonics with a phase shift, and the phase-shifted harmonics vary with the quantization level. The figure shows no apparent pattern. Therefore, both the harmonic amplitude and the phase must be taken into consideration when calculating the demodulation errors.

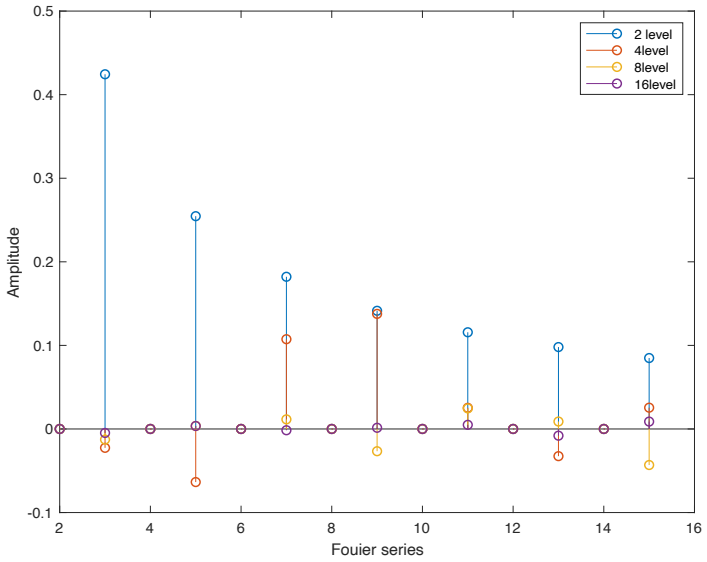

Figure 3-6 Harmonics of four-level, eight-level, and 16-level quantized sine waves

3.1.4 The proposed readout system

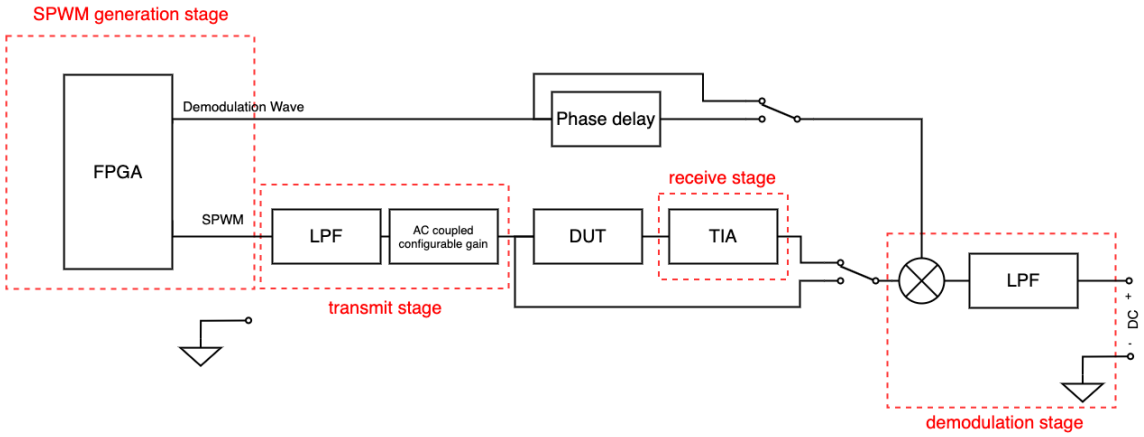

Figure 3-7 System block diagram of the proposed sensor readout system

Figure 3-7 shows a full system block diagram of the proposed readout system, where the device under test (DUT) represents the soil chip. The system comprises four primary stages: the SPWM generation stage, the Transmit stage, the Receive stage, and the Demodulation stage. The SPWM generation stage produces the excitation signal from an FPGA. The Transmit stage removes the high-frequency PWM signal

and sets the correct signal amplitude. The Receive stage measures the sensor current. Finally, the Demodulation stage extracts the AC signal, which uses the synchronous detection scheme.

3.2 Design of the SPWM generation stage

Using the correct modulation scheme ensures that the SPWM signal covers the full frequency range. The amount of harmonics in the SPWM signal impacts the measurement error, which is explained in Section 3.2.3.

3.2.1 SPWM modulation scheme

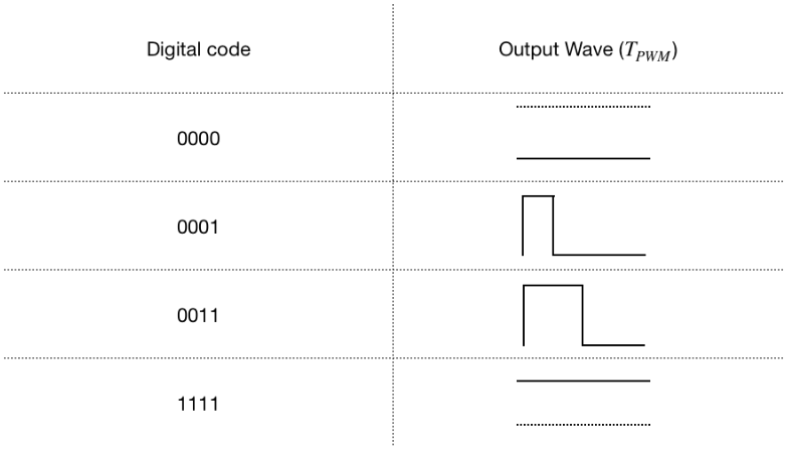

Figure 3-8 Convert binary code into PWM waves.

There are multiple ways of modulating a digital SPWM signal. One common way is to convert the binary code into a two-level wave, as in Figure 3-8, where a four-bit digital code is converted into a PWM wave. In this way, the FPGA requires a clock at least N times the carrier frequency to represent an N-level wave. Furthermore, the carrier frequency needs to be at least N times higher than the signal frequency to fit N PWM cycles into one period.

To estimate the required quantization level, a simulation is performed using the testbench in Figure 3-11 with a quantized sine wave. The system requires a sine wave with approximately 64 quantization levels and an error of lower than 0.65%. To produce such a signal at 1MHz, a clock of $64 * 1MHz * 64 \approx 4GHz$ is required. Since accurately generating a Giga-Hz frequency clock from a modern FPGA is highly difficult, this modulation scheme is not suitable for producing the required SPWM wave.

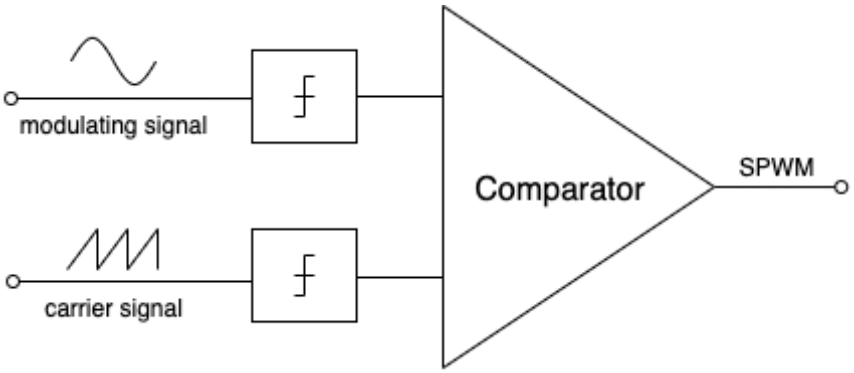

Figure 3-9 SPWM modulation scheme

Another modulation scheme, as represented in Figure 3-9, uses a digital comparator. Unlike the naturally sampled PWM, in this case, the modulation signal and carrier signal are sampled and held, which is the so-called uniformly sampled pulse width modulation [25].

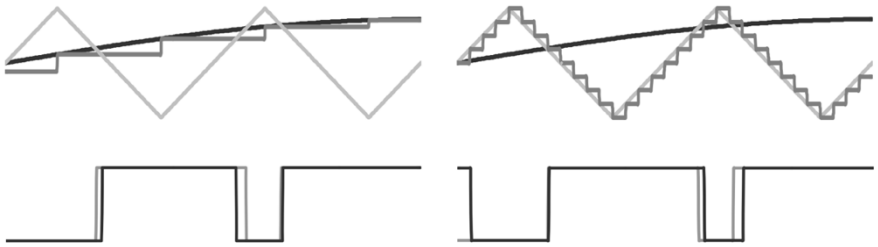

Figure 3-10 Digital PWM sampling error and quantization error [22]

Two types of error can occur, as illustrated in Figure 3-10 [22]. The first type of error occurs when the discontinued modulation signal intercepts the carrier wave at a different place than a continuous signal. The error refers to the sampling error [22]. The second error occurs when the quantized carrier wave causes distortion, which is described as a quantizing error because the pulse width is quantized to a few discrete values [22]. Both of these errors should be taken into account when evaluating the quantization noise of the digital SPWM. Increasing the quantization level of the modulation signal or the carrier wave helps to reduce the quantization noise in this SPWM signal.

$$F_{clock} = n \cdot F_{signal} \tag{14}$$

The quantization level is limited by the signal frequency and the clock speed. Eq. (14) shows that to have an n quantization level, the system needs a clock that is n times higher than the signal frequency. Increasing the quantization level of the modulation

signal is more manageable than the carrier signal since it is at a lower frequency than the carrier signal. The required quantization level for the modulation signal and carrier signal is simulated and explained in Section 3.2.3.

3.2.2 SPWM carrier frequency

The lower boundary of PWM carrier frequency is at least double the modulation signal frequency, so the carrier frequency should be at least 2 MHz. If the PWM carrier frequency is too close to the signal band, the LPF may struggle to attenuate the high-frequency PWM tones.

The FPGA clock speed limits the upper boundary. The modern FPGA can create a clock within the range of a few hundred MHz by utilizing an onboard PLL. The carrier signal should have more than 64 quantization levels. Thus, the PWM carrier frequency is placed around 10 MHz, where the required clock is around 640 MHz, as demonstrated in Eq. (14).

The exact location of the carrier frequency should preferably be at the frequency that misaligns with the signal's odd harmonics, as in this way, the demodulator picks up the fewest PWM tones. The PWM tones comprise the PWM carrier frequency and the intermodulation between the carrier frequency and input signal.

The system produces five different sinusoidal frequencies per decade, such as 100 kHz, 200 kHz, 400 kHz, 600 kHz, and 800 kHz in the hundreds of kHz range. The odd harmonics of these modulation signals are at 10 MHz, 10.2 MHz, 10.4 MHz, 10.6 MHz, and 10.8 MHz, for which the PWM tones should be avoided. The Transmit stage uses a carrier frequency of 10.3 MHz.

3.2.3 The amount of harmonics in the SPWM

The high-frequency PWM tones are removed by an LPF. The in-band harmonics in the modulation signal cause errors when measuring complex impedance. If the DUT is purely resistive, the harmonics do not intrinsically cause any error because the impedance is constant over frequency, as in Eq. (15).

$$R = \frac{V}{I} = \frac{\sin(\omega t) + \sin(3\omega t) + \sin(5\omega t) + \ldots}{\frac{1}{R}\left(\sin(\omega t) + \sin(3\omega t) + \sin(5\omega t) + \ldots\right)} \tag{15}$$

However, for a complex electrical impedance network, the impedance varies with frequency. These harmonics excite the DUT at a different frequency from the fundamental frequency. The harmonics then cause a measurement error, as in Eq. (16). Thus, the harmonic error required for the excitation signal must be identified.

$$Z(\omega) = \frac{V}{I} \neq \frac{\sin(\omega t) + \sin(3\omega t) + \sin(5\omega t) + \ldots}{\frac{\sin(\omega t)}{Z(\omega)} + \frac{\sin(3\omega t)}{Z(3\omega)} + \frac{\sin(5\omega t)}{Z(5\omega)} + \cdots} \tag{16}$$

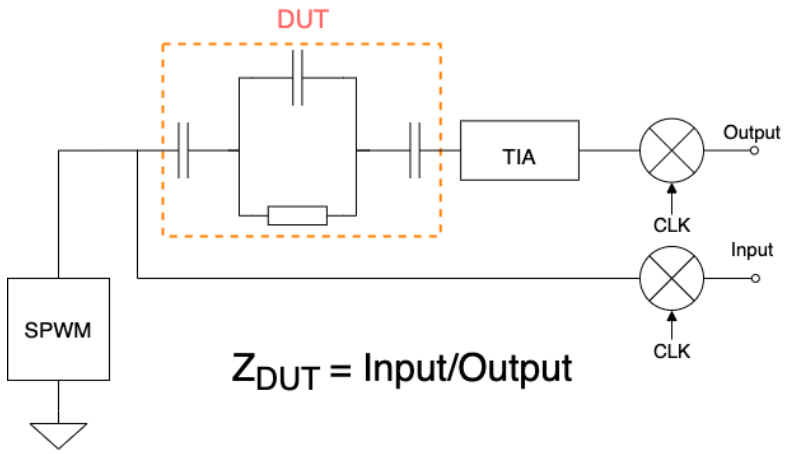

Figure 3-11 Testbench of harmonic error simulation

As mentioned in Section 3.2.1, the system expects a sine wave with approximately 64 quantization levels, so it requires a clock of around 660 MHz, which can generate a nine-bit sine wave at 1 MHz. However, a nine-bit sine wave and 64-level carrier signal, using the modulation scheme in Figure 3-9, do not give the desired error. Thus, the carrier signal increases the quantization level to 66. A simulation is performed with the testbench in Figure 3-11, using the SPWM signal. The square signal is used as the demodulation signal, the reason for which is explained in Section 3.5.1. Table 3-1 presents the simulated harmonic error.

Table 3-1 Harmonic error at different impedance corners

Error [%]	1 kHz	1 MHz
10 MΩ 10 pF	0.64	0.042
10 MΩ 500 pF	0.01	0.2683
100 Ω 10 pF	1E–05	0.0098
100 Ω 500 pF	0.00049	0.302

3.3 The transmit stage

3.3.1 The PWM attenuation LPF

The PWM-associated signals do not affect measurement accuracy, as explained in the previous section. The PWM attenuation LPF protects the sensor electrode from redox reactions. The PWM tones are one decade higher than the highest signal frequency. The absolute impedance of the sensor at the PWM frequency is approximately 20 dB lower than the signal frequency because the sensor network has a first-order roll-off from 1 MHz. The electric current caused by the PWM tones can exceed the sensor electrodes' limits. Thus, the LPF attenuates the high-frequency components, so it does not exceed the signal limit. According to Simulink simulations, the filter needs to be 3rd order, which cuts off at 2 MHz.

3.3.2 The AC coupled attenuator

Since the SPWM runs from zero to power supply level, the Transmit stage should remove the common-mode voltage in the SPWM in order to protect the sensor from the redox reaction. Moreover, this block sets the correct signal amplitude, which is similar to the benchmark system's 500 mV_{pp} and 20 mV_{pp}.

3.3.3 The output impedance of the transmit stage

Although the classic four-wire impedance measurement method is more robust against the series resistance than the two-wire, as shown in Figure 3-12, the soil sensor must use a two-wire setup, as explained in Chapter 1. Therefore, the system needs to consider any series resistance with the DUT, especially when the DUT is small.

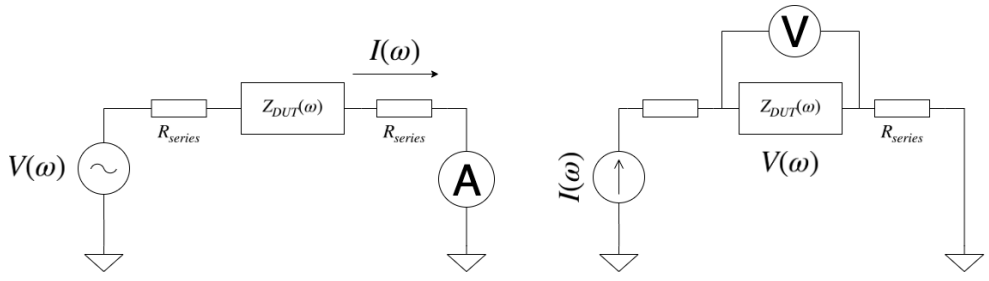

Figure 3-12 Comparison of the two-wire setup and the four-wire setup

The error of the Transmit stage output impedance is resolved by the second signal path that connects the "sensor_in" node to the Demodulation stage, as shown in Figure 3-7. In this way, the system can measure the exact voltage at the "sensor_in"

node, even if the voltage is attenuated due to the loading effect. This also confers the advantage that the system is insensitive to any constant gain errors from the Transmit and Demodulation stages. Because both the excitation voltage and TIA output experience the same gain in these two stages, the division operation cancels out the gain error when calculating impedance.

3.4 The receive stage

The Receive stage is a trans-impedance block, which prepares the sensor current for demodulation, by converting the electric current into a voltage signal.

Again, due to the usage of the two-wire measurement setup, the input impedance of TIA is critical. When $|Z_{DUT}| \approx 100\Omega$, an input impedance of one ohm could lead to a 1% measurement error. The input impedance of a TIA increases with the frequency because the operational amplifier (op-amp) has a limited gain-bandwidth product (GBW). Therefore, the error caused by the input impedance would be highly significant at a high frequency and low sensor impedance. As demonstrated in Table 3-1, the system could have a harmonic error of approximately 0.3% at low sensor impedance and high frequency, and the input impedance should be smaller than 0.7 Ω to avoid exceeding the 1% error budget.

3.5 The demodulation stage

The Demodulation stage uses synchronous detection to measure an AC signal. The choice of demodulation wave is discussed in Section 3.5.1. Section 3.5.2 explains the design parameters of the LPF, such as the filter cutoff frequency and order.

3.5.1 Choice of the demodulation signal

There are two options for the demodulation signal: the square wave and the SPWM signal. Depending on the harmonic property of the demodulation signal, different errors are expected. A simulation is performed to explore this error difference, as represented in Figure 3-13. To simplify the computation, the SPWM is represented by a quantized sinusoidal signal in the simulation. Then, the simulation is performed for different quantization levels.

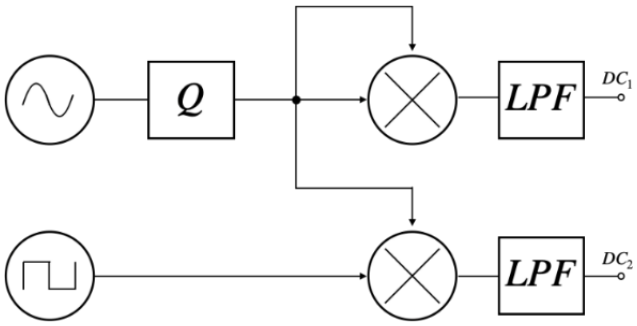

Figure 3-13 Simulation of a comparison of demodulation waves

Figure 3-14 illustrates that both errors decrease as the modulation signal quantization level increases. However, the error of demodulation with a quantized sine wave is more significant than a square wave.

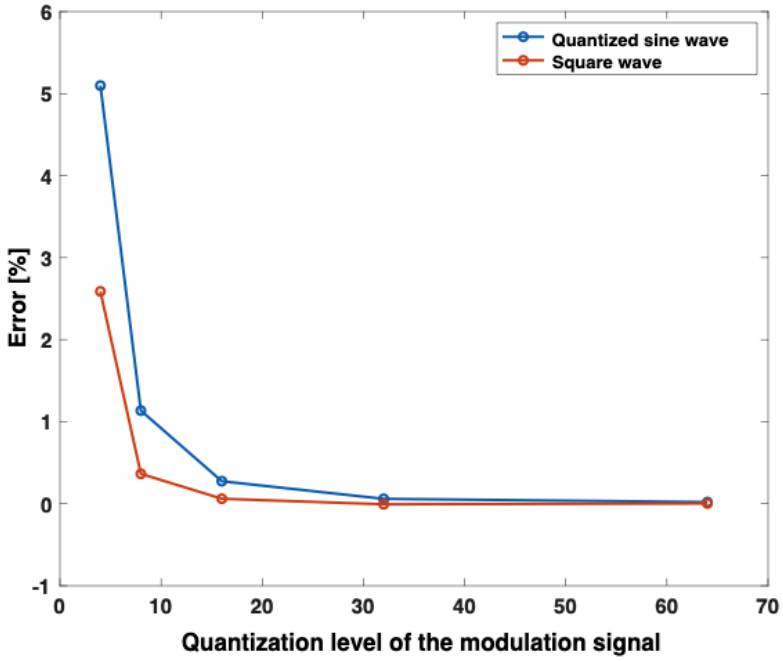

Figure 3-14 Comparison of the demodulation error for the quantized sine wave and square wave

The reason for this is the harmonic phase difference between the modulation signal and the demodulation signal. As introduced in Section 3.1.3, some harmonics are 180˚ phase-shifted when the quantization level is higher than two. If two quantized sinusoidal waves multiply with each together, all harmonics fold back to the baseband addictively. When using a square wave demodulates a quantized sine wave, the harmonics with 180˚ phase shifts fold back to the baseband subtractively. In this way, the demodulation error compensates for itself when demodulating with a square wave.

3.5.2 DC extraction LPF

DC extraction LPF extracts the DC signal after demodulation. Since the signal after demodulation comprises frequency components that double the input signal, ripples will be observed if attenuation is insufficient. The lowest excitation frequency is 1 kHz, so the cutoff frequency should be lower than the 2 kHz.

In addition, the passband of this filter determines the system noise bandwidth. If the cutoff frequency is too high, the system suffers from a high noise bandwidth. In contrast, the system will require a longer settling time if the cutoff frequency is too low. A second-order LPF cuts off at 10 Hz, giving 66 dB attenuation at around 1 kHz, for which the ripples create a 0.05% error in the worst-case scenario. This 0.05% error allows the system to have a worst-case error of 1%, which is explained in Section 3.6.

3.6 Conclusion

Table 3-2 presents a summary of the significant error sources at different measurement conditions. Based on Table 3-2, the proposed system is expected to have a worst-case measurement error of 1%, which is at high impedance and low frequency, or low impedance and high frequency. For high impedance and low frequency, the dominant error sources are the harmonic error and the noise due to the low signal level, whereas, for low impedance and high frequency, the dominant error sources are the TIA input impedance and harmonic error.

Table 3-2 Summary of the error sources

	TIA input impedance	Harmonic error	Noise	Residual ripples
Low frequency, low impedance	-	-	-	0.05%
High frequency, low impedance	0.7%	0.3%	-	-
Low frequency, high impedance	-	0.65%	0.3%	0.05%
High frequency, high impedance	-	0.27%	-	-

Chapter 4 Block-level design of the proposed readout system

In the previous chapter, requirements with regard to the individual blocks of the proposed system have been derived. This chapter will focus on the design of the overall readout system.

4.1 FPGA design

The FPGA generates an SPWM signal with a carrier frequency of 10.3 MHz. The modulation signal is encoded in a 9-bit digital sine wave, whose frequency ranges from 1 kHz to 1 MHz. In addition, the FPGA needs to produce the demodulation clock signal and other control clock signals. The design has been built using a basic FPGA development board called De0–Nano [26].

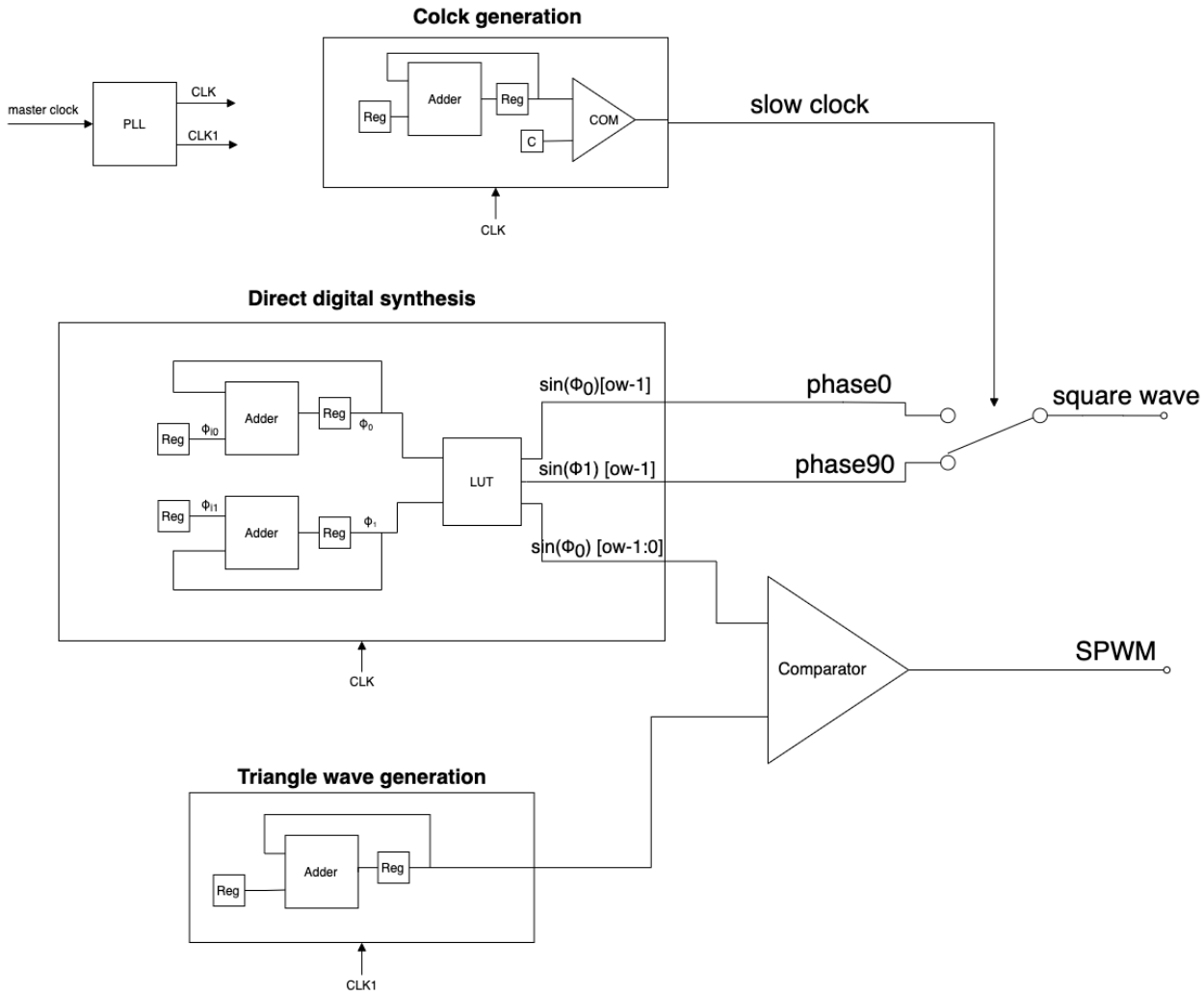

Figure 4-1 System block diagram of digital SPWM generation

Figure 4-1 shows the full system diagram for the FPGA design, which comprises three significant parts: the direct digital synthesis (DDS) stage generating a digital sinusoidal, the triangle wave generator, and a clock generator.

4.1.1 Direct digital synthesis

The DDS has two main parts: a phase accumulator and a sinusoidal wave lookup table (LUT). As its name suggests, the phase accumulator is a counter that increases by a specific phase step at every cycle. Changing either of the clock frequency or phase step changes the signal frequency produced. Eq. (17) calculates the phase step for achieving a specific frequency:

$$\Delta\Theta = \frac{2^N \cdot f_{\mathrm{Hz}}}{f_{\mathrm{clock}}} \tag{17}$$

where N is the number of bits in the phase register, f_{Hz} is the signal frequency, and f_{clock} is the FPGA clock.

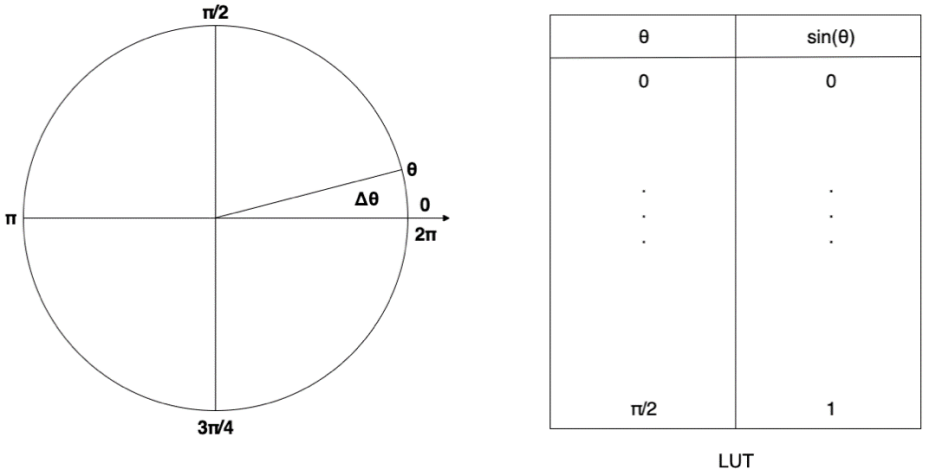

Figure 4-2 phase accumulator and sine-wave lookup table working principle

The phase accumulator output is fed into a sine-wave lookup table (LUT), as in Figure 4-2. The LUT converts the current phase into a sine-wave entry. Only a quarter of the sine-wave entry needs to be stored in the LUT because a full sinusoidal wave can be recovered by varying the sign, exploiting the sine function's symmetry, as explained in Figure 4-3.

Besides the SPWM wave, the FPGA needs to generate two square waves that are synchronized with the sine wave but separated by a 90° phase shift. The top bit of the digital sine wave inherently provides a square wave synchronized with the sine wave

because it changes its polarity every half-period. By adding a phase offset to that initial phase register, the FPGA can generate the second square wave with a 90° phase offset, as shown in Figure 4-1.

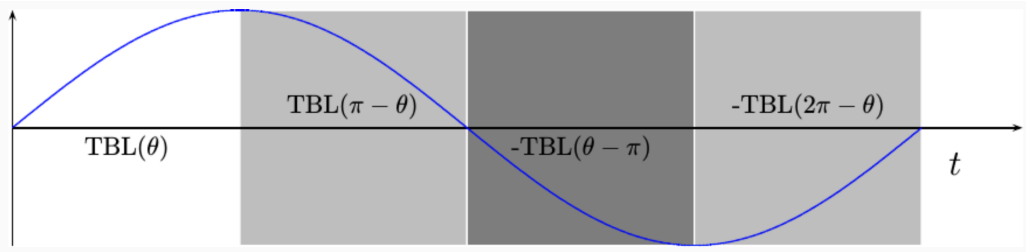

Figure 4-3 Sine-wave symmetry [27]

4.1.2 Triangle wave and clock generation

The triangle wave is the carrier signal for the PWM modulation. The triangle wave generator is simply a counter that adds one step to the current register at every clock cycle. When the register overflows, it resets itself and starts from zero again. This piecewise linear cycle provides the required triangle wave. The required wave frequency is 10.3 MHz with 66 steps, so the clock for the accumulator is 659.2 MHz. The onboard PLL generates this clock from an onboard oscillator.

The clock is for controlling distinct signal paths and switching square wave phases. Since the lowest cutoff frequency in the analog system is 10 Hz, the clock needs to run slower than 10 Hz. The onboard PLL cannot achieve such a low frequency, so the system uses another counter to generate the control signal. Whenever the counter is full, the output reverses its polarity, as shown in Figure 4-1. This process produces a slow clock, configurable by setting the counter size and the driving clock's frequency.

4.2 Analog circuit design

4.2.1 Transmit stage

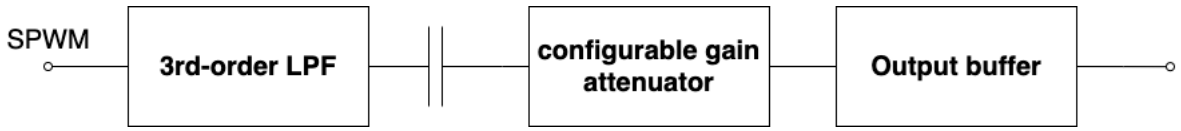

Figure 4-4 System block of the transmitting stage

Figure 4-4 reviews the functional block in the Transmit stage. The LPF attenuates the high-energy and high-frequency PWM tones at 10.3 MHz. As shown in Figure 4-5, the 3rd-order LPF comprises a 1st-order RC filter cascading into a 2nd-order LPF in a Sallen–Key topology. The cutoff frequency is 2 MHz.

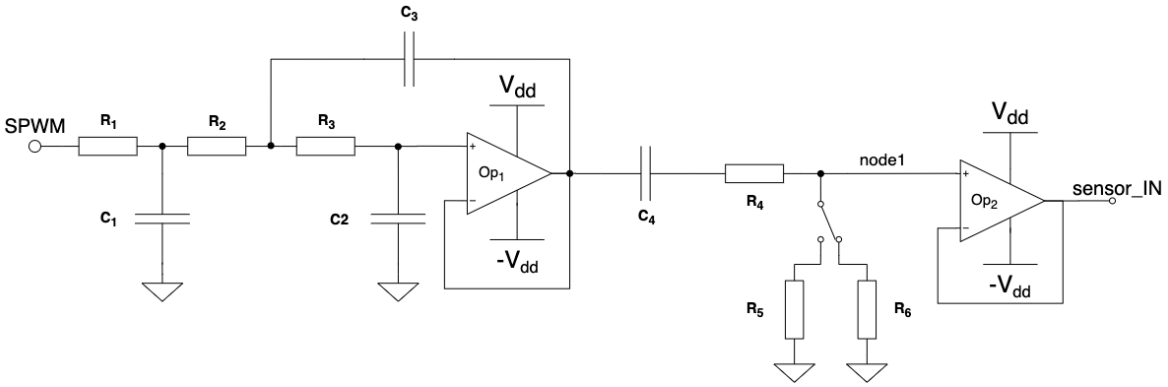

Figure 4-5 Circuit design of the transmit stage

The AC coupling capacitor C_4 removes the common-mode voltage. The configurable attenuator is realized with a resistor divider (R_4, R_5, and R_6) with an SPDT switch. A design procedure similar to that used for the benchmark system applies here. The bandwidth-limiting pole formed by the resistive divider and the input capacitor at "node1" should be above the signal 1 MHz. Here, the pole locates at 2 MHz, aligning with the LPF cutoff frequency. Capacitance C_4 determines the HPF corner, which is 10 Hz. The calculated values are displayed in Table 4-1. A unity-gain buffer drives the sensor. Because of the AC coupling, the buffer needs to work under dual supply voltages. The sensor itself imposes a high capacitive load (500 pF) under some conditions, so the buffer needs to drive this level of capacitive load. The ADA4625 [19] has been used as op-amp "Op_2".

Table 4-1 Components value in the transmit stage

R_1	866 Ω	**C_1**	100 pF	**Op_1**	AD8021
R_2	3.48 kΩ	**C_2**	100 pF	**Op_2**	ADA4625
R_3	1.3 kΩ	**C_3**	13 pF		
R_4	10.3 kΩ	**C_4**	1 μF		
R_5	1.83 kΩ				
R_6	62 Ω				

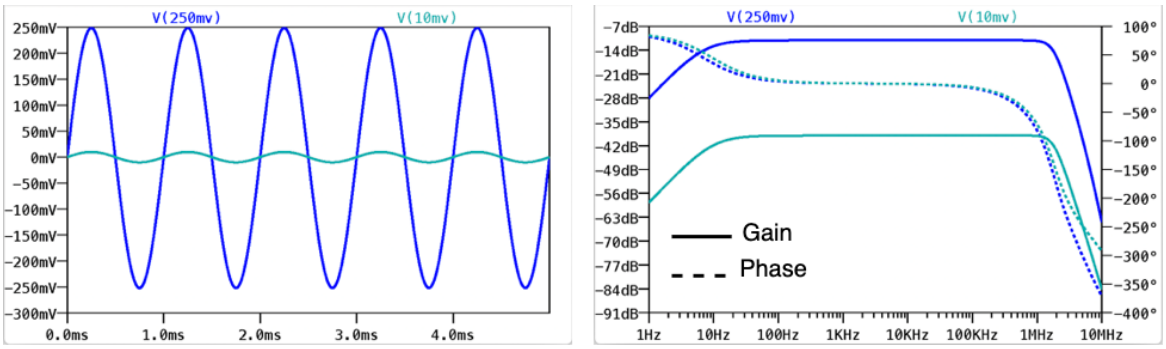

Figure 4-6 Spice simulations of the transmit stage

Figure 4-6 shows the Spice transient and AC simulations from the "SPWM" node to the "sensor_IN" node. The transient simulation was performed at 1 kHz. This and the AC plot show that the Transmit stage works as intended over the spectrum.

4.2.2 Receive stage

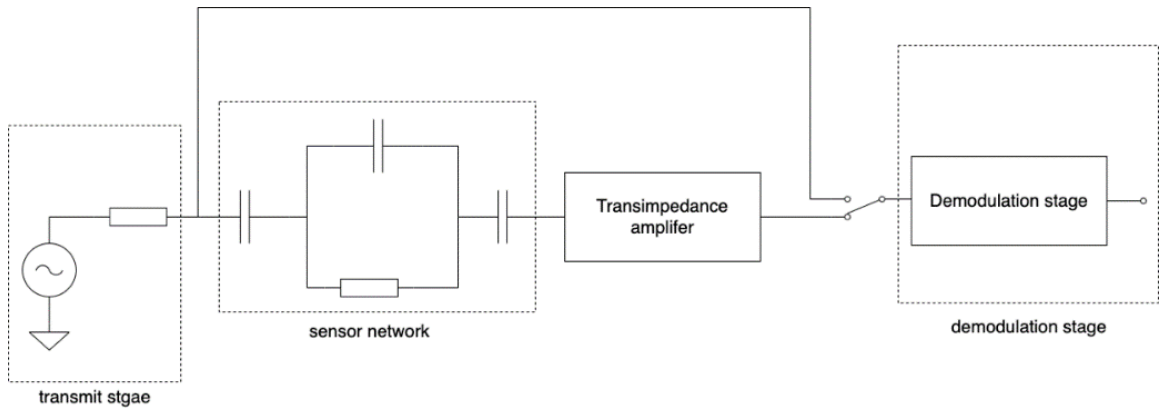

Figure 4-7 System blocks of the receive stage

The Receive stage is a transimpedance block (Figure 4-7) to which 0.65% transfer error is allocated in the system design. Since the transfer error depends on the transimpedance gain, this gain should be determined first. The ideal case would be to use the full signal swing to optimize the SNR (50 dB) so that the transimpedance gain is the full signal swing (300 mV headroom) divided by the most significant current swing. This gives $gain_{\mathrm{TIA}} = \frac{4.4\ \mathrm{V}}{200\ \mu\mathrm{A}} = 22\ k\Omega$.

Using the error function as in Eq. (5), we could estimate the required gain at 1 MHz in order to have the 22 kΩ TIA gain around 100 dB. This is not realistic, however, for an op-amp. Therefore, the Receive stage involves a two-stage design that includes a voltage gain block. This allows the TIA to achieve the target error of 0.65% while having a two-stage gain of 22 kΩ, as in Figure 4-8.

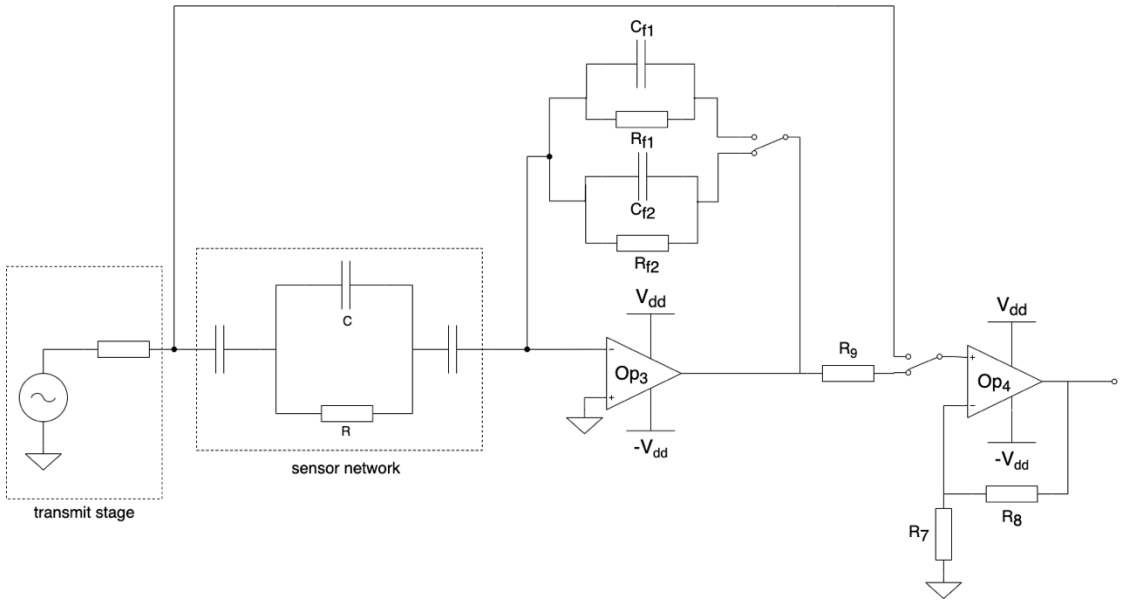

Figure 4-8 Circuit design of the receive stage

The voltage amplifier could also introduce gain errors because of the limited GBW of op-amp Op_3. Therefore, the voltage amplifier is inserted into the common signal path, as in Figure 4-8. This way, both signal paths experience the same gain error, and it does not influence the impedance measurement accuracy. Because of this property, the system should be designed to maximize this voltage gain. The signal swing when measuring the excitation voltage limits the voltage gain, which is equal to $\mathrm{gain_{vol}} = \frac{4.4\ \mathrm{V}}{500\ \mathrm{mV}} = 8.8\ V/V$. As a result, to achieve a two-stage gain of 22 kΩ, the TIA stage should have a gain of 2.5 kΩ.

Figure 4-9 shows the transfer error versus the feedback resistance (TIA gain), assuming 1 GHz GBW. Range I is when the lowest DUT is 100 Ω, and Range II is for 2.5 kΩ. The plot shows that the TIA gain should be below 340 Ω in Range I to keep the transfer error below 0.65%, assuming 1 GHz GBW. So, the TIA uses a different transfer gains for each of the excitation ranges: 330 Ω for Range I, and 2.49 kΩ for Range II.

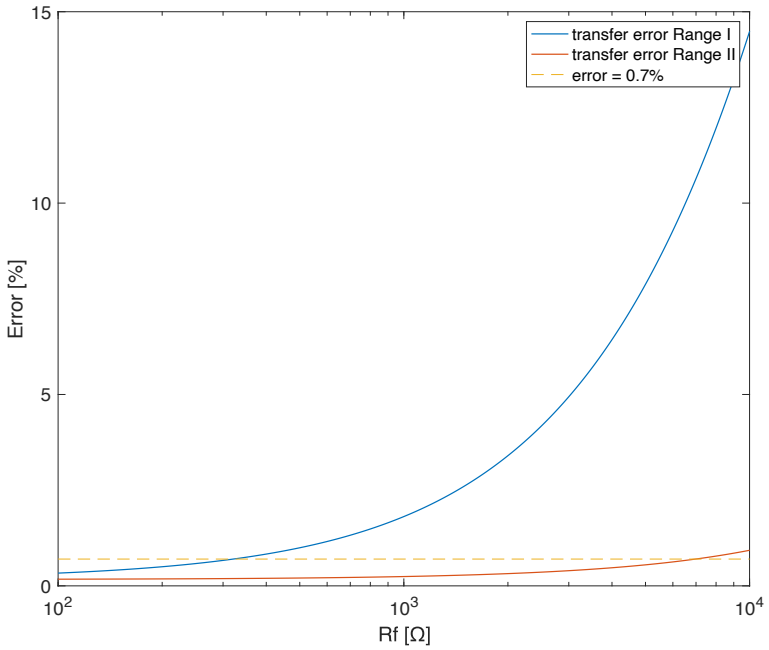

Figure 4-9 Error versus feedback resistor for the TIA

The requirements for op-amp Op_3 are: first, it needs to work under dual supply voltages; second, the input stage should have a low biasing current (FET input stage) to avoid offset voltage at the output; and third, the GBW should be around 1 GHz. One preference for Op_3 is unity-gain stability, as explained in the stability analysis. The ADA4817 [28] fulfills all the requirements and is used for Op_3.

Table 4-2 Component values in the receive stage

R_{f1}	330Ω	C_{f1}	16pF	Op_3	ADA4817
R_{f2}	2.49KΩ	C_{f2}	9pF	Op_4	OPA818
R_7	97.6Ω				
R_8	750Ω				

The next step is to calculate the compensation capacitance that ensures the stability of the TIA. The stability analysis of the TIA uses the transfer function of the AD4817 op-amp [28]. As explained in the previous chapter, the feedback resistor and the input capacitor form an extra pole in the loop gain. Placing a feedback capacitor compensates 45° phases at $1/(2\pi R_f C_f)$. The worst stability happens when a sensor

has a capacitance of 500 pF. Figure 4-10 shows the AD4817 open-loop gain and 1/β for two feedback resistances, which gives feedback capacitances 16 pF and 9 pF for R_f = 330 Ω and 2.49 kΩ, respectively.

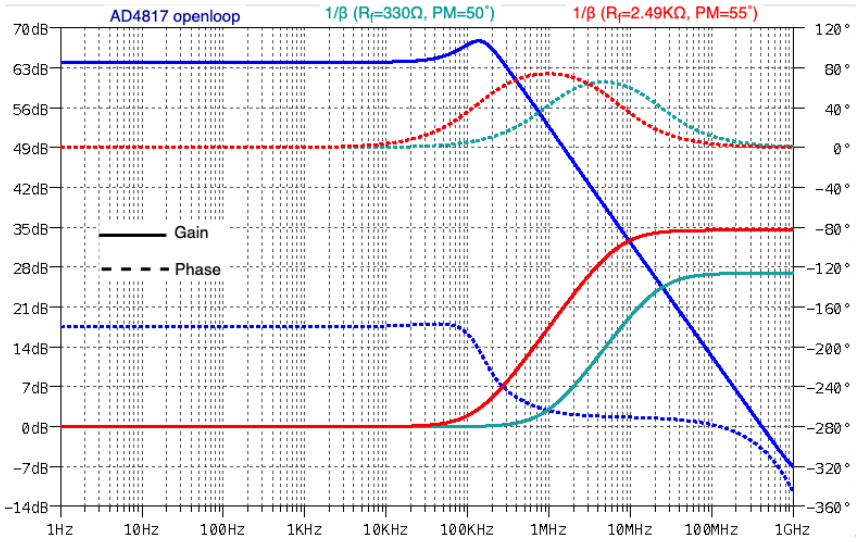

Figure 4-10 Op-amp open-loop gain and 1/β plot for Rf = 330Ω and Rf = 2.5KΩ

The reason for Op_2 having unity-gain stability is the potential instability hazard when the sensor capacitance is small. Taking $R_f = 2.5\ \text{k}\Omega$ and $C_f = 9\ \text{pF}$ for an example, as in Figure 4-11, the value of 1/β at high frequencies equals around 6 dB when C = 10 pF, and around 29 dB when C = 500 pF. If Op_2 requires a 10 dB gain to be stable, the red curve in Figure 4-11 starts oscillating. Therefore, Op_2 prefers to be a unity-gain stable amplifier, in case the sensor capacitance lies beyond the theoretical range.

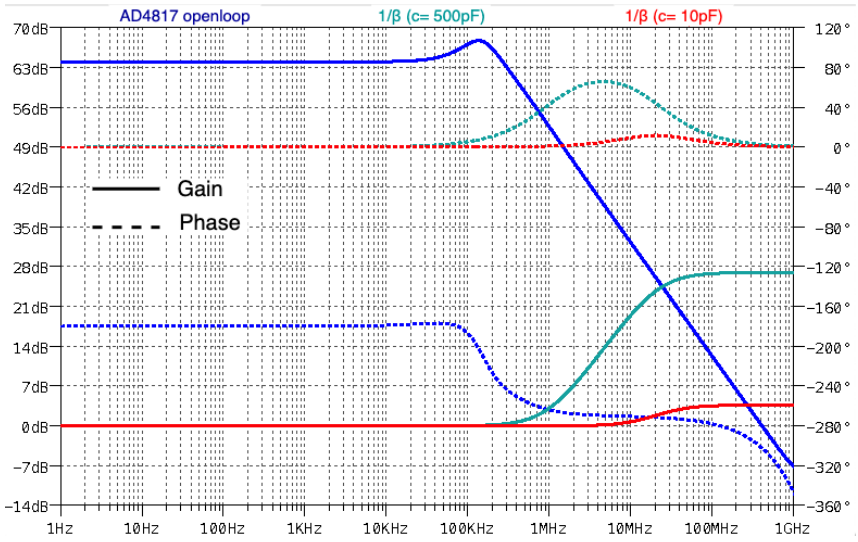

Figure 4-11 Op-amp open-loop gain and 1/β plot for sensor capacitance C = 500 pF and C = 10 pF when R_f = 330 Ω

Figure 4-12 shows the frequency response for two gain settings, which verifies that the TIA bandwidth is above 1 MHz in both settings.

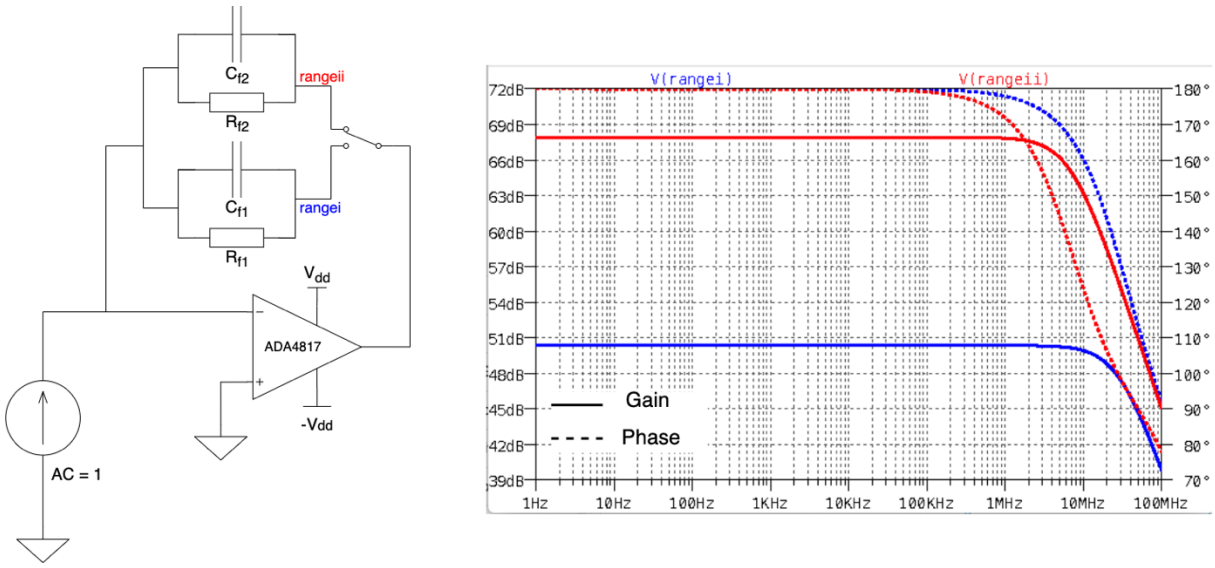

Figure 4-12 TIA frequency response

4.2.3 Demodulation stage

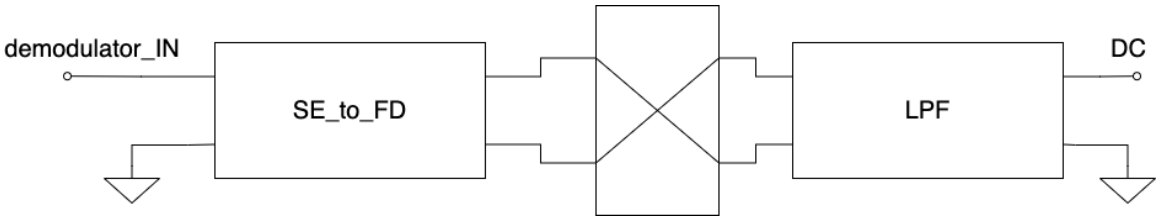

Figure 4-13 System block of demodulation stage

Figure 4-13 introduces the functional blocks in the Demodulation stage. First, the single-ended signal is converted to a fully differential signal. This gives the advantage of better matching between the chopping channels. Then, a chopper performs the demodulation. A LPF extracts the DC components after chopping and converts the differential signal into a single-ended signal.

As in Figure 4-14, the SE to FD conversion is achieved using a fully differential amplifier. The common-mode voltage at the amplifier output is determined by an external pin (REF). A voltage reference IC drives the pin to the $V_{dd}/2$ level to maximize the signal swing. The resistors after the feedback are to improve the capacitive load driving ability because the input capacitance of the switches, together with PCB traces, could potentially contribute 10 pF at nodes X1 and X2.

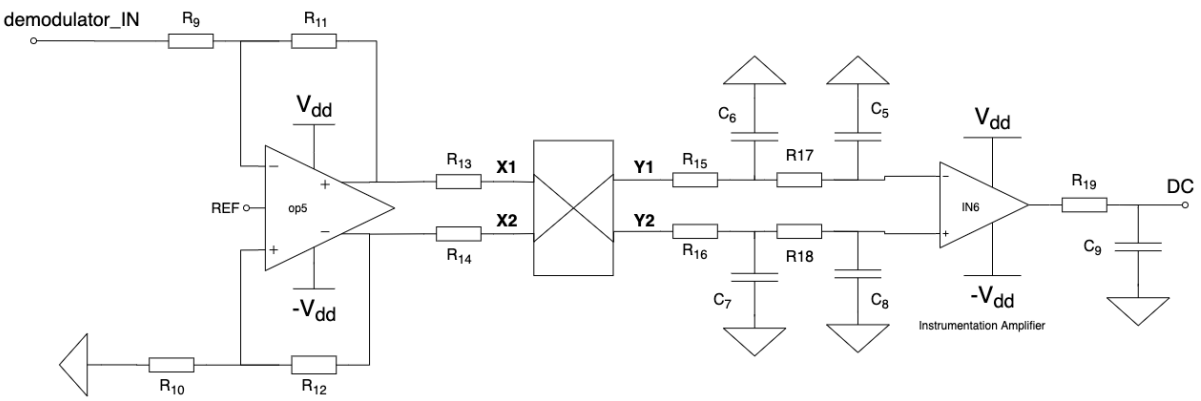

Figure 4-14 Circuit design of the demodulation stage

The onboard chopper is connected by two SPDT switches, as in Figure 4-15. Because the highest switching frequency is 1 MHz, the demodulator uses CMOS switches because mechanical switches would not work at such high frequency. The ADG787 switch [29] has been selected for its high-speed capability.

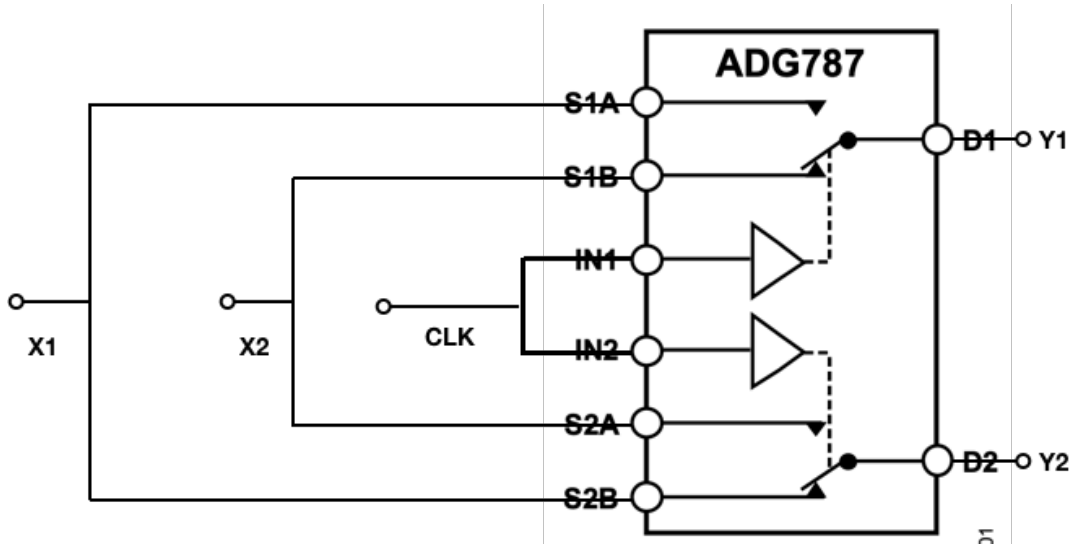

Figure 4-15 The chopper configuration by ADG787 [29]

Spice simulations were performed to verify the functionality of SE to FD conversion and the chopper switch. The simulation testbench supplies a sinusoidal wave at node "demodulator_IN" shown in Figure 4-14. The simulation covered the lowest and the highest signal level and was run at each of 1 kHz and 1 MHz. Figure 4-16 and Figure 4-17 show the simulation results at node "Y1" and "Y2" and "Y2" and "Y1" (Figure 4-14). So, the Spice simulations verify the functionalities of the Demodulator stage.

Table 4-3 Component values in the demodulator stage

$R_9 = R_{10}$	249 Ω	**$C_6 = C_7$**	660 nF	**Op5**	AD8139
$R_{11} = R_{12}$	499 Ω	**$C_5 = C_8$**	660 nF	**IN6**	LTC2053
$R_{13} = R_{14}$	43 Ω	**C_9**	440 nF	**Chopper**	ADG787
$R_{15} = R_{16} = R_{17} = R_{18}$	5 kΩ				
R_{19}	180 Ω				

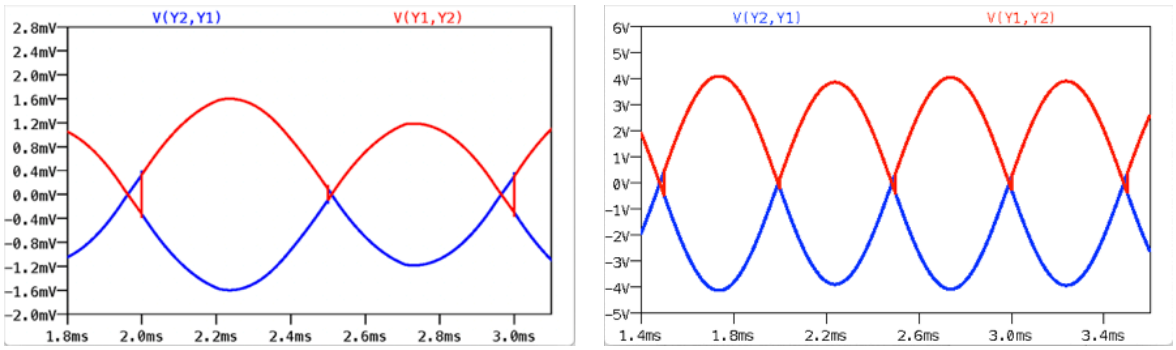

Figure 4-16 Demodulator simulation at 1KHz

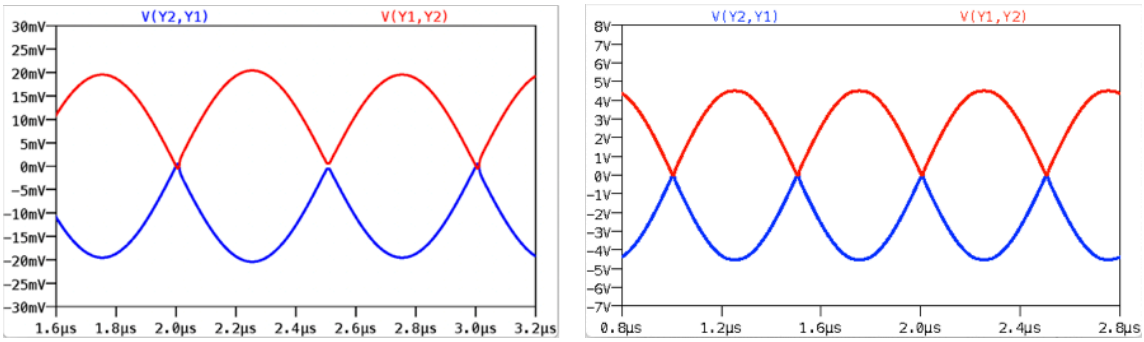

Figure 4-17 Demodulator simulation at 1MHz

The last part of the Demodulation stage is the DC LPF, which comprises a simple 2nd-order RC filter and a fully-differential to single-ended conversion block. The offset of this block is critical because it adds directly to the measurement. Due to chopping, offsets in front of the chopper are not essential if they do not clip the signal. Because the signal is at the baseband after demodulation, chopping again is not applicable. So,

controlling the offset of the DC LPF would be critical to the accuracy of the entire system.

The offset comes from multiple sources: the offset from the active device (the op-amp) and mismatches from the surrounding passive devices (resistors and capacitors). Modern op-amps have offsets in the magnitude of tens of microvolts. But mismatch due to improperly chosen architecture could cause a significant offset.

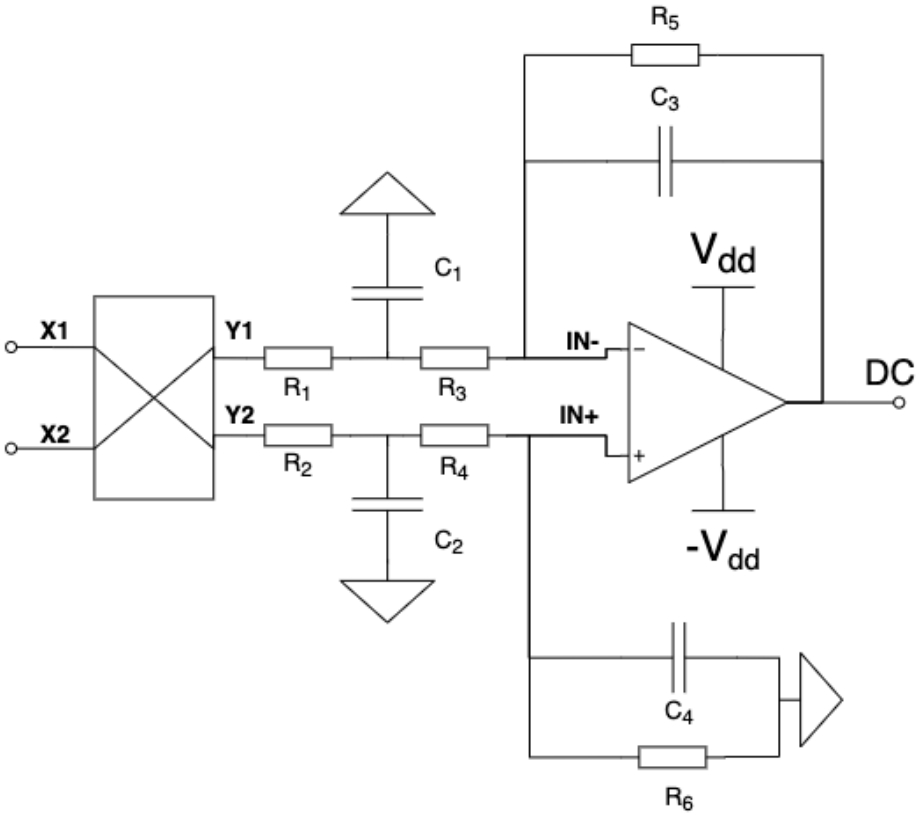

Figure 4-18 Common design of a fully-differential to single-ended conversion MFB LPF

Figure 4-18 shows a typical design for a 2nd-order LPF in MFB configuration, which converts a fully-differential signal to a single-ended signal. Assuming a unity gain from node Y1 to node DC($R_3 = R_5 = R_4 = R_6$): the op-amp offset transfers to node DC with a gain of 2 = $1 + \frac{R_5}{R_3}$. The common-mode voltage at nodes Y1 and Y2 equals 2.5 V. If the resistors have 1% mismatches, the channels are expected to have a 2% channel mismatch in the worst case. This means that node DC can have a worst-case 50 mV offset, which is large enough to ruin the system's accuracy.

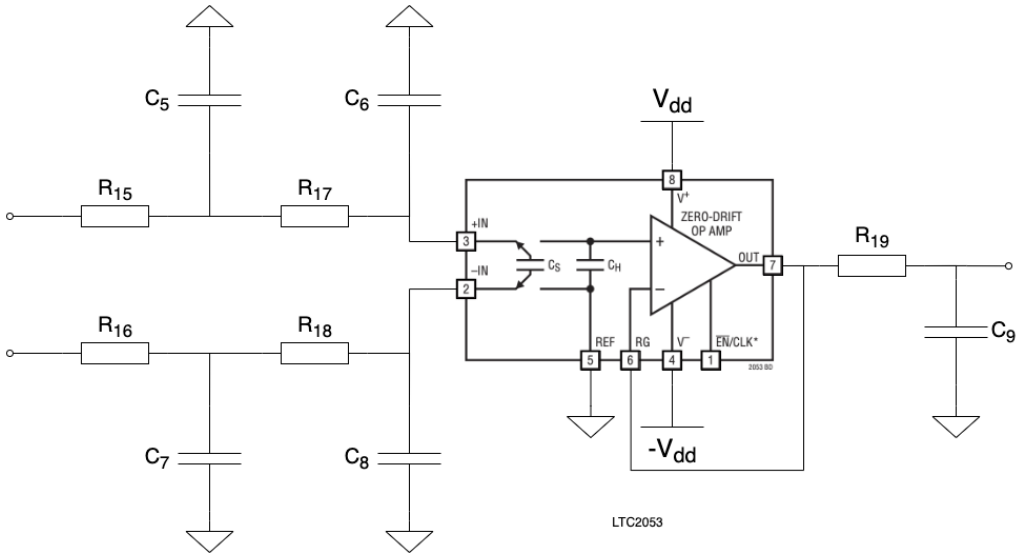

Figure 4-19 LPF with differential to single-ended conversion with LTC2053 [30]

Therefore, the system needs a structure with high CMRR and low offset, as in Figure 4-19. A simple RC LPF attenuates the high-frequency components, and an instrumentation amplifier affects the conversion from differential to single-ended. The criteria for selecting the instrumentation amplifiers are: dual power supply; state-of-the-art offset voltage; high CMRR. The gain accuracy is not crucial for this instrumentation amplifier because of the division operation afterward. The LTC2053 amplifier [30] has been selected for this application because of its excellent DC accuracy.

The LTC2053 uses charge-balanced sampled data techniques to convert the differential signal into a single-ended signal. Its input stage samples at a rate of 3 kHz [30]. The RC low-pass filter at the LTC2053 output limits the sampling artifacts at the input, as shown in Figure 4-19. The filter cuts off at 2 kHz because the sampling frequency is at 3 kHz. A Spice simulation was performed to examine the effect of including a filter at the output by applying a zero differential voltage at the input. Figure 4-20 shows the offset of the LTC2053 through the differences between differential input and output, which settles to around 17 µV (within the component's worst-case specification). The simulation (blue trace) shows many spikes when the instrumentation amplifier's output is not filtered. The simulation plot (red trace) hence shows that a simple RC LPF reduces sampling artifacts.

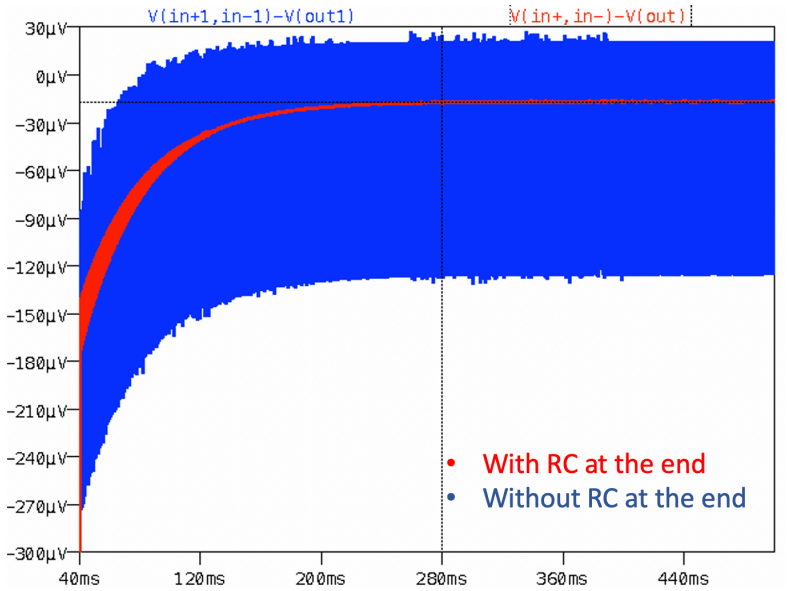

Figure 4-20 Simulation of LTC2053 offset with and without RC at the output

4.2.4 Digital to analog interface

The reason for having a separate digital circuit in the PCB is to reduce the influences of digital noise on the analog circuit. The digital section, therefore, has an isolated power supply and ground. A few single-bit digital isolators isolate the signal itself. There are several digital signals in the system: the SPWM signal, the square wave, and the control signal for the relay switch. The standard requirement for these isolators is to convert 3.3 V to 5 V.

The high-speed signals require a high-speed digital isolator to handle, for example, the demodulation square wave at 1 MHz. Manufacturers conventionally give the speed specifications of digital isolators in megabits per second (Mbps). So, to find the right digital isolators for the 1 MHz square wave, we need to convert the megabit rate into an equivalent oscillation frequency. A continuous signal (specified in hertz) changes state twice per period, so a 1 MHz square wave would present data at a rate of 2 Mbps [31]. Thus, the digital isolator needs to handle a throughput of at least 2 Mbps, if it is to avoid bandwidth limitations on a 1 MHz signal. Nowadays, digital isolators can achieve throughputs as high as 150 MBPS, which corresponds to an analog bandwidth of 75 MHz. The ISO721M isolator [32] has been selected for its high-speed (150 Mbps) character, in order to avoid additional attenuation of the high-speed signal. The SPWM can then have a pulse width in the hundred-megahertz range. The SPWM signal does not use the isolators. Instead, it is driven directly by an inverter because of the speed limit. The LPF limits the noise.

The other control signals are mainly for signal routing. The associated switching period is a few seconds; thus, these elements need not be capable of high-speed operation. Because relay switches are used, the digital isolator needs to have a high output current capability. Surface-mount relay switches G6J–Y [33] are used in the design, which require around 30 mA for switch operation [33]. The ADUM3221 isolator [34] chosen for controlling the relay switch signal, for its high output current capability (2 A per channel).

4.2.5 Noise analysis of AFE

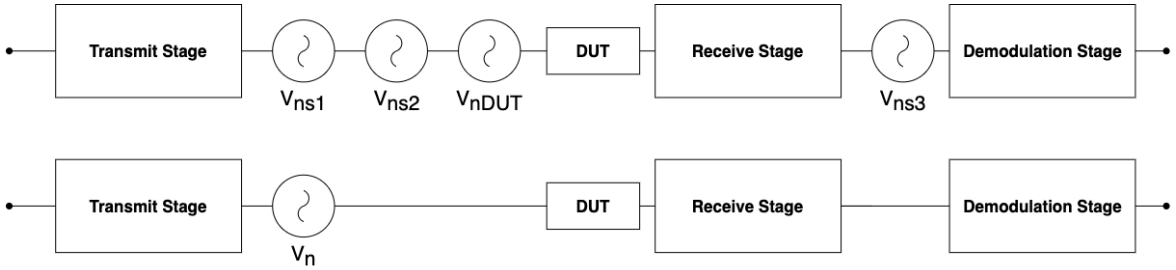

Figure 4-21 Block diagram of noise analysis

Signal-to-noise ratio (SNR) analysis was carried out for the readout system to estimate the noise in the system. As shown in Figure 4-21, the SNR is calculated at the output of the Transmit stage. Therefore, the noise of the Transmit stage refers to the output. The Receive and Demodulation stages, on the other hand, refers to the input. Eq. (18) shows the noise transfer gain for each stage to the equivalent noise source.

$$V_n = \sqrt{(V_{ns1}^2 + V_{ns2}^2 + V_{nDUT}^2 + \left(\frac{V_{ns3}}{gain \times \frac{R_f}{Z_{DUT}}}\right)^2)} \tag{18}$$

To analyze noise over the entire system, we begin by considering the worst SNR, which happens at the weakest signal level. This, in turn, occurs at the highest impedance level. Since the impedance level decreases as frequency increases, the worst-case SNR is when the frequency is 1 kHz.

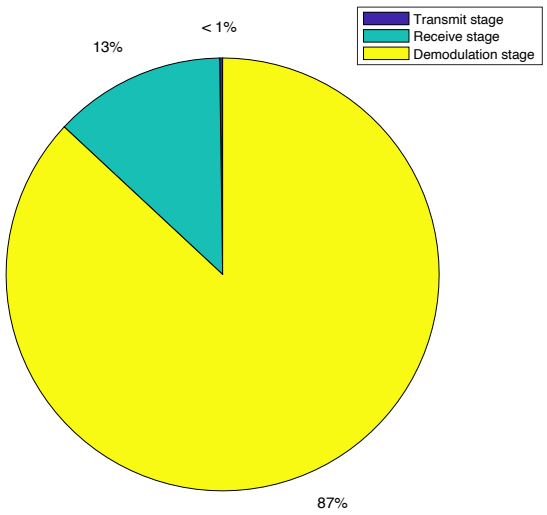

Figure 4-22 Noise distribution of analog circuit

Since the Demodulation stage effects a chopping operation, the calculation for the Transmit stage and Receive stage excludes all of the flicker noises up to that point. The estimation includes, however, flicker noise from the sources after the chopper. The calculated SNR is around 51 dB, which is beyond the 50 dB target. Figure 4-22 shows the noise distribution of the complete system. The Demodulation stage and the Receive stage are the most dominant sources because of the substantial attenuation gain presented by the sensor impedance and the TIA feedback network. Flicker noise and other DC artifacts in the Demodulation stage make this stage the most critical for noise performance. So, components before chopping could tolerably introduce a large flicker noise, as long as the 1/*f* corner is below the chopping frequency. However, we must pay attention to the DC performance when selecting components after chopping.

Chapter 5 Measurements and discussion

5.1 Measurement setup

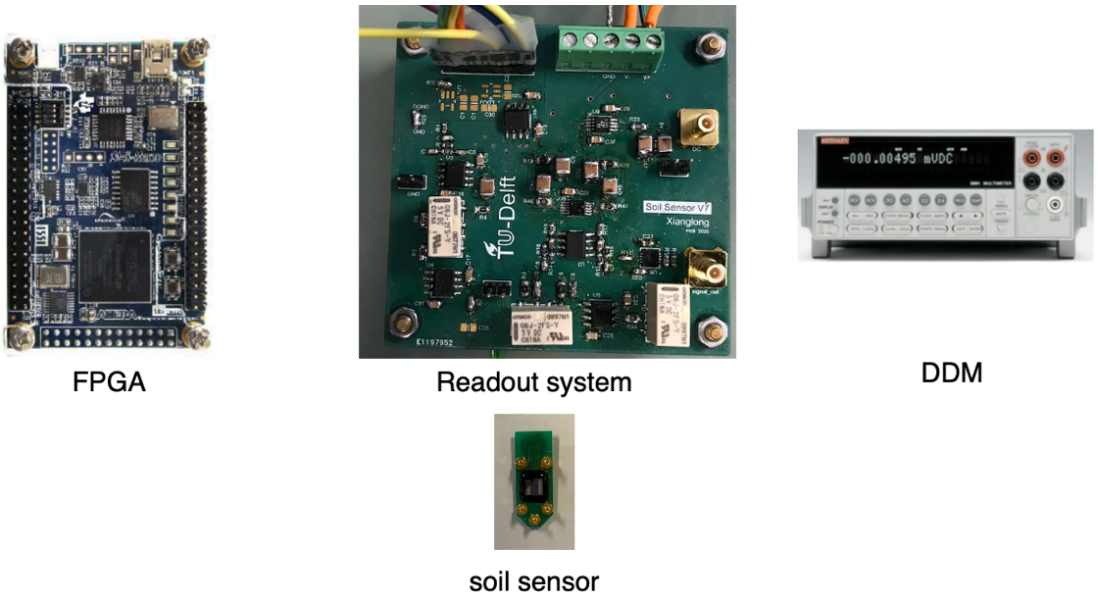

Figure 5-1 Measurement setup of the proposed readout system

Figure 5-1 shows the measurement setup. It comprises four parts, namely the FPGA development board [26], the PCB of the readout system, an impedance board (or the proposed sensor) [11], and a digital multimeter (DMM) [35].

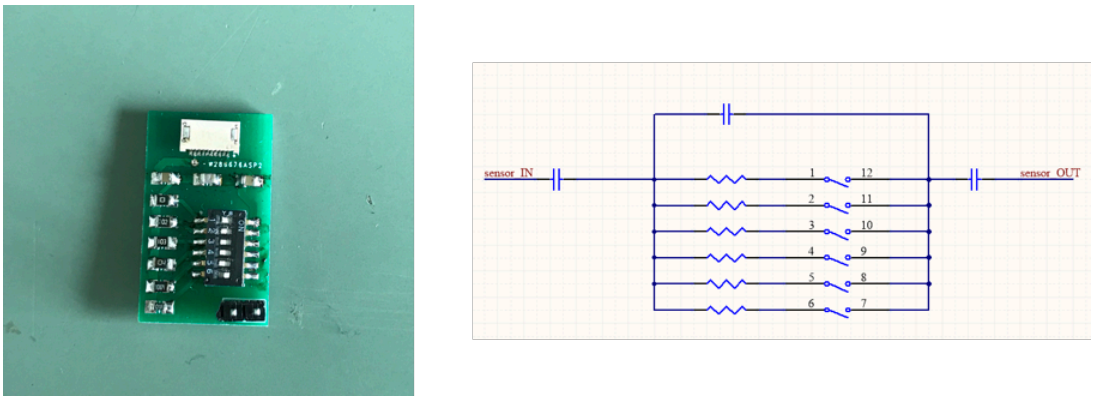

Figure 5-2 Schematic of impedance board

Figure 5-2 shows a schematic of the impedance board, which mimics the behavior of the proposed sensor. The impedance board can be represented by a capacitor in parallel with six different resistors, with the resistors independently selectable using the DIP switch block. One board has a capacitance of 470 pF; another has 10 pF. These two capacitances represent the capacitor corner in the impedance range. The resistances range from 100 Ω to 10 MΩ, stepping up by a factor of 10.

A DMM measures the DC voltage at the output node, and output values are stored for the impedance calculation. The reference value of the impedance board is measured by two LCR meters, namely, a Keysight impedance analyzer 4192A [36] and a GWInstek LCR meter LCR–6300 [37]. The 4192A [36] is responsible for measuring impedances under 1 MΩ from 1 kHz to 1 MHz, while the LCR–6300 [37] measures impedances higher than 1 MΩ, up to 300 kHz. The measurement error can be calculated by comparing the reference value with the measurement result. The measurements are taken in a grounded metal box to shield from the environment and other interference.

5.2 Measurement with impedance board

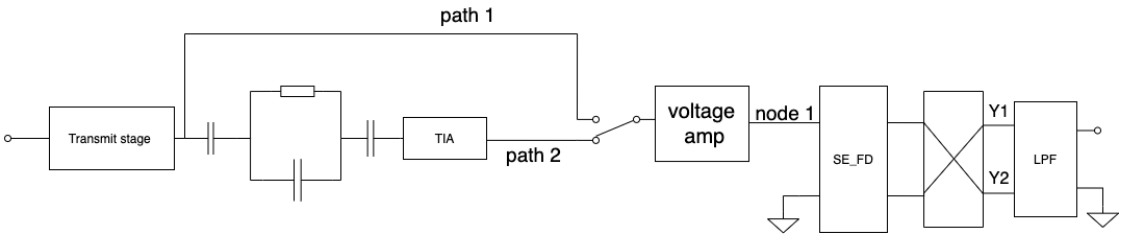

Figure 5-3 System block diagram

Figure 5-4 and Figure 5-5 show the voltage signal at node 1 in Figure 5-3, where the blue signal is when the switch connects to the Transmit stage, and the red signal is when the switch connects to the TIA. Neither figure presents any oscillations, which proves that the Transmit stage and Receive stage are stable and at the correct frequency.

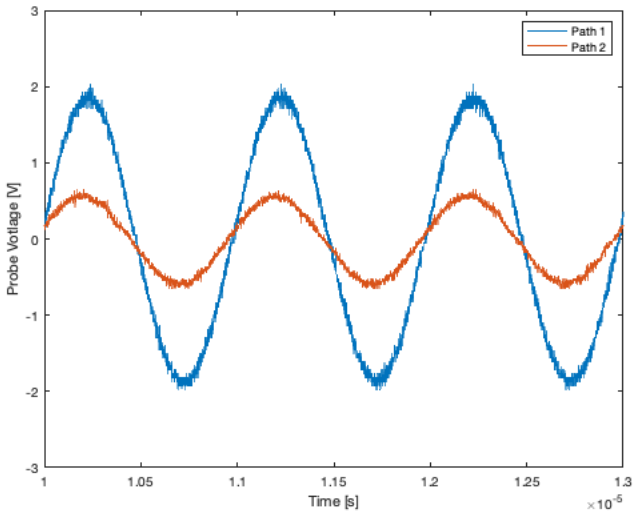

Figure 5-4 Signal at "node 1" at 1 MHz

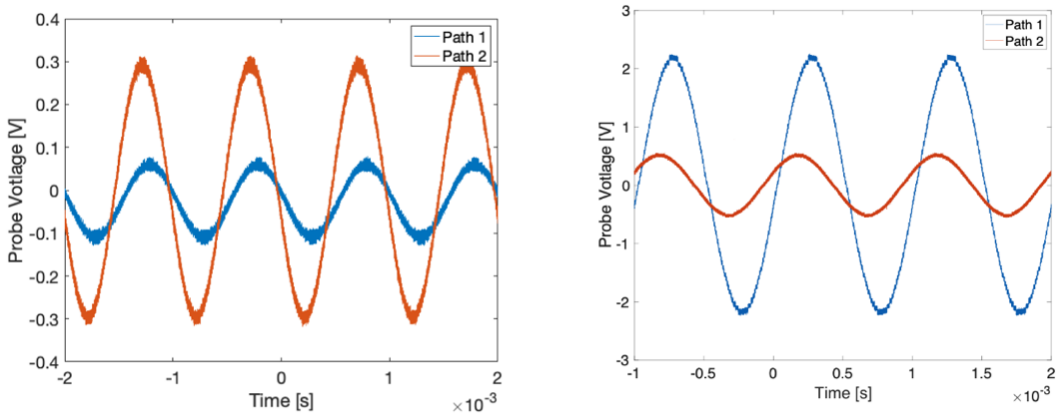

Figure 5-5 Signal at "node 1" at 1 kHz

Figure 5-5 shows activity in the low and high excitation ranges at 1 kHz. At node 1, the low-excitation amplitude is 170 mV_{pp}, and the high-excitation amplitude is 4.33V_{pp}. This means that the excitation amplitude for the sensor is around 20 mV_{pp} and 500 mV_{pp} because the voltage amplifier (Figure 5-3) has a gain of 8.6.

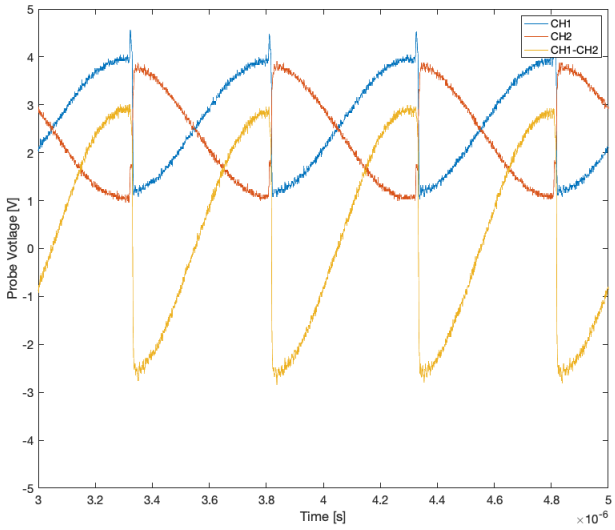

Figure 5-6 Signal probed at Y1 and Y2, at 1 MHz

Figure 5-6 shows the signal probed at Y1 and Y2 (Figure 5-3). CH1 and CH2 both show voltage spikes at each chopping time. This is a capacitive load charging phenomenon. The sizeable capacitive load here comes from the PCB traces or the oscillator scope probe. Fortunately, these voltage spikes are mostly common-mode signals. The differential signal (CH1–CH2) does not show as severe voltage spikes as the single-ended measurements.

During the measurement, one interesting finding concerns the influences of different ceramic capacitor insulator types. There are plenty of different capacitor dielectric materials available on the market; the common ones are the NP0, X7R, and X5R dielectrics. Non-linear capacitor response to voltage is well-known and is characterized by some manufactures, but using the wrong type of capacitors could prolong the settling behavior.

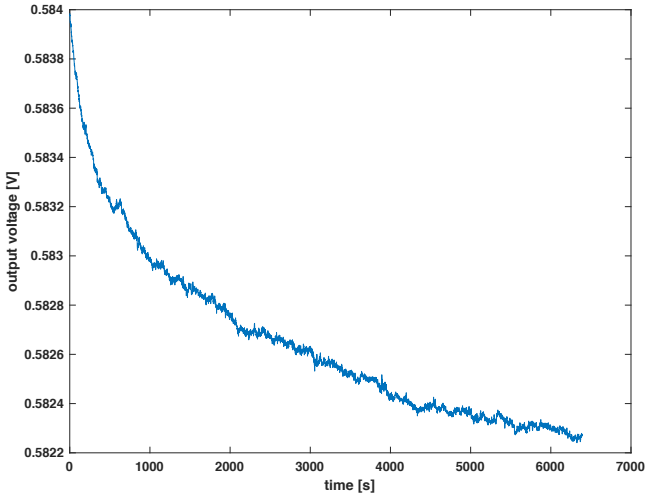

Figure 5-7 Slow settling behavior of the readout system

The system exhibits a slow settling phenomenon when reading the DMM values at the output of the PCB. Figure 5-7 shows that this integrator-like behavior lasts for several hours. Debugging the issue revealed that the X7R-based capacitor causes this slow behavior.

A straightforward experiment was performed to verify that an inappropriate capacitor can cause integrator-like behavior. As shown in Figure 5-8, the experiment compares two simple RC networks with the same time constant. One of them uses a NP0-based capacitor while the other uses a X7R-based capacitor. A voltage reference IC provides a constant DC voltage at the input node.

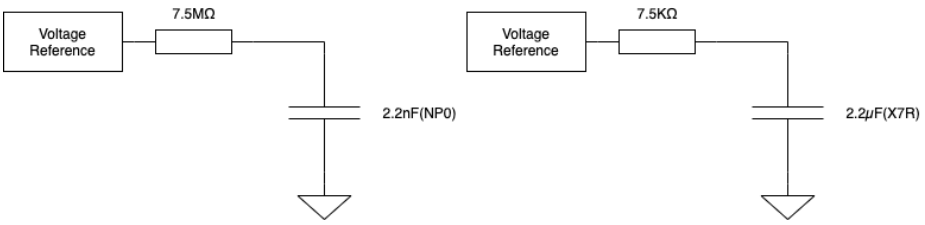

Figure 5-8 Capacitor experiment testbench

Figure 5-9 shows the settling of both setups. After around 2.7 hours, the settling behavior differs a great deal between them. The circuit with the NP0 capacitor settles much faster than the circuit with the X7R capacitor. Therefore, even though smaller footprints are not always available for NP0 type capacitors, using NP0 capacitors in the critical signal chain is recommended to prevent undesirable behaviors like noisiness, poor voltage dependency, and slow settling. As for the decoupling capacitors, these do not require fast settling. X7R-based capacitors would be suitable because of their low price and small footprint.

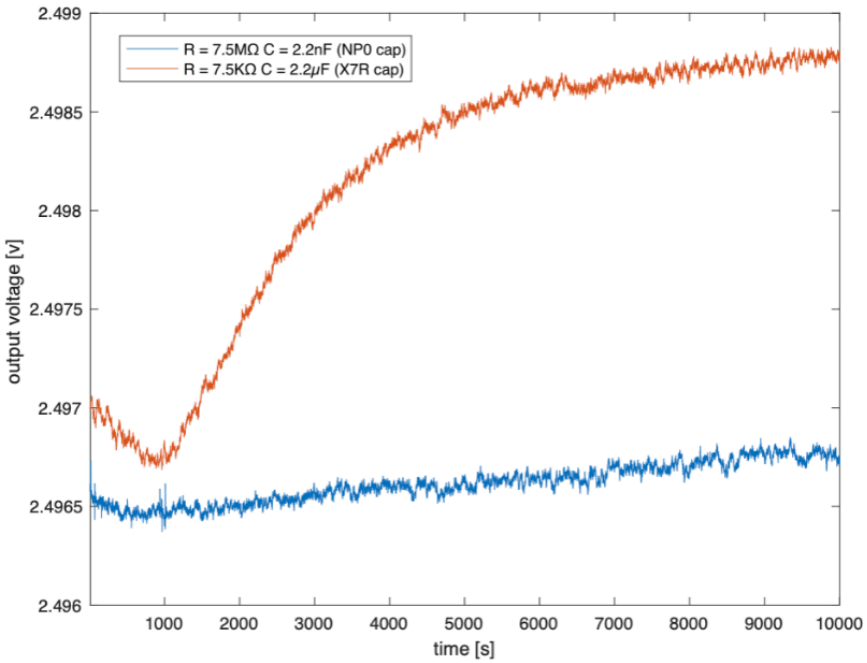

Figure 5-9 Capacitor insulator type experiment

Finally, Figure 5-10 presents the measurement error of the proposed readout system and suggests that the measurement error on the tested points is below 1%. The accuracy at 1 MHz is worse than at 1 kHz, which could be due to the TIA input impedance at the lower impedance level and chopping artifacts at the higher impedance level. At higher frequencies, the system shows more error than the expectation, which is caused by the chopping artifact shows up at a higher rate. The PCB demodulators need to deal with a relatively large parasitic capacitance. So, implementing the system at an IC level would reduce this error.

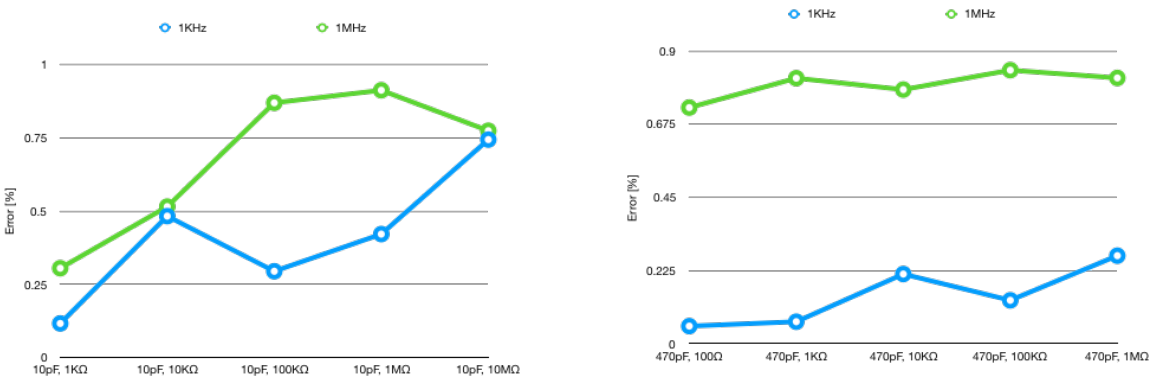

Figure 5-10 Accuracy of the proposed readout system

5.3 Measurement with the soil sensor chip

The readout system has been used with the sensor chip to verify its function. Due to the limitation of the laboratory equipment, the measurement shows only that the readout system can respond to different water-content conditions. The accuracy test with the sensor chip needs to be done at another laboratory in Japan.

Figure 5-11 Reference measurement with LCR meter [37]

A small PCB that interfaces with an LCR meter and the sensor was made to give a rough impedance reference for the sensor. Figure 5-11 shows the reference measurement in progress. The sensor chip is placed in the air, in water, and in salty water. The absolute impedance at each test is shown in Figure 5-12 by red circles; the impedance reading of the proposed system is shown by blue crosses. The measurement shows that the readout system could work with the sensor chip as

expected. However, the soil water content and ion concentration could not be well controlled with available laboratory amenities, so the accuracy test should be carried out in another laboratory.

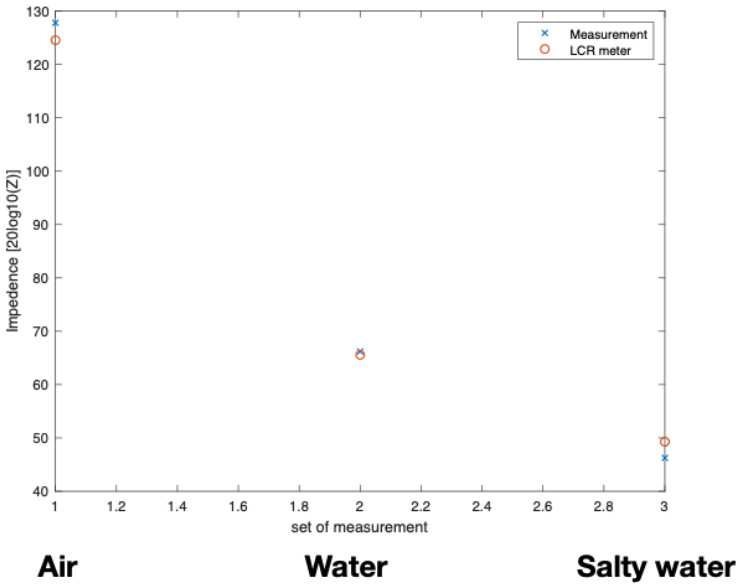

Figure 5-12 Measurement with the sensor chip

To conclude the measurement section: the proposed readout system successfully interfaced with the low-leakage soil sensor to give meaningful results. The readout system could achieve accuracy with less than 1% error when measuring the impedance board over the impedance and frequency corners. Moreover, for future studies, the actual accuracy of soil water content with the readout system needs to be measured.

Chapter 6 Conclusion

In summary, a low-leakage soil water-content sensor is proposed for the detection of rain-fall induced slope failure in 2017, which is based on the measurement of soil impedance [11]. So, the readout needs to measure the complex impedance network accurately (1%). Because of the low leakage current property, the readout system should measure over a broad frequency and impedance range from 1 kHz to 1 MHz and from 100 Ω to 8.6 MΩ, respectively. However, no commercial products cover this entire range.

In the thesis, a benchmark system is designed based on AD5933, a widely used integrated impedance analyzer. Its purpose is to benchmark the proposed readout system. The measurement shows that the performance of AD5933 is limited by the excitation frequency (up to 100K Hz) and also suffers from spectral leakage. By selecting a specific frequency free of spectral leakage, AD5933 produces the worst-case error of around 3%. This exceeds the target accuracy.

Therefore, an SPWM excitation-based readout system is proposed in this thesis. The system uses analog synchronous detection to measure an AC signal while achieving an excellent SNR. In the architecture study, a detailed analysis of demodulation using more than two quantization levels signal is performed. The counterintuitive finding is that the demodulation error from using a square wave is less than that from using a signal with more quantization levels because some signal harmonics are phase-shifted. Therefore, the SPWM excitation-based readout system demodulates with a synchronized square wave.

The proposed readout system is implemented at the PCB level. The measurement shows that the system achieves the target error below 1%. This performance not only exceeds the benchmark system but also extends the frequency from 100 kHz to 1 MHz.

Future studies can conduct accuracy tests with soil samples, as this has not been completed in the current study because of limited lab equipment. Aside from this, the system performance could be improved in several ways. First, the system could use the second demodulation stage, as shown in Figure 6-1. In this way, the excitation

voltage and the sensor current could be measured simultaneously. As a result, the measurement period is reduced by half.

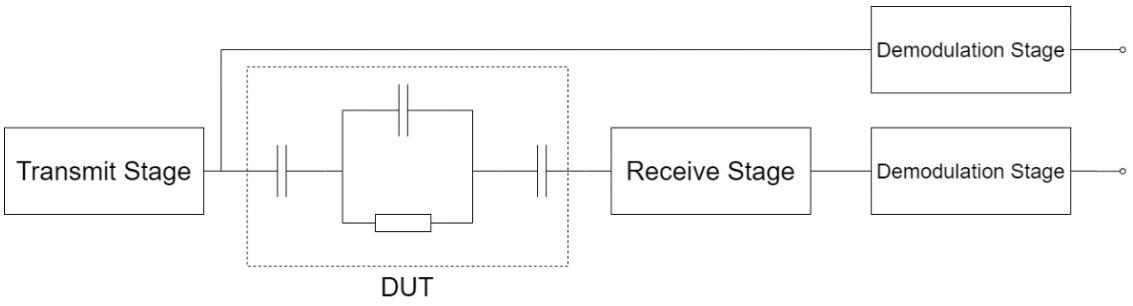

Figure 6-1 Potential improvement of the readout system

Second, the system could reduce harmonic error by improving the linearity of the digital SPWM. The options are using pre-compensation and using feedback. Similar studies have been conducted in [22] [38].

Moreover, a compact system could be achieved by adding an onboard digital processing unit so that the data processing could be performed onboard. The system needs an ADC at the end of the signal chain to digitize the signal. Then, the measurement values are saved in a memory block. A digital signal processing unit would perform the impedance calculation.

Finally, implementing the entire system at the IC level would reduce demodulation errors at 1MHz because the choppers need not deal with large parasitic capacitors, such as those in the PCB, and there is better matching between the channels.

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