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A Four-Way Series Doherty Digital Polar Transmitter at mm-Wave Frequencies

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***Abstract*— This article presents an efficient digital polar transmitter (DPTX) at mm-wave frequencies that exploit a novel N-way series Doherty combiner (SDC) to enhance its drain and system efficiency at deep power back-off (PBO). The proposed N-way SDC is scalable and can be implemented elegantly using N transformers and $N-1$ shunt capacitors. As a proof of concept, a four-way Doherty DPTX is realized with the proposed SDC in which four identical but independent digital phase modulators deliver a phase-modulated constant envelope signal to their corresponding digital power amplifiers to perform the required amplitude modulation. Fabricated in a 40 nm CMOS process, the proposed DPTX occupies a core area of 1.1 mm^2 and exhibits 18.7 dBm saturated output power and <-40 dBc LO feedthrough. It demonstrates a drain efficiency of 33%/36%/22% at 0/4.5/11.5 dB PBO at a 29.5 GHz carrier frequency. While transmitting a 300 MHz 64-QAM OFDM signal with a peak-to-average power ratio of 10.7 dB, the DPTX achieves 18%/8% average drain/system efficiency, -27.6 dB error vector magnitude, and -27.5 dBc adjacent channel leakage ratio. To the best of our knowledge, this work is the first reported mm-wave Doherty transmitter that includes the entire chain all the way from the binary data stream up to the modulated mm-wave output signal.**

***Index Terms*— Digital phase modulator (DPM), digital polar transmitter (DPTX), digital power amplifier (DPA), Doherty design guide, millimeter-wave transmitter (TX), power amplifier (PA), series Doherty combiner (SDC).**

I. Introduction

MASSIVE multi-input–multi-output (mMIMO) architectures and high-order modulation schemes with large peak-to-average power ratios (PAPRs) are widely used in fifth-generation (5G) mm-wave communication to improve the system's data rate and spectral efficiency [1]–[4]. This imposes several challenges on the transmitter (TX) design.

First, to accommodate the signal's PAPR, the power amplifier (PA) must operate in deep power back-off (PBO), which subsequently results in a dramatic degradation of both PA and TX average efficiencies. Hence, envelope tracking [5]–[8] and outphasing [9]–[14] techniques are employed in the literature to address this issue. However, the former's performance is limited by the envelope modulator's bandwidth (BW) and efficiency, while the latter requires complex signal processing blocks, thus reducing the system efficiency. A more wideband efficiency enhancement technique is the Doherty concept [15]–[31] for which the PA load is dynamically modulated to improve the PBO efficiency. However, the number of the peaking amplifiers in prior-art mm-wave Doherty PAs has been limited to two mainly due to poor scalability and high losses in the Doherty power combiner [21]. Therefore, either the efficiency enhancement was restricted to less than a 10 dB PBO range or a deep valley on the efficiency curve is observed [30].

The second challenge lies in the extensive power consumption of the baseband and mm-wave circuitries that are needed to drive the PA. Since the 5G standard restricts the maximum effective isotropic radiated power (EIRP), the output power of each TX reduces linearly as the number of antennas increases. However, in a conventional analog TX, the power consumption of the digital-to-analog converters (DACs), baseband filters, and upconverting mixers will not reduce proportionally to the output power, as the matching between the DAC's cells, noise, and linearity of the baseband filters and mixers will put a hard limit on the minimum current consumption of these blocks. Consequently, the system efficiency of conventional analog TXs generally degrades at lower output powers. A more promising approach is to employ digital TXs (DTXs) [32]–[41], in which the baseband DAC, mixer, and PA are all realized in the last stage. Consequently, the dc power of most of the TX blocks is scaled proportionally to the output power, thus realizing a class-B type back-off efficiency curve for the entire TX. For example, Qian *et al.* [36] demonstrated a mm-wave Cartesian DTX, achieving ~6% system efficiency at PBO = 10 dB. However, this structure suffers from an undesired interaction between in-phase (I) and quadrature (Q) DACs, degrading the TX linearity and requiring a sophisticated 2-D digital predistortion (DPD). On the other hand, [37]–[41] employs a digital polar architecture to achieve higher output power and efficiency. However, the resolution of their digital PA (DPA) used for amplitude modulation (AM) is insufficient to support high-order modulation schemes (i.e., 256 QAM). In addition, the low image rejection ratio (IRR) of their digital phase modulator (DPM) degrades the error

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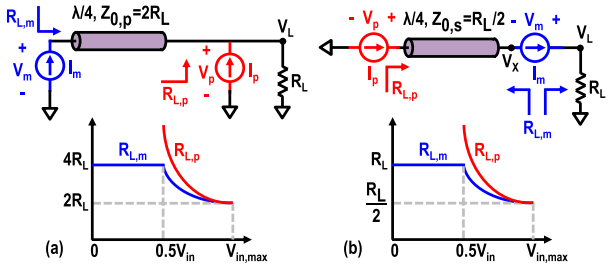


Fig. 1. Conceptual schematic and corresponding impedances of the main/peaking PAs for (a) parallel and (b) series Doherty structures.

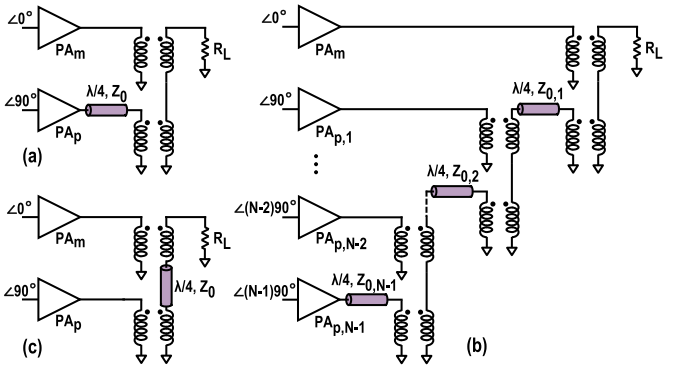


Fig. 2. Schematic of (a) conventional two-way SDC, (b) N-way SDC proposed by [21], and (c) modified schematic of the conventional two-way SDC.

vector magnitude (EVM). Besides the linearity issues, their average system efficiency is below 5% since they did not use any efficiency enhancement technique.

To improve on those limitations, this article reports a four-way series Doherty digital polar TX (DPTX) based on the following techniques [42]. First, a scalable N-way series Doherty combiner (SDC) is proposed to enhance system efficiency at deep PBOs. Second, a high-resolution DPA is exploited to perform the AM, while its output resistance roughly tracks the load impedance imposed by the Doherty structure, thus maintaining the output matching condition at deep PBOs. Third, the I and Q cells in the DPM are interleaved in the layout to minimize the gain and phase mismatch between I and Q banks, thus improving the DPM's phase resolution and IRR. This article is organized as follows. Section II presents the evolution of the proposed N-way SDC structure and its design flow. The detailed DTX architecture and circuit design are provided in Section III. Section IV presents extensive measurement results of the prototype, while Section V recapitulates this article with conclusions.

II. Evolution of N-Way Series Doherty Combiner

A conventional two-way parallel or series Doherty PA is composed of a main PA (PA_m), a peaking PA (PA_p), and a $\lambda/4$ transmission line (TL) acting as an impedance inverter, as shown in Fig. 1. In both Doherty flavors, when PA_p is entirely OFF, PA_m sees $2\times$ larger impedance than that of at full power, resulting in early saturation of PA_m and realizing an efficiency peak at PBO = 6 dB. At PBO $\leq$ 6 dB, PA_m load resistance ($R_{L,m}$) decreases due to the PA_p activity. Consequently, PA_m delivers more power to the load (R_L) while staying in saturation and operating at its maximum efficiency [15], [23], [28].

A. Parallel or Series Doherty Combiner?

In a traditional parallel Doherty combiner (PDC), as shown in Fig. 1(a), the TL converts PA_m output current (I_m) into an output voltage of $V_L = Z_{0,p} \times I_m$, where $Z_{0,p} = 2R_L$. As a result, the load resistance of PA_p and PA_m can then be estimated by $2R_L \times (I_m/I_p)$ and $2R_L \times (2-(I_m/I_p))$, respectively. Due to the parallel nature of this structure, both PAs always see a load resistance larger than R_L, thus limiting the maximum deliverable power to the load ($P_{L,\max}$). Moreover, since PA_p is directly connected to the load, $P_{L,\max}$ will be limited by PA_p's maximum voltage swing determined by the time-dependent dielectric breakdown (TDDB) and hot carrier injection (HCI) reliability issues. Hence, an extra matching network (MN) is required between R_L and PA_p to scale down the load resistance of Doherty PAs and enhance $P_{L,\max}$. However, this comes with a penalty on the system efficiency due to the excessive loss of the extra MN as a large impedance transfer ratio is often required.

A more promising approach is to use the SDC in which PA_m, PA_p, $\lambda/4$ TL, and R_L, are in series, as shown in Fig. 1(b). In this structure, the TL converts the PA_p output current (I_p) into an intermediate voltage of $V_X = Z_{0,s} \times I_p$, where $Z_{0,s} = 0.5R_L$, while the output voltage is merely proportional to the PA_m output current, $V_L = R_L \times I_m$. Compared to PDC, the load resistance of Doherty PAs reduces by $4\times$, thus facilitating the design of the PAs in the current domain. Moreover, in contrast to PDC, the maximum output voltage swing is equally divided between the main and peaking amplifiers, enhancing $P_{L,\max}$ by 6 dB without inserting any extra MN or sacrificing the PAs' long-term reliability.

It is also essential to compare the PDC and SDC BW. Since $P_{L,\max}$ is 6 dB higher in SDC PAs for the same R_L and supply voltage, the output current and, thus, parasitic capacitance ($C_{\text{out},m}$) of its PA_m should also be $4\times$ larger compared with its PDC counterpart. Consequently, the effective quality factors ($Q_L = C_{\text{out},m} R_{L,m} \omega_0$) of the PA_m's load in SDC and PDC are the same. Thus, both structures should offer identical operational BW from this perspective. Nonetheless, as the TL connects the load to PA_m in the PDC structure, $R_{L,m}$ becomes frequency-dependent, significantly degrading its BW, especially at PBOs, as shown in [43]. However, the PA_m current directly flows to the load in the SDC structure, thus realizing an output power of $0.5R_L I_m^2$ irrespective of frequency, widening operational BW. Consequently, an SDC structure is chosen in this work due to its larger BW and $P_{L,\max}$.

B. Toward a Scalable SDC

Fig. 2(a) illustrates a practical implementation of a conventional two-way SDC for which the voltage summation is realized by the series connection of the secondary winding

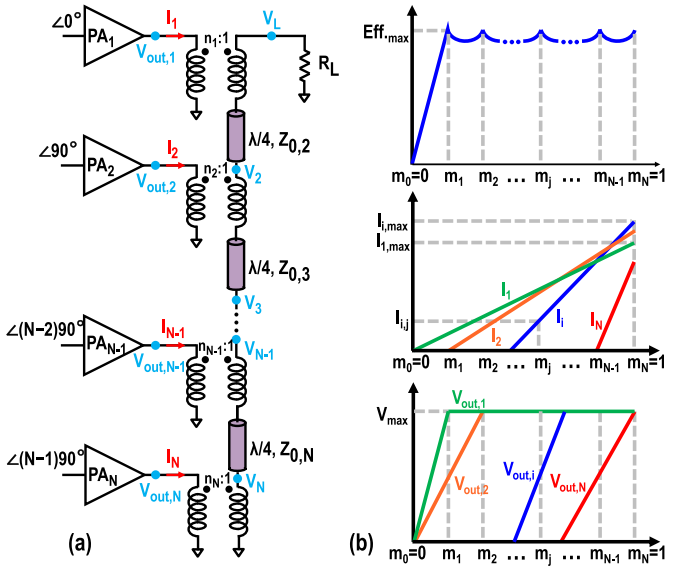


Fig. 3. (a) Proposed N-way SDC and (b) ideal efficiency, current, and voltage curves for arbitrary PBO points.

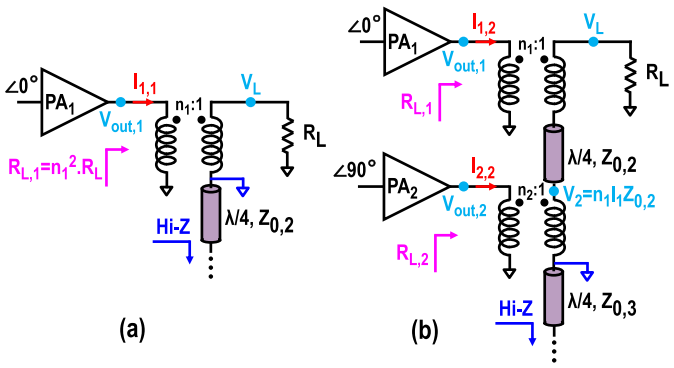


Fig. 4. Simplified SDC schematic at (a) first and (b) second PBOs.

of the PA$_m$ and PA$_p$ transformers. The most straightforward way to extend the structure to a three-way combiner is to replace its peaking amplifier with a conventional two-way SDC, as shown in Fig. 2(b) and proposed in [21]. However, this approach is not scalable and imposes several constraints. First, the number of transformers increases by a factor of two with Doherty order, i.e., $2(N-1)$ transformers for N-way SDC, thus dramatically increasing the SDC footprint and loss. Second, compared to the main PA, there are much more passive components (i.e., transformers and TLs) between the last peaking amplifier and the load. Hence, distributing the input signal uniformly between different PAs and realizing a symmetric layout would be highly challenging.

To address the abovementioned issues, the TL of the peaking amplifier in the conventional two-way SDC is first moved from the transformer's primary winding to its secondary coil, as shown in Fig. 2(c). The operation and voltage/current waveforms of the modified two-way SDC remain the same as the original circuit. However, it can be easily extended to an N-way SDC by cascoding $(N-1)$ peaking amplifier blocks, as illustrated in Fig. 3. The proposed N-way SDC can be compact and low loss as it only requires N transformers. Moreover, the physical distances between the PAs and the load can easily be made similar, which significantly simplifies the PA layout and LO distribution.

C. Design Guide

In this section, we will develop a general design guide for determining the TLs characteristic impedance ($Z_{0,i}$), transformers' turn ratio (n_i), and the PAs maximum current ($I_{i,\max}$) based on some high-level specifications, such as the maximum load power ($P_{L,\max}$), supply voltage ($V_{\rm DD}$), Doherty order (N), and the normalized input points ($m_j = V_{{\rm in},j}/V_{{\rm in},\max}$) in which the Doherty amplifier reaches its peak efficiency. For the sake of simplicity, we assume that all transformers and TLs are lossless in the following equations. Nevertheless, the analysis outcome will be sufficiently accurate to show the design tradeoffs and be used as the first design step.

At the first PBO point (i.e., m_1), all peaking amplifiers (PA$_{2,\ldots,N}$) are OFF and exhibit a high output impedance. Consequently, as shown in the simplified circuit in Fig. 4(a), the bottom terminal of the secondary winding of the topmost transformer can be shorted to the ground due to the impedance inversion of $\lambda/4$ TLs. At this point, the main amplifier (PA$_1$) reaches its maximum output voltage, $V_{\rm out,max} = \alpha \times V_{\rm DD}$, which is determined by considering the tradeoff between the amplifier's efficiency and linearity. Hence, PA$_1$ delivers $0.5\alpha V_{\rm DD} I_{1,1}$ to the load, which must match $m_1^2 \times P_{L,\max}$ to satisfy the Doherty operation. Therefore,

$$I_{1,1} = \frac{2m_1^2 P_{L,\max}}{\alpha V_{\rm DD}} \tag{1}$$

where $I_{1,1}$ is the PA$_1$ current at the first PBO, and generally, $I_{i,j}$ is defined as the current of the ith PA at the jth efficiency peak. By considering the linear relation between the PA$_1$ current and input voltage [see Fig. 3(b)], we have

$$I_{1,\max} = \frac{2m_1 P_{L,\max}}{\alpha V_{\rm DD}}. \tag{2}$$

Interestingly, the main amplifier must deliver more current if the semiflat region in the efficiency curve is shrunk. Similar to $I_{1,1}$ calculations, the transformer's turn ratio may be estimated as

$$\frac{1}{2} R_L I_{1,1}^2 \times n_1^2 = m_1^2 P_{L,\max} \rightarrow n_1 = \frac{m_1}{I_{1,1}} \sqrt{\frac{2P_{L,\max}}{R_L}}. \tag{3}$$

By replacing (1) in (3), n_1 expression is simplified to

$$n_1 = \frac{\alpha V_{\rm DD}}{m_1 \sqrt{2R_L \times P_{L,\max}}} \xrightarrow{\beta := \frac{P_{L,\max}}{(\alpha V_{\rm DD})^2/2R_L}} n_1 = \frac{1}{m_1 \times \sqrt{\beta}} \tag{4}$$

where β is the power enhancement factor, defined as the ratio of $P_{L,\max}$ to the maximum power that a single PA can deliver to R_L without having any impedance scaling MN. As expected, to achieve a higher $P_{L,\max}$ (i.e., larger β), (4) suggests reducing n_1 to scale down the load resistance of the main amplifier. However, similar to any PA, if a large $P_{L,\max}$ is targeted, the impedance transfer ratio (i.e., n_1 value) will be impractically small.

At the second PBO (m_2), PA_1 and PA_2 have reached their maximum output voltage [see Fig. 3(b)] and have to deliver $m_2^2 \times P_{L,\max}$ to the load. As a result,

$$m_2^2 \times P_{L,\max} = \frac{1}{2}\alpha V_{DD} I_{1,2} + \frac{1}{2}\alpha V_{DD} I_{2,2} = \frac{1}{2}\alpha V_{DD}\left(m_2 I_{1,\max} + \frac{m_2 - m_1}{1 - m_1} I_{2,\max}\right). \quad (5)$$

By replacing (2) in (5), the maximum current of the second PA is calculated as

$$I_{2,\max} = 2m_2(1 - m_1) \times \frac{P_{L,\max}}{\alpha V_{DD}}. \quad (6)$$

Since the other PAs are OFF, due to the impedance inversion of $\lambda/4$ TLs, the bottom terminal of the second transformer can be shorted to the ground, as shown in Fig. 4(b). Now, the voltage across the secondary coil of the second transformer can be calculated in two ways. On the one side, it is fixed by PA_2 output voltage and the turn ratio of the second transformer (n_2). On the other side, it is determined by the TL characteristic impedance ($Z_{0,2}$) and the load current imposed by the main amplifier. Consequently,

$$\frac{\alpha V_{DD}}{n_2} = n_1 m_2 I_{1,\max} Z_{0,2} \rightarrow n_2 = \frac{\alpha V_{DD}}{n_1 m_2 I_{1,\max}}. \quad (7)$$

By replacing (2) and (4) in (7), we have

$$n_2 = \frac{1}{m_2\sqrt{\beta}} \times \frac{R_L}{Z_{0,2}}. \quad (8)$$

Note that $Z_{0,2}$ offers a degree of freedom to designers to bring n_2 to the values that can be efficiently implemented on-chip. The same procedure and analysis can be employed at the remaining PBO points to reach generalized closed-form equations for all components in the proposed N-way SDC PA. For example, the maximum current of the ith PA may be estimated by

$$I_{i,\max} = 2(m_i - m_{i-2})(1 - m_{i-1}) \times \frac{P_{L,\max}}{\alpha V_{DD}}. \quad (9)$$

As expected, the current of all PAs linearly increases if either a larger $P_{L,\max}$ or a lower V_{DD} is required. Accordingly, the output power of PA_i at the jth efficiency peak (m_j) is calculated by

$$P_{\text{out},i,j}|_{j \geq i-1} = (m_j - m_{i-1})(m_i - m_{i-2}) P_{L,\max}. \quad (10)$$

Moreover, the load resistance of the PAs as a function of $m = (V_{in}/V_{in,\max})$ can be assessed by

$$R_{L,i} = \frac{R_L}{(m_i - m_{i-2})(m - m_{i-1})\beta}, \quad \text{for } m \geq m_{j=i}. \quad (11)$$

As anticipated, $R_{L,i}$ must be scaled down more aggressively if a higher $P_{L,\max}$ (i.e., larger β) is demanded. Furthermore, $(m - m_{i-1})$ in the denominator of (11) indicates that $R_{L,i}$ increases dramatically when the corresponding PA operates at its deep PBO, thus resembling the ideal SDC behavior. Finally, after lengthy algebra, the turn ratio of the transformers may be estimated as

$$n_i = \frac{1}{(m_i - m_{i-2})\sqrt{\beta}} \times \frac{\prod_{k=0}^{\left[\frac{i-1}{2}\right]} Z_{0,i-2k-1}}{\prod_{k=0}^{\left[\frac{i-1}{2}\right]} Z_{0,i-2k}} \quad (12)$$

where $Z_{0,0} = Z_{0,1} = R_L$, $m_0 = m_{-1} = 0$, and $[(i-1)/2]$ is defined to be the greatest integer that is less than or equal to $((i-1)/2)$. Note that β is typically much greater than 1 to obtain a larger $P_{L,\max}$, while $(m_i - m_{i-2})$ is considerably smaller than 1 to achieve a flat efficiency curve at deep PBO. As a result, n_i will be close to 1 as $\sqrt{\beta}$ and $(m_i - m_{i-2})$ in (12) cancel each other out in the first-order approximation, facilitating the on-chip implementation of the transformers. Furthermore, as suggested in (12), n_i and $Z_{0,i}$ should be optimized together to achieve practical values for both of them.

As can be concluded from (9) to (12), the placement of efficiency-peaking points significantly affects the design parameters. Fig. 5 illustrates its impact on the normalized $I_{i,\max}$, n_i, $Z_{0,i}$, and efficiency for a four-way SDC. As can be gathered from the red curves in Fig. 5, distributing the PBO points ($m_j = (1/N) \times (j \times (N+1) - N)^{1/2}$) uniformly over input power (P_{in}) is not wise since it leads to the deepest valley in the efficiency curve and the largest variation among the maximum current of the peaking PAs (i.e., $I_{2,\max}/I_{4,\max} \approx 7$). On the other hand, by spreading PBO points ($m_j = \sqrt[N-1]{N^{(j-N)}}$) evenly over $10 \times \log_{10}(P_{in})$, the flattest efficiency curve can be achieved; however, each transformer in the peaking PAs needs a different turn ratio, complicating the layout. Another option is to place PBO points such that all PAs deliver the same maximum current and, thus, have the same size, therefore significantly simplifying the PA design (see the black curves). However, the complexity is again pushed to the SDC design as its transformers still require different turn ratios. Finally, the PBO points can be placed uniformly across the input voltage (i.e., $m_j = j/N$). This considerably simplifies the SDC design compared to other methods as the transformers' turn ratio and characteristic impedance of TLs are almost the same for all peaking amplifiers [see Fig. 5(c) and (d)]. However, as plotted in Fig. 5(b), the first peaking amplifier must deliver 3× more current than the last one, thus demanding multiple PA designs.

D. SDC Prototype

By evaluating the benefits and drawbacks of the PBO distribution methods, considering the layout constraints at mm-wave frequencies, and assessing the practical range of TL characteristic impedance in CMOS technology, a four-way SDC based on the uniform PBO distribution across V_{in} is implemented in this work. To estimate the transformers' inductances ($L_{p,i}$ and $L_{s,i}$) and coupling factor ($k_{m,i}$), a rough estimation of the PA's output capacitance is needed. Since the maximum current of each PA and transistor's current driving capability are already known, the PA size and, consequently, its capacitance can be determined. At the operating angular frequency (ω_0), the transformer's primary inductance should resonate with the output capacitance of the corresponding PA ($C_{o,i}$). Therefore,

$$L_{p,i} = \frac{1}{C_{o,i}\omega_0^2} \quad \& \quad L_{s,i} = \frac{L_{p,i}}{n_i^2}. \quad (13)$$

The next challenge lies in the realization of bulky $\lambda/4$ TL on the chip. To save area and reduce SDC loss, as illustrated

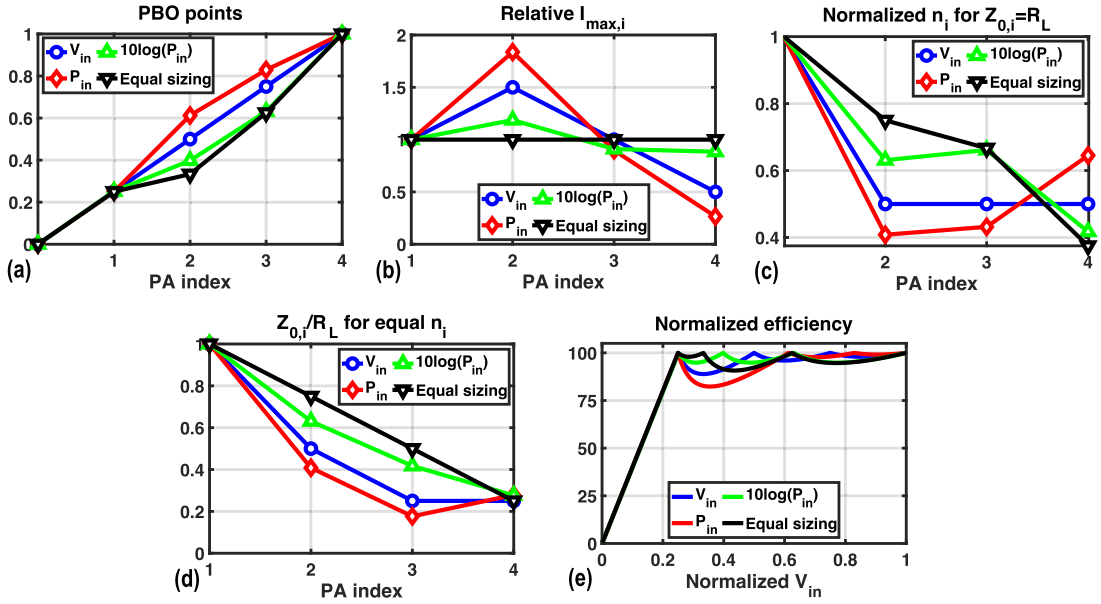


Fig. 5. (a) Efficiency-peaking points, (b) relative maximum current of the PAs, (c) relative n_i when $Z_{0,i} = R_L$, (d) $Z_{0,i}/R_L$ when $n_i = 1$, and (e) normalized efficiency curves for the proposed four-way SDC, while the efficiency peaking points are distributed uniformly across V_{in}, P_{in}, and $10\log_{10}(P_{\text{in}})$ or they spread such that the current and size of all PAs are the same.

in Fig. 6(a), each $\lambda/4$ TL is first replaced with its equivalent T-network model comprising two series inductors (L_i) and a shunt capacitor (C_i) that are estimated by $Z_{0,i}/(\omega_0)$ and $1/(Z_{0,i}\omega_0)$. The resulting series inductances (i.e., L_i and L_{i+1}) are incorporated in the leakage inductance of its adjacent transformer (i.e., $L_{s,i}(1-k_{m,i}^2)$. Hence,

$$L_{s,i}\left(1-k_{m,i}^2\right) = L_i + L_{i+1} \rightarrow k_{m,i} = \sqrt{1-\frac{Z_{0,i}+Z_{i+1}}{L_{s,i}\omega_0}}. \tag{14}$$

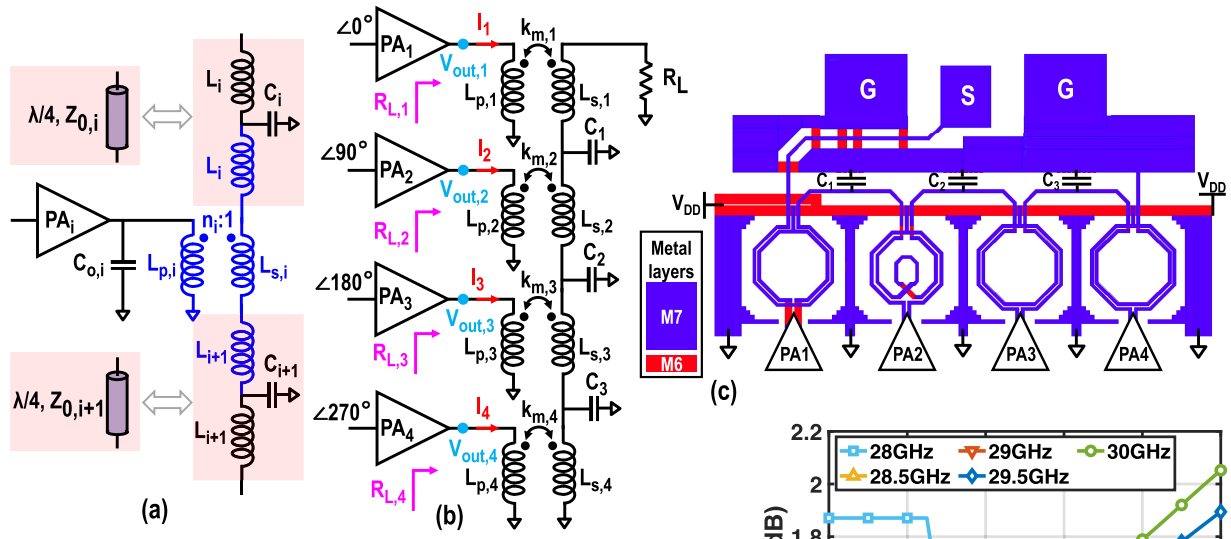
By replacing (13) in (14), the transformers' coupling factor can be approximated by

$$k_{m,i} = \sqrt{1-(Z_{0,i}+Z_{0,i+1})n_i^2 C_{o,i}\omega_0}. \tag{15}$$

Now, all essential equations are developed to design the proposed four-way SDC systematically. The procedure starts by determining V_{DD}, $P_{L,\max}$, and the placement of efficiency-peaking points across the input voltage. Then, n_1 should be calculated using (4) and checked if its value can be practically implemented on-chip. Otherwise, $P_{L,\max}$ or V_{DD} needs to be modified accordingly. The size of each PA and its corresponding parasitic output capacitance can be estimated by (9). The transformers' primary inductances are then calculated using (13) to absorb the PAs' output capacitances. Since the PBO points are distributed uniformly across V_{in} in this prototype, the second PA will be larger than the others [see Fig. 5(b)], resulting in a smaller primary inductance for the second transformer. $Z_{0,i}$ and $L_{s,i}$ may be approximated exploiting (12) and (13), respectively, after choosing $n_i \approx 1$ to practically achieve low-loss and compact on-chip transformers at mm-wave frequencies. Due to the chosen PBO distribution, the characteristic impedances of the last two TLs will be $R_L/4$. To finalize the design, the coupling factor of the transformers should be estimated by replacing the calculated values of n_i, $Z_{0,i}$ and $C_{o,i}$ in (15). However, due to the large $C_{o,2}$ and $Z_{0,2}$ values, $k_{m,2}$ becomes low, degrading the SDC efficiency dramatically. To increase $k_{m,2}$ and improve the SDC loss, n_2 is intentionally reduced by enlarging $L_{s,2}$, as suggested in (15). The above design procedure provides an adequate starting point for the implementation of the proposed SDC. However, recursive electromagnetic (EM) simulations are still required to capture the layout constraints (e.g., connection to ground-signal-ground, GSG pads) and fine-tune the combiner's parameters.

Fig. 6(b)–(d) reveals the final schematic, layout, and components values of the proposed four-way SDC, respectively. The resulted structure is as simple as a conventional series combiner, modified by adding three shunt capacitors between the transformers and driving the PAs with a progressive 90° phase shift. Since $L_{s,2} > L_{p,2}$ but not large enough to be implemented by a 1:2 transformer, the second turn of $L_{s,2}$ is realized by a relatively small spiral. The output GSG pads are deliberately placed in line with the SDC center to realize a similar distance between the output pads and the amplifiers. Any undesired coupling between the transformers would affect Doherty's operation and degrade the SDC loss and the TX linearity. To avoid that, the distance between the transformers is increased, and a ground plane is inserted around them.

Fig. 6(e) illustrates the SDC loss versus the normalized input voltage, m, for different frequencies extracted from momentum EM simulations. It is best to optimize the SDC loss at PBO points close to the PAPR of the desired signal. The structure loss is $\leq$1.4 dB for 4 dB$\leq$PBO$\leq$10 dB, where the probability density function (pdf) of a 64-/256-QAM signal is at its maximum. Note that the loss of a transformer-based MN is strongly a function of the resistive load seen at its secondary winding, as quantified in [44]. As this load significantly changes in the Doherty operation, a slightly larger loss (i.e., $\sim$2 dB) is observed at PBO $<$4 dB or $>$10 dB.



(d)

	#1	#2	#3	#4
L_p (pH)	184	144	212	212
L_s (pH)	210	254	218	218
k_m	0.6	0.47	0.62	0.62
n	0.94	0.75	0.97	0.97
Z_0 (Ω)	50	25	12.5	12.5

Fig. 6. (a) Replacing TLs with their equivalent T-model network, including two series inductors and a shunt capacitance, (b) schematic and (c) layout of the proposed four-way SDC, (d) its components' values, and (e) SDC loss versus the normalized input signal extracted from momentum EM simulations.

The loss variations over frequency are partly attributed to the inevitable misalignments among the resonant frequencies of the SDC's branches. This causes extra loss since the outputs of PAs are not summed perfectly due to the phase mismatches among the outputs of different SDC's branches. Moreover, the phase response of each resonator in the SDC is a function of its equivalent quality factor and, thus, its effective load resistance. Since the transformers' loads vary and differ in the SDC's branches in the Doherty operation, their outputs phases also shift unequally, introducing additional phase mismatches and loss.

III. Digital Polar Transmitter

Although a Cartesian-based TX can support a larger modulation BW (BW_{mod}), it suffers from a 3–dB worst case output power loss [40], thus reducing the system efficiency. Moreover, it needs two separated I and Q DACs at the output stage, thus demanding a 2× larger footprint, while the space between the SDC input ports is limited. Consequently, as shown in Fig. 7, a polar architecture is exploited in this work where four separated DPMs deliver a phase-modulated constant envelope signal to their corresponding DPAs to perform the required AM.

At the TX input, a common-source amplifier provides the input matching over the desired band and amplifies the input LO signal by ∼10 dB. A two-stage transformer-based quadrature hybrid [45], [46] with a >40 dB IRR over 16–35 GHz BW is then utilized to generate quadrature LO signals (LO_I & LO_Q) for the following DPMs. Two stages of 1:2 parallel power splitter based on coplanar TLs are employed to conveniently and uniformly distribute LO_I and LO_Q signals between four separated DPMs. To avoid excessive power loss due to the mismatch between the DPM's input impedance and the hybrid's output resistance, a transformer is also inserted between the two splitters to absorb the DPM's input capacitance and maximize the power transfer. Moreover, the required dc biasing of DPM is applied to the center tap of the transformer's secondary coil. Four DPMs are identical and realized by the weighted summation of LO_I and LO_Q signals based on their normalized I and Q data (e.g., $\hat{D}_{I,i} = D_{I,i}/(D_{I,i}^2 + D_{Q,i}^2)^{1/2}$). Hence, the 90° phase shift required among adjacent input ports of the four-way SDC can be conveniently realized by shifting the DPMs' input bitstream in the digital domain. The DPMs also act as a predriver and deliver a large and constant phase-modulated signal to their corresponding DPAs. As efficiency-peaking points are distributed uniformly across the input voltage, the relative sizes of the peaking DPAs to the main DPA are 1.5×, 1×, and 0.5×, respectively. The input data of different DPMs and DPAs are independently applied to the TX using 12 on-chip 1k-word SRAMs.

Due to the removal of analog reconstruction filters, the direct digital modulation creates images of the desired signal at the integer coefficients of the baseband sampling rate (f_s). The spectral images are attenuated by a sinc function due to DPA/DPM sample-and-hold operation. Consequently, the spurious-free dynamic range (SFDR) is calculated by

$$\text{SFDR} = 20\log_{10}\left(\left|\text{sinc}\left(1 - \frac{0.5 \times \text{BW}_{\text{mod}}}{f_s}\right)\right|\right). \quad (16)$$

Based on the 3GPP standard [47], the out-of-channel emission should be <−30 dBc, resulting in $f_s/\text{BW}_{\text{mod}} > 16$. In our

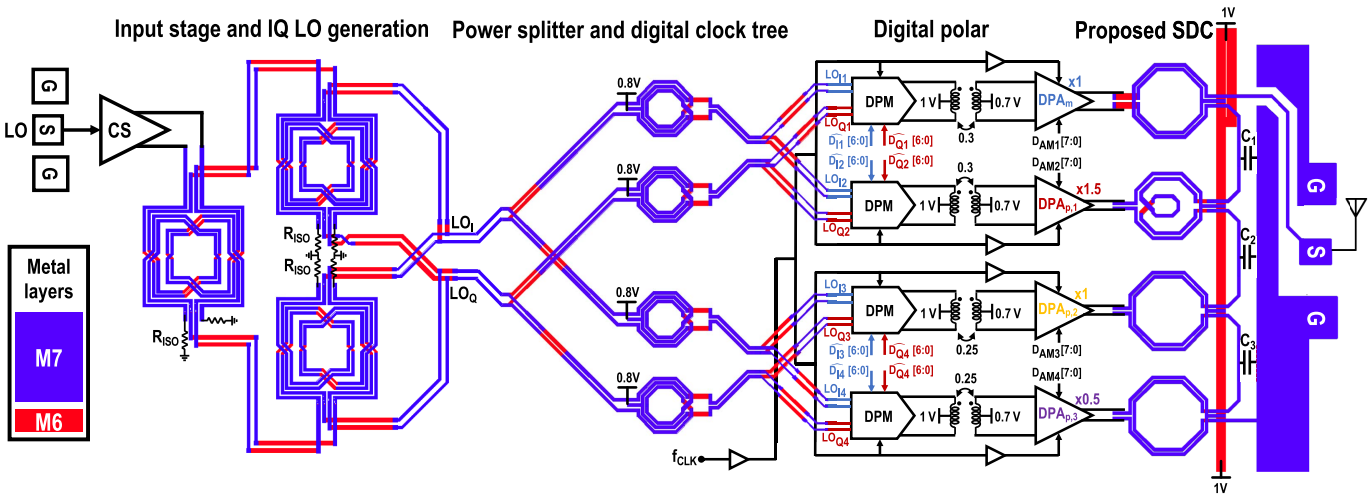


Fig. 7. Block diagram of the proposed DPTX.

design, f_s is 2.4 GHz limited by the maximum clock frequency of SRAMs, leading to $BW_{mod} = 150$ MHz. However, in practice, the output MN also attenuates the first sampling replica due to its bandpass characteristics. Therefore, even a larger BW_{mod} can satisfy the SFDR requirement.

Even if the TX's AM–AM and AM–PM nonlinearities are corrected by using a simple static DPD, the EVM will be limited by the DPA signal-to-quantization noise (SQR_{AM}), DPM's phase resolution (θ_Q), LO leakage power (P_{LO} in dBc), and DPM IRR (IRR_{PM} in dB) due to the components mismatch and LO_I and LO_Q gain/phase imbalance [48], [49]

$$EVM_{TX} = \sqrt{10^{\frac{SQR_{AM}}{10}} + \theta_Q^2 + 10^{\frac{P_{LO}}{10}} + 10^{\frac{IRR_{PM}}{10}}}. \quad (17)$$

By distributing the error budget uniformly among all parameters in (17), SQR_{AM}, P_{LO}, IRR_{PM} less than <-40 dBc, and $\theta_Q < 0.6°$ are required to achieve 2% (−34 dB) EVM.

A. Digital Phase Modulator

Due to the BW expansion of the polar architecture, an I/Q mixing DAC is chosen to directly modulate the mm-wave carrier with the baseband phase modulation (PM) data. The DPM comprises two 7-bit (including the signed bit) segmented I and Q mixing DACs to satisfy $\theta_Q < 0.6°$ and <1% amplitude variation at the DPM output, as shown in Fig. 8(b). Each DAC cell consists of a differential pair and a switchable tail transistor driven by its corresponding LO signal and the baseband PM data, respectively. Since the data are applied to the tail switch of the mixing cells, the DPM does not consume any power when its corresponding DPA is OFF, enhancing the system efficiency at PBO. A fully thermometer-coded design along with the retiming of the digital bitstream is used to minimize the timing mismatch and switching glitches, which are crucial in achieving high BW_{mod}. As the DPM's output signal experiences an about $6 \times BW_{mod}$ expansion, a wideband MN comprising a low coupling factor transformer [50] is placed at its output to transfer the PM signal to the DPA with <1 dB gain variation and <12 ps group delay variation over a 10 GHz BW.

Conventionally, the DPM is implemented using two physically separated I and Q mixing-DACs [37], [40]. Hence, due

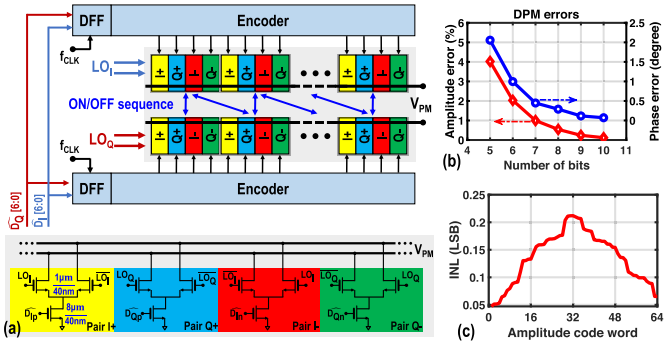


Fig. 8. (a) Simplified block diagram of the proposed DPM with interleaved I and Q cells. (b) Simulated phase and amplitude error versus the number of bits in the I/Q DACs. (c) Worst case INL of the I/Q DACs over 1000 runs of Monte-Carlo simulation.

to gradients in the gate-oxide thickness, substrate doping, and transistor's mobility, a global mismatch is observed between the I and Q DACs. This subsequently degrades the DPM phase resolution, IRR, and TX's far-out noise to much larger values than predicted by any statistical simulations. To resolve this issue, as shown in Fig. 8(a), the I and Q cells in the DPM are interleaved in the layout such that the effect of first-order process gradients along both axes is canceled. Nevertheless, even by employing a fully thermometer-coded DAC structure, the differential nonlinearity (DNL = (σ_I/I)) of DAC cells are quickly accumulated and form a much larger integral nonlinearity (INL) in the DAC transfer function. According to [51],

$$INL_{max} = 0.5\sqrt{2^{n_{I/Q}}} \times \left(\frac{\sigma_I}{I}\right) \quad (18)$$

where $n_{I/Q}$ is the number of bits in the I/Q mixing DACs. On the other hand, by using the Croon model [52], the drain-current mismatch can be calculated by

$$\left(\frac{\sigma_I}{I}\right)^2 = \frac{A_{VTH}^2\left(\frac{G_m}{I_D}\right)^2 + A_\beta^2}{W \times L} \quad (19)$$

where A_{VTH} and A_β are the threshold-voltage and current-factor proportionality parameters [53], respectively, and can

be obtained from measurements (as shown in [54], $A_{\mathrm{VTH}} = 3\ \mathrm{mV}\cdot\mu\mathrm{m}$ and $A_\beta = 0.6\%\cdot\mu\mathrm{m}$ for 40 nm CMOS technology). $W \times L$ is the active area of the differential pair transistors. Replacing (18) in (19) results in

$$W \times L = \frac{2^{n_{\mathrm{I/Q}}}}{4\mathrm{INL}_{\max}^2} \times \left(A_{\mathrm{VTH}}^2 \left(\frac{G_m}{I_D} \right)^2 + A_\beta^2 \right). \tag{20}$$

By considering $(G_m/I_D) = 5$ to optimize the device maximum oscillation frequency ($f_{\max}$) and using a minimum length transistor, W should be wider than 0.8 μm to achieve $\mathrm{INL}_{\max} < 0.5$ LSB. This has been also verified by means of a Monte-Carlo simulation with 1000 samples, as shown in Fig. 8(c).

B. Digital Amplitude Modulation

As illustrated in Fig. 9(a), each DPA comprises 2-bit binary (LSB) and 6-bit unary (MSB) segmented cells to satisfy the required $\mathrm{SQR}_{\mathrm{AM}}$ with some margin and provide enough dynamic range for DPD. The total size of each DPAs is determined by its required maximum current and turned out to have LSB cells of almost the same size as DPMs. Consequently, by having one extra bit in the DPAs, their INL will be theoretically $\times\sqrt{2}$ larger than DPMs and reaches $\sim$0.4 LSB, as observed from the Monte-Carlo simulation results in Fig. 9(b). Each DPA cell consists of a differential pair and a switchable tail transistor driven by its corresponding constant-envelope PM signal and the baseband AM data, respectively. In this design, the input and output signals with the same phase are routed in parallel with two consecutive metal layers. Capacitive and inductive coupling between those lines provides a compensation current to cancel the undesired feedback due to the parasitic gate–drain capacitance (C_{gd}) of each transistor. This neutralization technique enhances the DPA's power gain and reverse isolation [55], thus significantly reducing the LO leakage at the TX output.

C. AM–AM Linearity

It is also instructive to investigate the inherent AM–AM linearity of the proposed digital Doherty TX and compare it with its analog counterpart. The simplified schematics of the main branch of both analog and digital Doherty PAs are shown in Fig. 10(a) and (b), respectively. In the analog PAs, the output power is controlled directly by changing the amplitude of the input voltage, V_{in}, while, for the DPAs, a constant amplitude signal is applied at the DPA's input, and the amplitude code word (ACW) controls the output power. In both structures, based on the resistive division between the output ($R_{\mathrm{out},1}$) and load ($R_{L,1}$) resistances of the main PA/DPA, a fraction of the main PA/DPA output current flows into the load (R_L) and creates a load voltage (V_L). Consequently, the voltage gain of the analog Doherty PA can be estimated by

$$G_{\mathrm{SDC},A} = \frac{V_L}{V_{\mathrm{in}}} = G_{m,1} \times \frac{R_{\mathrm{out},1}}{R_{\mathrm{out},1} + R_{L,1}} \times R_L \tag{21}$$

where $G_{m,1}$ is the transconductance gain of the main PA. In this structure, $G_{m,1}$ and $R_{\mathrm{out},1}$ are almost constant, while

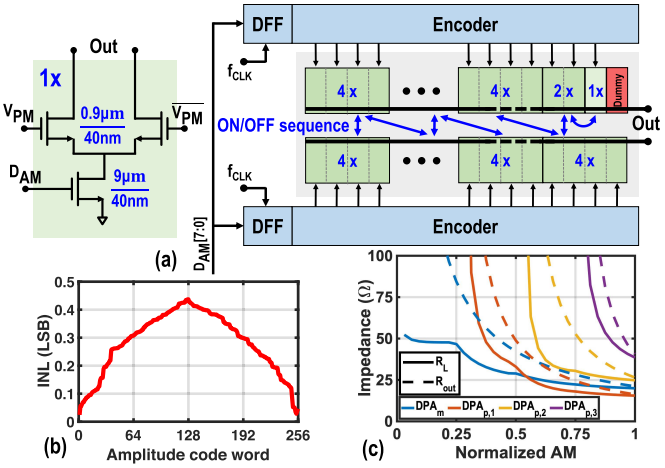


Fig. 9. (a) DPA simplified block diagram along with sizes of the transistors for the LSB cell of the main DPA, (b) its worst case INL over 1000 runs of Monte-Carlo simulation, and (c) output and load resistance of the main and peaking DPAs versus normalized input voltage.

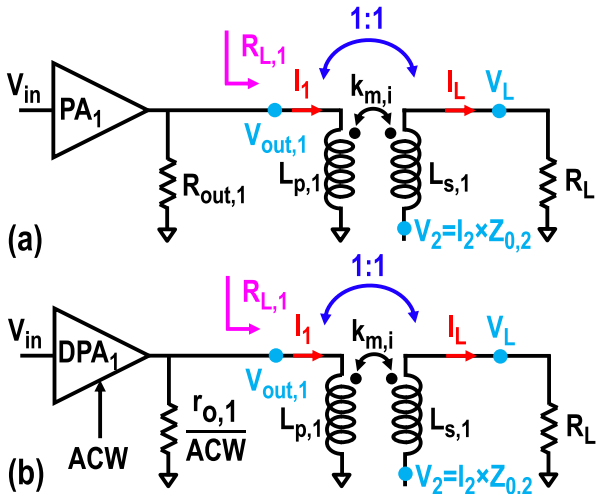


Fig. 10. Simplified schematic of the main branch of (a) analog Doherty PA and (b) digital Doherty PA.

$R_{L,1}$ reduces when the peaking PAs turn on. Hence, PA experiences gain expansion before going to saturation, as can also be gathered from the measured gain plots in [22], [28], and [29]. Ideally, $R_{\mathrm{out},1}$ should be designed to be much larger than $R_{L,1}$ to avoid any AM–AM distortion. However, it is not practically possible to satisfy that condition, especially when a large output power is required to be delivered at mm-wave frequencies. A possible solution is to use cascode topology to increase $R_{\mathrm{out},1}$. However, the large difference between $R_{\mathrm{out},1}$ and R_L significantly degrades S_{22}, as can be observed in the measurement results in [26] and [27].

For the digital Doherty PAs, the output power is controlled by turning on and off the DPA's cells. Hence, the DPA gain is defined as the ratio of V_L to ACW estimated by

$$G_{\mathrm{SDC},D} = \frac{V_L}{\mathrm{ACW}} = g_{m,1} V_{\mathrm{in}} \times \frac{r_{o,1}}{r_{o,1} + \mathrm{ACW} \times R_{L,1}} \times R_L \tag{22}$$

where $g_{m,1}$ and $r_{o,1}$ are, respectively, the transconductance and output resistance of the LSB cell in the main DPA.

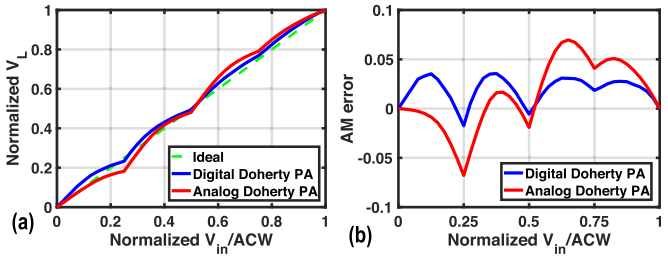


Fig. 11. Simulated (a) AM–AM and (b) deviation from the ideal curve (AM error) for analog and digital four-way series Doherty PAs.

In this case, as ACW increases, more cells in peaking PAs get involved, and $R_{L,1}$ reduces due to the load modulation. Consequently, the ACW $\times$ $R_{L,1}$ variation versus the output power reduces significantly as the variations of $R_{L,1}$ and ACW cancel each other out in the first-order approximation, thus improving the AM–AM linearity of the digital Doherty structure compared with their analog counterparts. In other words, DPA's output resistance increases by reducing ACW and approximately follows the load modulation imposed by the SDC [see Fig. 9(c)], creating a stable loading condition for the DPAs.

To validate this discussion, the simulated linearity performances of analog and digital Doherty amplifiers are compared when the SDC is ideally implemented with lossless components. The sizes of the analog main and peaking PAs are exactly the same as their corresponding digital counterparts when all DPA cells are ON. Fig. 11(a) and (b) shows the simulated AM–AM curves and their deviation from the ideal line (i.e., AM error), respectively. As expected, the digital Doherty PA shows more linear performance in the entire operation range. In the analog configuration, due to the large $R_{L,1}/R_{\text{out},1}$ variations, the AM–AM curve is below the ideal line for the first half of the output range and goes to the upper side for the second half. Although the digital Doherty PA demonstrates a better AM–AM linearity compared to the analog one, it still needs DPD to satisfy the EVM requirements of the 5G applications. However, a more linear structure would require a simpler DPD with lower resolution and shorter training time, thus potentially improving the total system efficiency and complexity.

D. Time Alignment

Similar to any Doherty structure, any time misalignment between the Doherty branches can distort the output signal, thus degrading the TX linearity performance. To resolve this issue, a clock tree distribution network is employed to synchronize the PM and AM data in different Doherty branches. The clock distribution is implemented using top metal layers to reduce interconnect resistance. Therefore, a single buffer could drive the entire network, eliminating the power consumption of distributed buffers and minimizing the clock skew. On the other hand, similar to any polar architecture, the delay mismatch between the PM and AM paths (τ) increases the magnitude of the third-order intermodulation distortion (IM3D). According to Su and McFarland [56],

$$\text{IM3D} = 2\pi\,(\text{BW}_{\text{mod}} \times \tau)^2. \tag{23}$$

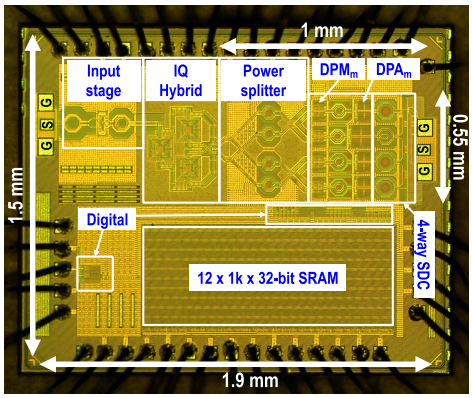


Fig. 12. Die micrograph of the proposed DPTX.

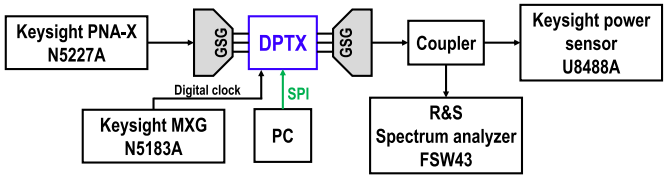


Fig. 13. Simplified block diagram of the measurement setup.

Considering a desired BW_{mod} of 400 MHz, τ must be $<$100 ps to achieve IM3D <-40 dBc. As can be gathered from Fig. 7, the PM and AM signals are recombined in the DPA. On the one hand, the baseband PM data go through the DPM and its output MN, consequently experiencing some delay. On the other hand, as the DPA is farther away from the clock generation block, the baseband AM data are sampled with a latency compared to the PM data. Those delays can be designed to be approximately equal to minimize AM and PM misalignments at the TX output. In this work, to reduce the time mismatch even further, the original data are applied to an off-chip fractional delay function with up to 2 ps resolution, and the time-shifted results are uploaded into the corresponding on-chip memory.

IV. Experimental Results

The proposed TX was fabricated in a 40 nm bulk CMOS process with ultrathick metal. As shown in Fig. 12, it occupies $1.9 \times 1.5\,\text{mm}^2$, including pads and the 12 1k-32bit SRAMs. The core size of the TX, including the I/Q power splitter, DPMs, DPAs, and SDC, is $1 \times 0.55\,\text{mm}^2$; thus, it is thin enough to be incorporated into mMIMO arrays even when requiring the TX to fit in a $\sim$600 μm pitch. The DPTX runs off a 1.0 V supply, while the SRAM and digital circuitries operate on a separate 1.1 V domain. The baseband data (i.e., $D_{\text{AM},i}$, $\hat{D_{I,i}}$, and $\hat{D_{Q,i}}$ in Fig. 7) are generated in MATLAB and loaded into the SRAMs via a serial peripheral interface (SPI). As illustrated in the measurement setup in Fig. 13, GSG probes are employed to apply the required LO signal to the TX and measure its output performance. The losses of the cables and probes are deembedded by performing thru-reflect-load (TRL) calibration up to the probes' tips using Keysight PNA-X N5227 and Cascade calibration substrate. Hence, the loss associated with input and output GSG pads is not de-embedded and included in the TX measured results.

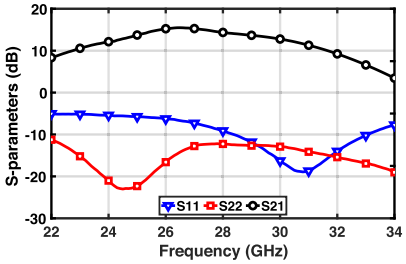


Fig. 14. Measured small-signal S-parameter.

N5227 is also employed for s-parameter measurement and to generate the required LO in the large signal and modulation measurements. Rohde & Schwarz FSW43 measures the TX spectral purity and EVM performance, while Keysight power sensor U8488A evaluates its output power.

Figs. 14 and 15 show the S-parameters and large-signal continuous-wave (CW) measurement results, respectively. S_{21} peak is 15 dB at 26.5 GHz with a -3 dB BW from 24 to 31 GHz. The input matching is better than -10 dB from 28.3 to 33 GHz, while $S_{22} < -10$ dB across all the measured frequencies. At 29.5 GHz, the TX achieves 18.7 dBm saturated output power (P_{sat}), and a maximum drain efficiency ($\eta_{D,\text{max}}$) and system efficiency ($\eta_{\text{TX,max}}$) of 36% and 24%, respectively. The power consumptions of DPAs, DPMs, and all digital blocks except for SRAMs are included in the system efficiency calculations. Moreover, the TX demonstrates $P_{\text{sat}} > 18$ dBm, $\eta_{D,\text{max}} > 33\%$, and $\eta_{\text{TX,max}} > 21\%$ over a frequency range from 26.5 to 29.5 GHz. As can be gathered from Fig. 6(b), the measured drain efficiency (η_D) versus the output power resembles the ideal four-way Doherty response from 28 to 30 GHz. At 29.5 GHz, the TX demonstrates four η_D peaks of 31%/36%/35%/22% at PBO = 0/2/4.5/11.5 dB, enhancing η_D by 1.6×/2.1× over a reference ideal Class-B PA at PBO = 4.5/11.5 dB. The η_D decline at the deepest PBO is due to the additional SDC loss, as justified in Section II-D. More interestingly, as illustrated in Fig. 15(d), the system efficiency (η_{TX}) is almost constant over the second half of the input ACW as a consequence of the Doherty operation and digital behavior of the proposed TX in which the idle cells in the DPMs and DPAs are entirely OFF at PBO.

To evaluate the intrinsic IRR of the DPM and uncalibrated LO feedthrough (LOFT) of the TX, a single sideband tone at different offsets from the LO frequency is generated by the DPM, while the main DPA is entirely ON, and all the peaking DPAs are OFF. Without any calibration, IRR > 42 dB and LOFT < -40 dBc are measured, as shown in Fig. 16.

Fig. 17(a) depicts the measured AM–AM characteristics of the proposed TX at 29.5 GHz before applying DPD. For ACW < 0.25, only the main DPA is ON, and the TX is almost linear. When ACW exceeds 0.25, the first peaking PA gradually starts engaging its subcells, thus modulating the resistive load seen by the transformers and reducing the SDC loss, as explained in Section II-D [see Fig. 6(e)]. As a result, the TX gain deviates from its initial value for 0.25 < ACW < 0.4. From ACW = 0.4, until the last peaking DPA is engaged (i.e., ACW = 0.75), the SDC loss is almost constant [see Fig. 6(e)], and consequently, the TX gain goes back to its

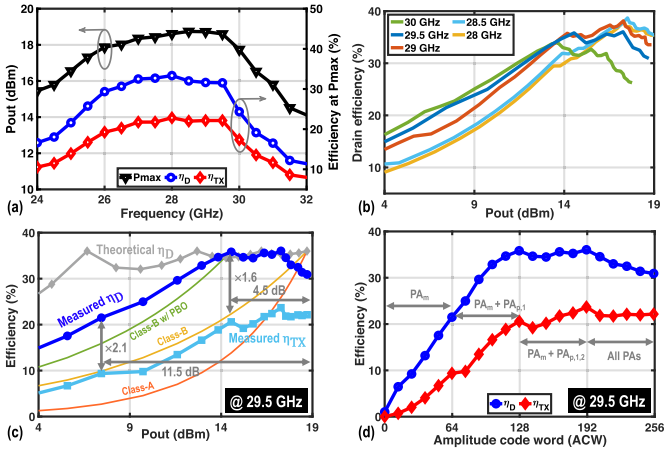


Fig. 15. Large-signal CW measurement results. (a) P_{sat}, $\eta_{D,\text{max}}$, and $\eta_{\text{TX,max}}$ versus operating frequency, (b) and (c) η_D versus output power (P_{out}) for different carrier frequencies, and (d) η_D and η_{TX} across DPA's ACW at 29.5 GHz.

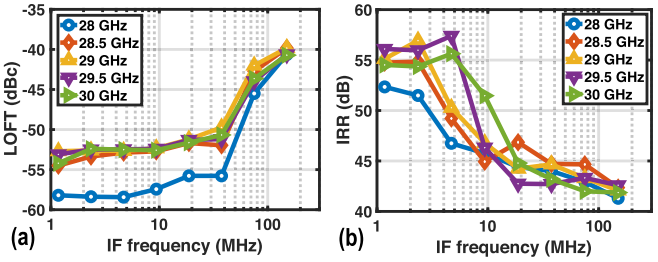


Fig. 16. (a) DPM's IRR and (b) TX LOFT versus IF frequency.

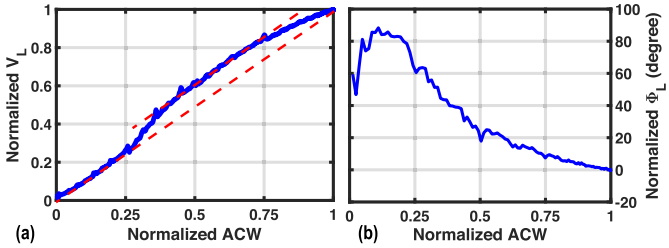


Fig. 17. Measured (a) AM–AM and (b) AM–PM of the proposed TX at 29.5 GHz without applying DPD.

initial value. Finally, in the last region (0.75 < ACW < 1), the TX experiences gain reduction due to the SDC loss increase and DPAs' saturation.

Fig. 17(b) shows the AM–PM curve when the TX generates a two-tone signal with a tone-spacing of 2.34 MHz, and the phase of the demodulated output signal is measured. Generally, the output delay increases by reducing ACW, as the output resistances of DPAs raise, while their output capacitances are almost constant. However, for ACW < 0.05, the output phase reduces as the leakage from the main DPA inputs becomes comparable with the desired signal. Moreover, due to the sudden engagement of the peaking DPAs, the output phase slightly drops at ACW = 0.25, 0.5, and 0.75.

To compensate for the PM-PM and PM-AM distortions caused by undesired interactions between I and Q banks in the DPM and also the AM–AM and AM–PM nonlinearities of the DPA, a lookup table (LUT)-based static 2-D DPD [57] is employed for the rest of the measurement results. The TX's output spectrum for a 150 MHz 64-QAM modulated

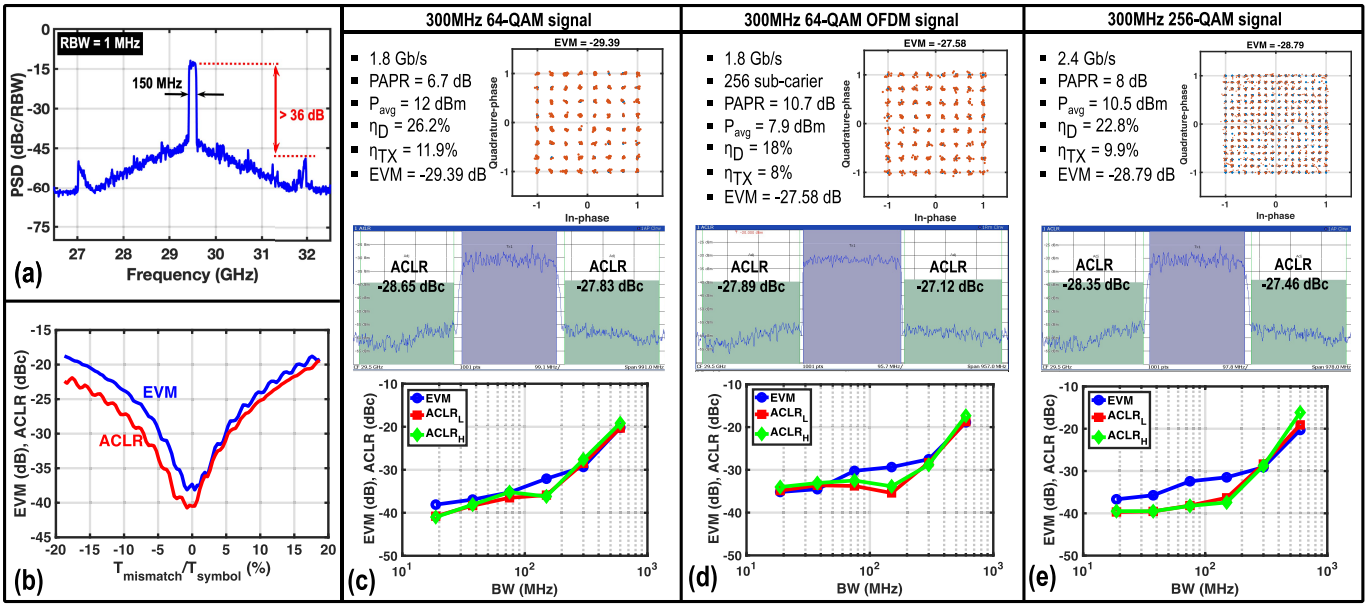


Fig. 18. Measured (a) output spectrum, and (b) EVM and ACLR versus delay mismatch between the AM and PM paths. Measured TX performance while transmitting a 300-MHz (c) 64-QAM single-carrier, (d) OFDM, and (e) 256-QAM single-carrier signal.

signal with $f_s = 2.4$ GSample/s is depicted in Fig. 18(a) where the sampling spectral replicas are suppressed more than 36 dB due to the SDC filtering and the DPA/DPM zero-order hold operation. Fig. 18(b) shows the measured EVM and adjacent channel leakage ratio (ACLR) versus the delay mismatch between AM and PM paths for a single-carrier 20 MHz 64-QAM modulated signal. As indicated in (23), the delay mismatch degrades ACLR by a 6 dB/octave slope. Moreover, the delay mismatch must be smaller than 2% of the symbol period to achieve <-35 dB EVM.

Fig. 18(c)–(e) shows the measured output constellation and spectrum of the TX for different modulation schemes and BWs. For a single-carrier 64-QAM signal with 6.7 dB PAPR and 300 MHz BW_{mod}, the TX achieves 26.2% average drain efficiency ($\eta_{D,\text{ave}}$), 11.9% average system efficiency ($\eta_{\text{TX,ave}}$), -29.4 dB EVM, and -27.8 dB ACLR while delivering 12 dBm average output power (P_{ave}) to the load. The TX is then challenged by a 300 MHz 64-QAM OFDM signal with 10.7 dB PAPR to demonstrate its efficiency at deep PBO. In this case, it exhibits $\eta_{D,\text{ave}}$ of 18%, $\eta_{\text{TX,ave}}$ of 8%, -27.6 dB EVM, and -27 dBc ACLR. Furthermore, the TX demonstrates $P_{\text{ave}} = 10.5$ dBm, $\eta_{D,\text{ave}} = 22.8\%$, $\eta_{\text{TX,ave}} = 9.9\%$, ACLR $= -27.5$ dBc, and EVM $= -28.8$ dB while transmitting 300 MHz 256-QAM signal to increase its data rate to 2.4 Gbit/s. As can be gathered from the last row in Fig. 18, for all tested modulation schemes, the TX's EVM and ACLR improve up to 6 and 10 dB, respectively, by reducing $\text{BW}_{\text{mod}} < 150$ MHz.

Fig. 19 shows the measured power breakdown of the proposed TX in two test cases at 29.5 GHz. First, when the TX generates a CW signal at its maximum power, all DPAs and DPMs are active and consume 229 and 84 mW, respectively. In the second test, the TX transmits a 64-QAM 300 MHz modulated signal with ~6.7 dB PAPR. Due to the Doherty operation, the dc power of DPAs almost decreases linearly with the output power and reaches 60 mW. Moreover, the

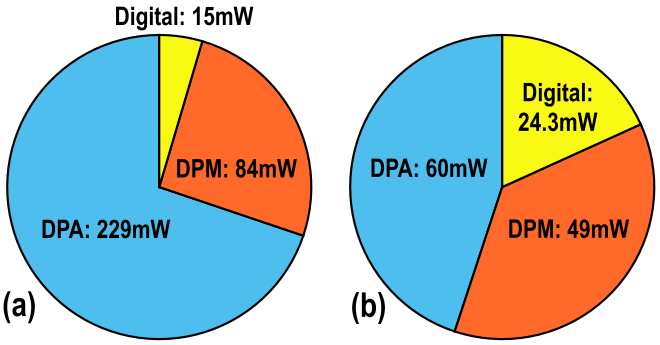


Fig. 19. Measured power breakdown when the TX generates (a) CW signal at its peak power and (b) 64-QAM 300 MHz modulated signal with ~6.7 dB PAPR.

DPMs power dissipation decreases to 49 mW since only two DPMs are active on average at ~6.7 dB PBO. However, the digital circuitries are switching more in this case and consume 9.3 mW more.

Table I summarizes the performance of the proposed TX and compares it with the state-of-the-art mm-wave digital and analog TXs and PAs. Analog PAs/TXs without efficiency enhancement technique [58], [59] are also added to demonstrate the energy efficiency benefits of the proposed Doherty network. This work demonstrates the highest Doherty order (four-way) with an outstanding drain and system efficiency at an 11.5 dB PBO. Moreover, it is the first reported mm-wave Doherty structure that includes the entire TX chain, all the way from binary I/Q data up to the modulated mm-wave output signal.

A. Discussion

Although an LUT-based 2-D DPD is employed to compensate for static AM–AM and AM–PM nonlinearities, the

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART MM-WAVE PAS AND TXS

				mm-wave digital TX			mm-wave analog Doherty TX/PA				Outphasing TX/PA		Analog TX/PA	
Parameter	**This work**			Thakkar, JSSC'19 [40]	Qian, JSSC'20 [36]	Nguyen, RFIC'20 [37]	Wang, JSSC'19 [26]	Nguyen, JSSC'20 [27]	Nguyen, ISSCC'19 [21]	Pashaeifar, ISSCC'21 [29]	Li, JSSC'21 [14]	Rabet, JSSC'20 [10]	Garay, ISSCC'21 [58]	Zhu, CICC'21 [59]
PA/TX	**TX**			TX	TX	TX	PA	PA	PA	TX	TX	PA	PA	TX
Architecture	**Digital polar**			Digital polar	Digital Cartesian	Digital polar	Analog Cartesian	Analog Cartesian	Analog cartesian	Analog cartesian	Analog cartesian	Analog cartesian	Analog cartesian	Analog cartesian
Full chain (bits-in RF-out)	**Yes**			Yes	Yes	Yes	No	No	No	No	No	No	No	No
Eff. enhancement	**Series Doherty**			N/A	Impedance variation comp.	N/A	3-bit mixed signal Doherty	Coupler-based Doherty	Doherty	Doherty	Inverse outphasing	outphasing	Dual-drive technique	N/A
Order of Doherty Network	**4-way**			N/A	N/A	N/A	2-way	2-way	3-way	2-way	N/A	N/A	N/A	N/A
Technology	**40 nm CMOS**			28 nm CMOS	28 nm CMOS	28 nm CMOS	45 nm SOI CMOS	45 nm SOI CMOS	45 nm SOI CMOS	40 nm CMOS	45 nm SOI CMOS	130nm SiGe	45 nm SOI CMOS	65 nm CMOS
Frequency (GHz)	**29.5**			63	23	60	27	60	57	27	29	27.5	30	28
V_{DD} (V)	**1**			0.9	1	0.9	2	2	2	1	2	4	1.9	--
P_{max} (dBm)	**18.7**			11.5	19.02	12.6	23.3	20.1	21.2	20	22.7	19	20.1	18.4
$\eta_{D,max}$ (%)	**36**			39	34.4	26	40 (PAE)#	26 (PAE)#	21.8 (PAE)#	39.8	42.6	34	59.3	21.3 (PAE)#
$\eta_{TX,max}$ (%)	**24***			N/A	22.1	N/A	N/A	N/A	N/A	28.5	34	N/A	N/A	N/A
η_D (%) @ 6dB/11.5dB	**33/22**			22.2/--	17.9/--	7/3**	33.1/15** (PAE)#	16.6/10** (PAE)#	19.5/12** (PAE)#	30/15 (@26GHz)**	30/11**	23/13**	30/13**	12/5**
η_{TX} (%) @ 6dB/11.5dB	**15*/10***			N/A	N/A	N/A	N/A	N/A	N/A	19/9 (@26GHz)**	N/A	N/A	N/A	N/A
Modulation scheme	**64-QAM**		**256-QAM**	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	5G NR FR2	64-QAM
Signal type	**OFDM**	**SC†**	**SC**	SC	SC	SC	SC	SC	SC	SC	SC	OFDM	N/A	SC
PAPR (dB)	**10.7**	**6.7**	**8**	N/A	N/A	N/A	6.5	N/A	N/A	N/A	6	N/A	N/A	N/A
BW (MHz)	**300**	**300**	**300**	3500	500	1760	1000	500	500	800MHz	500	100	200	400
EVM (dB)	**-27.58**	**-29.39**	**-28.79**	-24.7	-28.9	-27.4	-25.3	-27.2	-27.2	-24.6	-25.3	-26.2	-25	-28.7
ACLR (dBc)	**-27.5**	**-28**	**-28**	N/A	-33.6	N/A	-29.6	-32.65	-32.65	-32.35	-29.8	-33	-26.5	-27.5
P_{avg} (dBm)	**7.9**	**12**	**10.5**	6	9.96	5.8	15.9	13.5	13.5	11.36	16	11.9	11.4	13.5
$\eta_{D,avg}/\eta_{TX,avg}$ (%)	**18/8**	**26.2/11.9**	**22.5/9.9**	--/4.4	14/--	8.5/3.9	29.1 (PAE)#/--	17.5 (PAE)#/--	17.5 (PAE)#/--	17.6/10.5	23.8/--	20.2 (PAE)#/--	17 (PAE)#/--	5.2 (PAE)#/--
DPD	**Yes**			Yes	Yes	Yes	No	No	No	No	Yes	No	No	No
Core area (mm²)	**1.1**			3.24††	0.2	0.115	0.52	0.76	3.61††	1.38	0.96	0.77††	0.21	0.6§

* The power consumption of DPAs, DPMs, and digital circuits (except SRAM) is considered in the SE calculation. ** Estimated from the plots. # The power consumption of PAs and pre-drivers is included.
† Single carrier. †† Die size calculated from die micrograph. § Half of a single TRX element area

measured EVM still degrades when BW_{mod} exceeds 150 MHz. Consequently, it is instructive to investigate the main contributors to the TX EVM at low and high modulation BWs. The DPA and DPM quantization noise and the TX's LOFT mainly limit EVM to around -40 dB at low BWs, as discussed in Section III and quantified in (17). As BW_{mod} increases, the impact of memory effects, BW expansion of PM signal, and finite sampling frequency on the EVM become dominant.

Memory effects are variations in the TX nonlinear characteristics due to the history of the input data. The major contributor to the memory effects in the proposed TX is the change in drain voltage due to the nonzero power supply impedance caused by bond wires and a limited amount of high-quality on-chip decoupling capacitors. Hence, the drain voltages of the DPA/DPM's transistors experience a different voltage depending on the previous samples, changing their gain and phase response. Another source of memory effects originates from switching the tail transistor of the DPA/DPM cells, generating a voltage step at the source terminal of their differential pairs, which then couples to the gate through their parasitic gate–source capacitance. The resulting gate voltage variation should settle before the next sample arrives to diminish the memory effects. In the proposed TX, regardless of the modulation BW, the sample rate is always fixed (i.e., f_s). However, by increasing BW_{mod}, the upsampling rate decreases, and the variation between two adjacent samples increases significantly. Therefore, the drain/gate voltage experiences bigger jumps that result in larger gain and phase error for the next symbol. Although a 2-D DPD could partially compensate for the memory effects, it requires a large number of symbols in the training phase, while the SRAM length used in the TX limits the accuracy of this correction.

On the other hand, standard LUT-based 2-D DPDs have the same correction for all frequencies. However, the TX AM–AM and AM–PM characteristics vary over frequency. Consequently, the DPD EVM improvement becomes limited as BW_{mod} raises.

Moreover, the skirt of the replicas of the BW expanded PM signal at the integer coefficients of the sampling frequency appears on top of the desired in-band PM signal. Ideally, multiplying the resulting PM signal with AM data will cancel the leakage of the PM replicas in the reconstructed output signal, thus maintaining TX EVM. However, the limited BW of the interstage MNs in the PM path filters parts of the PM replicas. As a result, the reconstructed signal will be distorted, limiting TX EVM. Due to the data dependency of this phenomenon, the resulting nonlinearity cannot be fully compensated by a static DPD. All the abovementioned reasons contribute to EVM degradation of the proposed TX for $BW_{mod} > 150$ MHz.

V. CONCLUSION

In this article, a scalable N-way SDC was proposed that can be compactly and efficiently realized by using N transformers and $N-1$ TLs. Guidelines were developed for the SDC design based on the required maximum power and the distribution of the efficiency-peaking points. The proposed SDC is then employed in a four-way Doherty DPTX, where four independent DPMs and DPAs, respectively, modulate the phase and amplitude of a mm-wave carrier with the baseband data. It is

shown that the combination of the DPA and SDC can alleviate AM–AM distortion as the DPA output resistance roughly follows the variations of the SDC input resistance imposed by the active load modulation. Moreover, the DPM's cells in the I and Q mixing DACs are interleaved in the layout to minimize their current mismatch, thus resulting in IRR $>$ 40 dB. Fabricated in a 40 nm CMOS process, the 1.1 mm^2 TX achieves 18% average drain efficiency and $-$27.6 dB EVM while transmitting a 300 MHz 64-QAM OFDM signal with a 10.7 dB PAPR.

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