R. J. Albuquerque

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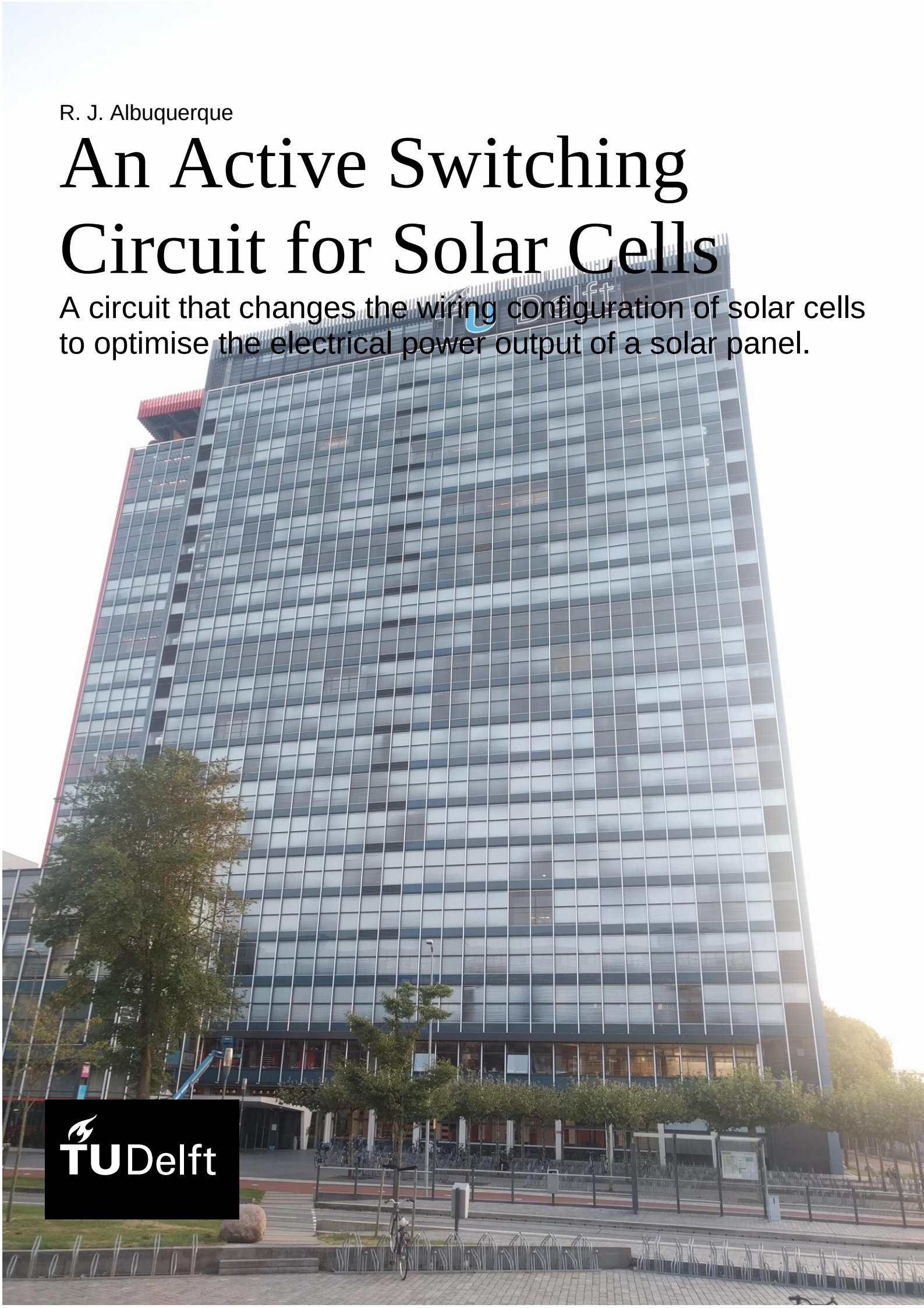

An Active Switching Circuit for Solar Cells

A circuit that changes the wiring configuration of solar cells to optimise the electrical power output of a solar panel.

By

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R. J. Albuquerque
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Abstract

The electrical output of a solar panel can be optimised in several ways, through the inclusion of bypass diodes (BPDs) or to have a maximum power point (MPP) tracker or DC optimiser to ensure that the panel is always operating at its global MPP. However most of these systems have to be implemented externally to the panel. A new system, the Solar Cell-level Power Management (SCPM) circuit was proposed as a means to actively sense shading and switch between three wiring configurations as inspired by matrix converter theory. The SCPM circuit would operate for 16 solar cells arranged in a 4 x 4 cell solar panel and be able to change the wiring configuration of these sixteen cells using 11 MOSFET switches. The base unit of the panel is a substring composed of four solar cells in series and the circuit would switch from 16 x 1 with 16 cells in series, 8 x 2 with 8 cells in a string with two strings in parallel and 4 x 4 with 4 cells in a string and with four strings in parallel. The shading would be measured through four current sense resistors and amplifiers, with one of these pairs in each substring and a differential operational amplifier system to measure the voltage across the strings. The current and voltage measurement help determine the power output of the panel. A Simulink model of the system was first created and a panel with 4 x 4 solar cell arrangement ordered and then measurements made with shading to verify if the shading model was accurate. From these results a Simulink model for the SCPM circuit was designed to test the theory of its functionality and if such a circuit could be controlled to switch between the three wiring configurations. The SCPM circuit was successfully built and was able to operate in this way however due to operation of all 11 switches in the triode mode of operation and the necessity to include blocking diodes to negate the effect of the MOSFET body diode, the SCPM circuit's electrical efficiency was greatly reduced.

Glossary

BJTs – Bipolar Junction Transistors

BoM – Bill of Materials

BPDs – Bypass Diodes

FETs – Field Effect Transistors

LLP- Loss of Load Probability

MOSFETs – Metal Oxide Semiconductor Field Effect Transistors

MPP – Maximum Power Point

MPPT – Maximum Power Point Tracking

MPU – Microprocessor Unit

N-FETs – N-channel FETs

NPNs – N-type, P-type, N-type

PCB – Printed Circuit Board

P-FETs – P-type FETs

PNPs – P-type, N-type, P-type

PV – Photovoltaic

SC – Shading Configuration

SF – Shading Factor

SCPM – Smart Cell-level Power Managed

Wi-Fi or WiFi – Wi-Fi Alliance Communication Protocol

Contents

1 Introduction

1.1. Problem Statement

The energy transition from conventional fuel sources to renewable energy sources is now well underway [1]. One of several renewable energy sources leading this transition is photovoltaic (PV) technology utilising PV panels and these have shown great promise both in commercial solar farms and in small scale residential applications. Solar generation adoption in both cases has a problem when shading occurs that can greatly diminish the electrical power output of a PV system. The focus of this thesis is to determine and implement a means for ensuring that the electrical output power of a PV panel is always optimised. The system and its circuit must function despite shading occurring and will operate by changing the wiring configuration of solar cells within the solar panel to achieve the optimised power output.

1.1.1 Shading

Photovoltaic panels if mounted properly in direct sunlight, can yield power close to their rated Wp values (the more uniform sunlight the more power). One of the problems however is shading and the occurrence of this when a solar panel shades an adjacent one and can drastically reduce the power output of a PV panel when not in direct sunlight [2, 3]. This especially affects solar panels where several cells are organised into strings of 20 solar cells in length.

Shading of a few cells in the string can result in a reduction in current for the whole string or the activation of a bypass diode in parallel with the 20 solar cells and thus reduce the total power output of the panel through bypassing a single string. Another means of ensuring greater shading tolerability is to have a large proportion of cells in a panel oriented in parallel thus the total current output is the sum of the individual cell currents. However this results in larger output current from the panel and is not desirable due to greater power dissipation losses in the cables. This is especially in the case where long power cable lengths are used for connection to DC optimizers or inverters.

1.1.2 Bypass Diodes

When a cell undergoes shading it goes from forward bias to reverse bias and provides a pathway for current to flow albeit at a reduced current for all cells in the string. This can create a hotspot in the shaded cell due to heat dissipation and thus effect both its operation lifetime, that of the other solar cells in its string and the laminate of the solar panel as self-heating occurs [4].

The use of Bypass Diodes (BPDs) can mitigate this effect by providing an alternative pathway through which current can flow during shading conditions, however this has the previously mentioned effect of decreasing the output power of the overall solar panel [5]. BPDs are typically low forward voltage drop diodes of 0.4-0.6 V such as Schottky diodes that are able to handle high solar cell currents on the order of 3-10 A. Thus the limiting factor in BPD selection are these two factors. The functionality of the BPD concept is illustrated in Figure 1.

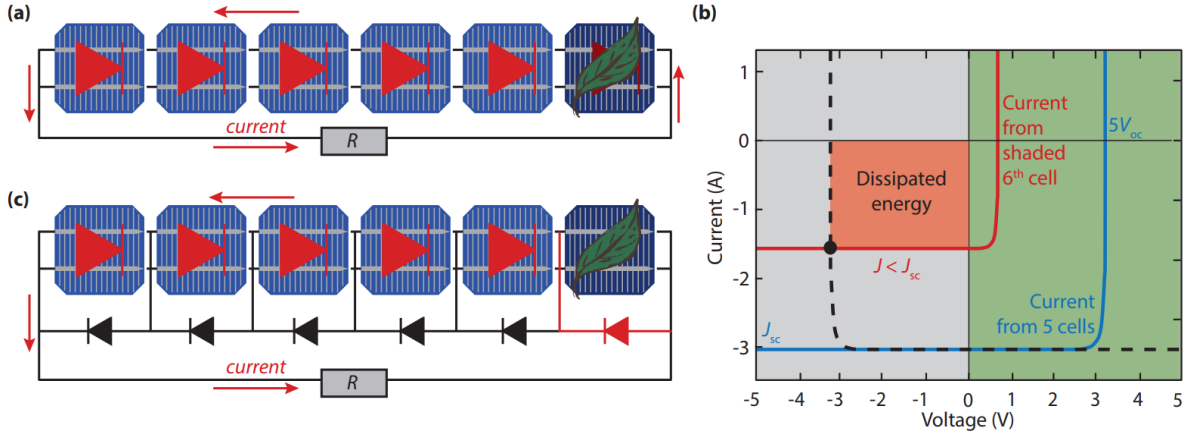


Figure 1: A solar panel consisting of (a) a string of six solar cells with one partially shaded, this (b) has a significant effect on the I-V curve of the string. (c) Bypass diodes are employed to mitigate this effect caused by partial shading. From [5].

In Figure 1a, there are six solar cells arranged in series and one is shaded. This results in the red line of "Current from shaded 6th cell" in Figure 1b. There is a large dissipated energy due to current passing through the now reverse-biased shaded cell. In Figure 1c, the ideal case of having one bypass diode per cell is shown where the shaded cell can be bypassed through its BPD and this results in the blue line of "Current from 5 cells" in Figure 1c. Here it can be clearly seen that there is no power dissipation in the shaded cell and thus the max power point is determined by the five illuminated cells. There is however some power dissipation across the BPD however this is negligible compared to the previous dissipated energy. One of the ideas that was investigated was having a BPD in anti-parallel with each cell to overcome the effect of shading. There is a wealth of research conducted on this [6, 7, 8] and in most cases using smart BPDs [9].

This arrangement of all cells in series would also achieve the optimum cell orientation of having all cells in series in a solar panel to get the highest output voltage. It would result in the reduction of losses caused by higher current output when solar cells are connected in the parallel orientation for greater shading tolerability. An investigation using simulations was carried out for quantifying this concept and its methodology is presented in chapter 2 and the results with a validation of the simulation results and an explanation of the differences presented in chapter 4.

1.1.3 Smart Bypass Diodes

A smart bypass diode (smart BPD) operates in the same way as the BPD theory explained previously however it seeks to lower the forward voltage drop across the BPD and thus reduce heating caused by current flowing through this component. The smart BPD that is found to be the best in commercial application and thus used extensively in the literature is the SM74611 Smart Bypass Diode from Texas Instruments and it is available in an integrated package. The smart BPD block diagram is presented in Figure 2 and its functionality is described in its datasheet [10].

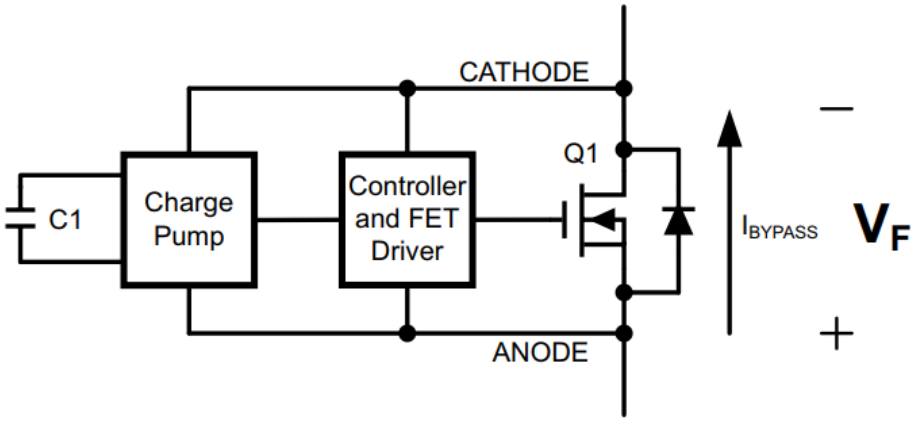


Figure 2: The SM74611 block diagram taken from the data sheet [10].

1.1.4 Active Switching

The use of a single BPD per solar cell has the problem of inability to control when a BPD is turned on or off with conventional BPDs and smart BPDs. This means that the optimum power output cannot be controlled by the user and is thus dependent on the Maximum Power Point Tracker (MPPT) of the inverter. Even if an actively controlled BPD was implemented it was found that the MPPT would ensure that any benefit of this system would be negated. This discovery will be expanded on in a later section through simulations.

Thus a new system for optimisation of electrical output power on a cell level is required. Using matrix converter theory [11] a system can be created and through careful control of this matrix converter the power output of the solar panel optimised when shading occurs.

1.2. Shading and its Effects on Solar Cell Power Output

Shading is a major problem for both small and large scale PV systems. In small scale applications such as residential PV installations shading is caused by obstacles such as trees, chimneys and from adjacent panels [12, 13] and these can have a considerable effect on the electrical power output of the system. Shading can have several effects on the performance of a solar cell:

1) The power obtained from a solar cell is less than the rated power and this increases the loss of load probability (LLP) [12].

2) The creation of local hot spots in the shaded area of the PV panel can reduce the operational life time of the solar cells [13].

There are several methods used to overcome shading in the literature and these include:

1) The use of Bypass Diodes (BPD) connected in anti-parallel with the shaded cells for a string of cells or a single BPD per cell to provide a pathway for the panel current to flow. This approach requires the insertion of bypass diodes into the panels. Problems associated with this approach are the increased cost of production and results in power losses when current is routed through the bypass diodes [15].

   An investigation was conducted into what was presently being done in the integration of a single bypass diode per solar cell in PV panels to determine how these methods could be used to improve the shading tolerability of first a solar cell and then the solar panel as a whole. The investigation looked at what was specifically considered in implementing a single BPD per solar cell [6] and the challenges faced with doing this practically.

   It was found that several means were implemented in test cases [12] and through modifying individual solar cells [12] however all of these methodologies lacked the ability to control when the BPD was activated and in some cases would never turn on during operation

of the Maximum Power Point Tracking (MPPT) controller. This was proven through Simulink simulations of the system as presented in the next chapter.

Thus an opportunity exists for how to optimise the output power of the solar cells during the shading condition and how this can be implemented without the use of BPDs.

2) When considering large PV systems there is the possibility of having sections of a module or parts of an array connected to individual Maximum Power Point (MPP) tracking DC-DC converters or micro-inverters (module level power electronics) thus ensuring different sections of the module or array are operating near their MPP [15]. This can result in an increase in the electrical efficiency of the system [16, 17, 18] however they also result in a high number of DC-DC converters in the system which in turn can increase setup costs. In this approach the system can only aim for the highest power point available at the electrical terminals of the panel instead of making the panel increase the power output to its terminals.

3) Another means of ensuring greater shading tolerability for a PV system is the use of changing wiring configurations for the solar cells of a module to always provide an optimum output power. PV modules available commercially are composed of multiple solar cells with fixed wiring configurations, however through changing solar cells in a combination of series and parallel [20] it is possible to improve the shading tolerability of the PV module as a whole.

Research thus far has been focused on changing the wiring configurations of PV modules arranged in PV arrays [21, 22, 23]. The focus of previous research looks at how the circuit topologies can be implemented and the control algorithm for these circuits is investigated [15]. The complexity of the circuit with a high number of sensors and switches is not optimised [15].

The purpose of this thesis is to investigate how an electronic system can be implemented that allows for controllability of the wiring configurations of solar cells and to be able to measure current and voltage to determine the optimum wiring configuration to extract the maximum power from the PV module under different conditions of shading, incident solar radiation and temperature.

1.3. Smart Cell-level Power Managed PV Module

This research opportunity led to the design of an alternate solar cell wiring configuration system and the filing of a patent [24] which captures a general description of the circuit that would later be developed to meet the patent claims.

1.3.1 The Field of the Invention

The present invention is in the field of a cell-level power managed PV-panel, and a means for operating the panel, such as operating a large number of PV-panels for application in a solar farm [24]. A multitude of individual PV cells is present at the front side of the panel that are controlled through a circuit that changes their wiring configurations [24].

1.3.2 Background of the Invention

In the field of energy conversion, PV systems are used and these systems are composed of PV panels that use an arrangement of solar cells to convert solar energy to electricity [24]. When multiple solar cells are placed in series in a string or parallel to get a higher voltage or current, respectively, this can lead to some disadvantages in the system when shading occurs.

Systems are not optimised in terms of energy production, since the use of energy, the availability of energy and consumption patterns in any environment are continuously changing. Integration with other household applications and appliances is still in its infancy and sometimes not available to designers [24]. Thus existing PV systems show large power output losses and significant

quantities of generated power are unusable because of low power at low light conditions, due to sub-optimal performance of cells because of shading and thus affecting the total electrical output power of a PV-module [24]. As mentioned previously, using a micro-inverter for each module cannot increase the maximum power point of the module and only extracts the available maximum power from each PV module.

In large PV systems, shading can cause power losses that are not proportional to the shaded area and where there is shading, hot-spots in shaded PV cells can occur thus contributing to accelerated aging of the PV module. Bypass diodes are being used in commercial PV modules to reduce the effects of hot spots or shading on a PV module. Active bypass systems have been developed recently to reduce the occurrence of these hot spots and to provide higher electrical efficiency. In conventional PV modules this can still result in output power being lost when a small area of the module is shaded on the order of 1/3 of the PV module power [24].

The presented topology therefore relates to an improved cell-level power managed PV-module and a method of operating such a module, which solves the above problems of existing systems by providing better power output results without affecting the functionality of the PV module [24]. The focus of this report is to show how through changing the wiring configurations to avoid the use of BPDs, a greater power can be extracted from the solar cells under shading conditions. In addition to this, a circuit will be designed and implemented to achieve this change in wiring configurations during several shading conditions.

1.4. Motivation for the Thesis

An opportunity thus exists for a system to use a minimum number of switches and sensors to optimise the electrical output power of a solar panel. Each cell could be controlled by switches to create an active switching matrix with the cell wiring configuration changed as the shading conditions change.

Since a matrix converter for the typically 60 cells in a commercially available solar panel could result in the use of 3,600 (60^2) switches. To implement this prototype system, a smaller panel of sixteen cells arranged in a four by four orientation as illustrated in Figure 3 will be investigated further for a proof of concept. This can then be scaled up as desired for commercially available panels. This arrangement would require 256 (16^2) switches but by treating a group of 4 cells as a base unit instead of each cell individually the number of wiring configurations will be limited to three. In this arrangement, 11 switches for the 16 solar cells can be utilised and this method of implementation will be elaborated on in a later section.

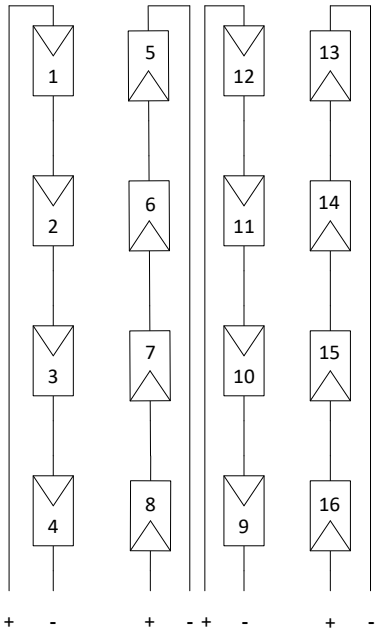


Figure 3: Wiring diagram of the panel with sixteen cells. There are four string consisting of four solar cells in a string.

1.4.1 Research Questions

The thesis investigation seeks to answer the following research questions:

- Can a system be created where through switching between several wiring configurations of solar cells during the case of changing shading conditions, a better electrical power output can be produced?
- Is this system better in terms of optimization of electrical power output than through implementing bypass diodes which may not be activated by the MPPT of the inverter?
- Can this system thus have a greater electrical power output than commercially available solar panels that utilize BPDs?
- Can a new means of solar panel be suggested that uses a minimized topology with the 16 cells and then expanded to the commercially available solar panels that use 60, 72 and 96 solar cells. Thus will this circuit be energy efficient and economically viable?

1.4.2 Scope of the Thesis Project

To answer the research questions an investigation is carried out to determine if having individual BPDs per group of four cells is better than having switches actively controlling the wiring configuration of the group of four solar cells. From this comparison the best solution in terms of power output and energy efficiency of the system is chosen and the better topology built up into a circuit for deployment with the previously mentioned 16 solar cells arranged in a 4×4 solar cell arranged panel.

1.5. Thesis Outline

The thesis report will thus look at simulating several wiring configurations and circuit topologies under several different shading conditions using MATLAB Simulink in Chapter 2 with simulation results presented in Chapter 4, then look at the methodology used to design the optimising circuit in Chapter 3 before implementing the final circuit design on a Printed Circuit Board (PCB). The measurements to validate the simulation models and shade testing of a customised panel first without the optimising circuit and then with it, will be presented and the results discussed in Chapter 4. The arrangement in this chapter is such that simulation and measurement results are presented alongside each other for ease of comparison. The conclusions of the investigation and recommendations for future work are then presented in Chapter 5.

2 Circuit Modelling and Simulations

An introduction into the models and simulations that were looked at in this investigation are presented in this chapter. The chapter is split into two parts, the first deals with the simulations for the 4 x 4 solar panel composed of 16 solar cells with one subsection treating the three wiring configurations of general case m x n where m refers to cells in a string and n the number of strings in parallel thus the three wiring configurations are 16 x 1, 8 x 2 and 4 x 4 cells and the second subsection looks at the simulations of the 16 x 1 wiring configuration with two and then four bypass diodes (BPDs).

For ease of comparison of simulated and measured data (and thus validate the simulation models) all results are presented in chapter 4. However, the parameters used for simulations and the design specifications for the customised panel and the methodology for making the shading measurements on the actual panel are presented in this chapter.

The second part deals with the circuit topologies considered in creating the Single Cell-level Power Management (SCPM) circuit. The models and simulations considered are presented here and the methodology used to make shading measurements for the circuit are described. The results for both simulations and actual measurements are presented in chapter 4 to make it easier for comparison and to validate the simulation models.

2.1. Simulations to Investigate the Performance of the 4 x 4 Panel

The three wiring configurations to be tested are presented. These are with 16 cells in series (16 x 1 configuration) with wiring in Figure 4a, with eight cells in a string in series with two strings in parallel (8 x 2 configuration) with wiring in Figure 4b and with four cells in a string in series and with four strings in parallel (4 x 4 configuration) with wiring in Figure 4c.

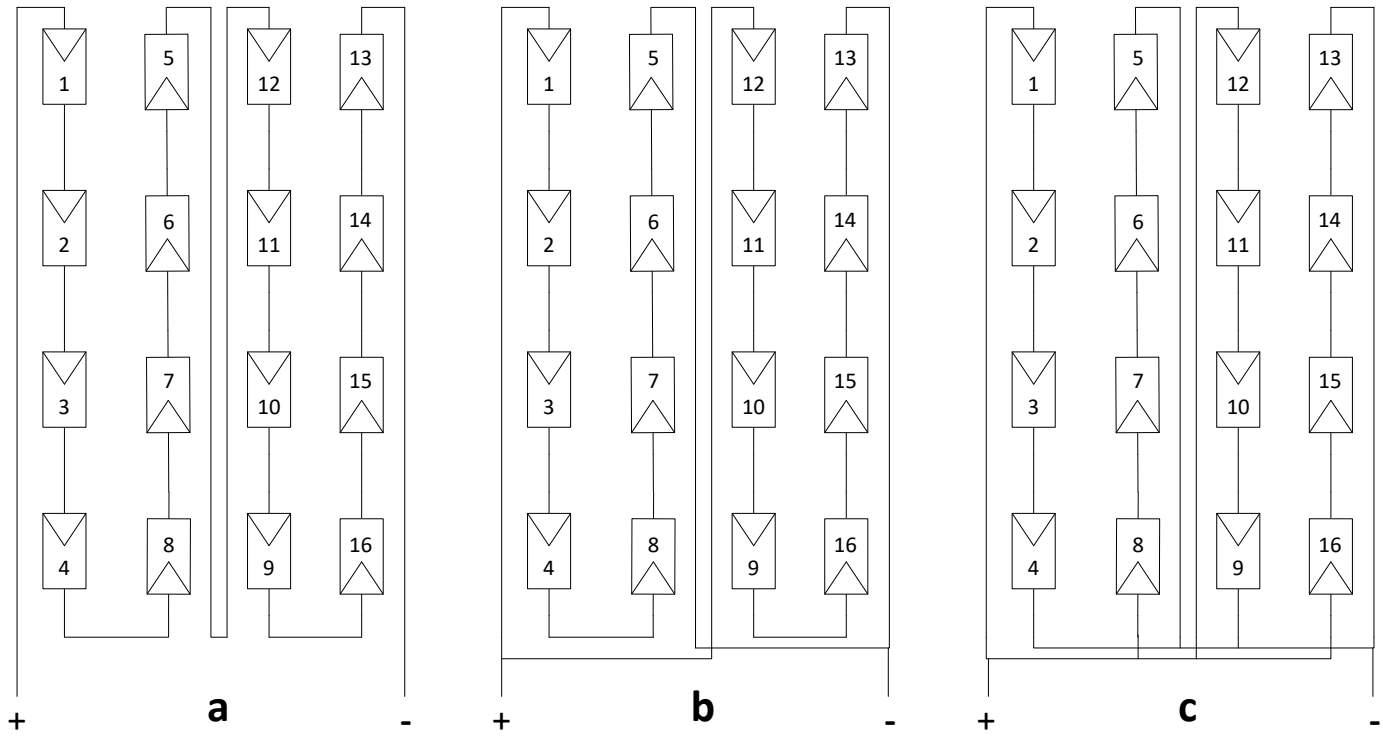


Figure 4: The three different wiring configurations (a) the 16 x 1, (b) the 8 x 2 and (c) the 4 x 4 wiring configuration

These wiring configurations were implemented in MATLAB Simulink using the following component parameters based on the SunPower Maxeon Gen II Interdigitated Back Contact (IBC) cells which are used in the custom panels made and their values presented in Table 1. These component parameters are the basis for all Simulink simulations in this thesis report. The single diode model was used to simulate each solar cell. The following Current vs Voltage (I-V curve) and Power vs Voltage (P-V curve) curves are the base line for all shading comparisons made later in this report.

Table 1: The solar cell parameters used in modelling the solar cells in MATLAB Simulink

Parameter Name	Value	Units
Series Resistance of a Solar Cell, R_s	50	Ω
Shunt Resistance of a Solar Cell, R_{sh}	0.0010	Ω
Short Circuit Current I_{SC}	6.30	A
Saturation Current, I_{sat}	1×10^{-10}	A

The values for the solar cell shown in terms of individual circuit elements in Figure 5.

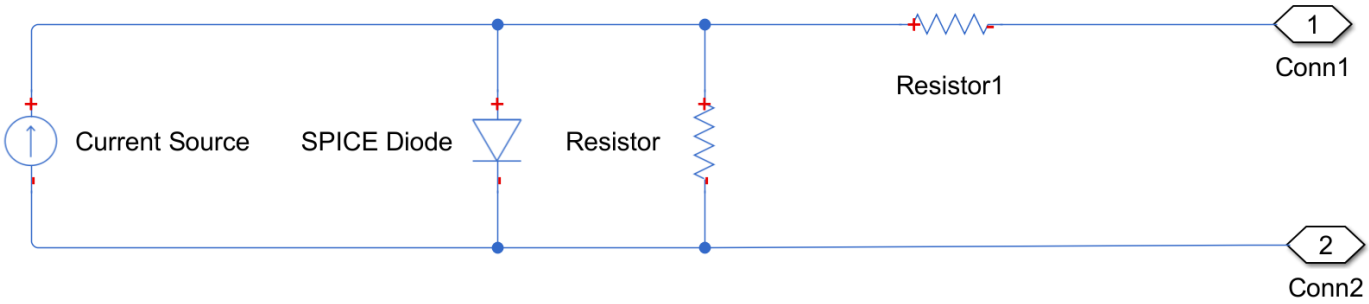


Figure 5: The equivalent circuit of a solar cell with series (Resistor1) and shunt resistance (Resistor) adapted from [5].

The current source from Figure 6 is modelled with the following values where the DC current represents the short circuit current of 6.30 A for the lowest production grade of the SunPower Maxeon Gen II cells.

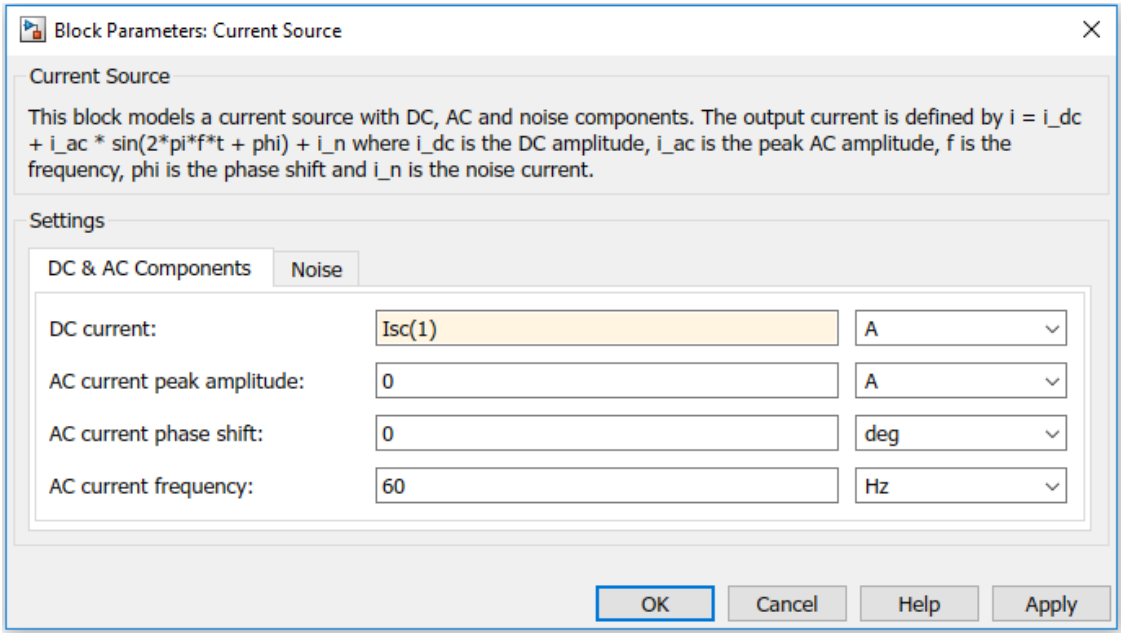


Figure 6: The parameters for the Current Source used in Figure 5.

A SPICE Diode was used for modelling the solar cell with the following parameters shown in Figure 7. This was deemed sufficient for general simulations however further investigation needs to be done to determine a more accurate diode model that can be used in Simulink.

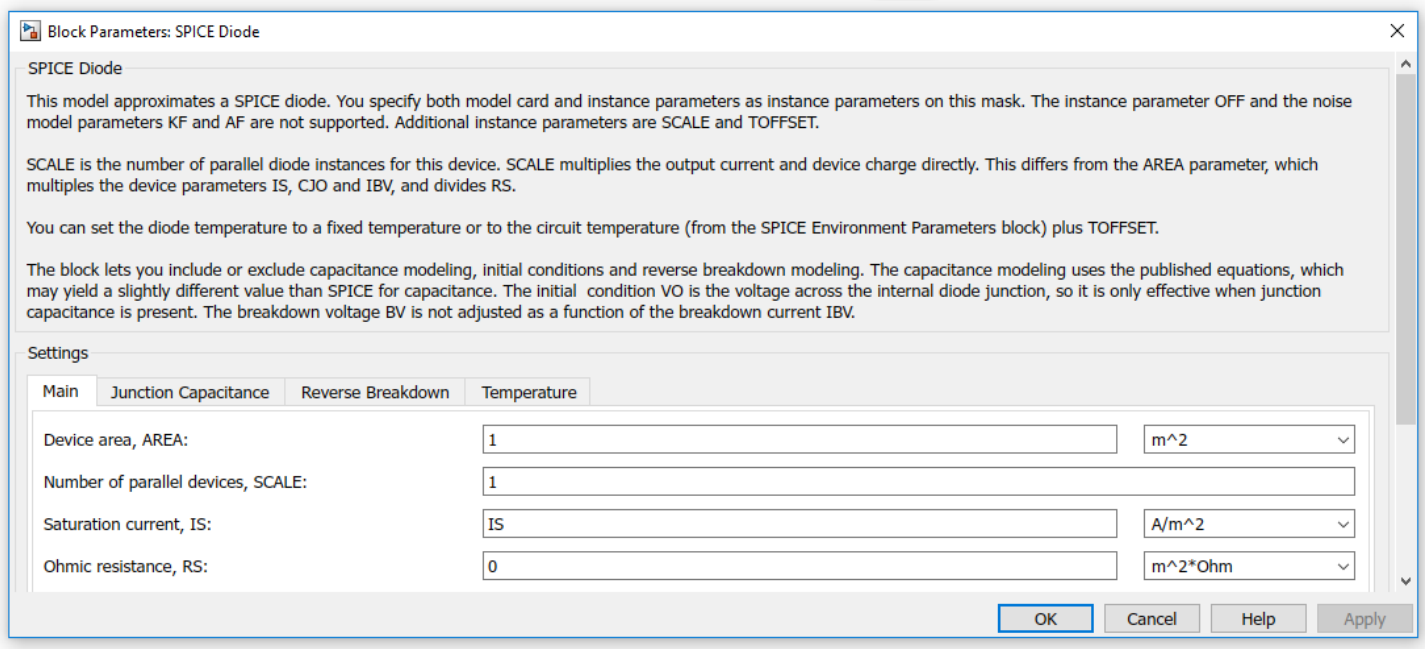


Figure 7: The parameters for the SPICE Diode used in Figure 5.

2.1.1 The 16 x 1 solar cell configuration

The 16 x 1 solar cell wiring configuration was implemented in Simulink and is shown in Figure 8.

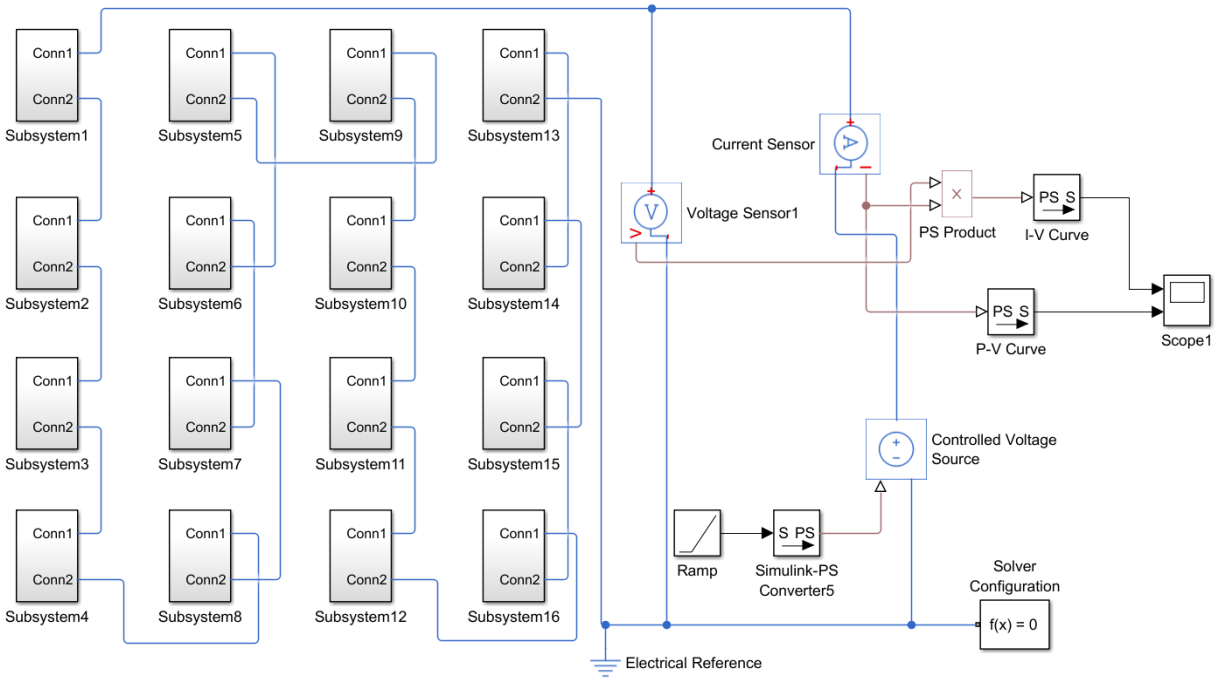


Figure 8: The 16 x 1 wiring configuration in MATLAB Simulink

The I-V curve and the P-V curve of this wiring configuration are presented in section 4.2.

2.1.2 The 8 x 2 solar cell configuration

The 8 x 2 solar cell wiring configuration was implemented in Simulink and is shown in Figure 9.

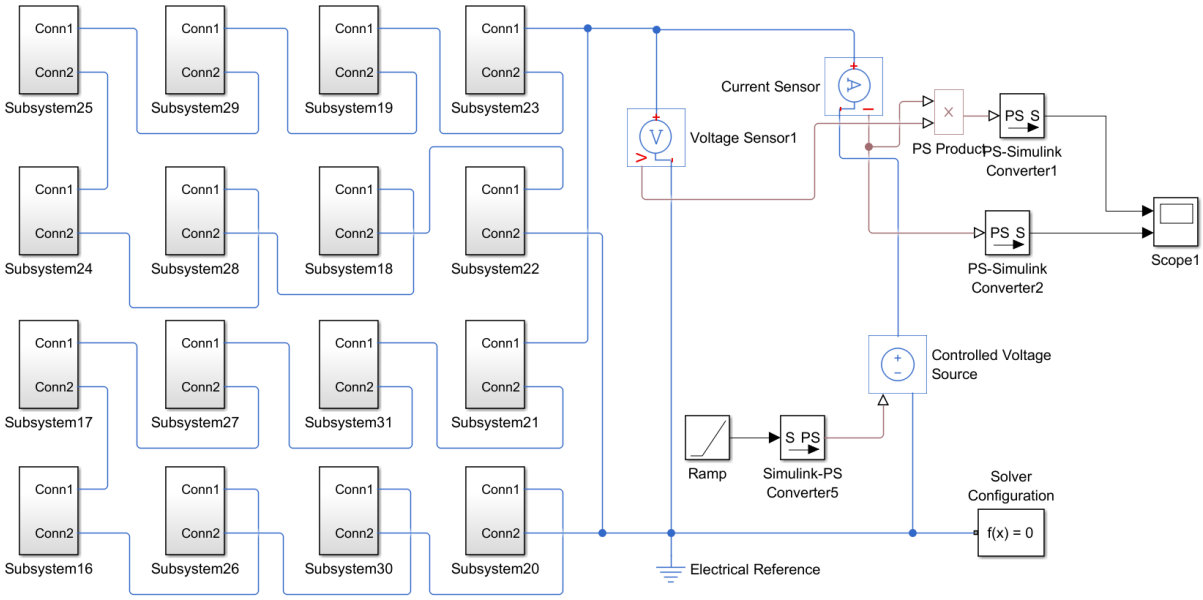


Figure 9: The 8 x 2 wiring configuration in MATLAB Simulink

The I-V curve and the P-V curve of this wiring configuration are presented in section 4.2.

2.1.3 The 4 x 4 solar cell configuration

The 4 x 4 solar cell wiring configuration was implemented in Simulink and is shown in Figure 10.

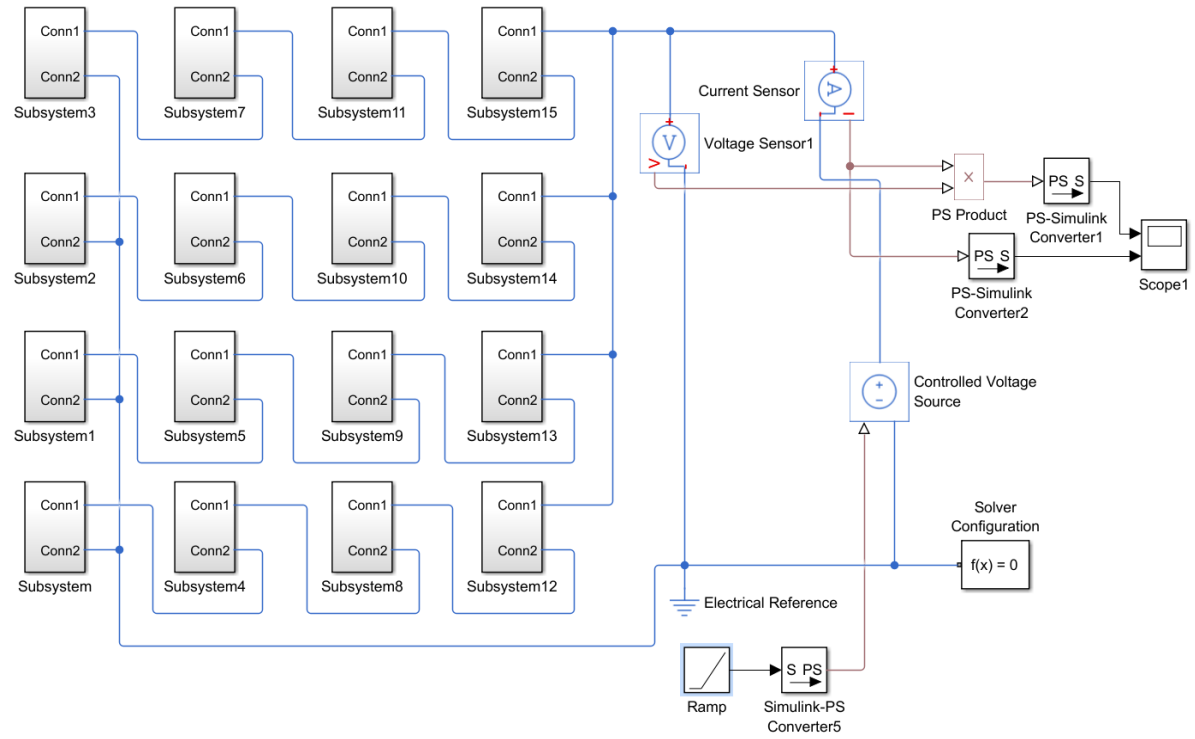


Figure 10: The 4 x 4 wiring configuration in MATLAB Simulink

The I-V curve and the P-V curve of this wiring configuration are presented in section 4.2.

These simulations form the baseline of the three wiring configurations and can be compared with the custom solar panels measurements to validate the solar panel Simulink model. This is done in section 4.2. The baseline will also be used to compare all shading configuration, simulation and measurement results of the panels in these different wiring configurations in chapter 4.

2.2. Shading Configurations Tested

There are several shading configurations that can be tested with the panel of sixteen cells in the three wiring configurations, both with and without the inclusion of bypass diodes. However this investigation has reduced the number to be investigated to a comparison of just six shading configurations. These are presented graphically in chapter 4 of this report with the three varying wiring configurations.

The green squares refer to fully illuminated cells and the red to cells that are shaded through changing the transmission level of the light going through the plastic sheets making up the cell coverings. The six shading configurations will be simulated for each of the three wiring configurations presented in the previous section with the 16 x 1 wiring configuration having two types, with two BPDs (one per eight solar cells in series) and with four BPDs (one per four solar cells in series).

For ease of comparison, the P-V curves will be assessed since the I-V curves change between the three wiring configurations. The most distinct of these P-V curves will be used later on to test the efficiency of the circuit with the panels. Thus a total of 50 tests will be conducted, with the Simulink simulation results and measurement results shown in chapter 4.

The panel presented in Figure 11 was first tested in the three wiring configurations mentioned previously to determine the unshaded I-V and P-V curves of the panel. There are four strings of four solar cells connected in series and these are Cell 1 to 4, Cell 5 to 8, Cell 9 to 12 and Cell 13 to 16. They form the building blocks of the three wiring configurations.

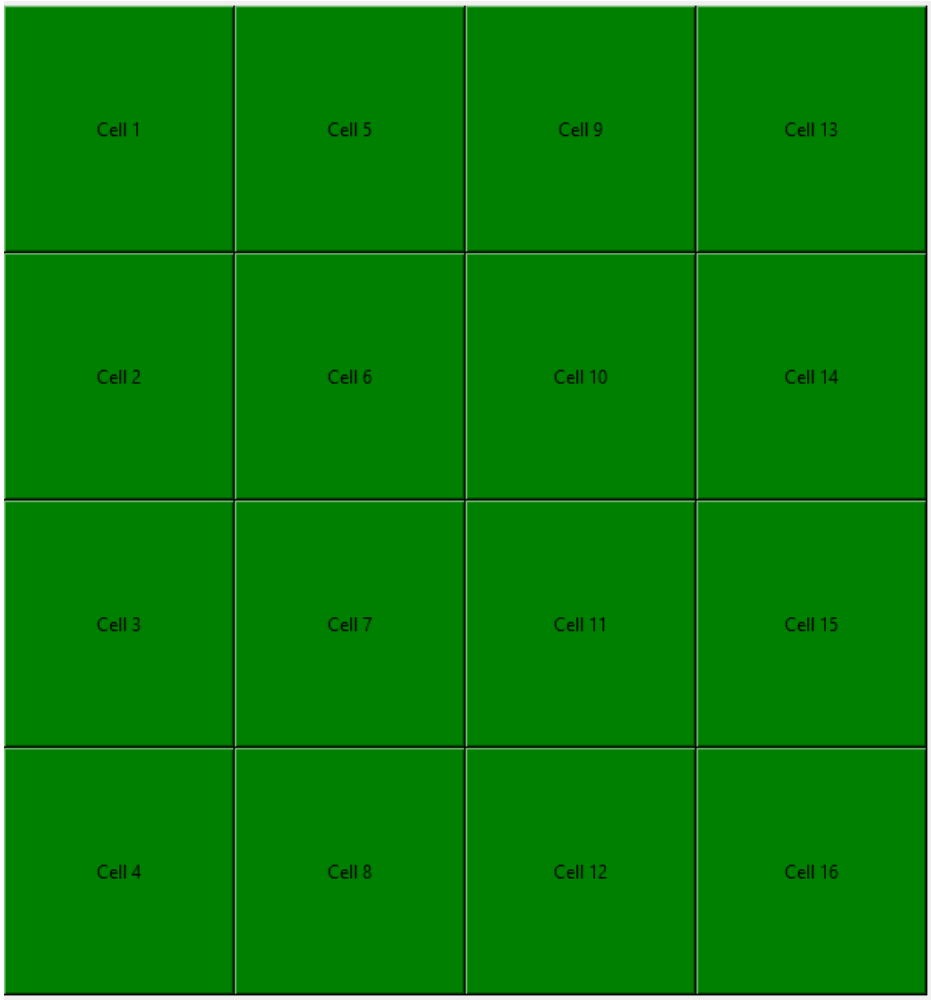


Figure 11: The 16 cell solar panel with solar cells arranged in a 4 x 4 arrangement.

The six shading configurations are presented in chapter 4 to prevent repetition and to aid in the explanation. A commentary is provided on the simulation and actual measurement results and the findings compared in section 4.3.

2.3. Simulations to investigate if Bypass Diodes can be omitted

To compare the performance of solar panels with BPDs to solar panels that did not employ them, several Simulink simulations were carried out with a 16 solar cell based panel with the solar cells having the three different wiring configurations mentioned previously. The Current vs Voltage (I-V) and Power vs Voltage (P-V) curves are compared. The latter are independent of circuit current changes between the three wiring configurations and are thus easier to compare in terms of maximum power points.

2.3.1 The 16 x 1 Solar Cell Wiring Configuration with two BPDs

In this orientation the 16 solar cells in the panel are arranged in series and are simulated using Simulink. The simulation model of the 16 x 1 solar cell wiring configuration with two BPDs in parallel is conducted initially and is presented in Figure 12.

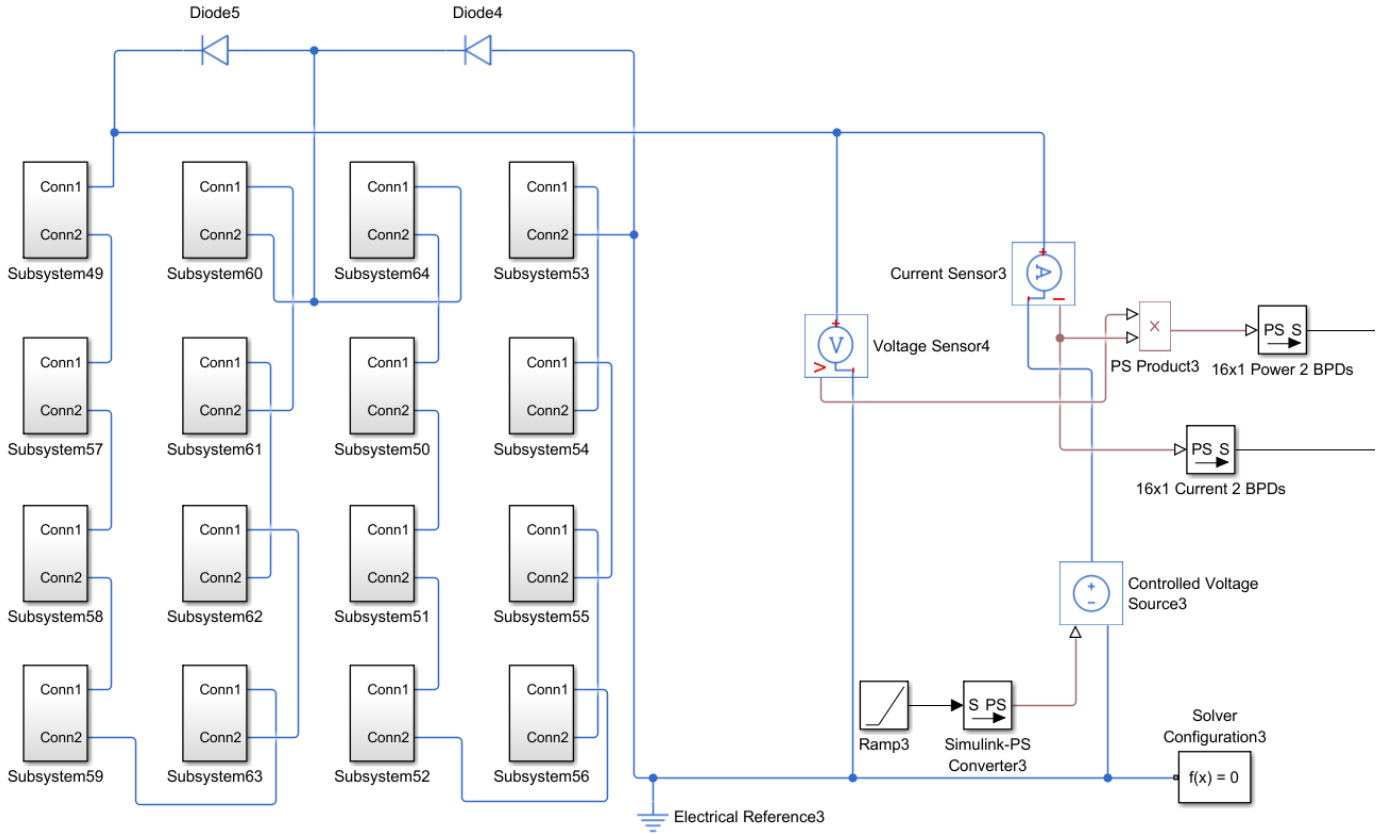


Figure 12: The 16 x 1 wiring configuration with two bypass diodes.

The I-V curve and the P-V curve of this wiring configuration are presented in section 4.2.

2.3.2 The 16 x 1 Solar Cell Wiring Configuration with four BPDs

The second 16 x 1 configuration employs four BPDs, which are placed in parallel with a string consisting of four solar cells in series as shown in the wiring diagram in Figure 13.

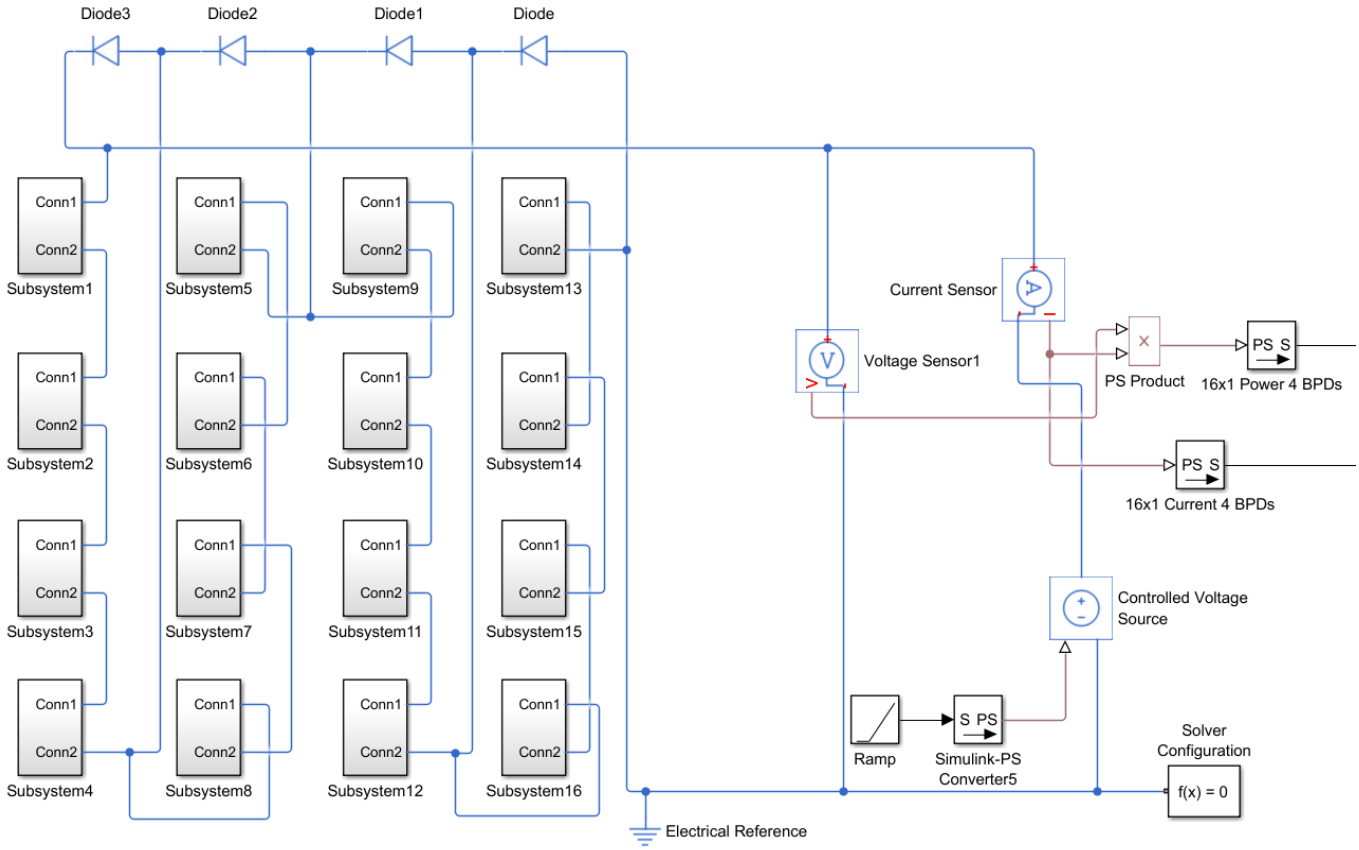


Figure 13: The 16 x 1 wiring configuration with four bypass diodes.

The I-V curve and the P-V curve of this wiring configuration are presented in section 4.2.

2.3.3 The 8 x 2 Solar Cell Wiring Configuration

The 8 x 2 cell wiring orientation uses eight solar cells in a string in series with two strings in parallel and are simulated using Simulink. An illustration of the 8 x 2 solar cell wiring configuration is presented in Figure 14.

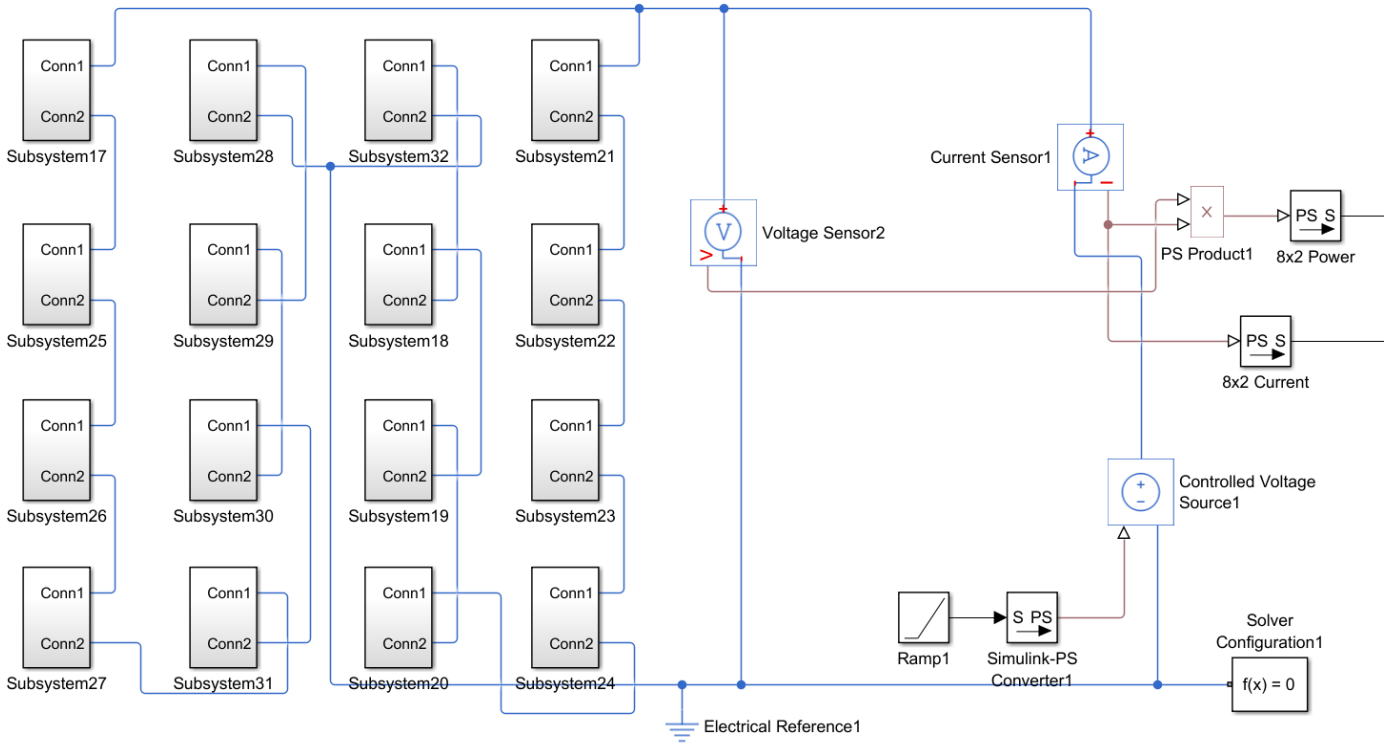


Figure 14: The 8 x 2 wiring configuration.

The I-V curve and the P-V curve of this wiring configuration are presented in section 4.2.

2.3.4 The 4 x 4 Solar Cell Wiring Configuration

In the 4x4 orientation the 16 solar cells in the panel are composed into a string of four solar cells, with four strings in parallel and the Simulink model illustrated in Figure 15. There are no BPDs in this configuration since they would be redundant and instead this is the best case wiring configuration if there is a high degree of shading. Better performance of parallel configuration at shading have been shown experimentally by researchers and mathematically proven [25].

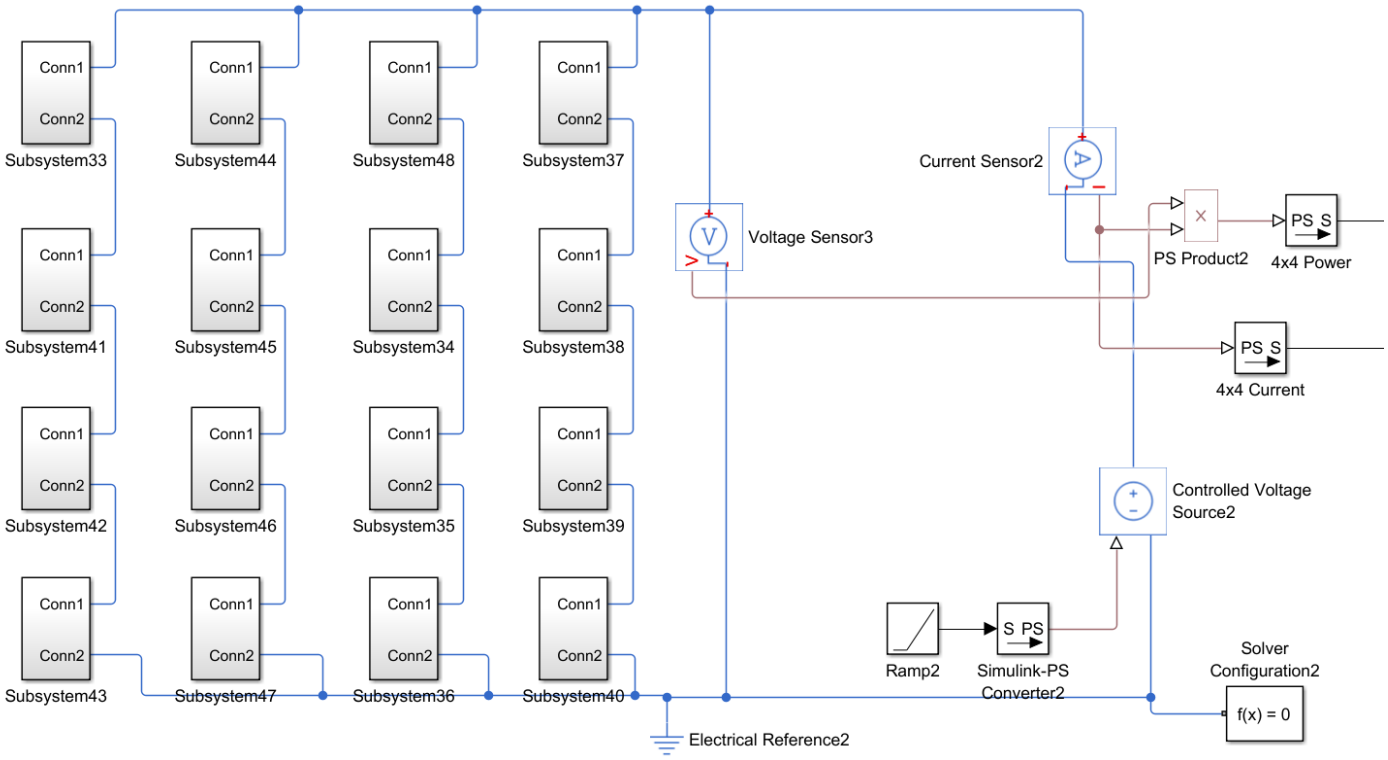


Figure 15: The 4 x 4 wiring configuration.

The I-V curve and the P-V curve of this wiring configuration are presented in section 4.2.

2.4. Method for Quantifying Shading

Shading of the solar cells can be quantified and replicated using plastic sheets of 150 micron thickness of clear polyethylene. The methodology for measuring shading involved taking measurements of 15 of these plastic sheets handled with gloves and cleaned with ethanol and wiped with microfiber cloth to remove all fingerprints and residual dust during the initial handling stage. These plastic sheets were stacked from 0 to 15 in height to take measurements using the AAA-class Large Area Solar Simulator (LASS) produced by EternalSun to emulate Standard Test Conditions (STC) of approx. 1000 $W.m^{-2}$.

A spectrometer was also used as illustrated in Figure 16 and was shaded from surrounding light (albedo and reflected light from the LASS) through the construction of a black box rig that was placed around the spectrometer to ensure no incorrect transmission measurements. On top of the edges of the box, were placed the plastic sheets to decrease the transmittance and hence increase the shading of the light from the LASS being measured by the spectrometer.

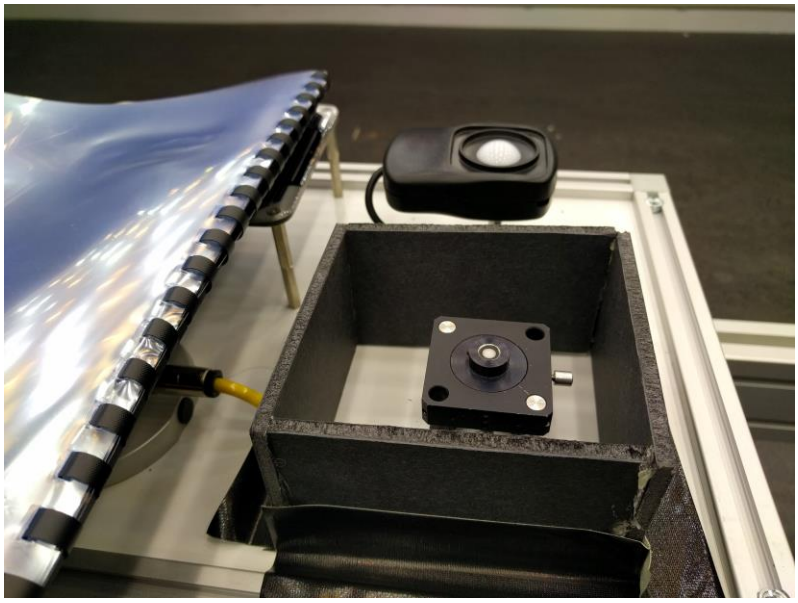


Figure 16: A box rig for reducing error in the spectrometer measurement.

The spectrometer measured the absorbance of light in the range of 297 nm to 1050 nm. Thus the effect of increasing the number of plastic sheets and its effect on the light spectrum of the LASS was determined and it was found that the effect of the plastic on the spectrum of light was negligible. The graphs of absorbance that show the effect on absorbance with increased shading is presented in Figure 17 with the top most line “Transmission Test 0” showing the baseline where there is no shading. A selection of the remaining 15 measurements for transmission corresponding to the 15 plastic sheets that were measured, follow in the graph.

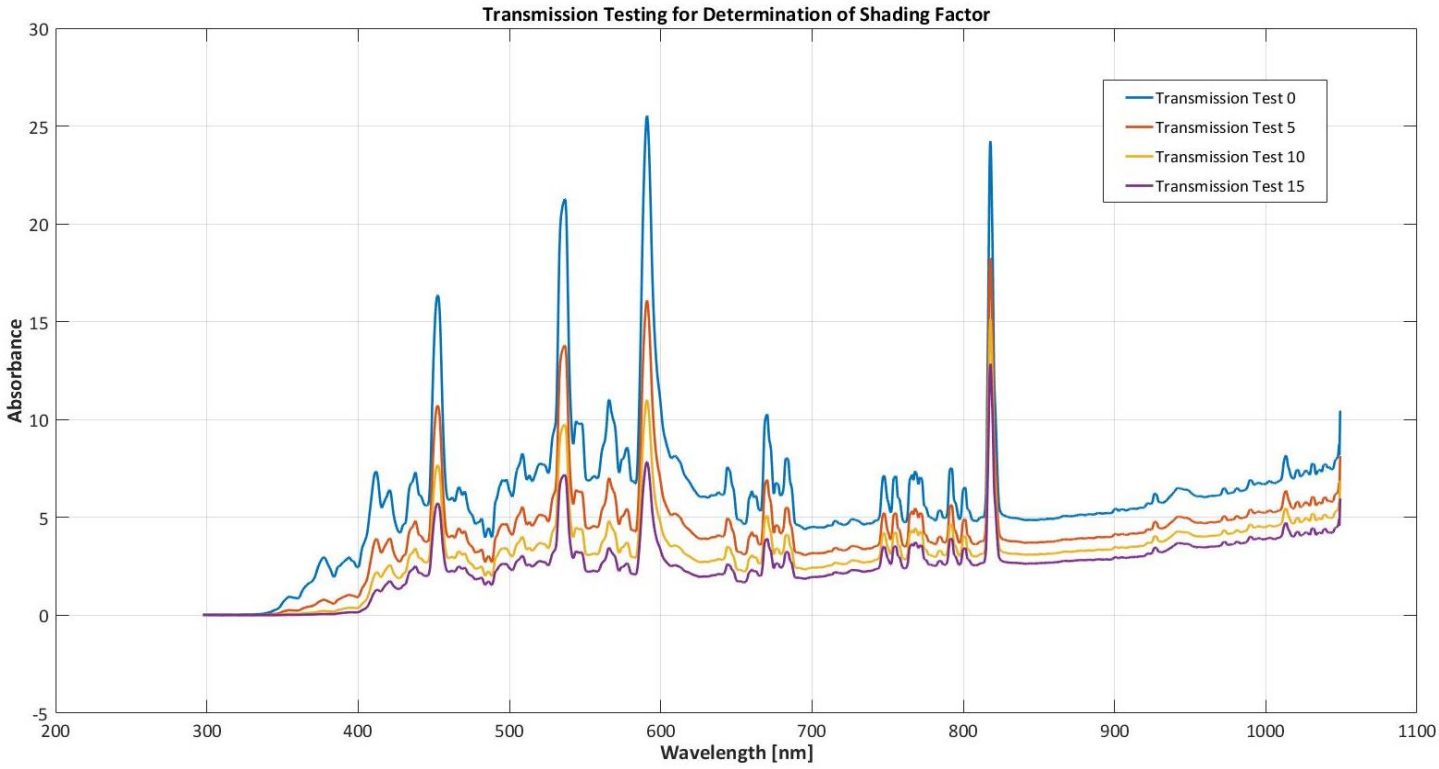


Figure 17: Absorbance of plastic sheets as they are increased from 0 to 15 to measure transmission.

The spectrometer was placed in a fixed location under the LASS as illustrated in Figure 18 and the spectrometer measurements logged on a laptop. There were 15 plastic sheets flipped over individually in the booklet to take 16 measurements in the previously displayed light spectrum.

Figure 18: With the plastic screens for shading testing under the LASS.

All 15 plastic sheets were bound to make it easier to increase the stacking of the sheets and great care was taken that the stacked plastic sheets did not bend and formed a seal for light on the top of the black box to ensure no reflected light affected the spectrometer measurements. A close-up of the above setup with the last measurement of the 15th plastic sheet is presented in Figure 19.

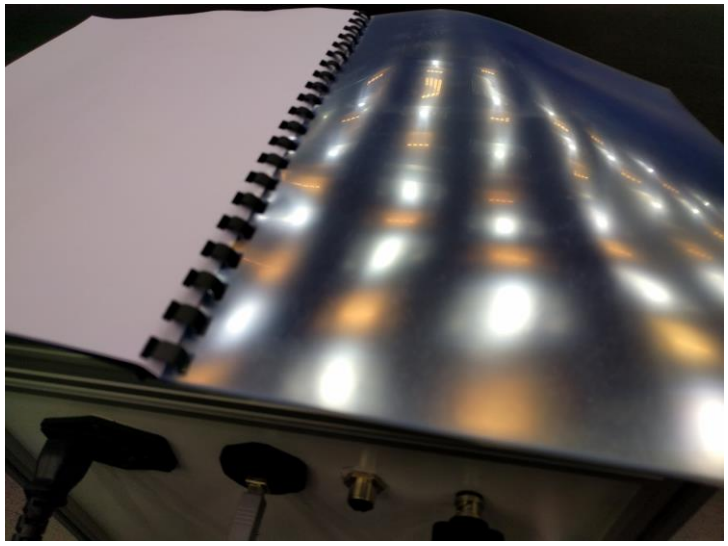


Figure 19: Top view of the testing of the last of the 15 screens under the LASS.

The absorbtion data was collated and from analysing this data the four measurements of interest are summarised below. The red panels indicating shading in the figures in chapter 4 are thus varied with shading fraction of 0.45 and 0.55 corresponding to 10 sheets and 15 sheets, respectively, layered on top of each other. The results of these measurements are presented in Table 2.

Table 2: Transmission Data in terms of the number of plastic sheets utilized to quantify shading.

Material Sheet Nos.	Transmission (%)	Transmission Fraction	Shading Fraction
2	85.0	0.85	0.15
5	70.4	0.70	0.30
10	55.4	0.55	0.45
15	45.3	0.45	0.55

2.5. Specifications for a New Circuit to Improve Shading Tolerability

The circuit designed would need to have switches with low 'ON' resistances and be able to have the ability to pass currents of 10 A (= 1.25^2 x I_{sc}, I_{sc} = 6.11 A) [27] and be able to function with low voltages which are multiples of the V_{oc} (= 0.611 V).

The switches would turn on and off at low frequencies thus switching losses would not be a concern but the conduction losses would be of greater concern. The switches that could best implement these requirements are the use of MOSFETs since the other switch types, BJTs (have higher conduction losses than MOSFETs) and IGBTs/IGCTs (have higher costs and complexity to implement). Relays (both mechanical and solid state) were an option considered however quickly discarded since they have a low operation lifetime for mechanical relays (100,000 times switching and would have to be replaced in situ which is a problem) and their cost for the right voltage and current ratings was prohibitive for solid state relays.

Thus the two types of MOSFETs, n-type and p-type would be compared and based on the type with the lowest $R_{ds,On}$ values (for the current rating), their low threshold voltages (to be driven either directly or with a driver from a 3.3 V Microprocessor (MPU) signal) and their current carrying capabilities (and ability to dissipate the power from $R_{ds,On}$), a choice made for the switch to be used. It was found that using surface mount packages would best meet these requirements and so adequate precautions were taken to dissipate the power produced. This will be elaborated on in chapter 3 when the circuit layout is discussed in detail.

The MOSFETs chosen and their respective properties are presented in Table 3 for N-FETs and Table 4 for P-FETs. The parameter names used and their values are also what was used in the Simulink simulation model elaborated on in the next section.

Table 3: The N-FET Parameters for the switches in Simulink.

N-FET Parameters		
Description	Parameter in Simulink	Unit
The Drain-Source ON Resistance ($R_{DS,On}$)	R_DSN = 0.012;	Ω
Drain Current for the $R_{DS,On}$ (I_D)	IR_DSN = 6;	A
Gate-Source Votage (V_{GS})	Vgs_R_DSN = 15;	V
Threshold Voltage (V_{th})	Vth_N = 3;	V

Table 4: The P-FET Parameters for the switches in Simulink.

P-FET Parameters		
Description	Parameter in Simulink	Unit
The Drain-Source ON Resistance ($R_{DS,On}$)	R_DSP = 0.012;	Ω
Drain Current for the $R_{DS,On}$ (I_D)	IR_DSP = -6;	A
Gate-Source Votage (V_{GS})	Vgs_R_DSP = -15;	V
Threshold Voltage (V_{th})	Vth_P = -2.5;	V

2.6. Determination of the Circuit to Implement the New System

Matrix converter theory was used to determine the optimum number of switches to use and from the 16 solar cells in the panel the optimum number of switches found was 256 [11]. On further optimisation and by reducing the number of wiring configurations to three it was found that only 11 switches needed to be used. The orientation of the switches to implement these wiring configurations is found in Figure 20. This forms the basis for the power circuit and the selection of the switch orientation will be elaborated on through the use of the following tables.

An Excel spreadsheet was created to determine the mode of operation of the MOSFETs based on their applied drain, source and gate voltages in their specific orientations and this is presented in Table 5 for N-FETs and Table 6 for P-FETs in the 16 x 1 configuration.

The means of interpreting these tables is to look at the N-FET table and to determine which modes of operation are possible. Since all switches can operate in triode mode when ON it means that switches 1, 3, 6, 9 and 11 which are ON in the 16 x 1 configuration can all be N-FETs.

Table 5: Evaluation of N-FET switches in the 16 x 1 wiring configuration.

	Volts				ON/OFF Test		
	ON	**N-FET**	**OFF**	**Parameters**	**ON**	**OFF**	**Mode**
Switch 1	0	**Vd**	0				
	0.15	**Vs**	0.15				
	15	**Vg**	0	Vgs > Vth	1	0	
	-0.15	**Vds**	-0.15	Vds > Vgs - Vth	0	1	**Triode**
	14.85	**Vgs**	-0.15	Vds < Vgs - Vth	1	0	
Switch 3	2.25	**Vd**	2.25				
	2.1	**Vs**	2.1				
	15	**Vg**	0	Vgs > Vth	1	0	
	0.15	**Vds**	0.15	Vds > Vgs - Vth	0	1	**Triode**
	12.9	**Vgs**	-2.1	Vds < Vgs - Vth	1	0	
Switch 6	4.5	**Vd**	4.5				
	4.35	**Vs**	4.35				
	15	**Vg**	0	Vgs > Vth	1	0	
	0.15	**Vds**	0.15	Vds > Vgs - Vth	0	1	**Triode**
	10.65	**Vgs**	-4.35	Vds < Vgs - Vth	1	0	
Switch 9	6.75	**Vd**	6.75				
	6.6	**Vs**	6.6				
	15	**Vg**	0	Vgs > Vth	1	0	
	0.15	**Vds**	0.15	Vds > Vgs - Vth	0	1	**Triode**
	8.4	**Vgs**	-6.6	Vds < Vgs - Vth	1	0	
Switch 11	9	**Vd**	9				
	8.85	**Vs**	8.85				
	15	**Vg**	0	Vgs > Vth	1	0	
	0.15	**Vds**	0.15	Vds > Vgs - Vth	0	1	**Triode**
	6.15	**Vgs**	-8.85	Vds < Vgs - Vth	1	0	

In Table 6 and utilising the five switches that compose this wiring configuration, it can be clearly seen that switch 1 is neither saturation nor triode when ON and thus P-FETs can only be selected for switches 3, 6, 9 and 11.

Table 6: Evaluation of P-FET switches in the 16 x 1 wiring configuration.

	Volts				ON/OFF Test		
	ON	**P-FET**	**OFF**	**Parameters**	**ON**	**OFF**	**Mode**
Switch 1	0	**Vs**	0				
	0.15	**Vd**	0.15				
	15	**Vg**	0	Vgs < Vth	0	0	
	0.15	**Vds**	0.15	Vds < Vgs - Vth	1	1	**Neither Mode**
	15	**Vgs**	0	Vds > Vgs - Vth	0	0	
Switch 3	2.25	**Vs**	2.25				
	2.1	**Vd**	2.1				
	15	**Vg**	0	Vgs < Vth	0	1	
	-0.15	**Vds**	-0.15	Vds < Vgs - Vth	1	0	**Triode**
	12.75	**Vgs**	-2.25	Vds > Vgs - Vth	0	1	
Switch 6	4.5	**Vs**	4.5				
	4.35	**Vd**	4.35				
	15	**Vg**	0	Vgs < Vth	0	1	
	-0.15	**Vds**	-0.15	Vds < Vgs - Vth	1	0	**Triode**
	10.5	**Vgs**	-4.5	Vds > Vgs - Vth	0	1	
Switch 9	6.75	**Vs**	6.75				
	6.6	**Vd**	6.6				
	15	**Vg**	0	Vgs < Vth	0	1	
	-0.15	**Vds**	-0.15	Vds < Vgs - Vth	1	0	**Triode**
	8.25	**Vgs**	-6.75	Vds > Vgs - Vth	0	1	
Switch 11	9	**Vd**	9				
	8.85	**Vs**	8.85				
	15	**Vg**	0	Vgs < Vth	0	1	
	0.15	**Vds**	0.15	Vds < Vgs - Vth	1	0	**Triode**
	6.15	**Vgs**	-8.85	Vds > Vgs - Vth	0	1	

The switches employed in the 8 x 2 wiring configuration are shown in Table 7 for N-FETs and Table 8 for P-FETs. Again it can be seen that all N-FETs are capable of operating in this configuration and do so in the triode mode.

Table 7: Evaluation of N-FET switches in the 8 x 2 wiring configuration.

	Volts				Saturation Test		
	ON	**N-FET**	**OFF**	**Parameters**	**ON**	**OFF**	**Mode**
Switch 1	0	Vd	0				
	0.15	Vs	0.15				
	15	Vg	0	Vgs > Vth	1	0	
	-0.15	Vds	-0.15	Vds > Vgs - Vth	0	1	**Triode**
	14.85	Vgs	-0.15	Vds < Vgs - Vth	1	0	
Switch 3	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs > Vth	1	0	
	0.15	Vds	0.15	Vds > Vgs - Vth	0	1	**Triode**
	12.9	Vgs	-2.1	Vds < Vgs - Vth	1	0	
Switch 5	4.5	Vd	4.5				
	4.35	Vs	4.35				
	15	Vg	0	Vgs > Vth	1	0	
	0.15	Vds	0.15	Vds > Vgs - Vth	0	1	**Triode**
	10.65	Vgs	-4.35	Vds < Vgs - Vth	1	0	
Switch 7	0	Vd	0				
	0.15	Vs	0.15				
	15	Vg	0	Vgs > Vth	1	0	
	-0.15	Vds	-0.15	Vds > Vgs - Vth	0	1	**Triode**
	14.85	Vgs	-0.15	Vds < Vgs - Vth	1	0	
Switch 9	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs > Vth	1	0	
	0.15	Vds	0.15	Vds > Vgs - Vth	0	1	**Triode**
	12.9	Vgs	-2.1	Vds < Vgs - Vth	1	0	
Switch 11	4.5	Vd	4.5				
	4.35	Vs	4.35				
	15	Vg	0	Vgs > Vth	1	0	
	0.15	Vds	0.15	Vds > Vgs - Vth	0	1	**Triode**
	10.65	Vgs	-4.35	Vds < Vgs - Vth	1	0	

In Table 8, switches 1 and 7 cannot operate in either mode and thus only switches 3, 5, 9 and 10 can be P-FETs.

Table 8: Evaluation of P-FET switches in the 8 x 2 wiring configuration.

	Volts			Saturation Test			
	ON	**P-FET**	**OFF**	**Parameters**	**ON**	**OFF**	**Mode**
Switch 1	0	Vs	0				
	0.15	Vd	0.15				
	15	Vg	0	Vgs < Vth	0	0	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	1	**Neither Mode**
	15	Vgs	0	Vds > Vgs - Vth	0	0	
Switch 3	2.25	Vs	2.25				
	2.1	Vd	2.1				
	15	Vg	0	Vgs < Vth	0	1	
	-0.15	Vds	-0.15	Vds < Vgs - Vth	1	0	**Triode**
	12.75	Vgs	-2.25	Vds > Vgs - Vth	0	1	
Switch 5	4.5	Vd	4.5				
	4.35	Vs	4.35				
	15	Vg	0	Vgs < Vth	0	1	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	0	**Triode**
	10.5	Vgs	-4.35	Vds > Vgs - Vth	0	1	
Switch 7	0	Vs	0				
	0.15	Vd	0.15				
	15	Vg	0	Vgs < Vth	0	0	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	1	**Neither Mode**
	15	Vgs	0	Vds > Vgs - Vth	0	0	
Switch 9	2.25	Vs	2.25				
	2.1	Vd	2.1				
	15	Vg	0	Vgs < Vth	0	1	
	-0.15	Vds	-0.15	Vds < Vgs - Vth	1	0	**Triode**
	12.75	Vgs	-2.25	Vds > Vgs - Vth	0	1	
Switch 11	4.5	Vd	4.5				
	4.35	Vs	4.35				
	15	Vg	0	Vgs < Vth	0	1	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	0	**Triode**
	10.65	Vgs	-4.35	Vds > Vgs - Vth	0	1	

The modes of operation for N-FETs and P-FETs in the 4 x 4 configuration are presented in Table 9 and Table 10, respectively. It was found that all switches used in this configuration (switches 1, 2, 4, 5, 7, 8, 10 and 11) can be N-FETs however all the low-side switches would have to be N-FETs since P-FETs would have no modes of operation if employed as switches for 1, 4, 7 and 11.

Table 9: Evaluation of N-FET switches in the 4 x 4 wiring configuration.

	Volts				Saturation Test		
	ON	**N-FET**	**OFF**	**Parameters**	**ON**	**OFF**	**Mode**
Switch 1	0	Vd	0				
	0.15	Vs	0.15				
	15	Vg	0	Vgs > Vth	1	0	
	-0.15	Vds	-0.15	Vds > Vgs - Vth	0	1	**Triode**
	14.85	Vgs	-0.15	Vds < Vgs - Vth	1	0	
Switch 2	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs > Vth	1	0	
	0.15	Vds	0.15	Vds > Vgs - Vth	0	1	**Triode**
	12.9	Vgs	-2.1	Vds < Vgs - Vth	1	0	
Switch 4	0	Vd	0				
	0.15	Vs	0.15				
	15	Vg	0	Vgs > Vth	1	0	
	-0.15	Vds	-0.15	Vds > Vgs - Vth	0	1	**Triode**
	14.85	Vgs	-0.15	Vds < Vgs - Vth	1	0	
Switch 5	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs > Vth	1	0	
	0.15	Vds	0.15	Vds > Vgs - Vth	0	1	**Triode**
	12.9	Vgs	-2.1	Vds < Vgs - Vth	1	0	
Switch 7	0	Vd	0				
	0.15	Vs	0.15				
	15	Vg	0	Vgs > Vth	1	0	
	-0.15	Vds	-0.15	Vds > Vgs - Vth	0	1	**Triode**
	14.85	Vgs	-0.15	Vds < Vgs - Vth	1	0	
Switch 8	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs > Vth	1	0	
	0.15	Vds	0.15	Vds > Vgs - Vth	0	1	**Triode**
	12.9	Vgs	-2.1	Vds < Vgs - Vth	1	0	
Switch 10	0	Vd	0				
	0.15	Vs	0.15				
	15	Vg	0	Vgs > Vth	1	0	
	-0.15	Vds	-0.15	Vds > Vgs - Vth	0	1	**Triode**
	14.85	Vgs	-0.15	Vds < Vgs - Vth	1	0	
Switch 11	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs > Vth	1	0	
	0.15	Vds	0.15	Vds > Vgs - Vth	0	1	**Triode**
	12.9	Vgs	-2.1	Vds < Vgs - Vth	1	0	

Table 10: Evaluation of P-FET switches in the 4 x 4 wiring configuration.

	Volts				Saturation Test		
	ON	**P-FET**	**OFF**	**Parameters**	**ON**	**OFF**	**Mode**
Switch 1	0	Vs	0				
	0.15	Vd	0.15				
	15	Vg	0	Vgs < Vth	0	0	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	1	**Neither Mode**
	15	Vgs	0	Vds > Vgs - Vth	0	0	
Switch 2	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs < Vth	0	1	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	0	**Triode**
	12.9	Vgs	-2.1	Vds > Vgs - Vth	0	1	
Switch 4	0	Vs	0				
	0.15	Vd	0.15				
	15	Vg	0	Vgs < Vth	0	0	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	1	**Neither Mode**
	15	Vgs	0	Vds > Vgs - Vth	0	0	
Switch 5	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs < Vth	0	1	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	0	**Triode**
	12.9	Vgs	-2.1	Vds > Vgs - Vth	0	1	
Switch 7	0	Vs	0				
	0.15	Vd	0.15				
	15	Vg	0	Vgs < Vth	0	0	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	1	**Neither Mode**
	15	Vgs	0	Vds > Vgs - Vth	0	0	
Switch 8	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs < Vth	0	1	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	0	**Triode**
	12.9	Vgs	-2.1	Vds > Vgs - Vth	0	1	
Switch 10	0	Vs	0				
	0.15	Vd	0.15				
	15	Vg	0	Vgs < Vth	0	0	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	1	**Neither Mode**
	15	Vgs	0	Vds > Vgs - Vth	0	0	
Switch 11	2.25	Vd	2.25				
	2.1	Vs	2.1				
	15	Vg	0	Vgs < Vth	0	1	
	0.15	Vds	0.15	Vds < Vgs - Vth	1	0	**Triode**
	12.9	Vgs	-2.1	Vds > Vgs - Vth	0	1	

2.7. Simulations to determine the efficacy of the new system

The modes of operation for adequate switching of the MOSFETs is a choice between saturation and triode (or ohmic) modes. The saturation mode of operation is better due to the MOSFET being independent of the drain current and only dependent on the gate voltage [28]. The triode mode of operation is dependent on the drain current and thus can have a higher ON resistance [28] which is not desirable for this application.

Despite several attempts with different N-FET and P-FET MOSFET combinations, it was not possible to get the MOSFETs to operate in saturation mode where the induced channel of the MOSFETs could easily handle drain currents of the magnitude of 10 A. Instead this could be done operating the MOSFETs (whether n-type or p-type) in the triode mode.

The reason that the triode mode was selected was because as seen in both N-FET and P-FET tables, the drain-source voltage was too low. The difference of the gate-source voltage and the threshold voltage either exceeded the drain-source voltage for N-FETs resulting in triode mode or the conversely the drain-source voltage was greater than the gate-source and threshold voltage difference resulting in the triode mode for P-FETs also.

In the end P-FET switches with lower $R_{DS,ON}$ for the desired current of 10 A were found and thus making low-side switches (1, 4, 7 and 11) as N-FETs and the rest in the wiring configuration a P-FET was found to be the most optimum approach.

The final choices of MOSFETs and their orientations are presented in Figure 20. The low side MOSFETs are N-FETs and the rest are P-FETs. On close inspection, the keen electronics engineer will note the inverted orientation of some of the MOSFETs and this is to ensure that the body diodes do not cause a shorting or bypassing of a MOSFET and thus result in improper control of the transition between wiring configurations.

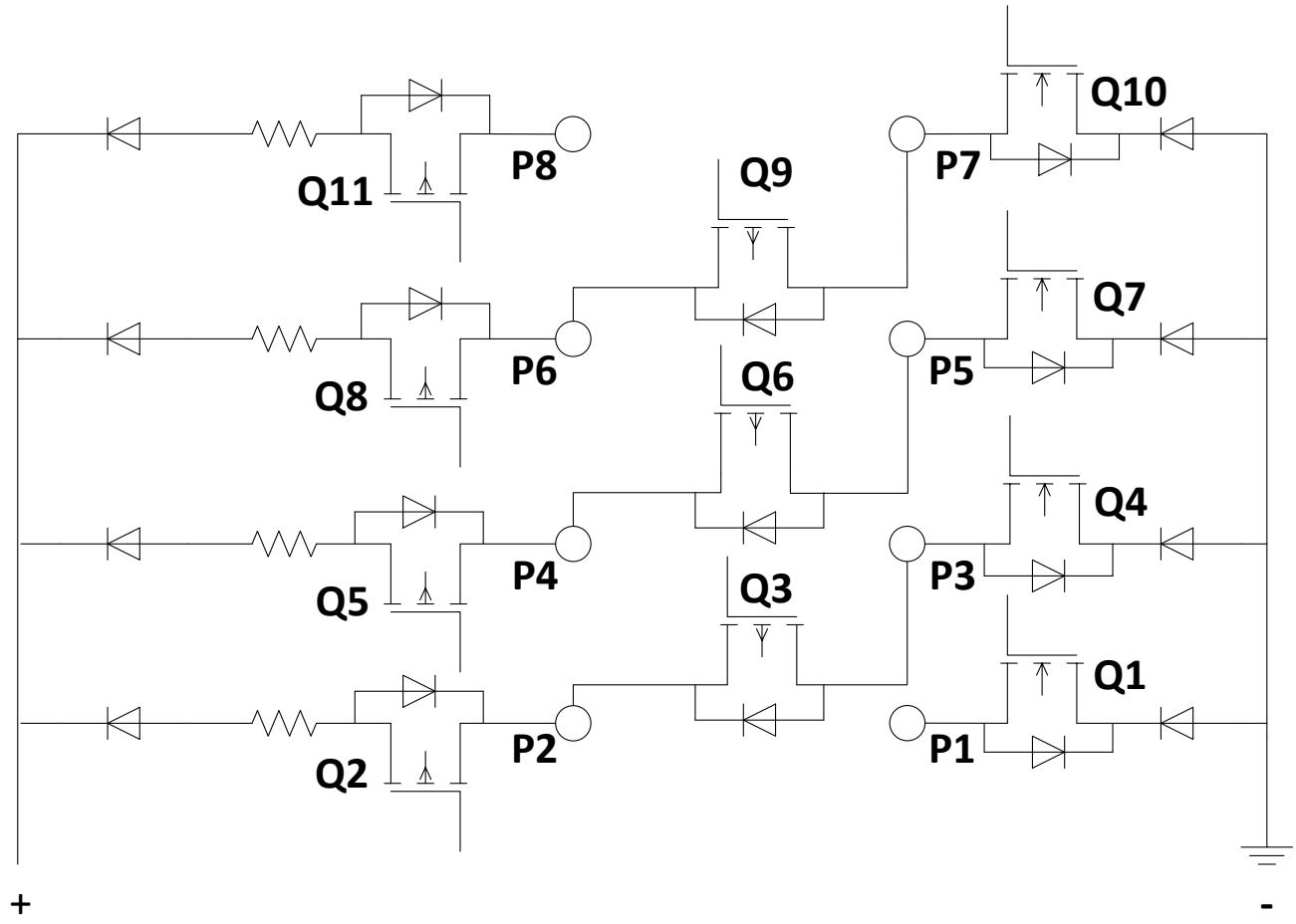


Figure 20: The circuit diagram of the SCPM circuit showing the final orientation of the MOSFETs.

Connected to the terminal pairs P1 and P2, P3 and P4, P5 and P6, P7 and P8 are four solar cells connected in series to form a string with the polarity shown in Figure 21.

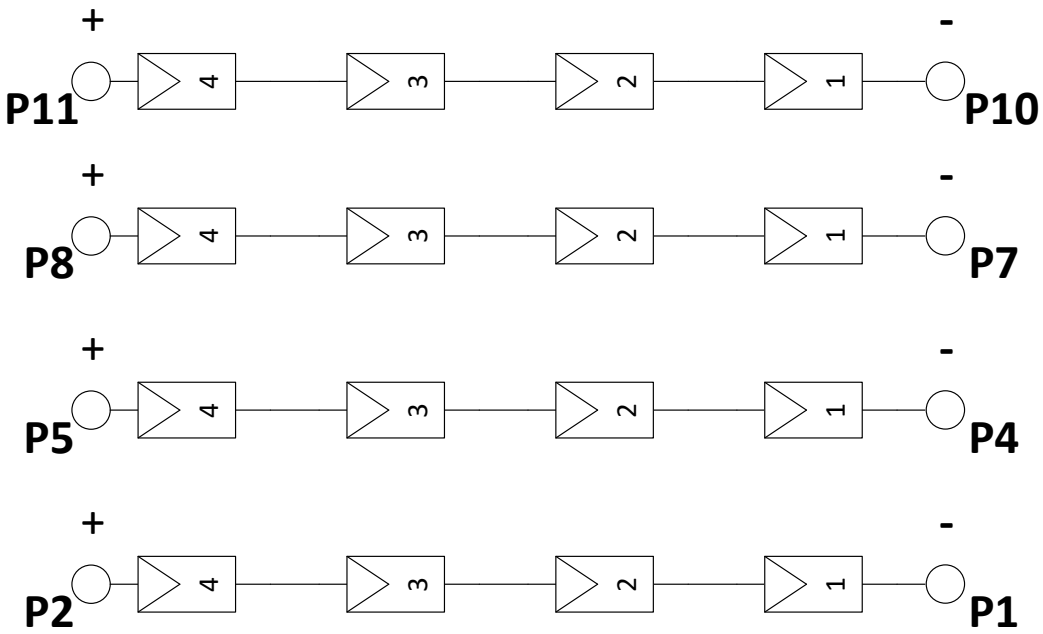


Figure 21: Wiring diagram of the string of four cells to the terminal pairs.

The switches would need drivers so that the induced channels of the MOSFETs could adequately handle the desired currents without causing heating and so a driver circuit that could provide electrical isolation had to be implemented. Thus a power BJT circuit was used to ensure the MPU could drive the input to the DC-DC converter used for electrical isolation and the output of this component supply the ON and OFF signals to the gate drive resistor for the MOSFETs. The design of these circuits are expanded on in chapter 3 and this section will instead focus on the components employed in the Simulink simulation model.

A Simulink model was created of the proposed circuit topology of Figure 20 to determine circuit functionality with the MOSFET orientation chosen. This Simulink model control and thus its ability to switch between the three wiring configurations is carried out using MATLAB code. The I-V and P-V curves of the three wiring configurations with shading were also tested and presented as simulation and measurement results and these will be compared in section 4.2.

2.8. Summary of the Simulations

Thus an adequate electronic circuit solution was found to implement the three different wiring configurations required and it was developed to make a solar panel more shading tolerant from the solar cell level to increase the electrical power output efficiency of the system.

The first stage was the use of different shading configurations and with varying shading factors to determine how power output varies through comparison of the I-V and P-V curves. The use of different wiring configurations helped determine the extent of shading tolerability of the panel. A circuit was designed that would help implement these wiring configurations and realise them using MOSFETs. This circuit was simulated using Simulink and its performance compared with the previous measurements made without the use of the electronic circuit. The Simulink models will be validated in chapter 4 when the results are analysed.

3 The Smart Cell-level Power Managed PV Module

A thorough explanation of the functionality of the circuits that form the Printed Circuit Board (PCB) are presented here which include the power, the control, the sensing and auxiliary circuit schematics. The methodology used to select the specific components and what electrical ratings they have are explained.

The PCB design methodology is described here and the specifications considered in making choices such as track dimensions, positioning of components, thermal and mechanical factors such as cooling of components during operation and the location of spacers and mounting holes are elaborated on.

The functionality of this circuit is then discussed in terms of hardware implementation for the three wiring configurations before proceeding to an explanation of its control using software. A treatment of the control algorithm and the software operation is explained using a flow chart and state diagrams. The different functions, their capabilities and their limitations are elaborated on. The theoretical power consumption of the circuit, its Bill of Materials (BoM) and its cost are also presented in this chapter. The circuits presented in this design stress achieving functionality of the circuit and remain to be optimised in a later revision of the circuit.

3.1. The Power Circuit

The power circuit forms the heart of the electronic circuit since it allows for switching between the three wiring configurations. It is composed of the following sub circuits that are presented as an overview in Figure 22. The circuit orientation was discussed previously in chapter 2 and here its support circuits such as the gate resistor, gate to source resistor for gate capacitance discharge and current sensing resistors and the choice of their values discussed.

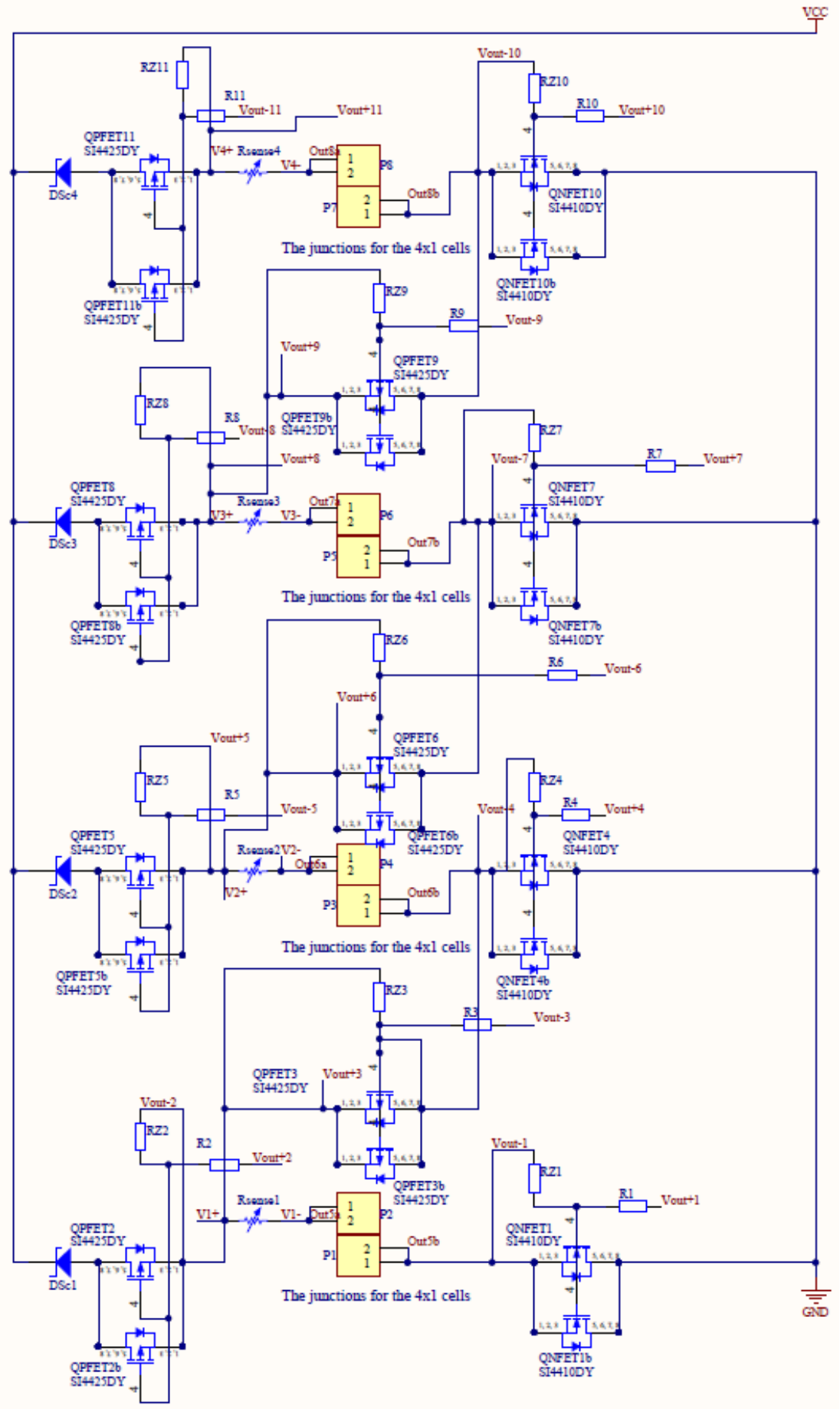


Figure 22: The Schematic Diagram of the Power Circuit showing blocking diodes, the current sense resistors, switches and connections for the strings of four solar cells.

3.1.1 The MOSFET switches composed of both N-FET and P-FET types

A combination of N-FET and P-FET switches are employed for switching between the wiring configurations. There are four N-FETs and seven P-FETs making up the complement of 11 switches of the power circuit.

The orientation of the switches is such that the body diodes do not act as an undesirable conduit of current and thus allow for the switches as the only means of redirecting current. Their orientation though unconventional has thus been carefully thought through before implementation.

The factors used to choose the FET switches for both types are a low $R_{DS,ON}$ (typically 10 mΩ) for the desired drain current of I_D of 10 A. A low gate threshold voltage such that a large channel can be induced with the gate driver voltages employed of 15 V from the DC-DC converter. These values resulted in the selection of two switches, the N-FET

3.1.2 Current Sensing Resistors

The current sensing resistors have a value of 12 mΩ ± 5% and is a cement coated wire wound resistor. Through the use of a current sense amplifier presented in the next section are used to measure currents between 0 and a maximum of 10 A expected solar cell current through the string. The maximum differential voltage produced across the current sensing resistor is thus 120 mV. This signal experiences a gain of 20 V/V that is limited to 2.54 V which is the maximum voltage that can be measured by the ADC connected to the microprocessor by I^2C.

3.1.3 The Electrical Connections for PV Panel Strings

The electrical connections are the means by which the individual strings of the customised PV panel are connected to the PCB and are chosen based on a low series resistance of 1 mΩ based on the datasheet. The goal is to reduce the contribution to the series and shunt resistances of the PV panel with these connections.

3.1.4 The Solar Cell Protection Circuits

The solar cell protection circuit is composed of a high current rated (30A) and low forward voltage rated Schottky diode that acts as a blocking diode to prevent a higher voltage in adjacent strings from causing currents to flow back into strings with lower voltages caused by changes in temperature, irradiance or electric fault.

3.2. The Control and Sensing Circuits

The control and sensing circuits are presented in Figure 23 and are composed of the following sub circuits and are described from left to right in the following subsections.

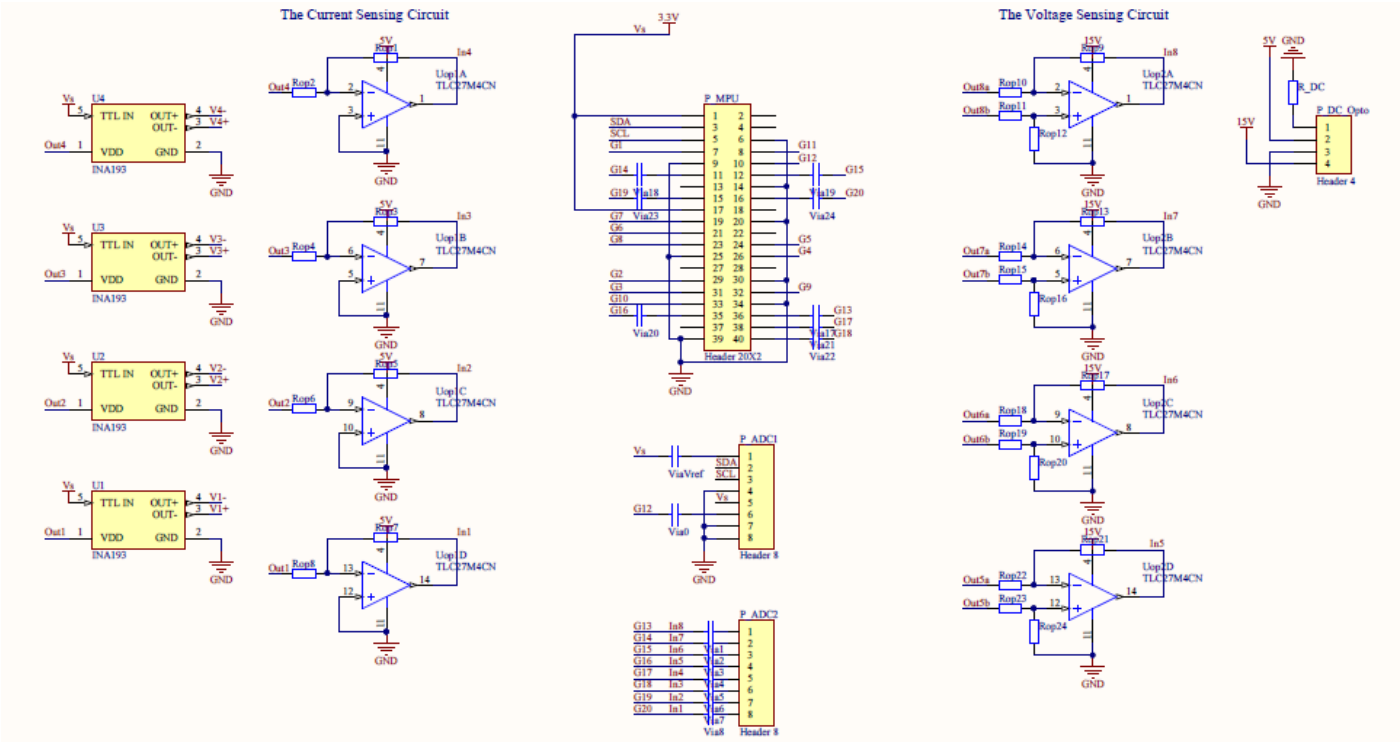


Figure 23: The Control and Sensing Circuits.

3.2.1 The current sense amplifiers

The current sensing differential amplifiers are connected in parallel with the current sense resistors and provide a voltage between 0 and 2.4 V to the ADC for measuring the current. By measuring across the range from 0 to a maximum of 10 A it can be determined when shading occurs since the irradiation is proportional to the current measured. The current sense amplifier is an integrated circuit presented in Figure 24. The power supply of the current sense amplifier is 3.3 V and the output voltage should not exceed the maximum input voltage of the ADC of 2.54 V, when the measured signal would appear saturated.

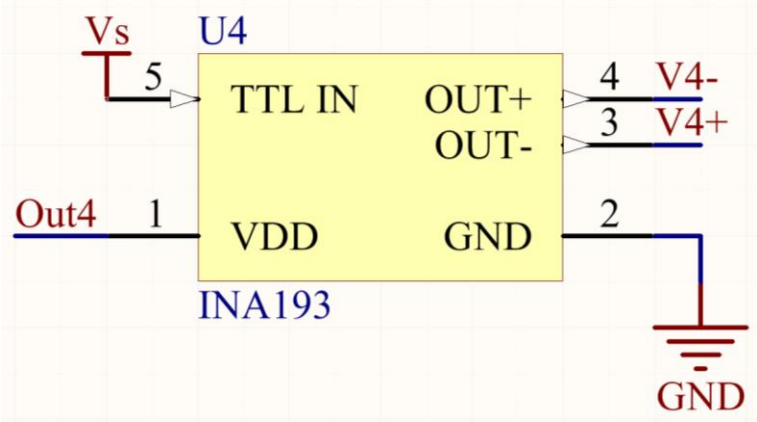


Figure 24: The Current Sense Amplifier.

3.2.2 The current sense amplifier output signal conditioning circuit

The current sensing signal conditioning circuit is an inverting operational amplifier configuration which can be employed with a gain of 1 if the 20 V/V is sufficient for getting signal clarity should irradiance fluctuations not be large. The circuit is shown in Figure 25 and is connected

between the output of the current sense amplifier and the ADC input pin for each of the four strings of the customised solar panel. The power supply of the operational amplifier is 5.0 V.

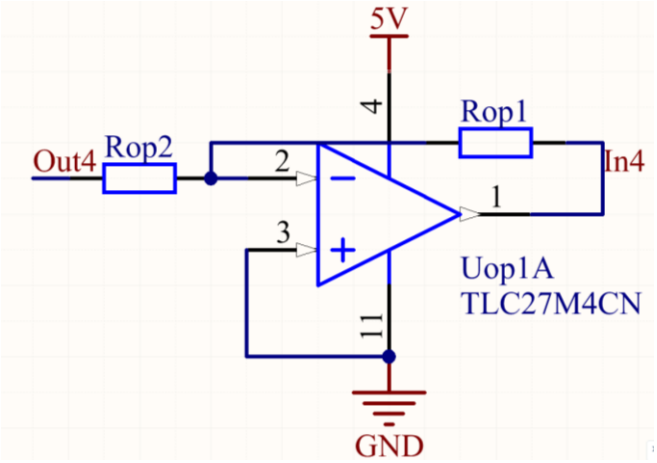


Figure 25: The Current Sense Amplifier Signal Conditioning Circuit.

3.2.3 The Microprocessor development board interface

The Microprocessor Unit (MPU) consisting of a Raspberry Pi W Zero development board interface in Figure 26 is the brains of the operation and is the means by which the power, control, sensing and auxiliary circuits are manipulated. The MPU has 27 General Purpose Input Output (GPIO) pins to control these circuits through an output voltage that varies between 0 – 3.3 V. The MPU was chosen over other MPUs and Microcontroller Units (MCUs) since it has WiFi and Bluetooth LTE communication protocols integrated and allows for an easily designed graphical user interface (GUI) for a low cost.

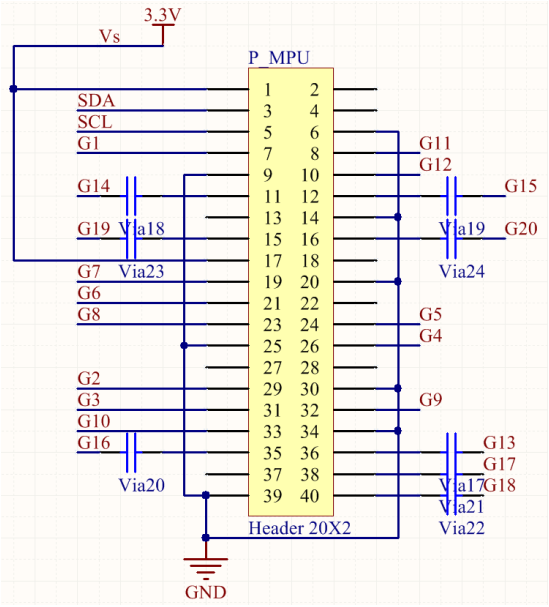


Figure 26: The Microprocessor Unit Connection.

This MPU is also well suited to the task since rapid circuit changes (requiring high clock and switching frequencies) are not required for the proposed circuit functionality. The size and memory storage capabilities are also favourable for this application and thus it was chosen over other development boards and environments. The MPU is positioned in such a way to allow for connection of the mini-USB and mini-HDMI adapters for giving keyboard, mouse and HDMI cable access for programming and viewing the GUI.

3.2.4 The ADC that employs I²C communication

The MPU GPIO pins that only allow for digital input/output (I/O), Inter-Integrated Communication (I^2C), Serial Peripheral Interface (SPI) and USART/UART protocols and thus a means of interpreting the analogue signals measured must be used. The ADC128D18 from Texas Instruments was used since it provides precision measurement of analogue signals in an Analogue-to-Digital (ADC) package that integrates the I^2C protocol.

This allows for ease of communication with the MPU and utilises less pins than the SPI (four pins utilised by the microSD card reader) and UART/USART (two pins but without the ability for having multiple devices or apportioning devices with different addresses) protocols. The I^2C protocol utilises two pins however it has the ability to add up to 8 devices of different I^2C addresses allowing for greater expansibility of the system if a conventional panel were to be controlled by one MPU. The ADC Integrated Circuit (IC) with its breakout board for ease of connection and troubleshooting is presented in Figure 27.

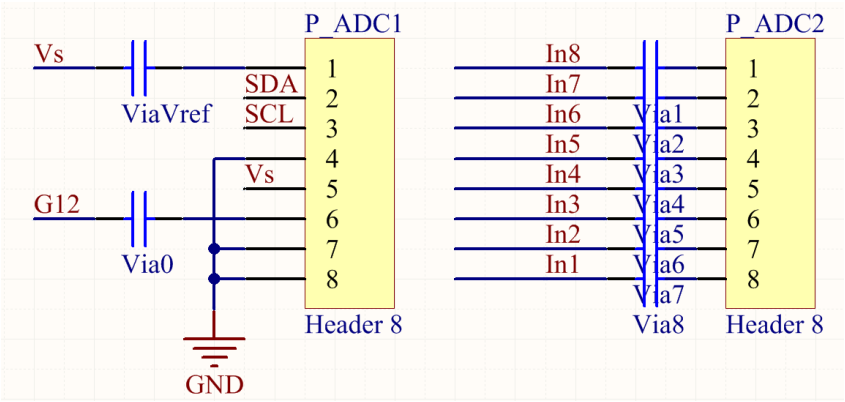


Figure 27: The Connection for the Breakout Board of the ADC IC.

The ADC employed has eight ADC pins allowing for four current sense amplifier measurements and four voltage sense amplifier measurements for the four strings. The ADC also integrates and inbuilt thermistor/thermocouple allowing for accurate ambient temperature measurements of the circuits. In operation this component will be placed in close proximity with the PV panel surface to measure the panel temperatures during operation and to correct voltage and current measurements with temperature fluctuations. The power supply of the ADC is 3.3 V to not exceed the maximum input voltage of the MPU GPIO pins of 3.3 V.

3.2.5 The Voltage Sensing Circuit

Voltage sensing circuit in Figure 28 is another means of quantifying PV panel output power fluctuations since this information coupled with the current measurements give a good indication of the power produced by each string of the customised PV panel. As the wiring configuration is changed the voltage and current measurements can help determine and quantify each of the three Maximum Power Point (MPP) values. The output of the circuit (which replaces the output of the panel) connects to an MPP tracker or DC optimiser to always operate at the MPP and thus the effect of shading can be directly measured on changes in the MPP.

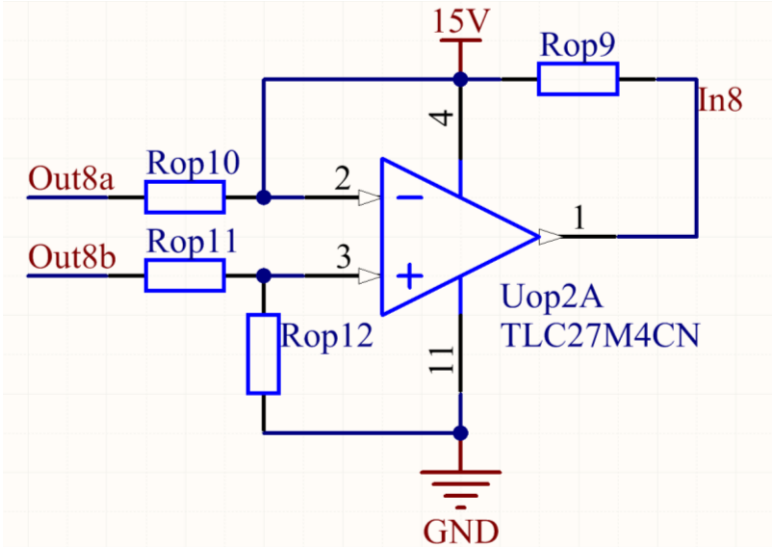


Figure 28: The Voltage Sensing Circuit using a Differential Amplifier.

The voltage sensing circuit is composed of a differential op-amp circuit that is matched to ensure a high common-mode rejection ratio to suppress this type of signal noise and allow a higher differential gain to ensure purity of the signal being measured by the ADC. This op-amp circuit needs to have a higher voltage supply since it has to measure voltages up to a maximum of 10.0 V for an open-circuit voltage (V_{oc}) of 16 cells in the 16 x 1 wiring configuration and thus has its own 15 V power supply to prevent the input signal from saturating and with a differential gain of 0.33 to decrease the ADC input voltage to a maximum of 3.3 V.

3.2.6 The Voltage Sensing Circuit Power Supply

The power supply in Figure 29 is provided by a combination of the voltage regulator which steadies the output voltage of 5 V and then supplies this to a DC-DC converter which has a voltage ripple less than 10 mV thus ensuring a stable supply voltage to the op-amp employed.

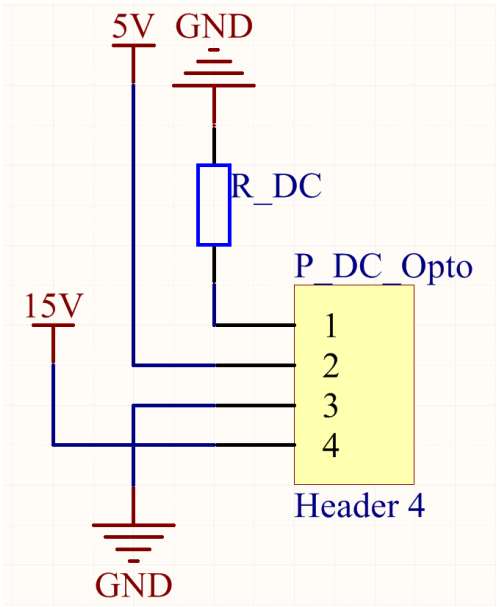


Figure 29: The Voltage Sensing Circuit Power Supply.

3.3. The Auxiliary Circuits

The auxiliary circuits are presented in Figure 30 and are composed of the following sub circuits:

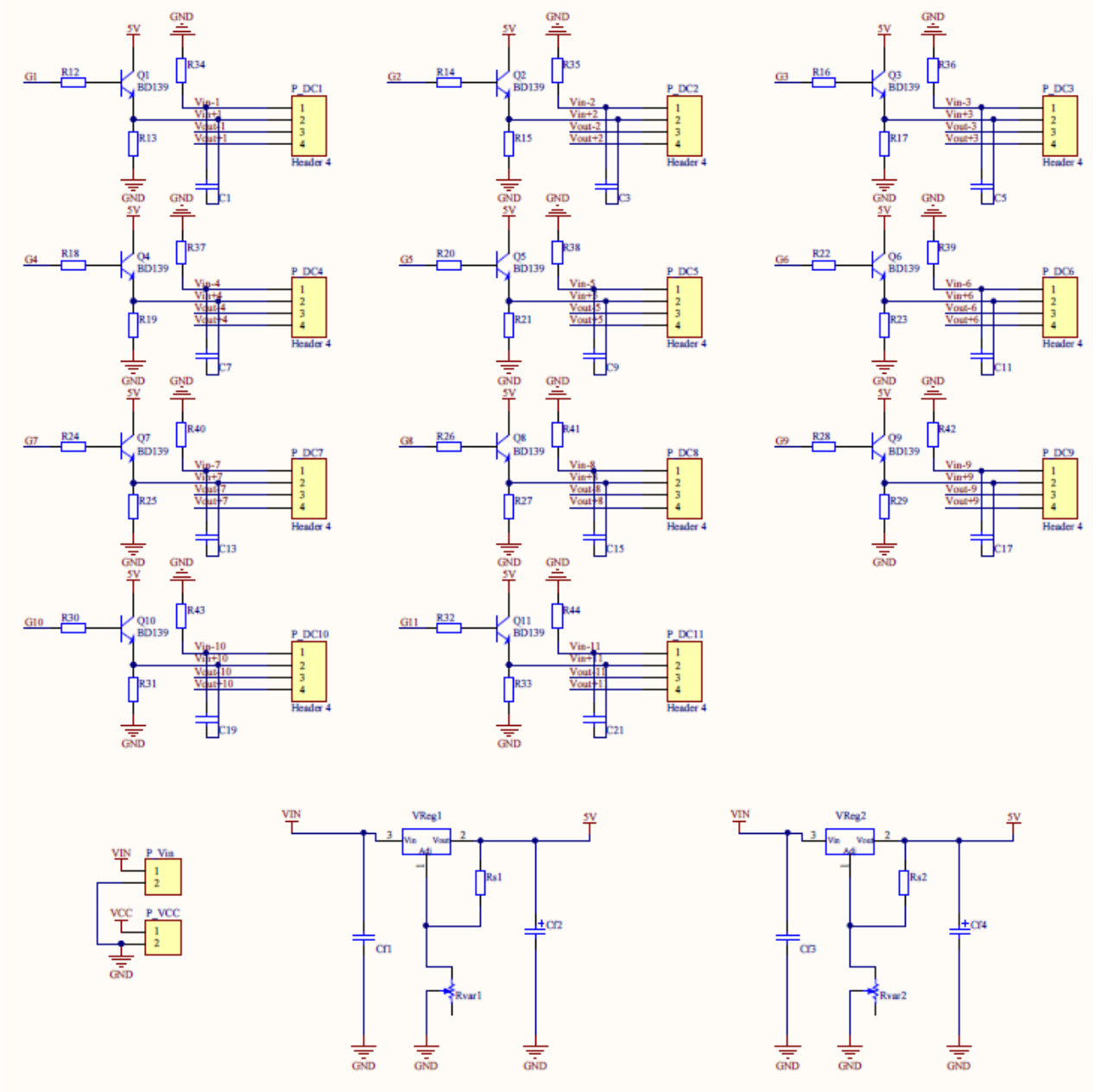


Figure 30: The Auxiliary Circuits.

3.3.1 The Intermediary Circuit

The MPUs as mentioned previously have a maximum output voltage of 3.3 V and thus need an intermediary circuit on the left in Figure 31, between the MPU and the drivers. This circuit has to take 3.3 V and output 5 V to drive the DC-DC converters which have a very specific input and output voltage and current rating.

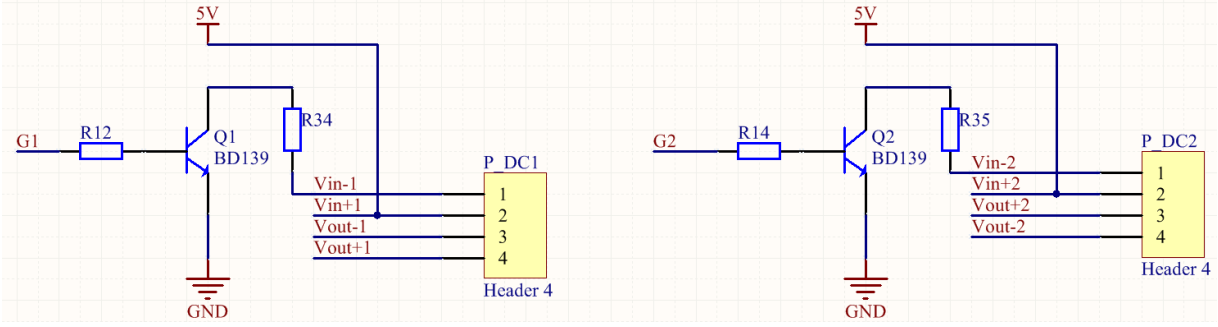


Figure 31: The Intermediary Circuit.

Since there is no high frequency switching there is no need to worry about dead-time, back Electromotive Forces (EMFs) or shoot-through currents as seen in faster switching power electronic applications. A simple NPN power BJT can be used to take the low voltage and current input from the MPU pins to supply a higher voltage and current to the DC-DC converter.

3.3.2 The DC-DC Converter drivers for the switches

The DC-DC converter driver circuits are presented on the right in Figure 34, are rated at 1 W and require an input voltage of 5V and current of 250 mA. This is supplied by current limiting the input voltage by carefully selecting the collector resistance for the NPN power BJT in the intermediary circuit. Thus the output voltage can be supplied with a 67 mA output current which in turn is current limited through the Zener resistance that forms a part of the MOSFET gate resistance protection circuit. Again since there is no rapid switching necessary and so the discharge time for the output of the DC-DC converters does not affect the operation of the circuit. The DC-DC converter with label P_DC1 is used to drive an N-FET and the DC-DC Converter with label P_DC2 is used to drive a P-FET.

3.3.3 The Connections for the Regulator, DC Optimiser and the Regulator Circuits

A two pin connection where an input voltage of 7 V and 4.2 A (current limit) from a bench top regulated DC power supply is provided to the two regulators connected in parallel to produce the desired output voltage and current required. A 6 mm plated through hole is provided for the positive and negative connections for the DC optimiser or MPP tracker to ensure that the PV panel regardless of its wiring configuration is always operating at its MPP. The setup for both connections is shown on the left of Figure 32.

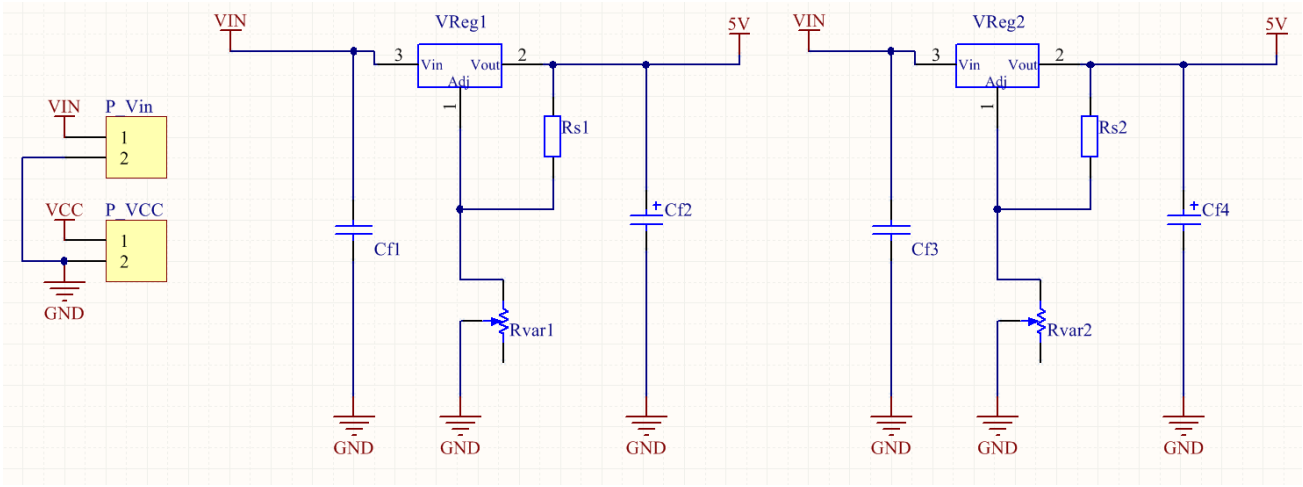


Figure 32: Connections for the Regulator, DC/DC Optimiser and Regulator Circuits.

There are two regulators used to supply 5 V and 4.4 A to the intermediary circuits and the current sense op-amp as shown on the right of Figure 34. The high currents are a requirement to ensure that all 11 intermediary circuits and the voltage sense op-amp power supply which draw 250 mA each can be supplied with adequate power. The op-amp used for current sensing which is also supplied with 5 V draws a fraction of this current.

3.4. Implementation of the Circuit on PCB and Design Methodology

In this section the factors that went into implementing the previously described circuits on a PCB are elaborated on and discussed in detail.

3.4.1 The Prototype PCB Circuit and Design Methodology

There are several design considerations that go in to designing the PCB since the key is to have smaller PCB dimensions to keep electrical power losses to a minimum which increase with longer PCB track lengths. The maximum current in each string is expected to go as high as 8.08 A

when in the 16 x 1 wiring configuration and the maximum current in the junction tracks when the four strings are connected in parallel is in the 4 x 4 wiring configuration is 27 A.

3.4.2 The Power Circuit

There are two design approaches for how to position the power circuit, the first to concentrate all MOSFETs and current handling devices into the centre of the PCB. The advantages of this approach are allowing for common nodes to share larger pads for mutual heat dissipation and the ability to have a common heat sink if required. The disadvantages of this system is the possible formation of hotspots where there is a concentration of heat due to insufficient ventilation or cooling of the components.

The second approach is to have all power components on the external edge of the PCB. The advantages of this approach is the prevention of heat accumulation in one spot since all edges are adequately ventilated however the disadvantages inherent with this arrangement are longer power track lengths between the switches resulting in higher resistances and so higher power dissipation in the PCB.

The first approach was followed since it had disadvantages that could be easily mitigated through the use of wider copper areas for MOSFET pins to allow for heat dissipation and to counter the disadvantages of the second approach since these wider copper areas also contributed to lower track resistances and so lower power dissipation in the tracks.

3.4.2 The Control and Sensing Circuits

The control and sensing circuits were compromise with the positioning of the driver circuits. For these latter to be as close to the switches as possible the control and sensing circuits had to have long signal tracks between their outputs and the ADC pins. The effect of this compromise was expected to be negligible by ensuring a high Common-Mode Rejection Ratio (CMRR) for the two operational amplifier circuits employed for the current sensing (inverting operational amplifier since the current sense amplifier has a high CMRR) and for the voltage sensing (a differential operational amplifier).

3.4.3 The Auxiliary Circuits

The auxiliary and the driver circuits were positioned towards the far edge of the board where the VCC and VIN pins were located to power the regulators and for ease of access to the power output of the PCB for the DC/DC optimiser. These were situated around the outside of the board in close proximity to the switches they controlled. The concern with the latter circuits was to reduce any introduced capacitance that could cause an increase and decrease in the DC-DC converter input and output voltages on the order of 1 second which could create problems when switching between wiring configurations.

However the time between switching occurs between large time intervals on the order of several minutes between wiring configurations and the changes are made sparingly over the hour, the occurrence of slow charging and discharging of the converter and so slow turn on and off of the switches was not a concern.

3.4.4 The Order of Assembly of the SCPM Circuit

The PCB was first continuity tested to ensure that there was no islanding between grounds planes. Where this occurred it was fixed by electrical connections with the rest of the ground plane of the PCB. Then the regulator circuits were soldered on, tested and tuned to output the desired 4.83 V that would be supplied to the input of the BJTs composing the intermediary circuit between the MPU and the input of the DC-DC converter.

The next step was the soldering of the 20 x 2 receptacle for the MPU and the auxiliary and driver circuits to test the operation of these. When this was sufficiently functional the MPU was used to control the drivers and when the desired output voltage of 15 V was measured across the output of the DC-DC converter, the current sense amplifiers, the current sense resistors, the MOSFETs and the electrical connectors for the PV panel strings added. All of these components are in close proximity so the smaller components had to be added first.

Lastly the sensing circuits of the current and voltage sensing operational amplifiers were added and the ADC with I^2C functionality added and tested. Due to time constraints of the project a constant current source connected to the electrical connections of each string and supplying a fixed current could not be employed to test the current sense amplifier and the voltage sensing of the string. These tests would have to be performed when the custom made panel was connected up to the SCPM circuit.

3.4.5 The PCB Layout (both Unpopulated and Populated)

The unpopulated PCB is shown in Figure 33 and Figure 34 for the front and back of the PCB, respectively. The power circuits, the current sense resistor and amplifier are seen in the area labelled 1, the interface and driver circuits can be seen in area 2, the regulator circuits and power input and output connections for the PCB in area 3, the op-amps for current and voltage sensing are in area 4, the ADC that interfaces with the MPU is in area 5 and the MPU in area 6.

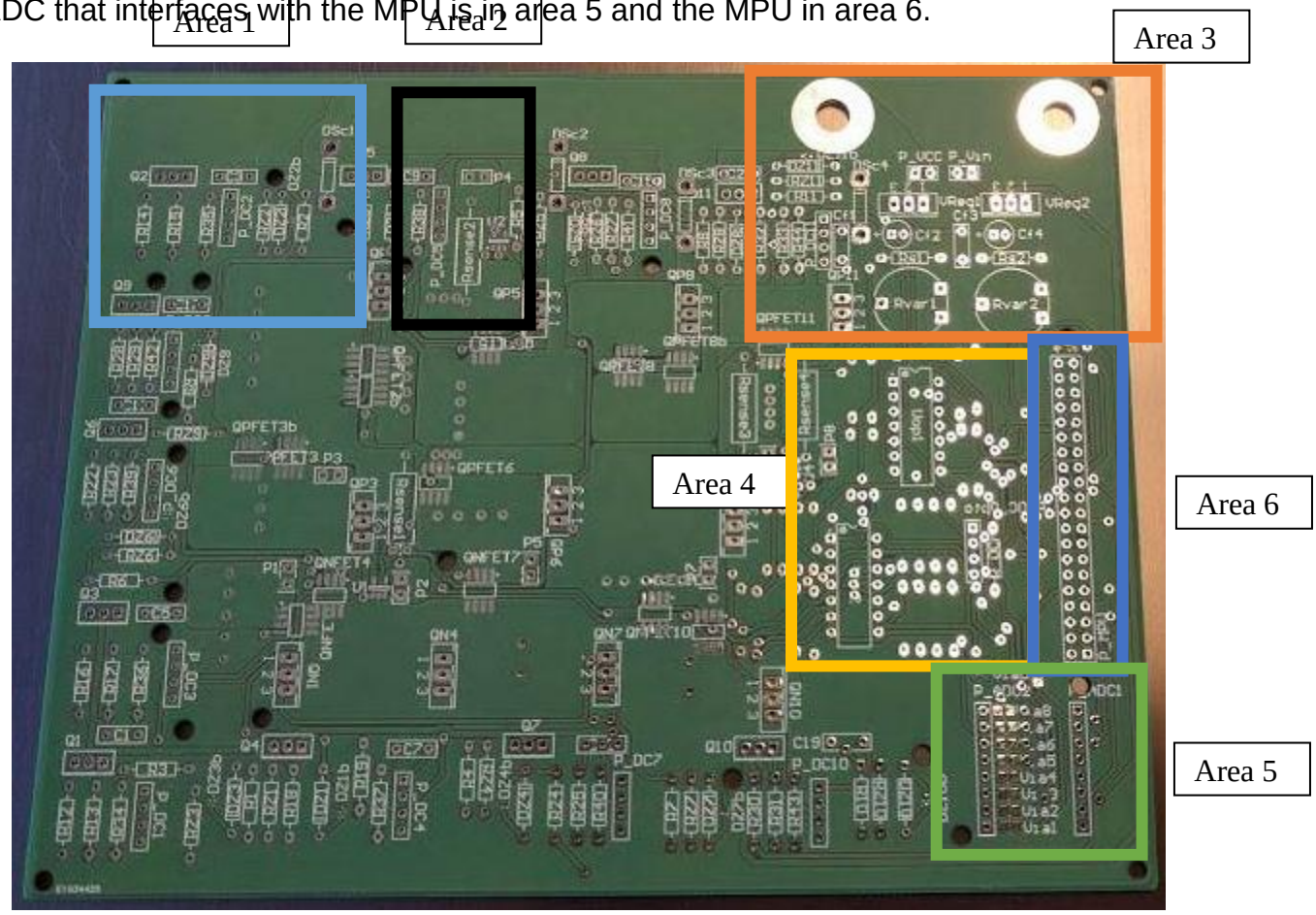


Figure 33: The front of the unpopulated PCB.

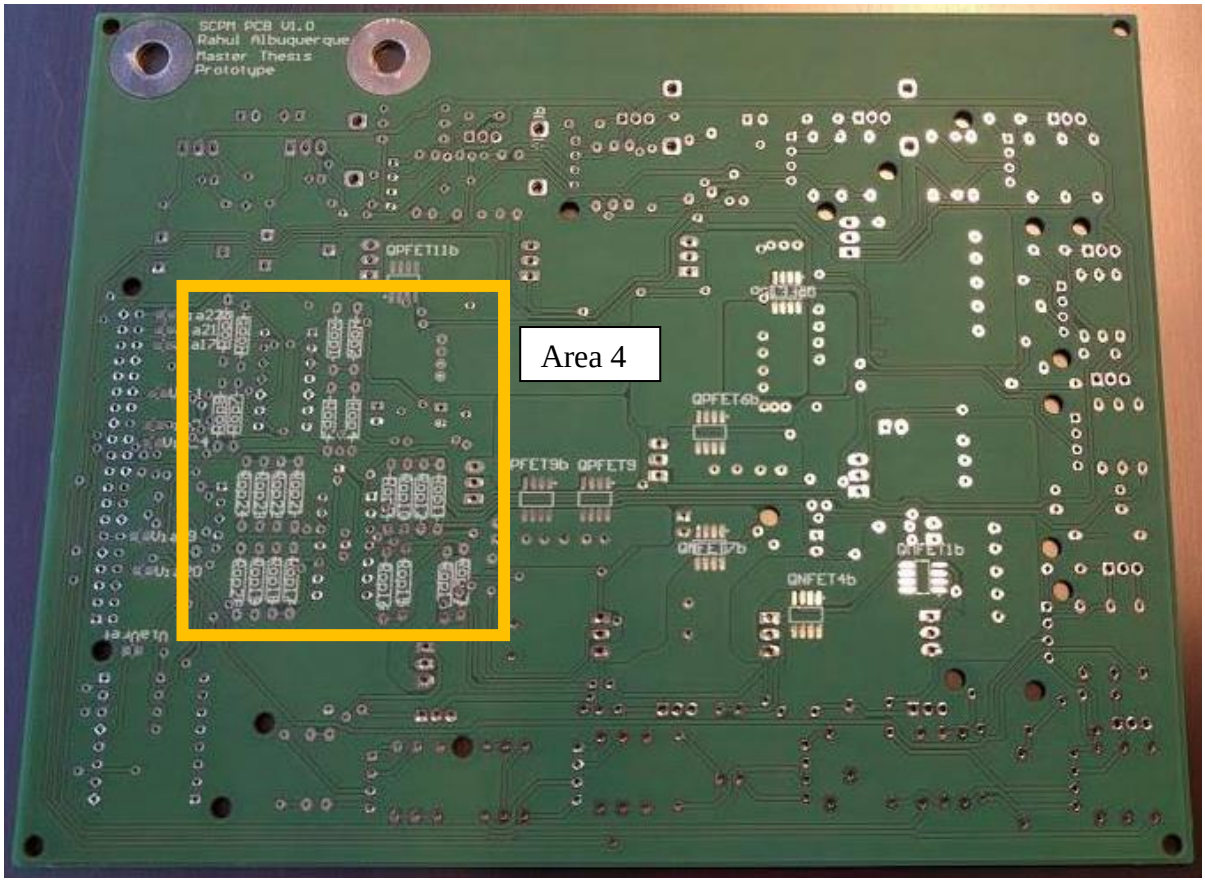


Figure 34: The back of the unpopulated PCB.

The same PCB is shown here populated based on the project preferences in Figure 35 and 36 and the same areas described earlier in this section are shown in the figures below. The banana plugs used for the PCB output can be clearly seen and the wire used to supply the regulators with power can also clearly be seen. The strings of the PV panel are connected using the banana plug sockets that are labelled and these were deemed a solution for now for ease of connection of the panel. The MPU is shown in a way where the power cable, the mini-USB and mini-HDMI cables can be connected from the top of the figure to allow for ease of powering, programming and connection of a PC monitor for the graphical user interface. The areas are again labelled for ease of identification of the different sub circuits and correspond to the labels of the unpopulated PCB.

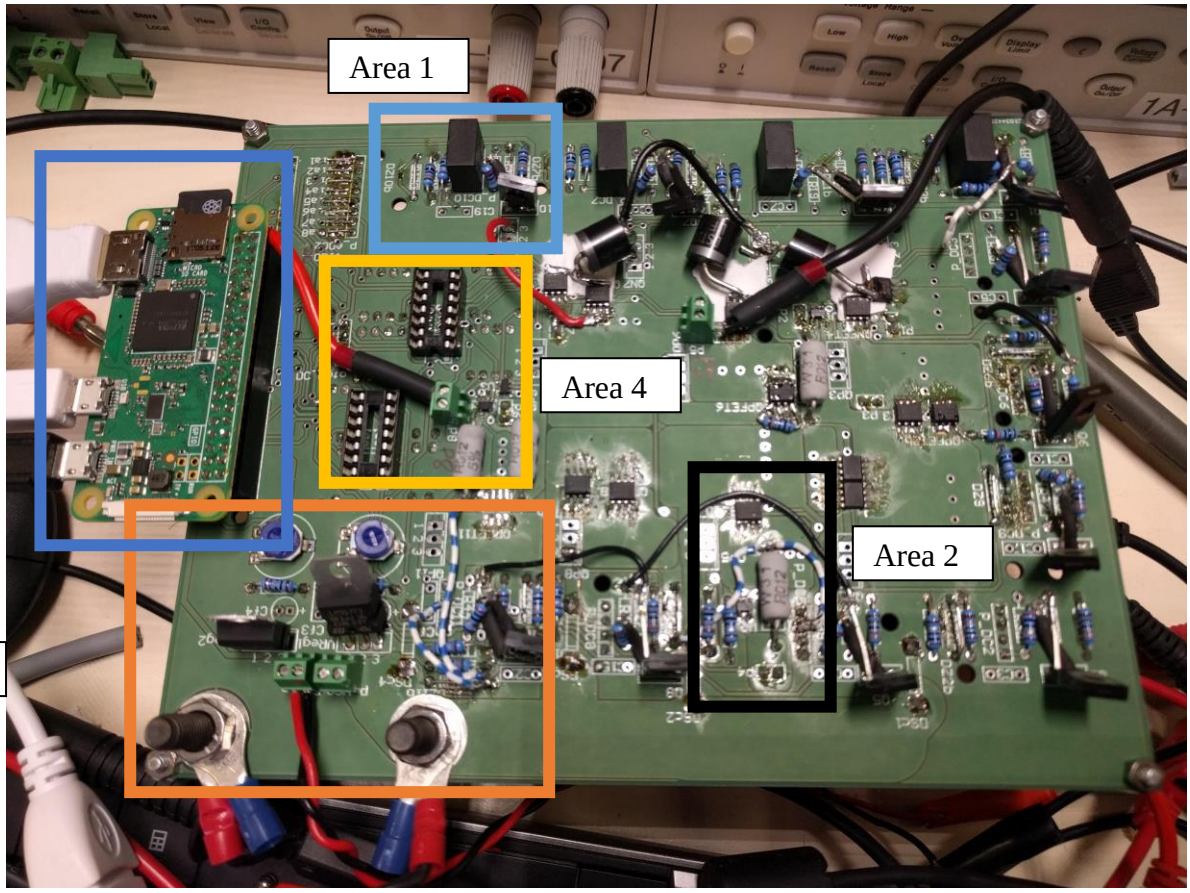


Figure 35: The top of the partially populated PCB.

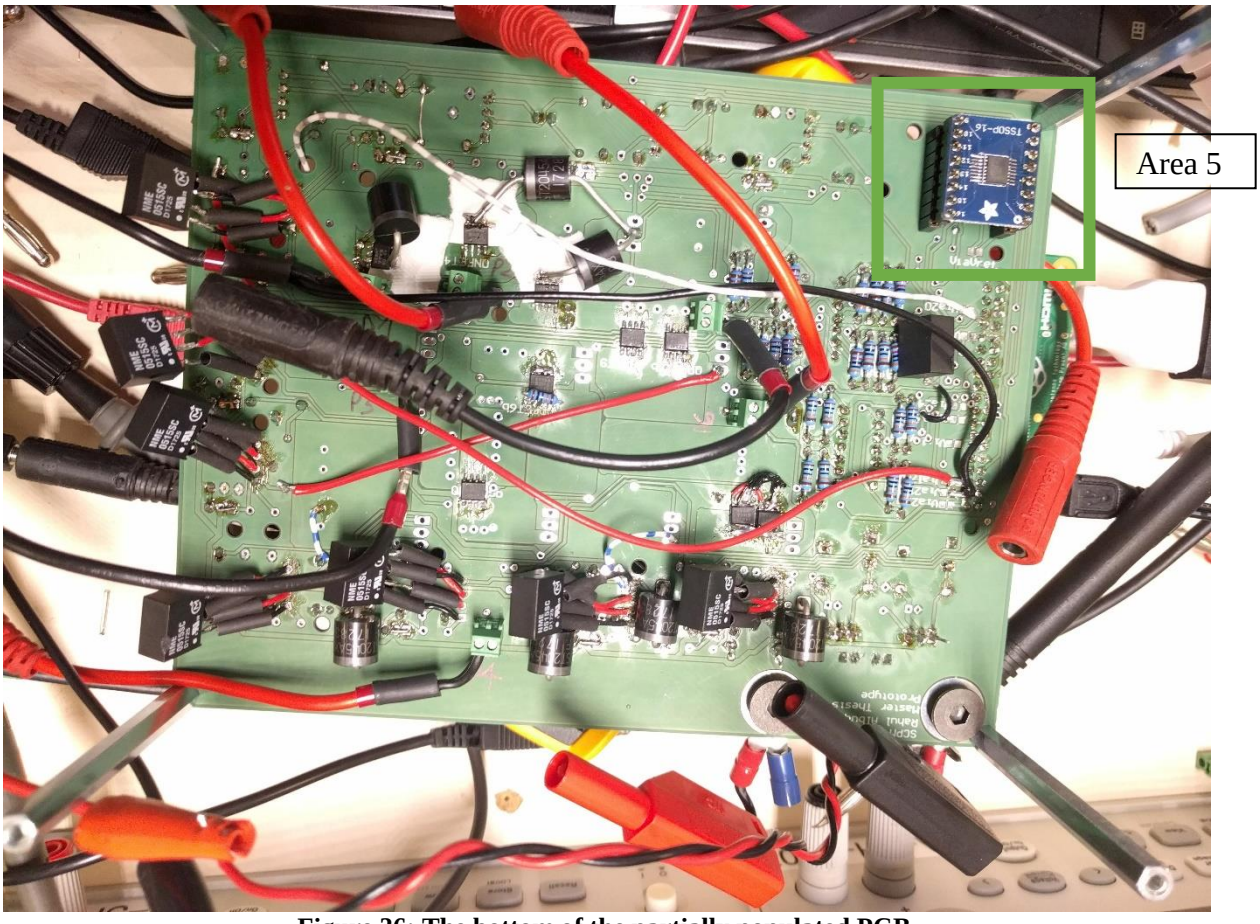


Figure 36: The bottom of the partially populated PCB.

3.5. Circuit Functionality during Shading

The SCPM circuit functionality depends on hardware and software working closely in tandem. On initialisation of the first command the 4 x 4 configuration is selected and the DC optimiser or MPP tracker operates to bring the voltage and current output to the maximum power point of a load. This allows for measurement of current and voltage by all current sense and voltage sense circuits before transitioning to the 8 x 2 wiring configuration to perform the same measurements and then the 16 x 1 wiring configuration where these measurements are performed again.

The goal is to then determine which of these wiring configurations gives the highest maximum power point, the present level of shading, irradiance and temperature and to thus settle on the optimum of these three wiring configurations. The means for implementing this control algorithm is presented in the next section.

3.6. Software Implementation Explanation

The software algorithm is described by the flowchart in the patent [24] and seen in Figure 37.

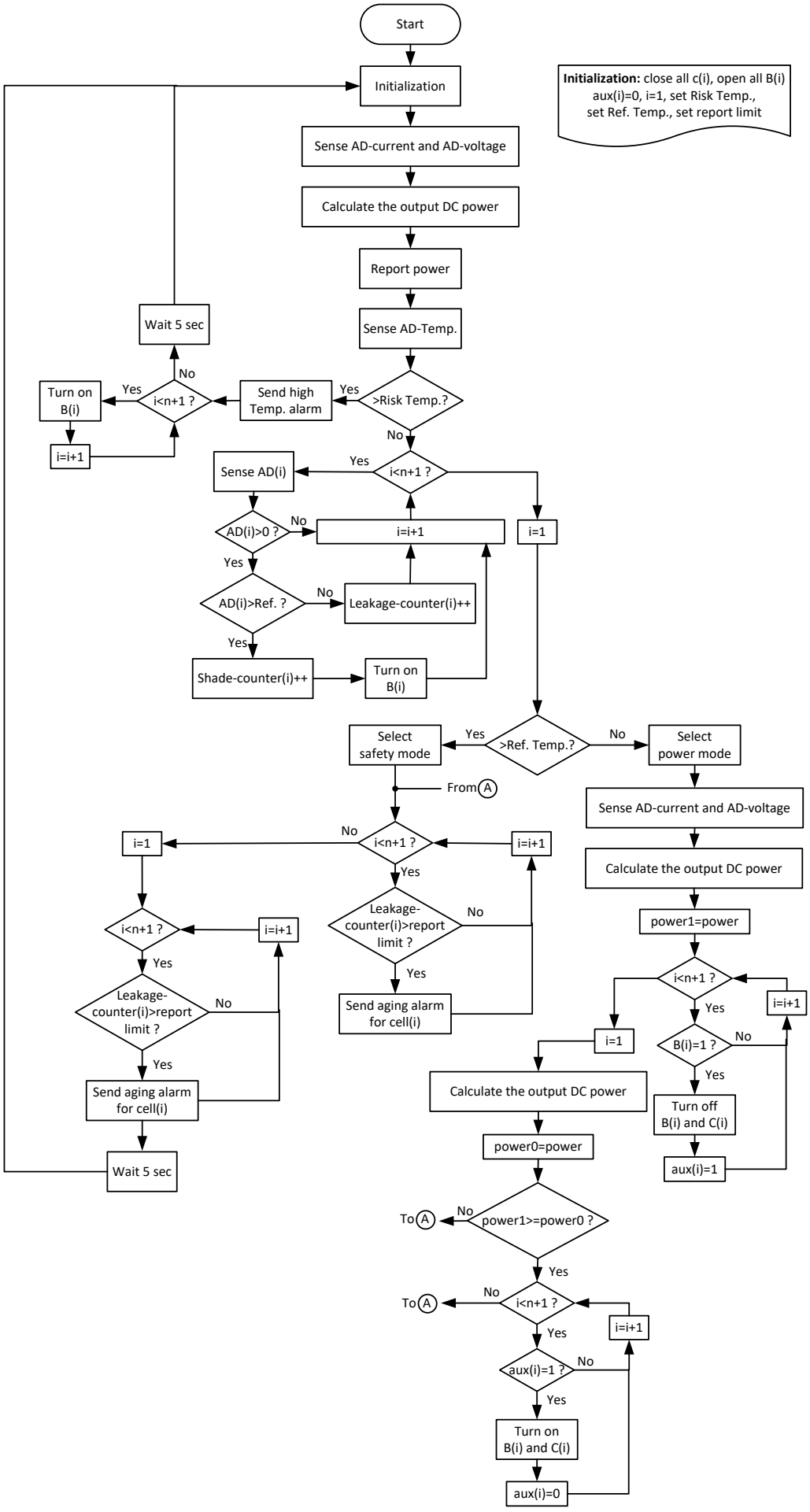
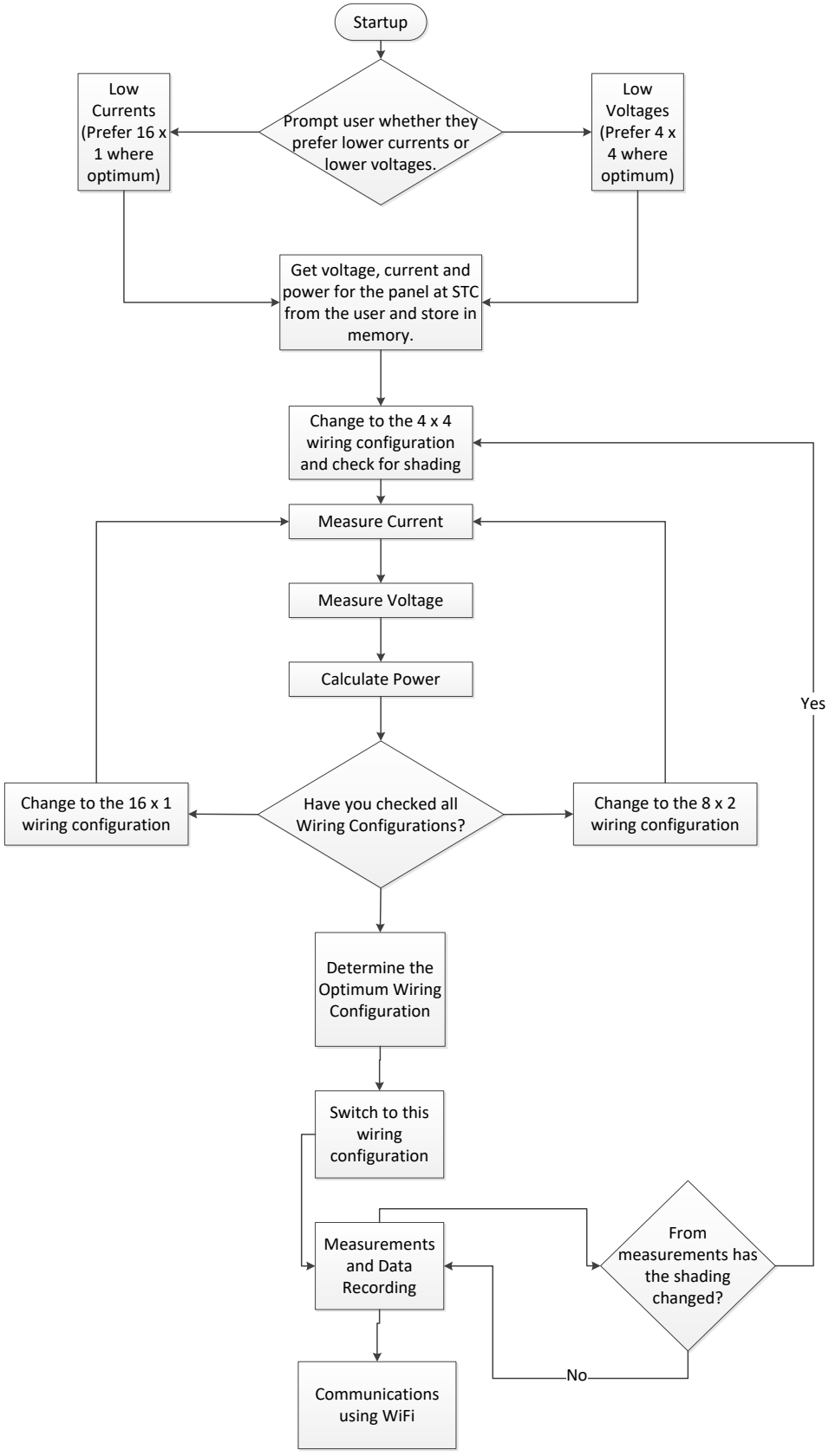


Figure 37: The Software Algorithm from the Patent.

The flowchart is quite basic in terms of functionality and needed more detail added for the case of shading occurring, quantifying the level of shading and measuring the values of voltage, current and so calculate power for each string. The new algorithm proposed and implemented would determine when to switch between the three wiring configurations. Thus the previous flowchart has been greatly expanded on and is presented and explained in greater detail in Figure 38 with the aid of state diagrams.



The different states and functions employed by the software will now be discussed in detail in the subsections of this part of the report.

3.6.1 Start-up and Initialisation

The MPU on start-up will prompt the user or installer through the GUI about their PV system setup, do they desire lower currents (for long cable lengths in their setup) or lower voltages (for charge controllers or inverters that can handle lower input voltages) and then move on to determine the ideal conditions of current, voltage and power when there is no shading.

The best way to do this is by a user or installer entering the voltage, current and power ratings of the panel under Standard Test Conditions (STC) when there is no shading of the panel. After running this function and storing it in memory the function that changes to the 4 x 4 wiring configuration to be able to measure current and voltage across all four strings. It then activates the current sensing and voltage measurement functions.

3.6.2 Current Sensing

Since all four strings are in parallel in the 4 x 4 wiring configuration, the current flowing through all four current sense resistors can be determined and the current through the four strings and for the panel as a whole determined. The panel current is the total current in the four strings.

3.6.3 Voltage Measurement

The voltage across all four strings can be measured using the differential amplifiers utilised for this purpose. The values of the string voltages along with the current can be used by the power calculation function.

3.6.4 Power Calculation

Through measuring the current and voltage, the power supplied by each string can be determined by simple multiplication. If the DC optimiser is utilised to make the load seen by the PCB operate at the maximum power point, then the power supplied by the panel at this point can be determined by this function.

3.6.5 Switching Wiring Configurations

On completion of measurements from the 4 x 4 wiring configuration, the wiring configuration is changed to 8 x 2 and the previous functions for current and voltage measurements run and power calculated for the strings and panel in this wiring configuration. When these are completed the wiring configuration is changed to 16 x 1 and the current, voltage and power obtained.

In this way the wiring configuration with the most power output for the particular shading level is determined and the wiring configuration is switched for the panel to output the most power. Through the repetition of these measurement runs every seven minutes changes in shading can be detected and acted upon to ensure that the optimum wiring configuration is chosen and implemented.

In the case where two or more wiring configurations show the same measured power, the information provided by the user or installer through the GUI about low current or low voltage requirement will be taken into account. The wiring configuration that gives the optimum power and the desired low current or low voltage will be implemented.

3.6.6 Measurements and Data Recording

The measurements and data recording is performed every time the wiring configuration is changed and if there is WiFi connectivity (which is tied to time and location for the Raspberry Pi) then this data can have a time stamp added to determine when shading occurs or to either operate off or verify weather data from the Dutch PV Portal 2.0 [29]. The data is recorded on the microSD card from which the Raspbian operating system for the Raspberry Pi is booted from and the Python code executed from.

3.6.7 Communications using WiFi

For the future version of the SCPM, the communications system can be implemented where there is a WiFi system available. During development of the code and of this system, eduroam was readily available to provide a WiFi connection and thus data could be displayed graphically on web browsers by the Raspberry Pi MPU. Thus a real time display of information can be provided. The use of a remote desktop tool for running updates to the operating system and for future upgrades to the code is also possible when WiFi is available.

3.7. The Design of a Custom-made Solar Panel

The use of BPDs was not necessary and so a new PV panel which could change its wiring configuration between the three desired wiring configurations investigated had to be made.

A custom panel of 16 cells was created of 4 x 4 Interdigitated Back Contact (IBC) high efficiency solar cells (with efficiencies between 22.3 - 22.7 % depending on grade) from the SunPower Maxeon Gen II series of cells. Thus the theoretical values for the panel from the solar cell datasheet [26] are a maximum current for each branch would be 6.01 A per string of 4 cells in series, 12.00 A for the 8 x 2 wiring configuration and a maximum panel current of about 24.04 A for the 4 x 4 wiring configuration. The voltage specifications would vary from 2.32 V for the 4 x 4 wiring configuration, 4.64 V for the 8 x 2 wiring configuration and 9.28 V for the 16 x 1 wiring configuration, all operating at the theoretical maximum power point.

The mechanical dimensions, given in millimetres (mm) are presented in Figure 38 and the panel was ordered from Solbian Energie Alternative Srl which produced two of these panels. Due to an error in the ordering process, bypass diodes were included in the custom-made panels, however these were removed in such a way to not adversely affect the output of the panels once modified.

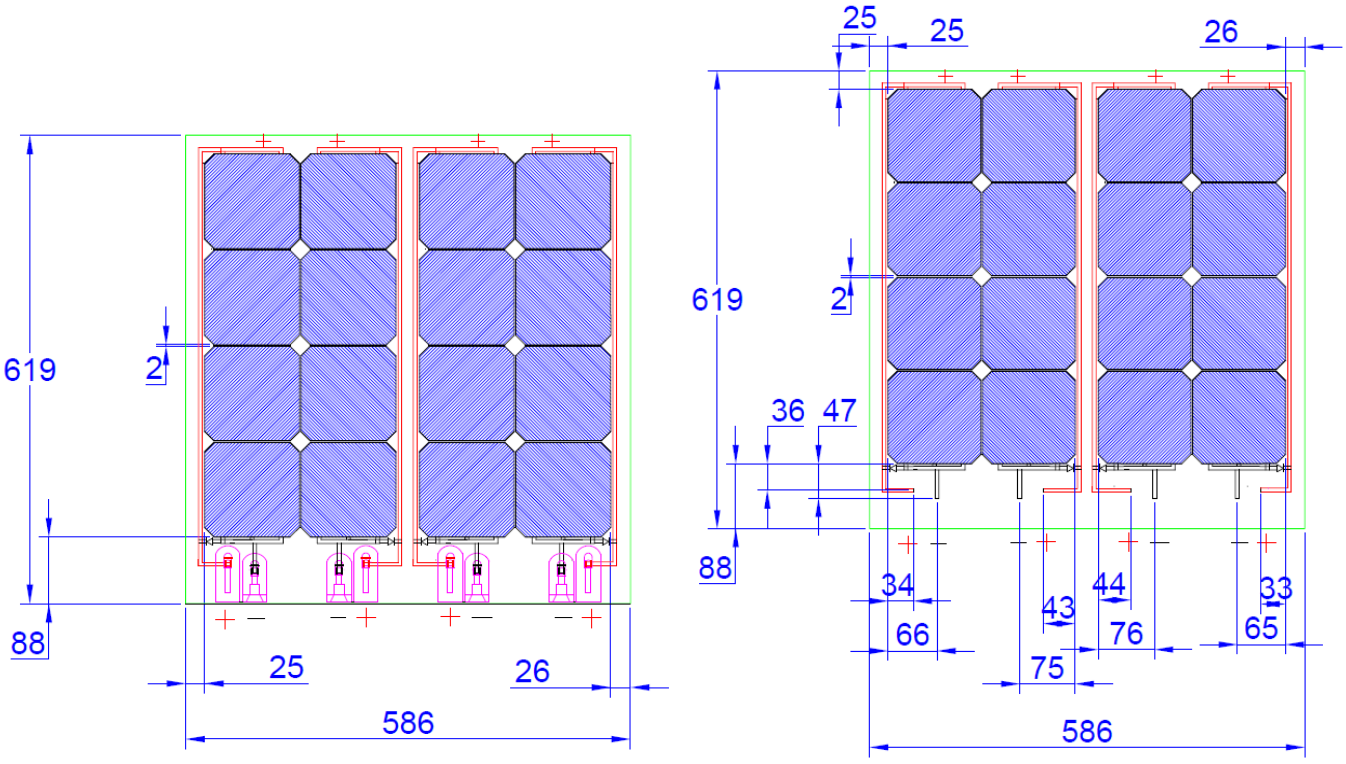


Figure 38: The 16 Cell Solar Panel Dimensions in mm.

The connectors chosen for the electrical outputs of the panel are the MC-4 connectors which have a resistance of 0.5 mΩ [30] and the cables for electrical connections had a resistance of 10 mΩ/m. The wiring output (MC-4 male or female connectors to male banana plugs) was thus measured to be below 10 mΩ. The electrical connection to the IV tester was kept as short (smaller resistance) as possible at 10 mΩ through having two 2 m long cables in parallel. Thus the total series

resistance from MC-4 to MC-4 connector would be 40 mΩ (two MC-4 to banana plug and two banana plug to I-V tester connections).

3.8. The Tests Carried Out for Shading Testing and Results Measured

The purpose of the code and control algorithm are to constantly measure current through and voltage across all strings to determine when shading is occurring in each string. It thus determines what the shading is and when to change between the three wiring configurations as mentioned in section 3.5.

To determine the values of current and voltage under the different shading conditions manual control of the circuit was needed to change between the three wiring conditions and take measurements. This was done for the three promising configurations described below after manual shading measurements of the panel were taken in the six shading configurations described in the first half of chapter 4.

3.8.1 The Three Shading Conditions to be Tested Using the PCB

The three shading conditions that were tested using the PCB are shading configurations 3, 4 and 6 (these will be elaborated on in section 4.3 to prevent repetition) since these favour the 4 x 4, the 8 x 2 and the 16 x 1 configurations, respectively, when measured without the circuit. A comparison with the measurements made with the circuit would show both the how effective the circuit was in operating and to quantify power losses due to the operation of the circuit.

3.9. Resistances and Power Dissipation of the SCPM Circuit

The resistances of the connectors, cables and PCB are presented for the three wiring configurations in the next three wiring configurations.

3.9.1 The 16 x 1 Wiring Configuration

The current per string of 16 cells is 6.11 Amps and this translates to theoretical power loss in the panel with 16 x 1 wiring configuration presented in Table 11. As can be seen from the 52 W rated panel, 12.94 W are lost across the switches, the sense resistor, the blocking diodes and the MC4 connectors.

Table 11: The Theoretical Power Dissipated in the 16 x 1 Wiring Configuration.

Resistances			
Description	**Value [Ω]**	**Power Dissipation [W]**	**Percentage Loss [%]**
N-FET 1	0.012	0.42	3.63
P-FET 3	0.009	0.32	2.73
P-FET 6	0.009	0.32	2.73
P-FET 9	0.009	0.32	2.73
P-FET 11	0.009	0.32	2.73
Rsense4	0.012	0.42	3.63
2 x Blocking Diodes		7.10	61.37
8 * MC4 with 50 mm	0.4	2.37	20.46
Total	0.46	11.57	

3.9.2 The 8 x 2 Wiring Configuration

The current per string of eight cells is 6.11 Amps and this translates to theoretical power loss in the panel with 8 x 2 wiring configuration presented in Table 12. As can be seen from the 52 W rated panel, 14.22 W are lost across the switches, the sense resistor, the blocking diodes and the MC4 connectors.

Table 12: The Theoretical Power Dissipated in the 8 x 2 Wiring Configuration.

Resistances			
Description	**Value [Ω]**	**Power Dissipation [W]**	**Percentage Loss [%]**
N-FET 1	0.012	0.42	3.39
P-FET 3	0.009	0.32	2.54
P-FET 5	0.009	0.32	2.54
N-FET 7	0.012	0.42	3.39
P-FET 9	0.009	0.32	2.54
P-FET 11	0.009	0.32	2.54
Rsense2	0.012	0.42	3.39
Rsense4	0.012	0.42	3.39
4 x Blocking Diodes		7.10	57.22
8 * MC4 with 50 mm	0.4	2.37	19.07
Total	0.012	0.42	

3.9.3 The 4 x 4 Wiring Configuration

The current per string of 4 cells is 6.11 Amps and this translates to theoretical power loss in the panel with 4 x 4 wiring configuration presented in Table 13. As can be seen from the 52 W rated panel, 20.68 W are lost across the switches, the sense resistor, the blocking diodes and the MC4 connectors.

Table 13: The Theoretical Power Dissipated in the 4 x 4 Wiring Configuration.

Resistances			
Description	**Value [Ω]**	**Power Dissipation [W]**	**Percentage Loss [%]**
N-FET 1	0.012	0.42	1.98
P-FET 2	0.009	0.32	1.49
N-FET 4	0.012	0.42	1.98
P-FET 5	0.009	0.32	1.49
N-FET 7	0.012	0.42	1.98
P-FET 8	0.009	0.32	1.49
N-FET 10	0.012	0.42	1.98
P-FET 11	0.009	0.32	1.49
Rsense1	0.012	0.42	1.98
Rsense2	0.012	0.42	1.98
Rsense3	0.012	0.42	1.98
Rsense4	0.012	0.42	1.98
8 x Blocking Diodes		14.21	67.01
8 * MC4 with 50 mm	0.4	2.37	11.17
Total	0.532	21.20	

The blocking diodes even with a low forward voltage drop of 0.3 V can dissipate between 57.22 % (for the 8 x 2 wiring configuration) to 67.01 % (for the 16 x 1 wiring configuration) of the total power loss. The total theoretical power losses of the system are on the order of 21.21 % to 38.86 % for 16 x 1 and 4 x 4 wiring configurations, respectively of the power supplied by the panel with a theoretical unshaded output value of 54.46 W.

4 Results from Simulations and Measurements

A summary has been provided thus far for the test of the theory using Simulink simulations. Measurements on custom built modules were then conducted to validate the simulation models and a Smart Cell-level Power Management (SCPM) circuit designed that could actively switch between the three wiring configurations. In this section a test methodology is described to conduct the measurements for both manual and SCPM circuit controlled, wiring configurations.

Two comparisons will be conducted, the first, between the simulations and the measured data of the wiring configurations taken manually and the second a comparison between the circuit simulation results and the measured data from the SCPM circuit used to switch between the wiring configurations. The results will then be analysed, discussed and the comparison between findings presented in the last part of this chapter. An extra case where two different bypass diodes are compared by measurement is also conducted to discuss the importance of the right choice of bypass diode to reduce power losses in a panel employing them.

4.1. Test Protocol for the Custom Made Panel and the SCPM Circuit

4.1.1 Intent of the Test Protocol

To generate I-V and P-V curves for the custom made Solbian panels with the internal bypass diodes disabled and for the SCPM circuit to verify the Simulink models created and explained in chapter 2. Thus determine if the use of the different wiring configurations is adequate for improving shading tolerability and determine if a system without Bypass Diodes (BPDs) can work.

4.1.2 Methodology

4.1.2.1 For the panel in 16 x 1 wiring configuration with 2 BPDs and 4 BPDs.

The LASS, the Keithly and the BK Precision Electronic Load are used to measure the I-V and P-V curves of the panels for the 4x4 panel in the 16 x 1 wiring configuration with 2 BPDs and with 4 BPDs in the six different shading configurations shown in the figures below in order of 1 to 6.

In the figures the red refers to shaded cells and the green to unshaded cells. The shading is changed by varying the shading factor for each shading configuration. The temperature along with

these measurements will also be taken and corrections made for temperature and irradiance variations from STC.

The shading is achieved with the shading factor 0.45 and 0.55 explained earlier in section 3.7. Thus two different I-V and P-V curves will be generated for each of the shading factors and for the six shading configurations, giving 12 individual P-V and I-V curves. These 12 individual tests need to be determined for the panel with 2 BPD and with 4 BPDs giving a total of 24 P-V and I-V curves.

A further four tests comparing smart BPDs (SM74611KT) with Schottky diodes with the lowest forward voltage drop will also be made with shading configuration 2. The tests involved two unshaded tests and two tests with a shading factor of 0.55.

4.1.2.2 For the panel in 8 x 2 wiring configuration without BPDs.

The shading is achieved with the shading factors of 0.45 and 0.55. Two different I-V and P-V curves will be generated for each of the two shading factors and for the six shading configurations, giving 24 individual P-V and I-V curves.

4.1.2.3 For the panel in 4 x 4 wiring configuration without BPDs.

The shading is achieved with the shading factors of 0.45 and 0.55. There are four different I-V and P-V curves will be generated for the two shading factors and for the three shading configurations, giving 14 individual P-V and I-V curves. Two custom panels connected in series with the 4 x 4 wiring configuration will be used since the IV tracer software current limits at the currents of 25 A and 2.4 V. The panels connected in series deliver 25 A but at a higher voltage of about 5.5 V.

4.1.2.4 SCPM circuit implementation and panel test in 16 x 1, 8 x 2 and 4 x 4 wiring configurations.

The measurements using the circuit are optimised from the above 52 test measurements to show when different wiring configurations should be employed. The circuit controller will be programmed to manually make the transitions between the different wiring conditions as explained previously. Shading configuration 1 can be ignored since it only impacts the 16 x 1 wiring configuration, SC 2 and 3 show what happens when one string is shielded thus a 8x2 or 4x4 configuration is best suited for this application. SC 4 and 5 show what happens when 3 and 4 strings, respectively, have one cell shaded in their strings and SC 6 is a combination of SC 2 and 4 and thus can show how all wiring configurations can be tested to obtain the maximum output power of the cells for different shading.

Thus the tests to be performed are for SC 3, 4 and 6 with the circuit for the two SF of 0.45 and 0.55 for ease of comparison with the previous manual measurements. Two different I-V and P-V curves will be generated for each of the two shading factors and for the three wiring configurations. This will be used to test how the circuit can change between these three different wiring configurations based on trying to optimise the power output of the panel during the different shading conditions.

4.1.2.5 Conclusions that can be drawn from the test results

The data collected above will help validate if it is better to have a change in wiring configuration when there are different shading conditions present and determine if the circuit topology is better than using BPDs. It will also help quantify when at low shading conditions (with a comparison of shading factors of 0.45 and 0.55) if one of these three methodologies (no BPDs, with BPDs or the SCPM circuit) is better and when there may be a need to switch between the three wiring configurations in different shading conditions to maximize the electrical power output.

4.1.2.6 Setup:

One unused panel will have the cell size plastic sheets placed on top of it (15 sheets on the cells to be shaded) and then these transferred to the cells to be shaded on the panels. The arrangement for the 16 x 1, 8 x 2 and 4 x 4 wiring configurations are shown in Figures 43, 44 and 45, respectively. The wiring employed for electrical output connections for both panels are shown in Figures 46 and 47. In this case MC-4 to banana plug connectors were utilized since these offered the lowest connector resistors as described in sec

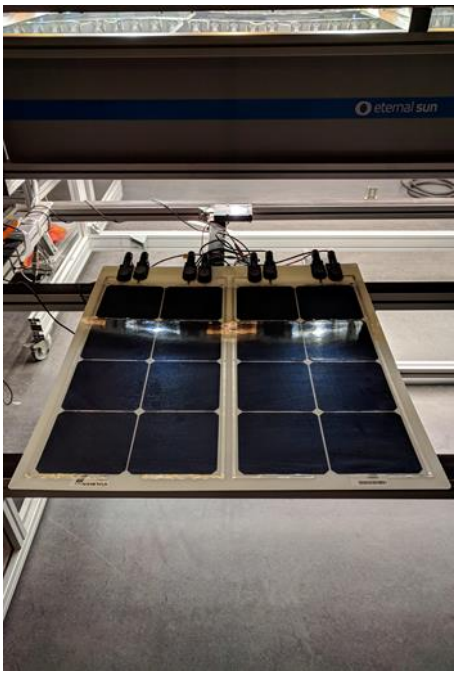


Figure 39: The 16 x 1 Wiring Configuration.

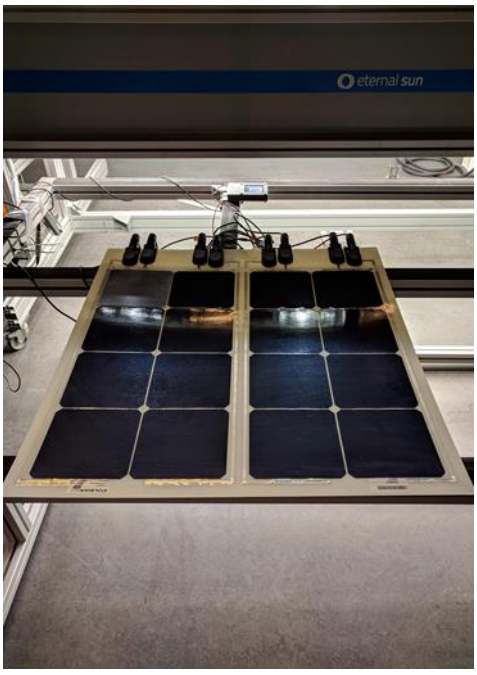


Figure 40: The 8 x 2 Wiring Configuration.

Figure 41: The 4 x 4 Wiring Configuration with two panels in series.

4.2. The Results from the Shaded Panel Testing

The simulation results for the unshaded panels in all three wiring configurations are shown in Figure 42. It can clearly be seen that all three panels produce the same output power and have the same value for the maximum power point at different voltages.

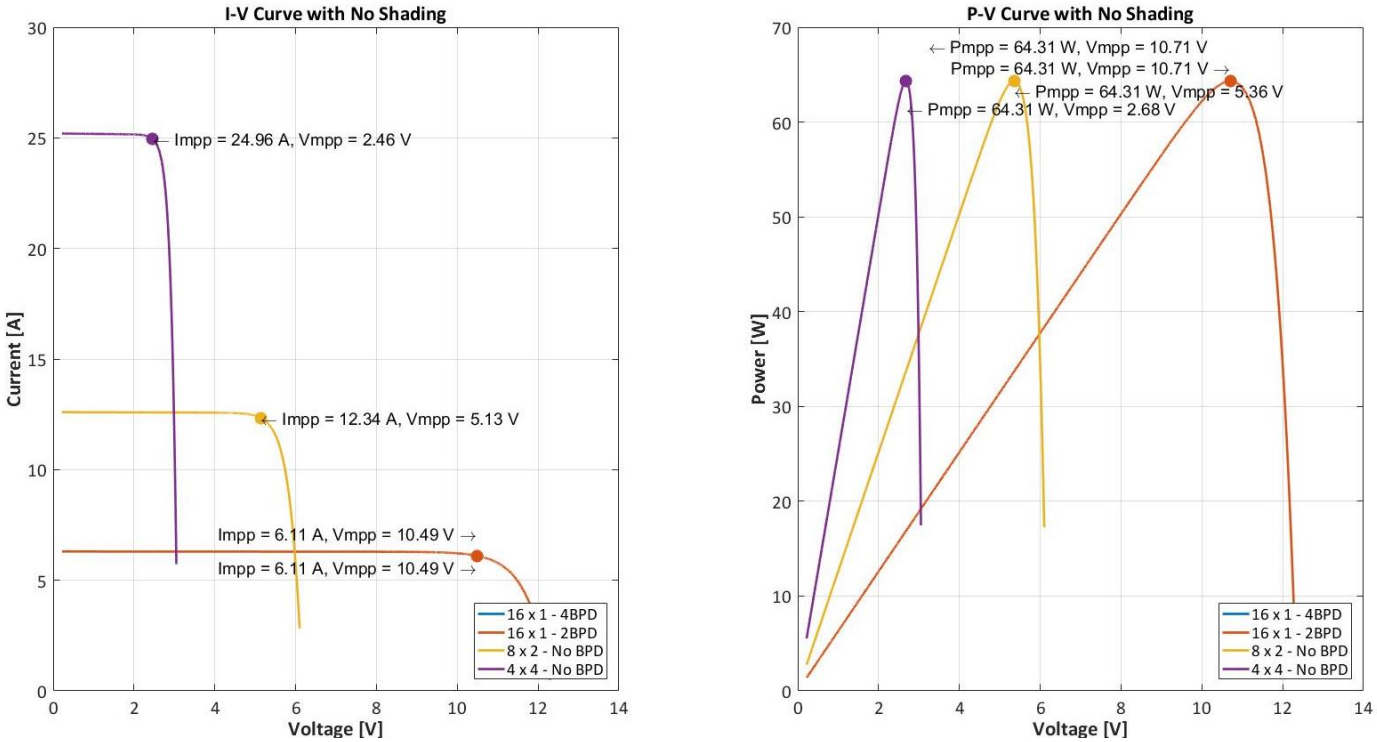


Figure 42: The Simulation I-V and P-V Curves of the Three Wiring Configurations with BPDs.

The measured results using the LASS were determined as the base line against which all shading would be compared and are illustrated in Figure 43. The reason for the 4 x 4 configuration having double the power than the other two configurations is due to the software for measuring the I-V and P-V curves current limiting at 2.4 V and 25 A and thus two custom made panels with 4 x 4 wiring configuration had to be connected in series to give a higher voltage. The 4 x 4 panel has a P_{mpp} of 45.03 W, V_{mpp} of 1.74 V and the measured I_{mpp} of 22.52 A when unshaded. The second panel remained unshaded for all tests.

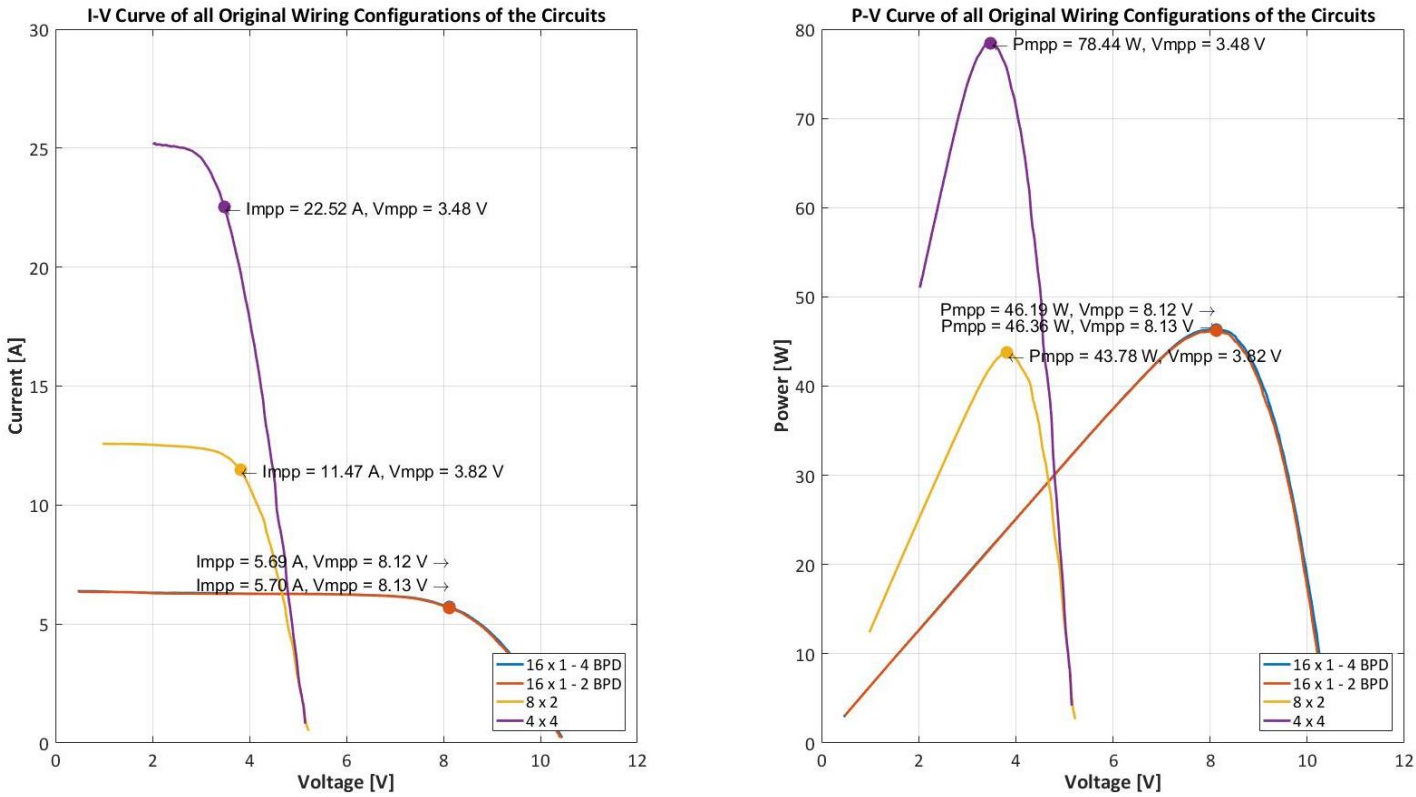


Figure 43: The Measured I-V and P-V Curves of the Three Wiring Configurations with BPDs.

4.2.3 Shading Configuration 3: Cell 1, 2, 3 and 4 are shaded

The red cells in Figure 44 refer to cells shaded with a shading factor of 0.45 and then 0.55. This shading configuration will activate bypass diodes and is considered to investigate how the longer strings of the 16 x 1 and 8 x 2 wiring configurations will perform when one quarter and half of the wiring configuration, respectively, are shaded.

Figure 44: Shading Configuration 3 Illustrated.

4.2.3.1 With Shading Factor (SF) of 0.45

The simulations results in Figure 45 show that the 4 x 4 wiring configuration will perform the best as expected however the 16 x 1 with 4 BPDs appears to perform as well as the 8 x 2 since it can bypass the substring with the shaded cells. Conversely, the 16 x 1 with 2 BPDs performs the worst since the BPD will cause 8 cells to be bypassed.

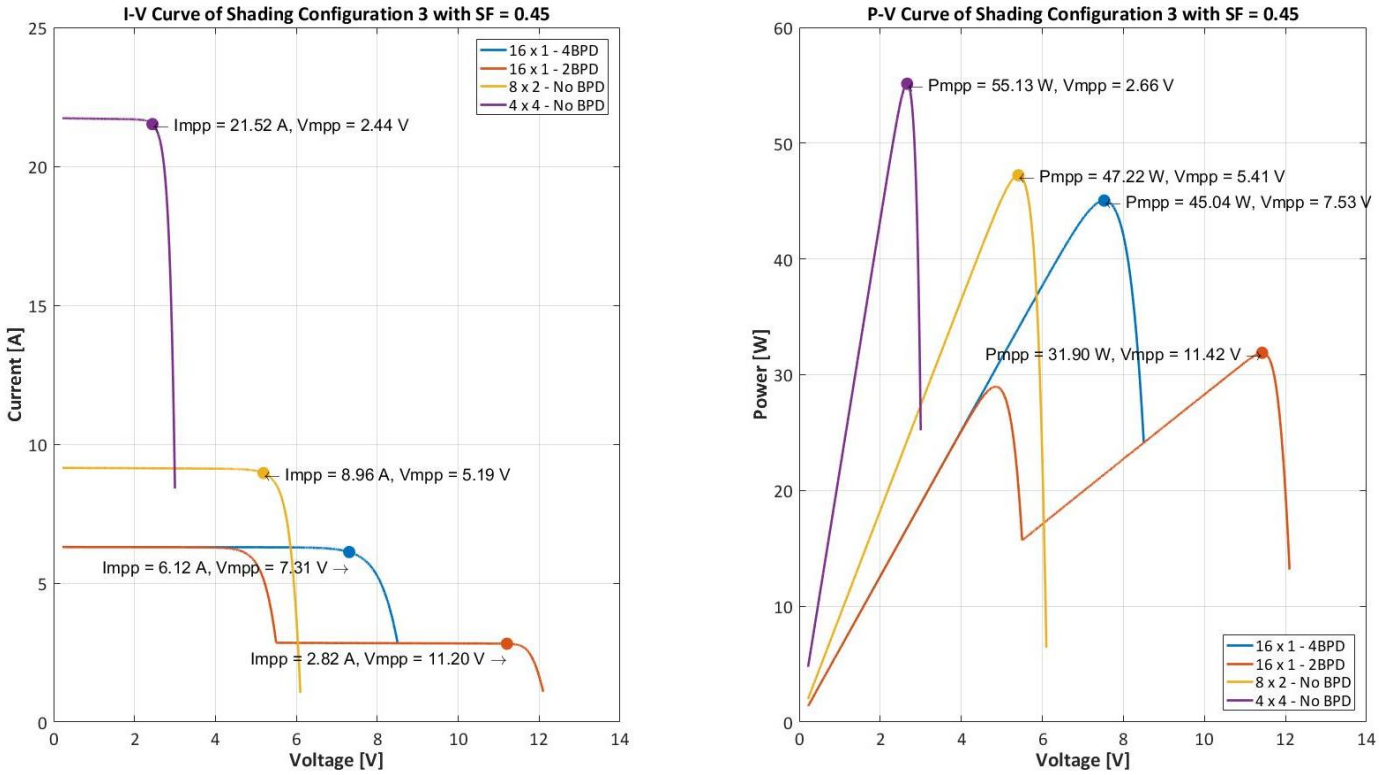


Figure 45: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 3 and Shading Factor 0.45.

When the panel is measured and the results displayed in Figure 46, the 4 x 4 wiring configuration is found to have a P_{mpp} of 36.84 W which though higher is only 2.5 W higher than the 8 x 2 and 16 x 1 with 4 BPDs wiring configurations. This can be explained by the values selected to estimate the cell's series and shunt resistances were too low and the conductor and cable losses were not considered in the simulation.

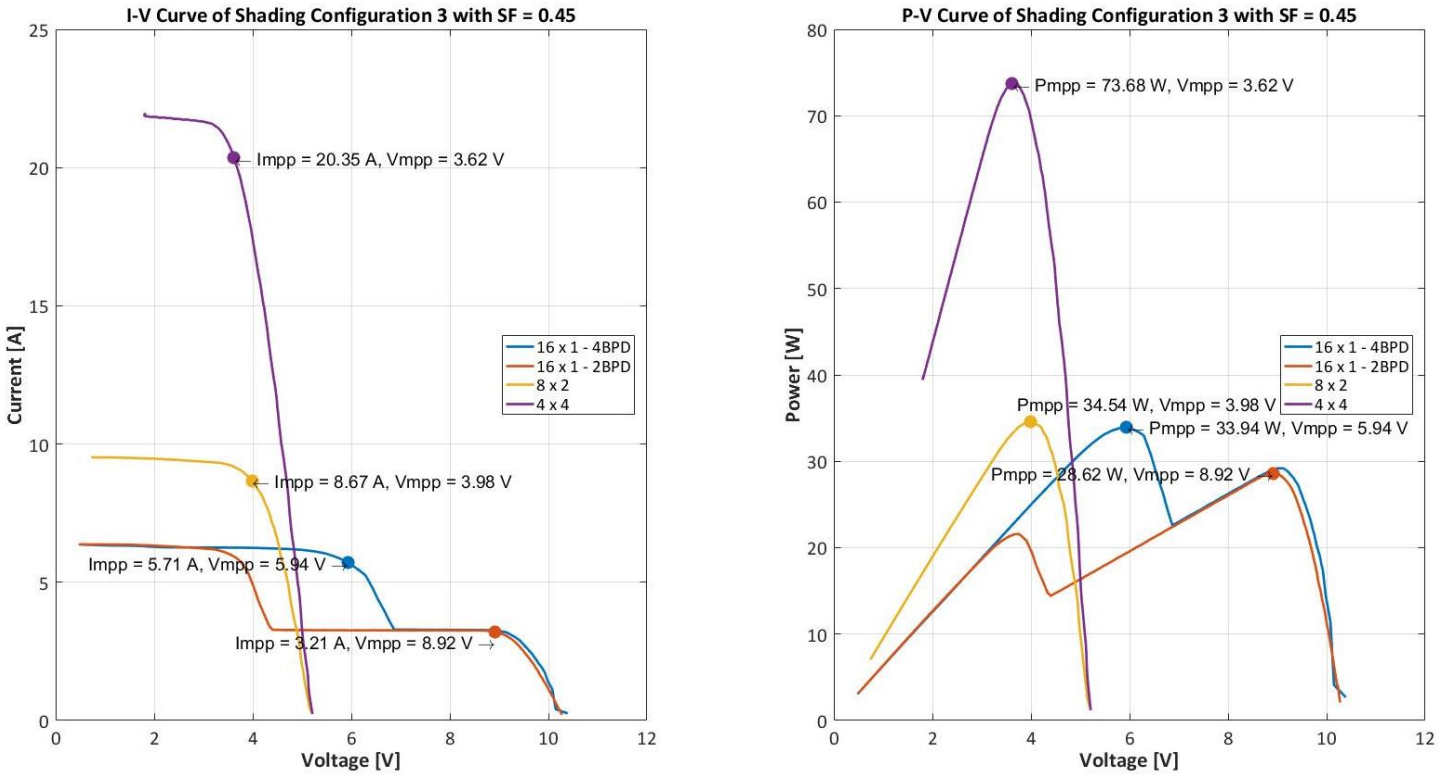


Figure 46: The Measured I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 3 and Shading Factor 0.45.

4.2.3.2 With Shading Factor (SF) of 0.55

Simulations were performed for a higher shading factor in Figure 47 and there was a greater distinction in maximum power output for the 8 x 2 over the 16 x 1 with 4 BPDs. The 4 x 4 and 8 x 2 are better for maximizing power output at greater shading level in this shading configuration.

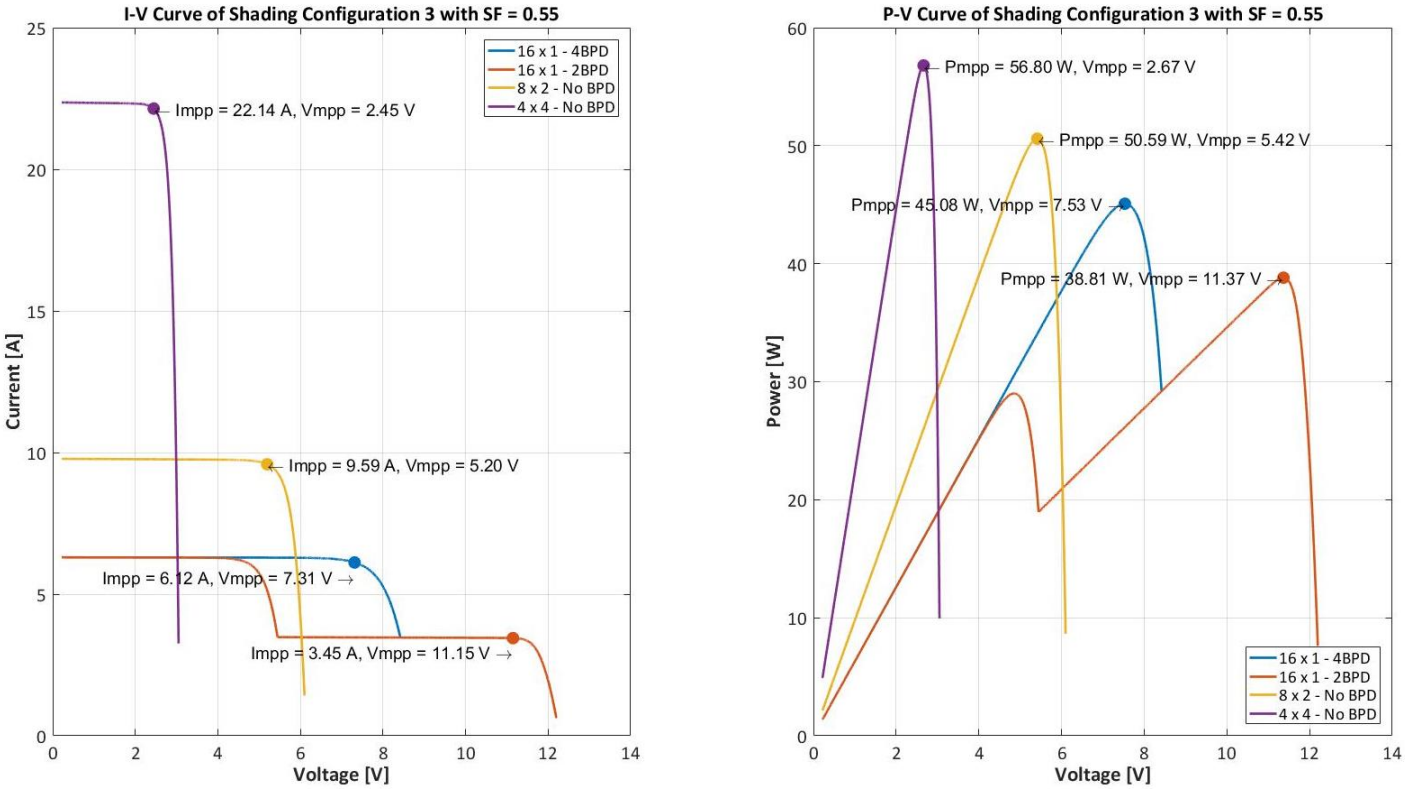


Figure 47: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 3 and Shading Factor 0.55.

The panel was measured and the results presented in Figure 48. The 4 x 4 wiring configuration has a maximum output power of 35.80 W and this is marginally better (by 1.93 W) over the maximum power point of the 16 x 1 with 4 BPDs which has the next best power output.

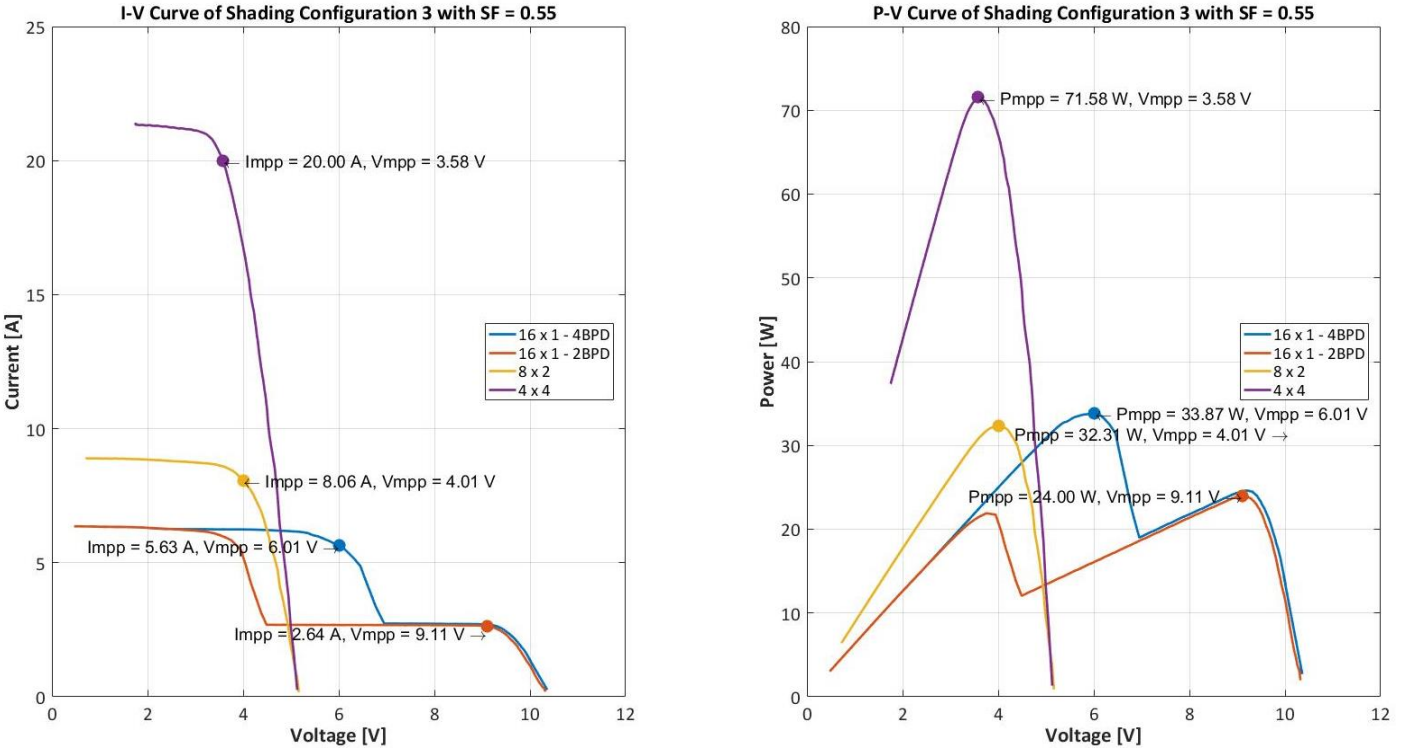


Figure 48: The Measured I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 3 and Shading Factor 0.55.

4.2.4 Shading Configuration 4: Cell 1, 5 and 9 are shaded

This shading configuration in Figure 49, should not activate bypass diodes since only one cell is affected in three substrings and is considered to investigate how the longer strings of the 16 x 1 and 8 x 2 wiring configurations will perform when they experience changes in shading factors of 0.45 and then 0.55.

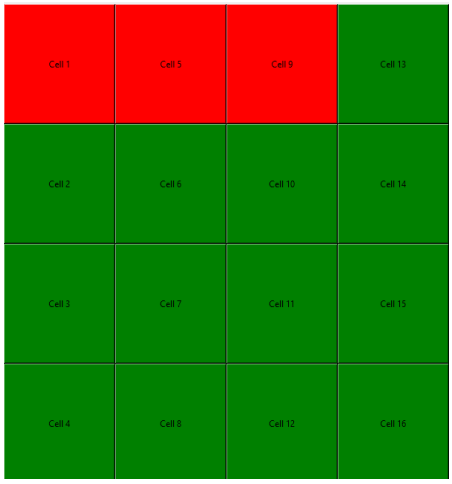


Figure 49: Shading Configuration 4 Illustrated.

4.2.4.1 With Shading Factor (SF) of 0.45

The results from the simulation are presented in Figure 50 and it can be seen that in this shading configuration that the 8 x 2 and the two 16 x 1 wiring configurations all have similar power outputs. The 4 x 4 still has the greater shading tolerability by having the highest power output.

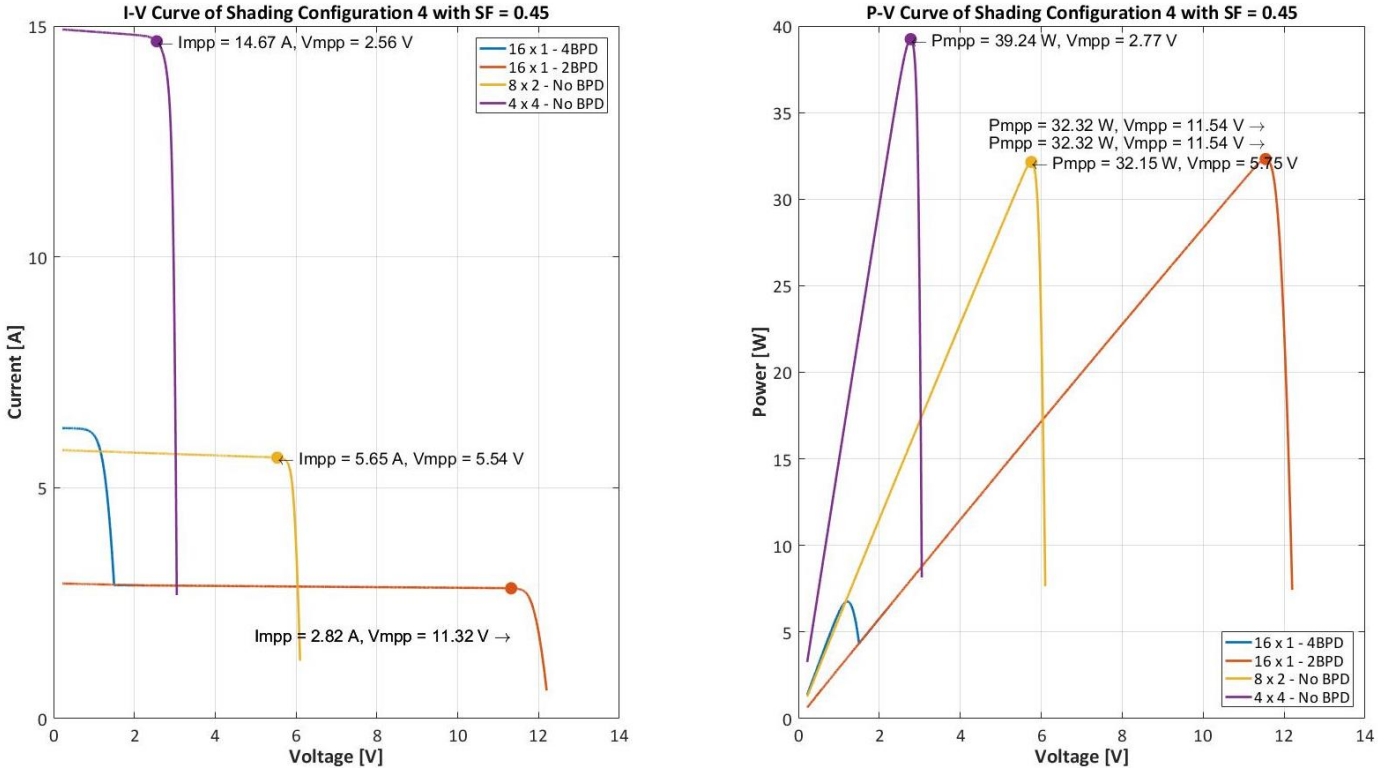


Figure 50: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 4 and Shading Factor 0.45.

The results from panel measurement are displayed in Figure 51. The 4 x 4 wiring configuration has a maximum power point of 30.08 W and this is very similar to that of the 8 x 2 and both of the 16 x 1 wiring configurations. Shading configuration 4 can thus utilise all wiring configurations since

it shades three out of the four substrings, thus decreasing the power output of the panel almost evenly.

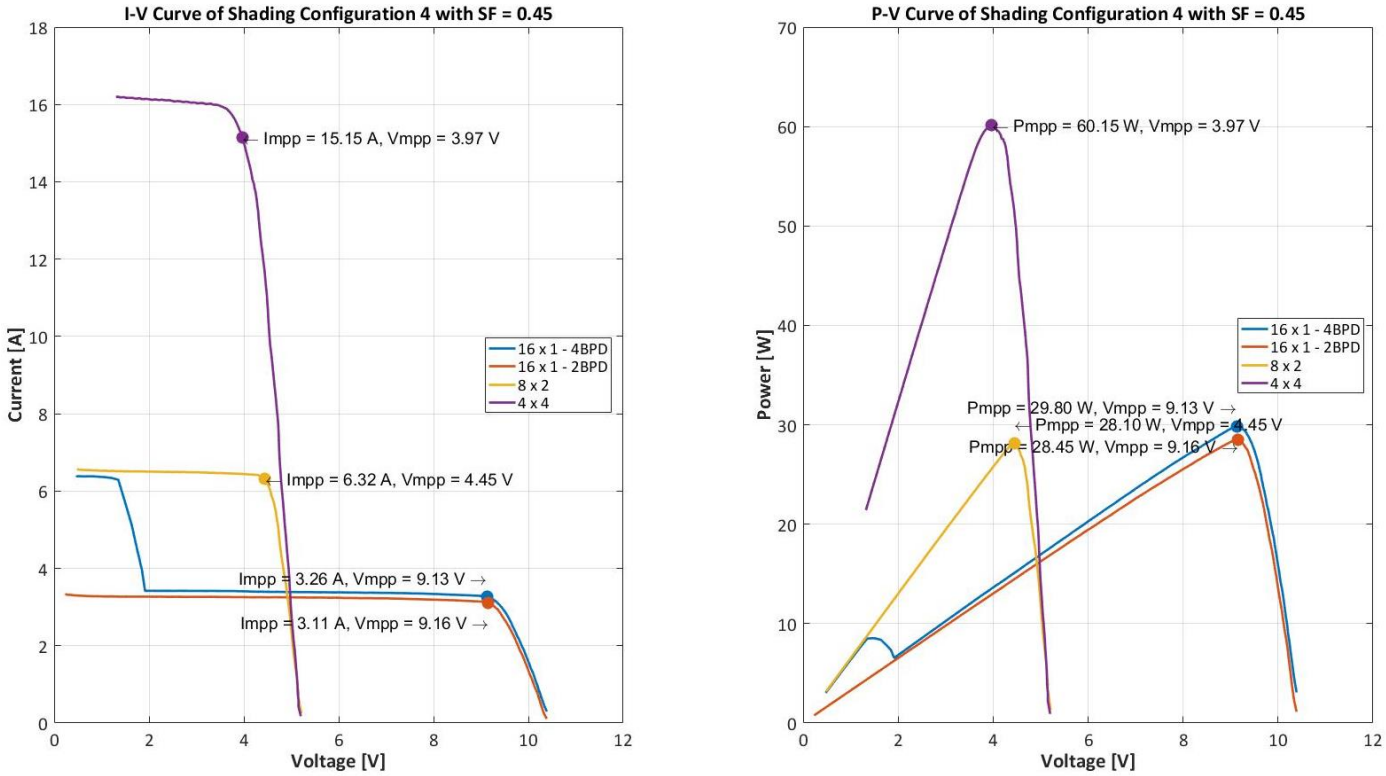


Figure 51: The Measured I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 4 and Shading Factor 0.45.

4.2.4.2 With Shading Factor (SF) of 0.55

The simulation results now have their shading factor increased to 0.55 in Figure 52. Despite differences between other shading configurations when the shading factor is increased, the performance of the 8 x 2 and 16 x 1 are still comparative in these results.

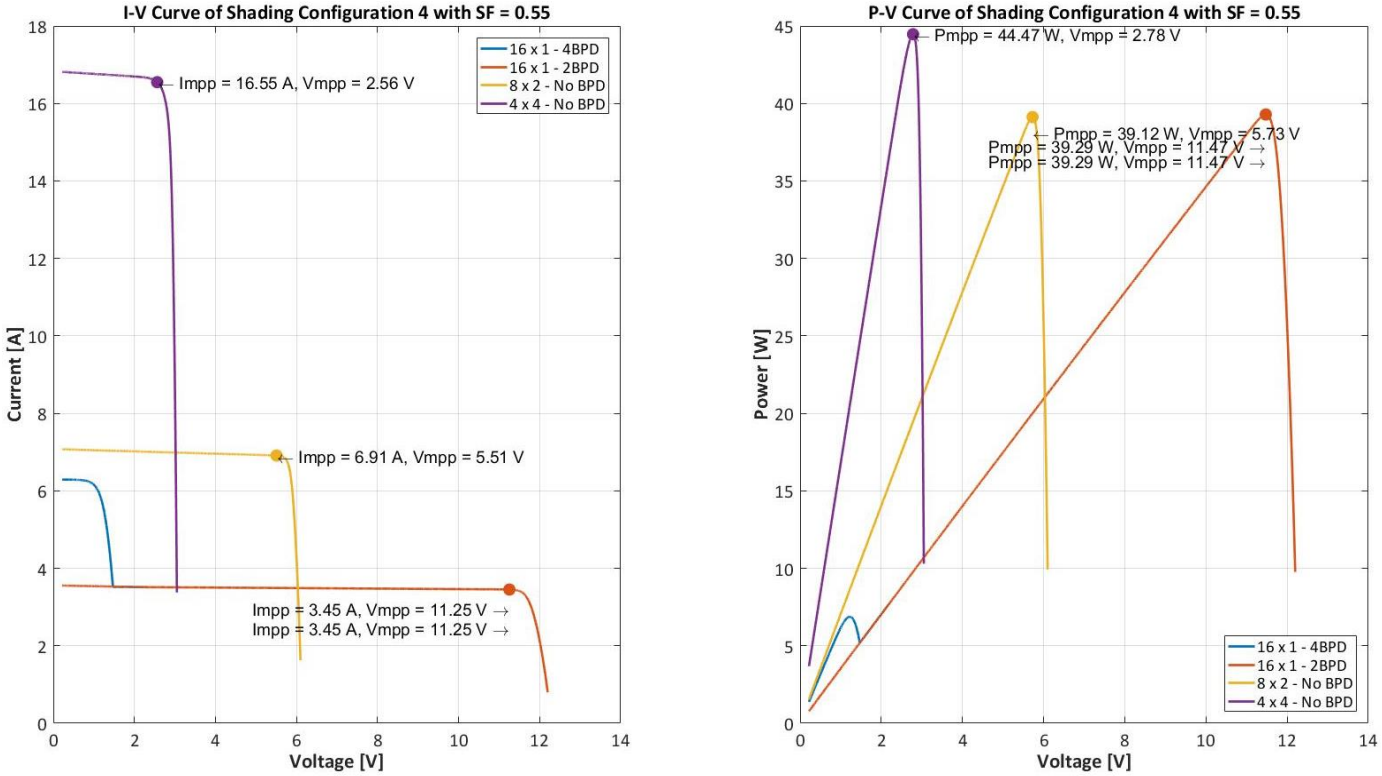


Figure 52: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 4 and Shading Factor 0.55.

The panel measurement results are displayed in Figure 53 and the maximum power point for the 4 x 4 configuration found to be 27.21 W. The 4 x 4 wiring configuration is only marginally better than the next best configuration which is the 16 x 1 with 4 BPDs. The 8 x 2 and the 16 x 1 with 2 BPDs perform similarly to each other and this is due to both having one cell in the second substring for the 8 x 2 and on cell in the substring with the second BPD being shaded.

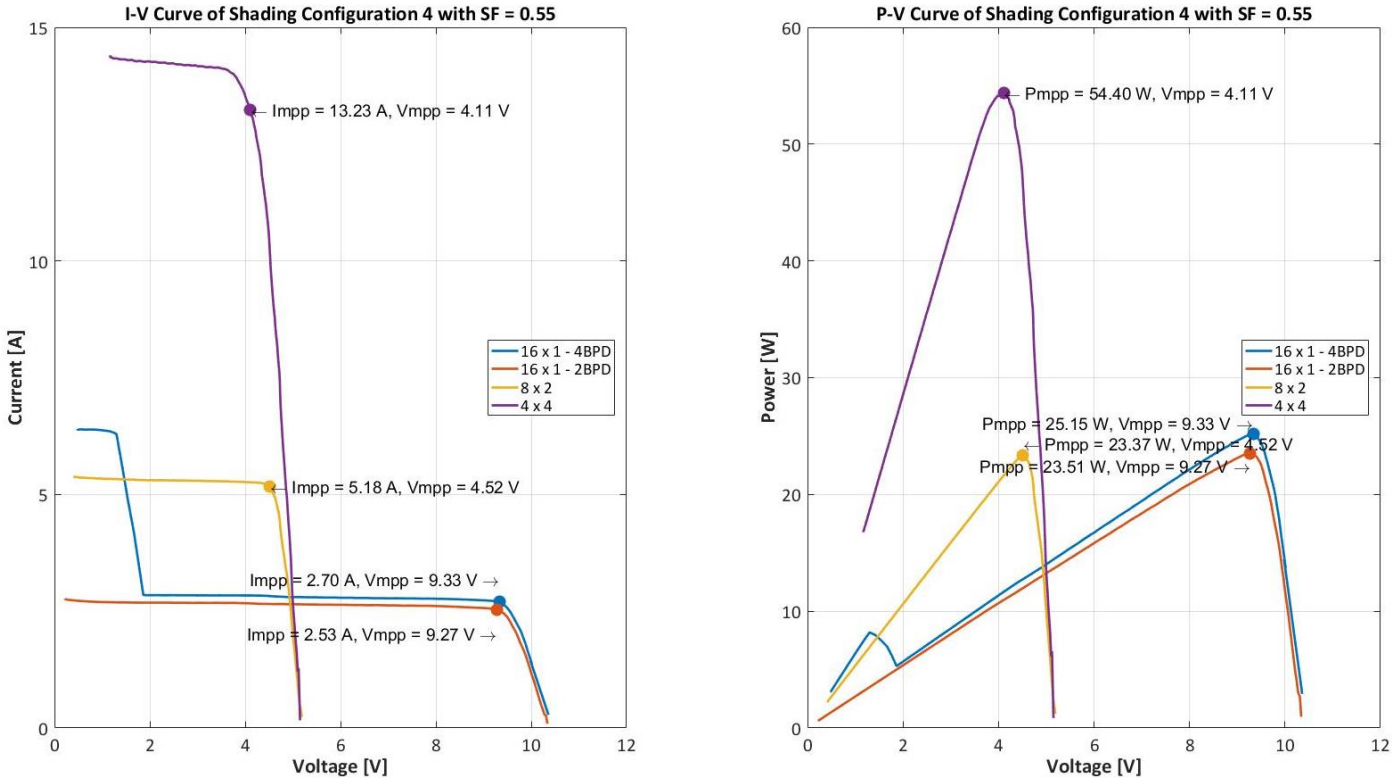


Figure 53: The Measured I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 4 and Shading Factor 0.55.

4.2.6 Shading Configuration 6: Cell 1, 2, 3, 5, 6 and 9 are shaded

The shading configuration in Figure 54, should activate some bypass diodes since several cells are affected across three substrings and will help determine which wiring configuration will perform the best when the shading factors are 0.45 and then 0.55. This shading configuration will prove that the 4 x 4 wiring configurations is the most shading tolerant since three of the four substrings are affected by shading.

Figure 54: Shading Configuration 6 Illustrated.

4.2.6.1 With Shading Factor (SF) of 0.45

The simulation results are shown in Figure 55 for this shading configuration and because of the non-symmetrical shading across three of the four strings forming the panel. The 4 x 4 wiring configuration appears to be the best with the highest power output and the 8 x 2 and 16 x 1 wiring configurations showing similar power outputs.

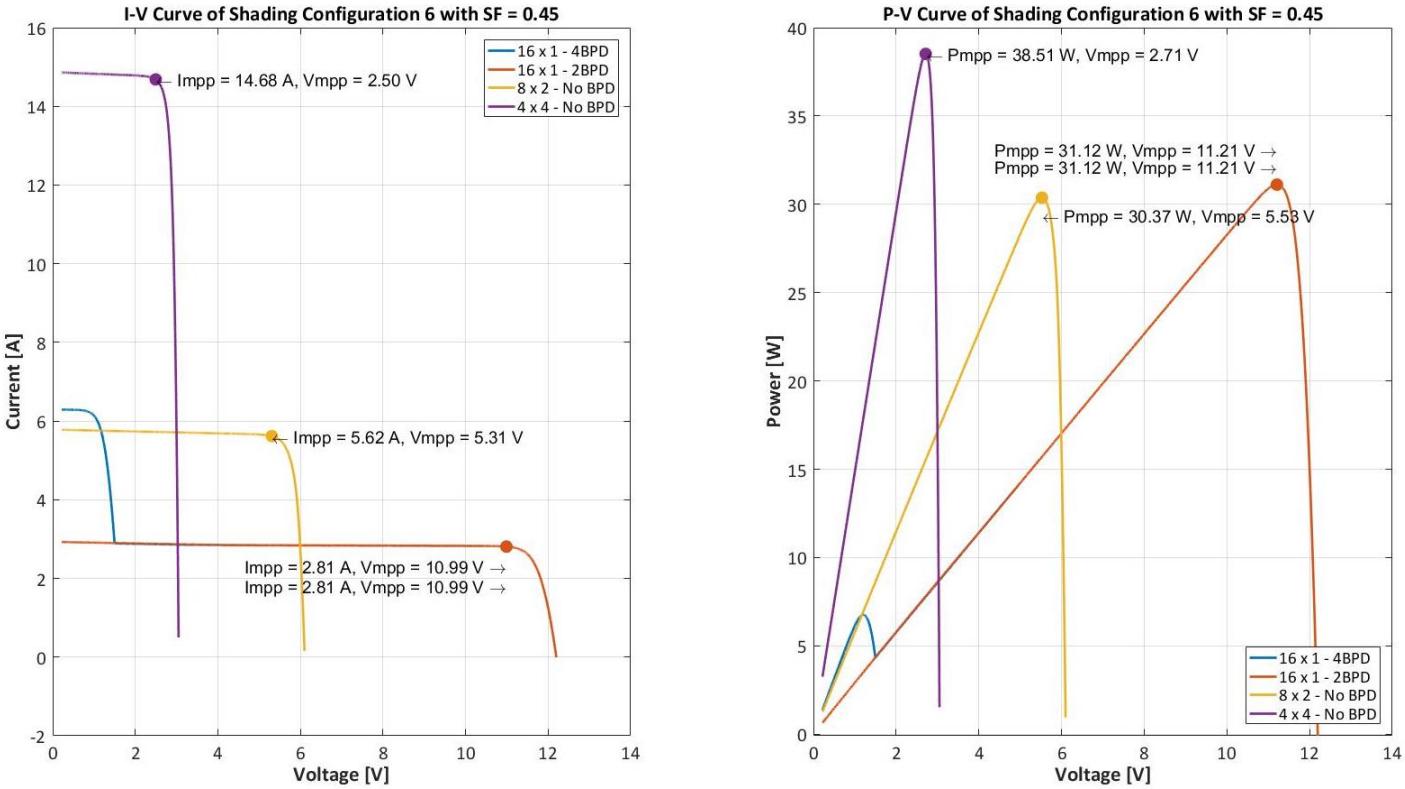


Figure 55: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 6 and Shading Factor 0.45.

The panel was then measured and the results plotted in Figure 56 to compare simulation and actual measurements and it was found that the 4 x 4 wiring configuration with a maximum power point of 30.39 W had a higher power output by 2.20 W than that of the 16 x 1 with 4 BPDs of 28.19 W with the 16 x 1 with 2 BPDs and the 8 x 2 soon following.

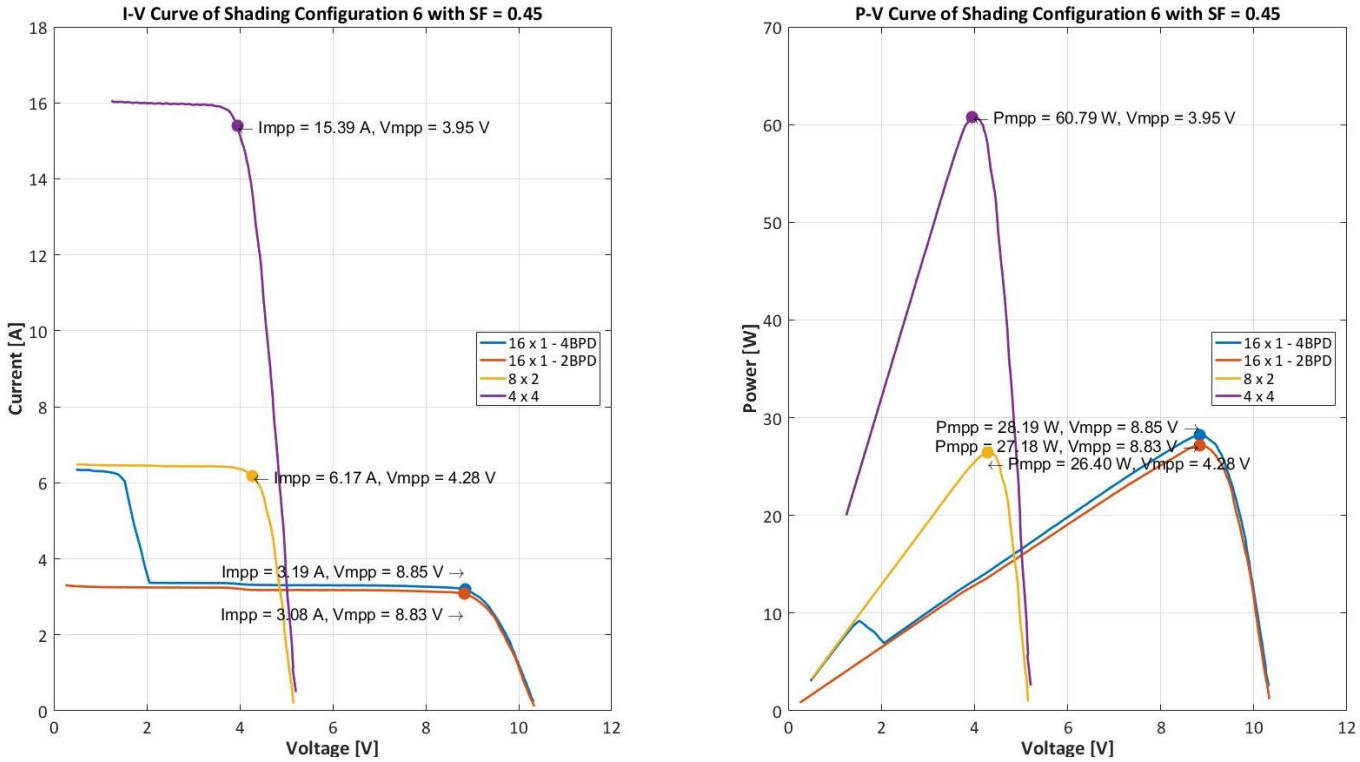


Figure 56: The Measured I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 6 and Shading Factor 0.45.

4.2.6.2 With Shading Factor (SF) of 0.55

The simulation results for the increased shading factor of 0.55 is presented in Figure 57. The higher shading still results in the 4 x 4 wiring configuration having a higher power output, however now the 16 x 1 configurations are more dominant in terms of power output than the 8 x 2 which was dominant under the shading factor of 0.45.

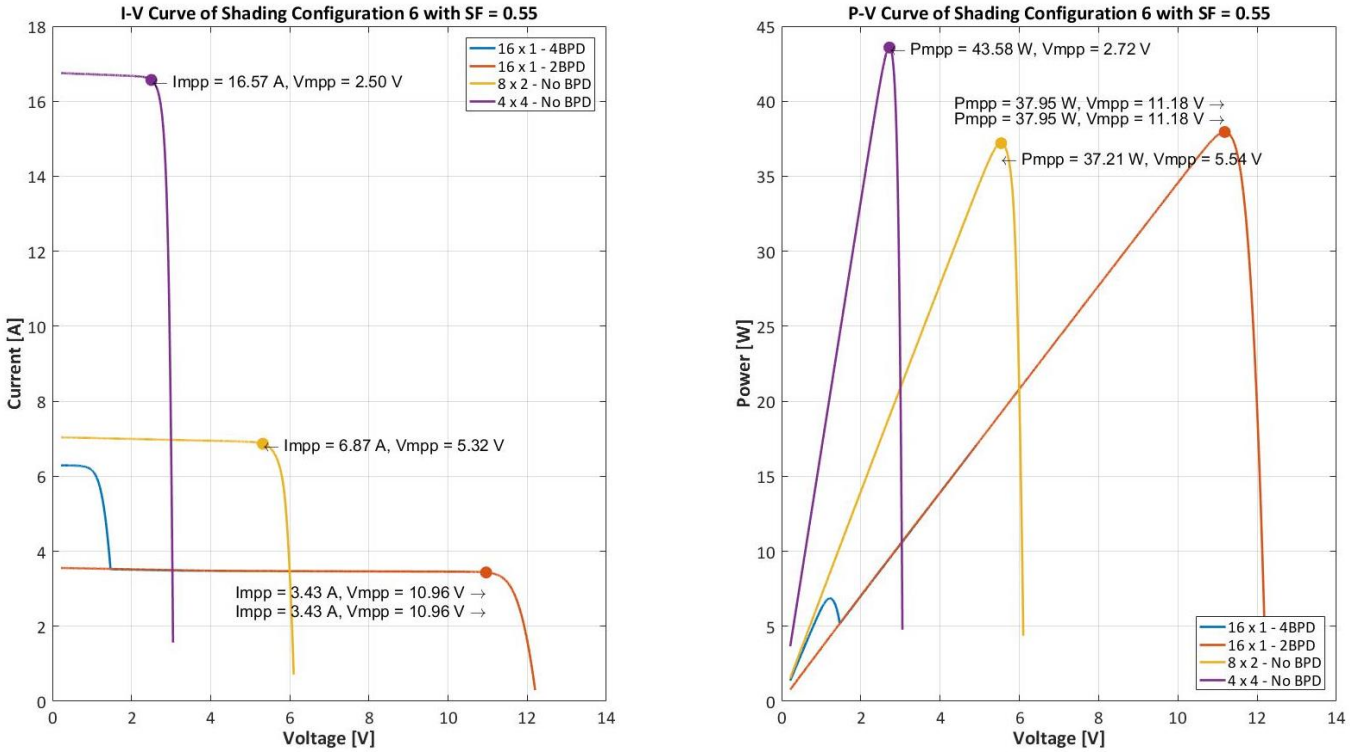


Figure 57: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 6 and Shading Factor 0.55.

The measurements of the panel are shown in Figure 58 and the highest power output was from the 4 x 4 wiring configuration with a maximum power point of 27.08 W. This was found to be

4.58 W higher than the next wiring configuration of 16 x 1 with 4 BPDs. The measured results agreed with the simulation results, that the 16 x 1 configurations were better than the 8 x 2 at a shading factor of 0.55.

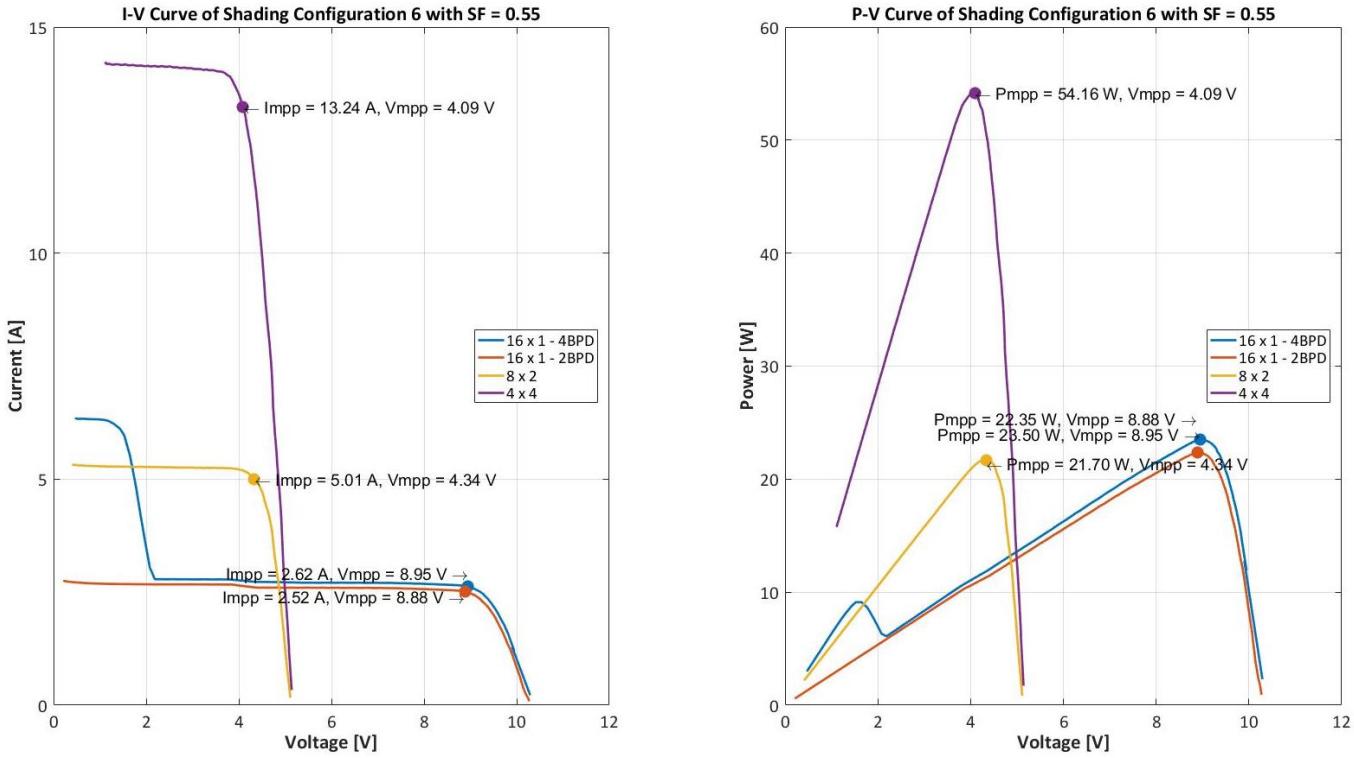


Figure 58: The Measured I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 6 and Shading Factor 0.55.

4.2.7 Extra Testing with Shading Configuration 2: Cell 1 and 2 are shaded

A final test was done with the results displayed in Figure 59 to compare BPD types between the Smart Bypass Diodes SM74611 from Texas Instruments and the Schottky Barrier Rectifier DST2045AX. This comparison looked to determine which was a better diode choice and it found that the latter the Schottky Barrier Rectifier performed better in the shading configuration 2 and had a maximum power point of 1.32 W higher than the smart BPDs.

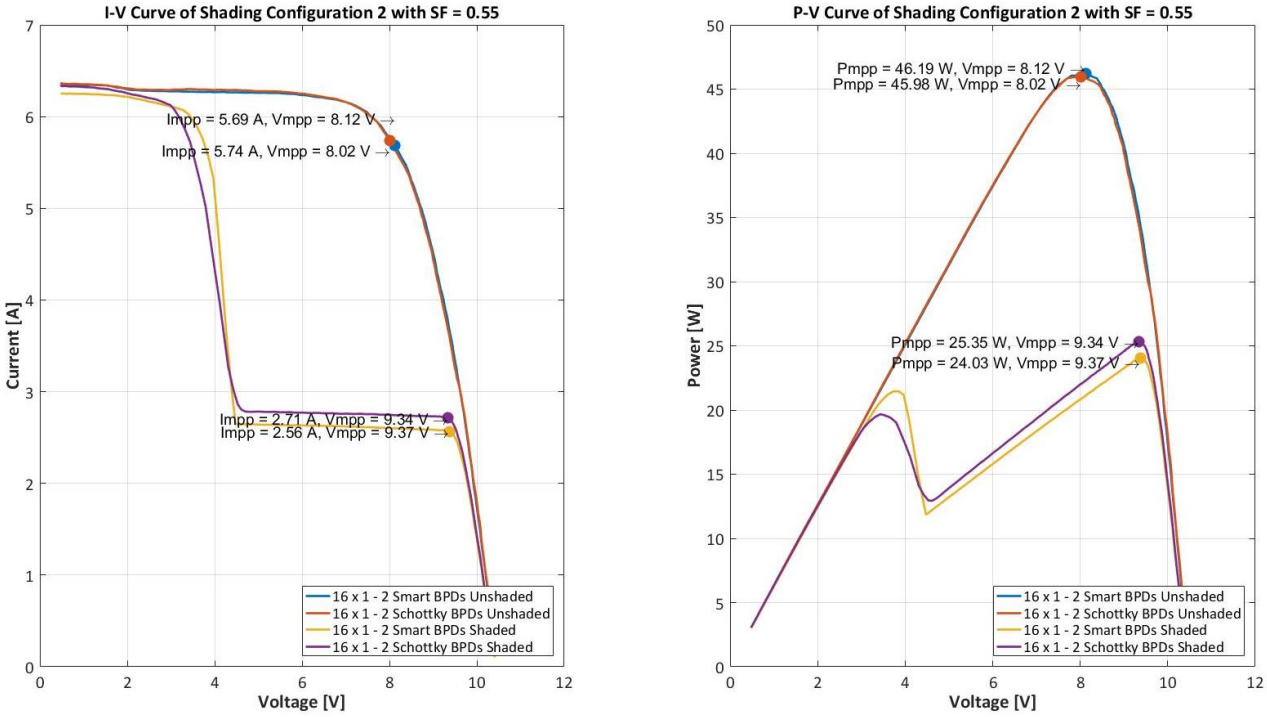


Figure 59: Extra Testing with Shading Configuration 2 to compare two bypass diode options.

4.3. The Results from the Circuit Testing

The tests conducted previously were done manually by changing the wiring configurations to validate the simulations. In this section a circuit was designed and implemented in Simulink and a select few of the shading configurations of 3, 4 and 6 were repeated first with simulations and then using the circuit that was later built. A comparison of the unshaded simulated panel and then the panel were measured, both with the circuit. The results presented in Figure 60 and 61.

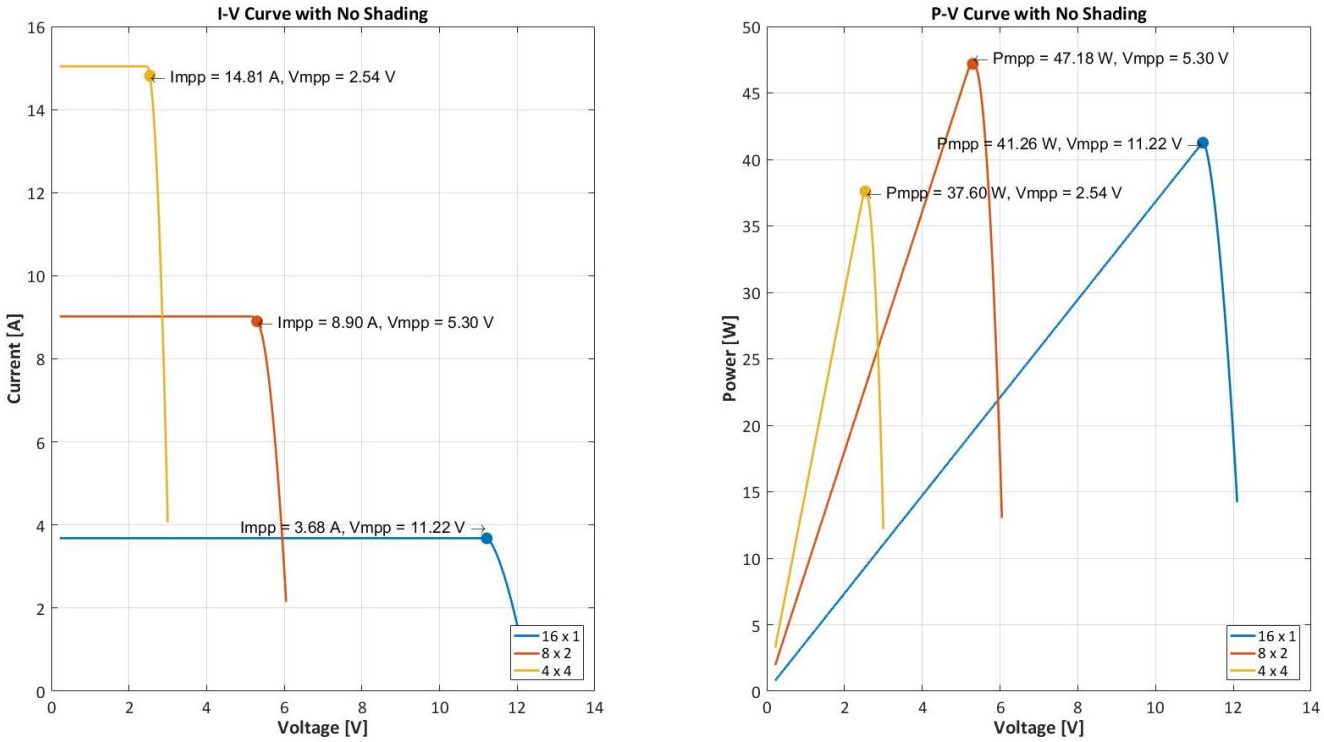


Figure 60: The Simulation I-V and P-V Curves of the Three Wiring Configurations with the Circuit

The panel measurements were drastically different compared to the simulations and this can be explained by two occurrences. The first is that there was large power dissipation across the Schottky diodes (see section 3.9) and secondly the 8 x 2 wiring configuration malfunctioned during measurement because current from one string of eight cells leaked into its adjacent string reducing the maximum power measured by half (P_{mpp} of 28.06 W). The 4 x 4 wiring configuration had a maximum power point of 21.16 W which was comparative to the measured 16 x 1 configuration.

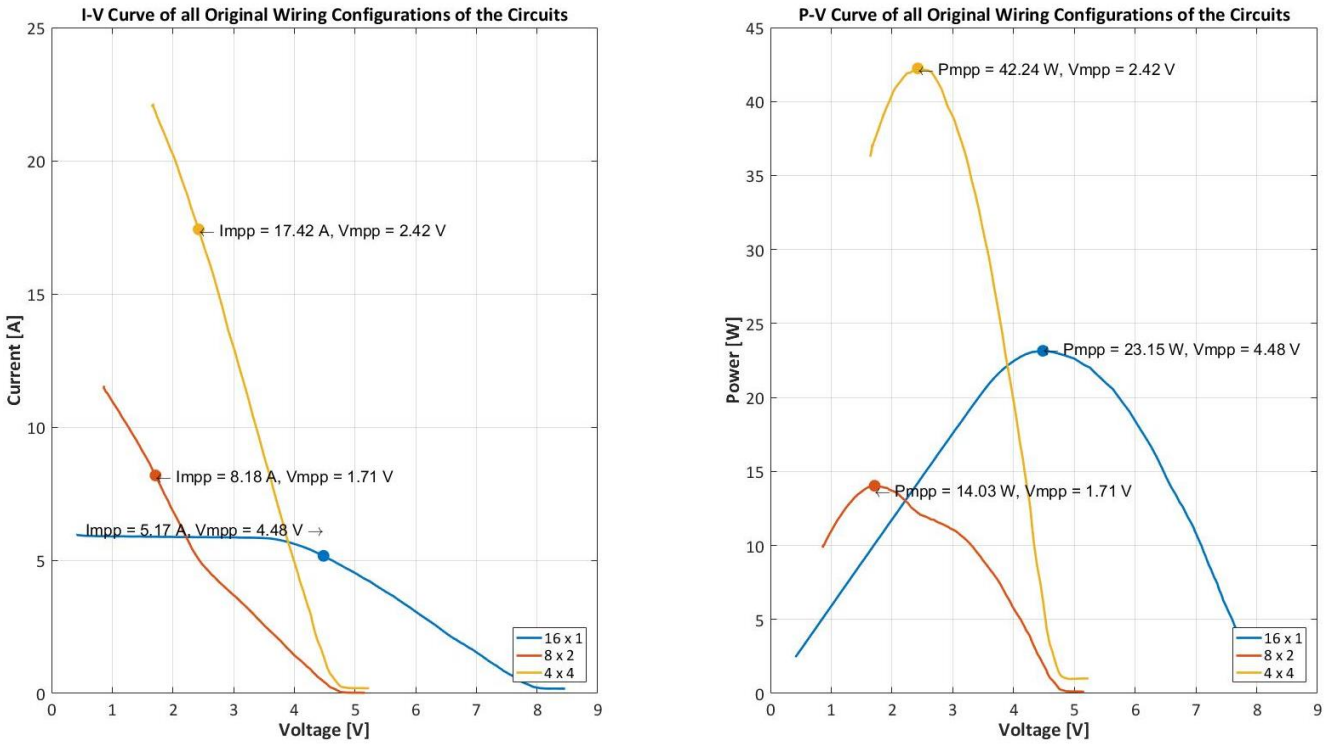


Figure 61: The Measured I-V and P-V Curves of the Three Wiring Configurations with the Circuit

4.3.1 Shading Configuration 3: Cell 1, 2, 3 and 4 are shaded

The shading configuration shown in Figure 62 will remove power from an enitre substring of four cells and is considered to investigate how the longer strings of the 16 x 1 and 8 x 2 wiring configurations will perform when one quarter and half of the wiring configuration, respectively, are shaded.

Figure 62: Shading Configuration 3 Illustrated.

4.3.1.1 With Shading Factor (SF) of 0.45

The 8 x 2 wiring configuration will be able to produce the most maximum output power as a result of this shading configuration as seen in the simulation results in Figure 63.

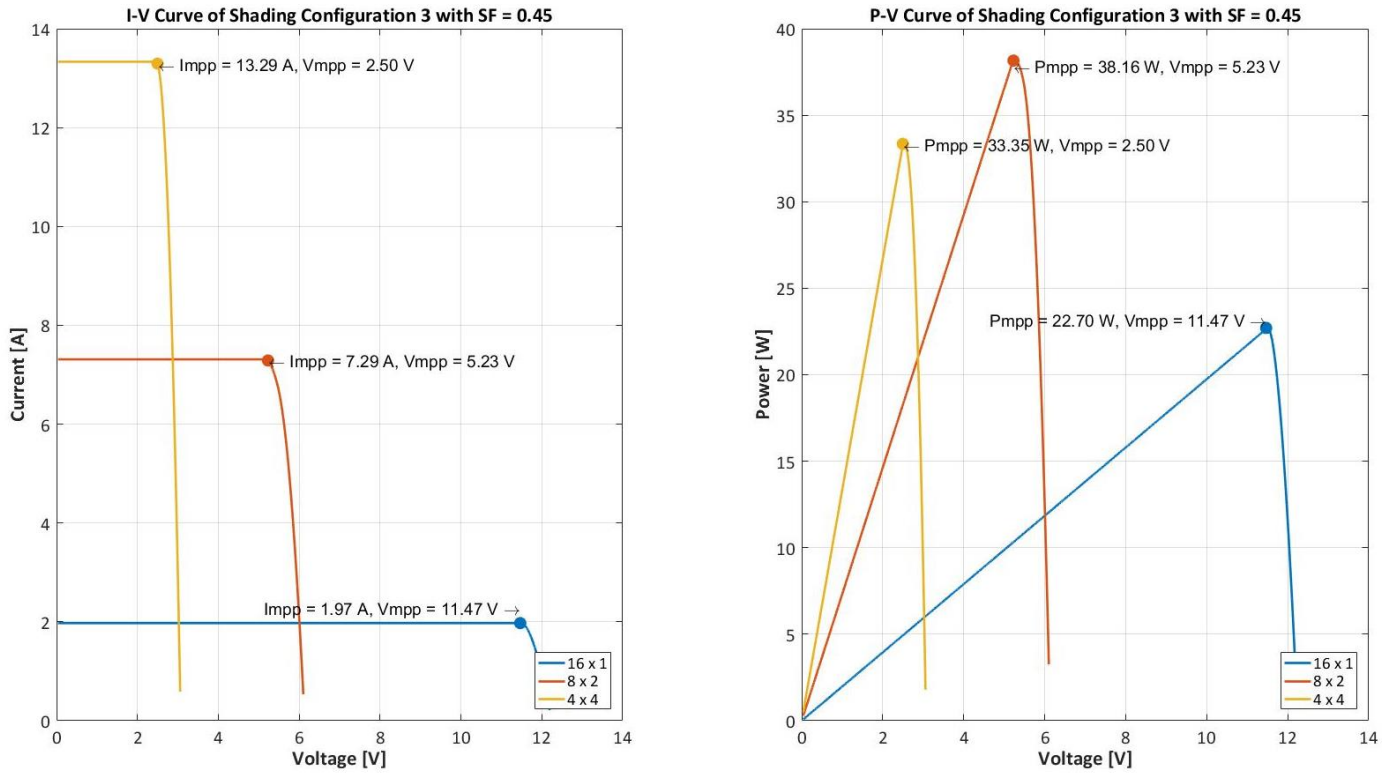


Figure 63: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Circuit, Shading Configuration 3 and Shading Factor 0.45.

The panel was then measured using the circuit and the results shown in Figure 64. It was found that the 4 x 4 wiring configuration had a P_{mpp} of 19.61 W, the 8 x 2 a P_{mpp} of 28.54 W and 18.02 W for the 16 x 1. The lower values for the 4 x 4 and 16 x 1 are again due to power dissipation in the Schottky blocking diodes employed.

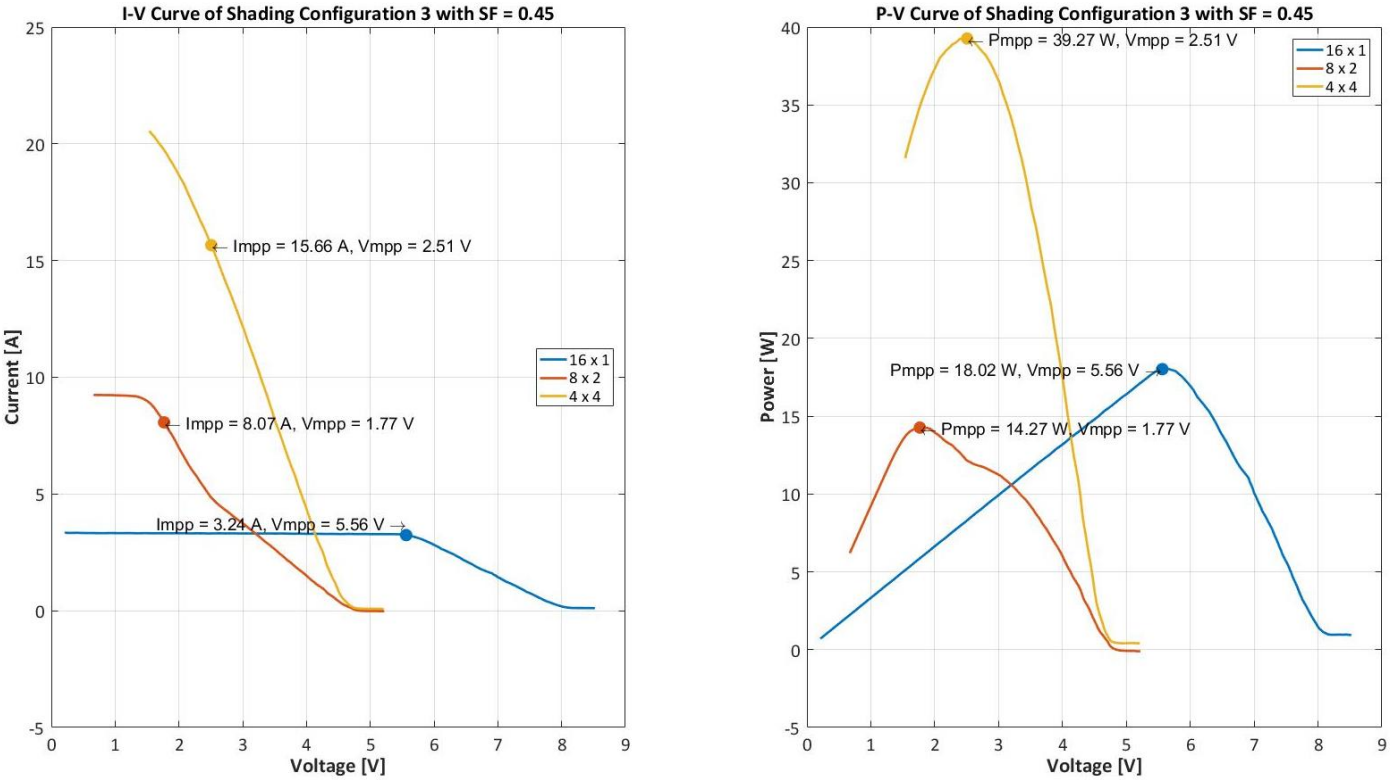


Figure 64: The Measured I-V and P-V Curves of the Three Wiring Configurations with Circuit, Shading Configuration 3 and Shading Factor 0.45.

4.3.1.2 With Shading Factor (SF) of 0.55

The results from the simulation are presented in Figure 65 and the 8 x 2 wiring configuration is still expected to perform better followed by the 4 x4 and 16 x 2.

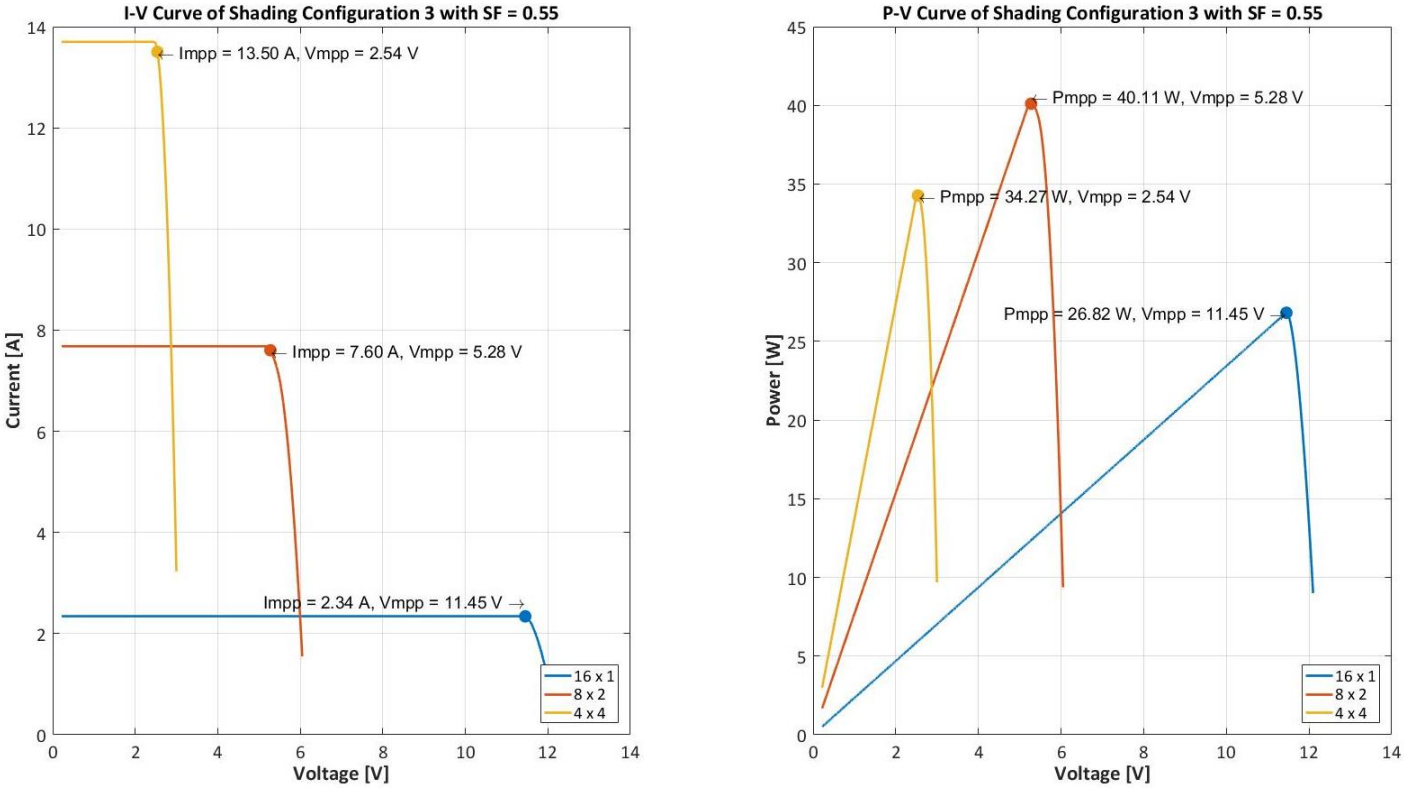


Figure 65: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Circuit, Shading Configuration 3 and Shading Factor 0.55.

The panel with the circuit was measured and the results presented in Figure 66. The 8 x 2 is expected to have 27.08 W at its maximum power point, the 4 x 4 have 19.14 W and thus be higher 3.21 W than the P_{mpp} of the 16 x 1 wiring configuration.

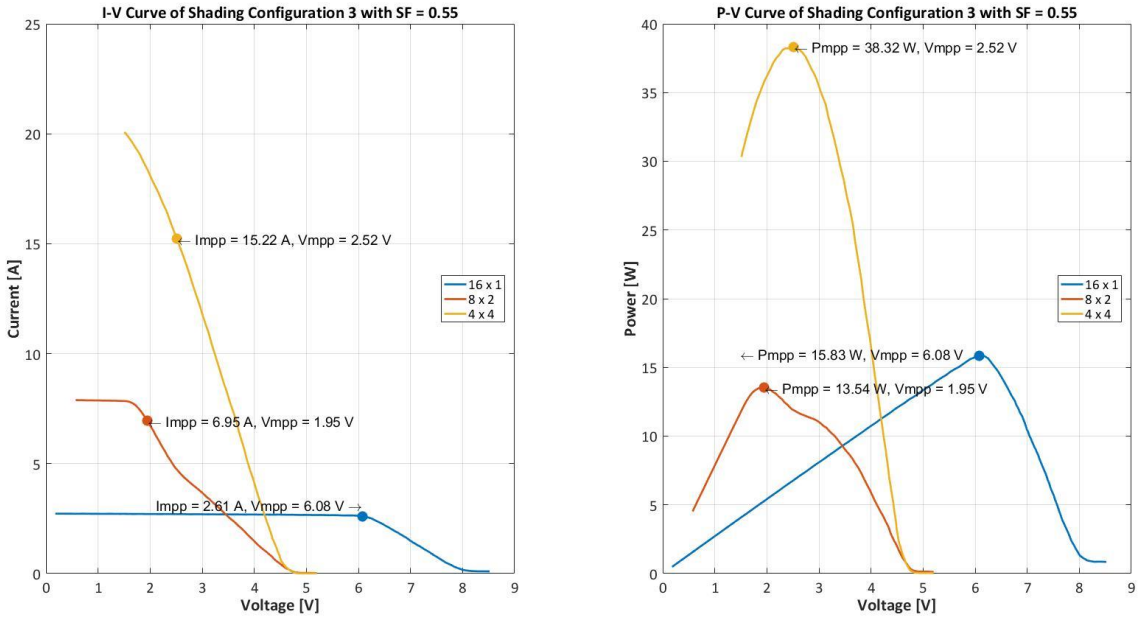


Figure 66: The Measured I-V and P-V Curves of the Three Wiring Configurations with Circuit, Shading Configuration 3 and Shading Factor 0.55.

4.3.2 Shading Configuration 4: Cell 1, 5 and 9 are shaded

This shading configuration in Figure 67, has one cell affected in the three substrings and is considered to investigate how the longer strings of the 16 x 1 and 8 x 2 wiring configurations will perform when they experience changes in shading factors of 0.45 and then 0.55.

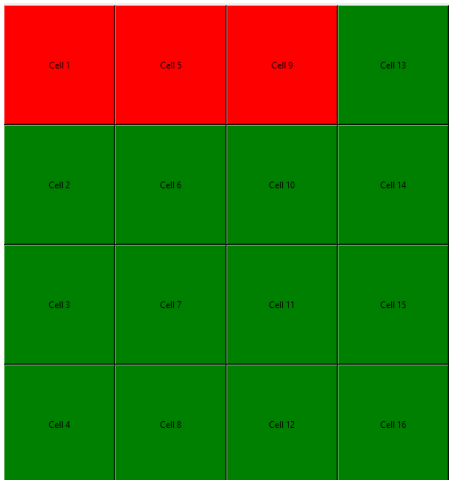


Figure 67: Shading Configuration 4 Illustrated.

4.3.2.1 With Shading Factor (SF) of 0.45

The simulation results in Figure 68, show that the maximum power point has a spread of 0.72 W and should be evenly affected as one cell in three of the four substrings is affected.

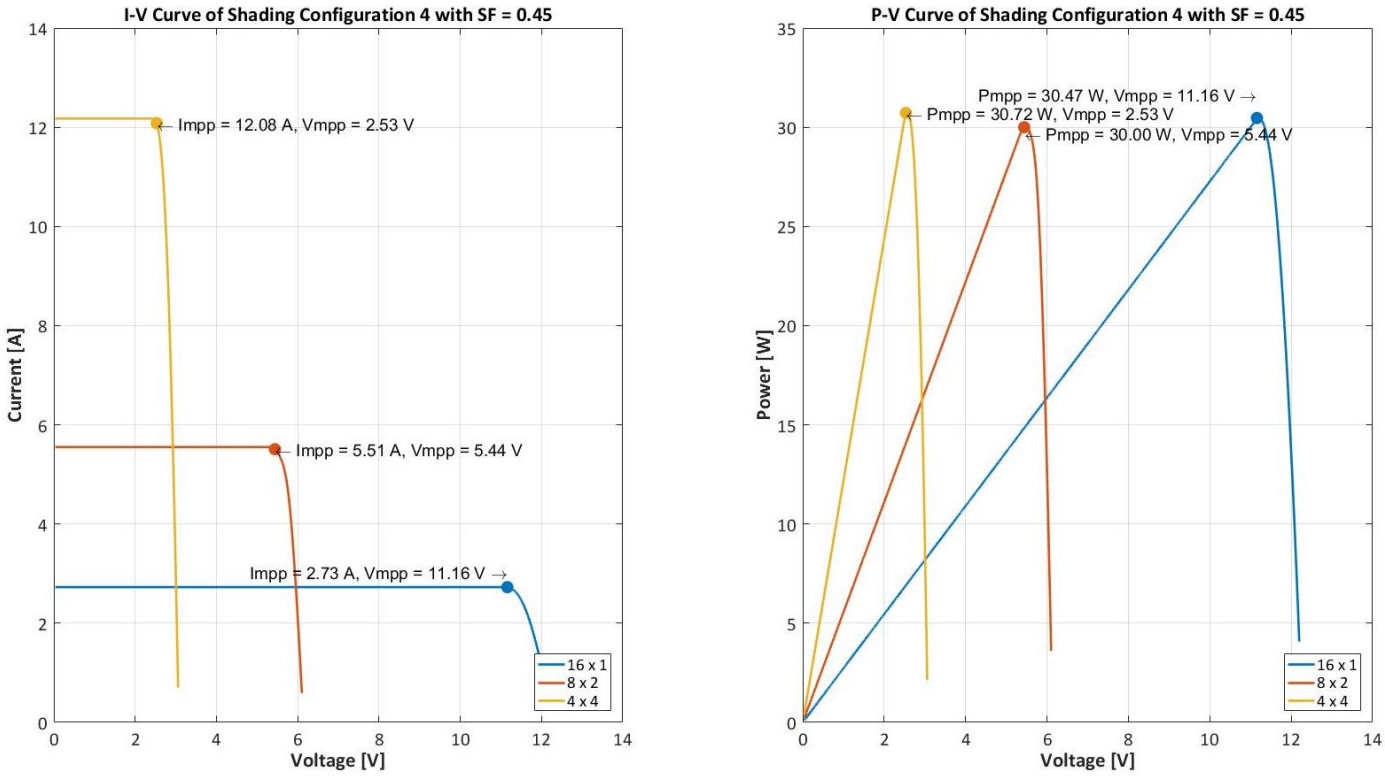


Figure 68: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Circuit, Shading Configuration 4 and Shading Factor 0.45.

The measurements from the panel using the circuit are presented in Figure 69. The 4 x 4 wiring configuration has a power output of 18.43 W, the 8 x 2 of 21.14 W and the 16 x 1 the lowest of 17.99 W the range in power is due to the resistances of the cables used to make measurements.

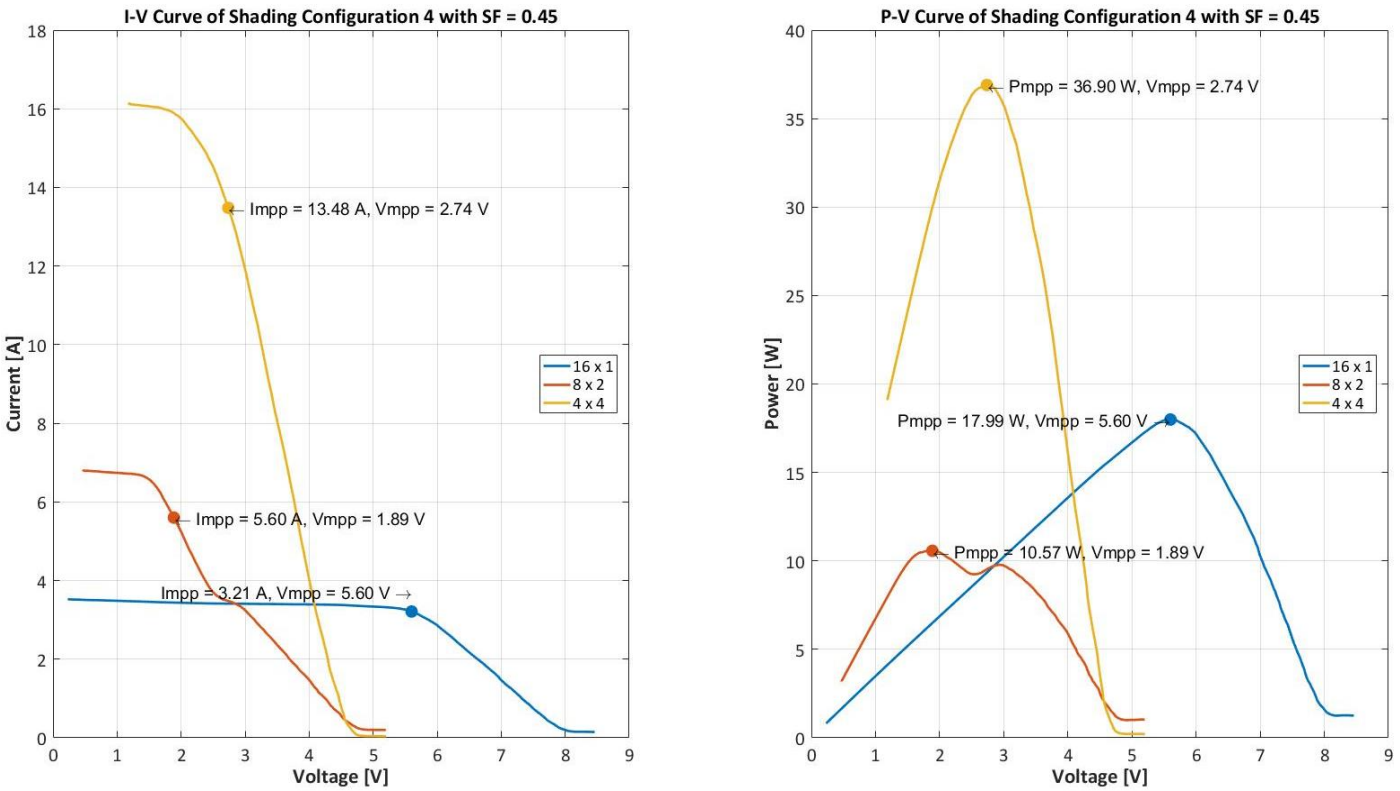


Figure 69: The Measured I-V and P-V Curves of the Three Wiring Configurations with Circuit, Shading Configuration 4 and Shading Factor 0.45.

4.3.2.2 With Shading Factor (SF) of 0.55

The simulation results when the shading factor is increased are displayed in Figure 70. The 8 x 2 configuration should again perform slightly better than the other two since it only three of its four, string of four cells is affected and thus able to supply marginally higher power than the 4 x 4.

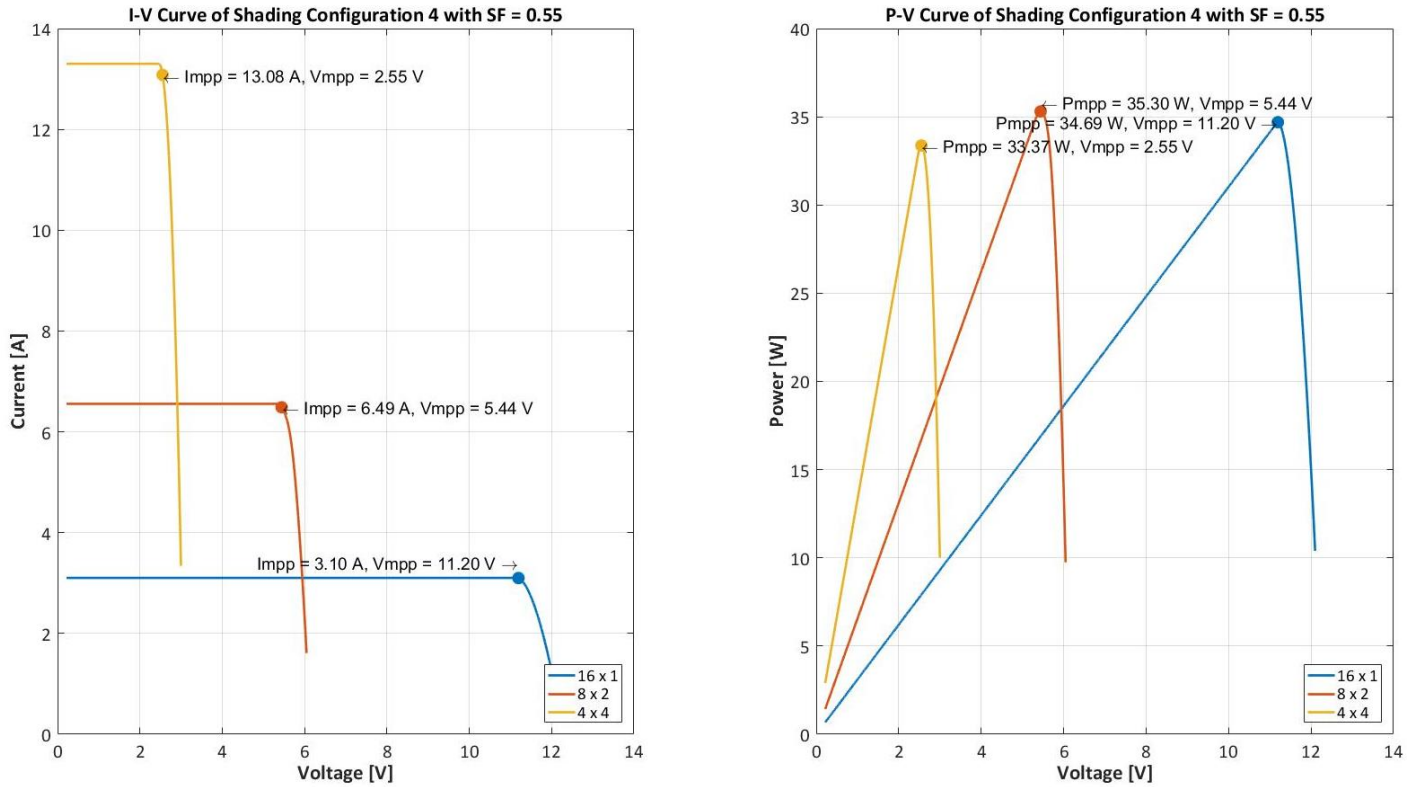


Figure 70: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 4 and Shading Factor 0.55.

The measurements with the circuit are presented in Figure 71 with the 4 x 4 wiring configuration having a maximum power output of 17.16 W, the 8 x 2 of 17.84 W and the 16 x 1 of 15.14 W. Thus the 8 x 2 still appears to be the better configuration.

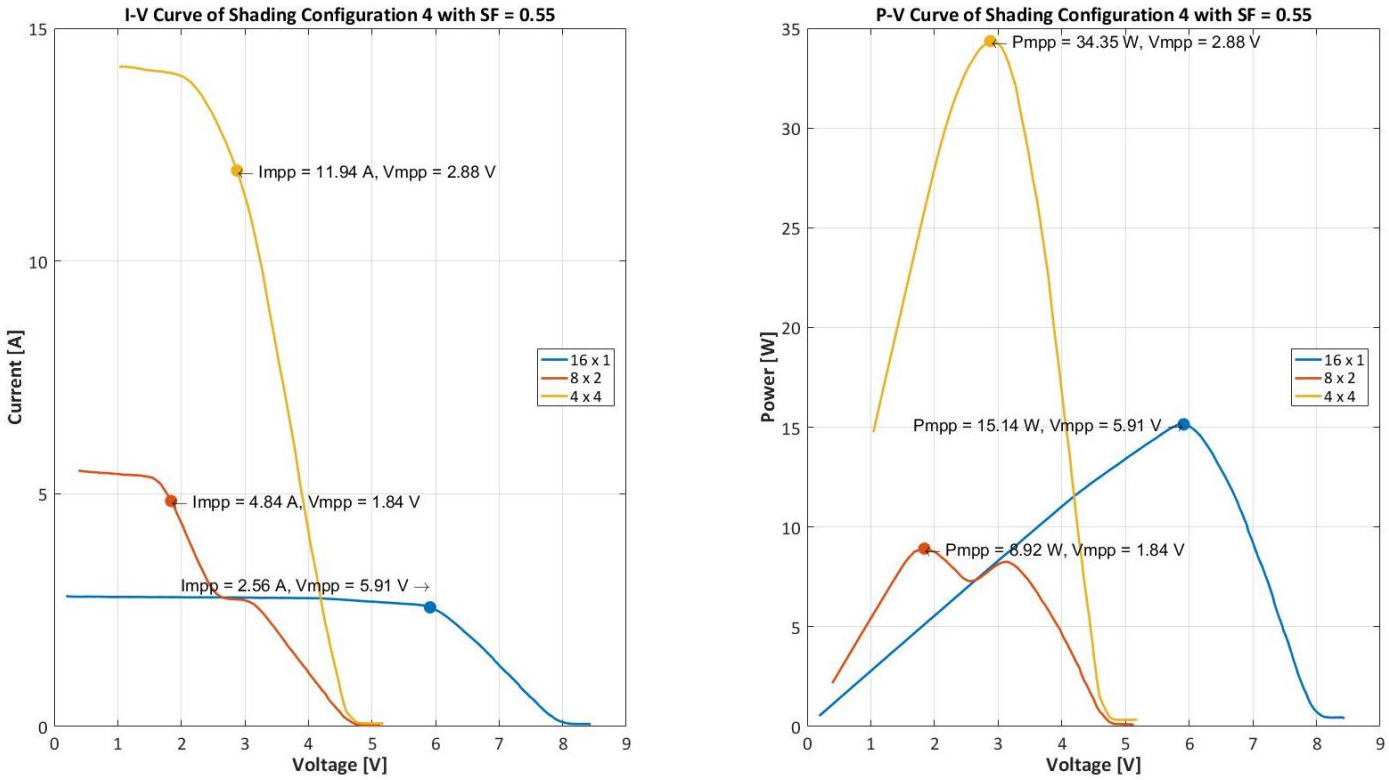


Figure 71: The Measured I-V and P-V Curves of the Three Wiring Configurations with Circuit, Shading Configuration 4 and Shading Factor 0.55.

4.3.3 Shading Configuration 6: Cell 1, 2, 3, 5, 6 and 9 are shaded

The shading configuration in Figure 72, should affect all wiring configurations since several cells are affected across three substrings and this will help determine which wiring configuration will perform the best when the shading factors are 0.45 and then 0.55. This shading configuration will prove that the 4 x 4 wiring configuration is the most shading tolerant since three of the four substrings are affected by shading.

Figure 72: Shading Configuration 6 Illustrated.

4.3.3.1 With Shading Factor (SF) of 0.45

The simulation results for this shading configuration are presented in Figure 73. The 4 x 4 is now expected to be dominant followed by the 8 x 2 and 16 x 1.

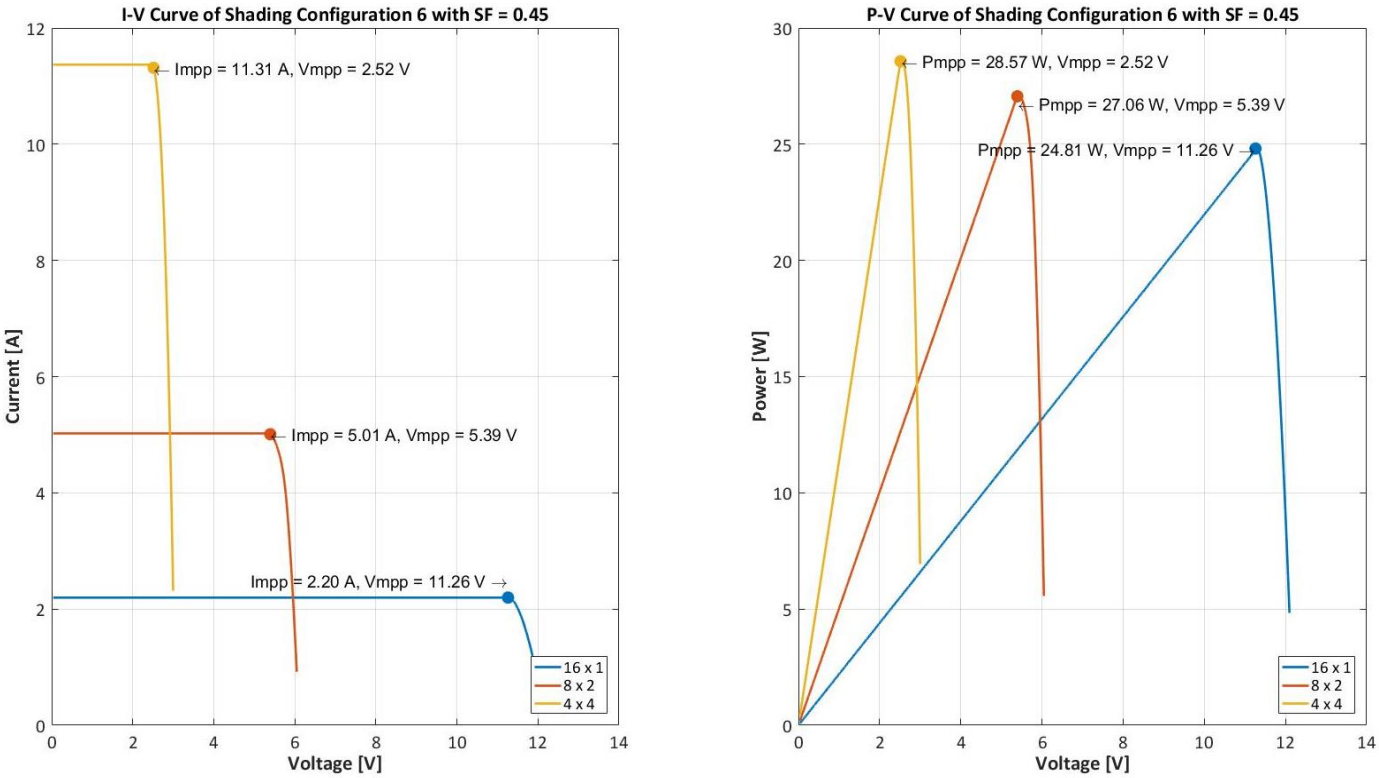


Figure 73: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 6 and Shading Factor 0.45.

The results of the measured panels with the circuit displayed in Figure 74, show that the 4 x 4 wiring configuration has a maximum power output of 18.49 W, the 8 x 2 of 20.22 W and the 16 x 1 of 17.22 W. Thus due to the problems of employing more Schottky diodes and thus more power dissipation, the 8 x 2 wiring configuration is better.

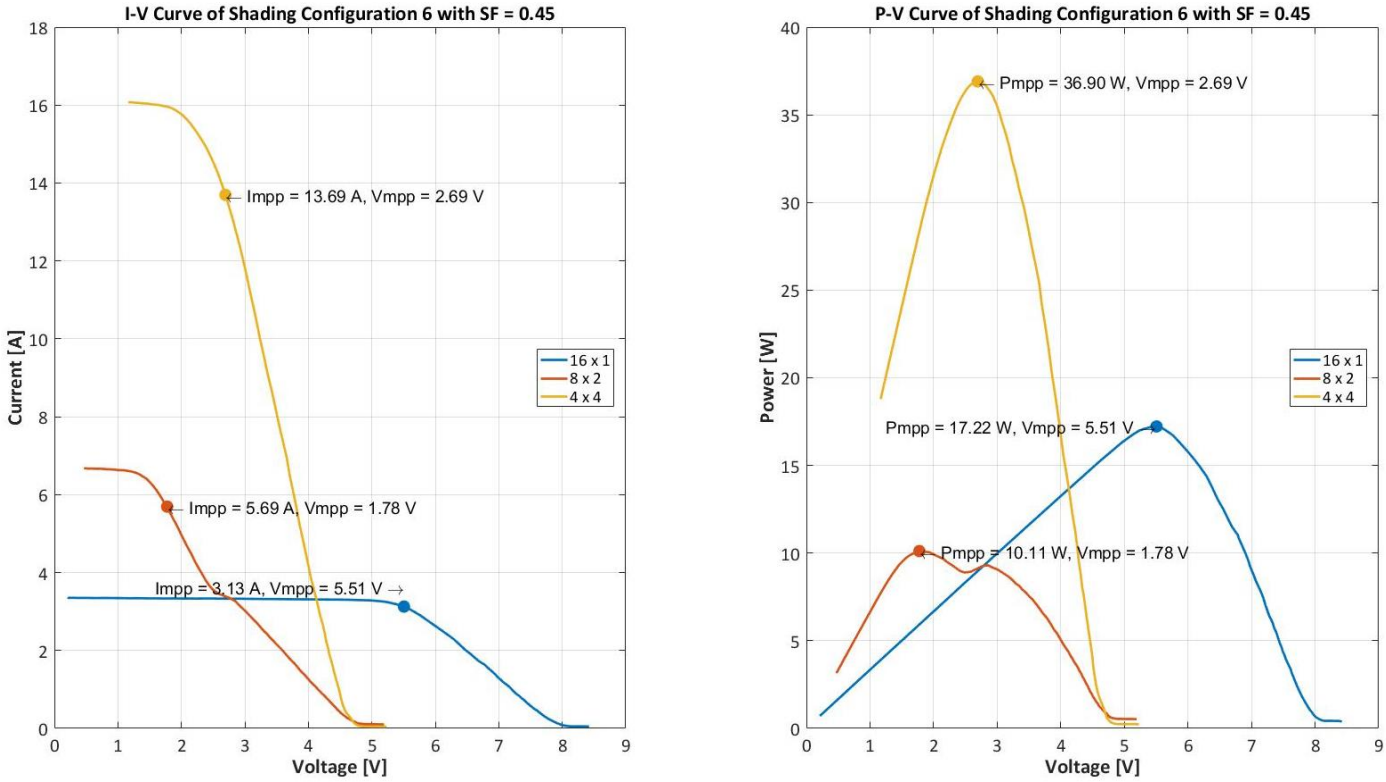


Figure 74: The Measured I-V and P-V Curves of the Three Wiring Configurations with Circuit, Shading Configuration 6 and Shading Factor 0.45.

4.3.3.2 With Shading Factor (SF) of 0.55

When the shading factor is increased the simulations results given in Figure 75 show that the 8 x 2 is now more dominant than the other two wiring configurations.

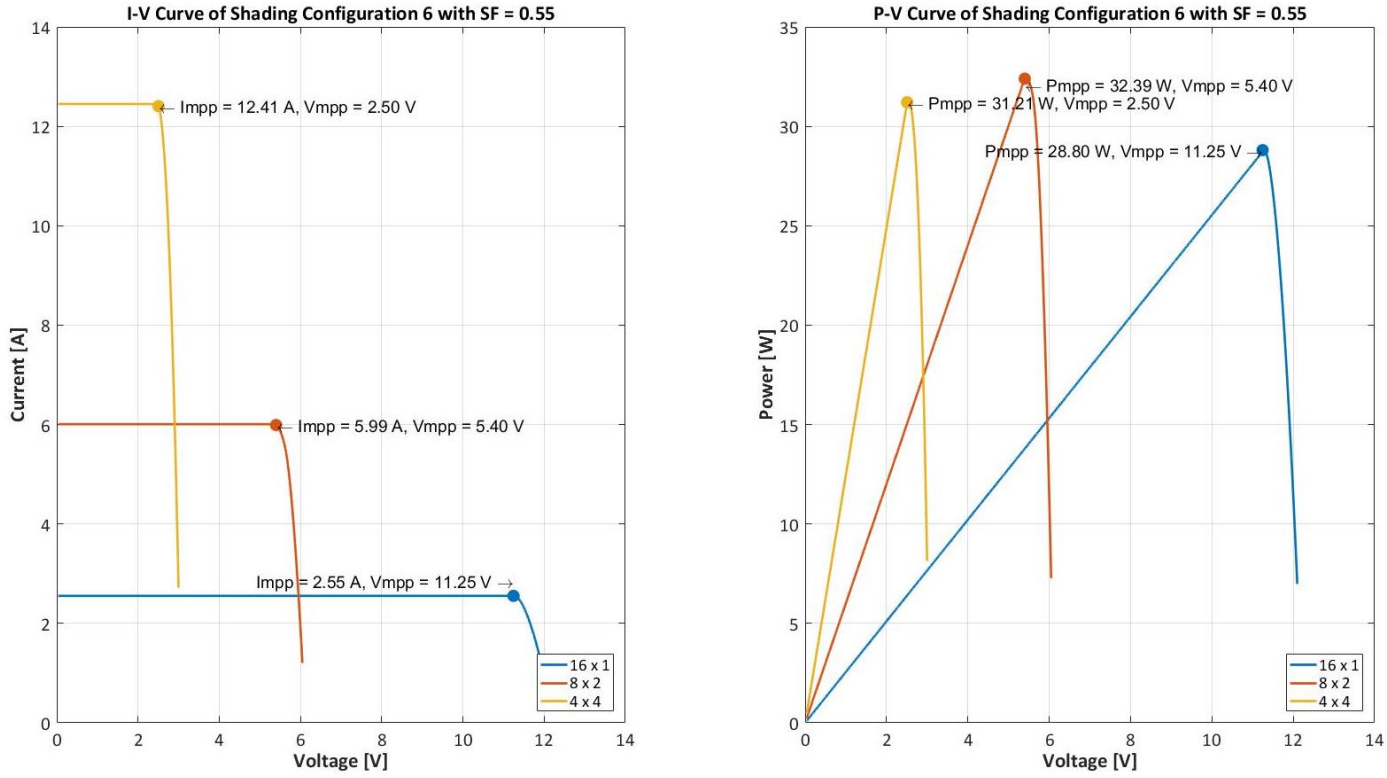


Figure 75: The Simulation I-V and P-V Curves of the Three Wiring Configurations with Shading Configuration 6 and Shading Factor 0.55.

The results of the panel measured with the circuit in Figure 76 show that the 4 x 4 wiring configuration has a maximum power point of 17.32 W, the 8 x 2 of 17.54 W and the 16 x 1 of 14.62

W. Thus the 8 x 2 is marginally better than the 4 x 4 wiring configuration and 2.92 W better than the 16 x 1 wiring configuration.

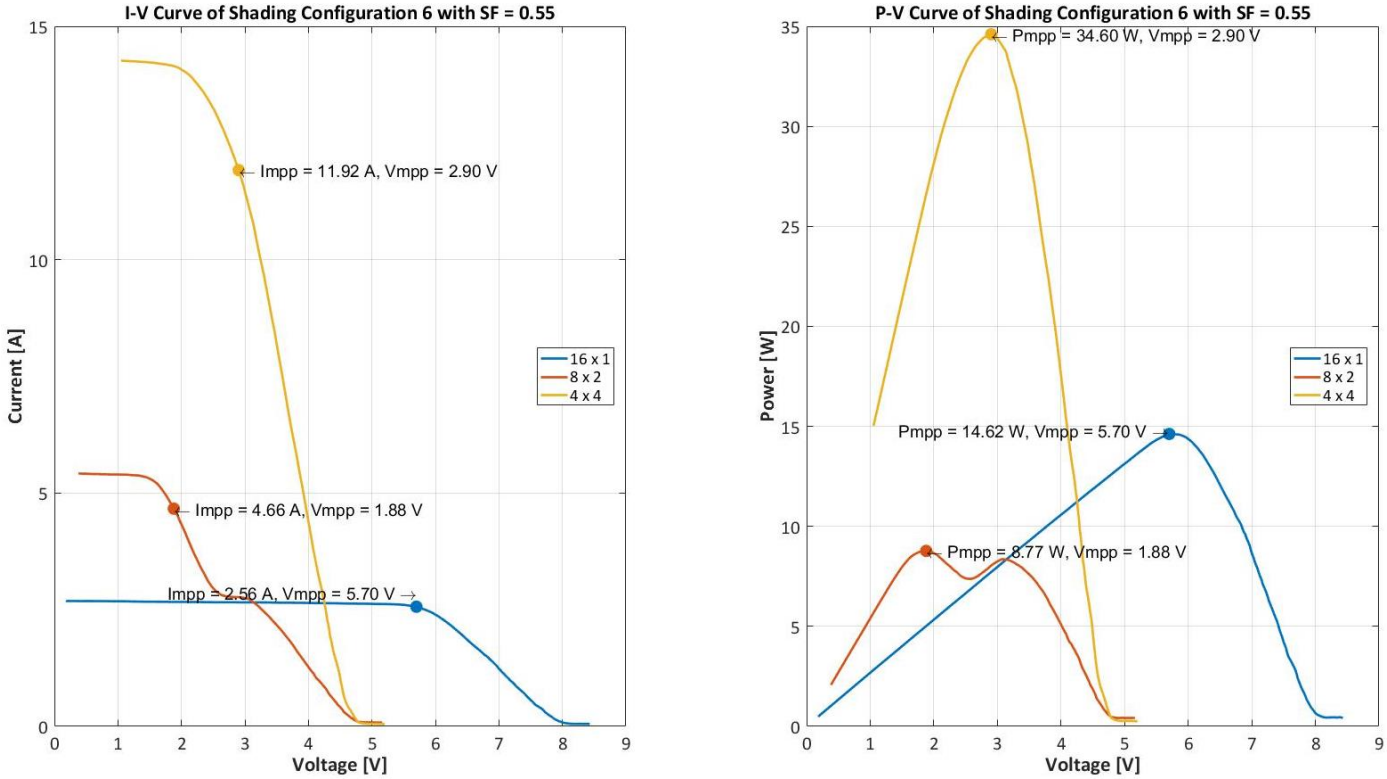


Figure 76: The Measured I-V and P-V Curves of the Three Wiring Configurations with Circuit, Shading Configuration 6 and Shading Factor 0.55.

4.4. Present a comparison between the theoretical and actual findings

The comparison will be in two parts, the first dealing with the differences between simulation and manual panel measurements and the second between simulation and the panel measured using the circuit.

Accurate values for the series and shunt resistances of the SunPower Maxeon Gen II Solar Cells were unavailable in the literature and the equipment to accurately measure these values in-house was unavailable either. The literature provided ample information on the series and shunt resistance of a panel that employed these cells and despite intrapolating this information for one cell for the simulations, this led to disparities between the simulated and panel-measured voltages and currents. Thus despite getting similar trends to the simulation results in the measured results for the panel, the latter values could not be accurately used to improve the simulation models.

Thus the same simulation values for series and shunt resistances, taken from literature were used in the second simulation using the circuit designed. The same problems between simulation and measurement results with the circuit were encountered and these were further exacerbated because of improper models to account for track resistances in the PCB, connector resistances for both the panel, the panel to PCB connector the output load connectors and the cable lengths from the panel to the PCB. There was also the inability to measure accurately resistances on the order of 1 mΩ (the lowest resistance measurement that could be accurately made was 10 mΩ).

Another factor of great concern was that all MOSFETs employed, whether n-type or p-type always operated in the triode or ohmic region making them dependent on the magnitude of the drain currents flowing through them in addition to the magnitude of the gate-source voltage applied. This meant that the induced channels may not have been sufficient to allow for current to flow optimally for the switches further contributing to the resistance of the circuit leading to greater power losses.

The simulation models had no means of incorporating these despite taking greater care to include all available information in the MOSFET component models. A solution to this problem could be through having longer strings of solar cells, so that the drain to source voltage is higher and thus components in the triode mode can be driven into the more energy efficient and thus desirable saturation mode. This latter mode would have lower series resistances [27].

Schottky diodes were used as blocking diodes, these were deemed the diodes with both the lowest forward voltage drop, current carrying capability and thermal stability under these previous conditions resulted in larger power losses (typically 1.83 W per diode), especially as the 8 x 2 and 4 x 4 wiring configurations used four and eight Schottky diodes, respectively.

All of these factors resulted in much lower power measurements between the simulation and panel when the circuits are employed. In some cases the total power losses were as high as half the power output of a panel. Any comparison of the panel output between manual measurements and circuit measurements showed that the latter was energy inefficient to as high as 50 %. Thus the design considerations of track and connector resistances, component operation mode and voltage drops across blocking diodes have to be minimized before a competitively energy efficient system can be designed.

4.5. Comparison of power losses between theoretical and practical

A comparison is made between the theoretical power losses calculated in section 3.9 and the measured power losses from the results in this section. The current values used are for the unshaded case for all three wiring configurations using the circuit measured current from section 4.3.

4.5.1 The 16 x 1 Wiring Configuration

The current per string of 16 cells is 5.71 Amps and this translates to a measured power loss in the panel with 16 x 1 wiring configuration presented in Table 14. As can be seen from the 52 W rated panel, 11.09 W are lost across the switches, the sense resistor, the blocking diodes and the MC4 connectors. This total power translates to a 32.39 % loss from the panel when controlled by the circuit.

Table 14: The Measured Power Dissipated in the 16 x 1 Wiring Configuration.

Resistances			
Description	**Value [Ω]**	**Power Dissipation [W]**	**Percentage Loss [%]**
N-FET 1	0.012	0.39	3.53
P-FET 3	0.009	0.29	2.65
P-FET 6	0.009	0.29	2.65
P-FET 9	0.009	0.29	2.65
P-FET 11	0.009	0.29	2.65
Rsense4	0.012	0.39	3.53
2 x Blocking Diodes		6.85	61.77
8 * MC4 with 50 mm	0.4	2.28	20.59
Total	0.46	11.09	

4.5.2 The 8 x 2 Wiring Configuration

The current per string of eight cells is 4.09 Amps and this translates to measured power loss in the panel with 8 x 2 wiring configuration presented in Table 15. As can be seen from the 52 W rated panel, 7.95 W are lost across the switches, the sense resistor, the blocking diodes and the MC4 connectors. This total power translates to a 22.08 % loss from the panel when controlled by the circuit.

Table 15: The Theoretical Power Dissipated in the 8 x 2 Wiring Configuration.

Resistances			
Description	**Value [Ω]**	**Power Dissipation [W]**	**Percentage Loss [%]**
N-FET 1	0.012	0.20	2.53
P-FET 3	0.009	0.15	1.89
P-FET 5	0.009	0.15	1.89
N-FET 7	0.012	0.20	2.53
P-FET 9	0.009	0.15	1.89
P-FET 11	0.009	0.15	1.89
Rsense2	0.012	0.20	2.53
Rsense4	0.012	0.20	2.53
4 x Blocking Diodes		4.91	61.74
8 * MC4 with 50 mm	0.4	1.64	20.58
Total	0.484	7.95	

4.5.3 The 4 x 4 Wiring Configuration

The current per string of 4 cells is 6.11 Amps and this translates to theoretical power loss in the panel with 4 x 4 wiring configuration presented in Table 16. As can be seen from the 52 W rated panel, 14.70 W are lost across the switches, the sense resistor, the blocking diodes and the MC4 connectors. This total power translates to a 40.99 % loss from the panel when controlled by the circuit.

Table 16: The Theoretical Power Dissipated in the 4 x 4 Wiring Configuration.

Resistances			
Description	**Value [Ω]**	**Power Dissipation [W]**	**Percentage Loss [%]**
N-FET 1	0.012	0.23	1.55
P-FET 2	0.009	0.17	1.16
N-FET 4	0.012	0.23	1.55
P-FET 5	0.009	0.17	1.16
N-FET 7	0.012	0.23	1.55
P-FET 8	0.009	0.17	1.16
N-FET 10	0.012	0.23	1.55
P-FET 11	0.009	0.17	1.16
Rsense1	0.012	0.23	1.55
Rsense2	0.012	0.23	1.55
Rsense3	0.012	0.23	1.55
Rsense4	0.012	0.23	1.55
8 x Blocking Diodes		10.45	71.11
8 * MC4 with 50 mm	0.4	1.74	11.85
Total	0.532	14.70	

As can be seen in the comparison of the three tables, the blocking diodes produce the largest power dissipation amongst all the components used in the SCPM circuit and thus should be the first components that should be changed in future revisions. Following this the materials of the MC4 connector and the switches need to be changed to further reduce their losses since these are the next two components that affect the output power from the SCPM circuit.

5 Conclusions and Recommendations

5.1. Conclusions

The investigation to determine whether the use of bypass diodes or the use of active switching was better was successfully carried out. Using Simulink for the simulation work and then using a custom made solar panel to measure performance during shading testing, the validity of the simulation model was determined through this comparison. The trends shown by the simulation results agreed with the results of the manual measurements of the panel however not in terms of magnitude of the values. This latter was due to the inability to validate the Simulink model since equipment capable of measuring accurate series and shunt resistance of the cells (The Pasan solar cell tester was not functional) and for the panel the equipment in the department cannot make these measurements accurately. Thus a more precise and accurate model could not be developed.

An SCPM circuit was designed, built and tested before it was employed to change the wiring configurations as the shading factor and the shading configurations over the panel were changed during testing. The shading measurements conducted on the SCPM circuit when compared to measurements made on the manually changed wiring configuration showed that it was successful in determining that changing wiring configurations are better than having one BPD for a minimum grouping of four cells since they provide one global maximum operating point instead of several.

The Simulink model did not consider resistance measurements for the connectors (for the strings, the PCB and the cables between the MC-4 connectors and the PCB), the components (operating in triode mode instead of saturation mode) and the voltage drops across the Schottky blocking diodes that all contributed to significant SCPM output power losses.

The goal to develop the SCPM circuit from the patent claims was successful. To show the proof of concept and functionality of the SCPM system both from manual measurements and then through the use of the circuit was successful. The Simulink models developed first for manual measurements and then for measurements with the SCPM circuit both showed that the active switching of the wiring configuration, in theory was better in terms of electrical output, than the use of a single bypass diode per cell.

5.2. How the Research Questions were met

The research questions that were successfully investigated:

- Can a system be created where through switching between several wiring configurations of solar cells during the case of changing shading conditions, a better electrical power output can be produced?

  The SCPM system was designed to do this and it is able to switch between three wiring configurations, 16 x 1, 8 x 2 and 4 x 4 to be able to get a higher output power from 16 solar cells arranged in a panel in a 4 x 4 solar cell orientation.

- Is this system better in terms of optimization of electrical power output than through implementing bypass diodes which may not be activated by the MPPT of the inverter?

  The SCPM system is not better than existing systems in its present state since it has not been optimised in terms of reduction of power losses to produce an output power that surpasses that of the manually measured modules.

- Can this system thus have a greater electrical power output than commercially available solar panels that utilize BPDs?

  After carrying out the optimization of the SCPM circuit and scaling it to handle a higher power rating as described in section 4.4. This would result in a higher drain-source voltage for the switches to operate in saturation mode, the circuit can then be compared with commercially available panels that utilize bypass diodes.

- Can a new means of solar panel wiring system be suggested that uses a minimized topology with the 16 cells and then expanded to the commercially available solar panels that use 60, 72 and 96 solar cells. Thus will this circuit be energy efficient and economically viable?

  One approach would be to have long strings of cells that are able to provide a higher drain-source voltage for the MOSFET switches and thus have the switches operate in the saturation region. This would allow for easier integration of the present circuit into a commercial panel however to optimize its functionality more optimum wiring configurations would have to be found.

5.3. Recommendations to Improve the SCPM Circuit

The SCPM Circuit can be improved in the following ways:

- A means of making the Simulink models align more closely with manual measurements and circuit assisted measurements would need to be found. This would help test shading for larger panel arrangements presently used commercially with 60, 72 and 96 solar cells.
- Validated models could be used for designing systems of higher voltages, currents and thus higher power ratings.
- A means of reducing power losses in the circuit needs to be found since the highest power losses of 61-71% depending on the wiring configuration can occur due to the forward voltage drop and the high currents passing through the blocking diodes.
- There is also a considerable power loss of 21% from the eight MC4 contacts thus materials with lower resistivity should be used where possible.
- The findings in section 4.5 showed that the performance of the circuit could be improved by a different choice of FET switches with lower on resistances. At present switch losses make up less than 20 % of the accounted Joule losses and these could be further reduced. One of the reasons for these high losses is due to operation in the triode mode which has greater

resistive losses than the saturation mode. One solution was to have higher drain-source voltages through having more than four cells in a string, so that instead of operating in the triode mode the switches would possibly be in the saturation mode.

- A more thorough search for switches could be selected to operate in the saturation mode. This mode would result in less power dissipation in the on resistance and afford greater control of the switch, independent of the value of the drain current.
- The PCB should be redone so that the connections of the cells are on the edges of the board and this would make for easier connection of the solar cells and for troubleshooting them.
- The PCB designed was a two layer board however to make the distance between the MPU signals and the driver and intermediary circuits shorter, perhaps a four layer PCB could be used.
- A tighter control on track dimensions and resistances would also help keep power losses in the board to a minimum.

5.4. Future Work

Work that can still be implemented based on the findings in this project are the use of a smaller PCB and better dimensioned PCB tracking to greater reduce power losses in the system. Tighter controls on the resistances of the both the mechanical connectors and the wiring of the strings to the panel is required. The switches need to be designed in any future iterations to be able to handle current spikes should these occur when switching between topologies and tighter control of this would become a concern if rapid levels of switching and with higher currents are required. The inclusion of a more uniform feedback system to determine when the system is switching would also be beneficial in troubleshooting the system.

The communication system could be developed and integrated since only a generic means of communicating data was considered. A question of should this information be displayed in real time or stored remotely for use at a later date needs to be answered. The communication system could also be used to talk to other SCPM circuits if more than one is employed in a PV system. It is envisaged that if larger strings are used then one SCPM per module would certainly be possible however implementing the circuit for several modules would be more cost effective.

Since the focus of this thesis project was on proof of concept of the system the minutiae of the system were not explored more than what was needed to achieve basic functionality. This means the optimisation of the circuit was postponed to the next versions. It is highly recommended that a more thorough impact assessment be done on minimising resistances, connection lengths, switching losses and a means be found for reducing the power losses in the diodes or a new design without diodes but replacements for them. This approach would help the SCPM circuit have better electrical output performance and thus increase its competitiveness in terms of electrical efficiency and cost with some of the other approaches mentioned earlier to optimise a PV panel’s electrical output.

A Appendices

A-1 Bill of Materials

Transistors	Description	Supplier Code
Q1	BD139 NPN Transistor	182-5611
Q2	BD139 NPN Transistor	182-5611
Q3	BD139 NPN Transistor	182-5611
Q4	BD139 NPN Transistor	182-5611
Q5	BD139 NPN Transistor	182-5611
Q6	BD139 NPN Transistor	182-5611
Q7	BD139 NPN Transistor	182-5611
Q8	BD139 NPN Transistor	182-5611
Q9	BD139 NPN Transistor	182-5611
Q10	BD139 NPN Transistor	182-5611
Q11	BD139 NPN Transistor	182-5611

Pol Caps	Description	Supplier Code
Cf2	1 uF electrolytic	123-6666
Cf4	1 uF electrolytic	123-6666

Caps	Description	Supplier Code
C1	4.7 uF	2752827
C3	4.7 uF	2752827
C5	4.7 uF	2752827
C7	4.7 uF	2752827
C9	4.7 uF	2752827
C11	4.7 uF	2752827
C13	4.7 uF	2752827
C15	4.7 uF	2752827
C17	4.7 uF	2752827
C19	4.7 uF	2752827
C21	4.7 uF	2752827
Cf1	100 nF ceramic	171-2471
Cf3	100 nF ceramic	171-2471

Solar Panel String Connectors	Description	Supplier Code
P1	2 pin header 10 A rating	2112482
P2	2 pin header 10 A rating	2112482
P3	2 pin header 10 A rating	2112482
P4	2 pin header 10 A rating	2112482
P5	2 pin header 10 A rating	2112482
P6	2 pin header 10 A rating	2112482
P7	2 pin header 10 A rating	2112482
P8	2 pin header 10 A rating	2112482
P_VCC	2 pin header 10 A rating	2112482
P_Vin	2 pin header 10 A rating	2112482

Microprocessor	Description	Supplier Code
P_MPU	Raspberry Pi Zero W	Kiwi Electronics

DC-DC Converters	Description	Supplier Code
P_DC1	CRE1S0515SC	1021460
P_DC2	CRE1S0515SC	1021460
P_DC3	CRE1S0515SC	1021460
P_DC4	CRE1S0515SC	1021460
P_DC5	CRE1S0515SC	1021460
P_DC6	CRE1S0515SC	1021460
P_DC7	CRE1S0515SC	1021460
P_DC8	CRE1S0515SC	1021460
P_DC9	CRE1S0515SC	1021460
P_DC10	CRE1S0515SC	1021460
P_DC11	CRE1S0515SC	1021460
P_DC_Opto	CRE1S0515SC	1021460

Header 8	Description	Supplier Code
P_ADC1	Pin Strip 8-Pin	1097955
P_ADC2	Pin Strip 8-Pin	1097955

Current Sensor	Description	Supplier Code
U1	INA193AIDBVR	2764673
U2	INA193AIDBVR	2764673
U3	INA193AIDBVR	2764673
U4	INA193AIDBVR	2764673

Voltage Regulator	Description	Supplier Code
VReg1	LM317T Volt Reg	975-6027
VReg2	LM317T Volt Reg	975-6027

Current Sense Resistor	Description	Supplier Code
Rsense1	Resistance:0.012ohm; Voltage Rating:100V; Resistor Element Material:Wirewound; Resistor Case Style:Axial Leaded; Power Rating:3W; Resistance Tolerance:± 5%; Product Range:W31 Series; Temperature Co	9497080
Rsense2	Resistance:0.012ohm; Voltage Rating:100V; Resistor Element Material:Wirewound; Resistor Case Style:Axial Leaded; Power Rating:3W; Resistance Tolerance:± 5%; Product Range:W31 Series; Temperature Co	9497080
Rsense3	Resistance:0.012ohm; Voltage Rating:100V; Resistor Element Material:Wirewound; Resistor Case Style:Axial Leaded; Power Rating:3W; Resistance Tolerance:± 5%; Product Range:W31 Series; Temperature Co	9497080
Rsense4	Resistance:0.012ohm; Voltage Rating:100V; Resistor Element Material:Wirewound; Resistor Case Style:Axial Leaded; Power Rating:3W; Resistance Tolerance:± 5%; Product Range:W31 Series; Temperature Co	9497080

Resistors	Description	Supplier Code
MOSFET Gate Resistors		
R1	NFET Gate Res 1 Ω	9341153
R2	PFET Gate Res 1 Ω	9341153
R3	PFET Gate Res 1 Ω	9341153
R4	NFET Gate Res 1 Ω	9341153
R5	PFET Gate Res 1 Ω	9341153
R6	PFET Gate Res 1 Ω	9341153
R7	NFET Gate Res 1 Ω	9341153
R8	PFET Gate Res 1 Ω	9341153
R9	PFET Gate Res 1 Ω	9341153
R10	NFET Gate Res 1 Ω	9341153
R11	PFET Gate Res 1 Ω	9341153

Driver Components		
R12	3.3 kΩ	9341749
R14	3.3 kΩ	9341749
R16	3.3 kΩ	9341749
R18	3.3 kΩ	9341749
R20	3.3 kΩ	9341749
R22	3.3 kΩ	9341749
R24	3.3 kΩ	9341749
R26	3.3 kΩ	9341749
R28	3.3 kΩ	9341749
R30	3.3 kΩ	9341749
R32	3.3 kΩ	9341749

DC-DC Converter Resistors		
R34	20 Ω	9341510
R35	20 Ω	9341510
R36	20 Ω	9341510
R37	20 Ω	9341510
R38	20 Ω	9341510
R39	20 Ω	9341510
R40	20 Ω	9341510
R41	20 Ω	9341510
R42	20 Ω	9341510
R43	20 Ω	9341510
R44	20 Ω	9341510
R_DC	20 Ω	9341510

OpAmp Biasing		
Current Sensing		
Rop1	10 kΩ and 100 kΩ	9341110 and 9341129
Rop2	10 kΩ and 100 kΩ	9341110 and 9341129
Rop3	10 kΩ and 100 kΩ	9341110 and 9341129
Rop4	10 kΩ and 100 kΩ	9341110 and 9341129
Rop5	10 kΩ and 100 kΩ	9341110 and 9341129
Rop6	10 kΩ and 100 kΩ	9341110 and 9341129
Rop7	10 kΩ and 100 kΩ	9341110 and 9341129
Rop8	10 kΩ and 100 kΩ	9341110 and 9341129

Voltage Sensing		
Rop9	30 kΩ	9341706
Rop10	100 kΩ	9341129
Rop11	100 kΩ	9341129
Rop12	30 kΩ	9341706
Rop13	30 kΩ	9341706
Rop14	100 kΩ	9341129
Rop15	100 kΩ	9341129
Rop16	30 kΩ	9341706
Rop17	30 kΩ	9341706
Rop18	100 kΩ	9341129
Rop19	100 kΩ	9341129
Rop20	30 kΩ	9341706
Rop21	30 kΩ	9341706
Rop22	100 kΩ	9341129
Rop23	100 kΩ	9341129
Rop24	30 kΩ	9341706

Regulator Tuning		
Rs1	120 Ω	9341218
Rs2	120 Ω	9341218

Gate-Source Resistance		
RZ1	100 kΩ	9341129
RZ2	100 kΩ	9341129
RZ3	100 kΩ	9341129
RZ4	100 kΩ	9341129
RZ5	100 kΩ	9341129
RZ6	100 kΩ	9341129
RZ7	100 kΩ	9341129
RZ8	100 kΩ	9341129
RZ9	100 kΩ	9341129
RZ10	100 kΩ	9341129
RZ11	100 kΩ	9341129

Variable Resistors	Description	Supplier Code
Rvar1	500R Trimmer	108-235
Rvar2	500R Trimmer	108-235

SM N-FETs	Description	Supplier Code
QNFET1	SI4840BDY-T1-GE3	2335320
QNFET1b	SI4840BDY-T1-GE3	2335320
QNFET4	SI4840BDY-T1-GE3	2335320
QNFET4b	SI4840BDY-T1-GE3	2335320
QNFET7	SI4840BDY-T1-GE3	2335320
QNFET7b	SI4840BDY-T1-GE3	2335320
QNFET10	SI4840BDY-T1-GE3	2335320
QNFET10b	SI4840BDY-T1-GE3	2335320

SM P-FETs	Description	Supplier Code
QPFET2	SI4459ADY-T1-GE3	1858953
QPFET2b	SI4459ADY-T1-GE3	1858953
QPFET3	SI4459ADY-T1-GE3	1858953
QPFET3b	SI4459ADY-T1-GE3	1858953
QPFET5	SI4459ADY-T1-GE3	1858953
QPFET5b	SI4459ADY-T1-GE3	1858953
QPFET6	SI4459ADY-T1-GE3	1858953
QPFET6b	SI4459ADY-T1-GE3	1858953
QPFET8	SI4459ADY-T1-GE3	1858953
QPFET8b	SI4459ADY-T1-GE3	1858953
QPFET9	SI4459ADY-T1-GE3	1858953
QPFET9b	SI4459ADY-T1-GE3	1858953
QPFET11	SI4459ADY-T1-GE3	1858953
QPFET11b	SI4459ADY-T1-GE3	1858953

OpAmps	Description	Supplier Code
Uop1	TLC27M4CN	1103018
Uop2	TLC27M4CN	1103018
ADC Chip	ADC128D818CIMT/NOPB	2395888

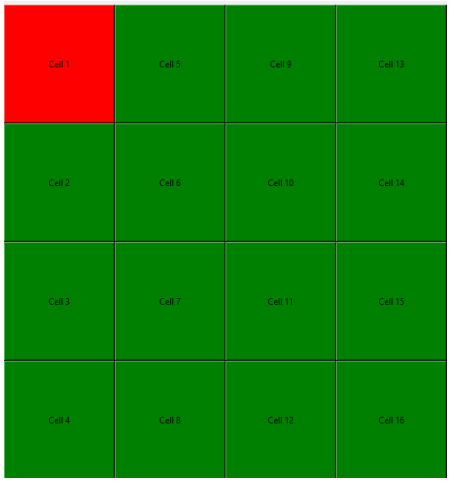
Schottky Diodes	Description	Supplier Code
DSc1	DST2045AX	2762784
DSc2	DST2045AX	2762784
DSc3	DST2045AX	2762784
DSc4	DST2045AX	2762784

A-2 Microprocessor Pinouts for the Raspberry Pi Zero W

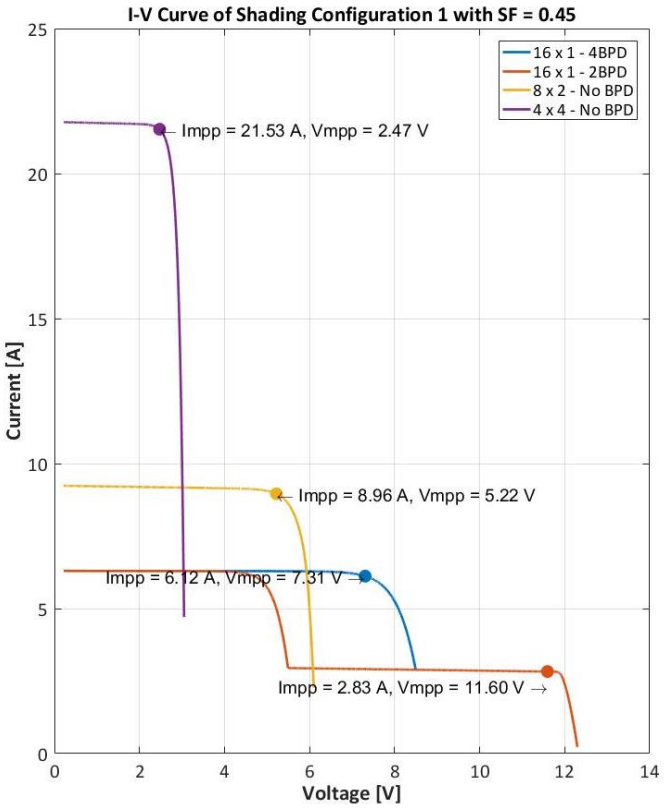
Pin Numbers	Name	Description	Assignment
1	3V3		
2	5V0		
3	GPIO2	SDA (I2C Data) has a fixed pull-up resistor (3.3V)	Used for ADC for Current Sensing
4	5V0		
5	GPIO3	SDL (I2C Clock) has a fixed pull-up resistor (3.3V)	Used for ADC for Current Sensing
6	GND		
7	GPIO4	GPCLK0 - Input and Output Pin	
8	GPIO14	Input and Output Pin	Switch 10
9	GND		
10	GPIO15	Input and Output Pin	Switch 11
11	GPIO17	Input and Output Pin	
12	GPIO18	Input and Output Pin	
13	GPIO27	Input and Output Pin	
14	GND		
15	GPIO22	Input and Output Pin	
16	GPIO23	Input and Output Pin	
17	3V3		
18	GPIO24	Input and Output Pin	
19	GPIO10	Input and Output Pin	Switch 6
20	GND		
21	GPIO9	Input and Output Pin	Switch 5
22	GPIO25	Input and Output Pin	
23	GPIO11	Input and Output Pin	Switch 7
24	GPIO8	Input and Output Pin	Switch 4
25	GND		
26	GPIO7	Input and Output Pin	Switch 3
27	ID SD		
28	ID SC		
29	GPIO5	Input and Output Pin	Switch 1
30	GND		
31	GPIO6	Input and Output Pin	Switch 2
32	GPIO12	Input and Output Pin	Switch 8
33	GPIO13	Input and Output Pin	Switch 9
34	GND		
35	GPIO19	Input and Output Pin	
36	GPIO16	Input and Output Pin	
37	GPIO26	Input and Output Pin	
38	GPIO20	Input and Output Pin	
39	GND		
40	GPIO21	Input and Output Pin	

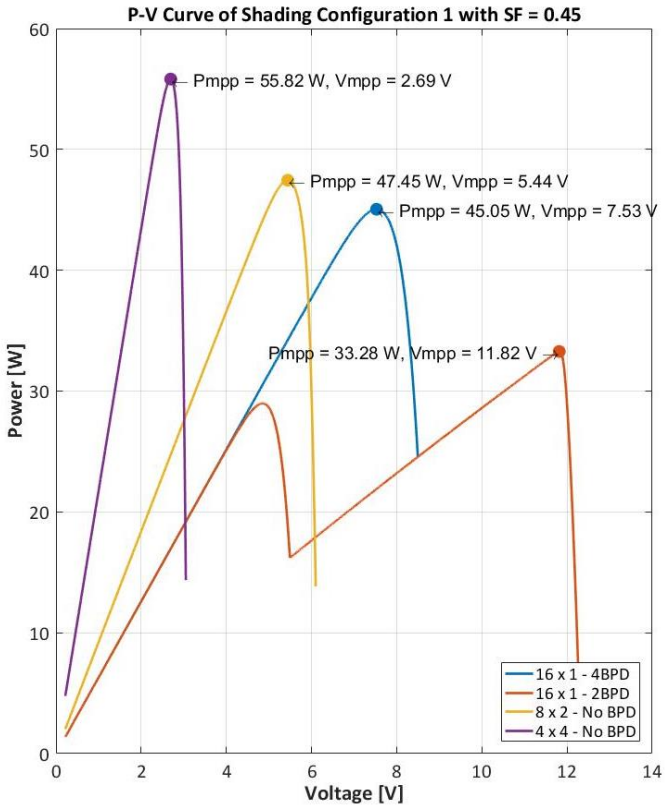
A-3 Extra Shading Configurations Measured but not used

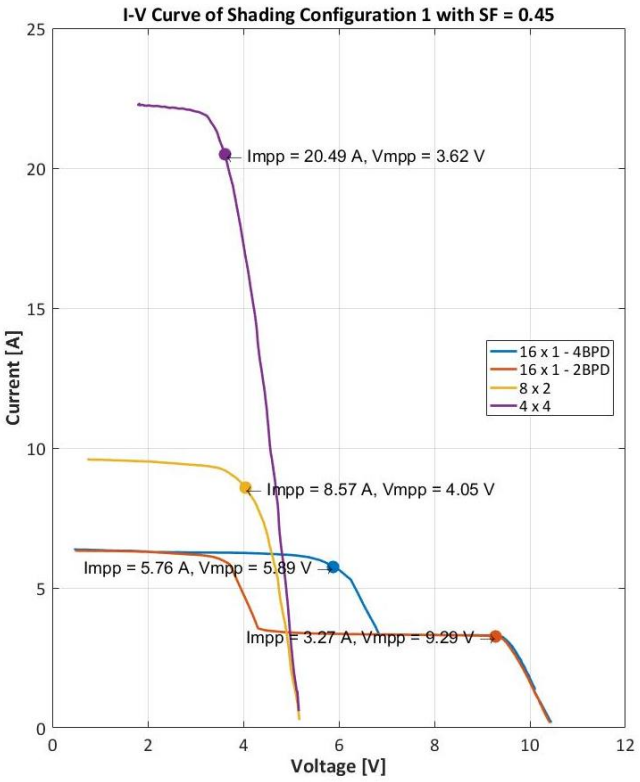
Shading Configuration 1: Cell 1 is shaded

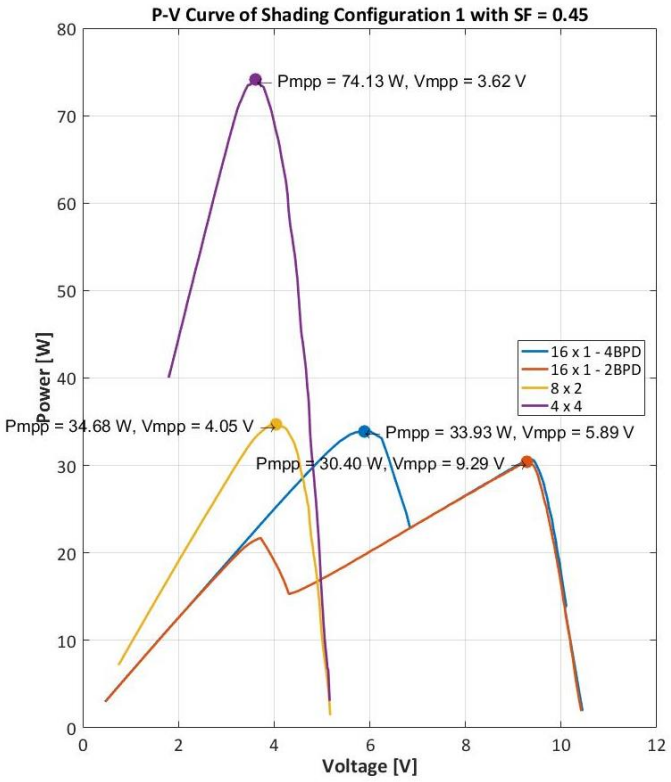


With Shading Factor (SF) of 0.45









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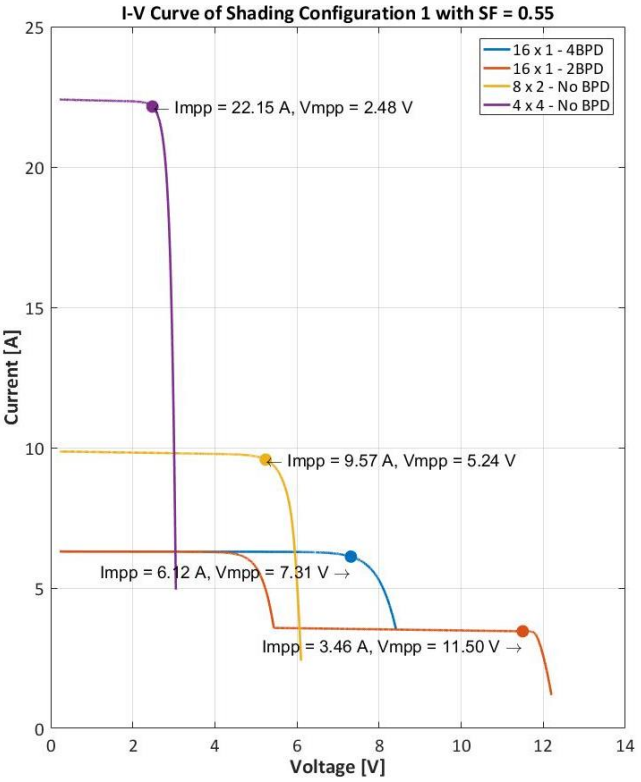
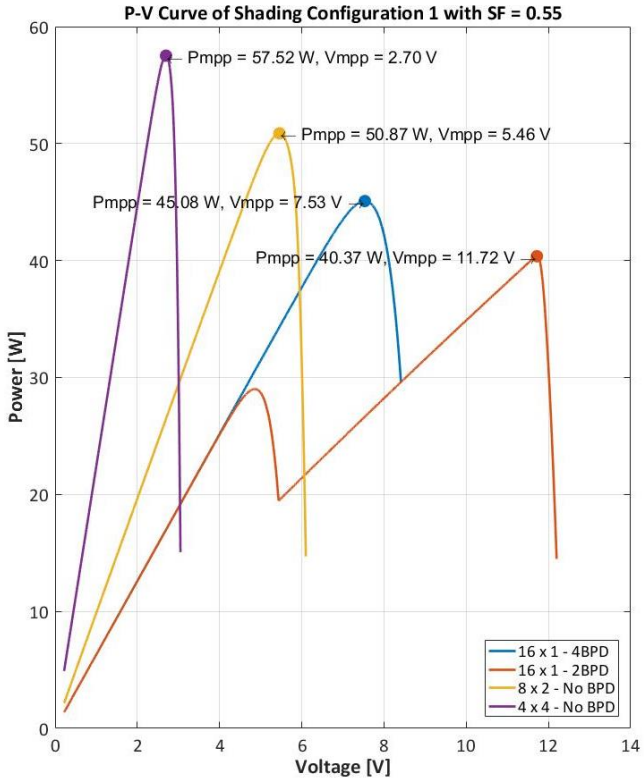
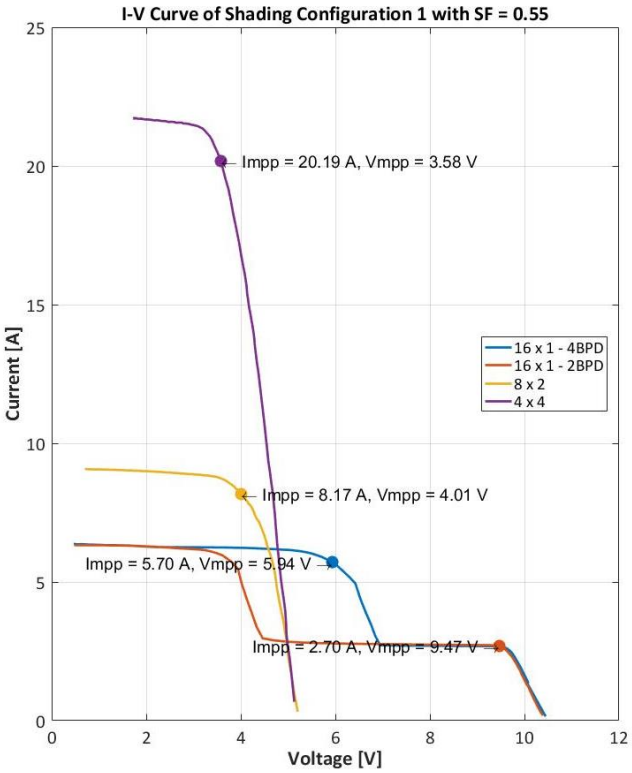
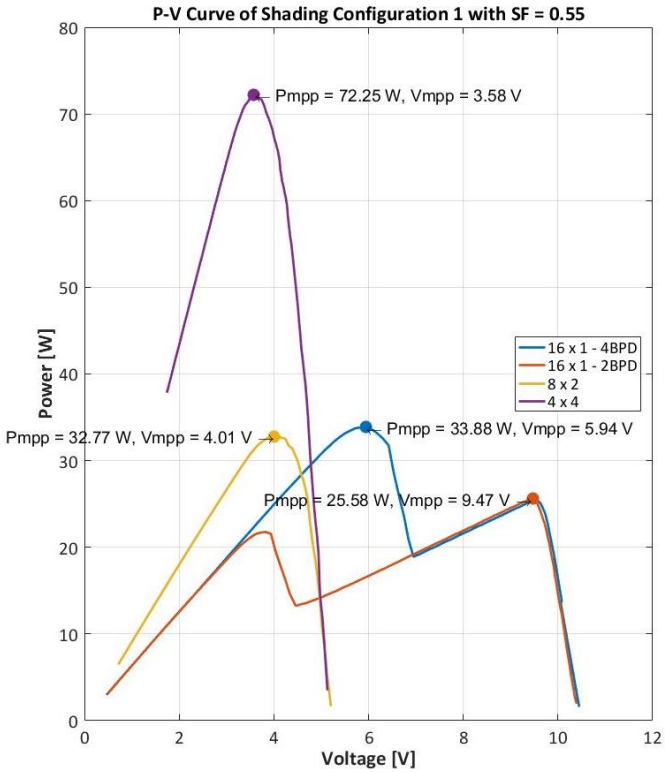
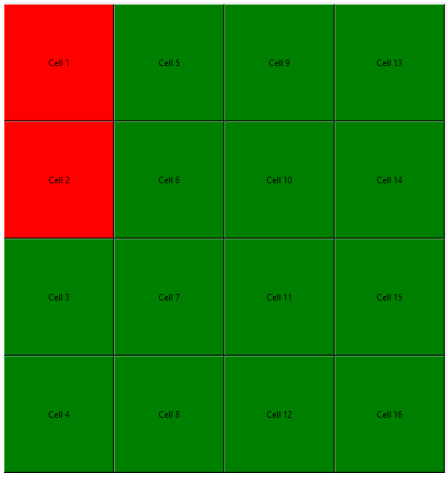




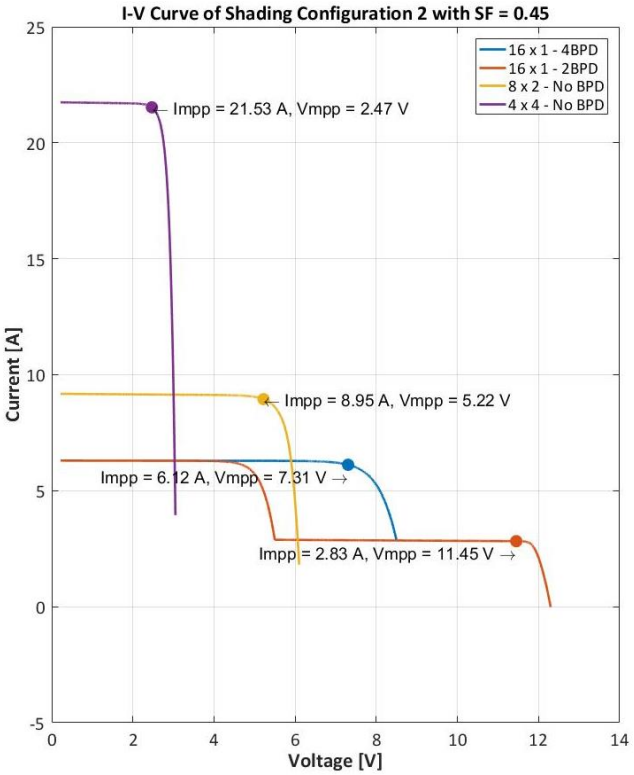


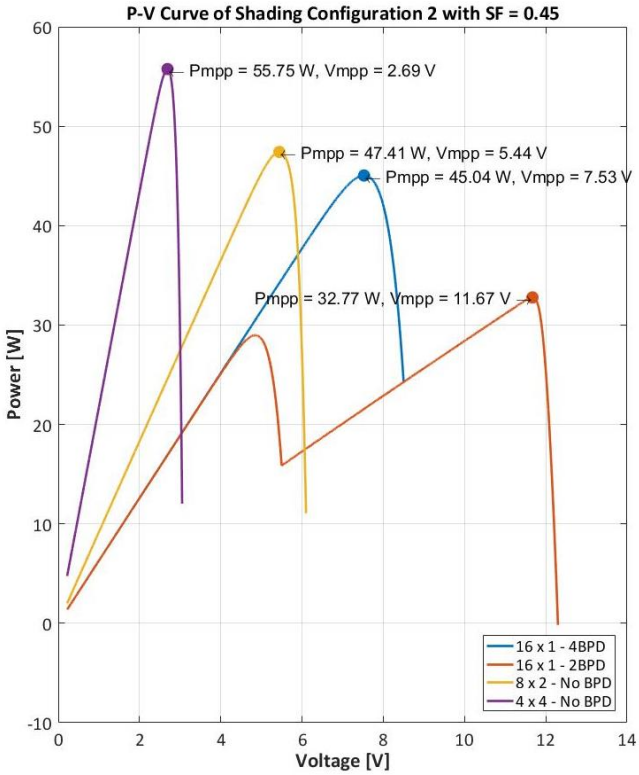


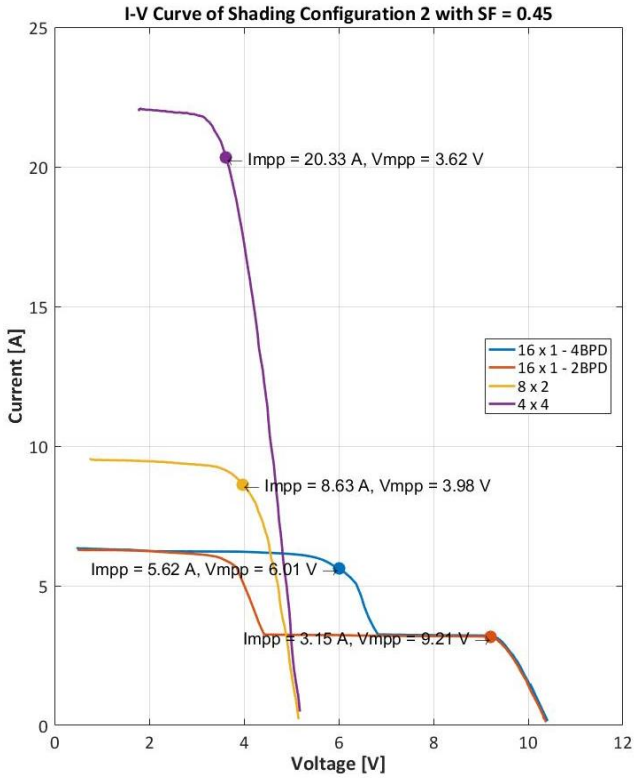
Shading Configuration 2: Cell 1 and 2 are shaded

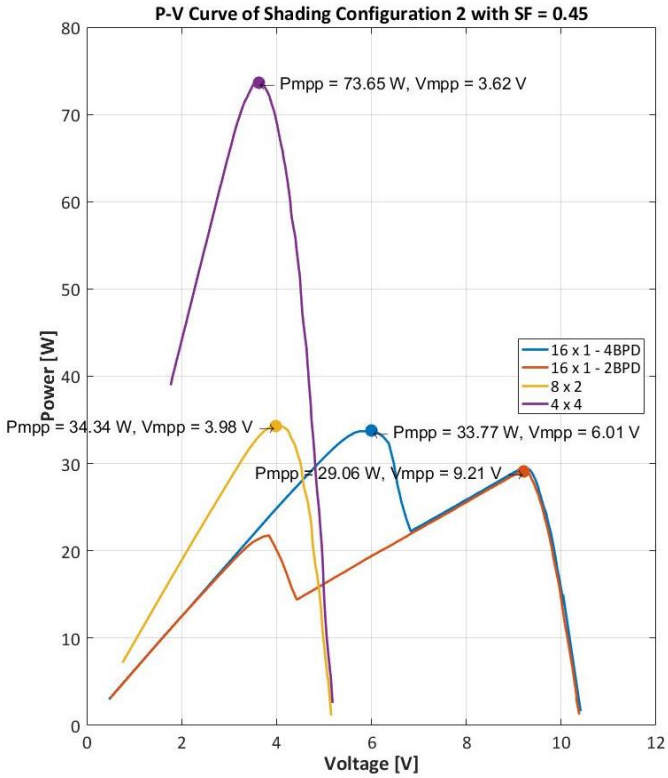


With Shading Factor (SF) of 0.45

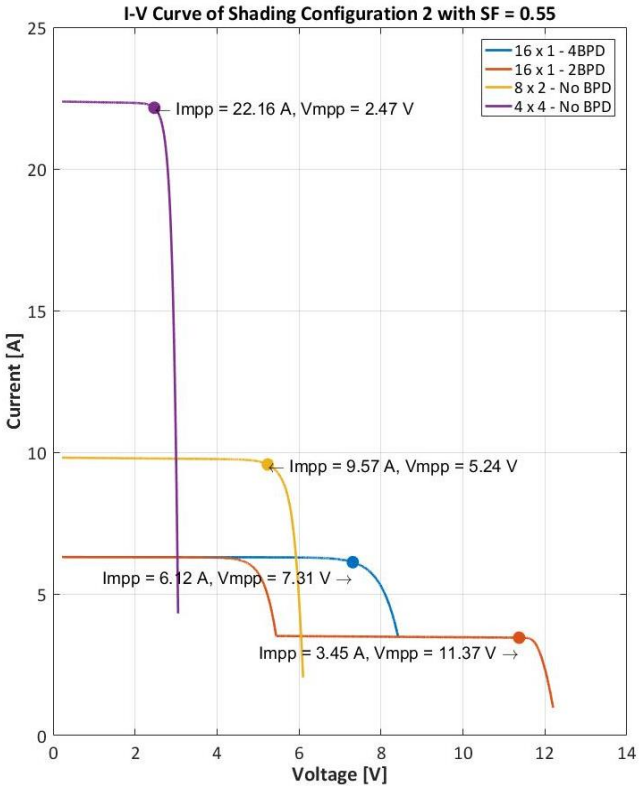


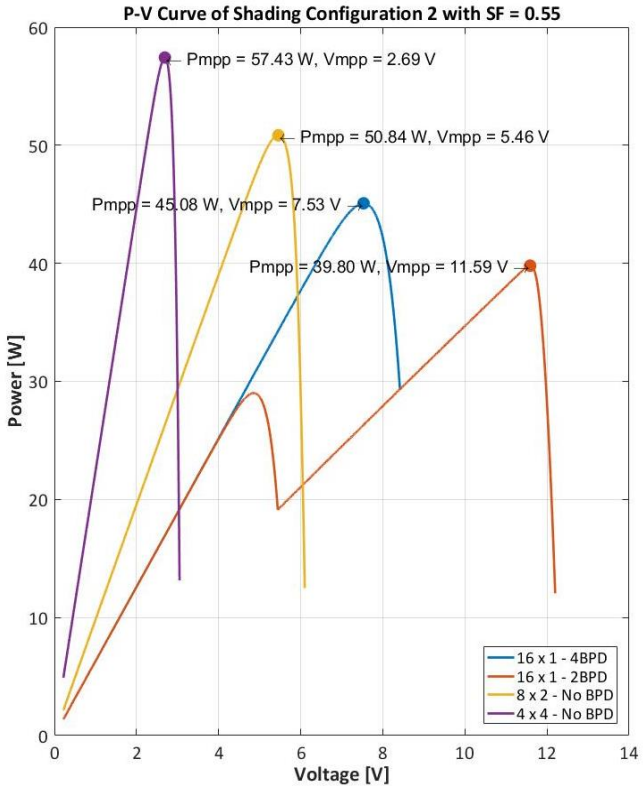


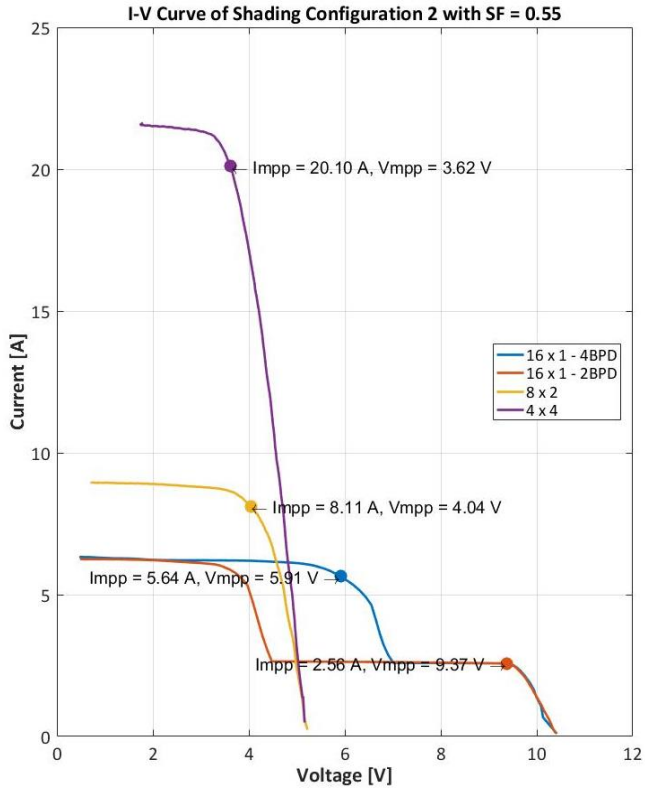


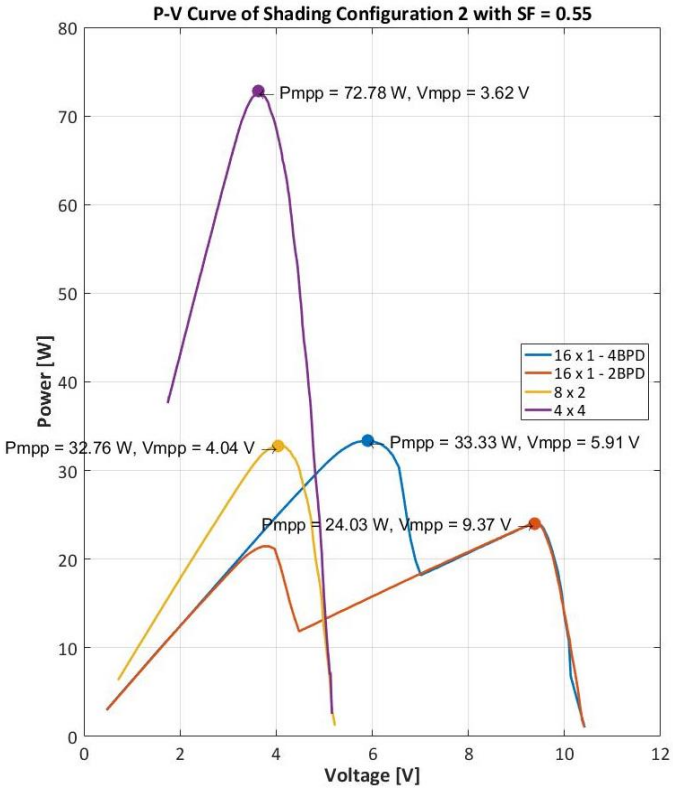


With Shading Factor (SF) of 0.55

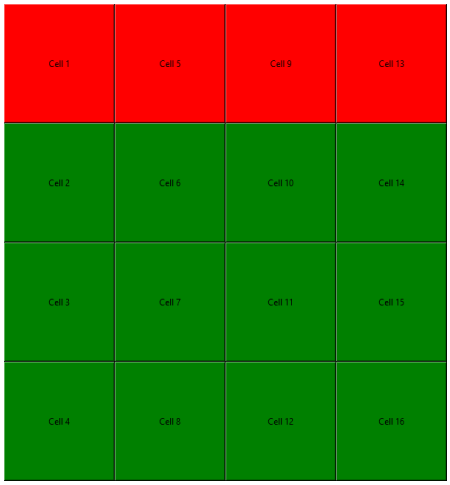




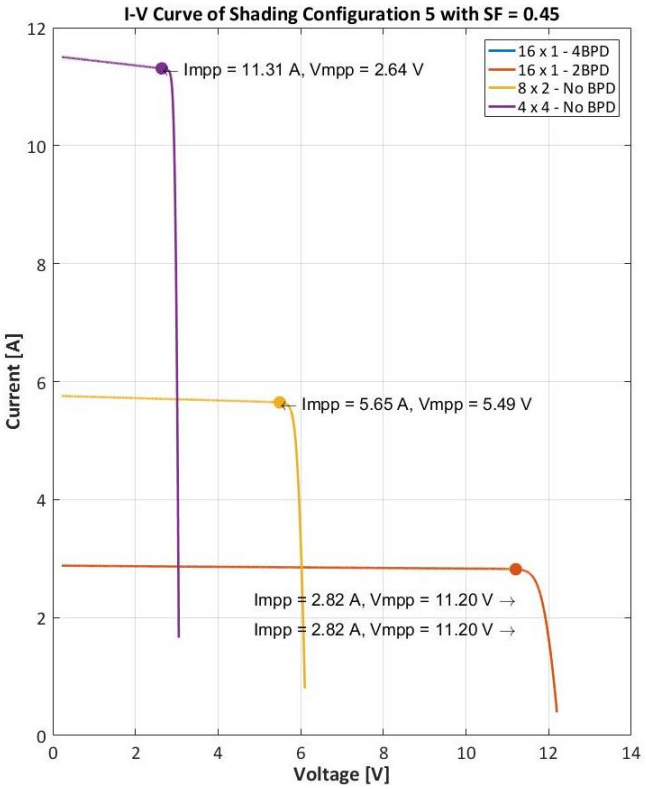


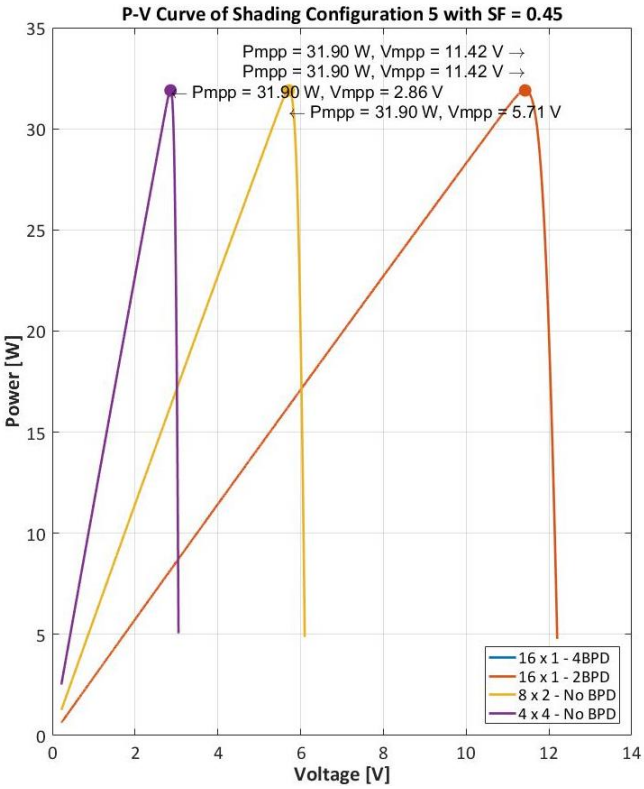


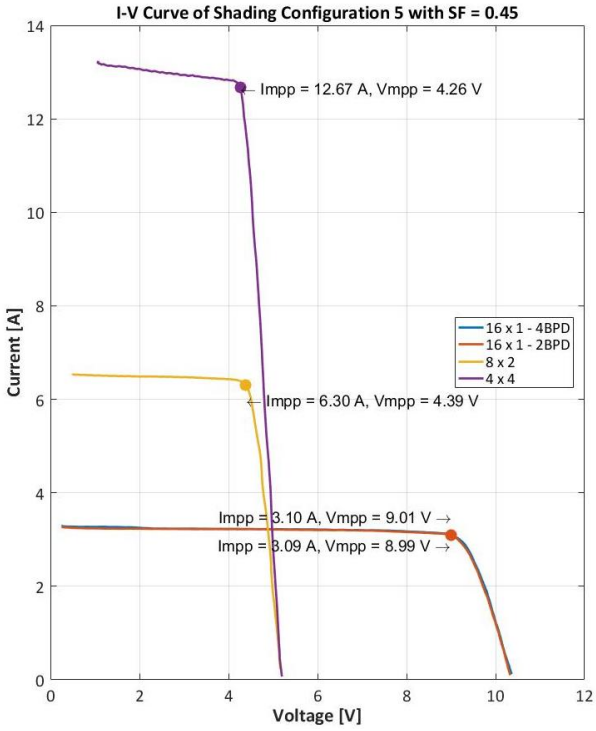
Shading Configuration 5: Cell 1, 5, 9 and 13 are shaded

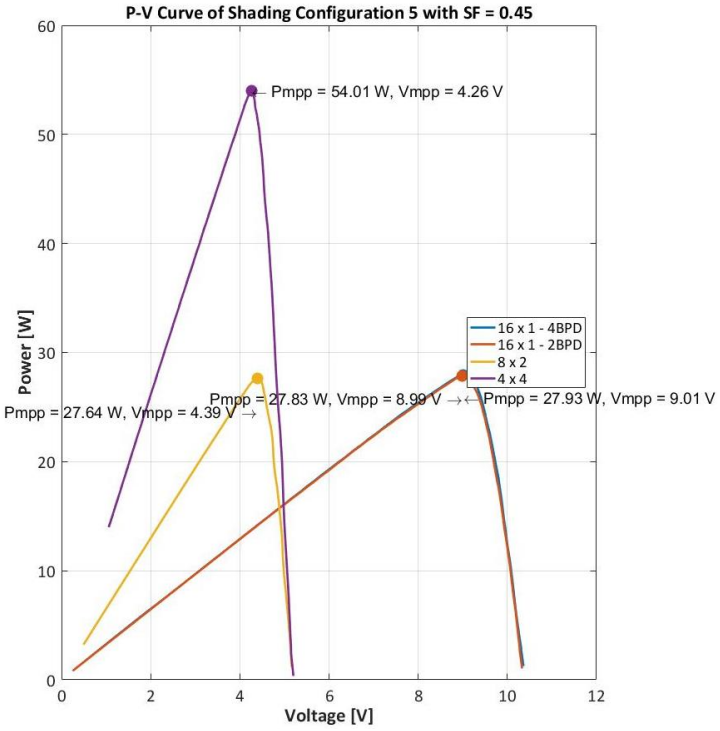


With Shading Factor (SF) of 0.45

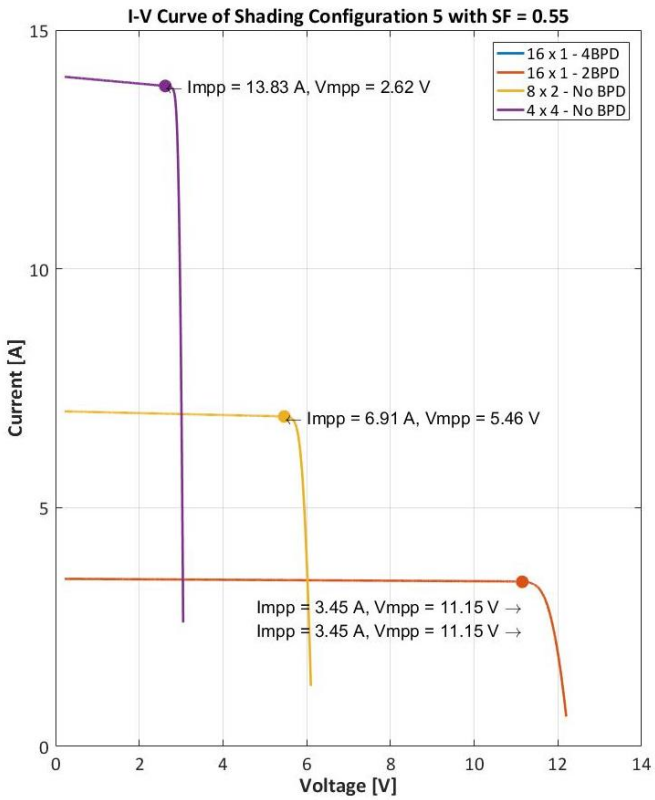


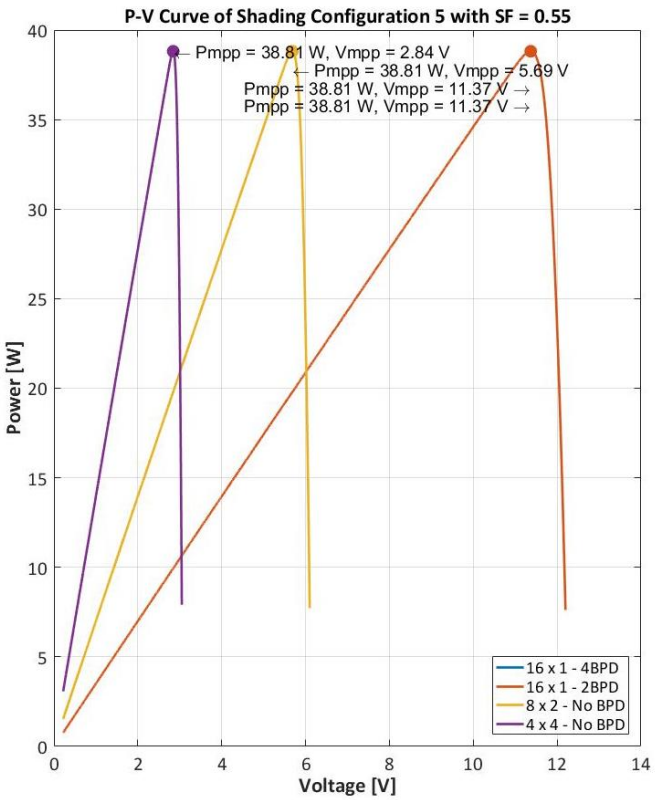


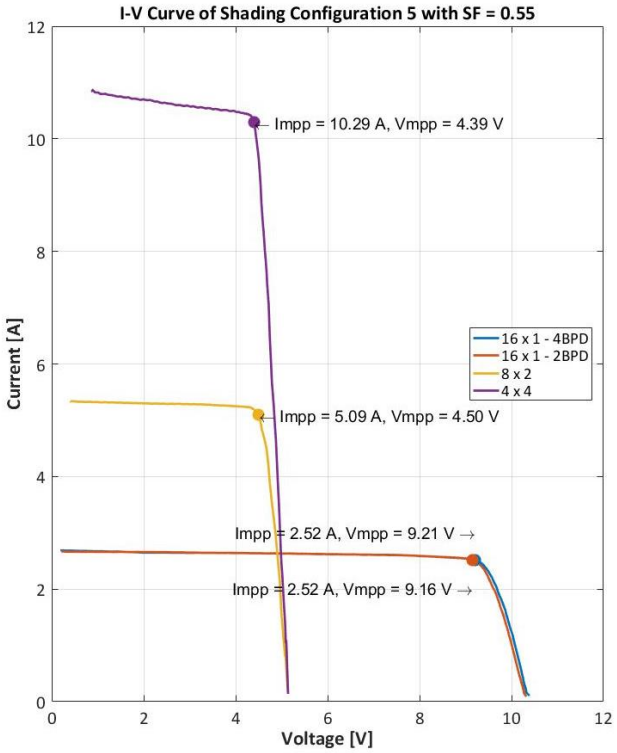


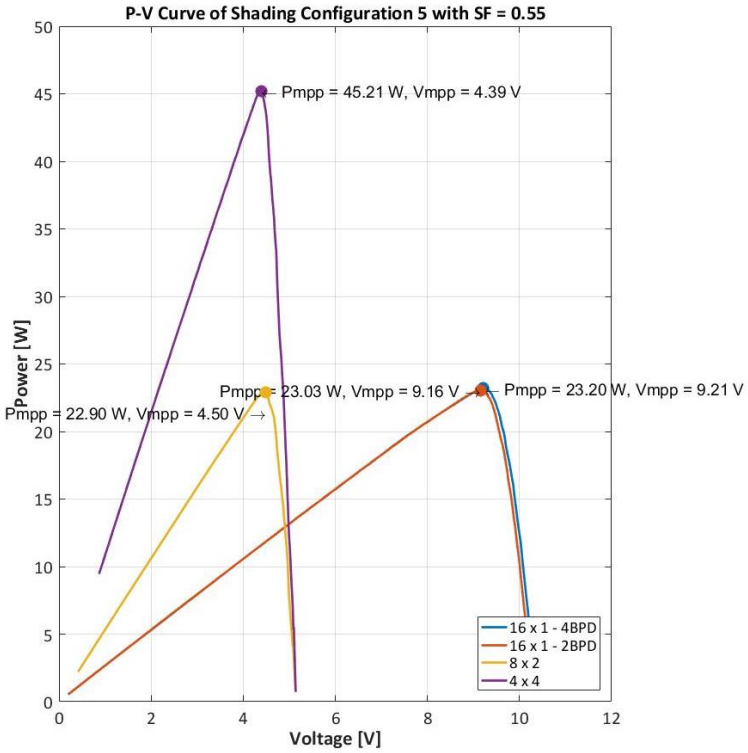


With Shading Factor (SF) of 0.55






I-V Curve of Shading Configuration 5 with SF = 0.55
Current [A]
Voltage [V]
Impp = 10.29 A, Vmpp = 4.39 V
Impp = 5.09 A, Vmpp = 4.50 V
Impp = 2.52 A, Vmpp = 9.21 V
Impp = 2.52 A, Vmpp = 9.16 V
16 x 1 - 4BPD
16 x 1 - 2BPD
8 x 2
4 x 4


P-V Curve of Shading Configuration 5 with SF = 0.55
Power [W]
Voltage [V]
Pmpp = 45.21 W, Vmpp = 4.39 V
Pmpp = 23.03 W, Vmpp = 9.16 V
Pmpp = 23.20 W, Vmpp = 9.21 V
Pmpp = 22.90 W, Vmpp = 4.50 V
16 x 1 - 4BPD
16 x 1 - 2BPD
8 x 2
4 x 4

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