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ROM-FOM Interface Optimization for Efficient Thermomechanical Simulations of Electronic Components

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Abstract

Model order reduction techniques are developed and utilized to make numerical simulations more efficient. The use of Reduce Order Models (ROM) also enables data exchange with external parties without disclosing the sensitive information present in a Full-Order Model (FOM). It is crucial to optimize for both the efficiency and accuracy of a ROM to keep a minimal deviation from the FOM. The complexity of a ROM-based simulation depends on the definition of the ROM as well as its connection with the remaining FOM. This paper investigates the effect of different ROM-FOM interface definitions for a test case consisting of an electronic package-on-PCB assembly. A virtual Design of Experiments (DoE) was carried out with a total of 41 cases considering three different locations and up to four different constraint equations for the ROM-FOM interface. The effect on the accuracy and time-efficiency of the ROM-based thermomechanical simulations are compared with respect to the full Finite Element (FE) model. The *deformable* configuration for the interface generally showed the most accurate results, while the *rigid* configuration was the most efficient across the board. The *beam* configuration did not always follow an expected trend based on the order of elasticity values of the assigned materials. Based on the deformation results and the time associated with ROM generation and use-pass, multiple optimal solutions from the DoE are discussed.

1. Introduction

Computational methods such as Finite Element Analysis (FEA) are widely used for analysing thermal, mechanical, and electrical behaviour of electronic packaged components and associated electronics-enabled systems. Complex analyses demand more computational resources and simulation time, which can be cut down by using a Reduced-Order Model (ROM) of certain (sub)component or (sub)system of an electronic product. ROMs tend to have lower accuracy compared to the Full-order Models (FOM) and are primarily considered for improving the simulation efficiency [1-3].

Counterintuitively, ROMs can be more computationally expensive in practice with the existing infrastructure of the available methodologies and developed software. However, they are particularly handy for exchanging data with external parties without the need of sharing detailed models [4]. Thus, when protecting sensitive information is a priority, the use of ROMs (compact models) is not just a matter of choice, convenience, or resource availability but becomes a necessity. The efficiency and the accuracy of a ROM often compete with each other and cannot be achieved at the same time [5]. Therefore, it is important to choose a ROM which strikes a balance in running efficiently and attaining acceptable accuracy.

The computational complexity of a ROM primarily depends on the definition of the model order reduction technique, *i.e.*, the methodology utilized to obtain the ROM. Moreover, for a certain reduction technique, the complexity varies based on the choice of the ROM-FOM interface, which defines *where* and *how* the ROM (sub-component) is connected to the rest of the FOM (component). This paper aims to addresses the latter aspect by investigating the effect of the ROM-FOM interface definition on the accuracy of the results compared to that of a full Finite Element (FE)-based model while optimizing for the efficiency of the computation.

First, a workflow of creating a Super Element (SE)-based ROM of an electronic package is presented. Then, the ROM-FOM interface, *i.e.*, the connection between the package ROM and the remaining FOM (solder + PCB) was defined using different definitions of the constraint equations and at three different layers within the package. A Virtual Design of Experiments (VDoE) was carried out for a total of 41 cases of ROMs, and the results are compared with that of the original FOM of the complete package-PCB assembly. The accuracy of the thermomechanical deformation and the time-efficiency of the simulations were compared, and the possible optimal cases are discussed.

2. Finite Element-based FOM

A test case of a package-on-PCB assembly was prepared using FE modelling. Figure 1 indicates the utilized geometry. The model considers a single Quad Flat No-leads (QFN) package with a centrally placed silicon die attached to copper Lead-Frame (LF) using die-attach adhesive. In addition, there are copper pads at each corner of the package, and this sub-assembly is encapsulated by Epoxy Moulding Compound (EMC). The package is connected to the PCB using four solder interconnects at its corners. The PCB is modelled as a homogenized equivalent layer.

The main objective of the prepared FE-model is to simulate the thermomechanical behaviour of the considered electronic system and utilize the workflow to evaluate thermal stresses in solder joints for the estimation of fatigue lifetime. Considering this goal, four landing

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copper-pads embedded into the PCB were modelled separately to make the region surrounding the solder joints more detailed for better accuracy. Moreover, the package geometry is prepared such that a ROM-FOM interface can be defined at different layers within the package, keeping the solder joints and PCB always a part of the remaining FOM.

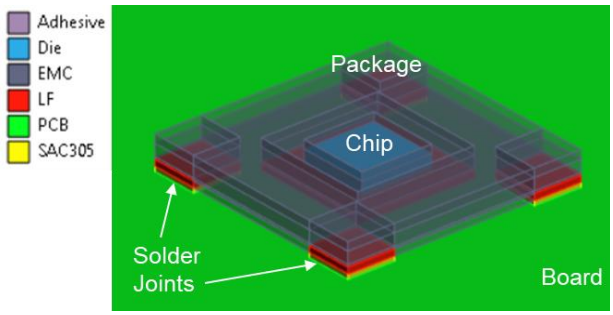

Figure 1: The geometry of the package-on-PCB assembly test case. The QFN package contains a centrally placed silicon die attached to the copper leadframe (LF) with the die-attach (adhesive) and encapsulated with EMC. Four solder joints connect the copper pads of the package and PCB.

A cyclic thermal load induces the accumulation of damage in solder material due to plastic strains and eventually leads to fatigue failure. This is governed by the out of plane deformation (or warpage) due to a mismatch of Coefficient of Thermal Expansion (CTE) of different materials of the assembly. It is crucial to get the failure prediction from a ROM-based simulation same as or as close to the FOM. Therefore, the warpage plot of the solder-PCB sub-assembly was utilized for benchmarking the accuracy of ROM-based models. Figure 2 shows the spatial plot of the out-of-plane deformation for the FOM under a temperature variation from 125 °C to -40 °C. This plot is used as the reference for comparing results of different ROM-based simulation cases.

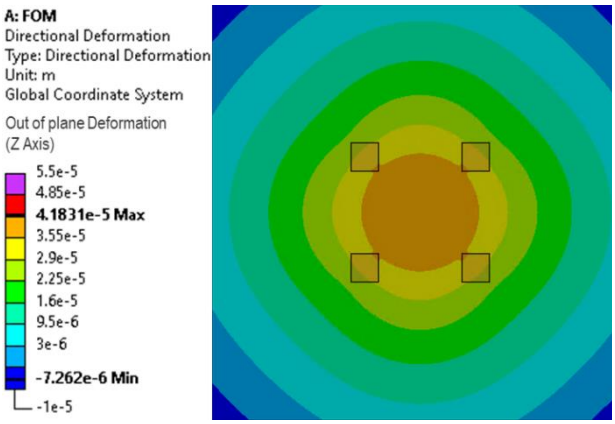

Figure 2: The out-of-plane deformation of the solder-PCB subassembly in the FOM under a temperature variation from 125 °C to -40 °C. This spatial plot is used as the reference for benchmarking the accuracy of different cases of ROM-based simulations.

3. Substructure-based FEA (ROM)

A substructure-based approach was utilized to create an effective compact model of the package, considering it as the intellectual property (IP) to be protected. This method generates an equivalent superelement of the package subassembly. Figure 3 shows a quarter geometry cross section of the package-on-PCB test case and highlights the materials in different layers.

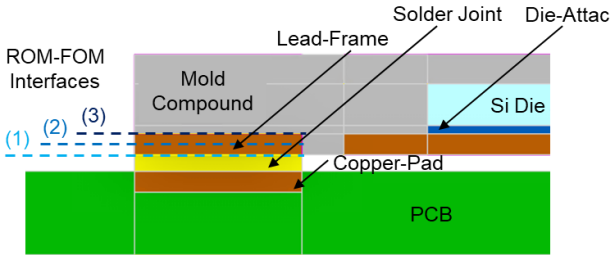

Figure 3: The cross section of the test case assembly indicating different layers of materials and the three considered locations of the ROM-FOM interface.

Substructure Generation

First, the entire system assembly was partitioned by defining the ROM-FOM interface at one of the three different locations – (i) between package-leadframe and solder joint, (ii) within the package-leadframe, and (iii) between package-leadframe and moulding compound. The considered interfaces are also indicated in Figure 3.

Next, the steps for substructure generation were carried out on the package side of the geometry. Four surfaces were defined as the scope geometry for creating master nodes of the resulting superelement. For example, the lower surface of each copper pad of the package became the scoped geometry for the *interface 1*. For simplicity and efficient simulations, each scoped geometry was assigned only one master node with six Degrees of Freedom (DoF). This step connects each node on the scoped geometry's FE mesh to the respective master node using Multi-Point Constraint (MPC) equations. MPCs are the set of additional equations that map the DoF of the scoped nodes to those of the respective master nodes.

Figure 4 shows a schematic representation of how a scoped geometry is connected to a master node using a set of equations (*MPC_1*), which forms the SE-based ROM of the package subassembly. Three main types of MPCs were considered – *deformable*, *rigid*, and *beam*. A *deformable* relation makes the DoF of master nodes dependent with only 6 MPCs, while a *rigid* relation makes the DoF of 81 scoped nodes dependent with 486 (6×81) MPCs. A *beam* relation acts as a beam (finite) element with a defined circular cross section and assigned material properties. For every beam definition, the cross section diameter was kept the same as the side of the square copper pad, and either one of the interface materials was assigned. For example, a *beam* MPC for the *Interface 3* could have EMC and LF (copper), while the *Interface 2* has only LF as the option for materials to be assigned.

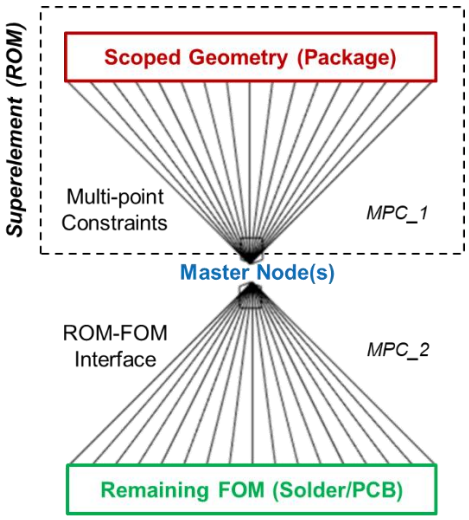

Figure 4: A schematic representation of two sets of multipoint constraints for the ROM-FOM interface. MPC_1 connects the scoped geometry to master nodes to form a superelement-based ROM, and MPC_2 connects the ROM substructure to the remaining FOM.

Then, a matrix reduction step was defined, which removes the dependent DoF applicable for the chosen MPC relation using static condensation. The goal of the SE generation step is to obtain the effective load vector to be applied to the remaining FOM. A thermal load vector corresponding to a unit temperature difference (ΔT = 1 °C) was obtained from this step by exporting the resulting substructure file.

ROM Integration and Load Vector

A separate setup was created based on the original FOM for utilizing the prepared ROM. Based on the location of the interface for each case, the package geometry was excluded. The thermal load conditions were kept identical for the remaining FOM. Then, the generated ROM substructure of the package was imported and tied to the rest of the FOM geometry, *i.e.*, the PCB, solder joints, and the remaining package subcomponents (if applicable), using another choice of MPC relation (*MPC_2*). Figure 5 shows the integrated ROM, which is now represented by only the geometric outer boundary (wireframe) of the package, keeping the inner layers completely hidden.

At the same time, the effective thermal load is applied to the master nodes, which now scope the corresponding surfaces on the other side of the ROM-FOM interface. The same set of MPC definitions (*deformable*, *rigid*, and one or more *beam* configurations) were utilized. The default thermal load (force and moment) exerted by the imported ROM corresponds to the package deformations due to a unit temperature increase (*i.e.*, ΔT = 1 °C). Thus, a custom subroutine (script) was utilized to scale the thermal load vector as a function of temperature at different time steps [6], matching the temperature profile applied to the FOM subassembly.

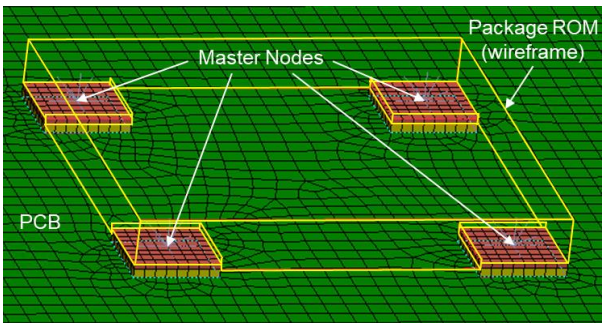

Figure 5: An example of the integrated ROM substructure of the package (for Interface 3), which hides the inner layers completely. The effective thermal load vector is applied at the master node connections between the ROM and FOM.

The mathematical representation of the effective thermal load scaling is given in Equation (1),

$$[\boldsymbol{K}]\{\boldsymbol{u}\} = \{\boldsymbol{f}^{\mathrm{th}}\} + w(T) \cdot \{\boldsymbol{f}^{\mathrm{th}}_{\mathrm{ROM}}\} \quad (1)$$

where $\boldsymbol{K}$ is the global stiffness matrix of the remaining FOM, $\boldsymbol{u}$ is the displacement vector, $\boldsymbol{f}^{\mathrm{th}}$ is the load vector due to applied thermal load conditions, $\boldsymbol{f}^{\mathrm{th}}_{\mathrm{ROM}}$ is the default load vector from ROM due to the ΔT = 1 °C, and $w(T)$ is the temperature (T)-dependent scaling parameter. Note that the temperature dependent properties for the materials in the remaining FOM (*e.g.*, solder) also scale the $\boldsymbol{K}$ matrix as per the applied thermal condition.

Virtual Design of Experiments

A virtual design of experiments was created based on all the possible combination of the system partitioning location and the two sets of MPC definitions applicable for the chosen ROM-FOM interface. The simulation results are compared with that of the original FOM (indicated in Figure 2) to find a few most accurate cases; and the required computational time was also compared. The DoE is summarized in Table 1 and Table 2. B-Sol, B-LF, and B-MC indicate a *beam* MPC definition utilizing solder, leadframe (copper), and moulding compound (EMC) materials, respectively.

Table 1 shows the variation of the accuracy of ROM-based simulations by comparing the percentage deviation of the maximum warpage value with respect to 0.04183 mm of the original FOM. Table 2 shows the comparison of model efficiency by comparing the surplus computation time in seconds of the ROM-based simulation with respect to 14.797 seconds for the original FOM. Note that this comparison only considers the time required for the SE use- pass, *i.e.*, the substructure generation time is excluded. Substructure generation time for all definitions of *MPC_1* remains close to the 30 seconds mark for the *Interface 1* and *Interface 3*, whereas it is around 40 seconds for the *interface 2*. Figure 6 shows the comparison of spatial plots of warpage of the remaining FOM for all combinations of the MPC definitions for the *interface 1*. Similar plots for the other two interfaces were also obtained.

Table 1: The percentage deviation of the maximum warpage value of the ROM-based simulation with respect to 0.04183 mm of the original FOM.

Legend:

< 5%	5-10%	10-15%	15-20%	> 20%

(a) Interface 1: between Package-LF and Solder Joint

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	-2.93	2.94	6.79		14.46
B-Sol	1.13	6.97	10.79		18.41
B-LF	2.48	8.31	12.13		19.74
B-MC					
Rigid	4.92	10.74	14.55		22.17

(b) Interface 2: within Package-LF

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	-0.82		5.10		10.39
B-Sol					
B-LF	6.50		12.42		17.67
B-MC					
Rigid	12.67		18.65		23.88

(c) Interface 3: between EMC and Package-LF

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	1.33		3.48	5.55	9.19
B-Sol					
B-LF	6.71		8.78	10.88	14.52
B-MC	10.19		12.29	14.39	18.02
Rigid	16.06		18.20	20.31	23.93

Table 2: The surplus computation time in seconds of the ROM-based simulation (use pass only) with respect to 14.797 seconds for the original FOM.

Legend:

< 40%	40-50%	50-60%	60-65%	> 65%

(a) Interface 1: between Package-LF and Solder Joint

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	5.00	10.28	8.39		4.45
B-Sol	6.44	8.80	8.70		6.41
B-LF	5.81	8.34	9.30		6.17
B-MC					
Rigid	5.02	7.31	7.20		4.73

(b) Interface 2: within Package-LF

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	7.25		7.06		5.50
B-Sol					
B-LF	7.56		9.58		7.14
B-MC					
Rigid	7.61		7.95		8.14

(c) Interface 3: between EMC and Package-LF

MPC1↓ \ MPC2 →	Deform	B-Sol	B-LF	B-MC	Rigid
Deform	10.03		10.20	10.20	8.64
B-Sol					
B-LF	8.78		8.70	9.30	8.36
B-MC	8.59		9.69	8.66	6.92
Rigid	5.89		7.16	9.38	5.25

4. Results and Discussion

The results obtained from the VDoE are compared for the quality and efficiency of the ROM-based simulations. The data in Table 1 and Table 2 are classified into several zones (denoted by colours) to highlight the observed trends. The reasoning behind a few MPC combinations are discussed and the possibilities of an overall optimal solution are explored.

The trends in Table 1 show that for all three interfaces, the inclusion of a *rigid* configuration in any of the *MPC_1* and *MPC_2* definitions gives the least accurate results. This is because a *rigid* configuration retains the original shape of the scoped geometry [6], which restricts thermal expansion in some ways and produces unrealistically high thermal stresses. Thus, a *rigid* configuration is not the most suited for thermomechanical problems. On the other hand, it significantly increases the time-efficiency of the SE use-pass, as indicated in Table 2. This also holds true for the time required for SE generation (not included in Table 2) for all three interfaces. It can be explained by the fact that a *rigid* definition treats all the scoped nodes as dependent, which eliminates a large number of DoF and greatly reduces the size of the stiffness matrix by, requiring fewer computational resources.

Inclusion of the *deformable* configuration generally keeps the accuracy high. With a *deformable* definition, FEM solver keeps the DoF of the scoped nodes independent, making it the same in number as in the original FOM. Thus, it does not gain much of an advantage in the efficiency as the *rigid* configuration, which is evident from the data in Table 2. Among various MPC combinations of the considered cases, the *deformable-deformable* configuration shows one of the most accurate results (see Table 1). But this consistency does translate to its time-efficiency, as observed by quite inconsistent trends in Table 2 across the three interfaces. Therefore, the suitability of the *deformable* configuration seems to be material dependent.

The results in Table 1 collectively indicate that it is important to consider the interfacing layers while choosing an optimal MPC configuration pair. The suitability of a MPC definition also depends on the material properties of the respective scoped geometries. For instance, consider the combination of the *deformable* and *rigid* definition for

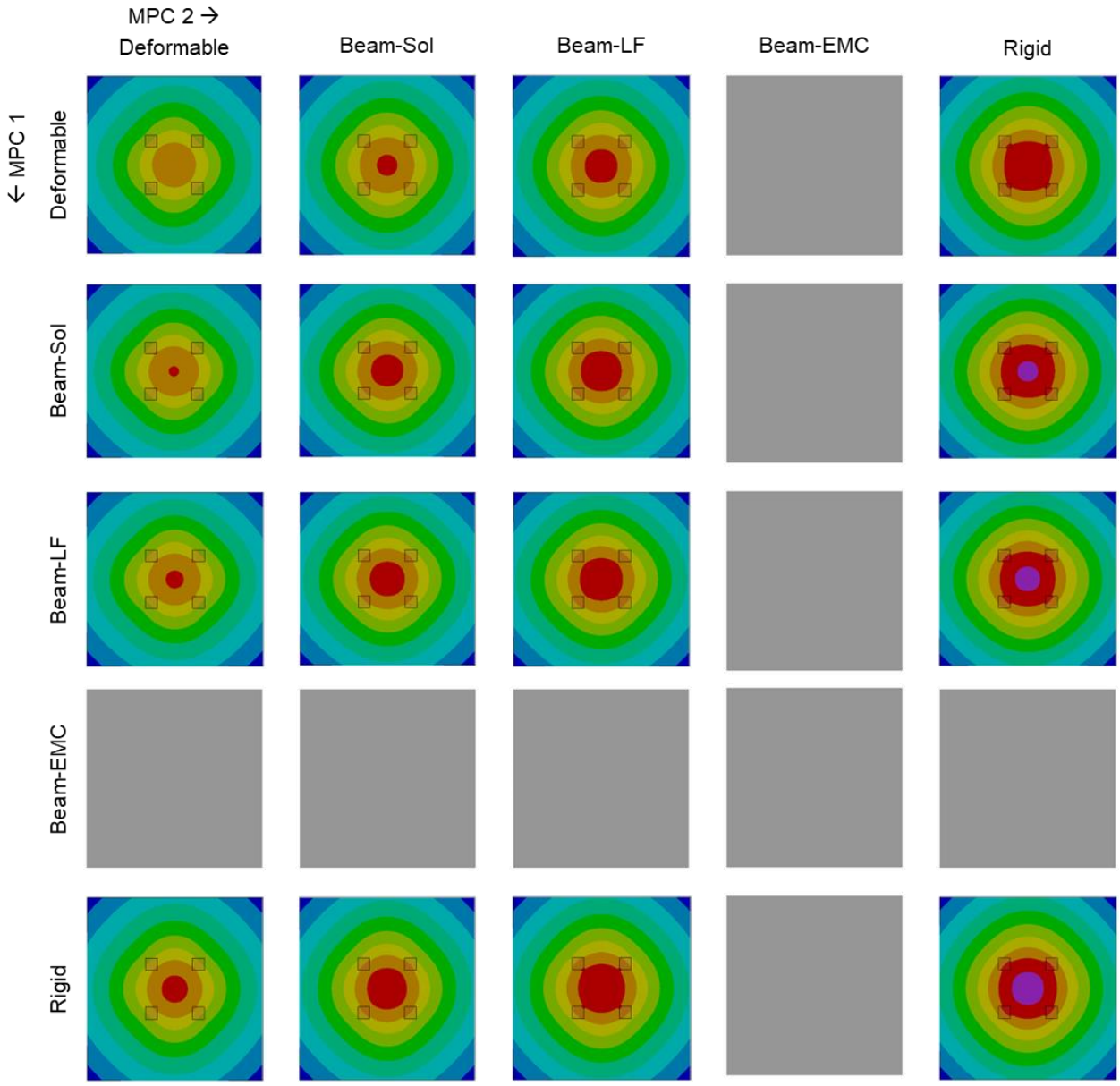

Figure 6: The comparison of spatial plots of warpage of the solder-PCB subassembly (FOM) for all combinations of the MPC definitions for interface 1. All subplots follow the same scale as Figure 2 for the out-of-plane deformation.

the *Interface 1*. It involves copper and solder, the former of which is much stiffer than the latter with a ratio of the elasticity moduli (E_{LF}/E_{sol}) ranging from 4:1 to 2.25:1. The *rigid-deformable* configuration pair works well with a less than 5% deviation of warpage with respect to FOM. Similarly, when the location of interface is moved to between the EMC and LF (*Interface 3*), the stiffness ratio of the scope geometry 1 and 2 (E_{EMC}/E_{LF}) is a much lower 1:6 compared to the *Interface 1*. The *rigid-deformable* configuration for this is one of the worst combinations for accuracy.

The same logic justifies the case where these MPC relations are swapped (the *deformable-rigid* configuration pair) being much worse for *Interface 1* (nearly 15% deviation) and slightly better for the *Interface 3*. This proves that the *rigid* configuration could be considered when a relatively stiff material is involved and should only be assigned to that scoped geometry. It can be paired with a *deformable* configuration if the other scoped layer has a relatively much lower stiffness.

A *beam* configuration sits in between the *rigid* and *deformable* configurations in terms of accuracy of results. However, the trend does not always follow an expected trend based on the increasing order of material stiffness values (which is EMC, solder, and copper). For the *Interface 1* (Table 1(a)), the colour trend clearly shows that the result accuracy of the *beamSol* and *beamLF* configurations fits perfectly between the *deformable* and

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rigid configurations in the order of their relative stiffness values. This can be observed in the spatial plots shown in Figure 6, where a gradual increase in the out-of-plane deformation is observed as a function of increasing column and row numbers.

For the *Interface 3* results (Table 1(c)), the order of decreasing result accuracy is followed only if *beamEMC* is placed after *beamLF*, which is the opposite of the order of relative stiffness. One of the reasons is that the EMC has a slightly lower CTE than LF, which allows less thermal expansion for the *beamEMC* configuration. In addition, EMC occupies a large volume in the package compared to any other materials. These two aspects combined put *beamEMC* closer to the *rigid* configuration than *beamLF* in terms of accuracy. In other words, a much higher volume fraction of EMC and a slightly lower CTE compensates for its lower stiffness. Thus, the quality of results also depends on a combination of material properties (stiffness and CTE) and the relative share of the chosen interfacing material in the ROM geometry.

Moreover, the *beam* configuration, by its definition, serves as a 'spot weld' joint. Thus, it would be more effective for geometries with a lower width to thickness ratio than the ones considered in this study, *e.g.*, a solder joint with smaller dimensions and higher standoff height.

Multiple cases in the DoE could be chosen as the overall optimal solution based on the deformation results and the time associated with the ROM use-pass. For example, all four cases with *MPC_2* set to *deformable* for the *interface 1* show the least deviation from FOM for the results and the surplus time. The *deformable-deformable* pair for the *interface 2* is the global optimum for accuracy and also gives an acceptable time-efficiency. Lastly, the *beamLF-deformable* and *beamLF-beamLF* are the only combinations for the *interface 3* which have a good balance of accuracy and efficiency.

5. Conclusion and Outlook

Reduced-order models can be more computationally expensive as opposed to the common belief of them always being more efficient than FOMs. However, ROMs facilitate IP protection, and thus, can be a great way of information exchange with external parties. The accuracy and efficiency of ROMs often compete with each other and need to optimized.

The VDoE shows that there could be more than one optimal solution when it comes to finding the most suitable location and MPC definition for a ROM-FOM interface. The inclusion of the *deformable* configuration generally results in higher accuracy. However, the optimal MPC choice depends on the thermomechanical properties of the involved material and also on its volume fraction in the ROM geometry, especially when the EMC is one of the interfacing layers. When a heterogeneous interface is involved, the ratio of stiffness and the disparity in CTE values should be taken into consideration when making a choice for a suitable MPC configuration.

The current work utilized a linear superelement that generates a thermal load vector corresponding to ΔT = 1 °C, which is then scaled according to the applied thermal load to get an effective load vector from the package-ROM. In future work, utilizing a temperature dependent SE would be explored by directly scaling the stiffness matrix of the SE (package ROM) instead of linearly scaling the resulting load vector. The effect of more than one master nodes per interface on the accuracy of the results would also be explored with the current and other shapes and aspect ratios for the solder joints.

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