MSc THESIS

Design of a Sub-harmonically Injection-Locked TDC Array for Space Applications

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Design of a Sub-harmonically Injection-Locked TDC Array for Space Applications

THESIS

submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL ENGINEERING

by

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Date : 31/August/2016

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Abstract

Over the past two decades, successful orbital missions undertaken to map the Earth, Mars, Mercury and the Moon have proved that light detection and ranging (LIDAR) measurements are powerful catalysts in space exploration. LIDAR based technologies help evaluate the topography of a land and its surface features along with gathering data to understand the habitability of planetary bodies by creating depth maps. In systems which involve time-of-flight (TOF) techniques, depth maps are created by sending a laser pulse to a target and detecting the reflected pulse by an appropriate photodetector. The detected signal is then supported by electronic circuitry which records the TOF and estimates the distance between the target and the laser source. Bound by the amount of measurements that a LIDAR should perform, there are many technical challenges due to varying system requirements like payload constraints, operating conditions in space, instrument size and power budget.

In this thesis, two major tasks were carried out, targeting imaging application in Ultraviolet (UV) and visible spectral range. A front-end readout circuit specifically designed for III-Nitride based UV avalanche photodiodes (APDs) is presented. Specific challenges of the readout are discussed in detail followed by measurement results. Further, a time-correlated single-photon counting (TCSPC) based TOF sensor is presented with silicon based single-photon avalanche diodes (SPADs) at the detector end. The sensor is fabricated in a 65 nm 3D IC CMOS technology, where the SPADs are integrated in the top tier and the processing electronics in the bottom tier. The 8x8 time-to-digital converter (TDC) array used to measure the TOF achieves a resolution of about 60 ps, thus providing a minimum measurable range of about 9 mm. The maximum achievable dynamic range is 150 m. The array incorporates concepts like coupling and injection locking to minimise the overall system jitter and provide a superior phase noise performance.

Acknowledgements

The past year working on my thesis has culminated into a rewarding one and I owe the result of this journey to many people who I came across. Foremost among them is my advisor, Prof. Edoardo Charbon. I would like to extend my utmost gratitude to him for giving me the opportunity to work on an exciting and challenging project. His vision oriented and critical discussions always ushered that additional motivation to continuously aim for the best.

I would like to extend my warm acknowledgement to Prof. Albert Theuwissen, who along with Prof. Edoardo instilled in me, adequate interests in the world of Image Sensors. Through their course, I could explore various possibilities in this field. My special thanks also go to Dr. Carl Jackson who offered to spend time during our monthly progress reviews.
Further, I would like to thank Prof. Lina Sarro to give me an opportunity to work on an exciting project on carbon nanotubes. I was exposed to a completely new realm of electronics in this venture.
Many thanks goes to Dr. Shouleh Nikzad, Dr. Bruce Hancock and Dr. Douglas Bell from NASA's JPL, who gave me a thoroughly enriching experience during my internship at JPL.

Further on, I would like to extend my sincere thanks to Augusto Ximenes to give me a chance to work with him to design the TOF imager. I cannot quantify how much I have learnt working with him. I am very grateful for all the technical tips I have gained through his expertise and the interesting discussions we have had through this project.

I am very grateful to Chao Zhang to help me kick-start in many of my first attempts in the past one year. It really helped me a lot in carrying forward independently. I am so glad that I had a wonderful group to be a part of. I would like to thank all my colleagues, who are also my friends now- Augusto, Bahador, Bishnu, Esteban, Arin, Ting, Rosario, Lin, Junjie, MJ, Michel and Siddharth. Their motivation and support meant a lot through this journey.
My special thanks to Antoon Frehe for his continuous technical support. His timely assistance at several times helped in accelerating my work.

I extend my special thanks to all my friends in Delft and abroad for the wonderful memories I cherish. They added an extra crown of happiness. Finally, I would like to extend my passionate thanks to my family in India who held patience for the two years of my Masters journey without seeing me and gave me invaluable support. Distance no bar, without them, I am nothing.

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Chapter 1

Introduction

1.1 Overview of 3D Vision

The capability to sense an environment and the ensuing reflexes have become driving factors for mankind to continually contribute towards development of sensors. Among the fascinating class of sensors, 3D vision systems have catapulted the interests of a number of technology enthusiasts in a variety of applications, for example, in the automotive sector, medical field, imagers to operate in space. The 3D vision-based image sensors enable creating depth map by estimating the distance of objects in a scene of interest with respect to a certain reference. Thus, they are popularly used for Light Detection and Ranging (LIDAR) application as a remote sensing technique for surveillance, identifying targets and navigation purposes. Several methods have been developed for such applications like the triangulation method, time-of-flight based systems, holography, interferometry etc. The work in this thesis focusses on the design of time-of-flight (TOF) based image sensors for space applications[1].
The basic measurement principle used in TOF imagers is to measure the time difference between a light pulse (more commonly a laser pulse) aimed at a target and the pulse which is reflected from that target. The underlying distance is then calculated based on the speed of light.

$$d = \frac{c}{2}.t_{TOF} \tag{1.1}$$

where d is the distance, c is the speed of light in vacuum and t_{TOF} is the time of flight. This method is also referred as the direct TOF technique. In an indirect TOF technique, the distance is estimated by calculating the phase difference between an emitted continuous wave sinusoidal signal and the reflected signal.
In another approach, the source of illumination (like a laser pulse) is synchronized to the photodetector to estimate the distance of a target from the source based on the time of arrival of single photons at the detector. This scheme is called as Time-Correlated Single-Photon Counting (TCSPC) and has been in use for several decades now. A similar approach has been incorporated in this work, the details of which are described in subsequent chapters.
Using TOF techniques for LIDAR applications require high speed photodetectors in order to detect the reflected optical signal along with fast front-end electronics to read out the detected signals. Geiger mode avalanche photodiodes have been a popular choice as detectors for TOF applications because of their high gain, high quantum efficiency and single-photon counting capability.

1.2 Image Sensors for Space Applications

Technological advancement has been a key catalyst for the implementation of 3D imaging systems with high performance and reasonable cost, thus accommodating applications from different spheres. That being said, while tailoring imaging systems for space application, it is very pivotal to recognize and understand the environmental conditions that exist in space and thus, develop 3D imagers which cater to such requisites. In this section, some of the imaging applications with respect to space are discussed.

1.2.1 Planetary Science

Planetary science applications focus on acquiring the surface topography of various bodies like the moon and other planets in the solar system. Characterizing the morphology of these bodies helps in analysing the habitability of planets. Several missions from NASA towards exploration of Mars, for instance have substantiated the evidence of life in the planet[2]. Most of the measurements performed in order to validate the finding have given valuable data concerning the atmospheric density variations, concentration profiles of various elements like hydrogen, oxygen, nitrogen etc have been achieved with LIDAR based imaging instruments.

1.2.2 Earth Science

Earth Science comprises of all the orbiting instruments which monitor the natural activities of the atmosphere and land. Many of these instruments are LIDAR based sensors helping climatic research reach new heights of precision and resolution. 3D Wind LIDAR is a popular example where pulsed lasers are used to extract wavelength shift occurring from atmospheric molecules as a result of wind[2][3]. Proven precision from the instruments used in the past repeatedly show that LIDAR based sensors are suitable candidates for such applications.

1.2.3 Landing Applications

Safe landing to target sites in hazardous terrains like that of moon and planets in the solar systems demand high accuracy. Since LIDAR vision system can deliver highly resolved 3D maps of a target terrain, they remain as key choice for such applications. The landing accuracy has considerably increased over several space flight missions undertaken to Mars, for example by NASA. Further more, valuable input about the proximity to land and an insight about the atmospheric conditions of a certain target can thus help in identification of probable landing zones for spacecraft and guarantee accurate guidance to safer navigation.

1.2.4 Space Rendezvous

A space rendezvous is required in order to align a spacecraft and a space station (or another space craft) in the same orbit. Thus, a LIDAR imaging system helps by providing accurate information on the position vectors and approach velocity of the two spacecraft during the rendezvous.

This feature is particularly also used for crewed missions to ensure accurate mating during re-entry to Earth, for instance.
The applications of LIDAR in space will continue playing an important role and the challenges associated with increasing need for high speed, high accuracy and large dynamic range will require innovation in sensor design and development phase.

1.3 Components of TOF Imager

1.3.1 Optical Source

Laser is used as a source of illumination to emit pulses with varying repetition rates and covering wide range of wavelengths. Especially for space applications, the wavelengths required range from 200 nm to 1000 nm, covering the electromagnetic spectrum from Ultraviolet (UV) to Infrared (IR). Several types of lasers from fiber to semiconductor lasers are being employed as LIDAR transmitters with high efficiency and optimal power operating over a range of temperatures for space applications described in the previous section.

1.3.2 Photodetector

Photodetectors are important components of a TOF imaging system. Catering to varying range of wavelengths, detectors with high responsivity at wavelengths of interest are required with single-photon counting capability. In this thesis, Gallium Nitride (GaN) based photodetectors for UV wavelengths (200-380 nm) and Silicon based Single-Photon Avalanche Diodes (SPADs) for visible and near infrared wavelengths are considered while designing the receiver electronics.

1.3.2.1 Silicon based SPADs

A SPAD is a p-n junction diode which is reverse biased above a certain voltage called the breakdown voltage to operate in a high gain region. Due to the presence of high electric field under such a bias, any photon impinging the surface of a SPAD may trigger impact ionisation, thus accelerating the process of electron-hole multiplication. This creates a situation of avalanche and the operation in this region is also referred to as the Geiger mode of operation. Thus, any incoming photon impinging the surface of the SPAD results in a sharp current pulse which is utilised to estimate the time of arrival of the photon in TOF applications. The I-V characteristics of a typical SPAD are shown in the Figure 1.1[4].
When a photon hitting the SPAD surface triggers an avalanche effect inside the SPAD, a front-end circuit is required which is capable of performing a course of action such that the SPAD can detect subsequent hits. The tasks performed by the front-end electronics include the following[4]:

- Sensing the avalanche
- Quenching the avalanche by reducing the bias across the SPAD
- Recharging the junction so that SPAD is biased to operate in the Geiger mode to detect another photon

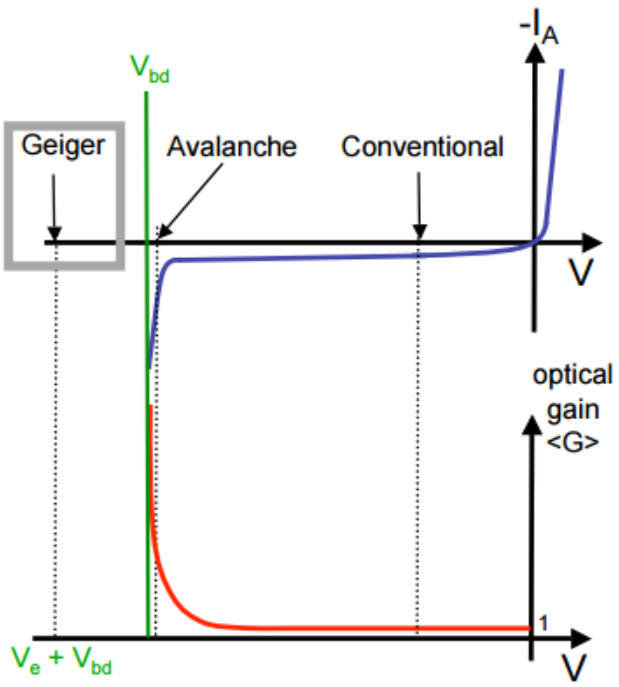


Figure 1.1: I-V characteristics of a typical SPAD in Geiger mode[4]

Further, the main parameters used to characterize the SPADs are photon detection probability (PDP) which determines the sensitivity of a given SPAD, the dark count rate (DCR) which defines the rate at which the secondary carriers trigger an avalanche in the absence of any illumination and timing jitter or timing resolution which reflects the fluctuation in the electric pulse generated by the front-end circuit after a photon hit. Usually timing jitter is expressed in terms of full width at half maximum (FWHM). The CMOS based SPADs have high spectral responsivity mostly in the visible wavelengths[5][6].

1.3.2.2 GaN Avalanche Photodiodes

The UV region in the electromagnetic spectrum is important in order to study about the stars, cosmos, galaxies along with the thin atmospheres in space. However, owing to the fact that UV instruments are starved of photons, photon counting detectors become an essential requirement. Gallium Nitride (GaN) and its alloys have been used to render solar blind UV Avalanche Photodiodes (APDs) due to their band gap nature (3.4 eV for GaN) enabling them to achieve high carrier multiplication and thus, a high gain in the UV region. These APDs have shown more than 50 % quantum efficiency[7]. The GaN APDs considered in this work were designed and developed at NASA's Jet Propulsion Laboratory in California. Figure 1.2 depicts the structure of one of the fabricated GaN devices.

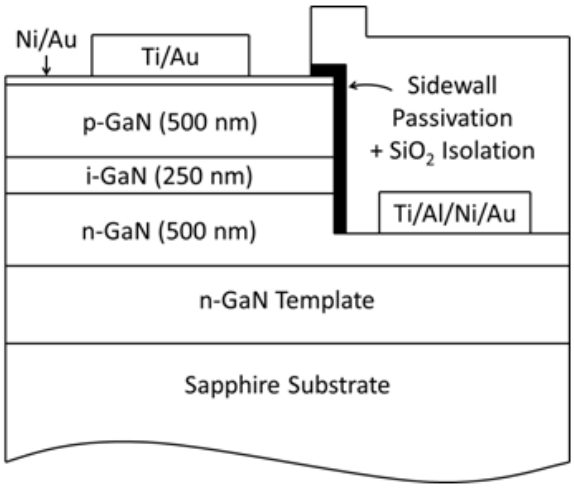


Figure 1.2: Device geometry of GaN APD[8]

As can be seen, these diodes are p-i-n structures based on a sapphire substrate which help reduce the defects and thus, leakage during device processing[8]. The GaN APDs were fabricated in varying sizes with diameters ranging from 10μm to 100 μm, achieving a gain as high as 2.5X10^5 in the UV wavelength. In the Figure 1.3, one can see the external quantum efficiency achieved from GaN APDs.

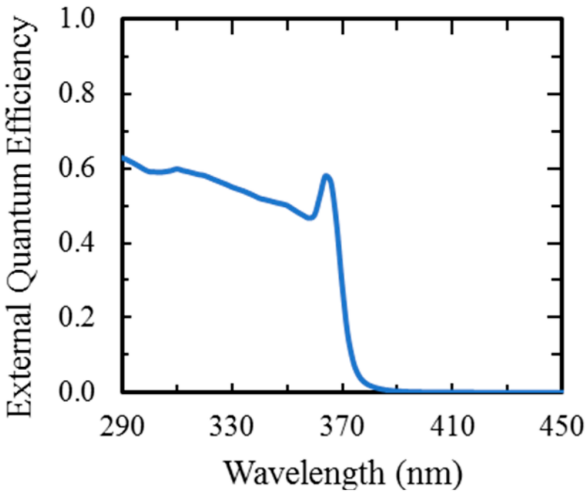


Figure 1.3: External Quantum Efficiency[8]

As can be seen in the above figure, these diodes provide an external quantum efficiency of about 60 % at 360 nm. The spectral responsivity of the GaN APDs at this wavelength is shown below in Figure 1.4. Further, similar to the principle described for SPADs, the GaN diodes need to be reverse biased at high voltages in order to facilitate carrier multiplication. However, the range of bias voltages required for the GaN APDs are in the range of 60-100 V[7]. A compatible front-end circuit is required to carry out the quenching mechanism and consequently, to readout the signal generated by the GaN APD.

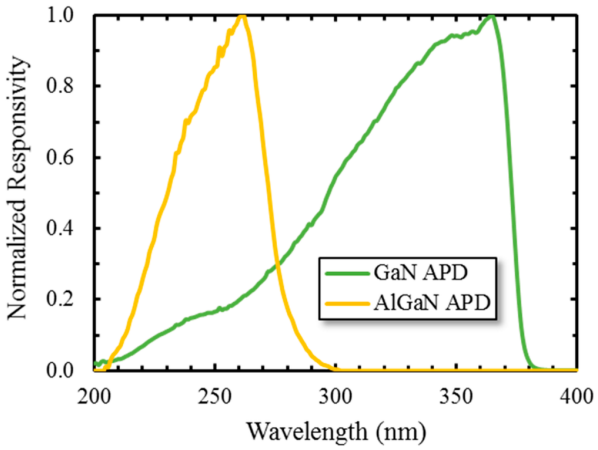


Figure 1.4: Normalized Responsivity[8]

1.3.3 Electronic Circuitry

Electronics play a crucial role in any space related missions. Special focus is required to achieve low power, high speed integrated readout electronics in order to have optimum performance with the detectors described above, especially when low size and compactness also become important factors. Planetary sensor and instrumentation need electronics operating over wide range of temperatures along with high performing design metric. When considering single-photon counting detectors, a compatible solution for front-end electronic readout along with high speed back-end circuitry are both typically necessary to build a TOF Imager. In this thesis, for the GaN APD discussed in the previous section, a hybrid structure is proposed where the detector is bonded to a readout integrated circuit (ROIC) designed and fabricated in silicon. The bonding is proposed to be done using indium bumps at JPL. Furthermore, a 3D IC CMOS technology has been exploited to develop a prototype for a TOF application integrated with SPADs at the detector end.

1.4 Organization of Thesis

The thesis is organized as follows.

- Chapter 2 focusses on the front-end electronics developed for the GaN detectors designed at JPL. It describes the detector characteristics, the challenges and specifications for the readout circuit and finally, the implementation of the circuit.
- Chapter 3 delves into the working principles of the TDC for the TOF application along with a simulation based analysis of the core concepts used in the design.
- Chapter 4 discusses the building blocks of the TDC and describes their circuit level implementation along with their layouts.
- Chapter 5 explains the measurement results obtained from the GaN readout circuit and the post-layout simulation results obtained from the TDC.
- Chapter 6 concludes this thesis summarizing the findings from this work and gives an insight on future scope.

Chapter 2

Front-End Electronics

In the previous chapter, an overview of two different kinds of detectors for visible and UV wavelengths was discussed. This chapter describes the CMOS readout circuit designed for the GaN detectors. The GaN sensor proposed here is a hybrid structure where the detector is processed in III-Nitride material and readout circuit is designed and fabricated in silicon, to be later hybridized using Indium bumps. The readout circuit is designed and fabricated in 0.35 µm high voltage CMOS technology.

2.1 CMOS Readout for GaN APDs

Detector characteristics- As introduced in Section 1.3.2.2 of Chapter 1, GaN APDs offer high gain and spectral responsivity in the UV region. These APDs when biased at a voltage in the range of 60-80 V, generate a current on the order of hundres of picoamperes. A typical I-V characteristic of one of the GaN devices is shown below in Figure 2.1.

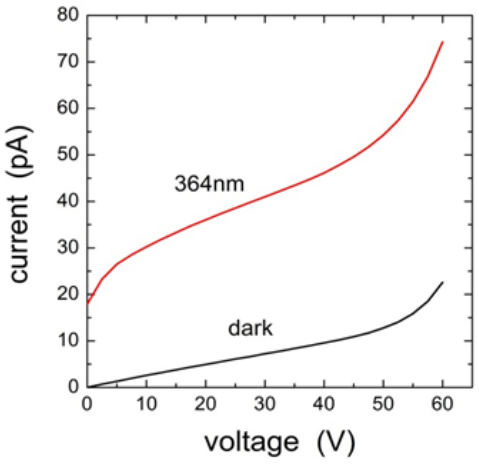


Figure 2.1: I-V characteristics of GaN APD[7]

The GaN APDs require beyond 90 V to avalanche and not all of the fabricated devices can sustain avalanche without any self-damage. Thus, the readout at this point, was designed for the GaN APDs operating in the linear mode; the characteristics of the APDs in this mode are shown in Figure 2.1. As can be seen, the GaN detectors still require very large bias voltages, about 60-70 V to facilitate electron multiplication in the linear region. Thus, it was furthermore important to account for the high reverse voltages applied on the photodiodes and ensure isolation from the low voltage CMOS circuit to prevent any damage to the device and/or the readout.

2.1.1 Readout Specifications

Based on the detector characteristics, an equivalent diode circuit model was chosen, consisting of the photodiode current along with its equivalent capacitance. The primary goal of this work was to assess and derive the percentage of readout compatibility with the detectors. A simple Capacitive Transimpedance Amplifier (CTIA) was thus designed based on the given specification and constraints from the detector end.
As shown in Figure 2.2, the basic idea of the CTIA would be to integrate the incoming photodiode current (I_{pd}) on the feedback capacitor (C_{fb}) and generate an equivalent output voltage such that the low-frequency DC gain would be set by the ratio of photodiode capacitance (C_{pd}) and the feedback capacitance (C_{fb}). The feedback capacitor is reset by the transistor (MP_{reset}) before every integration. As soon as the reset switch is released and the photodiode current starts to flow in, the voltage at the input node starts to rise, causing the output voltage to fall. The small rise at the input node is due to finite gain (A) of the CTIA. The negative feedback of the amplifier however, maintains the input node at virtual ground and the output of the amplifier thus starts to drop from the initial value set by the reset transistor.

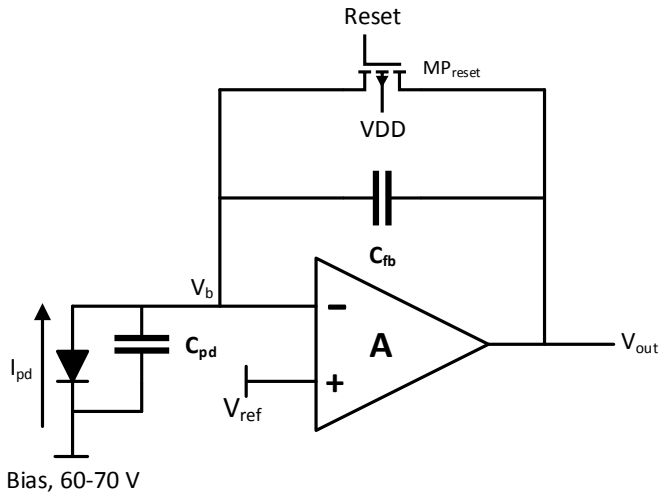


Figure 2.2: CTIA Basic Principle

Thus, the incoming photodiode current is neatly integrated via the feedback path, generating an

output voltage corresponding to the following equation.

$$I_{pd}(s) + \frac{V_{out}(s)}{A}(sC_{fb} + sC_{pd}) = V_{out}(s)(sC_{fb}) \tag{2.1}$$

where, A is the open loop gain of the amplifier. Thus when A$\gg\frac{C_{pd}}{C_{fb}}$,

$$V_{out} = \frac{1}{C_{fb}} \int I_{pd} dt \tag{2.2}$$

The target specifications for the CTIA are made based on the characteristics of the detectors described above. These photodiodes are reverse biased at voltages in the range of 60-100 V, generating currents on the order of a hundred pA. Some of the important design characteristics are:

- The equivalent photodiode capacitance is estimated to be around 1 pF, thus giving us the freedom to choose C_{fb} based on the gain required. In this design, three different gains are provided by using different C_{fb}.
- CTIA operating bandwidth is chosen to be on the order of 1 MHz, given that the timing performance of the GaN devices is on the order of several hundred µs to a few ms.

With the given information on the detectors, an approximate target specification for the readout was derived. The following table summarizes those specifications.

Table 2.1: Summary of CTIA Specifications

Parameter	**Specification**
Transimpedance Gain	Around 50 dB
3 dB Frequency	$\approx$ 1 MHz
Feedback Capacitance (C_{fb})	Variable (50, 150, 450 fF)
Load Capacitance (C_{load})	30 pF
Input Capacitance (C_{pd})	1 pF

2.1.2 CTIA-Design and Implementation

The choice of an amplifier topology for the CTIA was driven by the requirement of target specifications, certainly and simplicity. Thus, a common-source structure and a cascoded architecture were considered as initial choices. A cascoded structure guarantees additional gain by boosting the output impedance when compared to a common-source stage. However, given that the bandwidth and gain requirements are not high, a common-source architecture is used as the core cell for the CTIA design in this proof-of-concept. Figure 2.3 shows the circuit diagram of the designed CTIA. In order to not degrade the voltage level at the output and drive the output pad, an NMOS source follower (MN2-MN3) is used as an output buffer. Additionally, another source follower circuit (MN4-MN5) is connected to the input of the CTIA to track the voltage at the input node, V_b. The tracking of the input node is specially useful in case of a current surge, for instance during an avalanche. The details of providing a source follower to monitor the input will be revisited in the subsequent section.

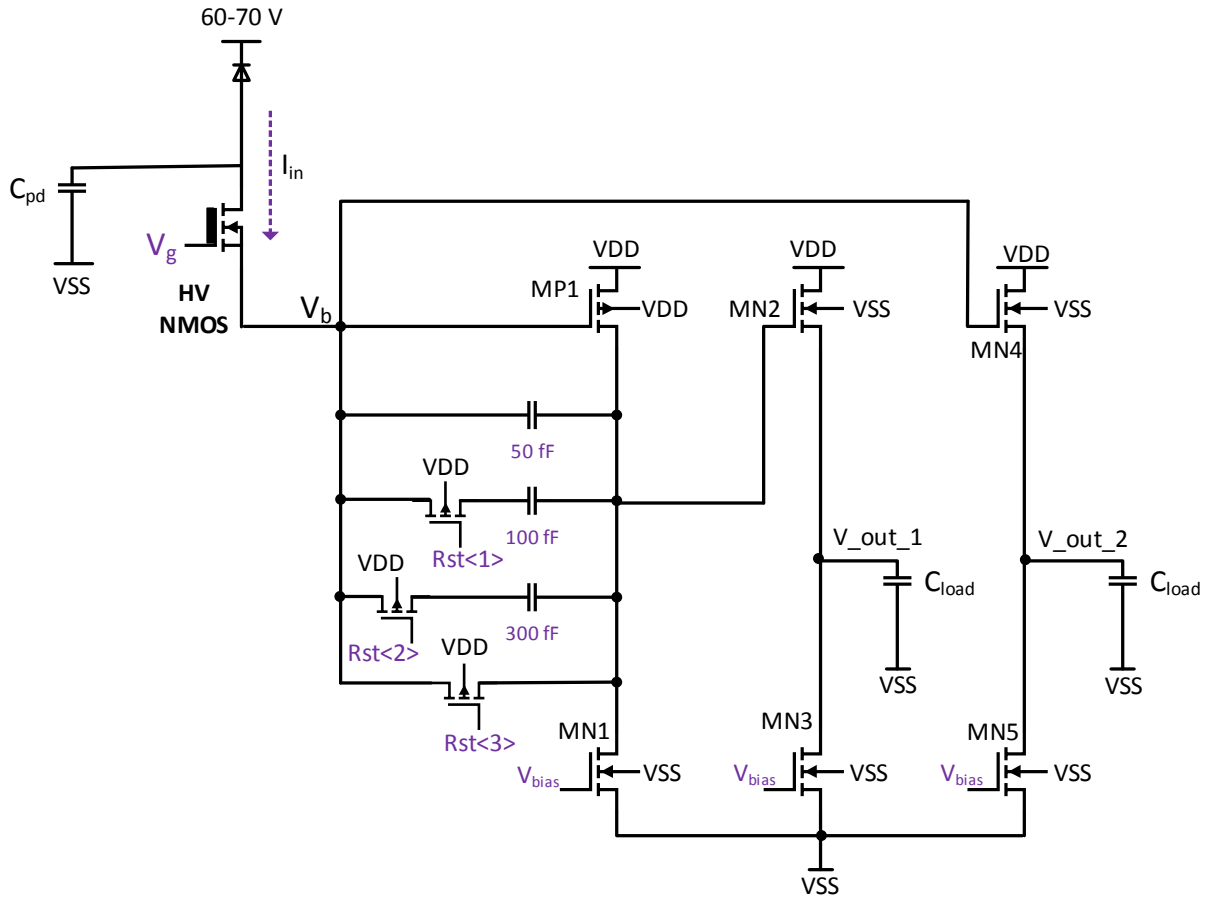
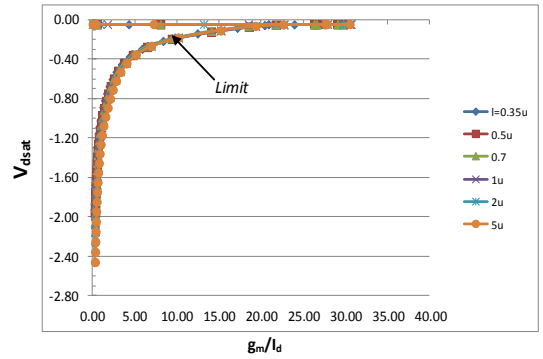
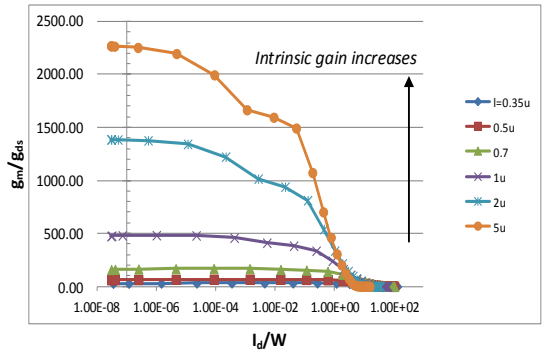


Figure 2.3: Transistor level schematic- CTIA

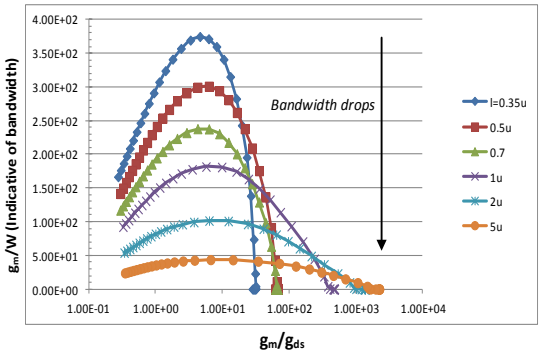
Since the GaN APD is of p-on-n type; in other words, the structure of the GaN device (shown in Figure 1.2) is based on a n-type sapphire substrate. Hence, when the substrate is biased at the high positive voltage, a positive current will flow into the amplifier. For the same reason, a PMOS input (MP1) with an NMOS load (MN1) is selected. A PMOS transistor with Rst<3> pin to control its gate is used to reset the feedback capacitor and bias the CTIA transistors in the appropriate operating points. The bias voltage (V_{bias}) for the load is generated from a simple current mirror. The first step towards designing the CTIA circuit was to estimate the performance characteristics of the PMOS and NMOS transistors in 0.35 µm technology. Several characteristic plots were derived from the simulations on the PMOS and NMOS transistors. Parameters like the intrinsic gain of the transistor g_m/g_{ds}, the transconductance-to-drain current ratio g_m/I_d, and the overdrive voltage V_{dsat} and their relationships were obtained to size the transistors with appropriate width (W) and length (L). Following are the plots shown for the PMOS transistors in Figure 2.4. Similar plots were obtained for NMOS transistors before choosing their dimensions.



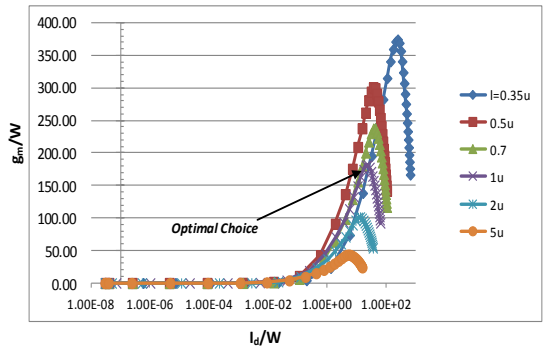
(a) V_{dsat} vs g_m/I_d



(b) g_m/g_{ds} vs I_d/W



(c) g_m/W vs g_m/g_{ds}



(d) g_m/W vs I_d/W

Figure 2.4: Simulated performance characteristics of PMOS transistor in ams 0.35 μm process

All of the above simulations were performed over increasing channel lengths of the transistor. As can be seen from the above plots, in order to have a high g_m/I_d, there was indeed a limit on the V_{dsat} (here, 0.2 V in order to have a g_m/I_d of 15). Another interesting fact from Figure 2.4b was selecting the correct channel length for the input PMOS (MP1 in Figure 2.3) to ensure high intrinsic gain as the minimum length transistor cannot provide a high gain for the required g_m. From Figure 2.4c, one can see that the bandwidth significantly drops for longer channel lengths. Considering the constraints for the design and based on the above modelling, 1 μm was selected as an optimal choice for channel length as can be seen in Figure 2.4d. The sizing of all the transistors were similarly derived. Further, based on the values of the bandwidth and the load capacitance, the g_m of the input PMOS is estimated according to the following equation:

$$g_m = 2\pi.f.C_{load} \tag{2.3}$$

A g_m of 0.18 mS was chosen as a target derived from the above equation for the required speed from the CTIA. Thus, with a g_m/I_d requirement of about 15, this translated into an equivalent current of $\approx$12 μA to obtain the required gain and bandwidth.

2.1.3 Design Challenge

One of the biggest challenges in this design was to protect the low voltage CMOS readout circuit from the high reverse bias voltages applied on the photodiode. Furthermore, when a photon is

detected, the hot carrier that is produced creates an avalanche in the detector layers due to the high electric fields in the device. This is the mechanism for gain in APDs. However, the carrier multiplication must be quickly quenched to avoid damage to the APD. Exploiting the high voltage technology used in this design, a convenient solution was to use a HV NMOS transistor (shown in Figure 2.3 and in Figure 2.5 below) as a clamp.

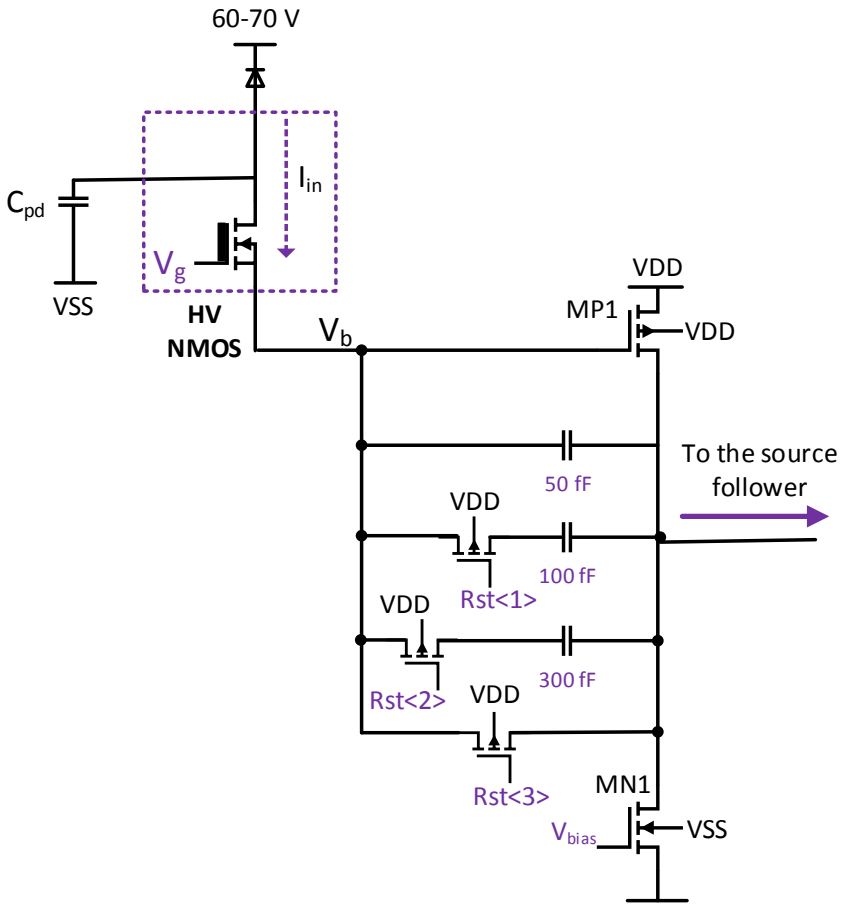


Figure 2.5: HV NMOS as a protection to the low voltage CMOS Readout Circuit

The clamp bias is set such that, initially, this transistor is in its ohmic region. Under this starting condition, the detector sees full bias since there is little voltage drop across the HV NMOS. Eventually, after the integration is complete, as described before, the input voltage V_b begins to rise as the incoming current can no longer integrate on the feedback capacitance. If this is left unattended, the rising input voltage can exceed to damaging levels. However, in this design, the rising input in turn reduces the gate-to-source voltage of the HV NMOS and eventually, this transistor shuts off. When this happens, the incoming photodiode current will stop flowing through the HV NMOS and end up charging the photodiode capacitance C_{pd}. This action results in reducing the bias across the diode and this is specially, useful in case of current surge during avalanche.

Thus, when there is an avalanche breakdown, following course of action will happen in the CTIA circuit:

- Integration of the current
- Saturation of the CTIA
- Shut-off of the HV NMOS
- Reduction in diode bias and eventually, quenching

The high voltage on the APD will appear at the drain of the HV NMOS, but the technology limits for this transistor allows us to exploit it for this purpose. After the shutting off of the HV NMOS, the CTIA should be reset which sets the appropriate operating points for all the transistors and at this point, another integration cycle can resume.

2.2 Summary

In this chapter, a readout circuit for the GaN detectors was described. The proposed circuit will support the GaN detector array to carry out initial measurement and help assess the compatibility with CMOS. Measurement results from the hybrid combination will cater to better understanding of the timing resolution of the APDs and add valuable suggestions in terms of design metrics to develop superior designs in future. For instance, the currently employed manual reset signal can be replaced with timed/ programmable ones eventually. Additionally, if these detectors are able to sustain avalanche in future, single-photon counting applications will find a place and appropriate back-end electronics can then be designed with these detectors for TOF applications. The detectors can be directly connected to CMOS processing electronics via bump bonding thus facilitating high degree of parallelism and scalability such that any electronic circuitry can be scaled in proportion to the size of the detector array. Given the benefit of hybridization, there are going to be specific challenges accompanying this technique. Bump bonding, usually adopted for hybrid sensors, does not permit small pitches and thus, the benefit of scalability comes only at a cost of occupying larger area with such interconnection. Nevertheless, progress towards evaluating the compatibility of substrates, ie, between Silicon involved in CMOS technology and detector substrates will bring some advantage to mitigate this challenge.

Chapter 3

TOF Measurement- Background and Analysis

Designing and testing a front-end circuit for GaN APDs described above is the first step in the direction of building UV imagers with these detectors. This front-end prototype is seemingly helpful to assess the performance of GaN detectors and their compatibility with CMOS circuits. However, in order to achieve single-photon counting capability, these GaN APDs need further development at the process and device level to operate sustainably in the avalanche mode. Thus, within the scope of this thesis, a TOF measuring circuit is proposed with SPADs at the detector end. This TOF circuit prototype will help substantiating some of the key concepts utilised in the design, to be later incorporated with detectors of any kind. Furthermore, a 65 nm CMOS technology is used to design the ASIC with SPADs bonded to them through 3D connections. A conceptual representation of a 3D IC technology is shown below:

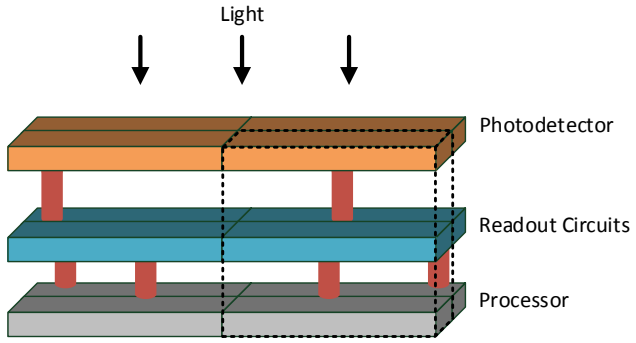


Figure 3.1: Conceptual Representation of 3D IC technology (Redrawn from [19])

This chapter describes the concepts used in the TOF measurement along with their working principles followed by a section on analytical simulations.

3.1 TOF Measurement- Core Concepts

3.1.1 Introduction- Time-to-Digital Converter

A time-to-digital converter (TDC) is utilised to determine the time of flight of the photons incident on a SPAD. There are generally two ways to measure this; in one approach, the time delay is measured between the start time being triggered by the signal which is captured by the SPAD and a laser pulse which further communicates a signal for the stop pulse. This is then quantized into a digital code. The simplest way to measure the time interval using this method is based on a counter. A simple timing diagram illustrating the concept is shown below:

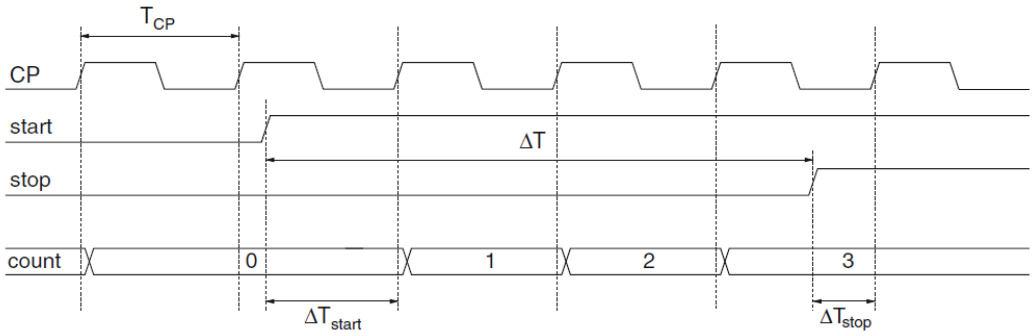


Figure 3.2: Working principle of a counter based TDC[9]

The interval is measured by counting the number of clock cycles such that:

$$\Delta T = NT_{CP} + \epsilon_t \tag{3.1}$$

where,

$$\epsilon_t = \Delta T_{start} - \Delta T_{stop} \tag{3.2}$$

In another approach which is partly also used in this thesis, an event-driven method is incorporated where the time of flight is measured only when an incoming photon triggers the SPAD and thus, records an event. In this case, the SPAD signal acts like a stop pulse. Before delving into the details of concepts used in this work, the design specifications are briefly discussed.

3.1.2 Design Specifications

In this design, a subgroup is a self contained structure, defined as a group of 64 pixel circuits laid out in 8 rows and 8 columns. A TDC is shared between two such subgroups to measure the TOF of photons. In this architecture, the TDC runs all the time and the TOF information is generated with respect to the sampling of an event by the SPAD. This technique, thus permits multiple samplings and more number of events to be detected over a single frame. The pictorial representation of the subgroups along with the shared TDC structure is shown below in the Figure 3.3.

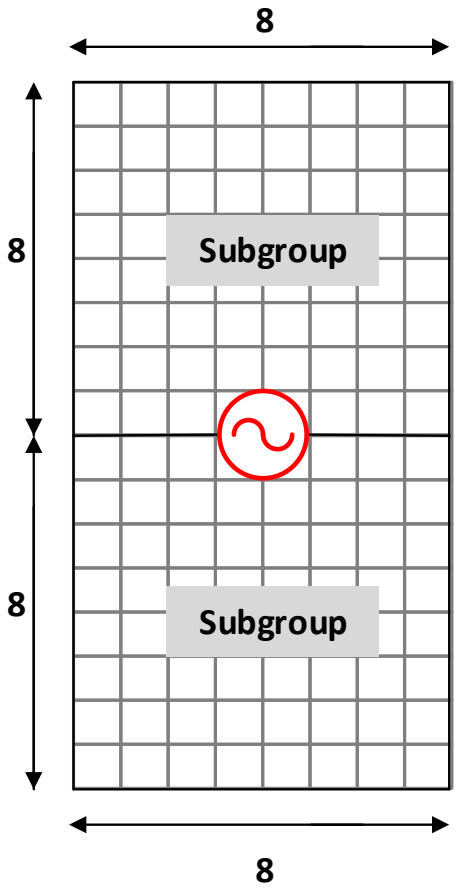


Figure 3.3: Pixel-TDC Structure

For a LIDAR intended for space applications, where a depth map is desired, it is important to have a reasonable resolution and dynamic range. For instance, a typical tracking operation would need a range as high as 5000 m or more and on the contrary, at shorter distances of about 100m, an imaging LIDAR can be used for docking purposes. Thus, in this work, a short distance range has been considered with a maximum achievable range of about 150 m and a resolution of 9 mm[3]. This resolution in the space domain translates into an equivalent timing resolution of about 60 ps in an optical medium. In any TOF measuring system, the achievable resolution is dictated by different noise sources in a system. These sources arise mainly from the jitter of the SPAD, the TDC quantization noise and the integrated RMS jitter in the TDC. Considering that these noise sources are statistically independent, the total contribution from each of them can be written as a sum of their variances.

$$\sigma^2{}_{total} = \sigma^2{}_{spad} + \sigma^2{}_{TDC,jitter} + \sigma^2{}_{TDC,quantization} \tag{3.3}$$

Translating Equation 3.3 in terms of full width at half maximum (FWHM) expression gives,

$$FWHM_{total} \approx \sqrt{FWHM^2{}_{spad} + 2.335.\sigma^2{}_{TDC,jitter} + 2.335.\sigma^2{}_{TDC,quantization}} \tag{3.4}$$

where, the TDC quantization noise is given by the following equation[16].

$$\sigma^2{}_{TDC,quantization} = \frac{t^2{}_{res}}{12} \tag{3.5}$$

Here, t_{res} is the resolution of the TDC. In a TOF system like this, the major contribution to the noise arises from the SPAD jitter and the rest is dictated by the TDC as can be seen from the above equations. The core of the TDC used in this design consists of a counter which is used to measure the integral part of the TDC final code and a closed loop voltage controlled ring oscillator (VCO) which is used to estimate the fractional part of the TOF being measured. VCO, thus determines the resolution of the TDC. Considering that the resolution required is about 60 ps, this implies an equivalent standard deviation of about 17.32 ps from the TDC quantization noise according to Equation 3.5.

Further, in order to quantify the jitter contribution from the TDC ($\sigma^2{}_{TDC,jitter}$), a typical figure of merit (FOM) widely used to compare qualities of VCO is used. This FOM is derived by considering the oscillation frequency of the VCO, the power dissipation and the offset frequency at which the phase noise is measured as shown below[17].

$$FOM_{VCO} = 10log\Big(\mathcal{L}_{VCO}(f_m).\frac{f_m}{f_{osc}}.\frac{P_{VCO}}{1mW}\Big) \tag{3.6}$$

where, $\mathcal{L}_{VCO}(f_m)$ is the phase noise of the VCO, f_m is the offset frequency at which the phase noise is measured, f_{osc} is the oscillation frequency of the VCO and P_{VCO} is the power dissipation. The unit of FOM_{VCO} is in dBc/Hz. A FOM of -160 dBc/Hz was used as a target to derive the phase noise requirements on the VCO at 1 MHz offset frequency and a VCO oscillation frequency of 1 GHz based on Equation 3.6. With a power budget of about 200 µW for the VCO, the resulting phase noise requirement was -93 dBc/Hz at 1 MHz offset frequency. Finally, the integrated rms jitter is calculated to be close to 16 ps. This is obtained by integrating the phase noise over a bandwidth (in this case, from 100 kHz- 100 MHz), the typical calculations for which are shown in Appendix A. An additional advantage of a resolution of 60 ps is the possibility to consume lesser power due to almost equal contribution of the TDC noise sources, with $\sigma_{TDC,jitter} = \sigma_{TDC,quantization} \approx 17$ ps in Equation 3.3.

The $FWHM_{total}$ in Equation 3.4 is now calculated based on the contribution from the three main noise sources described. Having estimated the values of the TDC jitter and its quantization noise, the remaining entity is the SPAD jitter. To evaluate the maximum value for $FWHM_{total}$, the best case value for SPAD jitter (65 ps FWHM) is considered based on the work from the past[6]. Thus, $FWHM_{total}$ in Equation 3.4 results in a value close to 80 ps. With this estimation, the TDC resolution is still enough for the application requirement.

Further, the aforementioned dynamic range of 150 m implies a TOF measurement range of about 1 µs. With the TDC dynamic range of 14 bits, it is possible to meet the requirements of this application with a resolution of about 60 ps achievable from the VCO and a high-frequency counter running at 1 GHz.

As shown in Figure 3.3, the sharing of TDC between two subgroups provides an advantage in terms of area for the TDC per subgroup. Based on the total area available for the subgroups with the TDC, the area available for the TDC was approximately 150 µm x 10 µm, such that the TDC area per subgroup was half of this value. The table below summarizes the design specifications for the TDC.

Table 3.1: TDC Specifications

Parameter	**Value**
Technology	3D IC 65 nm CMOS
TDC Area	≈150 µm x 10 µm
TDC Resolution	60 ps
TDC Dynamic Range	14 bits
Target resolution (in distance)	9 mm
Maximum Range (in distance)	150 m
Phase Noise at 1 MHz offset frequency	-93 dBc/Hz

Since integrated jitter is of substantial concern, much focus in this work has been given on minimising this figure. With an aim of keeping the jitter minimal, several concepts have been used for this purpose. Coupling of oscillators and sub-harmonic injection locking are two of the main concepts exploited in this design to suppress the phase noise of the VCOs. These concepts are introduced and analysed in this chapter and the circuit level design and implementation is described in the next chapter.

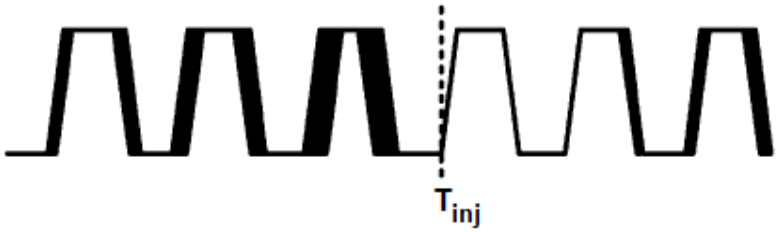
3.1.3 Coupled Oscillator Network and Sub-harmonic Injection Locking

The effect of integrated jitter in the time domain is reflected as phase noise of the oscillator in the frequency domain. Ring oscillators (also used in this design) are generally prone to accumulated jitter and thus, result in poor phase noise performance. Thus, quite often closed loop ring oscillators are preferred in a phase-locked loop (PLL) with a reference signal which has a superior phase noise performance. Additionally, in a distributed system which consists of a network of oscillators, every oscillator node is coupled to its neighbouring node, facilitating "mutual interaction". Such a mutual coupling between the oscillators results in synchronization over time due to a non-linear phenomenon known as Injection Locking. This phenomenon has been exploited for a long time now in order to improve the overall phase noise characteristics of the oscillators in a network.
When a signal of a certain frequency is injected, there is a shift in the oscillator frequency from its free-running value to that of the injected signal or one of its harmonics based on the frequency of injection. When this happens, the phase noise of oscillators is considerably reduced as it injection-locks to this cleaner reference signal[11]. This is typically in accordance with the following equation,

$$S_\phi = S_{inj} + 20log_{10}N_{inj} \tag{3.7}$$

where, S_ϕ is the output phase noise, N_{inj} is the ratio of the oscillator frequency to the injection frequency and S_{inj} is the phase noise of the injected reference. In the time-domain, this effect implies the correction of zero crossings of the oscillator waveform every rising edge of the injection signal due to realignment. This eventually results in the reduction of the accumulated jitter, the conceptual representation of which is shown below in Figure 3.4.

(a) Free running oscillator



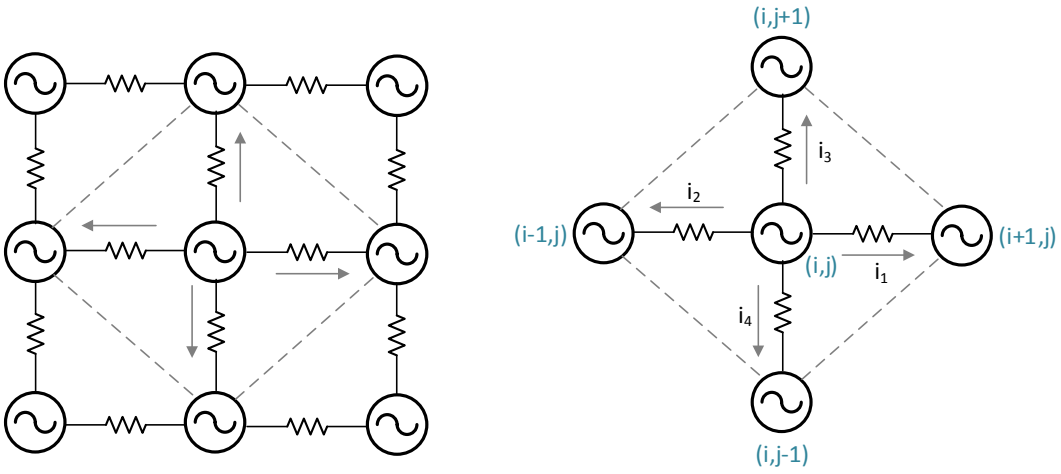
(b) Injection locked oscillator

Figure 3.4: Concept- Jitter Reduction due to injection locking[10]

As can be seen from the above figure, an injection signal at time T_{inj} results in the realignment of the oscillator edge with that of the injected signal, thus leading to a reduction in the accumulated jitter. For the above reasons, in this TOF design, the TDCs along with the subgroups are laid in an arrayed fashion such that the VCO in every TDC is coupled to the VCO of the neighbouring TDC, thus forming a mesh of coupled oscillators internally. Along with that, the VCOs are phase locked to a sub-harmonic reference signal, which serves as the injection pulse. The mutual coupling between the VCO cells along with the reference signal being injected, causes realignment as described above. This action usually results in perturbations in the form of tiny charge injection until the VCOs in the network synchronize over time. In the next section, these concepts are modelled and analysed with simulations performed on MATLAB.

3.2 Analysis of Coupling

In order to understand the concept behind the synchronization of coupled oscillators and injection locking, analytical simulations were performed on MATLAB. In this section, coupling phenomena is primarily discussed to explore and understand the dynamics involved in this process. Considering a mesh of coupled oscillator network, every oscillator is directly coupled to 4 other oscillators as shown below in Figure 3.5. Every grid point in the mesh represents a coupled oscillator node. The coupling between the oscillators has a finite impedance. Whenever there is any phase misalignment among the oscillators, a current proportional to the phase error will flow through this coupling, trying to bring back the misaligned oscillators into a phase lock condition. This is basically the action of injection locking phenomenon taking place in the mutually coupled network. When the oscillators, over time attain injection lock, there would be no current flowing in between the coupled nodes and the oscillator network becomes synchronized again. In the unit cell described above, these injection currents are denoted as i_1, i_2, i_3 and i_4 in the X and Y direction.



(a) Mesh of Coupled Oscillator Network **(b)** A Unit Cell- Coupling with 4 adjacent oscillators

Figure 3.5: Oscillator Network

Several works have been done in the past to model coupled oscillator networks in applications spreading across various domains and most of the analysis has been inspired from the famous Adler's Equation. The generalized Adler's equation is utilized to analyse injection locking in any kind of oscillator[12][13]. In this work, ring oscillators are considered and in order to analytically model this phenomenon in ring oscillators, a nonlinear phase macromodel based approach has been exploited to capture the dynamics of injection locking. An oscillator would ideally give a periodic steady state response synchronized with other oscillators in the network. However, in situations of phase misalignment, the synchronization gets perturbed as mentioned above, giving rise to minor currents flowing through the coupling between individual oscillators. These currents thereby act as perturbations to the otherwise, steady and periodic nature of the oscillator.

The theory for simulating this phenomenon is based on describing the oscillator dynamics by an ordinary differential equation. This equation is developed by formulating the nodal equations at the coupled node of the ring oscillator. Since, this method also aligns with the nodal analysis used in circuit simulators, the formulation of differential algebraic equations to describe the oscillator dynamics coincided well in the nonlinear phase macromodel. The numerical analysis of the perturbations counts on the Floquet theory of periodically time varying systems of ordinary differential equations. The macro modelling techniques are based on the fact that the injection mechanism due to perturbation affects the phase of an oscillator response more than any amplitude variation[14][18]. The steady state response of an oscillator in the absence of an injection signal (referred as the unperturbed condition) is given as

$$V_s(t) \tag{3.8}$$

$V_s(t)$ is obtained by numerically solving the differential equation pertaining to an oscillator. Further, the perturbed steady state solution in the presence of a perturbation denoted as $b(t)$ is described by,

$$V_s(t + \alpha(t)) + y(t) \tag{3.9}$$

where $\alpha(t)$ is the phase shift deviation caused due to the external perturbation $b(t)$. Thus, the perturbed solution approaches the unperturbed solution when time shifted by a value close to $\alpha(t)$. The term $y(t)$ is the orbital deviation reflecting any amplitude variation, in the presence of this external perturbation. However, considering that the orbital deviations are small[14][18], the perturbed steady state solution reduces to the form,

$$V_s(t + \alpha(t)) \tag{3.10}$$

Every oscillator is mathematically modelled by a set of nonlinear, coupled differential equations by applying the Kirchoff's current law at every coupled node. Since, the goal of the analysis was to understand the dynamics of coupling, a simple three phase single-ended inverter based oscillator with an RC load is assumed for an oscillator cell. Further, the coupling between the oscillators is considered as a π type RC network as shown in the Figure 3.7.

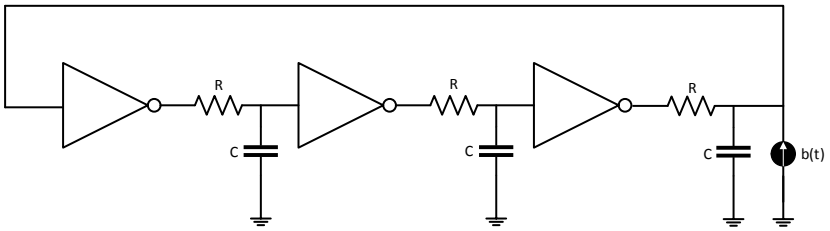


Figure 3.6: Ring oscillator model used

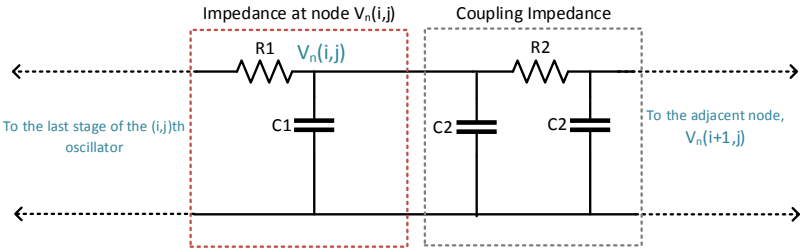


Figure 3.7: Coupling impedance model

Applying Kirchoff's current law to a node at position (i, j) by taking into account the currents from adjacent oscillators, the corresponding differential equation is described as,

$$\frac{dV_{(i,j)}}{dt} = \frac{f(v(t)}{R1(C1 + 4C2)} - \frac{V_{(i,j)}}{R1(C1 + 4C2)} + \frac{V_{(i+1,j)} + V_{(i-1,j)} - 2V_{(i,j)} + V_{(i,j+1)} + V_{(i,j-1)} - 2V_{(i,j)}}{R1(C1 + 4C2)} \tag{3.11}$$

where the first term $f(v(t))$ models the inverter nonlinearity characteristics. On careful observation, the third term in the equation which models the injection currents from the adjacent oscillators, can indeed be translated into a diffusion equation in the X and Y direction, representing the spatial contribution of the entire network of oscillators by applying the following,

$$V_{(i+1,j)} + V_{(i-1,j)} - 2V_{(i,j)} = \Delta x^2 \frac{\partial^2 V}{\partial x^2} \tag{3.12}$$

$$V_{(i,j+1)} + V_{(i,j-1)} - 2V_{(i,j)} = \Delta y^2 \frac{\partial^2 V}{\partial y^2} \tag{3.13}$$

In order to compute the perturbed steady state solution, the phase shift $\alpha(t)$ needs to be solved first. The solution of this quantity is given by the following differential equation,

$$\frac{d\alpha}{dt} = {V^T}_{(i,j)}(t + \alpha(t)).b(t) \tag{3.14}$$

where, ${V^T}_{(i,j)}$ represents the phase sensitivity of an oscillator node to external perturbations $b(t)$ and is referred to as the Perturbation Projection Vector (PPV). PPV defines the oscillator's phase sensitivity to a given external perturbation. There are thus, two main differential equations, (3.11) and (3.14) which need to be solved by numerical methods. These are solved on MATLAB by discretizing the partial differential equation (3.11) and computing $\alpha(t)$ over a number of iterations by applying the Neumann Boundary conditions.

$$\left(\frac{\partial u}{\partial n}\right)_{i=[1,m1],j=[1,m2]} = 0 \tag{3.15}$$

where, m1 and m2 denote the number of oscillators along X and Y direction. Further, the PPV component in the equation (3.14) is a periodic vector which is extracted using the Floquet Analysis. The PPV waveform for the ring oscillator described above, is shown below. In the following simulation, an oscillation cycle of 3 ns is considered and on observation, it is evident that PPV waveform repeats itself periodically.

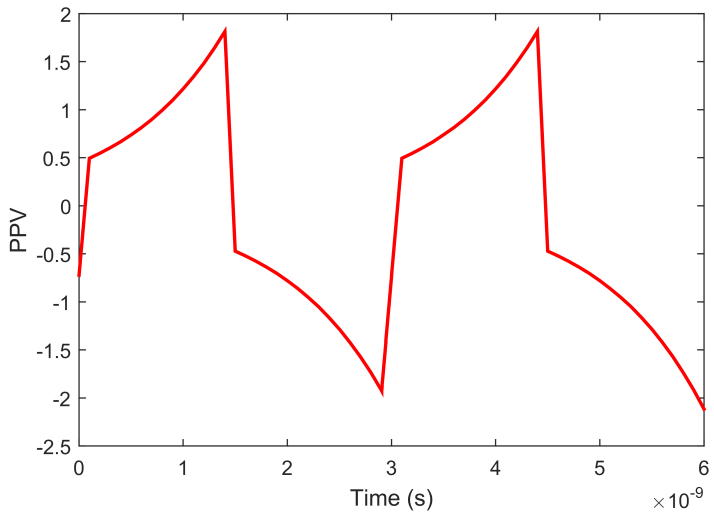


Figure 3.8: Perturbation Projection Vector of a 3 stage ring oscillator

3.2.1 Oscillator Network Simulation

In this section, the MATLAB simulations are discussed. A mesh of oscillators is considered for simulation, a part of the network is shown in the Figure 3.9 . Each node in the network represents the oscillator node and the coupling between them is a π type RC network described in the above sections. The RC parameters are chosen such that the oscillation period is 1 ns and that each of the nodes in the coupled oscillator network is 100 µm apart. This mutual spacing is considered as

a reasonable assumption for simulation purposes, given that the TDC is designed and laid out in a 65 nm technology.

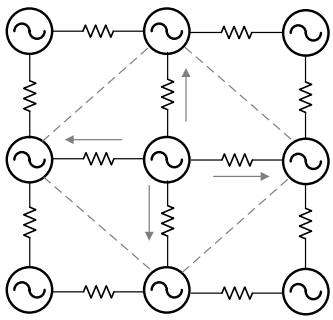


Figure 3.9: Mesh of oscillators

The injection locking phenomena due to the mutual coupling between oscillators will eventually bring all the oscillators in the mesh to converge to a constant phase shift after any phase misalignment in the network. It is important to study this, especially in the application point of view. The oscillators are a part of the TDCs and are used for the time-of-arrival measurement in case of an event. It is likely that the oscillators start with random phases initially and it is interesting to simulate the gradual phase alignment. In order to analyse this, a coupled network of 21x21 oscillators is solved for $V_{i,j}(t)$ and $\alpha(t)$, first with random initial phases between 0 and 2π. Each time step is equivalent to 50 ps, with every oscillation cycle 'T' corresponding to 20 time steps, thus accounting for the 1 ns oscillation cycle. The phase shift in units of radians are plotted over the number of time steps with random initial conditions in the Figures 3.10 and 3.11.

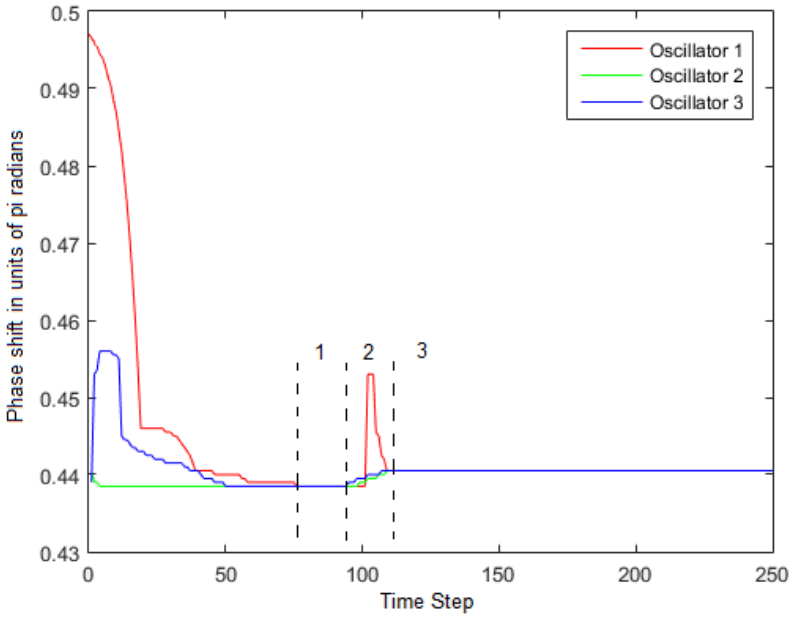


Figure 3.10: Phase shift in units of π radians- charge injection in two oscillators

Further, as one can observe, in the Figure 3.10, the phase starts with random values initially until it attains a constant phase in region 1 when the oscillators become phase locked for the first time. In the TDC, the oscillators are most likely to see a small charge injection whenever a sampling event occurs. This would directly translate into a minute phase shift at that oscillator node. For the same reason, a small charge δq on the oder of a hundred fC was injected at some of the oscillator nodes. In the Figure 3.10, equivalent charge is injected at two nodes(at oscillator 2-3) and phase shift of those along with an unperturbed oscillator (oscillator-1) is plotted. In the Figure 3.11, charge with different magnitudes is injected at 4 nodes in the centre of the 21x21 network and the phase shift of two of the perturbed oscillators are plotted. It can be seen in region 2 of both the figures that the perturbed oscillators become phase locked over time depending on the magnitude of the charge being injected. For instance, in the Figure 3.11, a relatively larger charge injected takes more number of timesteps (about 80 in Figure 3.11) to revert back to a synchronized condition from a perturbed state.

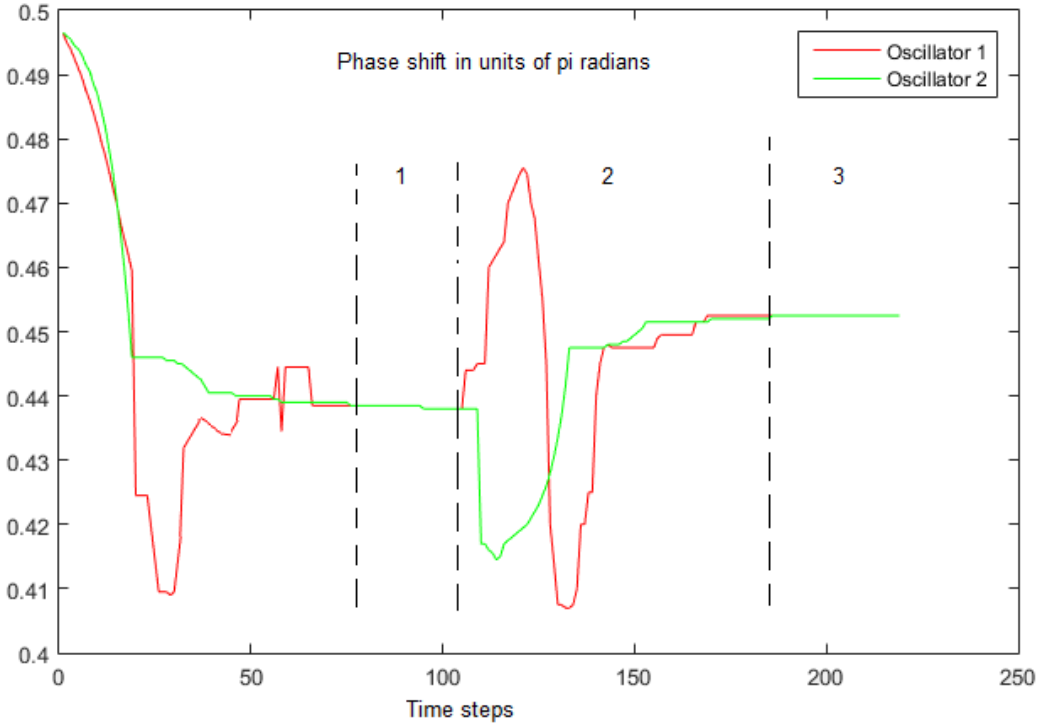
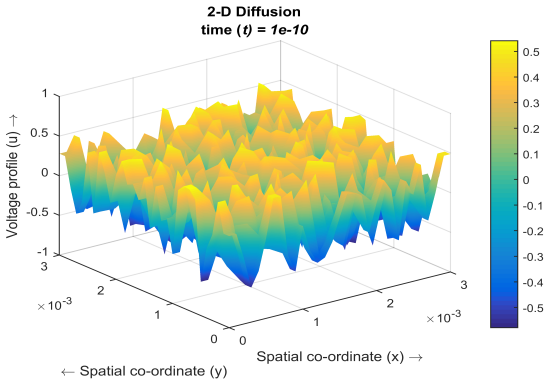


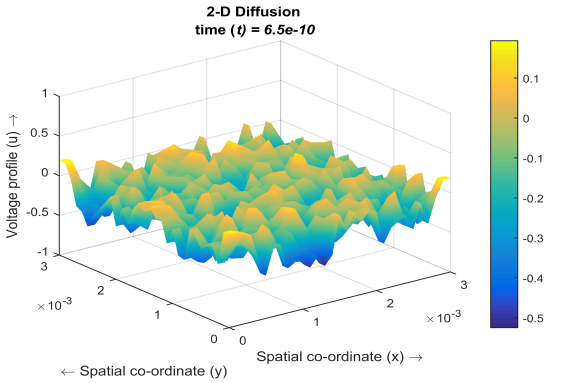
Figure 3.11: Phase shift in units of π radians- charge injection in four oscillators

3.2.1.1 Simulation with random and defined initial conditions

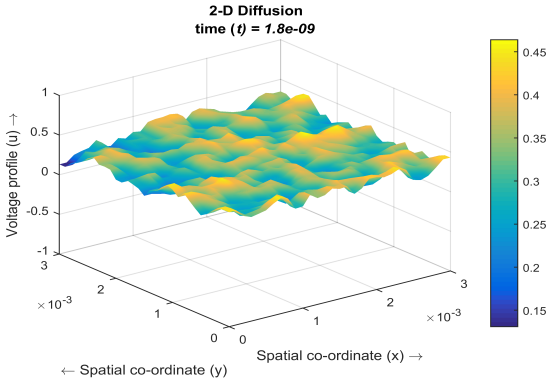
An oscillator network of 30X30 oscillators with an oscillation period T=1 ns and the coupling parameters R2=1 kΩ, C2=1 pF is simulated with random initial conditions. Each of the oscillator is spatially separated by 100 μm. Following is the surface plot of the voltage profile of the coupled oscillator nodes in the entire mesh and their evolution over time. As can be seen in the Figure 3.12, it takes about 4 clock cycles to attain synchronization. This time depends on the coupling impedance between the oscillators which basically determines the diffusion constant in the differential equation 3.11.



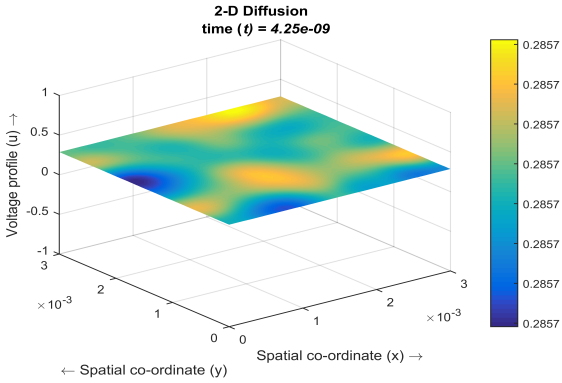
(a) Voltage profile at time t=0.1T



(b) Voltage profile at time t=0.65T



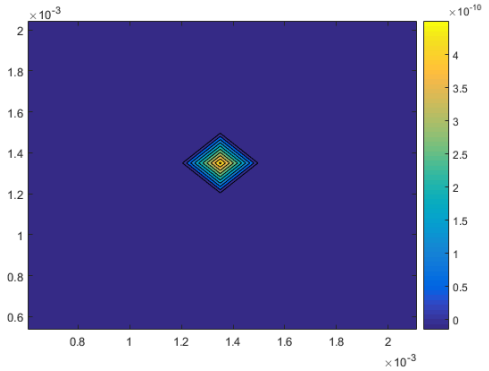
(c) Voltage profile at time t=1.8T



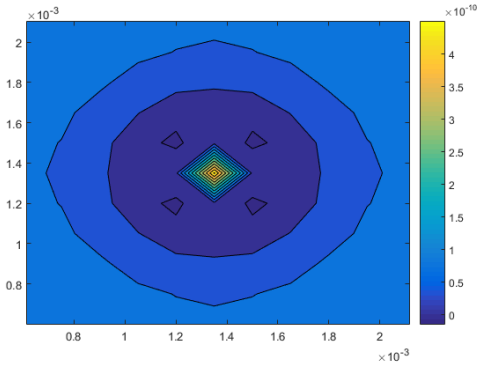
(d) Voltage profile at time t=4.25T

Figure 3.12: Voltage profile of 30X30 oscillator mesh

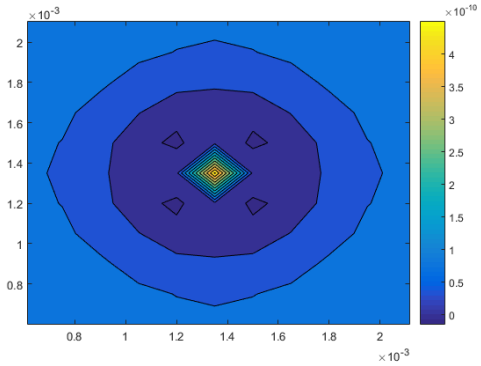
The phase synchronization is naturally also indicative in the phase shift simulations of the oscillators. A contour plot of the phase shift $\alpha(t)$ is shown for a mesh of 21X21 oscillators with defined initial conditions in the central region of the mesh in the Figure 3.13. It is indeed evident from the Figure 3.13 that the oscillators follow a pattern of self-organization within them over time, substantiating the fact that coupled oscillators, given random or defined initial conditions will eventually get locked to each other due to their mutual coupling. It can be observed that, the constant phase shift in all the oscillator converges towards each other at about 1.5 T, seen in the Figure 3.13d. As expected, the case with random initial conditions takes greater number of clock cycles to attain synchronization compared to defined initial conditions where the percentage of perturbation is minimal.



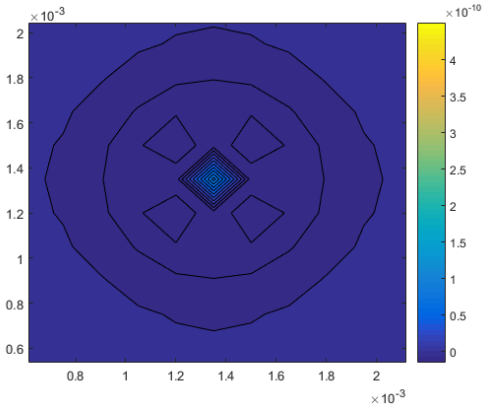
(a) Phase shift profile at time t=0



(b) Phase shift profile at time t=T



(c) Phase shift profile at time t=T



(d) Phase shift profile at time t=1.5T

Figure 3.13: Phase shift profile of 21X21 oscillator mesh with defined initial conditions

So far, in the above sections, natural coupling between oscillators was analysed to understand the locking behaviour among the oscillators. It can be summarized that the time it takes to attain phase synchronization depends on,

- Coupling between the oscillator nodes which in turn decides also the diffusion constant of the governing differential equation.
- The initial conditions for the phases (If it is completely out of phase, it would take more time to achieve phase lock).
- Number of oscillators in the network which are misaligned in phase, as lesser the number of oscillators misaligned, the less time it takes for the oscillators in the network to pull the perturbed oscillator to a phase lock with rest of the network. Moreover, number of stages in an oscillator also dictates this time.
- Finally, the coupling dynamics also depend on the architecture of the oscillator as the PPV function used for such an analysis is oscillator specific.

In the next chapter, the TDC architecture is completely described and the circuit level implementation based on the core concepts will be discussed.

Chapter 4

Design and Implementation of TDC

In the previous chapter, the specifications of the TDC were derived based on the application and the major concepts used in the TDC were discussed. In this chapter, the overall TDC architecture is first presented followed by the circuit level design and layout implementation of critical blocks. Finally, the chapter is concluded by highlighting the key features of this work.

4.1 TDC Architecture

The TDC used in this work employs a coarse-fine architecture, partly event-driven TOF measurement. The block diagram of the TDC with the internal blocks is shown in the Figure 4.1. It consists of a high frequency 10b - counter which is used to count integer number of clock cycles. The counter operates at an input frequency of 1 GHz, thus providing a range of 1.024 µs over 10 bits. These 10 bits make up the coarse code of the final TDC code. Along with the counter, there is a voltage controlled ring oscillator (VCO) used to determine the fine code. The control voltage for the VCO is provided by a PLL which uses a replica of the VCO used in the TDC. The VCO, thus operates in closed loop and a 50 MHz reference frequency which is used in the PLL also serves as the sub-harmonic injection signal for the VCO in the TDC; the details of this will be revisited subsequently. The VCO is a 16 phase pseudo-differential design which starts oscillating on power-up owing to the Barkhausen criterion. The high frequency up counter which is connected to one of the phases of the oscillator, keeps incrementing every oscillation cycle. Whenever a photon generates a SPAD response, the corresponding event is recorded as a digital stop pulse, also indicated as "TOF" in the Figure 4.1. This TOF pulse acts as the clock signal to the flip-flops which are used to sample the states of the oscillator and the counter whenever there is an event. The 16 sampled states of the VCO form the fine part of the TDC code. This code is pseudo-thermometer in nature and thus, is decoded to binary before combining with the 10b coarse code from the counter. The combined 14b code is then used to generate the final TDC code for TOF estimation.
The overall working of the TDC, with the VCO and counter can be further understood with the help of a simplified timing diagram shown in the Figure 4.2.

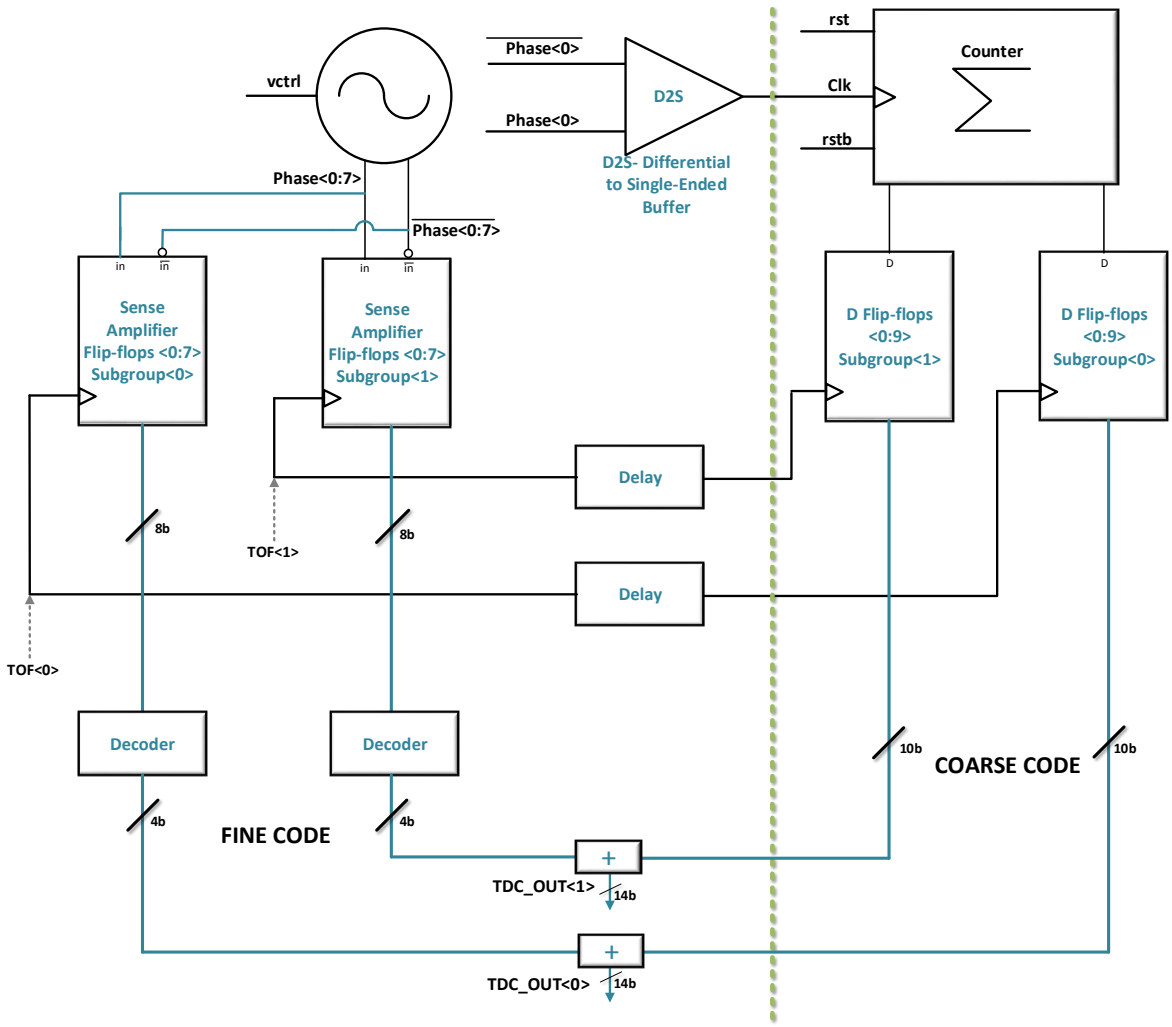


Figure 4.1: Building Blocks of TDC

4.1.1 Ring Oscillator Design

The ring oscillator is based on a voltage controlled pseudo-differential architecture. Unlike a single ended and a fully differential design, a pseudo-differential cell extends from the concept of having differential signals in a ring, except that the switching threshold of the pseudo-differential cell is defined directly with respect to the common ground due to the absence of a tail current source as in a fully-differential cell. The Figure 4.3 shows a true differential and a pseudo-differential unit cell to illustrate the difference. A pseudo-differential cell provides larger swing compared to a fully differential and the absence of the tail current source results in a larger common mode gain. The lower CMRR is still a problem when compared with a fully differential stage which could result in higher jitter. However, the concepts of coupling and injection locking between oscillators elucidated in the previous chapter contribute remarkably towards improvement of phase noise performance of the VCO. Another advantage when compared to a single ended unit cell is the possibility to use even number of stages in a differential configuration to sustain oscillation.

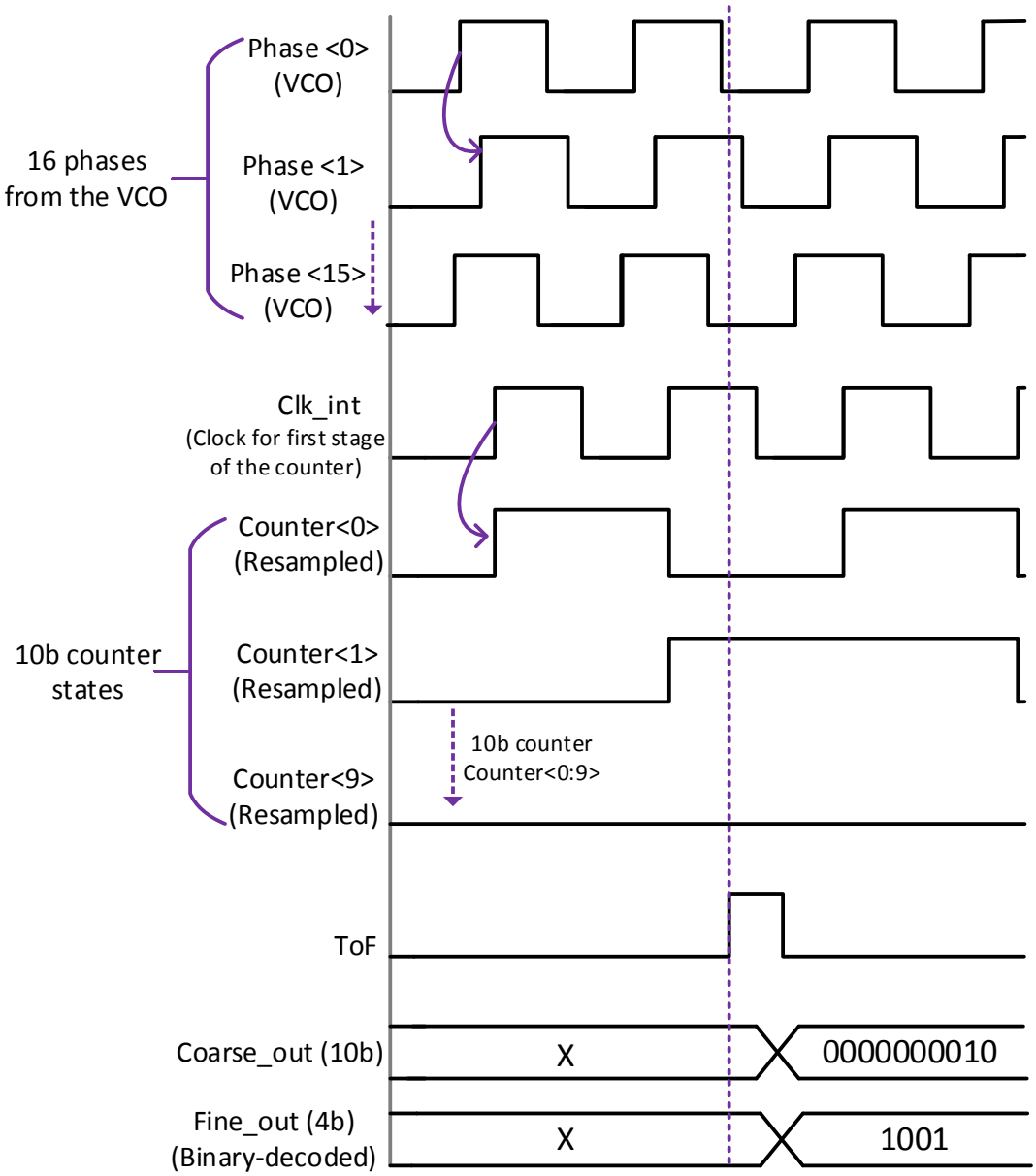
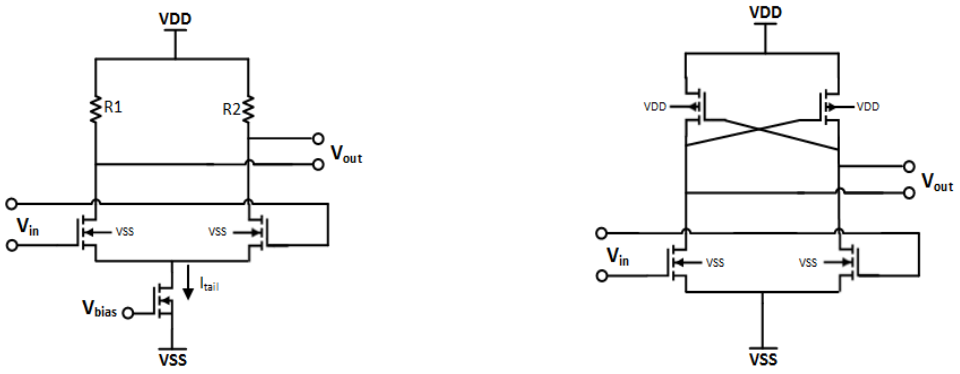


Figure 4.2: Simplified timing diagram



(a) Differential unit cell **(b)** Pseudo-differential unit cell

Figure 4.3: Unit cells for differential ring oscillator

The VCO in this TDC consists of 8 pseudo-differential units as shown in the Figure 4.4. Thus, there are 16 differential phases which will form a 16- bit pseudo-thermometer code when sampled. The oscillation frequency of the VCO is determined by a control voltage generated from the DAC which is fed to the gate of a PMOS transistor used as the current source. This can be seen in the transistor level circuit diagram in the Figure 4.6. The presence of a current source, thus helps save power with the VCO operating at a lower frequency when the resolution demand is not high.

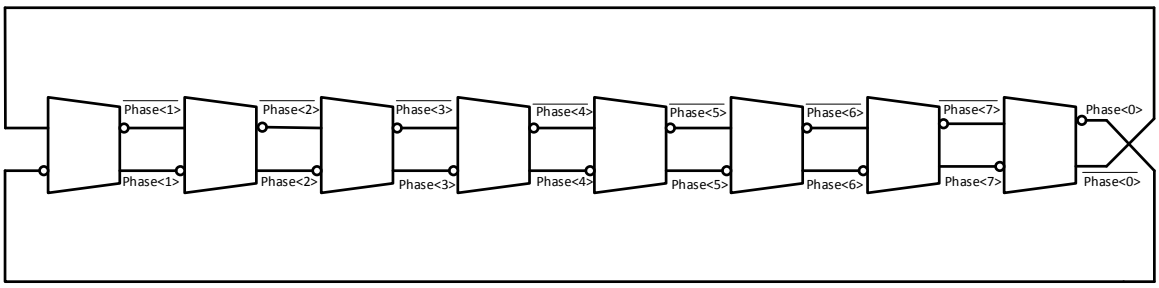


Figure 4.4: Pseudo-differential VCO

Because of the even number of stages, the differential signals from the final stage are inverted when they complete the loop. This is necessary in order to sustain oscillation in the loop. Each pseudo-differential unit comprises of two inverters coupled to each other through an inverter based latch to ensure positive feedback at each stage which sustains oscillation throughout. The unit cell is shown below in Figure 4.5.

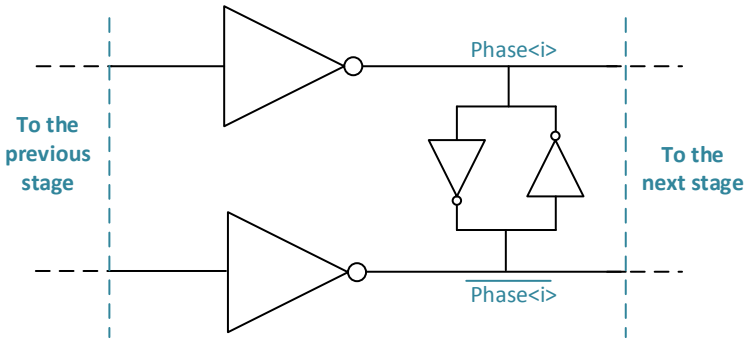


Figure 4.5: Pseudo-differential delay stage

The oscillation frequency required is 1 GHz. Thus, the pseudo-differential stage is designed such that the oscillation cycle or the time period of oscillation obeys the following formula:

$$T = 2.N.t_{delay} \tag{4.1}$$

Or,

$$f_{osc} = \frac{1}{2.N.t_{delay}} \tag{4.2}$$

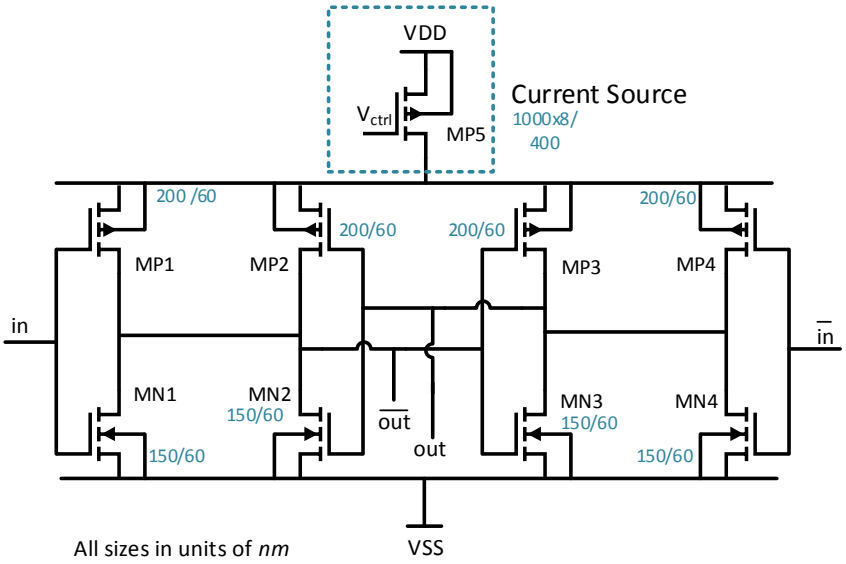
where T is the time period of the oscillator, t_{delay} is the propagation delay across a unit pseudo-differential cell and N is the number of stages. For an oscillation frequency of about 1 GHz and the number of stages equal to 8, a typical t_{delay} of 62.5 ps (average) per stage is obtained in this technology.

Transistor Level Circuit- VCO

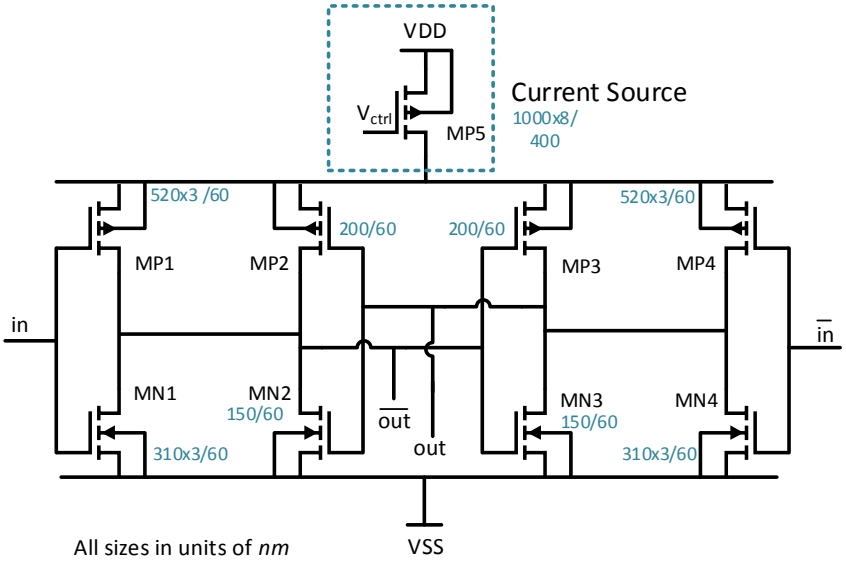
Ideally, in order to ensure equal t_{delay} and good linearity, every delay stage of the ring oscillator is sized equal assuming equal load conditions. However, in reality, due to unequal impedances at the oscillator nodes and additionally, also due to the coupling and injection locking being introduced, it is necessary to account for the changing conditions at the oscillator phases. In this design, each of the oscillators in the array is coupled to its neighbour through Phase<4>. Additionally, sub-harmonic reference signal is also injected at this node. This adds additional capacitances due to the extra wire parasitics at this node. From post-layout simulations and the parasitics extracted from Cadence PEX tool, it was observed that capacitance on the node Phase<4>is approximately four times higher than any other phase in the ring. In order to accommodate a higher load, the corresponding pseudo-differential stages were sized accordingly as shown in the Figure 4.6. The width (W) over length (L) is indicated for all the transistors in the figure. The current source is designed large in order to provide a wide tuning range of oscillation frequencies for changing control voltage. A longer channel length (400 nm in this design) is used which provides a larger intrinsic gain g_m/g_{ds}. Section 5.2.1 in Chapter 5 describes the results obtained from this VCO.

4.1.2 Sense-Amplifier Flip-flop (SAFF)

As seen in the Figure 4.1, sense-amplifier flip-flops are used in order to sense the true and complementary signals at the phases of the VCO. Setup time, hold time and clock-to-output propagation delay are important parameters in the design of latches and flip-flops[15].



(a) Delay stage for other phases



(b) Delay stage- Phase<4>

Figure 4.6: Transistor level schematic- Delay stage

SAFF based designs have shown lower delays from the time of data arrival to a transition at the output. Moreover, due to their symmetrical structure, it is possible to have similar timing resolution for the rising and falling edges of the data input and the sampled output. For the above reasons, SAFFs are designed in order to sample the 16 phases of the VCO. The transistors are sized to ensure as much symmetry as possible for the true and complementary signals.

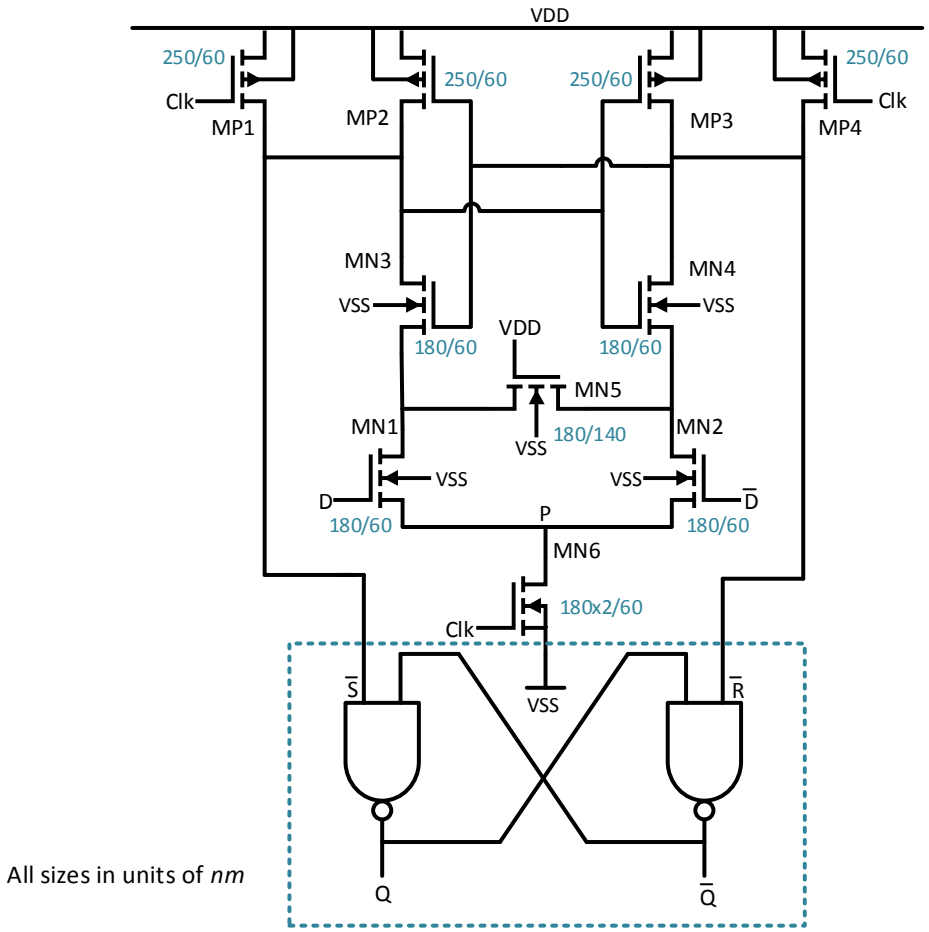


Figure 4.7: Sense amplifier flip-flop

The circuit diagram of the SAFF along with the transistor sizes is shown above in the Figure 4.7. The SAFF consists of a sense amplifier as its first stage and an S-R latch in the other stage (outlined by a blue square in the Figure 4.7). The sense-amplifier senses the differential inputs fed into the terminals D and $\bar{D}$, from the phases of the oscillator and makes transitions at its output on every leading edge of the clock signal. The clock signal (TOF) in our case is the pulse indicating the time of arrival of a photon at the SPAD which is further sent as a digital pulse to the TDC. The data at the output of the sense-amplifier does not change until the next rising edge of the clock. Similarly, the S-R latch holds the state of the sense-amplifier until the next rising edge of the clock.
When the clock signal is low, the nodes which are denoted as $\bar{S}$ and $\bar{R}$ are precharged to a logic high through transistors MP_1 and MP_4. This high state keeps the transistors MN_3 and MN_4 and thus, the common node P charged to V_{DD}-V_{th}. Hence, when the clock signal is low, all capacitances in the sense-amplifier are precharged. When the clock signal switches to high, depending on the data at the input, $\bar{S}$ and $\bar{R}$ attain different states, correspondingly making transitions at the output of the SAFF, Q and $\bar{Q}$. Additionally, the purpose of the transistor MN5 is to provide a path to ground following any data changes, especially to avoid leakage currents. The truth table in the Table 4.1 summarizes the operation of the SAFF. It is difficult to achieve almost equal delays for

Q and $\bar{Q}$ because in a structure shown in the Figure 4.7, the rising edge always occurs first (after one gate delay, when $\bar{S}$ goes low and Q goes high, in turn forcing $\bar{Q}$ to low) and the falling edge roughly after two gate delays. Thus, the sizing of the transistors is done with a goal of keeping this difference minimal. This will be revisited in the Results chapter in section 5.2.2.

Table 4.1: Truth Table- SAFF

Clk	**D**	**$\bar{\mathbf{D}}$**	**$\bar{\mathbf{S}}$**	**$\bar{\mathbf{R}}$**	**Q**
0	0/1	0/1	1	1	Previous state
1	0	1	1	0	0
1	1	0	0	1	1

4.1.3 Counter

A 10-bit asynchronous counter capable of operating at 1 GHz was designed to generate the coarse code of the TDC and facilitating a dynamic range of about 1 µs. The counter thus, keeps track of every oscillation cycle and increments on the rising edge of the oscillating pulse. The counter circuit consists of 10 D flip-flops accounting for 10 bits of the coarse code. $Phase<0>$ and $\overline{Phase<0>}$ of the VCO are used to generate the clock signal to the first stage of the asynchronous counter which triggers the counting process as shown in the Figure 4.1. It is important to isolate the differential signals from the VCO while feeding it to the clock input of the first stage of the counter. Thus, a differential-to-single (D2S) ended buffer is used in between them. The purpose of the D2S is to provide equal impedances to the true and complementary signals, $Phase<0>$ and $\overline{Phase<0>}$. Further, the complementary output $\bar{Q}$ of every subsequent stage in the counter acts as clock signal for the next stage to complete the counting circuit. The overall block diagram of the counter along with the supporting cells are shown in the Figure 4.9.

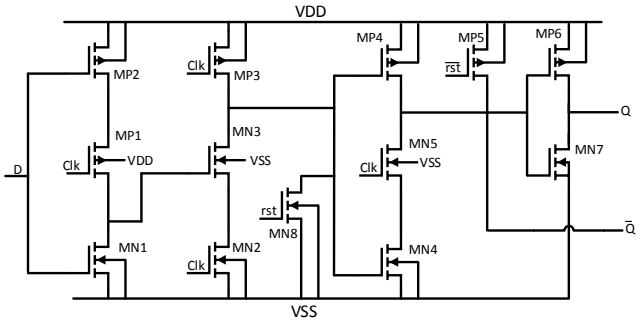


Figure 4.8: Counter Cell- TSPC D flip-flop

The counter is designed using true single phase clock (TSPC), positive edge triggered D flip-flops for the advantages of low clock load capacitance, fewer transistors and thus, smaller area. The circuit diagram of the TSPC D flip-flop used in this design is shown above in the Figure 4.8[1].

[1]The transistor level schematic along with their sizes for the counter block (counter unit stage and resamplers) is drawn in the Appendix B

4.1.3.1 Resampler

The 10-bit states of the counter are resampled synchronous to a clock signal. The resamplers (see Figure 4.9) are designed using D flip-flops similar to the unit cells of the asynchronous counter. Output Q of every stage at the asynchronous counter has a D flip-flop to sample the state at the rising edge of a clock signal. The clock signal to the first resampler (B<0> in Figure 4.9) is the same pulse which is fed into the first stage of the asynchronous counter. Every other clock input required to trigger the subsequent resamplers is fed via buffers to maintain the signal strength until it reaches the last resampler which samples the last bit of the asynchronous counter. The clock signals for the resamplers are denoted as $Clk\_int < 0:9 >$ in the Figure 4.9.

4.1.3.2 Sampler

In order to synchronize the TDC codes with the SPAD response whenever there is an event, another set of D flip-flops are used, referred as samplers in this design. The TOF pulse acts as the clock to these D flip-flops. The outputs from the Q terminal of the resamplers, also referred as $counter\_out < 0:9 >$ in the Figure 4.9, are connected to the inputs of the samplers. Thus, on the rising edge of the TOF pulse, the counter states are accordingly sampled to finally generate the coarse code of the final TDC output. As shown in Figure 3.3 of Section 3.1.2, there are two subgroups which share a TDC. Thus, there are two sets of samplers, as can be seen in the Figure 4.9, to record the time of arrival from two subgroups which share a TDC. The TOF pulse to every sampler is fed via buffers similar to the resamplers. It is important to match the buffer delay between the TOF signals and that of the clock signals for the resamplers to generate correct code. Thus, equivalent buffers are used for both the signal paths. In the Figure 4.9, the TOF signals for the two subgroups are denoted as tof_0 and tof_1.

4.1.4 Testing Circuit- TDC Array

In order to test the concept of coupling and injection locking, a TDC array of 8x8 TDCs was laid out, with a coupling element between the $Phase < 4 >$ and $\overline{Phase < 4 >}$ signals of every VCO in the TDC array.

Coupling of Oscillators The coupling element consists of transmission gates along the differential signal path of the $Phase < 4 >$ signals. The circuit diagram of the coupling element is shown below in Figure 4.10. As one can see, the coupling between oscillators can be enabled by sending signals $en\_coupling$ and $\overline{en\_coupling}$ to the transistors MN1-MN4 and MP1-MP4 respectively. The enable signals thus, provide a way to analyse the oscillators in the absence of coupling, if need be. This is specially useful, to characterize the phase noise performance of the VCO and study the dependence of coupling strength between oscillators as described in the previous chapter. Additionally, the sub-harmonic reference signal is injected through transistors MN5 and MN6. Thus, with this coupling element, it is possible to retain the coupling with or without injection locking with the sub-harmonic reference signal and perform characterization independently, if necessary.

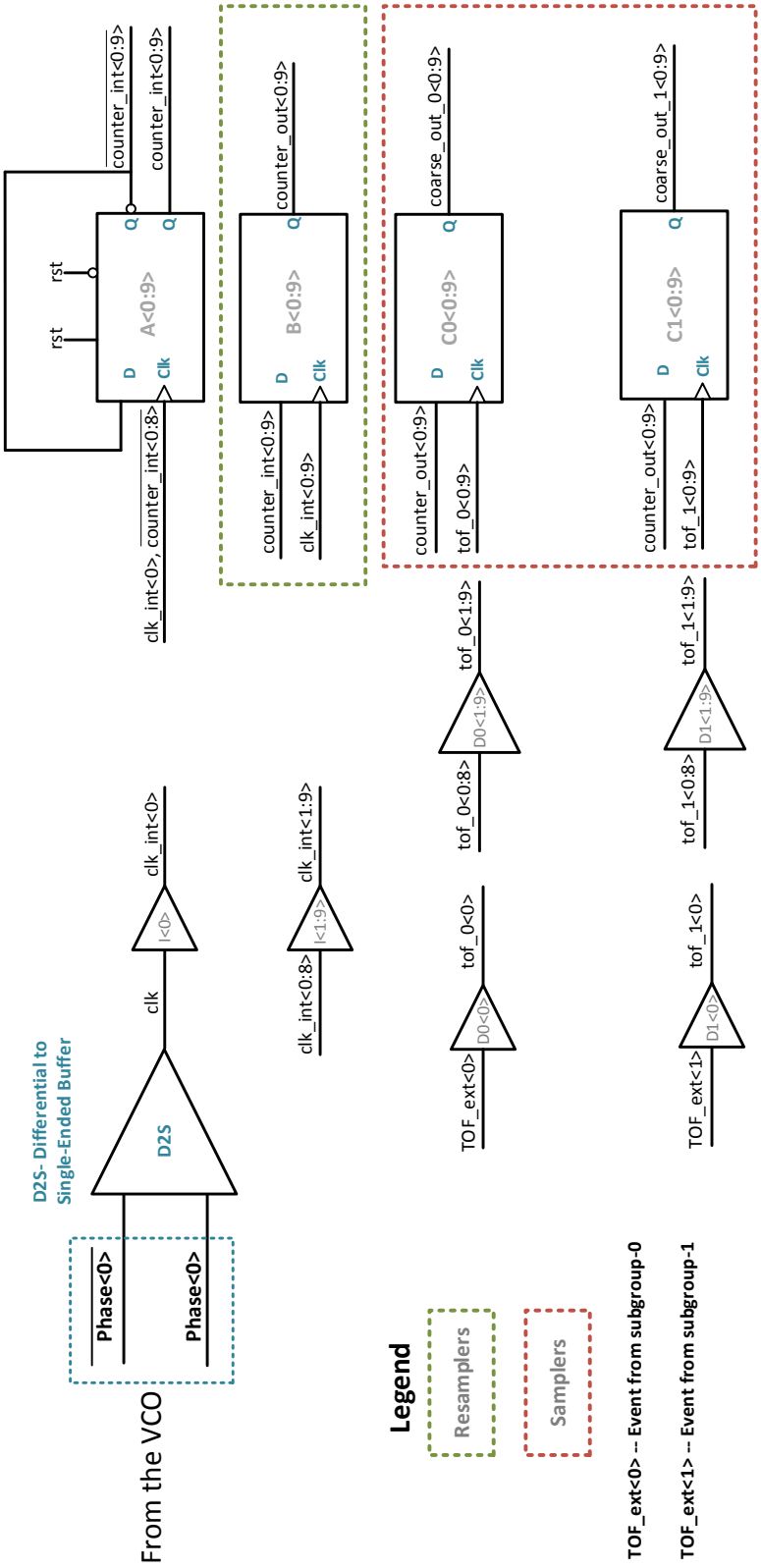


Figure 4.9: Block-level Schematic- Counter

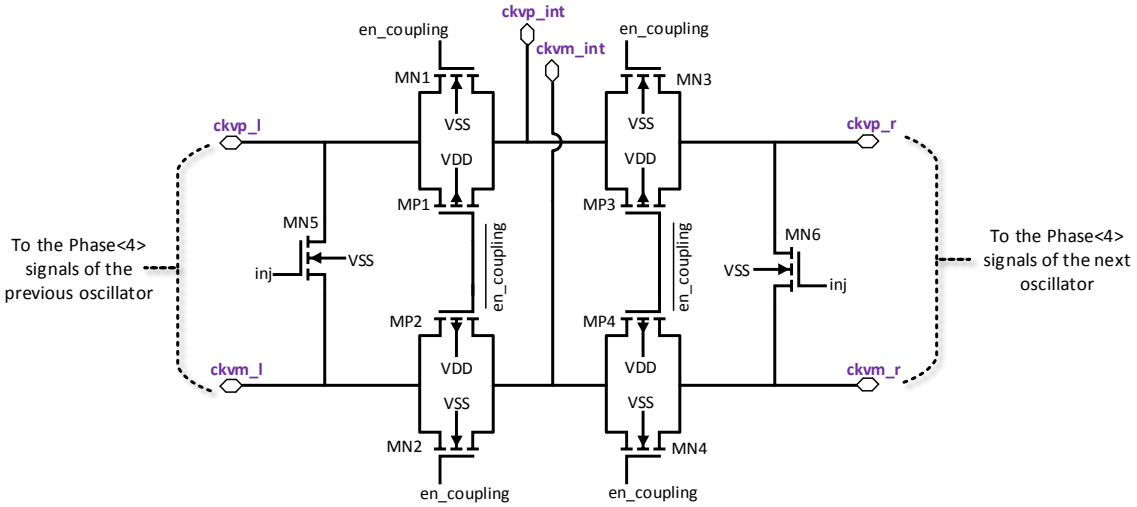


Figure 4.10: Coupling element

A buffered version of the sub-harmonic reference signal shorts to the $Phase < 4 >$ and $\overline{Phase < 4 >}$ signals through the terminal ckvp_l-ckvm_l and ckvp_r-ckvm_r during the windows when VCO oscillating edges coincide with that of the reference signal at the rate of the injection frequency. This results in pulling of the VCO edge towards realignment and thereby, suppressing the accumulated jitter from a previous time. The entire TDC array, with the coupling elements are shown in the Layout Gallery to follow.

4.1.5 Key points of this design

- *Operating the TDC*: The TOF system used in this work is partly event-driven, meaning that the VCOs keep running all the time and the TDC generates a code corresponding to a SPAD response whenever there is an event.
  Thus, when the TDC is operated at its full resolution derived from an oscillation frequency of 1 GHz, this results in a power consumption at a higher end. However, the control voltage gives the freedom to operate the VCO at a lower frequency when the requirement on the resolution is not stringent, thereby reducing the power consumption in this case.
- An approach of keeping the VCOs operating throughout, ensures continuous phase synchronization among the coupled oscillators and thus, efficient injection locking from the reference signal. This is substantial for a superior phase noise performance.
- Much focus has thus been rendered towards providing on-chip filtering and utilizing most of the area apart from the subgroups and the TDC for that purpose.

4.1.6 Layout Gallery- TDC building blocks

In this section, layouts of the critical building blocks of the TDC are discussed. The layouts of the individual blocks are designed according to the following floor plan.

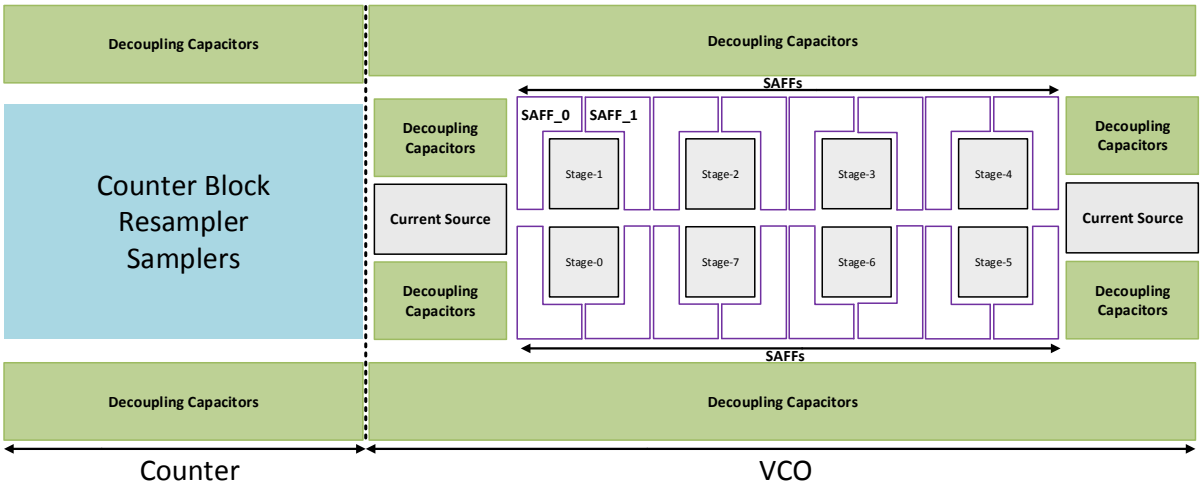


Figure 4.11: TDC floor plan

VCO

VCO is an integral block of the TDC given that the linearity is an important performance parameter. Hence, the VCO block has to be laid out with utmost attention. The 8 pseudo-differential stages are arranged in a ring as can be seen below. As pointed out in the previous sections, the additional capacitance in the Phase<4>arises because of,

- The longer connection from stage 4 to stage 5 as can be seen in Figure 4.12.
- Due to extra capacitances arising from the coupling connections to the neighbouring VCOs through Phase<4>.

For the same reason, stage 4 is sized larger with respect to the other stages.

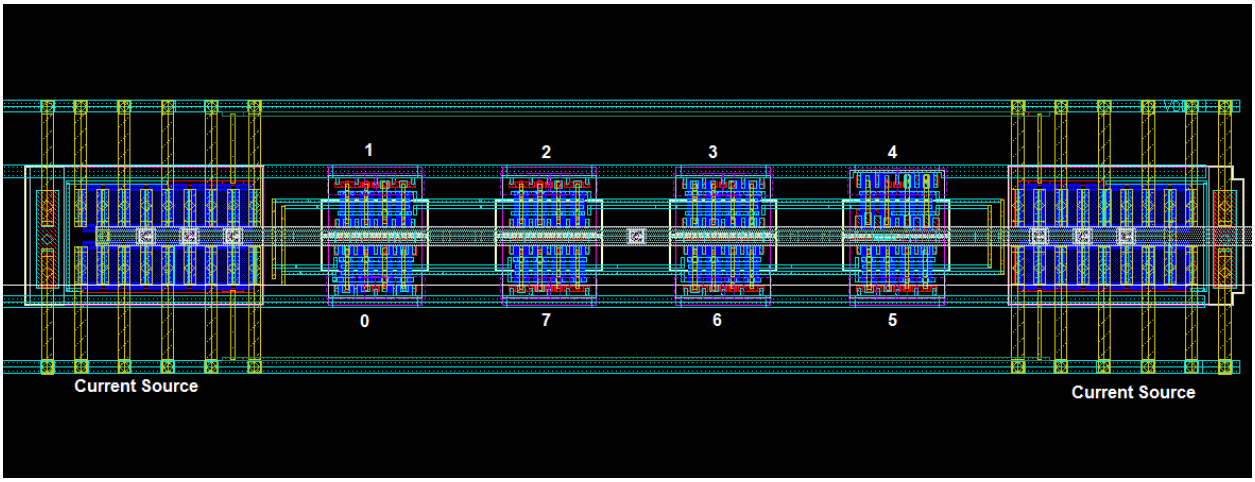


Figure 4.12: Layout- VCO

Sense amplifier flip-flops (SAFFs)- The SAFFs are laid in a way that the VCO phases are sampled with minimal delay due to a smaller interconnection between the VCO output terminals and the inputs of the SAFF. Complying with overall TDC structure as shown in Figure 4.11, the layout of the SAFF neatly fits in the specified floor plan.

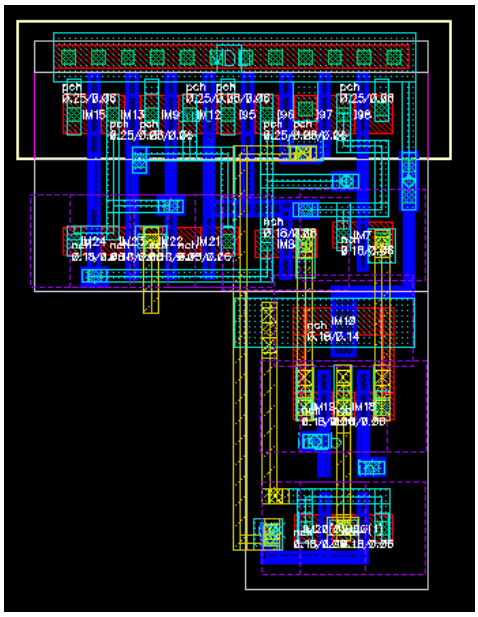


Figure 4.13: Layout- SAFF

Complete TDC

The complete TDC along with counter, VCO and decoupling capacitors is shown below in Figure 4.14. The signal path of the clocks for the samplers and the resamplers were laid as identical as possible in order to match the delays between them to generate correct code for measurement (Section 5.2.4 in Chapter 5 discusses the matching obtained after post layout simulation). The total area of the TDC designed is 144 µm x 11 µm.

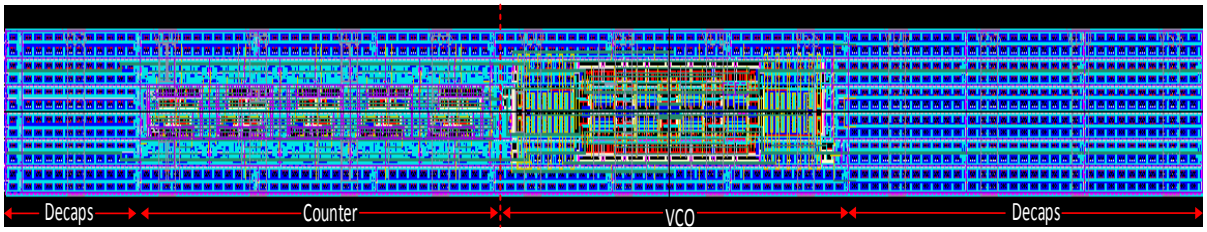


Figure 4.14: Layout- TDC

Layout of the TDC array consisting of 8x8 coupled TDCs is shown below. The array consists of the 64 TDCs mutually coupled through the coupling element described before. The size of the array is $\approx 1100\mu m$ x $1100\mu m$. This array, when fabricated will help in verifying the coupling concepts and provide a means to characterize the VCOs for their phase noise performances.

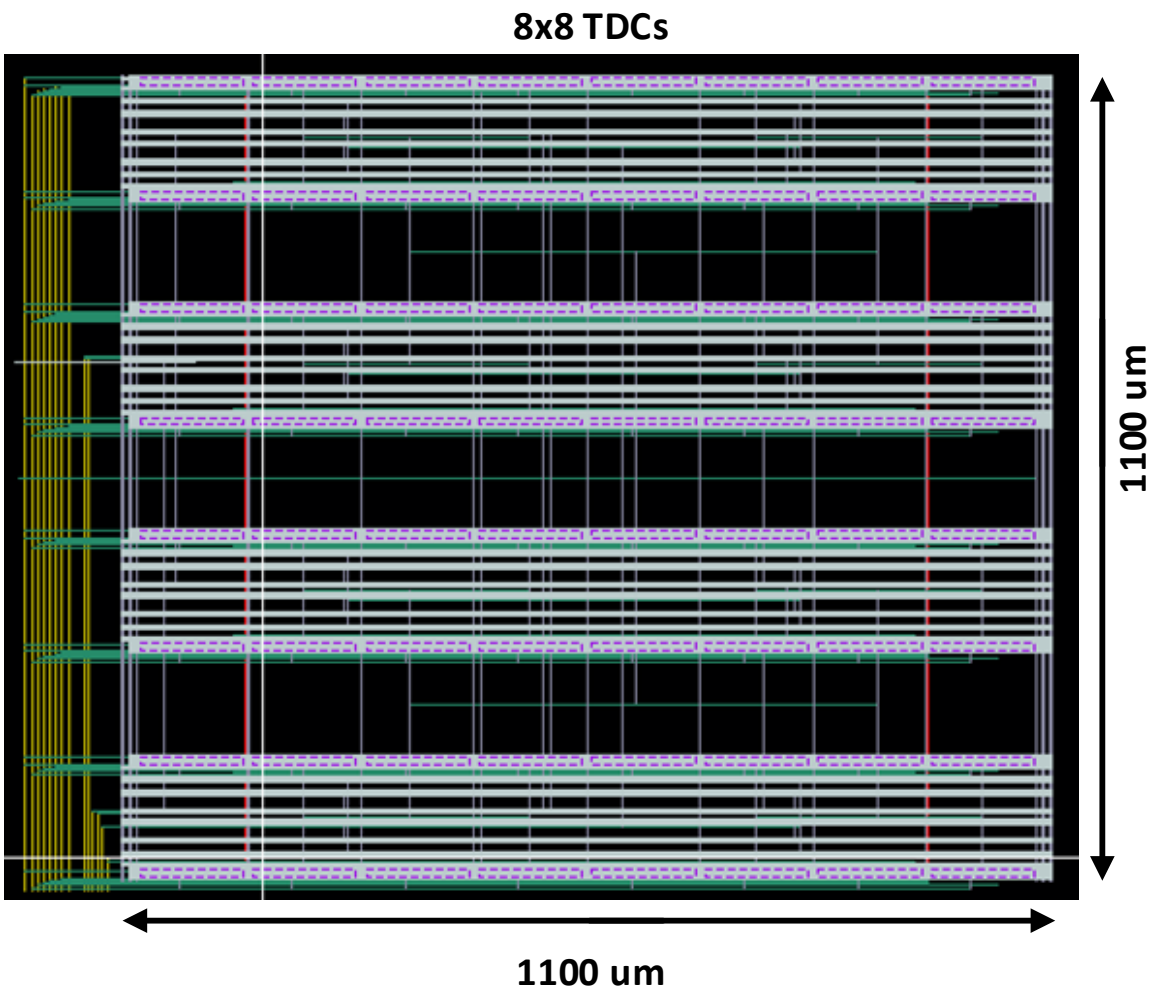


Figure 4.15: Layout- TDC array

4.1.7 Summary

This chapter explained the circuit level implementation of the TDC based on the concepts built in Chapter 3. Several factors which played critical role during the design phase were pointed out. Next chapter describes the measurement results for the GaN readout circuit discussed in Chapter 2 followed by the post-layout simulation results for the TDC.

Chapter 5

Results

The front-end circuit was fabricated and tested in 0.35 µm CMOS technology. The chip was independently tested at TU Delft to confirm its performance in terms of the functionality. The measurements on the readout IC with the detectors are currently being carried out at JPL to complete the characterization of the chip along with the detectors. This chapter presents the simulation and measurement results obtained from the preliminary testing performed. Further, the post layout simulation results of the TDC designed in 65 nm CMOS technology are presented.

5.1 GaN Readout Circuit

5.1.1 Simulation Results

5.1.1.1 DC Analysis

The results from the DC analysis of the circuit are shown in the Figure 5.1. The voltages are depicted as per the values obtained from Cadence simulation. All the transistors are biased to operate in the saturation region except the high voltage NMOS (HV NMOS in the Figure 5.1) which operates in the triode region for the reasons discussed in Chapter 2. The reset control, Rst<3> is used to set the transistors at the appropriate operating points required for the integration process to follow. The power consumption in the reset mode is ≈0.5 mW.
Further, as can be seen in the figure, having the the gate voltage for the high voltage NMOS_HV biased at 4.5 V and the input node of the amplifier V_b at 2.394 V keeps the HV NMOS in the ohmic regime, given that the threshold voltage of the HV NMOS used in this design is approximately 1.5 V.

5.1.1.2 Transient Simulations

The transient working of the CTIA starts with the reset switch (Rst<3>) initially closed and released at t=0. As soon as the switch is opened, the incoming photodiode current starts to integrate on the feedback capacitance and the voltage at the node input node V_b rises, causing the

output voltage V_{out1} to fall. The rise in the input voltage is due to the finite open loop gain (A) of the CTIA, such that $\Delta V_b = -\Delta V_{out1}/A$ and $\Delta V_{out1} = -Q/C_{fb}$, where Q is the integrated charge. Additionally, when V_{out1} drops to 0, the input PMOS (MP1 in Figure 5.1) shuts off and at this point, the feedback capacitor needs to reset in order to begin another integration. The working of the CTIA can be seen in the transient simulation plot in the Figure 5.2. The source follower outputs V_{out1} and V_{out2} are plotted for an input current of 1 nA.

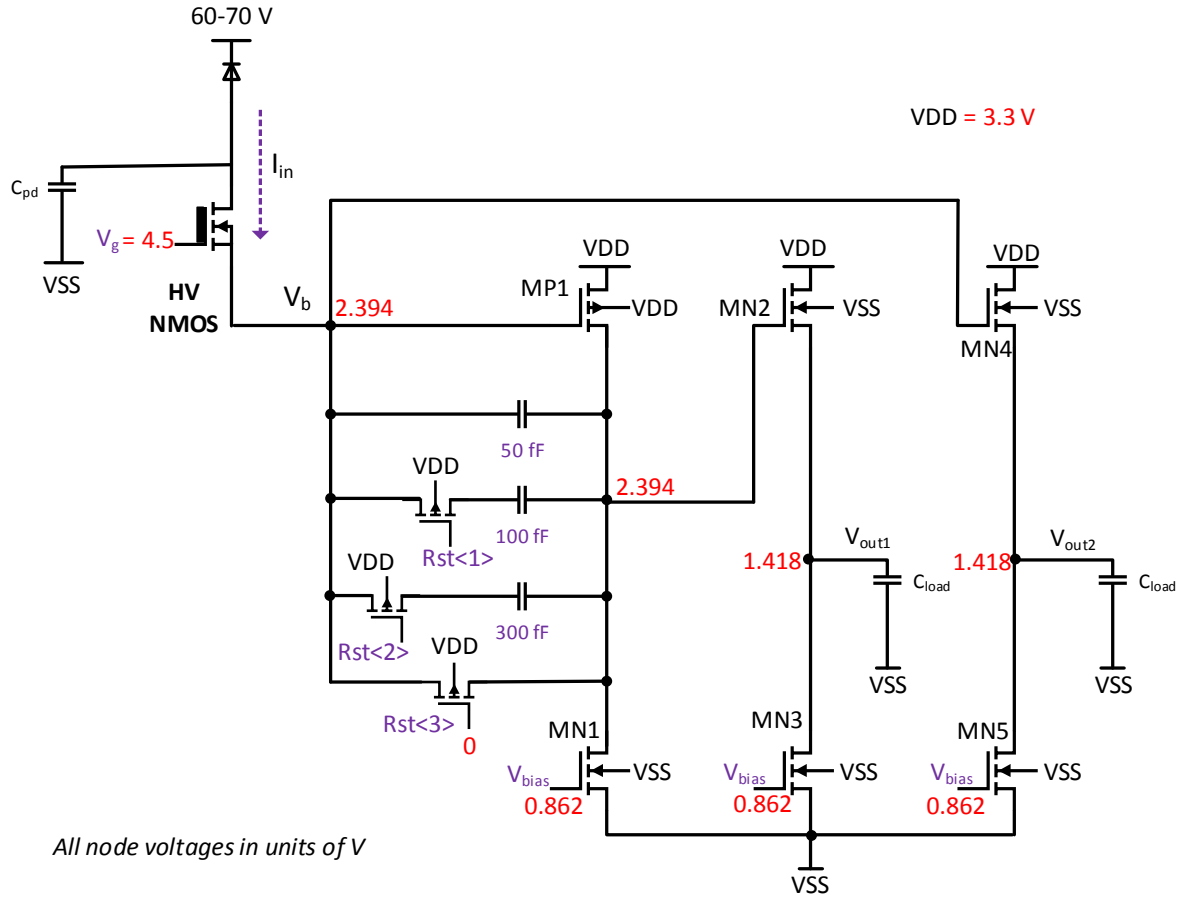


Figure 5.1: DC Analysis showing the bias voltages

The transient simulation in Cadence environment begins by setting an initial convergence aid to define the dc operating point for the transistors in the CTIA. This is done by assigning Rst<3> to 0 V. Thus, at t=0, the operating points of the CTIA transistors are set such that when Rst<3> is pulled to VDD, the integration instantaneously starts on the feedback capacitance. As can be seen in Figure 5.2, the initial voltage is $\approx$ 1.4 V for V_{out1} (Source Follower Output in Figure 5.2) and V_{out2} (Input Node V_b in Figure 5.2). The rising trend at the input node along with the negative ramp at the output based on the input current, confirm the required functionality of the CTIA.

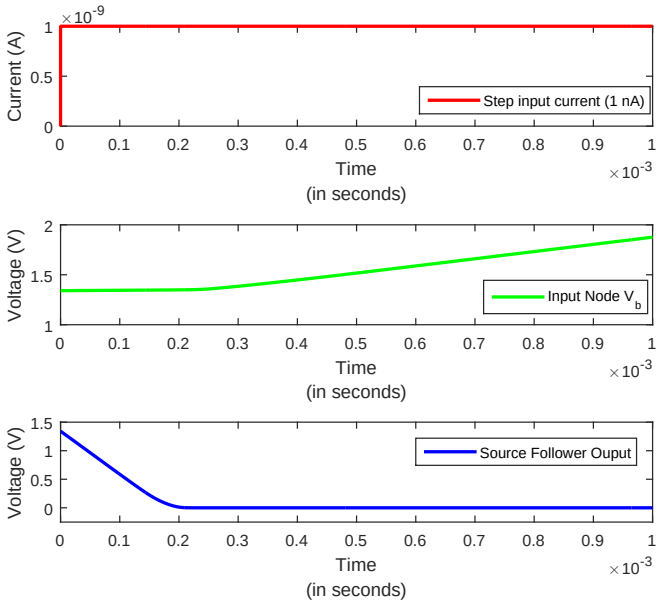


Figure 5.2: Transient analysis of the CTIA

5.1.2 Measurement Result- GaN ROIC

The fabricated chip was tested for primary checks in order to validate the functionality of circuit as obtained from the transient simulations performed on Cadence. The photomicrograph of a unit cell of the CTIA array is shown below in Figure 5.3

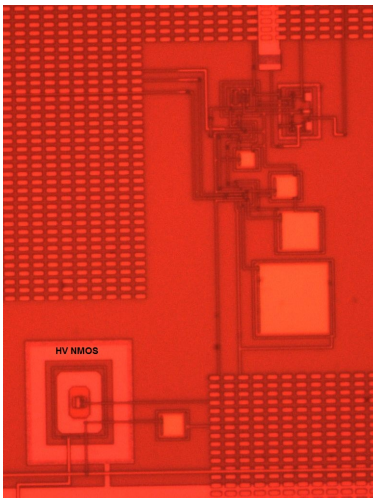


Figure 5.3: Photomicrograph- Unit cell CTIA

As described in Section 5.1.1.2, the overall CTIA functionality can be verified from the measurement results shown in Figures 5.4-5.8. A periodic signal is provided at the Rst<3> of the circuit in Figure 5.1 to control the process of integration.

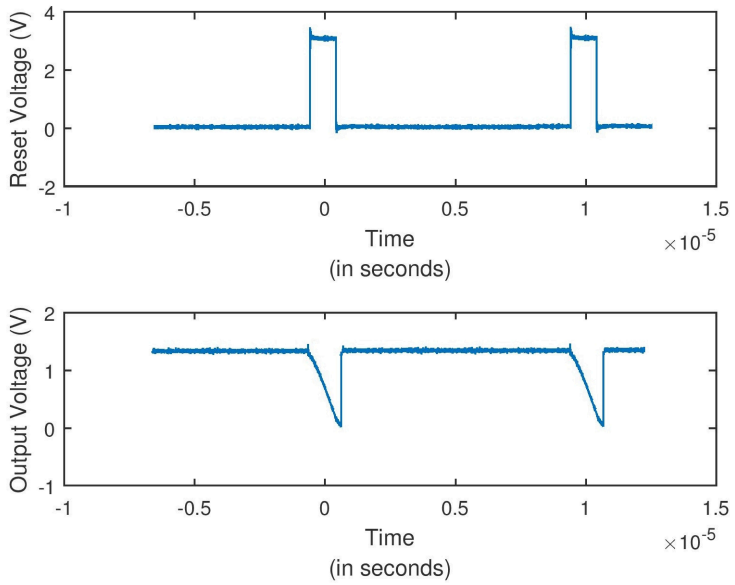


Figure 5.4: Control of bias, Reset mechanism, Integration

As can be seen in Figure 5.4, the turning-on of the reset switch, sets the operating points of all the transistors (initial voltage at the output ≈1.4 V, as observed during simulation). Pulling Rst<3> node to VDD, thus releases the reset switch to begin the integration on the feedback capacitance and causes the output voltage to ramp down as shown in the Figure 5.4. Additionally, amplification was checked with different input currents and feedback capacitances to confirm the achieved gain from the ROIC. A voltage source in series with a resistance on the order of $G\Omega$ was used at the input of the CTIA to emulate the low amplitude GaN APD current. A 1 pF capacitor was used at the input to emulate the GaN APD capacitance. The transient measurement result along with the post layout simulation for a given input are plotted for comparison in the Figure 5.5 and 5.6.

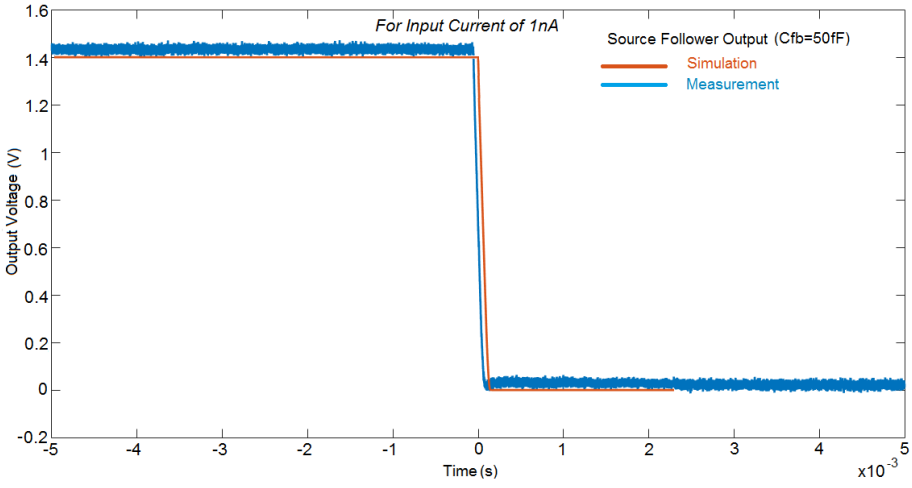


Figure 5.5: Feedback Capacitor = 50 fF, Input current= 1 nA

As can be seen, Figures 5.5 and 5.6 represent the upper and lower limits on the achievable gain from this design. For the lowest feedback capacitance used in Figure 5.5, C_{fb}=50 fF and an input current of 1 nA, the integration time obtained is the fastest as expected, on the order of a few hundred microseconds for an input capacitance of about 1-2 pF. This figure aligns well with the post layout simulation result obtained for the circuit with equivalent parameters. Similarly, Figure 5.6 shows the output plot for the highest feedback capacitance (450 fF) possible in this design. The frequency of the signals from the already fabricated GaN devices have a bandwidth in the range of several hundred kHz to a few MHz in certain devices. Since most of the GaN devices are not operating at very high speed, the current ROIC is considered sufficient to evaluate their performance. However, there is significant room for improvement in future designs.

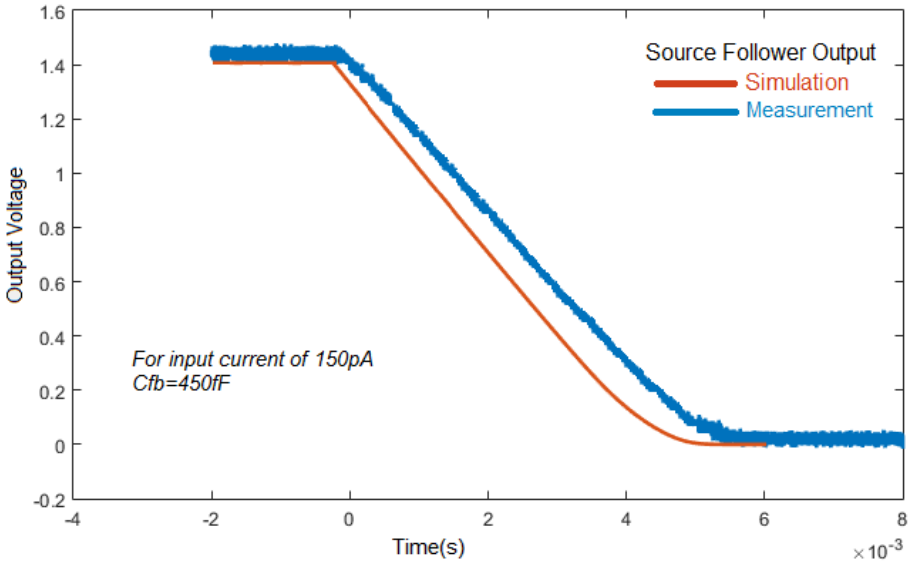


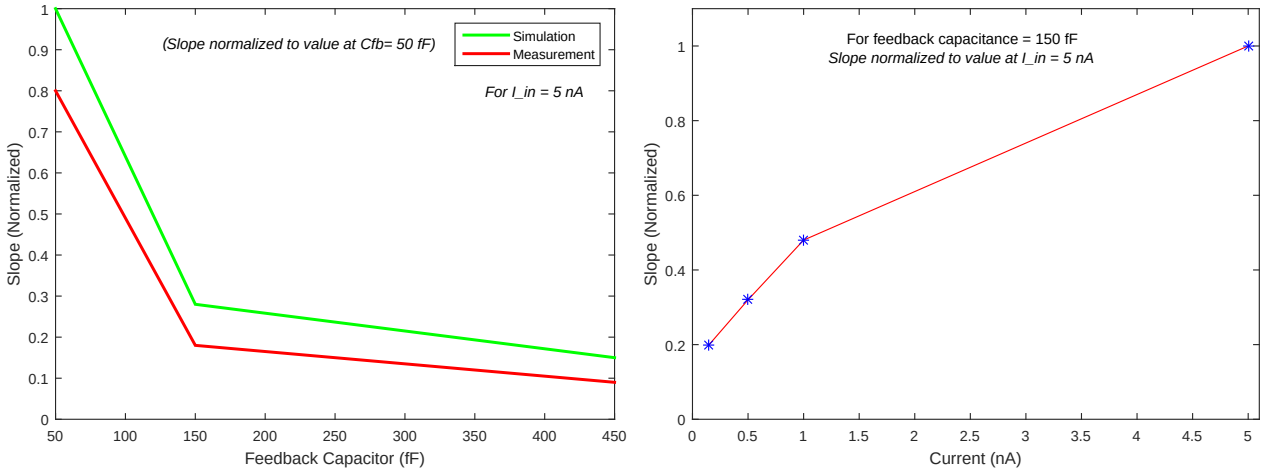
Figure 5.6: Feedback Capacitor = 450 fF, Input current = 150 pA

Gain Characteristics of the CTIA

In this test circuit, variable gain is achieved by providing different feedback capacitances which in turn also dictates the integration period for a given input current and the corresponding input capacitance. The governing equation is rewritten here for the ease of understanding.

$$V_{out} = \frac{1}{C_{fb}} \int I_{pd} dt \tag{5.1}$$

From a set of transient measurements performed for varying input currents and feedback capacitances, the slope of the curve is extracted from plots similar to those in Figures 5.5 and 5.6. The obtained result is shown in Figure 5.7. The trend from the inverse relationship of the feedback capacitances with the slope and the direct proportionality with current is observed in both these figures, as can be predicted from Equation 5.1.



(a) Normalized Slope vs Feedback Capacitor **(b)** Normalized Slope vs Input Current

Figure 5.7: Gain Characteristics of CTIA

Ideally, the direct proportionality of the slope with current will result in an intercept of zero on the Y-axis after extrapolation. The obtained result however, indicates otherwise. Moreover, the slope for an input current of 5 nA in Figure 5.7b is not coincident with the remaining points. One of the conclusions will imply that there is a possibility of junction leakage from the time of reset until the beginning of integration. It is important to quantify and determine the amount of this drift in order to ensure a correct measurement. Thus, the ongoing measurements at JPL with this chip will help provide conclusive assessment of the ROIC specifications.

Demonstration of input protection

The primary step to verifying the voltage limiting mechanism from the HV NMOS (see Figure 5.1 for the location) is to monitor the input node of the CTIA. This was done by testing the voltage at the source follower connected to the input node (labelled as V_{out2} in Figure 5.1). The obtained voltage plot from the measurement is shown in Figure 5.8.

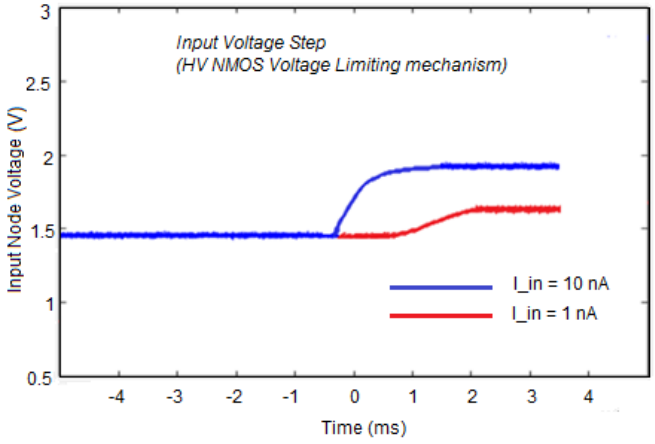


Figure 5.8: Tracking of Input Voltage using a Source Follower

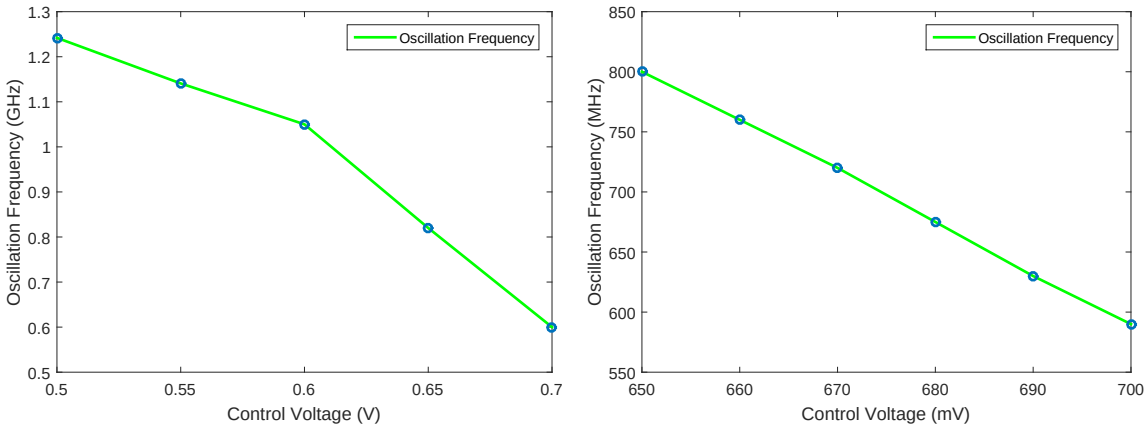
In the above plot, there is a clear observation of the rise in the input voltage (denoted as V_b in Figure 5.1) tracked by the source follower. The constant value initially reflects the ongoing integration process by the CTIA. As the integration on the feedback capacitance is complete, the input PMOS (Transistor MP1 in Figure 5.1) shuts off and the feedback action ceases to exist. This causes the input node to rise. As discussed in Chapter 2, this rise will eventually turn off the HV NMOS. This will help in debiasing of the photodiode, thereby quenching the avalanche in case, there is any. As a result of this, the low voltage CMOS circuitry is also isolated from any possible damage from the HV bias on the APD.

5.2 Post Layout Simulation Results- TDC

In this section, the post layout simulation results of various building blocks of the TDC are discussed.

5.2.1 Voltage Controlled Ring Oscillator

The current source determines the overall oscillating frequency of the VCO. The following plots reflect the sensitivity of the current source for small steps of the control voltage along with its wide range. In the figure below, oscillation frequency is plotted for varying control voltages at the nominal corner.



(a) Voltage Steps of 50 mV **(b)** Voltage steps of 10 mV

Figure 5.9: Variation in Oscillation Frequency with Control Voltage

As can be seen from the Figure 5.9b, for every 10 mV rise in the control voltage, the oscillation frequency drops by about 50 MHz. Subsequently, characteristic plots are obtained across different corners to observe the variation in the oscillation frequency at different temperatures at a control voltage of 0.5 V. The process corner conditions for the simulated results shown in the Figure 5.10 are listed below in Table 5.1.

Table 5.1: Simulation Parameters

Corner	Supply Voltage (V)	Temperature (deg C)
TT	1.2	27
SS	1.08	125
FF	1.32	-40
SF	1.2	27
FS	1.2	27

The SS corner gives the worst case oscillation frequency of about 950 MHz at room temperature. Additionally, it can be observed that the variation in frequency with temperature is the maximum for FF corner, about ±0.062% of its value at room temperature. However, these variations are not a major issue in this design since the relative oscillation frequencies in the coupled network are more important than their absolute values. Moreover, the current source is designed such that it covers a wide tuning range, thus accounting for the process variations.

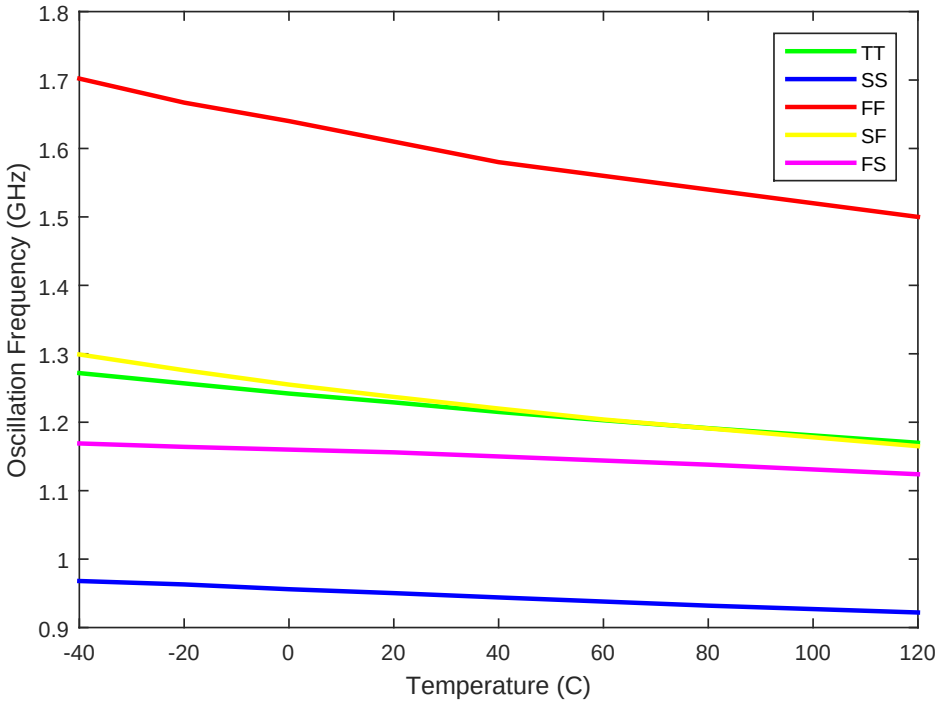


Figure 5.10: Variation in Oscillation Frequency with Temperature at V_{ctrl}=500 mV

5.2.1.1 Phase Noise

The in-band phase noise of the VCO is simulated and the results are shown in the following figure. Three cases are simulated in order to validate the improvement in performance due to sub-harmonic injection locking. In this simulation, four oscillators are coupled to each other using the coupling element circuit shown in the Figure 4.10 of Chapter 4 and a sub-harmonic signal with an injection frequency of 50 MHz is used.

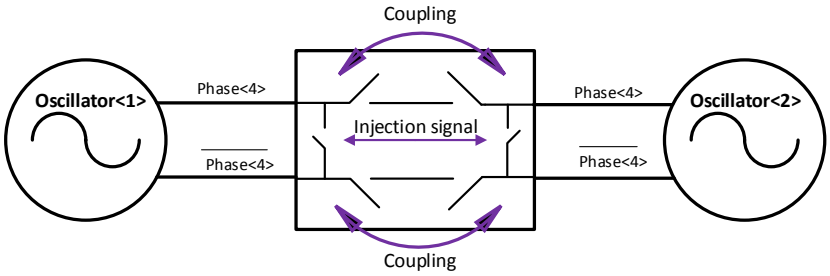


Figure 5.11: Coupled Oscillators

As described in the Section 3.1.3 of Chapter 3, the lower phase noise of the reference signal in combination with the locking of the VCO to the harmonic of this reference results in a better performance. In the Figure 5.12, one can observe that the sub-harmonic locking results in the best case phase noise of -101.8 dBc/Hz at 1MHz offset frequency, as against the one without injection locking or coupling. Without any coupling and hence, no injection, it can be observed that the phase noise is -90.77 dBc/Hz at 1 MHz offset frequency. The enabling of the coupling element already results in an improvement of close to 6 dB (-95.21 dBc/Hz) as can be expected from the combination of four oscillators being simulated. This was also seen in the analytical simulations performed in Chapter 3. It is probable that after fabrication, there is degradation in the phase noise and thus, jitter in the time domain compared to simulation results where the injection is performed using close to ideal source. But, it is believed that the relative improvement due to the injection locking will continue to exist even after fabrication, resulting in lesser jitter compared to a system without injection locking, for instance.

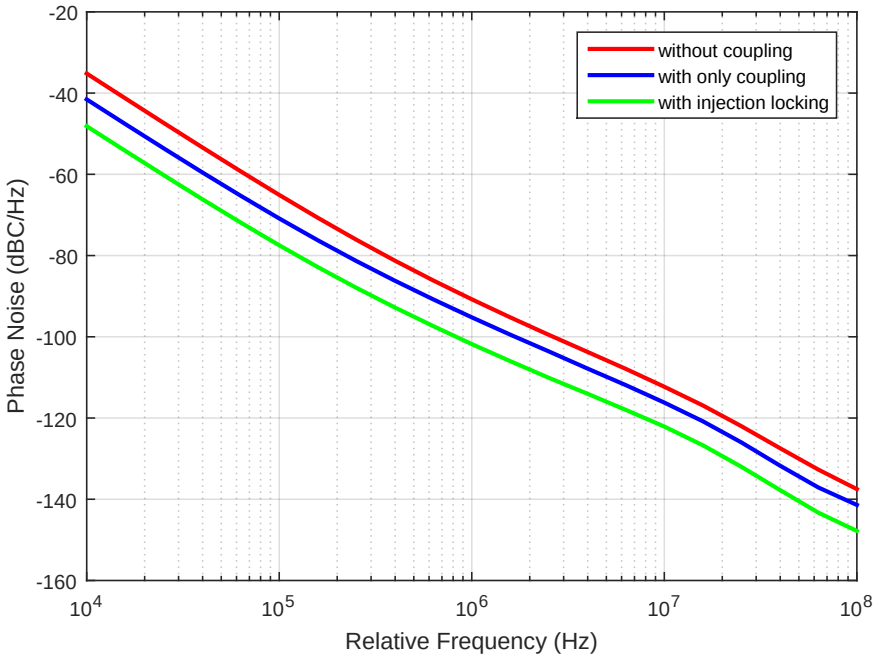


Figure 5.12: Phase Noise Performance of the VCO

Integrated RMS Jitter- As discussed in Section 3.1.2 of Chapter 3, the phase noise can be integrated to estimate the integrated RMS jitter in the time domain using the calculations shown in Appendix A. Integrating over a bandwidth of 100 kHz to 100 MHz, results in a jitter as tabulated below for the three cases of phase noise simulated above.

Table 5.2: Integrated RMS Jitter

Condition	RMS Jitter (ps)
Without coupling	15.22
With only coupling	8.173
With injection locking	3.82

5.2.2 Sense Amplifier Flip-Flop

Sense amplifier flip-flop (SAFF) is an important block since it is used to capture the 16 phases of the VCO. First, the typical waveforms of the SAFF are simulated and shown below for the ease of understanding. As explained in the Section 4.1.2, on the rising edge of the clock, since the data input is high, the node $\bar{S}$ (also seen in Figure 4.7) discharges to 0 V, which is followed by a transition to high at the output after certain delay.

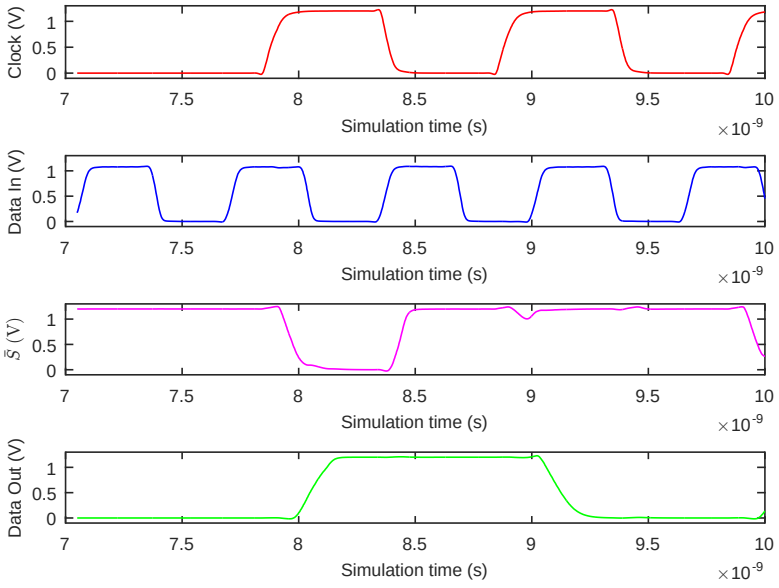


Figure 5.13: Typical SAFF waveforms

Ideally, in a sense amplifier based flip-flop, the sampling would be such that the output makes a transition to logic high when the clock samples the data beyond a switching threshold, typically at $V_{DD}/2$ in a perfectly symmetric design (marked as point M in the Figure 5.14). However, in practice, this threshold varies around the mid-value. Additionally, due to the set-up time constraints of the SAFF, the sampling of the input state is accompanied by a window of uncertainty. This window is depicted as T_{l-h} and T_{h-l} for low-high and high-low transitions in the Figure 5.14.

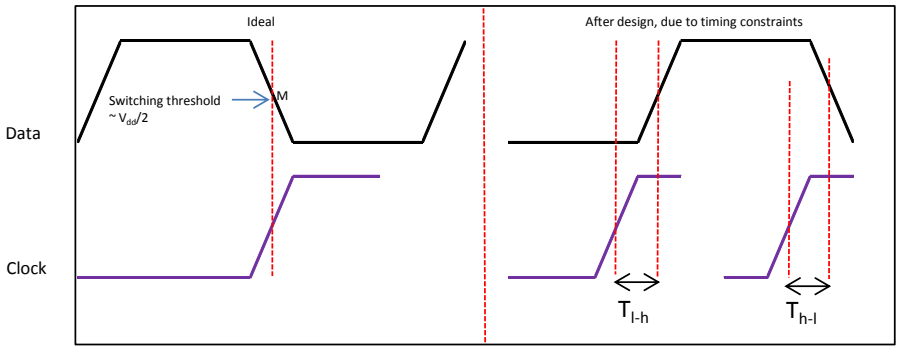
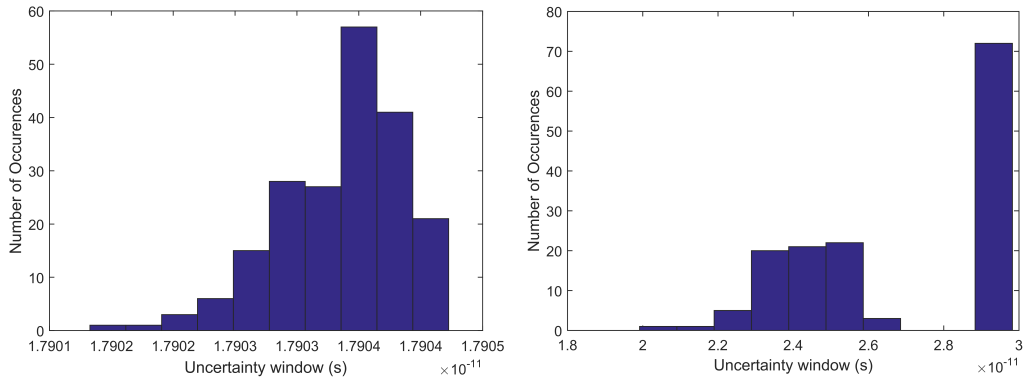


Figure 5.14: Uncertainty window in a SAFF

When the clock arrives T_{l-h} units of time prior to the rising input edge, the SAFF already samples the next state; in this case, the next state indicating a logic high. Likewise, it is possible that the rising edge of the clock pulse occurs T_{l-h} units later with respect to the rising edge of the input data and the sampling is delayed. It is important to keep these windows of uncertainty for rising and falling transitions minimal during the circuit design phase. In the SAFF designed for this TDC, the uncertainty windows defined in the above figure are determined after performing a Monte Carlo simulation on the SAFF. These plots are shown below in the Figure 5.15 for a low-to-high and high-to-low transition.



(a) For a low-to-high transition **(b)** For a high-to-low transition

Figure 5.15: Monte Carlo Simulation (N=100) - Sampling Window for Sense Amplifier Flip-Flop

As one can observe, for a low-to-high transition, the mean value of T_{l-h} is 17.9 ps and the standard deviation σ= 51.2 fs. Likewise, for a high-to-low transition (T_{h-l} in Figure 5.14), the mean is 26.98 ps and the standard deviation σ= 2.93 ps. The overall spread across the mean value is low and the worst case values are 17.904 ps and 29.825 ps respectively. These windows also suggest a direct implication in this imager design, where two subgroups share a TDC. An event in one subgroup followed by an event in the other subgroup with a time difference less than or equal to the obtained uncertainty windows will not be sampled correctly, in this case it would be ≈17.9 ps (considering the rising edges of *tof_0* and *tof_1* pulses in Figure 4.9). However, this is an issue in an extremely high frequency event. Thus, given that the activity of the event is not high in reality, the obtained values are not a major limitation.

5.2.3 Linearity

The linearity of the TDC is analysed by considering the performance of the VCO which forms the fine code and the counter, which dictates the coarse code of the TDC final code.

5.2.3.1 Performance of the VCO

The differential non-linearity (DNL) and the integral non-linearity (INL) are plotted from the post layout simulation of the VCO on Cadence. The obtained results for an oscillation frequency of 1 GHz are shown in Figures 5.16 and 5.17. It can be seen that the maximum DNL is 0.218 LSB and the maximum INL is 0.202 LSB. The results are plotted for two oscillation cycles and it can be observed that the linearity for both the cycles are consistent with each other, thus reflecting the expected linearity from the VCO. The maximum values occur at the transition from $Phase-3 \rightarrow Phase-4 \rightarrow Phase-5$ (and for their corresponding complementary signals) where, the propagation delay is larger compared to the other phases. This is expected since the pseudo-differential units of the VCO are laid out in such a way, as described in Section 4.1.1 of Chapter 4.

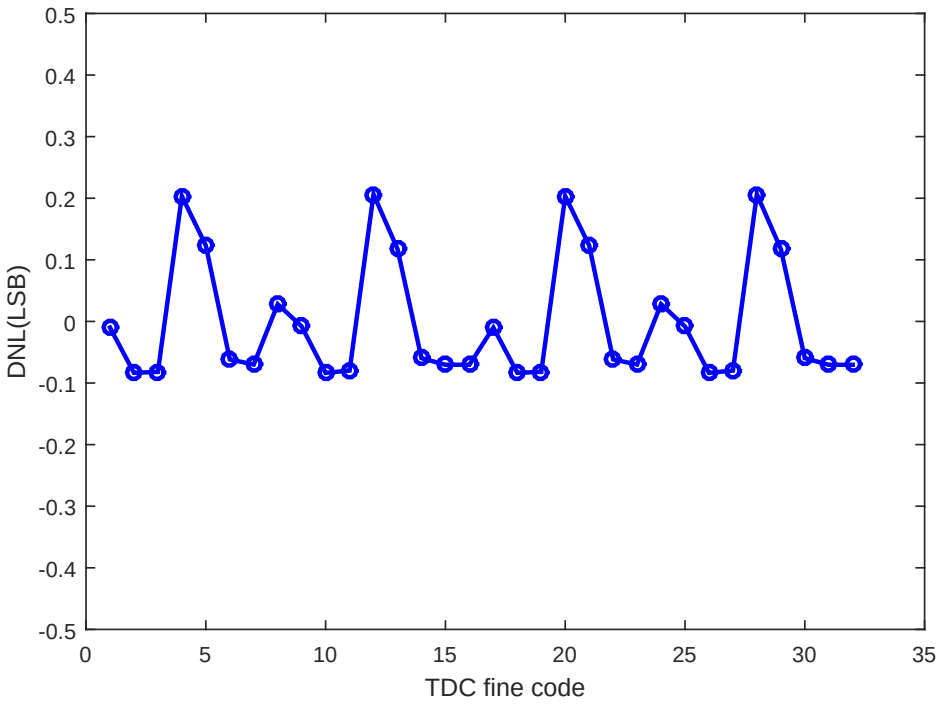


Figure 5.16: Differential Non-Linearity for two oscillation cycles

5.2.3.2 Variation in delay with temperature

It is important to evaluate the performance across a range of temperatures, especially considering that a typical application in space would make the system prone to extreme conditions. Thus, in this section, the variation of delay in the pseudo-differential units are plotted for temperature range of -40°C to 125°C at a supply voltage of 1.2 V in the Figure 5.18. The maximum difference in the average delay is 2.4 ps at 125°C compared to that at the room temperature. One can observe

that temperature variation in this range does not result in a large deviation in the delay, given the typical power supply of 1.2 V. In the next section, it will be observed that the worst case performance is determined from the corner simulation.

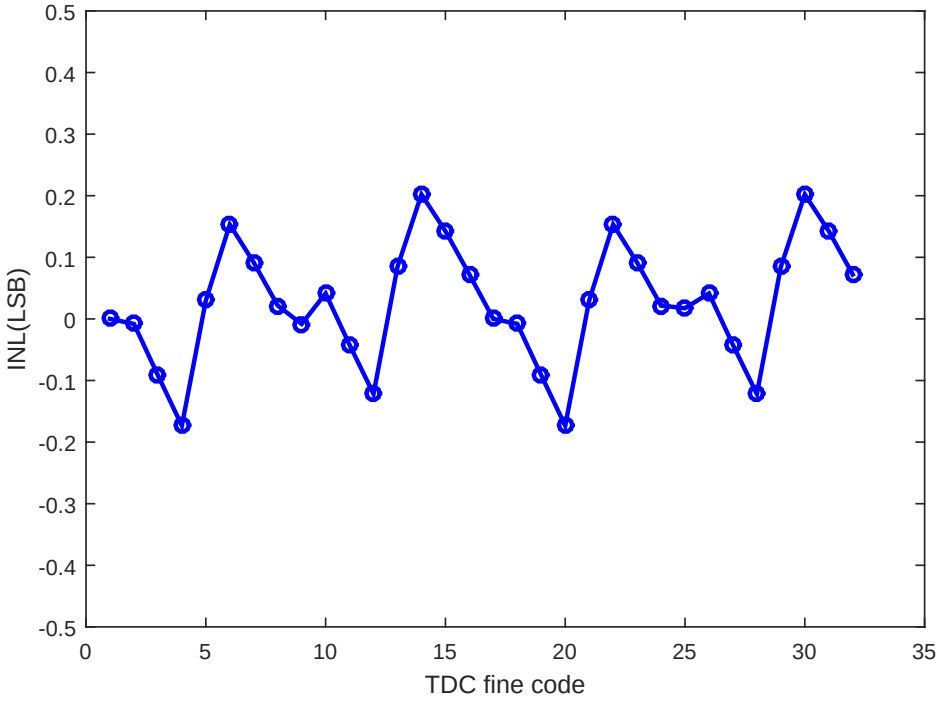


Figure 5.17: Integral Non-Linearity for two oscillation cycles

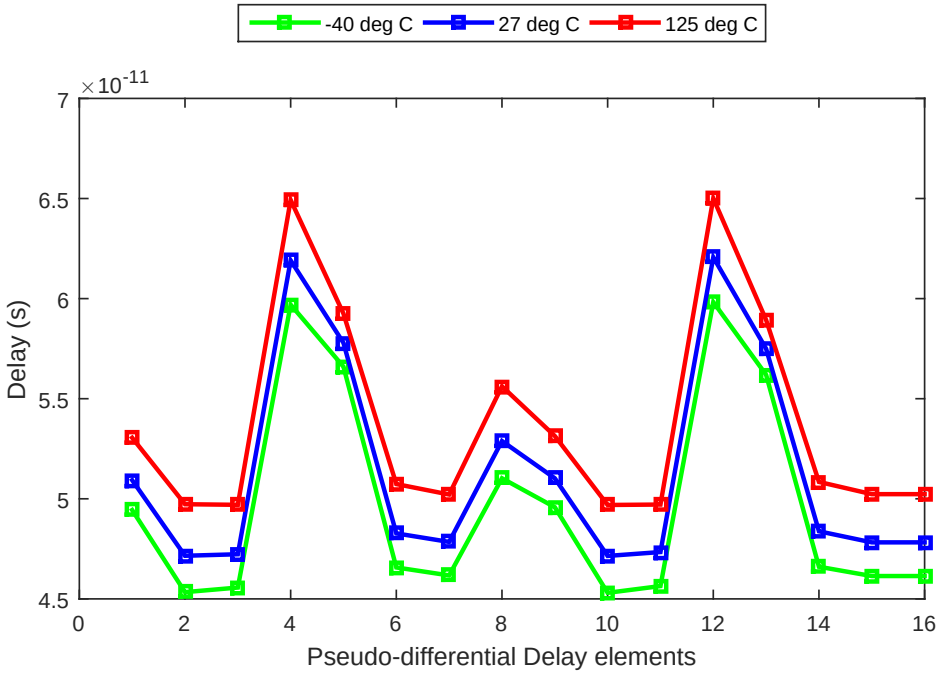


Figure 5.18: Delay Variation across temperature

5.2.3.3 TDC performance over corners

The delays at the VCO are further plotted at different corners for one oscillation cycle. The SS corner is simulated at a supply voltage of 1.08 V and a temperature of 125°C and the FF corner at a supply voltage of 1.32 V and temperature of -40°C to emulate the worst case scenarios. As can be seen below, SS and FF corner form the upper and lower boundaries for the average delay with SF, TT and FS results lying in between. Additional constraint in the power supply at ±10% of the typical value, contributes significantly towards the trend in FF and SS corners as can be observed from the Figure 5.19 below.

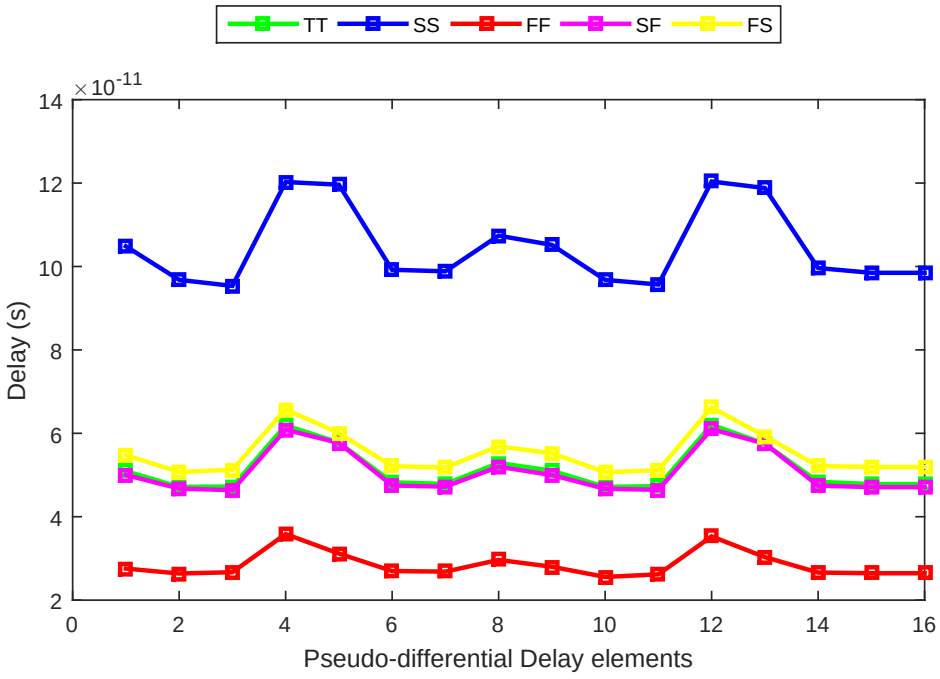


Figure 5.19: Delay Variation across process corners

The following table summarizes the average delays at different transistor model corners.

Table 5.3: Average Delay across process corners

Corner	Supply Voltage (V)	Temperature (deg C)	Average Delay (ps)
TT	1.2	27	51.44
SS	1.08	125	104.73
FF	1.32	-40	28.43
SF	1.2	27	50.72
FS	1.2	27	55.71

5.2.4 Counter

Speed of operation

A high frequency clock input is used to evaluate the performance of the 10-bit counter. It is specially important to check if the counter can count at a rapid rate, in this case at a frequency of about 1 GHz to ensure the required dynamic range of 1 µs along with the VCO. A transient simulation was run in order to cover the 10b range of the counter at different corners with input clock frequency from (1-2 GHz). The counter can increment at a frequency of 2 GHz at TT corner and in the SS corner, can still count at 1 GHz, covering the required range of 1 µs over the 10 bits.

Buffer Delay for Resampler-Sampler

As discussed in Section 4.1.3.2, it is very important to match the buffer delays along the clock signal path at the resampler and the sampler in the counter block. In the Figure 4.9, the clock buffers for the resamplers are denoted as **I<0:9>**, for the samplers, as **D0<0:9>** and **D1<0:9>** respectively for subgroups 0 and 1. The corresponding buffer delays for clk_int, tof_0 and tof_1 signals are plotted in the Figure 5.20 below at the nominal corner.

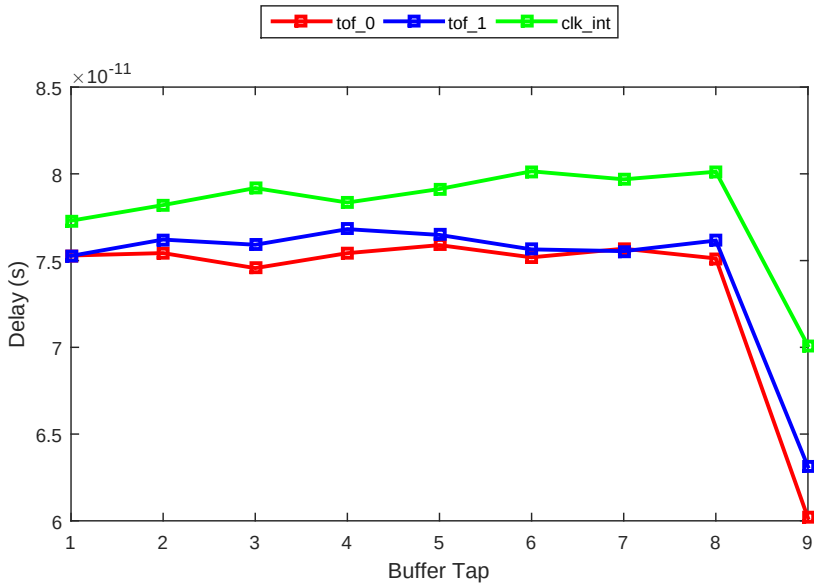


Figure 5.20: Matching between buffer delays

As can be seen, the average delay for clk_int, tof_0 and tof_1 are 78.012 ps, 73.642 ps and 74.573 ps respectively. With a relative deviation of about 5 ps of the clk_int path with respect to the tof path, it should still be possible to sample the states from the resamplers correctly, whenever there is an event.

5.2.5 Power Consumption

The whole TDC is simulated in order to derive the power consumption of the circuit. In our architecture, the VCOs run at all times for the reasons pointed out in Section 4.1.5 and whenever

there is an event, the corresponding states are sampled. In principle, lower the oscillation frequency of the VCO, lower is the power consumption of the TDC. In conditions that do not demand full timing resolution from the TDC, the control voltage is increased, in turn reducing the oscillation frequency. Under full resolution of the TDC with the VCO running at 1 GHz, the power consumption of the VCO is about 160.2 µW. When there is no sampling, the total power consumed by TDC is ≈700 µW. However, when the demand is not so high, the TDC can be operated at a lower oscillation frequency. With the VCO running at 100 MHz, the power consumption of the TDC is 220 µW.

5.2.6 Summary of specifications

A summary of specifications achieved from the post layout simulation results are tabulated below.

Table 5.4: Summary of results

Parameter	**Value**
Technology	3D IC 65 nm CMOS
TDC Area	144 µm x 11 µm
TDC Resolution	62.5 ps (mean)
TDC Dynamic Range	14 bits
Target resolution (in distance)	9 mm
Maximum Range (in distance)	150 m
Phase Noise at 1 MHz offset frequency	-101.8 dBc/ Hz (injection-locked)
DNL (VCO)	0.218 LSB
INL (VCO)	0.202 LSB
Power consumption (at f_{osc}= 1 GHz)	700 µW

Chapter 6

Conclusions and Future work

GaN Readout Circuit

In this thesis, two major tasks were accomplished for imaging application in space. The design of a front-end readout circuit in 0.35 µm CMOS for the GaN APDs was the first step towards developing UV imagers with these detectors in future. The measurement results presented in Chapter 5 only guarantee the standalone performance of the transimpedance amplifiers designed. Thus, testing and measuring the combined contraption at JPL will give accurate assessment to use the amplifiers with the GaN APDs. Additionally, as pointed out in Section 5.1.2 of Chapter 5, further characterization needs to be done to investigate the possible junction leakage in the CTIA. Moreover, noise analysis also needs to be performed and quantifying the input referred charge noise will be essential to ensure amplification of the diode current on the order of hundreds of picoamperes. Furthermore, verification of the voltage limiting action of the HV NMOS described in Chapter 3 and 5 will guarantee the protection of the low voltage CMOS from the high voltage on the APD. The ongoing testing of the readout IC with the GaN APDs at JPL will provide data, thereby suggesting precise metrics for future design. Based on those results, several other amplifier topologies can be explored in view of better compatibility, higher gain, speed and low power consumption.

TDC

The second major task undertaken in this thesis was the design of a sub-harmonically injection locked TDC array for LIDAR application in 65 nm 3D IC CMOS technology. The designed TDC, with the VCO operating in closed loop, results in a phase noise of -101.8 dBc/Hz at 1 MHz offset and a DNL and INL on the order of 0.2 LSB. The core area of the TDC is 144 µm x 11 µm. The obtained resolution is about 60 ps, guaranteed by the VCO and the dynamic range is 1 µs. Much focus was laid on limiting the overall jitter generated in the TOF system. Phase macro model based simulations performed on MATLAB provided additional impetus in understanding the dynamics involved in coupled oscillators. Another value addition in future would be to develop macro models on Verilog-AMS in order to emulate the architecture of the oscillator and predict with accuracy, the PPV for a given oscillator. This will give precise estimation of the locking dynamics for a given set of external perturbations and also help predict the phase noise of the system[14]. The testing and measurement of this chip will be required to substantiate the effect of injection locking in reducing the phase noise.

The post layout simulation results of the TDC are compared with state-of-the-art TOF imagers and

the comparison is tabulated below in Table 6.1. In addition to better linearity and dynamic range, the TDC in this work has an advantage of lower area and superior phase noise performance which when incorporated into a megapixel array, will permit large room for on-chip processing.

Table 6.1: Performance comparison with state-of-the-art

	[22], 2014	**[23], 2015**	**[24], 2013**	**This work (post-layout)**
Technology	130 nm	130 nm	180 nm	65 nm
Power Supply	1.5 V	1.2 V	1.8 V	1.2 V
Resolution	62.5 ps	71 ps	208 ps	62.5 ps
Dynamic range	64 ns	18.8 ns	853 ns	1 µs
Resolution (in distance)	9 mm	10.65 mm	31.2 mm	9 mm
Maximum range (in distance)	9.6 m	2.82 m	127.95 m	150 m
DNL	<4 LSB	+0.75 LSB	-0.52 LSB	+0.218 LSB
INL	<8 LSB	+0.65 LSB	0.73 LSB	+0.202 LSB

Appendix

A Integrated RMS jitter calculation

The SSB phase noise of an oscillator is plotted in units of dBC/Hz as a function of the offset frequency f_m. A typical phase noise curve as shown in Figure 1 below, is approximated into regions having lines with slopes $\approx 1/f^x$, where x=0, indicates a white noise region (shown as A4 in the figure below), x= 1, reflects the region with 20 dB/decade slope (A3) and so on.

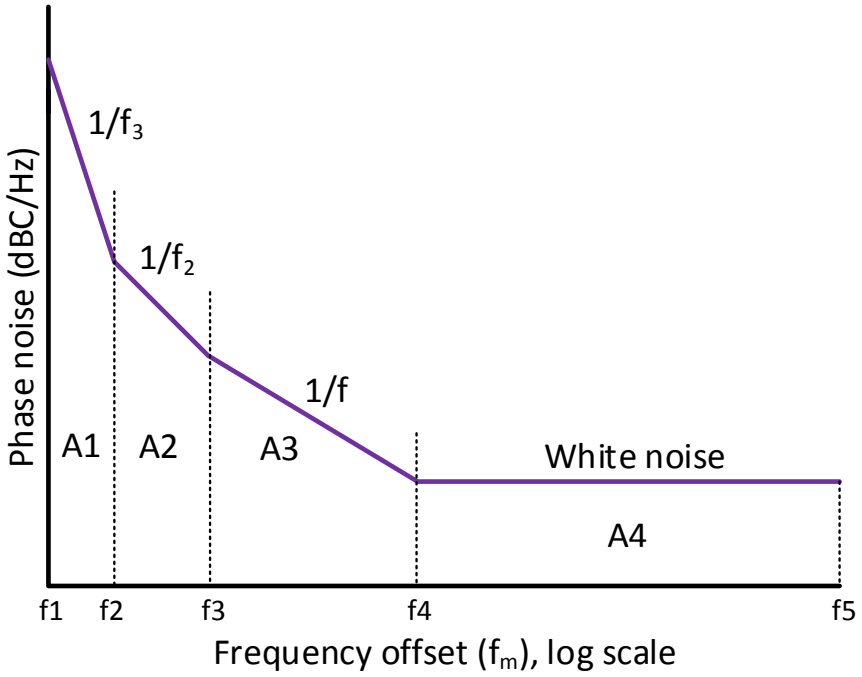


Figure 1: Oscillator phase noise

Given such a plot, the jitter is estimated by integrating the phase noise over the bandwidth of interest first. This would imply finding the area under the curve in Figure 1, such that total area A is given by,

$$A = 10log(A1 + A2 + A3 + A4) \tag{1}$$

The integrated value will have a unit in dBc. Further, the RMS jitter in radians is further calculated by the following equation[19][20].

$$Jitter_{radians} = \sqrt{2.10^{(A/10)}} \tag{2}$$

For a given oscillation frequency, f_{osc}, the jitter in seconds can be finally estimated as,

$$Jitter_{seconds} = \frac{\sqrt{2.10^(A/10)}}{2\pi f_{osc}} \tag{3}$$

B Schematics for the counter block

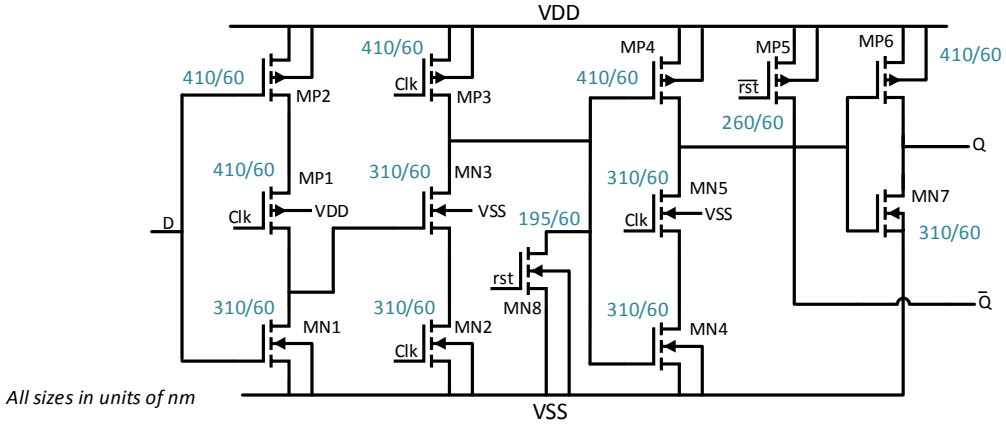


Figure 2: Unit cell- Asynchronous counter

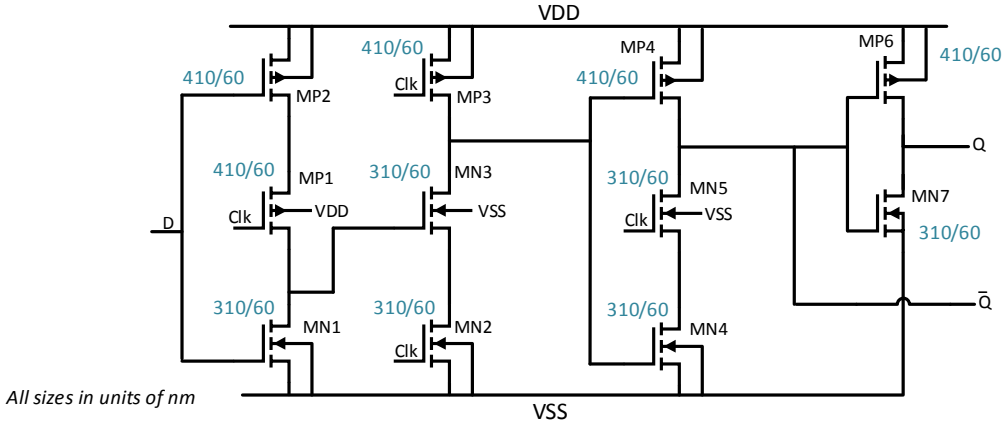


Figure 3: Resampler cell

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