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From 2-Dimensional Lithography To 3-Dimensional Structures

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Lithography for IC device fabrication is a high volume high accuracy production technology. Such production characteristics are also attractive for MEMS and 3 dimensional (3D) integration processes. However, advanced lithography has a strong 2 dimensional (2D) nature and is not optimized to fabricate 3D structures. In this work, 5 exposure and etch strategies are discussed to use advanced 2D lithography to fabricate 3D structures.

Introduction

Advanced IC device fabrication is a multi disciplinary complicated process [1] in which lithography plays an important role in terms of cost and complexity. The IC fabrication process flow comprises a sequence of processing and or stacking many virtually 2 dimensional (2D) process layers. The layout of each layer is designed in terms of XY positions and dimensions, defining either opaque or transparent areas; a binary mask. The 3rd dimension (Z) is usually not coded on the mask. Therefore, lithography as it is optimized for a high volume planar manufacturing technology has a strong 2D nature.

Today's integrated circuit (IC) device technology is a very successful integration technology, capable to integrate more than10^8 transistors in one planar system like a system-on-chip (SOC). It is therefore likely that advanced MEMS and other 3 dimensional (3D) integration and micro fabrication technologies will also employ this successful planar manufacturing approach.

Projection aligners like wafersteppers and waferscanners are the industries workhorses, however these tools are not designed for patterning non-planar 3D like structures [2]. Consequently different alignment, expose and etch strategies may be required for a successful fabrication of 3D structures. The technologies used for 3D integration MEMS and other micro fabrication technologies are very diverse and today, no clear litho requirements and roadmaps are defined. In this work, several expose and etch strategies, are discussed to convert 2D patterns into a wide range of different 3D structures.

Exposure tool requirements for 3D device fabrication

The mainstream IC technology today is CMOS process technology, a uniform well characterized manufacturing process where device scaling is the main challenge for lithography. The CMOS technology is planar, the resists films are thin and the devices are processed on one side of the wafer.

In 3D processing, there is no common manufacturing technology, dual side processing is customary, substrate topography can be several 100 μm and resist films are sometimes very thick, leading to long exposure and development times etc. Therefore, the lithographic requirements for 3D micro fabrication are more diverse. The main consequences of this diversity for alignment and exposure are discussed below.

Alignment

Contrary to front-end IC fabrication, in 3D micro fabrication, the alignment plane and imaging plane are no longer confined in one 2D XY plane. A thick resist layer or dual side processing implies that the alignment plane and image plane are separated by a distance ΔZ perpendicular to the XY plane. Furthermore, many 3D micro fabrication processes requires front to back alignment (FTBA), therefore FTBA hardware in the form of infra red alignment or additional optics is an almost indispensible option on 3D exposure tools.

Contact aligners use conventional optics and pattern recognition [3] thus the alignment performance depends on the optical quality of the out-of focus alignment. Alignment accuracies of 0.1 μm are reported [4]. But alignment on a contact aligner is a 2 point alignment and does not compensate for mask or wafer distortions, thermal expansion errors etc. Because the overlay is the result of the alignment process and subsequent lithographic processing, the overlay accuracy is usually less (larger sigma) than the alignment accuracy. For FTBA an overlay accuracy of 0.5 μm (3sigma) is reported [3].

The overlay accuracy for front side processing on an advanced projection aligner is much better than 100 nm. The FTBA overlay accuracy is usually less accurate, for an ASML PAS5500 waferstepper, 200 nm (3σ) is specified [5]. Although projection aligners are not designed for alignment on non-planar 3D like substrates it is shown that a waferstepper alignment system, based on phase gratings is fully functional in a wide range of processes used in 3D device fabrication. On an ASML PAS5000 waferstepper, used in this work, and overlay accuracy of 0.3 μm or better was obtained in processes like 500 μm out-of-focus alignment, FTBA etc. [6].

Exposure

For contact aligners, the resolution for proximity printing is limited to about 2 μm [7], however with vacuum contact printing, a resolution of 200 nm lines / 800 nm spaces is reported [8]. With specially designed illumination optics) are capable to resolve 30 μm lines/spaces at a mask-substrate distance of 500 μm [9].

A projection aligner can print features down to 32 nm, high resolution projection aligners have a very low depth of focus (DOF), not a very good property for 3D structure formation. Nevertheless, to employ the superior imaging characteristics on high topography substrates novel exposure technologies like multi step imaging (MSI) are developed [10].

Lithographic pattern transfer from 2D to 3D

For 3D micro fabrication, the 2D mask layout is transferred into an active 3D device layer by lithography and subsequent subtractive processing like etching or additive processing like plating. In some cases, the final resist pattern itself is a functional device layer [11].

The 3D device architecture and its associated substrate topography, determines to a large account which exposure strategy must be used for optimal result. 5 examples, to illustrate different exposure and etch strategies are listed below. Unless otherwise mentioned, the exposures are performed on an ASML PAS 5000 waferstepper.

Planar processing with conventional lithography: microsieve fabrication

In this example, the 3D functionality is enshrined in a stack of deposited thin films with different properties. The 2D binary lithographic pattern is vertically etched into the film stack followed by an isotropic selective etch to create the required structure(s) to fabricate a microsieve [12].

The fabrication process is schematically depicted in Fig.1. The first step is to prepare a sandwich structure that will eventually become the sieve's wall (Fig 1a). Three silicon nitride layers and three 100 nm thick silicon oxide layers are deposited alternatively on a silicon wafer. The silicon nitride forms the structural layers for the microsieve and the silicon oxide works as sacrificial layers. A photo resist layer is spin coated, the shape of sieve walls are patterned and then dry etched through the sandwich into the silicon substrate to build the "walls" (Fig.1b). All sacrificial layers are then removed in a single wet chemical etching step using buffered hydro fluoric solution (BHF) (Fig. 1c). The channels are sealed with a PDMS capping layer (Fig. 1d). Nanochannels with a precisely controlled height of 100nm are thus formed on the walls. A SEM picture of a fabricated structure before sealing is shown in Fig.1e.

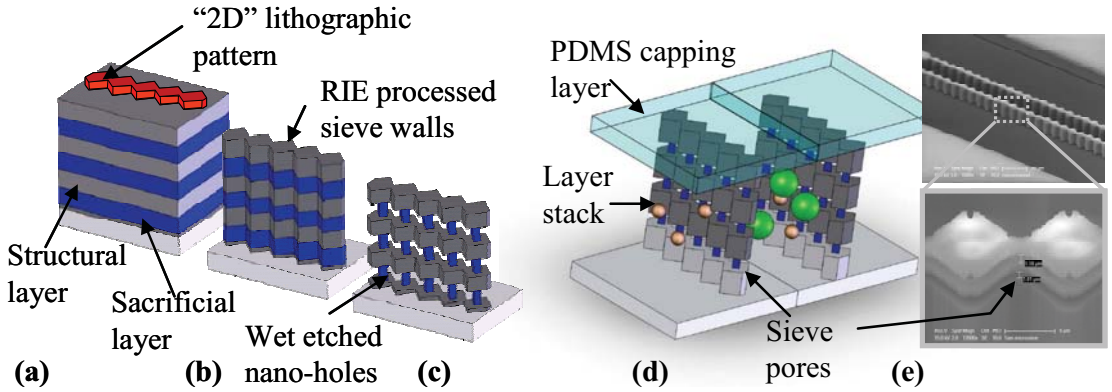

Figure 1: Schematic view of the process flow to fabricate the vertical-wall microsieve (a-c), a schematic detail of the completed device (d) and a SEM picture before PDMS capping (e).

Planar processing with conventional lithography: vertical silicon plate springs

Here a sequence of conventional 2D masking layers in combination with (deep) anisotropic etching processes is employed to create the required structures. To keep the topography compatible with the 2D nature of conventional lithography, all the masking layers must be defined before the (deep) etching processes are performed. This approach enables the use of conventional lithographic equipment and processes to fabricate the devices.

In this example, a vertical silicon plate spring (Fig. 2) [13] is fabricated with 3 masks. A back side cavity (BC) and a front side cavity (FC) to define the plate spring thickness and a device release cavity (DRC) to separate the devices. An overview of the process flow is given in figure 2, the fabrication starts with the deposition of 6 μm silicon oxide on both sides of double side polished silicon wafer. This oxide serves as hard masks for the deep reactive ion etch (DRIE) process. First the BC layer is exposed on the wafer back side and etched through the oxide. Next the DRC mask is exposed and 1.5 μm of oxide is etched. With a combined DRC-FC masking, the remaining oxide is removed at the DRC with a shorter oxide etch (figure 2b), which leaves 1 μm of oxide at the FC layer.

The BC areas are partially etched into the backside of the wafer followed by a BC lining oxide deposition (see Fig. 2c). Next the DRC is etched partly into the silicon, the

remaining FC oxide blocks the silicon etch in the FC areas (Fig. 2c). After the partial DRC silicon etch, the remaining FC oxide is removed using a maskless oxide RIE and the FC and DRC areas are further etched into the silicon (Fig. 2e). Finally, about 30 µm silicon is left in the FC areas to connect mass to the upright plate spring. The remaining oxide is removed using wet chemical etching to release the devices. From mass-spring resonance measurements, the plate spring thickness and thus FTBA overlay error was calculated and found to less than 300 nm [14].

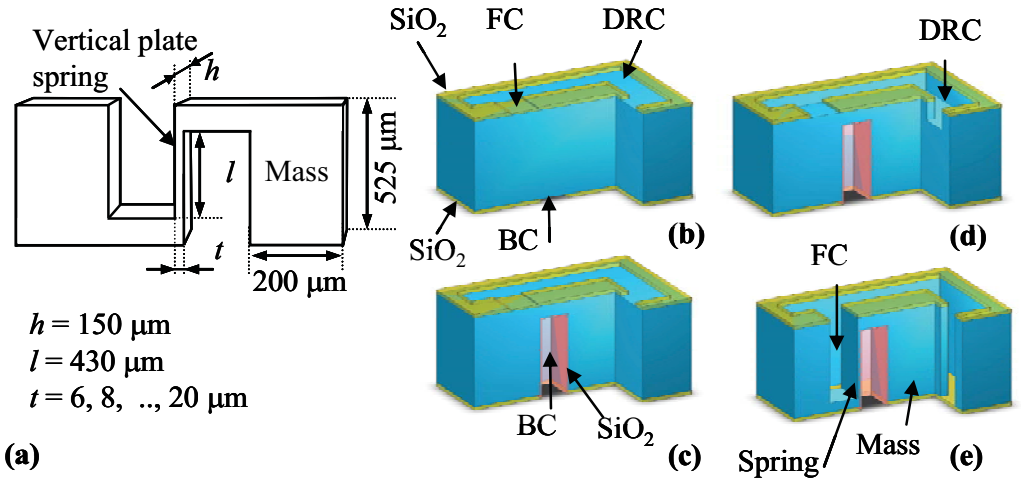

Figure 2: Schematic 3-D view of the mass-spring system with upright plate springs and the mass-spring dimensions used in this work (a). The process flow (b - e,) is explained in the text

Planar processing with gray scale lithography: dual side interconnect

With gray scale lithography, the 3rd dimension is coded in the transmission of the photomask. In this way, 3D resist patterns are formed after exposure and development. The relative thin 3D photoresist pattern is extruded into the 3rd dimension using (deep) reactive ion etching. This approach is used to fabricate a cost effective dual side interconnect for 3D integration purposes with through silicon vias (TSV) [15]. The formation of the TSV is given in figure 3.

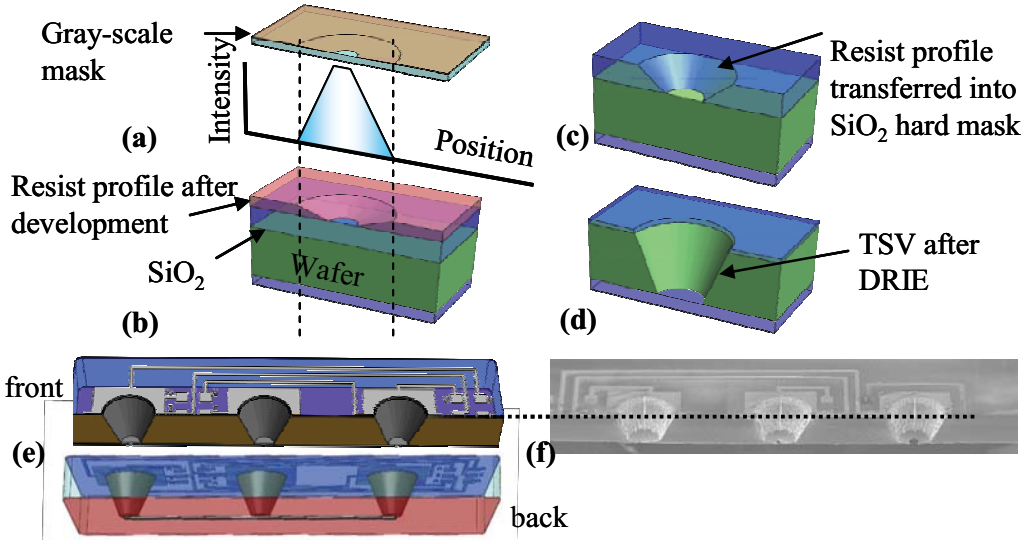

Figure 3: With gray scale fabricated TSV process flow (a-d), a schematic drawing of a Kelvin test structure with dual side interconnect test pattern with TSV (e) and a SEM image of a fabricated test structure (f).

A gray scale mask exposure (Fig 3a) is used to form a resist profile with sloped sidewalls (Fig 3b). This profile is transferred into the underlying oxide layer with RIE (Fig 3c) and further transferred through the silicon to form a TSV with lithographically designed sloped sidewalls (Fig 3d). A schematic diagram of a Kelvin test structure with dual side interconnects is given in Fig. 3e, a SEM cross-section is shown in Fig 3f.

The TSV slope determined by a designed mask transmission, not by a tuned DRIE process. An example of a TSV with partial vertical and partial sloped sidewalls is given in Fig. 4 a, an SEM cross section of such a via is given in Fig. 4b.

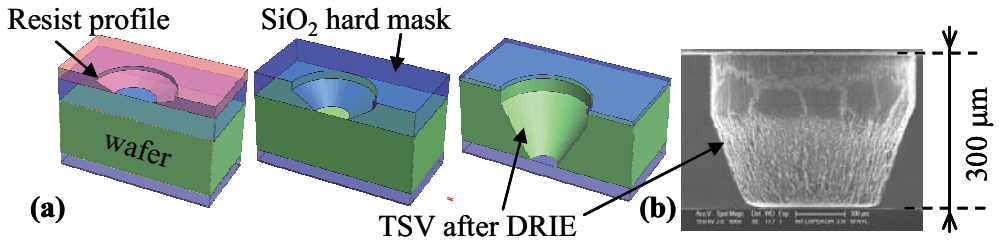

Figure 4: An example of a TSV with partial vertical and partial sloped sidewalls

Topography processing with thick photoresist: pattern transfer on vertical sidewalls

A binary mask exposure in thick photoresist, covering high topography structures can define structures on the sidewalls of that topography enabling for example vertical electrode definition in cavities [16].

Figure 5 shows a schematic description of the fabrication steps. First, 60 µm deep cavities are etched into the silicon substrate (Fig. 5a) by deep reactive ion etching (DRIE) and a 3 µm thick aluminium layer is deposited (Fig. 5b).

Next, SU8 photoresist is applied, completely covering the high topography surface (Fig. 5c). The photoresist both in the cavities and on the wafer surface is exposed using a contact aligner and developed (Fig. 5d). After aluminium etching, the SU8 mask is removed (Fig. 5e). A SEM image of a sidewall electrode is given in Fig. 5f.

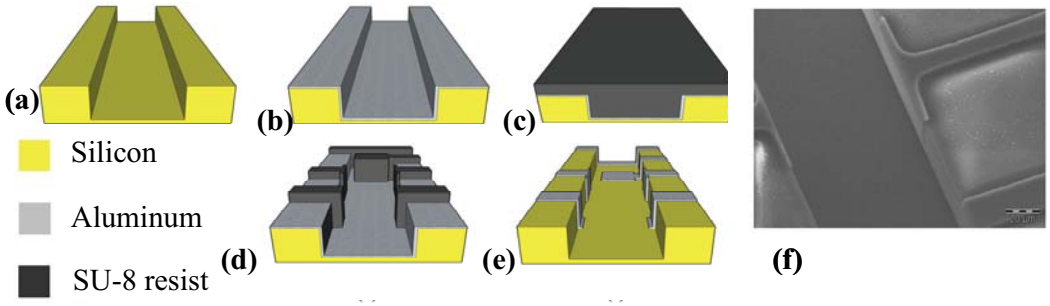

Figure 5: Schematic process flow for the fabrication of vertical sidewall electrodes (a-e), the process is explained in the text. A SEM image of a vertical electrode (f).

High resolution imaging in deep trenches

For imaging projection aligners on high topography, a large DOF is required, however there is a fundamental trade off between resolution and DOF. A good compromise is found in found in multi step imaging (MSI). MSI, developed for ASML PAS5500 wafersteppers, allows increasing the global focus offset range up to ±200 µm.

The focus system refers to the wafer surface and exposes with a focus offset to match the topography. This exposure strategy allows the imaging on the bottom of deep trenches. In a demonstrator experiment, a 3 μm thick resist film was spray coated on a wafer with 50 μm deep trenches, the trench width was 150 μm and 200 μm. With MSI, isolated features of 1 μm and 0.7 μm nominal widths were successfully imaged.

Conclusions

Mainstream lithography is optimized for IC fabrication. It is a mature production technology designed for high volume manufacturing. But the pattern transfer has a strong 2D nature. Today a wide range of etching techniques is available ranging from wet chemical isotropic etching till highly anisotropic DRIE (Deep reactive Ion Etching). It is the combinations of process sequences of wet/dry deep/shallow etching with 2-D lithography that allow us to fabricate a wide range of 3D structures.

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