Novel Application of Imprinting Lithography for Multi-bit Ferroelectric Memories

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Novel Application of Imprinting Lithography for Multi-bit Ferroelectric Memories

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Abstract

This thesis is about an innovative application of nano-imprinting lithography in organic ferroelectric memories, which can achieve multi-bit data storage. Two kinds of memory devices based on ferroelectric polymer are fabricated: ferroelectric capacitors and ferroelectric field effect transistors (FeFETs).

Here, thermal nano-imprint lithography was studied as a patterning method applied directly on poly(vinylidene fluoride-trifluoroethylene) functional polymer film. This technique helps us to replicate the grating structure of the imprinting stamp into P(VDF-TrFE) film without exposing the polymer film to corrosive etchants or high-energy radiation afterwards, thus suppressing excessive damage to the functional polymer material. Furthermore, the thermal curing process during imprinting assured that P(VDF-TrFE) exhibits ferroelectric properties.

Multi-bit memory, here defined as storage of multiple bits in a single device cell, can potentially make higher density ferroelectric memory at a lower price. The idea is based on ferroelectric response with regard to ferroelectric film thickness. The memory cells of capacitors and transistors, patterned by thermal nano-imprinting, were fabricated to test the functionality and performance of the proposed concept.

According to the results, the imprinting process did not cause any polarization loss in ferroelectric P(VDF-TrFE) film. On the contrary, with a proper control of the process condition, imprinted capacitors and transistors can be easily read and written for different bits.

The fabricated ferroelectric capacitors, with sizes down to 0.0589 mm^2, showed promising multi-bit functionality. The devices are very stable after the device retention test. Cells with four different imprinting patterns were compared, one with a repeating structure as line of 20 μm and a space of 10 μm represented the best multi-bit performance, in terms of identification of the operation voltage for different bits. As a result, a prediction of the imprinting pattern and the ferroelectric capacitor performance were given.

P(VDF-TrFE) film in the second application FeFETs were patterned with the manner as in capacitors. The smallest cell fabricated has a gate length of 5 μm and a gate width of 5 mm. The gate leakage current of the FeFET cell was only several nano-ampere, which is 10^5 times smaller

than the ON current. The memory window is near 20 V, and the current ratio for ON/OFF state is 10^5. Using a drain voltage of 50 mV, the state can be read out without changing the polarization in the P(VDF-TrFE). It is evident that the four states of the system retain distinguishable after the 10^4 second retention test.

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Chapter 1

Introduction

1.1 Motivation

To keep up with Moores Law of miniaturization of electronic devices with reduced cost and increased throughout, the semiconductor industry is under market pressure to apply more inexpensive materials and to develop new fabrication technologies to lower the production and startup cost. At the same time, they must guarantee that the quality and reliability of the products keep high standards. In order to meet these demands for next-generation products, organic materials and nano-imprinting technology have been used as promising solutions.

Over the last 20 years, tremendous progress has been achieved in the design and fabrication of organic electronic devices. Organic materials are capable to complement conventional inorganic materials with lightweight, inexpensive, and mechanically flexible organic semiconductors. Their principal advantages lie in the low temperature operation and the potentially high-throughput production. Their solution-based fabrication processes, such as spin coating, ink-jet printing, and other wet printing techniques, have been demonstrated to produce a variety of devices such as organic light emitting diodes (LEDs) [22], field-effect transistors (FETs) [26], solar cells [52], and sensors [29].

Compared with conventional photolithography, nano-imprinting lithography (NIL) does not require expensive optics or high-energy radiation sources. As a three-dimensional patterning process, NIL is not restricted to planar fabrication and can replicate patterns into certain fragile materials (i.e. biological materials) directly without exposure to corrosive etchants or high-energy radiation. Though the fabrication cost of the master stamp for imprinting is very high, the possibility to replicate other stamps from the master can lower the initial cost. The combination of the simplicity of the process and the availability of inexpensive equipment make NIL an attractive patterning method. After many years of development, NIL has become an important component for nanotechnology, with the possibility to scale devices down to the single macromolecule level. Table 1.1 shows a comparison between different lithography technologies.

Another advantage of NIL is its resolution. Since NIL relies on direct mechanical deformation of the resist material, it can achieve resolutions beyond the limitations set by light diffraction or beam scattering. Superior to some other competing manufacturing techniques,

Lithography type	Practical resolution limit	Feasibility	Throughput	Cost
EUV lithography[56]	10 nm	Good	High	High
E-beam[11]	10 nm	Good	Low	High
SPM[43]	15 nm	Good	Low	High
Imprinting[46]	5 nm	Good	High	Low

Table 1.1: Comparison of different lithography technologies [8].

such as Extreme ultraviolet (EUV) lithography, E-beam lithography and Scanning Probe Microscopy lithography (SPM), NIL has a relatively high resolution, down to 5nm, while at the same time it is able to be fabricated with high throughput and a relatively low cost. Furthermore, it can also be integrated with roll-to-roll (R2R) line production for patterning the flexible electronic devices. In 2003, NIL was considered a next generation lithography candidate on the International Technology Roadmap for Semiconductors (ITRS) [2] and found its way to the roadmap for the 32 nm node and beyond [18].

Since the first demonstration of NIL in the mid 1990s, patterned magnetic media for memory devices has become a key application of NIL technology [3]. By making micro- or nano-pattern formations via NIL techniques, high-density integration per unit area (high information storage capability) can be achieved in memory devices. Other than patterning magnetic media, NIL is also suitable for other memory materials, especially some organic polymers.

In this thesis, the microscaled devices are memories that utilize ferroelectric polymers. Information-storage devices fabricated from ferroelectric polymers such as poly(vinylidene fluoride) (PVDF) and its copolymers with trifluoroethylene (TrFE) have attracted much attention because of their potential use in nonvolatile memory technology.

Generally, ferroelectric materials with micro- or nano structures can be fabricated via either the top-down route or the bottom-up route.

For the top-down route, there are three main approaches: focused ion beam patterning (FIB) [53, 15], electron beam direct writing (E-beam) [4] and lithography methods. The first method FIB, which has a resolution down to 20 nm, changes the surface property due to the platinum ion doping. The second method, E-beam, though proven to be powerful in patterning ferroelectric arrays with lateral sizes down to 75 nm [5], uses aggressive particle beams that can damage the surfaces and deteriorate the ferroelectric or piezoelectric performance. Superior to those two methods, lithography techniques can build structured ferroelectric film from top-down with a simpler process and less cost. Imprinting lithography, as one of the lithography techniques, has been proved to be able to cause less damage to the target material by avoiding harsh developing and etching. It can also be well applied on both organic and inorganic ferroelectric materials. With the possibility of patterning in a roll-to-roll line, imprinting lithography has the potential for a much higher throughout than its current competitors.

In order to build the micro- or nano-structures from bottom-up, it can generally go through either physical or chemical means. Pulsed Laser Deposition [36] is one of the physical means of which the nanostructure can be achieved. Though it is possible to form

crystalline partials at the range of $4 \sim 20$ nm [50] via this method, the results suffers from poor registration and limited control over feature size, which in turn limits the practical interest of these systems. Sol-gel synthesis of nanostructures [47] is a typical chemical route for preparing the ferroelectric film, which is commonly used for inorganic ceramics. Recently, Langmuir-Blodgett deposition has been used for making ultra-thin film of ferroelectric polymers [48], however there are difficulties in making micro- or nano- 3D patterns by this method.

1.2 Aim and scope of the thesis

In this thesis, nano-imprinting lithography is used to pattern ferroelectric P(VDF-TrFE) – poly(vinylidene fluoride-trifluoroethylene). The main objectives of this thesis are:

1. To employ thermal imprinting lithography to pattern high quality ferroelectric P(VDF-TrFE) with grating structures, and to fabricate multi-bit ferroelectric memories utilizing imprinted P(VDF-TrFE). Two kinds of ferroelectric memory cells are fabricated: ferroelectric capacitors and ferroelectric field effect transistors.

2. To characterize and optimize the memory performance, given prediction of the pattern design.

3. To pave a way for fabrication multi-bit ferroelectric memories on flexible substrates that can be mass-produced on a roll-to-roll line.

This project was performed at Holst Centre/TNO in Eindhoven, The Netherlands. Technologies for manufacturing affordable flexible electronics are developed in Holst Centre/TNO together with its industrial partners in an open innovation environment.

1.3 Outline of this thesis

This thesis is structured as follows;

Chapter 1 is an introductory chapter, which explains the motivation and the objectives of the thesis.

Chapter 2 gives a general overview of imprinting lithography and ferroelectric memory. The current status of both techniques and the principles behind them are given. The ferroelectric properties of the organic polymer used in the thesis work are also described. Then, the idea to realize multi-bit memory functionality using imprint technology is proposed.

Chapter 3 presents the result of thermal imprinting quality on P(VDF-TrFE). The thermal imprinting quality of patterning grating micro-structure in ferroelectric P(VDF-TrFE) is investigated. The morphology properties of the imprinted patterns are studied and a discussion of causes and solutions for the imprinting defects are given.

Chapter 4 study the device performance of imprinted ferroelectric capacitors. The influence of the imprinting patterns, initial film thickness and area downscaling on the multi-bit memory performance is investigated.

Chapter 5 investigates the imprinted ferroelectric transistors, which uses non-destructive readout and mitigate the downscaling issue in capacitors. Also, the retention performance of the multi-bit ferroelectric memory is evaluated.

Chapter 6 concludes the thesis and provides some topics of future work.

Chapter 2

Background

This chapter is dedicated to the introduction of the nano-imprinting lithography, the current status of ferroelectric memory, the background related to the origin of the working mechanism in ferroelectric memory and the physical properties of the ferroelectric polymer employed in our work. The concept of multi-bit ferroelectric memory is also briefly explained.

2.1 Nano-Imprinting

Nano-imprinting lithography (NIL) is a promising lithographic technique for high-throughput patterning of polymer nanostructures at great precision and at low costs. It has been demonstrated to be suitable for large-area replication up to the wafer-level, with features down to the nanometer scale. It can be broadly divided into thermal nano-imprinting lithography (thermal NIL, also called "hot embossing"), and UV nano-imprinting lithography (UV NIL). In both processes, the replication is based on the squeeze flow of a viscous material between a stamp and a substrate via intimate contact. The demoulding process should be done after the resist fully conforms to the surface relief of the stamp.

In thermal NIL, the resist is heated above its glass transition temperature, while in UV NIL, the resist is exposed to UV light for curing. Since UV NIL requires a UV-curable resist, and thermal NIL can utilize any thermoplastic resists, thermal NIL has a high degree of freedom in the selection of materials. Imprinting processes involve the press of a stamp against a resist, however, in UV NIL, less pressure is required and imprinting is performed at a relatively low temperature. By using partially or wholly transparent stamps, UV NIL can solve the alignment problem better than thermal NIL. Table 2.1 shows a comparison between both methods. From a time- and energy-consuming point of view, UV NIL is superior to thermal NIL. Though thermal NIL requires much higher imprinting pressure, it sometimes helps to achieve a more uniform thickness distribution of residual films. In UV NIL, the process is sensitive to the parallelism and flatness of the stage and the stamp, as the resist is in liquid form, the resulting non-uniform thickness distribution of the residual can cause interference patterns [49].

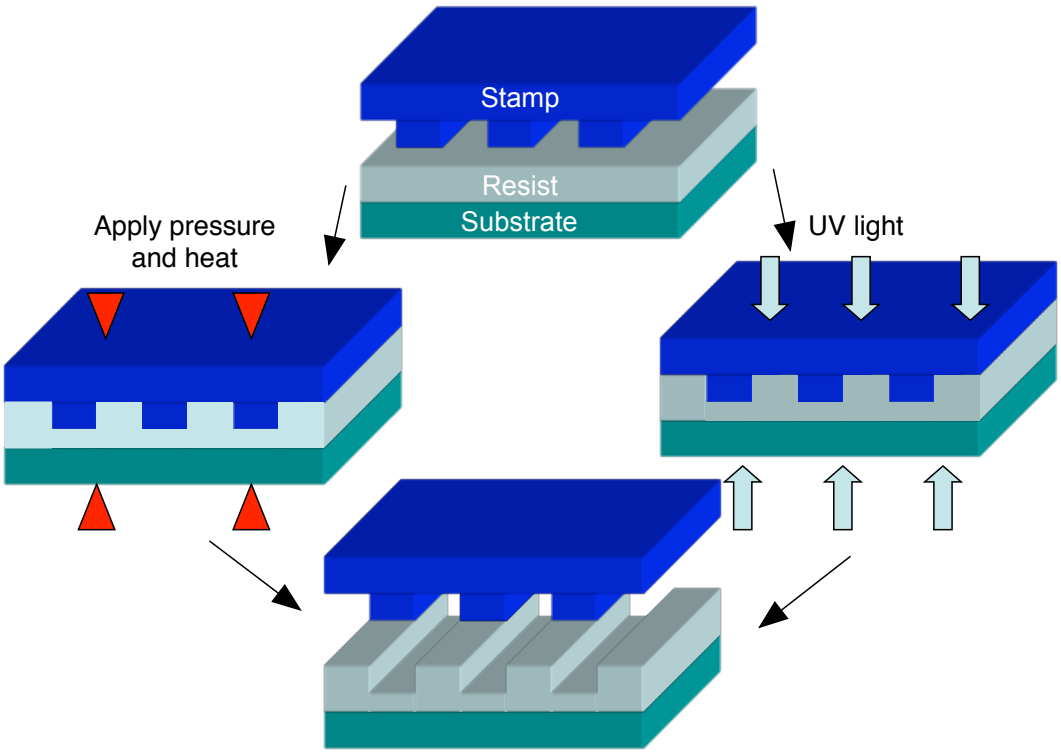


Figure 2.1: Schematic of the process for thermal NIL and UV NIL

	NIL Type	
	Thermal NIL	**UV NIL**
Pressure	20 – 100 bar	0 – 5 bar
$T_{imprinting}$	100 – 200 °C	20 °C (ambient)
$T_{demoulding}$	20 – 80 °C	20 °C (ambient)
Resist materials	Solid, thermoplastic	Liquid, UV curable
Stamp materials	Si, SiO_2	Glass, transparent
Stamp area	Full wafer, $>$ 200 mm diameter	25×25 cm^2

Table 2.1: Comparison of thermal NIL and UV NIL [8]

	Flash NAND	**FRAM**	**Inorganic FeFET**	**Organic FeFET**
Read time	70 ns	110 ns	20 ns	60 ns
Write time	1 ms	110 ns	500 ns	0.3 ms
Retention	10 years	10 years	30 days	$>$ 30 days
Cycling endurance	$> 10^5$	$10^{10} \sim 10^{12}$	$> 10^{12}$	10^3
Basic Cell	1T	1T-1C	1T	1T
Reference	[34]	[1]	[34]	[34]

Table 2.2: Specifications of ferroelectric memory versus flash memory

The various applications of nano-imprinting lithography includes hybrid plastic electronics, organic thin film transistors (TFTs) and electronics, diffractive optical elements, waveguide polarizers, high resolution organic light emitting diode (OLED) pixels, high density quantized magnetic disks and patterned magnetic media [16]. In 1997, a group in the University of Minnesota applied nano-imprinting in patterning Si field effect transistors [17]. Later, with the development of the imprinting technology and the memory technology, nano-imprinting has been more often used in patterning some other memory materials, such as in the $Ge_2Sb_2Te_5$ phase change material [58] and in ferroelectric materials. As a simple way to make ordered arrays of nanostructures, nano-imprinting has been previously demonstrated for patterning ferroelectric ceramics [21].

As previously mentioned, imprinting lithography is a process based on the squeeze flow of a viscous material between a stamp and a substrate, thus the interface properties strongly affect the imprinting replication quality. To prevent the resists from peeling away from the substrate, several approaches have been proposed: anti-adhesive coatings of the stamp [30, 45], non-sticking stamp materials [25], non-sticking resist materials [10], and dissolvable stamps [44]. In this thesis, Si stamps with anti-adhesive coatings were used, the details of which will be discussed in Chapter 3.

2.2 Ferroelectric Memory

Ferroelectric memory is a type of non-volatile memory that utilize materials that exhibit ferroelectricity, which will be discussed in detail in the next sections. The potential of ferroelectrics to become the ideal memory was already recognized decades ago[37]. At an early stage, ferroelectrics got worn out after repeated rewriting for computer memory. To solve this, we can either deposit ultra-thin films of ferroelectric material, or use a material tough enough to withstand being repeatedly erased and overwritten. Though ferroelectric properties can also be utilized in a wide variety of other applications, the primary research activity remains in the development of ferroelectric memory. A comparison of the device performance is shown in Table 2.2. As a matter of fact, modern inorganic ferroelectric materials perform well enough for memory applications, as evidenced by their commercial availability [48] .

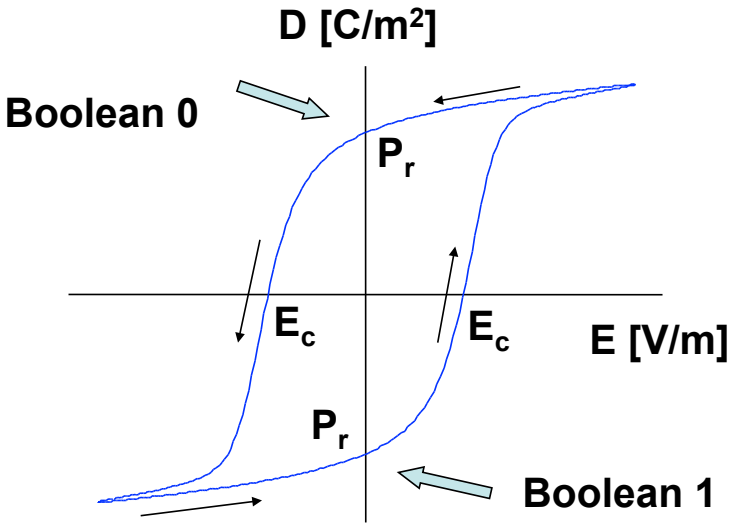


Figure 2.2: Typical hysteresis loop for ferroelectric materials

2.3 Ferroelectricity

Ferroelectricity was discovered in 1921 in Rochelle salt ($KNaC_4H_4O_64H_{\ 2}O$) by Valasek [54]. It was found that the *"electrical properties of Rochelle salt crystal are analogous to the magnetic properties of iron, the dielectric displacement D and polarization P varying with the electric field E in the same general manner as B and I vary with H for iron, and showing an electric hysteresis with loops distorted by an amount corresponding to the permanent polarization P_0."* [55]. After that, ferroelectricity remained a scientific curiosity for a long period of time until the discovery of ferroelectric ceramics *e.g.* barium titanate ($BaTiO_3$) in 1944 and later most notably, the lead zirconate titanate ($Pb(Zr,Ti)O_3$, PZT) family of materials. Today, these ferroelectric ceramics are widely used in industry for making transducers, thermistors, sensors, memory capacitors and more [19].

Materials that show ferroelectricity are called ferroelectric materials. In them, the memory function is based on the remanent polarization, which originates from the alignment of intrinsic dipole moments inside a crystalline material [48]. Therefore, a ferroelectric must be a crystal or at least a semi-crystal. However, not all crystalline materials are ferroelectric. If the crystal symmetry of ferroelectrics is too high, the dipole moments can cancel each other out completely.

Ferroelectric materials exhibit electric hysteresis with spontaneous polarization loops distorted by an amount corresponding to a remanent polarization P_r (seen in Figure 2.2). The remanent polarization P_r is the polarization that remains inside the material in the absence of an external voltage. The coercive field E_c represents the field necessary to bring the polarization to zero, which also represents the minimum field that required to switch the full remanent polarization [6]. The switching mechanism in ferroelectric materials generally in-

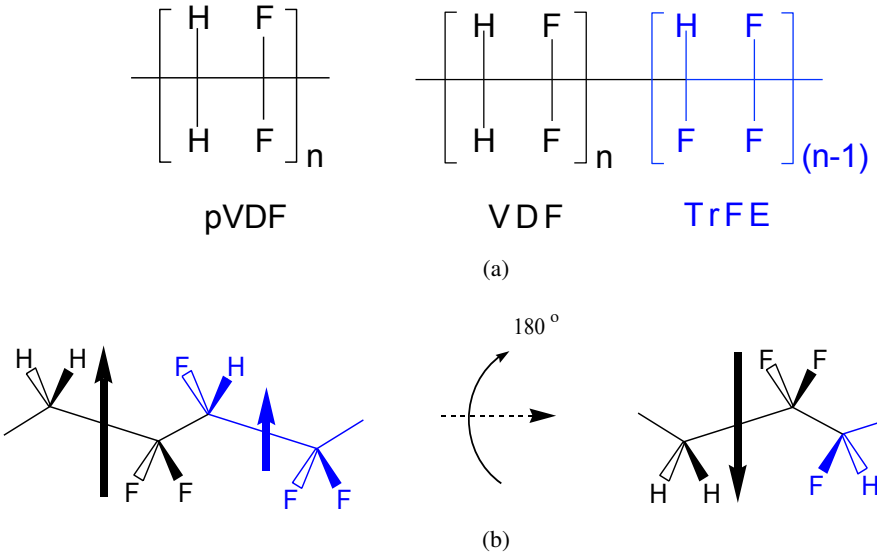
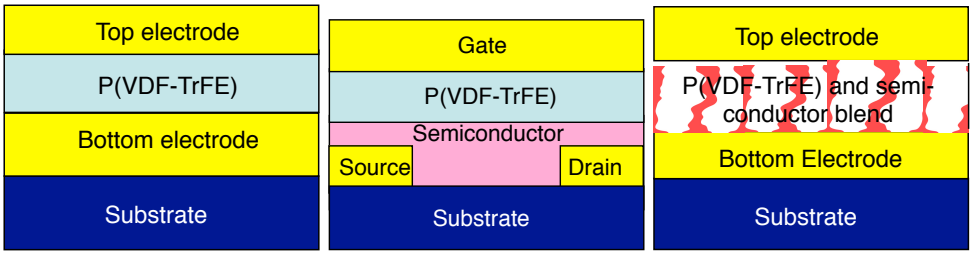


Figure 2.3: (a) Chemical structures of P(VDF) and P(VDF-TrFE); and (b) the polarization reversal operation in P(VDF-TrFE)

volves the nucleation and growth of ferroelectric domain regions, in which all the dipole moments have the same orientation. At low fields the external energy is not able to nucleate domains and make crystal grow. At fields close to the coercive field, the ferroelectric starts to polarize. And at fields higher than the coercive field, the ferroelectric saturates since the maximum amount of polarization has been reached. For practical operation of the ferroelectric material, the polarization switching should be done below the dielectric breakdown field of the material; otherwise the high electric field can destroy the device.

2.4 Organic ferroelectric polymers and its memories

Recently, organic ferroelectric polymers have been implemented in many devices because of their advantages over ceramics, such as low production costs, ease and flexibility of fabrication in a variety of thin-film forms, chemical stability, acceptable remanent polarization, excellent switching behavior, and resistance to degradation caused by strain or defects [42]. Among those ferroelectric polymers, poly (vinylidene fluoride), P(VDF) and its copolymer poly(vinylidene fluoridetrifluoroethylene), P(VDF-TrFE) are the most promising polymeric materials. The chemical formula of P(VDF) and P(VDF-TrFE) are shown in Figure 2.3 (a). P(VDF) was first recognized for its piezoelectricity by Kawai in 1969 [32]. Permanent dipoles that are formed between hydrogen and fluorine atoms can be rotated around the carbon backbone by applying an electric field large enough to induce conformational change of the polymer chain, resulting in bistability [35]. However P(VDF) thin films processed from a solution or the melt are not ferroelectric, since the dipole moments inside cancel each other due to the stereo-chemical conformation and the crystal structure. To make P(VDF) ferro-



(a) Capacitor (b) Transistor (c) Diode

Figure 2.4: Layout of ferroelectric devices

electric, it is necessary to change its conformation, which can be achieved by performing additional steps, such as stretching. Instead, it is also possible to use P(VDF-TrFE) to avoid these additional steps. Because of the steric hindrance from the additional fluorine atoms in poly(trifluoroethylene) P(TrFE), which induces an all-trans stereo-chemical conformation that aligns the direction of the dipole moments, solution-processed P(VDF-TrFE) films are ferroelectric from the very beginning. On the other hand, P(VDF-TrFE) thin films require an annealing step at a temperature around 140 °C for raising the crystallinity of the polymer and at the same time to enhance its ferroelectric response [38]. For details about these materials, readers are recommended to the references [40] and [34]. In P(VDF-TrFE), the polarization switching is carried out by 180°rotation of dipole moments around the chain axis (seen in Figure 2.3 (b)). The flipping of the $–CF_2–$ groups around the chain axis can occur once the electric field is larger than the energy barrier for dipole rotation. A coercive voltage is needed to completely trigger the flipping of the $–CF_2–$ groups around the chain axis in a two-dimensional surface lattice structure of P(VDF-TrFE) [28].

To improve the crystallinity of semicrystalline P(VDF-TrFE), an annealing process is always introduced. An important parameter of P(VDF-TrFE) is the Curie temperature T_c. Annealing above T_c can help to drive chain molecules in P(VDF-TrFE) to rearrange their positions and form a highly crystalline state. The potential for creating a ferroelectric memory technology based on P(VDF-TrFE) was recognized in 1983 [35]. So far, three types of ferroelectric memories that use P(VDF-TrFE) have been established; a ferroelectric capacitor, a ferroelectric transistor and a ferroelectric diode (Figure 2.4). Memory unit capacitors and diodes are sandwiching highly uniform thin film between two electrodes, while for transistors, the bottom electrode changed semiconductor substrates. In 1986, Yamauchi reported for the first time FeFET memory based on P(VDF-TrFE) [57].

2.5 Current status of P(VDF-TrFE) patterning

To micro- or nano-structure the ferroelectric cells is an effective way to increase the memory storage capacity. Though the selective etching of material using a patterned mask is common in complementary metal oxide semiconductor (CMOS)-based memory fabrication, it is not suitable for patterning functional polymer materials such as P(VDF-TrFE). To avoid

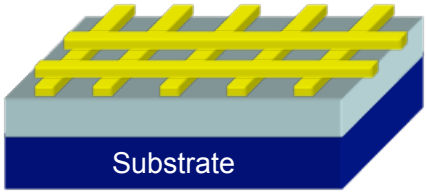


Figure 2.5: Memory with crossbar arrays

significant damage to the surface, as well as changes to ferroelectric properties under the harsh patterning conditions, P(VDF-TrFE) is preferred to patterned with soft lithography such as nano-imprinting.

One common way to realize memory and logic devices with high-density integration is to pattern crossbar arrays. A simple device structure consists of a switching material sandwiched between two metal nano-electrodes is shown in Figure 2.5. The bottom and top electrodes are aligned perpendicular to each other, building a crossbar array.

The works done by Kang *et al.*[31], Hu *et al.* [28] and recently Harnagea [20], are all targeting the formation of isolated ferroelectric 3D structures, which can be embedded in the crossbar arrays.

In [27], Hu *et al.* employed nano-imprinting lithography with stamps bearing nanotrenches (width ranging from 40 to 250 nm) to pattern P(VDF). By imprinting, P(VDF) crystals orient with the chain axis parallel to the walls of the stamp and with the fast growth direction along the trenches. Their work demonstrated that imprinting can used for adjusting the crystal ordering of P(VDF) locally.

In [31], Kang *et al.* fabricated various topographic P(VDF) microholes scaled down to 400 nm by imprinting with PDMS stamps. Utilizing a one step imprinting process, P(VDF) was selectively transformed into the ferroelectric phase.

One of the targets of this thesis is to employ imprinting lithography to pattern 3D grating structures in ferroelectric polymer, in order to achieve multi-bit functionality in a single memory cell. Since imprinting is used to modify a single memory cell in our work, ferroelectric material on the substrate is not isolated. On the contrary, the residue layer of the ferroelectric material is the key factor for our multi-bit memory functionality.

2.6 The principle of multi-bit ferroelectric memory

For a simple parallel-plate capacitor, as depicted in Figure 2.6, a charge separation in the plates causes an internal electric field. The value of this electric field can be derived from the external voltage and film thickness: $E = V/d$. The electric field has the same direction as the applied voltage. The value of charge displacement is $D = \varepsilon_{di}E$, with ε_{di} the dielectric permittivity. For a ferroelectric capacitor, where ferroelectric material sandwiches in two plates, the value becomes $D = \varepsilon_{di}E + P$, with an additional polarization P. The polarization P is originally generated from the internal electric dipoles. If two charges $+Q$ and $-Q$ are

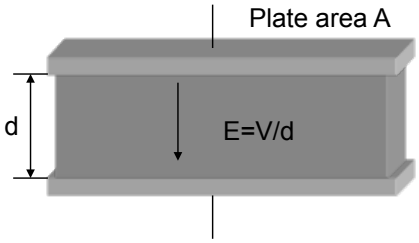


Figure 2.6: Schematic of a parallel-plate capacitor

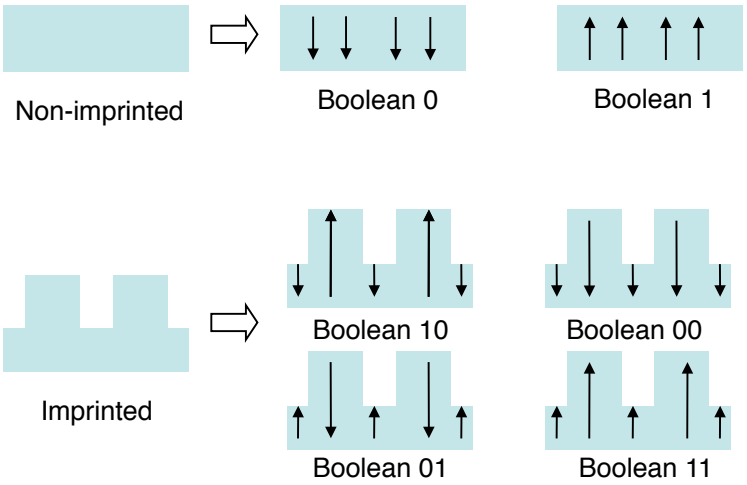


Figure 2.7: The memory mechanisms of P(VDF-TrFE) with uniform layer thickness and with grating structures

separated by a distance d in a dipole, an electric dipolar moment p forms as: $p = Qd$, with d the distance vector connecting two charges. Then the polarization P can be defined as the total electric dipolar moment: $P = \sum p$. It is clear that the value of P depends on the size, the orientation and the surface area density of the dipolar moments. Besides, since polarization P is hysteretic, this vector will depend on both the switching history and the instantaneous applied field.

As explained in the previous section, to rotate the dipole orientation in P(VDF-TrFE) is actually to flip the $-CF_2-$ groups as shown in Figure 2.3 (b). The electric field has to be larger than the energy barrier for dipole rotation to realize this flip. Therefore, a higher coercive voltage is needed to trigger a thicker ferroelectric film. For P(VDF-TrFE) with a grating structure, there would be four trigger voltage points corresponding to the two different layer thicknesses. By controlling the dipole direction, four memory states can be attained in the imprinted P(VDF-TrFE), while only two in the non-imprinted one as illustrated in Figure 2.7.

For a non-imprinted ferroelectric capacitor, writing "0" or "1" data requires the application of a voltage $+V$ or $-V$. Similarly, writing "00" or "11" data in the imprinted capacitor

also requires the application of $+V$ or $-V$, whereas the voltage must be higher than the coercive voltage for the thick film in order to drive all the dipoles down or up. When the applied voltage is just enough to rotate the dipoles of the thin film, the memory state will change from "00" to "01", or from "11" to "10", depending on the voltage is negative or positive. As a matter of fact, in order to write "01" or "10" data from a random state, the common approach is to first achieve "00" or "01", and then apply the opposite voltage to rotate the dipole direction in the thin film. Due to the ferroelectric property of P(VDF-TrFE), the memory state is retained in the absence of the external electric field. Since the read-out signal varies with the type of ferroelectric memory, the reading mechanism is different in ferroelectric capacitors and transistors. The details of the operational mechanism will be described later in Chapter 4 and 5.

Chapter 3

Imprinting ferroelectric polymers

In this chapter, the thermal imprinting quality of patterning micro grating structure in ferroelectric P(VDF-TrFE) is investigated. The morphology properties of the imprinted patterns are studied and a discussion of cause and solution for the imprinting defects are given.

3.1 Background

As a thermoplastic material, P(VDF-TrFE) has been demonstrated to be suitable for patterning with thermal imprinting [13]. Different from other groups works, which are mainly focused on making mesoscopic ferroelectric cell arrays by thermal imprinting [31, 20], our work focuses on employing thermal imprinting for the fabrication of micro grating structures in P(VDF-TrFE) films to achieve multi-bit ferroelectric memory.

3.1.1 Thermal imprinting

The thermal imprinting process is a process combining temperature and pressure, as explained in Figure 3.1. Normally, the imprinting temperature is preferred to be around

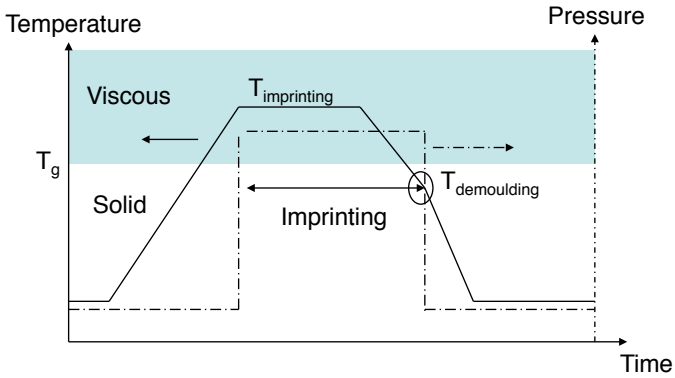


Figure 3.1: Temperature / pressure sequence for thermal-imprinting lithography

$50 \sim 70$°C higher than the glass transition temperature T_G of the imprinted material. This is because when the temperature is below T_G, the deformation of the imprinting material is very small. Furthermore, when the temperature is just above T_G, though the deformation is relatively large, it will recover after the force is released. Further increase of temperature to $50 \sim 70$ °C above T_G, the material exhibits a viscous liquid flow state, and the deformation is irreversible, which is proper for the imprinting process. During the demoulding process it is preferred to perform at a temperature lower than T_G. However, it should not be too low either, as the larger the operation temperature range, the bigger the thermal mismatch between the stamp and the substrate. This mismatch can introduce pattern distortions or stress that build-up during the cooling cycle, and it would affect the pattern fidelity and registration accuracy.

To determine the proper applied pressure, there are two main criteria that should be followed: First, the pressure should not be too high as to damage the mechanical properties of both the stamp and the substrate. Second, the pressure should not be too low as to be unable to compensate the lack of flatness of the substrate and the stamp, by conformal bending over large areas.

It has been known that for a long imprint time, polymers can replicate topographies with a high fidelity; however a shorter imprint time is sometimes preferred for the sake of high throughput. Since in most cases, the process parameters such as pressure p, temperature T, and time t can be varied to some extent, and trade-offs are possible between the parameters and, for example; a shorter t can be compensated by a higher P, or vice versa.

3.2 Experimental

Since our device was fabricated on Si substrates, imprinting with Si stamps can reduce defects introduced by the thermal expansion mismatch. The 4-inch Si stamps were prepared by photolithography. To fabricate the stamps, a positive resist (HPR504) was first spin coated on to the Si wafer, after UV exposure with a bright field mask by a Karl Suss mask aligner, and developing with PLSI, an etching process of the Si with plasma was performed. At the end, Si stamps with a protruding structure were obtained. The height of the protruding parts are 270 nm and 130 nm. There are four groups of horizontal dimension for line / space in the grating structure, which are 10 µm / 10 µm, 20 µm / 20 µm, 10 µm / 20 µm, and 20 µm / 10 µm, as illustrated by the Scanning Electron Microscope (SEM) images in Figure 3.2.

Since imprinting is a process based on the squeeze flow of a viscous material between a stamp and a substrate, the interface properties strongly affect the imprinting replication quality. In order to obtain a physicochemically stable surface without affecting the shape of the patterns on the stamp, the stamps were coated overnight with an anti-adhesive fluorinated silanes FDTS (1H,1H,2H,2H-Perfluorodecyltrichlorosilane, 97% ($C_{10}H_4Cl_3F_{17}Si$)) self-assembled monolayer (SAM) by vapor phase deposition in a desiccator. The SAM is a monomolecular layer with a thickness of 2–3 nm that is adsorbed on the stamp surface. The water contact angle test proved that the SAM coated Si surface is highly hydrophobic (Figure 3.3 (b)). However after repeated imprinting, fluorinated silanes always gradually

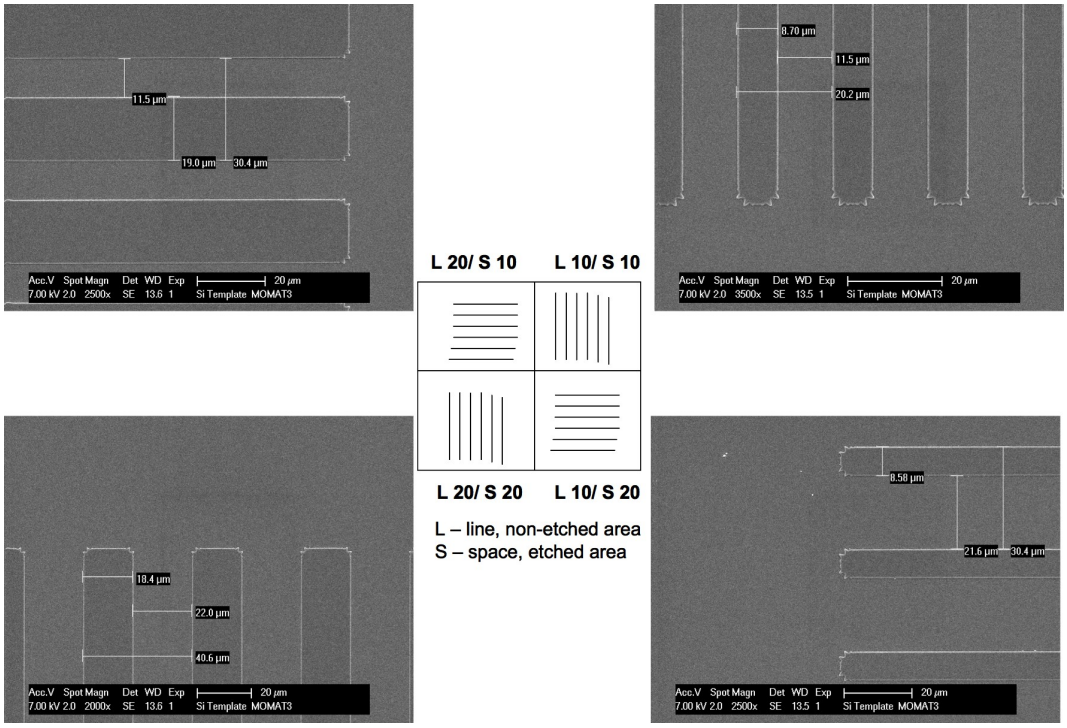
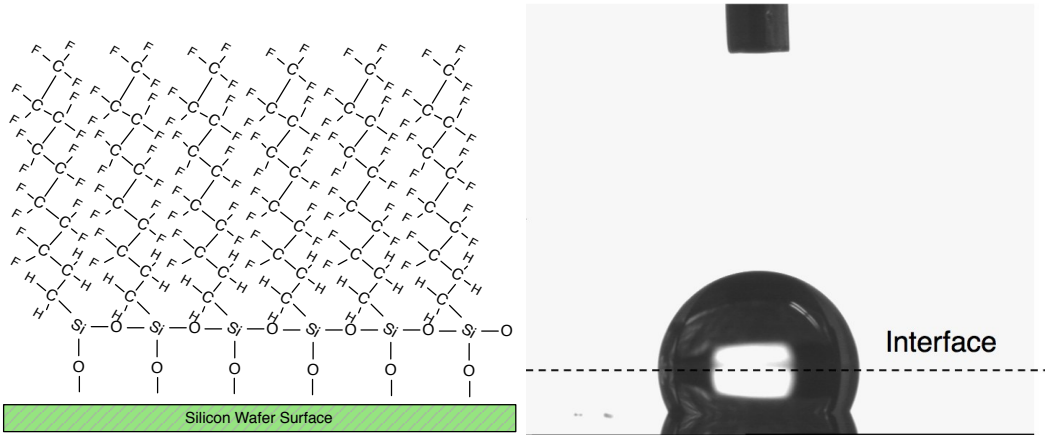


Figure 3.2: SEM images of the Si stamps with four horizontal dimensions for line / space

diffused from stamp to the imprinting material, and eventually left a hydrophilic surface on the stamp. Thus a periodic reapplication of the fluorinated silane SAM on top of Si stamp is required. And before applying SAM, a proper cleaning process of the stamps should be performed in order to remove any contamination.

3.2.1 Material preparation and imprinting process

P(VDF-TrFE) (weight ratio 77:23) offered by Solvay Solexis was dissolved in cyclohexanone or cyclopentanone at 65 °C with a concentration of 6 or 8 wt. % (weight percent). P(VDF-TrFE) films were spin coated onto the substrates from filtered solutions, where the filters have 0.2 µm pores. The spin speed is 2000 rpm for 1 minute, with a pre-spin of 4–5 seconds at 500 rpm. The film was pre-annealed at 95 °C before imprinting. The imprinting was performed with 3 tons on a 4-inch wafer (a pressure of 37 kbar) at 135 °C for 1 hour with a Specac press. The demoulding temperature was 65 °C. The schematic of the thermal imprinting machine is shown in Figure 3.4. Two planar hot plates are used, and an external heating and cooling system controls the temperature of the plates. The stack in between the two hot plates consist of aluminum foil and conductive foil, which are used to transfer the heat and to prevent mechanical damage to the stamps and substrate, as well as the hot plates.



(a) (b)

Figure 3.3: (a) Scheme of anti-adhesive treatment of FDTS on Si surface and (b) camera photograph of water droplet on Si stamp with fluorinated silane SAM on top. The water contact angle is 103.23°

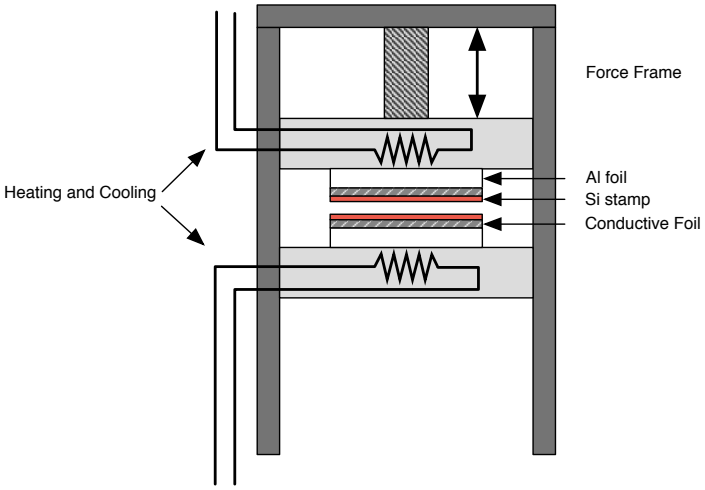


Figure 3.4: Schematic drawing of the thermal-NIL equipment

3.2.2 Characterization methods

An optical microscope and a SEM were used to characterize the Si stamps and the imprinted film quality. Differential Scanning Calorimetry (DSC) measurements were performed by using DSC Q1000 V9.9 Build 303 equipment with a heating rate of 10 °C/min and a scanning range from room temperature to 200 °C. Atomic force microscopy (AFM) measurements were performed with a Veeco Dimension 3100 SPM, using a Si probe in the tapping mode. The P(VDF-TrFE) layer thicknesses were determined by using a Dektak profilometer.

3.3 Results and discussion

When spin coating at the same speed, the film thickness depends mainly on the boiling point and viscosity of the solvent and concentration of the P(VDF-TrFE) solution. In this thesis, the spin speed was always 2000 rpm which resulted in the following layer thicknesses:

- 6 wt. % P(VDF-TrFE) in cyclohexanone: 230 nm
- 8 wt. % P(VDF-TrFE) in cyclohexanone: 410 nm
- 8 wt. % P(VDF-TrFE) in cyclopentanone: 370 nm

The glass transition temperature of the P(VDF-TrFE) used in our experiments is -40 °C, which means that theoretically the replication can even be performed at room temperature. However, in order to optimize the ferroelectric properties of P(VDF-TrFE) during the imprinting process, it is required to use an imprinting temperature between the Curie temperature T_C and the melting temperature T_m [28]. This is firstly because there is typically a reduction in crystallographic symmetry at the Curie temperature and this creates more than one symmetry-related, spontaneously polarized and distorted state below this temperature [51]; and secondly, because P(VDF-TrFE) does not recrystallize well from the melt, the polarization decreases dramatically when the imprinting temperature is higher than T_m. The thermal properties of the P(VDF-TrFE) used in this report were measured with DSC and displayed in Figure 3.5. According to the DSC results, the Curie transition and the solid-to-liquid (or liquid-to-solid) transitions of P(VDF-TrFE) occur at 129 °C and 141 °C, respectively. To fulfill the requirement above, the imprinting temperature was set at 135 °C.

The surface morphology results obtained by AFM (Figure 3.6) show that the annealing process at 135 °C helped to increase the crystallinity in P(VDF-TrFE), which is the requirement for presenting ferroelectricity. According to the phase image in Figure 3.6 (d), after annealing at 135 °C, films consist of crystallites, which are interconnected as a maze. The root-mean-square surface roughness is 4.5 nm, which is a typical value for semicrystalline polymers.

Theoretically, in the case of grating structures patterning, when the stamp height is h, the horizontal ratio of the line and space of the stamp is m (the horizontal ratio of the line and space of the imprinted polymer is $\frac{1}{m}$) and initial layer thickness D ($D \gg h$), the thickness of the thin part is $d = D - \frac{h}{m+1}$, and of the thick part is $d = D + m\frac{h}{m+1}$. For example, if $h = 270$

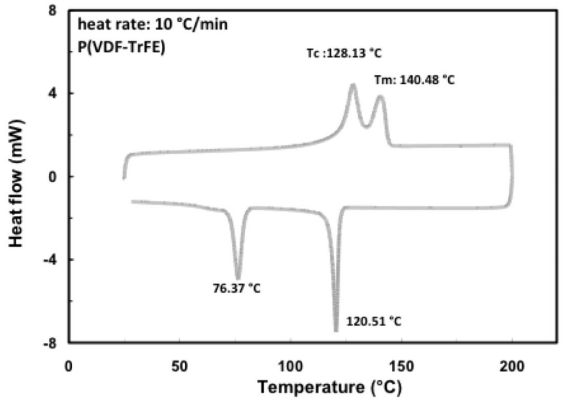
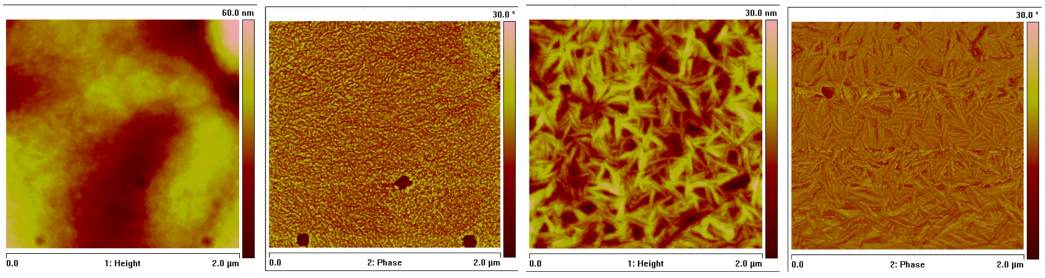


Figure 3.5: DSC results for P(VDF-TrFE) powder



(a) (b) (c) (d)

Figure 3.6: (a), (b) spin coated P(VDF-TrFE) after pre-annealing at 95 °C (c), (d) spin coated P(VDF-TrFE) after annealing at 135 °C for 1 hour on hotplate In which (a) and (c) are the height images, while (b) and (d) are the phase images.

nm and $D = 410$ nm, while $m = 0.5$, then $d_{thin} = 230$ nm and $d_{thick} = 500$ nm; while $m = 2$, then $d_{thin} = 320$ nm and $d_{thick} = 590$ nm; while $m = 1$, then $d_{thin} = 275$ nm and $d_{thick} = 545$ nm. It is clear that the film thickness of P(VDF-TrFE) varies with the initial layer thickness, the stamp height and the imprinting patterns. The experimental results of the film thickness by Dektak are illustrated in Table 3.1, which correlates with the theory. The difference for pattern Line: 20 µm, Space: 10 µm is caused by the stronger disperse during the imprinting process.

Other than the temperature, there are some other parameters during the imprinting process that needs to be taken into consideration. Imprinting P(VDF-TrFE) at 135 °C, some different defect modes of film were observed at the micro-scale level, as shown in Figure 3.8. The defects in (a) and (b) are caused by an improper demoulding process, and since they can cause shorts in the device, they are the most fatal defects. On the other hand, defects depicted in (c) and (d) are both related to incomplete filling. There are two possible reasons for this, either the imprinting time is not long enough or the air was trapped in between the interface. Without a well-defined height profile, a multi-bit memory property

Horizontal Dimensions	**Initial Layer Thickness** $D = 370$ nm **Stamp Height** $h = 270$ nm	**Initial Layer Thickness** $D = 410$ nm **Stamp Height** $h = 270$ nm	**Initial Layer Thickness** $D = 410$ nm **Stamp Height** $h = 130$ nm
Line: 10 µm **Space: 10 µm**	$d_{\text{thick layer}} = 531$ nm $d_{\text{thin layer}} = 227$ nm	$d_{\text{thick layer}} = 550$ nm $d_{\text{thin layer}} = 250$ nm	$d_{\text{thick layer}} = 420$ nm $d_{\text{thin layer}} = 290$ nm
Line: 10 µm **Space: 20 µm**	$d_{\text{thick layer}} = 561$ nm $d_{\text{thin layer}} = 285$ nm	$d_{\text{thick layer}} = 570$ nm $d_{\text{thin layer}} = 280$ nm	$d_{\text{thick layer}} = 460$ nm $d_{\text{thin layer}} = 330$ nm
Line: 20 µm **Space: 10 µm**	$d_{\text{thick layer}} = 466$ nm $d_{\text{thin layer}} = 187$ nm	$d_{\text{thick layer}} = 440$ nm $d_{\text{thin layer}} = 140$ nm	$d_{\text{thick layer}} = 404$ nm $d_{\text{thin layer}} = 269$ nm
Line: 20 µm **Space: 20 µm**	$d_{\text{thick layer}} = 512$ nm $d_{\text{thin layer}} = 239$ nm	$d_{\text{thick layer}} = 550$ nm $d_{\text{thin layer}} = 250$ nm	$d_{\text{thick layer}} = 440$ nm $d_{\text{thin layer}} = 310$ nm

Table 3.1: Imprinted P(VDF-TrFE) film thickness as measured by *Dektak profilometer*

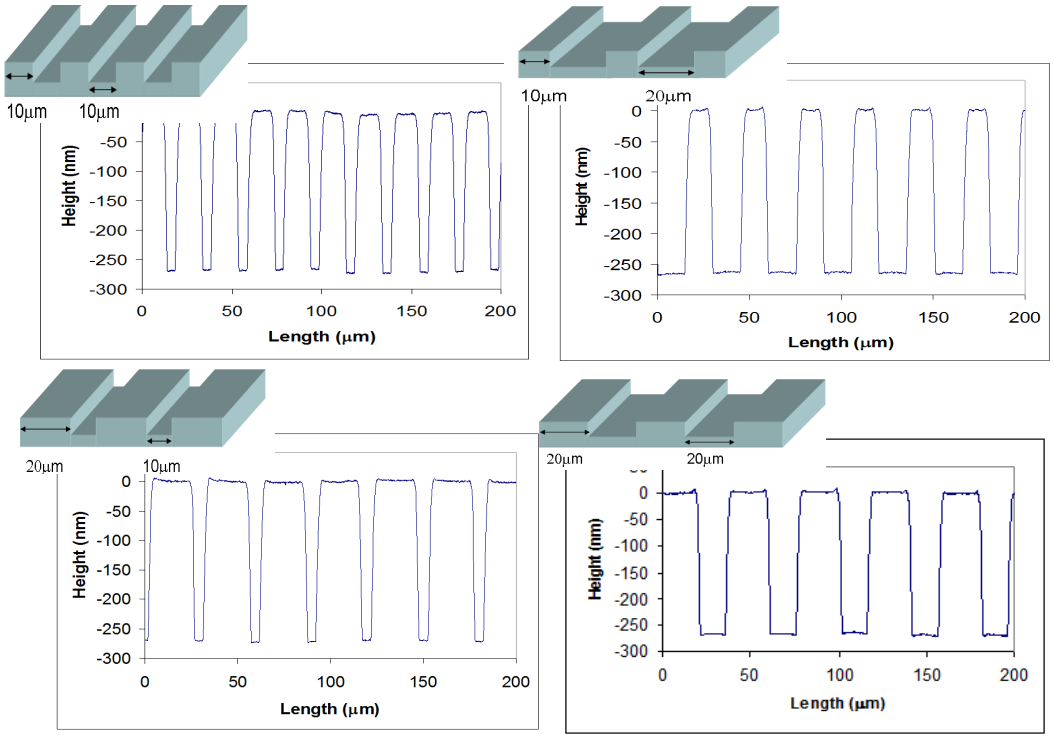


Figure 3.7: Surface scan profiles by Dektak profilometer (scan length: 200 µm) corresponding to imprinted structure with periodicity of line: 10µm / space: 10 µm, line: 10 µm / space: 20 µm , line: 20 µm / space: 10 µm, line: 20 µm / space:20 µm, respectively.

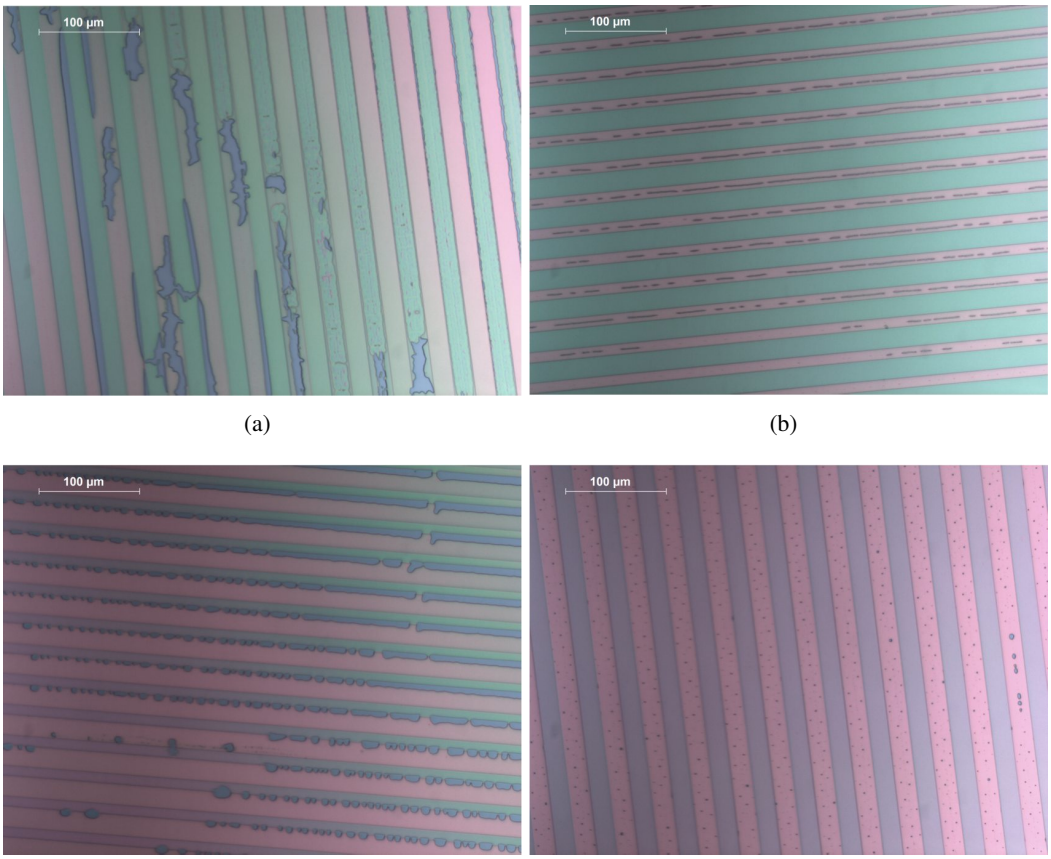
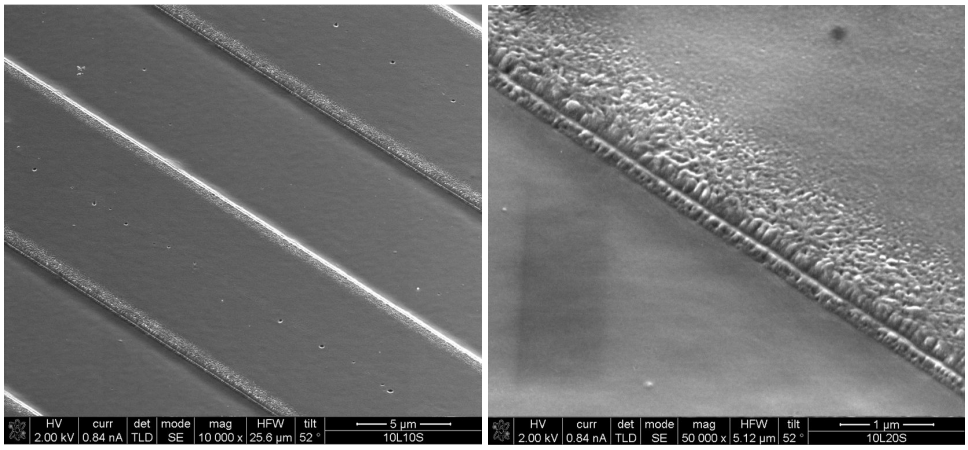


Figure 3.8: Optical microscope pictures of defect modes in the imprinted P(VDF-TrFE): (a) polymer peeled away from the substrate (b) polymer in the edge of the grating area peeled off from the substrate (c) incomplete fill with voids located in the middle of the thick area (d) incomplete fill with voids are scattered in the thick area.

cannot be present.

More detailed images taken by SEM are shown in Figure 3.9. Due to the different effects such as adhesion at the surface, friction comes from surface roughness, trapping of the polymer caused by the negative slopes of the cavity sidewalls, distortion or damage of the patterned structure during demoulding can occur. Though the anti-adhesive treatment can solve the adhesion problem and reduce the frictional forces, it cannot remove the strain induced by shrinkage, which results in local variation of lateral forces between stamp and polymer. In our case, the lateral forces during the demoulding process causes the edge of the hill for our imprinted P(VDF-TrFE) to be relatively rough, as shown in Figure 3.9.



(a) (b)

Figure 3.9: SEM images of imprinted P(VDF-TrFE)

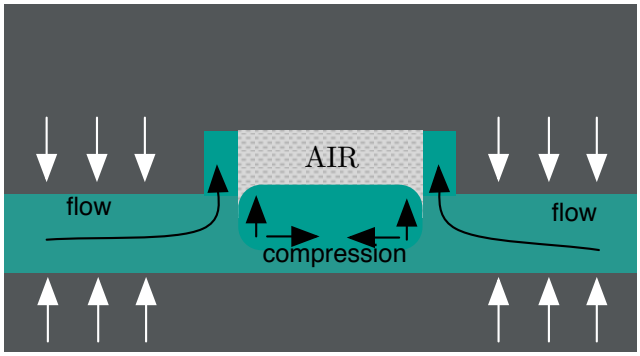
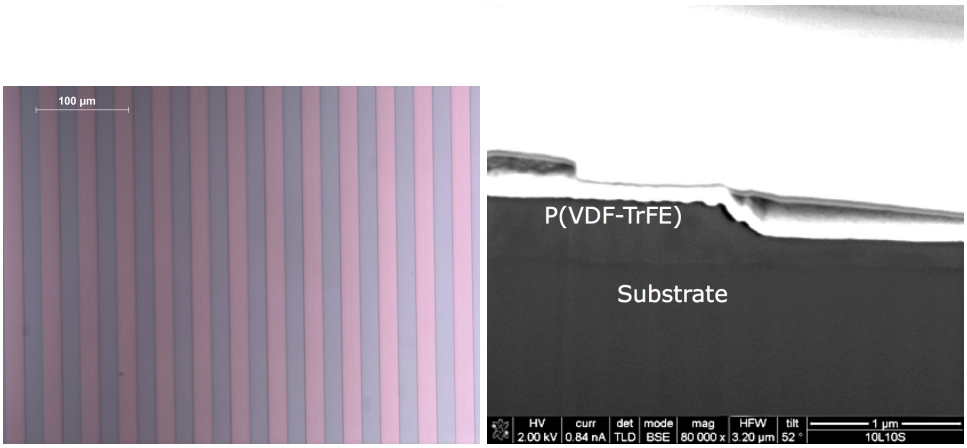


Figure 3.10: Typical polymer behavior during imprinting [24]

3.4 Discussion

As a matter of fact, the capillary action, the surface tension, the elastic nature of the polymers, the local shear in the polymer, as well as the distortion the stamp all have some impact on the imprinting quality. To understand the cause of the previously discussed imprinting defects and to find a way to eliminate them, it is important to understand the polymer behavior during the thermal imprinting process. A typical behavior of the polymer deformation during imprinting is shown in Figure 3.10 [24]. The stamp filling starts with the flowing of the polymer from the borders into the stamp cavity. The polymer expands through a nozzle and climbs up the cavity walls driven by both pressure and capillary force.

To remove the defects caused by the air trap, a system operating within the vacuum environment would be a good solution. To eliminate other defects, higher pressure, longer imprinting time, slower cooling rate, and so on, are preferred. Because P(VDF-TrFE) has a glass transition temperature of -40 °C, it is impractical to cool down the imprinting system



(a) (b)

Figure 3.11: (a) Optical microscope pictures, (b) cross-section SEM image of imprinted P(VDF-TrFE)

beneath this value for demoulding. Moreover, because of the different thermal expansion coefficients for stamp and polymer, the lower the demoulding temperature, the more stress will be introduced on the edge of the imprinted pattern, thus a less good replication will be made. After extensive testing, the optimized imprinting parameters for P(VDF-TrFE) are:

- Imprinting at 135 °C for one hour using an imprint pressure near 37 kbar (3 ton on 4-inch wafer)
- Heating rate of 2.3 °C/min. cooling rate of 2.3 °C/min.
- Demoulding temperature of 65 °C.

After setting the imprinting parameters as above, a nice defined imprinted P(VDF-TrFE) pattern can be obtained, as can be seen in Figure 3.11. In the SEM image, it is observed that the sidewalls of the structured P(VDF-TrFE) is not fully straight; this is due to the slightly skewed sidewall of the protrusion patterns on the stamp.

3.5 Conclusion

Retrieving high-fidelity imprint patterns without damage relies on a well controlled balance of forces at the interfaces between stamp, substrate, and imprinted polymer film. After extensive testing, well replicated patterns in ferroelectric P(VDF-TrFE) film has been fabricated.

Chapter 4

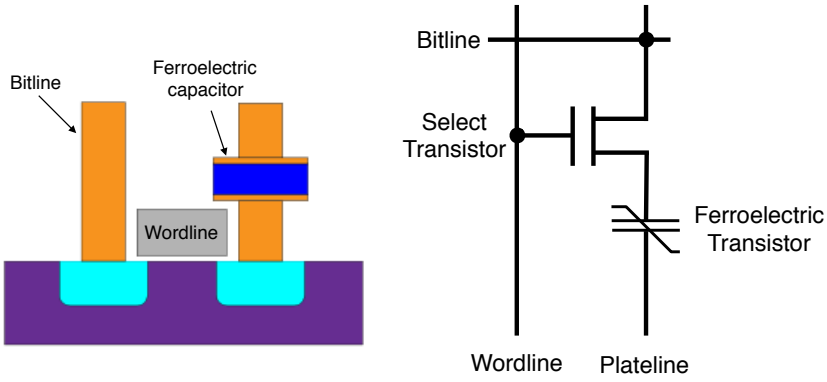
Multi-bit ferroelectric capacitors

In this chapter, a spatially modulated structure is fabricated using a thermal imprinting process of P(VDF-TrFE), which is versatile and scalable and has direct applications in the realization of multi-level ferroelectric capacitor cells for next-generation flexible electronics.

4.1 Background

The ferroelectric capacitor is one of the simplest types of ferroelectric memory devices. Information is stored in the capacitor by aligning the direction of the internal polarization with an applied electrical field. The details of the writing process for both imprinted and non-imprinted capacitors were previously explained in Chapter 2. To read the data from a ferroelectric capacitor, a switching voltage is employed. During this process, a low or a high charge displacement current response can be obtained depending on whether or not the polarization was aligned with the direction of the applied field. If the directions of the internal polarization and the applied field are not the same, the reading process destroys the polarization state and the stored information is lost due to the destructive read-out. Therefore, a reset voltage needs to be applied afterwards while the polarization direction was changed during the read operation.

When combined with a transistor, a ferroelectric capacitor can be used to construct a ferroelectric random-access memory (FeRAM), as seen in Figure 4.1. This FeRAM was first proposed in 1952 [12]. Besides the 1T1C (T-transistor, C-capacitor) structure, other structures such as 1T2C [59] or 2T2C [33] has also been developed. The simplest 1T1C FeRAM cell is similar to a DRAM cell with the exception of the plateline, which has a variable voltage level in order to enable the switching of the polarization of the ferroelectric capacitor, whereas the voltage level is fixed in the DRAM. As one of the alternative non-volatile memory technologies, FeRAM offers the same functionality as a flash memory. Moreover, compared with flash memory, FeRAM has lower power usage, faster write performance and a much higher maximum number of write-erase cycles.



(a) Configuration (b) Schematic circuit diagram

Figure 4.1: 1T1C FeRAM cell

4.2 Experimental

4.2.1 Device fabrication

Imprinted- and reference capacitors were fabricated on 4-inch Si substrates covered with a 2 µm SU8 planar photoresist or 2 µm SiO_2. On these substrates, gold bottom electrodes (30 nm) were first patterned by photolithography. P(VDF-TrFE) films were prepared by spin coating a filtered 6 or 8 wt. % solution of P(VDF-TrFE) in cyclohexanone or cyclopentanone at a speed of 2000 rpm for 60 seconds onto UV-ozone cleaned capacitor substrates. Finally, 100 nm gold top electrodes were evaporated through a shadow mask resulting in capacitor surface areas in the range of 0.0589 to 1.3676 mm^2. The process is explained in Figure 4.2 and Figure 4.3 shows a top-view of fabricated device cells.

4.2.2 Characterization methods

The P(VDF-TrFE) layer thickness was determined by using a Dektak profilometer. The characterization of D-V hysteresis loops for capacitors were done with a TF Analyzer 2000 system in FE-Module combined with a voltage amplifier.

4.3 Results and discussion

4.3.1 Ferroelectric properties of non-imprinted ferroelectric capacitors

Non-imprinted capacitors were first characterized to be used for reference. Figure 4.4 shows typical D-V hysteresis loops for the reference capacitor with 410 nm thick P(VDF-TrFE) layers. As can be seen from the D-V curves, at low voltages, the ferroelectric polarization is not strongly affected and there is no obvious hysteresis loop. The ferroelectric starts to polarize when the hysteresis amplitude is close to the coercive voltage, and it saturates at

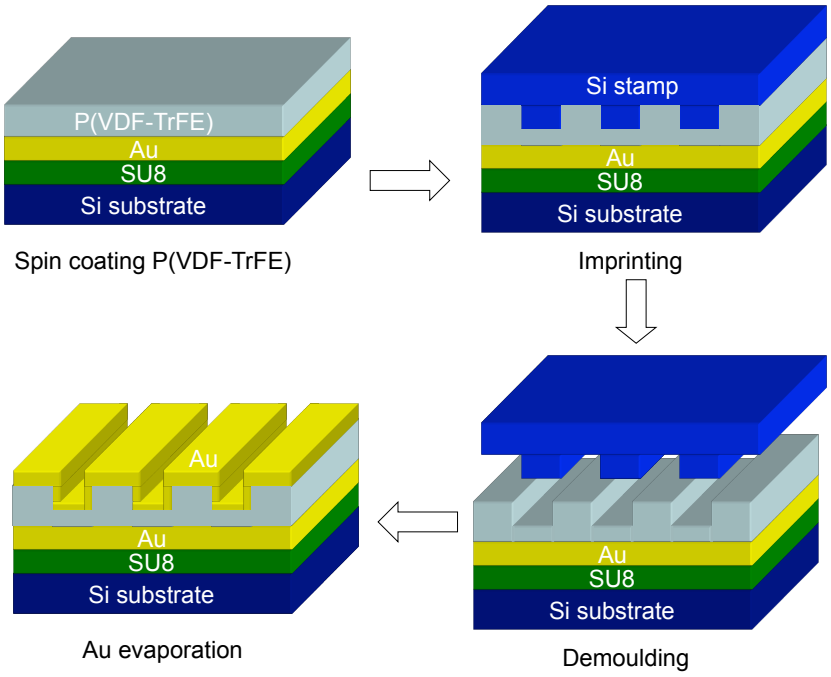


Figure 4.2: Fabrication steps of the imprinted capacitor

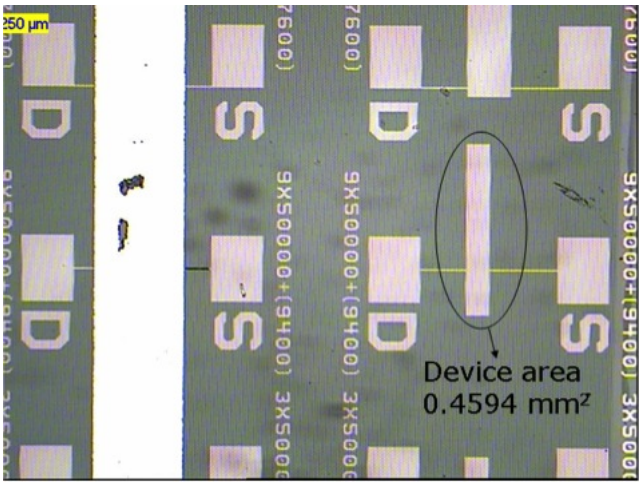


Figure 4.3: Optical microscope pictures of capacitors after top electrode evaporation (left) and before top electrode evaporation (right). Areas tagged *S* and *D* were the bottom electrode. The sizes of the active areas were 1.3676 mm^2, 0.4594 mm^2, 0.1584 mm^2, and 0.0589 mm^2.

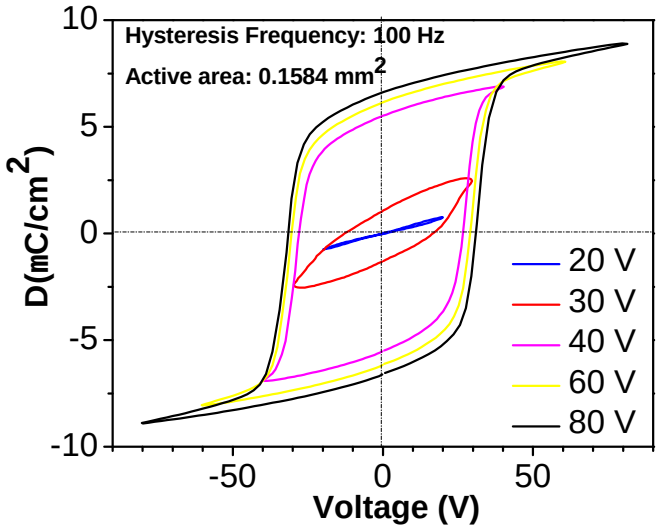


Figure 4.4: Hysteresis loop of non-imprinted capacitor with P(VDF-TrFE) of 410 nm

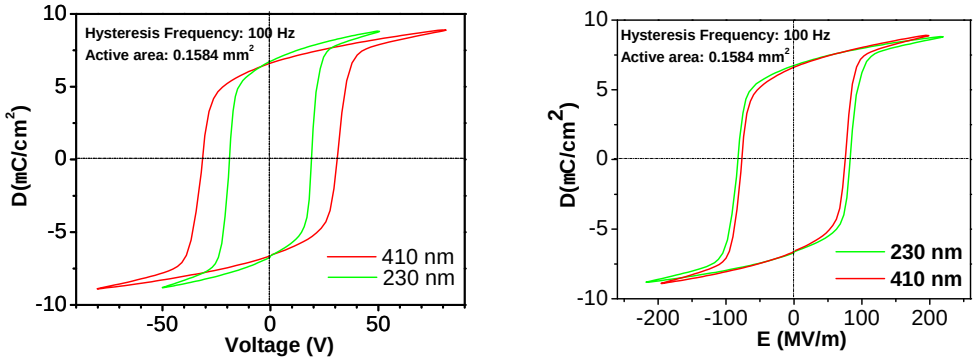
high voltages because all the dipoles have been aligned into one direction leading to the maximum achievable amount of polarization inside the material.

A comparison of ferroelectric capacitors with two different P(VDF-TrFE) layer thicknesses at saturated polarization states is illustrated in Figure 4.5. The D-V characteristics show that two capacitors have almost the same remanent polarization, but different coercive voltages. By converting D-V to D-E characteristics, the hysteresis loops for different layer thickness are almost identical, which confirms that the ferroelectric coercive voltage is a thickness dependent parameter. On the other hand, the ferroelectric properties such as the remanent polarization and coercive field of P(VDF-TrFE) is independent of layer thickness at the range of hundreds of nanometers [39]. For the P(VDF-TrFE) films without the imprinting process, the remanent polarization and coercive field are around 6.3 $\mu C/cm^2$ and 75 MV/m as measured.

For non-imprinted P(VDF-TrFE) capacitors, the minimum polarization voltage corresponds to the peaks in dD/dV-V graph, as can be seen in Figure 4.6. In practice, it was found that the non-imprinted P(VDF-TrFE) capacitors are safe when the electrical field is below three times the coercive field, which is around 75 MV/m. In other words, capacitors with layer thicknesses of 230 and 410 nm will be damaged when the hysteresis amplitude is 60 and 90 V, respectively.

4.3.2 Ferroelectric properties of imprinted ferroelectric capacitors

As explained in Chapter 2, the multi-bit memory function requires a spatially modulated P(VDF-TrFE). The D-V hysteresis loop of an imprinted P(VDF-TrFE) capacitor is shown in Figure 4.7. The remanent polarization is 7.4 $\mu C/cm^2$ at a hysteresis amplitude of 70 V.



(a) (b)

Figure 4.5: D-V characteristics and D-E characteristics of non-imprinted capacitors with P(VDF-TrFE) of 410 nm and 230 nm

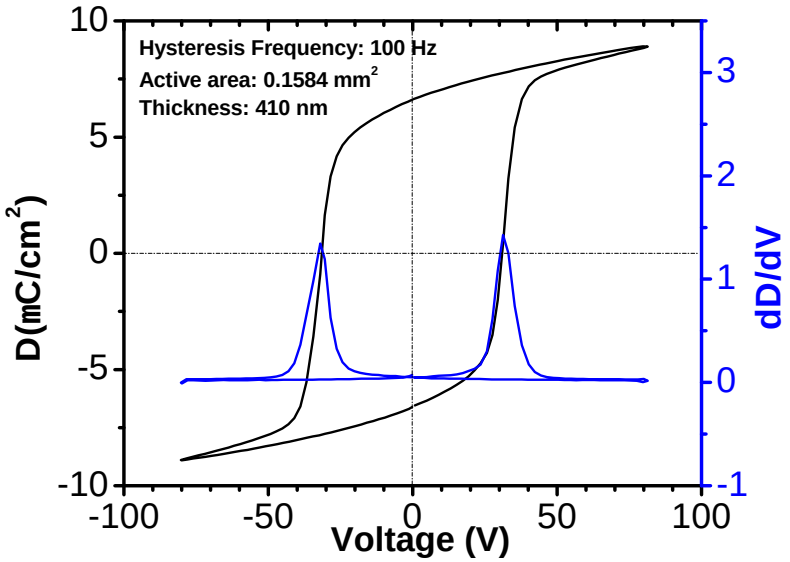
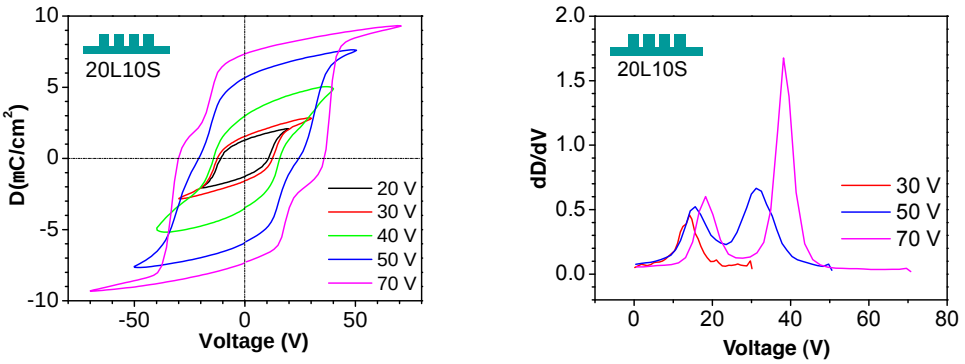


Figure 4.6: D-V and dD/dV-V characteristics of a non-imprinted capacitor with P(VDF-TrFE) thickness of 410 nm



(a) (b)

Figure 4.7: (a) D-V and (b) dD/dV-V characteristics of an imprinted capacitor measured with hysteresis frequency at 100 Hz, the active area is 0.1584 mm^2

When the ferroelectric film with two thickness levels is sandwiched between two conducting electrodes and a voltage is applied to the top and bottom electrode, the electric field inside the ferroelectric material varies with the thickness. Thus, it is required of a higher voltage to switch the thicker regions of the memory cell compared to the thinner regions. Hence, depending on the voltage and the duration of a read pulse, different regions of the ferroelectric film can be switched with parallel or opposite surface polarization. To obtain clearly separated peaks in the imprinted capacitor, it is very important to define the read and write voltage for multiple states; a proper combination of initial film thickness and imprinting stamp is the key to achieve this target.

Figure 4.7 shows the characterization of an imprinted ferroelectric capacitor, which has an initial P(VDF-TrFE) layer thickness of 370 nm and is imprinted using a stamp with a protrusion height of 270 nm. Clearly the slope of the D-V curve is different from previous figures. With a hysteresis amplitude up to 30 V, there is only one peak observed in the dD/dV-V curve, hence 30 V is sufficient to activate the thin P(VDF-TrFE) layer while not influencing the thick layer. When the voltage is increased to 50 V, a second peak appears. By further increasing the voltage, the peaks become more separated as shown in Figure 4.7 (b). Normally, for layer thickness around 200 nm, 70 V will cause a breakdown in the device. An interesting observation for the imprinted capacitor is that the device is quite stable with the hysteresis amplitude of 70 V, which normally for a device with one thin film around 200 nm has already been broken down.

The properties of imprinted P(VDF-TrFE) capacitors with different horizontal dimensions were also investigated. dD/dV-V characteristics of those capacitors are shown in Figure 4.8. Clearly, the performance of these capacitors vary with the dimensions. The remanent polarization values of different patterns are in the range of 6.5–7.4 μC/cm^2 with a hysteresis amplitude of 70 V. Devices with a line: 10 μm / space: 10 μm pattern and a line: 20 μm / space: 20 μm pattern are almost identical, due to the similar height distribution by patterning with same horizontal ratio between the thin and the thick layers. By using a

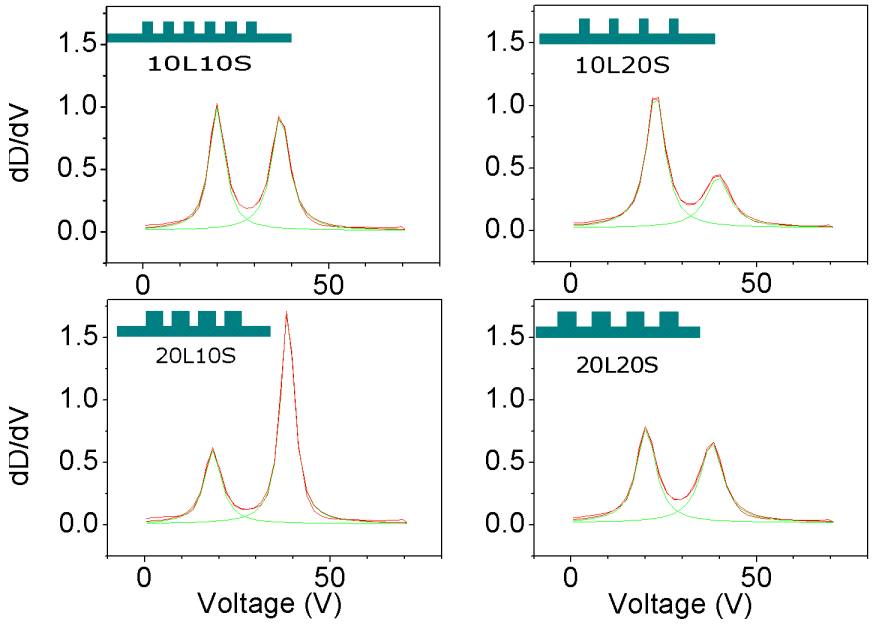


Figure 4.8: dD/dV-V characteristics of imprinted ferroelectric capacitors with four different horizontal dimensions. Devices were measured with hysteresis frequency at 100 Hz, and the active area is 0.1584 mm^2.

Horizontal Dimensions	Film Thickness	Peak Center	Peak FWHM
Line: 10 µm	227 nm	19.9 V	5.0 V
Space: 10 µm	531 nm	37.0 V	5.9 V
Line: 10 µm	286 nm	22.8 V	5.9 V
Space: 20 µm	561 nm	39.5 V	7.9 V
Line: 20 µm	187 nm	18.4 V	5.6 V
Space: 10 µm	466 nm	38.4 V	4.4 V
Line: 20 µm	239 nm	20.2 V	6.3 V
Space: 20 µm	512 nm	37.8 V	7.4 V

Table 4.1: Data derived from multi-peak fitting of the curves in Figure 4.8

multi-peak Lorenz fitting, it is possible to determine the critical voltage points for starting the polarization in different layers, the results of which are shown in Table 4.1.

For example, for the capacitor with the grating pattern of line: 20 µm / space: 10 µm, the peaks appear at 18.4 and 38.4 V, are corresponding to the layer with the thickness of 187 and 466 nm, respectively. In practice, it is always preferred to have less operation voltage and more specific control of each layer. According to Figure 4.8, this pattern is the most

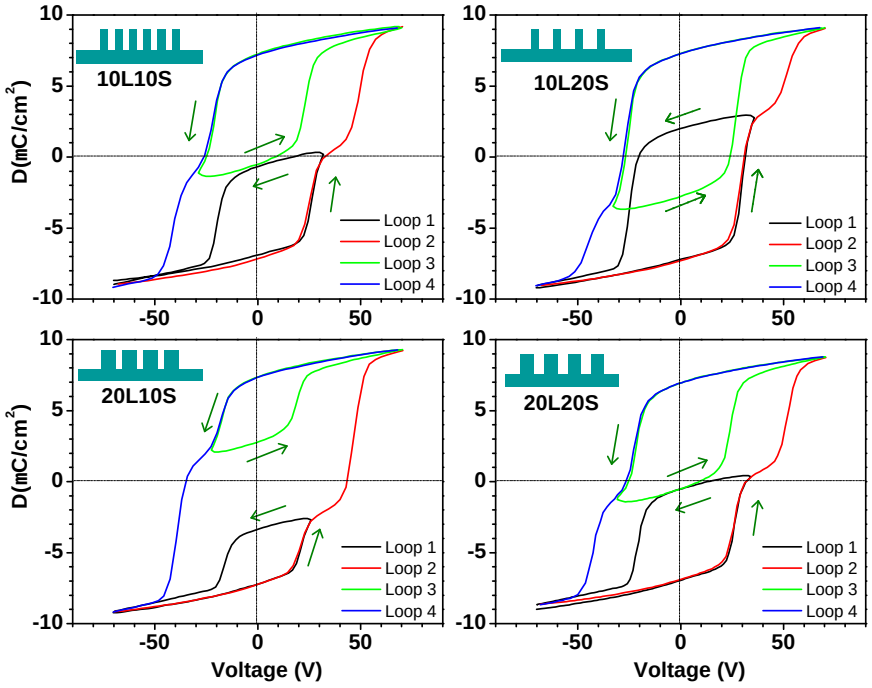


Figure 4.9: Hysteresis sub-loops imprinted capacitors with four different horizontal dimensions. The arrows indicate the sweeping directions.

distinguished peaks with lowest operation voltage.

Since the value of coercive field in the polymer film can be derived from $E = V/d$, where V is the coercive voltage and d is the layer thickness, the voltage can obtained from the center of the dD/dV peaks. The calculated E_c is 71 MV/m for the imprinted capacitor. For non-imprinted capacitors, the E_c value is around 75 MV/m; the similarity indicates that the imprinting does not make any device at the range of hundreds of nanometers.

4.3.3 Hysteresis sub-loops of imprinted ferroelectric capacitors

Figure 4.9 shows hysteresis sub-loops of a series of memories that were imprinted with different patterns. The line/space pattern is indicated in the inset of the corresponding figure. If high negative voltages are applied, the polarization of the thin and thick film regions will be parallel and the net remanent charge in this state will be equal to that of a device with a planar P(VDF-TrFE) film, i.e. $\sim$75 μC/m^2. We refer to this state as bit "11". As we gradually swept the voltage from -70 to 30 V, the electric field in the thinner region will reach the coercive field where the ferroelectric polarization switches. Now, the thick and thin regions will have surface polarization of opposite signs (bit state "10"). When the

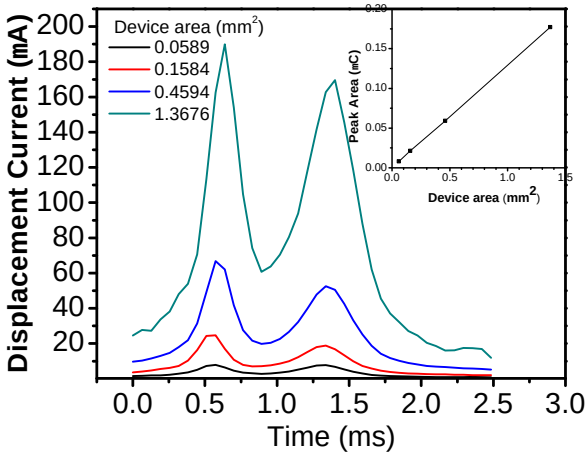


Figure 4.10: Displacement current vs. voltage for imprinted capacitors with different device sizes.

voltage is increased further, the electric field in the thicker regions also reaches the coercive field and also this region switches (bit state ”00”). If however we swept back to -30 V, then only the thinner region has switched, and the polarization direction of the thinner and thicker region are opposite (bit state ”01”). This shows that by applying the correct voltages, it is possible to program the memories into four different states.

When the polarization of the two regions were in the same direction, a remanent polarization P_r of 75 µC/m^2 was measured, irrespective of the imprint pattern. The remanent charge of the ”01” and ”10” state is about 0 C/cm^2 for the devices imprinted with line: 10 µm / space:10 µm and line : 20 µm / space: 20 µm. The remanent charge of the ”01” and ”10” state of the line : 10 µm / space : 20 µm and line : 20 µm / space:10 µm was $\pm$2.5 µC/m^2, in close agreement with the expected value. This implies that also in case of opposite surface polarity, the polarization charges are compensated very effectively by the metal electrode charges, and no significant lateral charge compensation in the ferroelectric occurs.

4.3.4 Area scaling of imprinted ferroelectric capacitors

In principle, the smaller the capacitor area, the smaller the readout signal (total displacement charge) will be. This would be a problem if we scale down the device area so much that the signal becomes too small to be detected. Also, with area downscaling, the device will be more sensitive to parasitic capacitances, which always cause a large linear polarization. In Figure 4.10, the displacement current vs. voltage was read from the measurement setup, the inset graph of the total charge vs device sizes illustrated that the read out signal is proportional to the device size.

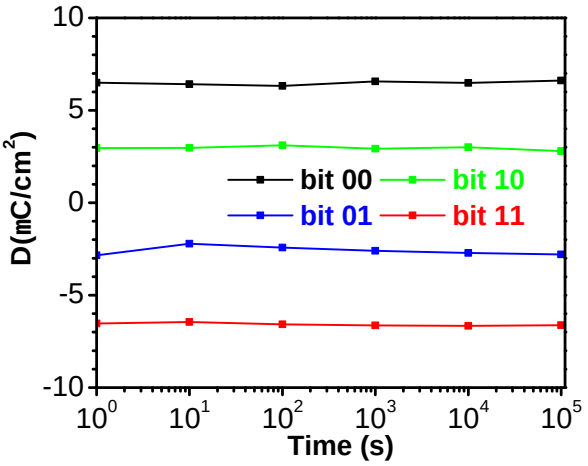


Figure 4.11: Data retention characteristics of the four bit states of a capacitor with line: 20 µm / space: 10 µm, measured with hysteresis frequency at 100 Hz. The active area is 0.1584 mm^2.

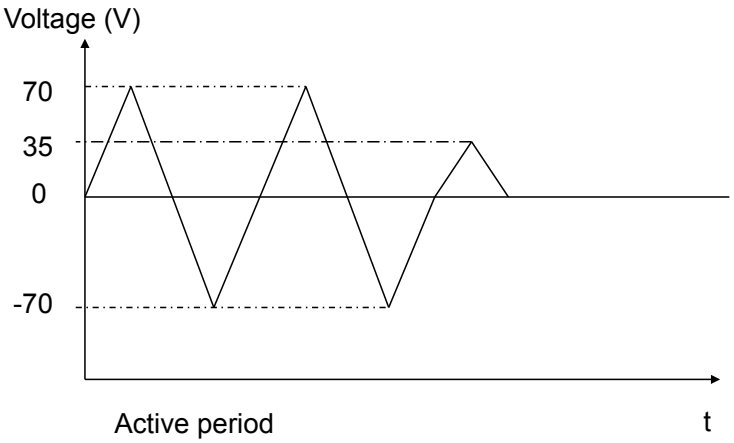


Figure 4.12: Pulse train used for retention test of bit state ”10”

4.3.5 Retention performance

Figure 4.11 shows the data retention characteristics of a imprinted capacitor with horizontal dimensions of line: 20 µm / space: 10µm. It measured the remanent switching current at a given time after it was programmed. In the pulse train that was used, the first two full loops from $+70$ to -70 V are required to assure that the initial polarization in the film is not random. Subsequently a pulse to 35 V is given to program the memory into the ”10” state. After 10 s, 100 s, 1000 s etc. a read pulse determines the polarization that is left. After 10^5 s, the loss of ferroelectric polarization is limited to around 90% of the initial value for all

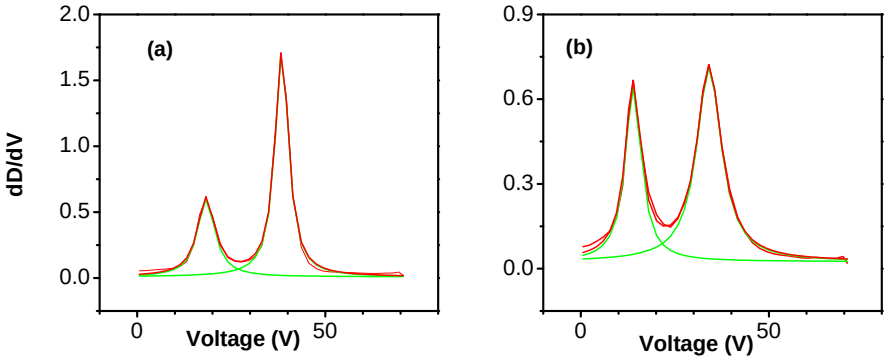


Figure 4.13: Comparison of dD/dV-V characteristics for imprinted capacitors with a pattern line: 20 µm / space: 10 µm, the imprinting stamp protrusion height is 270 nm (a) the initial P(VDF-TrFE) layer thickness of 370 nm; and (b) the initial P(VDF-TrFE) layer thickness of 410 nm.

bit states. Polarization loss of the ”01” and ”10” states was found to be similar to that of the ”11” and ”00” states. The hysteresis loop did not show a substantial difference after the retention test.

4.3.6 Discussion: Memory window for multi-bit ferroelectric capacitors

As mentioned in the previous section, to obtain four separate states in the imprinted capacitors, it is very important to define the read and write operation voltage. A proper combination of initial film thickness and protrusions of the imprinting stamp is the key to achieve this target.

For example, while the stamp protrusions height is 270 nm, and the P(VDF-TrFE) film has an initial thickness of 410 nm instead of 370 nm, the dD/dV-V characteristics of the capacitor exhibit obvious multiple peaks (Figure 4.13 (b)), same as the capacitor discussed in the previous section (Figure 4.13 (a)). However, the FWHM values for the peaks under some operate voltages are smaller in the previous capacitor, which means simpler observations of multiple data recordings.

By keeping the initial P(VDF-TrFE) layer thickness of 410 nm, and performing the thermal imprinting with a stamp with 140 nm protrusions, for the capacitor with horizontal dimension of line: 20 µm / space: 10 µm, this results in a thicknesses of 310 and 440 nm. In the dD/dV-V characteristics displayed in Figure 4.14, two peaks corresponding to the thin and thick layer (310 nm and 440 nm) can be observed. However, those peaks can hardly be distinguished from each other. This implies that by using this combination of initial film thickness and imprinting stamp, it is not possible to discriminate between the four different logic states.

		Film Thickness	Peak voltage	FWHM
Initial Layer Thickness $D = 370$ nm	Thin Layer	187 nm	18.35 V	5.59 V
Stamp Height $h = 270$ nm	Thick Layer	466 nm	38.44 V	4.35 V
Initial Layer Thickness $D = 410$ nm	Thin Layer	200 nm	13.94 V	5.20 V
Stamp Height $h = 270$ nm	Thick Layer	480 nm	34.09 V	7.95 V

Table 4.2: Data derived from multi-peak fitting for the curves in Figure 4.13

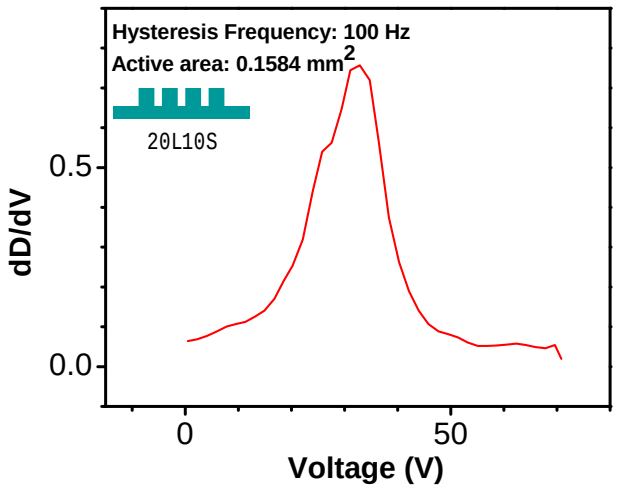


Figure 4.14: dD/dV-V characteristics of the imprinted capacitor with the pattern line: 20 µm / space: 10 µm, a initial P(VDF-TrFE) layer thickness of 410 nm, and stamp protrusion height is 140 nm, the active area of the device is 1.3676 mm^2, the device is measured at a hysteresis frequency of 100 Hz.

4.4 Conclusion

In this chapter, multi-bit capacitors with good retention performance have been fabricated by employing imprinting lithography. Discrimination between the four different logic states can be achieved by carefully choosing the film thickness and the imprinting pattern.

Chapter 5

Multi-bit Ferroelectric Transistors

In this chapter, non-imprinted and imprinted FeFETs based on polymeric semiconductor Gallium Indium Zinc Oxide with memory functionality are assessed. In particular, by employing thermal imprinting technology for patterning grating structures in ferroelectric P(VDF-TrFE) layers, multi-bit functionality can be achieved in FeFETs.

5.1 Background

5.1.1 State of the Art

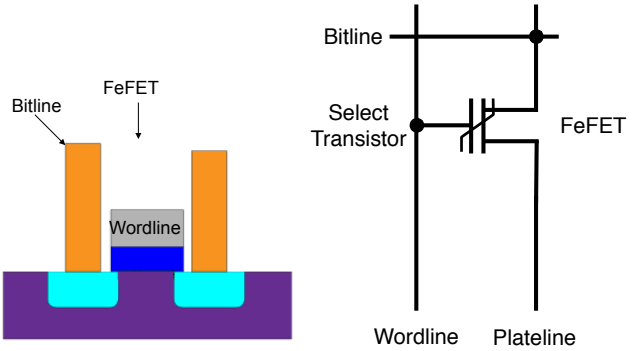
Ferroelectric field effect transistors (FeFETs) are attractive memory devices due to their non-volatile data retention, small size, rewriteability, non-destructive read-out, low-voltage operation and short programming time [7]. FeFETs were first published in 1957, after which great efforts has been made to develop the devices. A key advantage of FeFET is that charge accumulation in the channel helps the device to stabilize the polarization state. Along with the commercialization of inorganic FeFETs devices for decades [48], organic FeFETs based on polymers drew a lot of attention due to adequate materials and the ability to fabricate on flexible substrates. After many years of improvement, memory based on ferroelectric polymers is coming to an advanced stage of development.

Though the fabrication process of a FeFET is much more complex than that of a capacitor, FeFETs tackle the intrinsic problems that exist in the capacitors: the scaling behavior and the destructive read-out. In ferroelectric capacitors, the read-out current is proportional to the device area and the remanent polarization, seen in (5.1). Generally speaking, an area reduction would reduce the current. With the device area continuing to scale down, at a critical point, the signal will be too small to be detected.

$$I \propto \frac{P_r A}{t_{sw}}. \tag{5.1}$$

In contrast, in FeFETs, the readout current I_D scale with the ratio of W to L, where W and L are the channel width and length, respectively, as can be seen in (5.2).

$$I \propto \frac{W}{L} \mu V_D. \tag{5.2}$$



(a) Configuration (b) Schematic circuit diagram

Figure 5.1: A FeFET cell

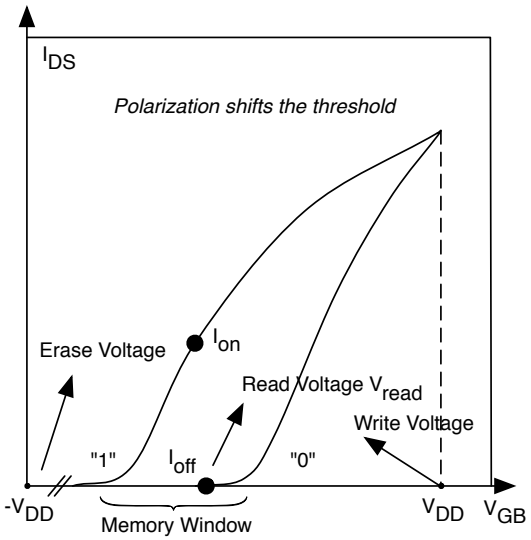


Figure 5.2: The current characteristics of a FeFET [14].

so if L and W are reduced by the same factor, the read-out signal is unaffected by scaling.

Operation Principle

A FeFET is basically a MOSFET (Metal Oxide Semiconductor FET) with a ferroelectric insulator used as a gate dielectric. Since applying a gate voltage can polarize the ferroelectric insulator, it gives rise to the memory functionality due to the attenuation of the charge carrier density in the semiconductor channel. The operating principle of a FeFET can be described, referring to Figure 5.2 in which an n-type semiconductor is used, as follows; when a positive gate voltage V_G is applied, the mobile electrons in the semiconductor accumulate at the interface, resulting in a high current response with the application of a small

drain voltage V_D. Thus the transistor is in the ON state. If a negative V_G is applied, the accumulated charges are depleted and the transistor returns to the OFF state, at which point the drain current I_D is very small. The difference between FET and FeFET lies in whether or not I_D has a hysteresis loop. For a FET without ferroelectric effect, the transistor returns from ON state to OFF state without I_D hysteresis. In contrast, the FeFET returns to an OFF state with a large hysteresis, which arises from the attenuation of the mobile charge concentrations in the semiconductor by the ferroelectric polarization of the gate ferroelectric insulator. Therefore, the memory effect of FeFETs is realized by associating ON and OFF states with the binary "1" and "0" states, respectively. In order to write "1", a positive V_G is needed to turn on the transistor, and to overwrite "0" with "1", a negative V_G has to be applied in order to turn off the transistor. To read the current response, just a V_D can be used. Without applying V_G, the polarization in ferroelectric material will not change. Thus, a FeFET is a nonvolatile memory combined with non-destructive read-out functionality.

Due to the complexity of writing and reading process for the imprinting FeFETs, the operation will be explained together with the device performance in results and discussions in Section 5.3.

5.2 Experimental

5.2.1 Device Fabrication

Imprinted and reference transistors were fabricated on 4-inch highly doped Si substrates with 500 nm SiO_2 and 30 nm gold source and drain were evaporated through a shadow mask on top. A 50 nm amorphous Gallium Indium Zinc Oxide (a-GIZO) (3% O_2) layer was then sputtered on the substrate. The carrier concentration of a-GIZO thin film varies with different process conditions and post treatments, and this thin film can act as a conductor, a semiconductor, or an insulator. In order to use the semiconductor properties of a-GIZO, FETs were annealed in air at 420 °C for 40 minutes before applying the ferroelectric polymer. P(VDF-TrFE) films were prepared by spin coating a filtered 8 wt. % solution of P(VDF-TrFE) in cyclopentanone at a speed of 2000 rpm for 60 seconds onto FET substrates. After the imprinting process, 100 nm gold top electrodes were evaporated through a shadow mask resulting in capacitor surface areas. The architecture of the imprinted transistor is shown in Figure 5.3.

5.2.2 Characterization methods

Atomic force microscopy (AFM) measurements were performed with a Veeco Dimension 3100 SPM, using a Si probe in tapping mode. The measurements of P(VDF-TrFE) layer thickness were performed by using a Dektak profilemeter. The I_D-V_G transfer curves were measured at room temperature in the dark and in N_2 atmosphere by using a probe station connected to semiconductor parameter analyzer (Agilent 5155B).

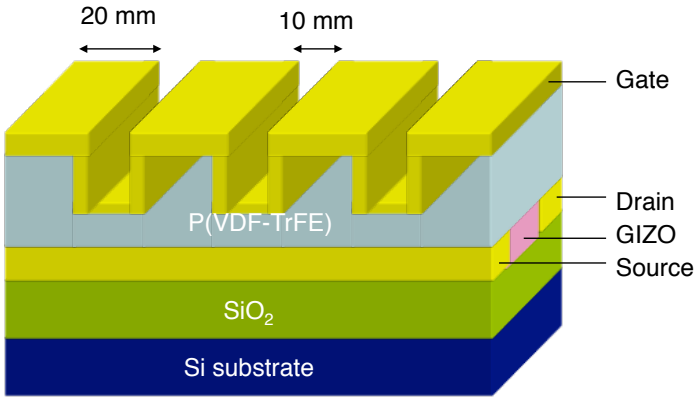
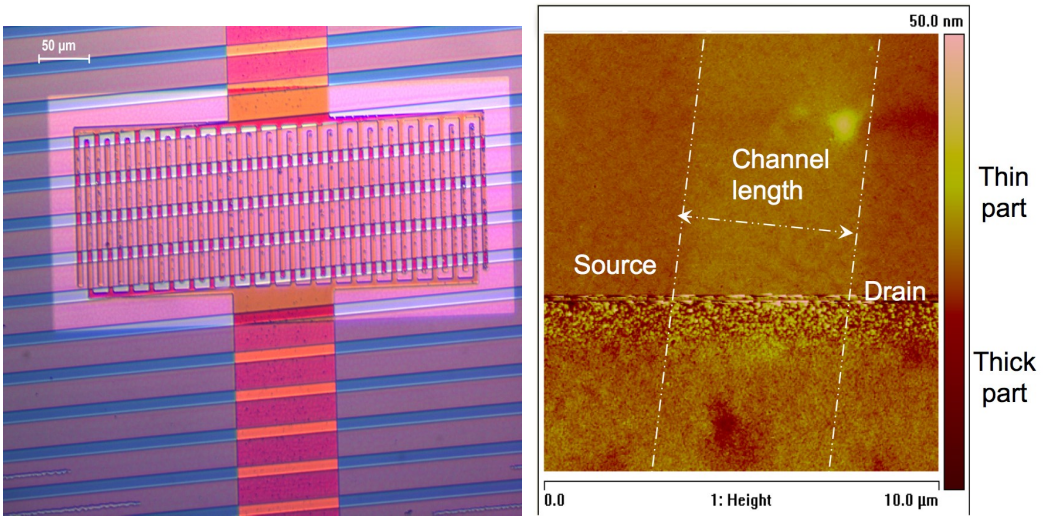


Figure 5.3: Schematic cross section of a transistor



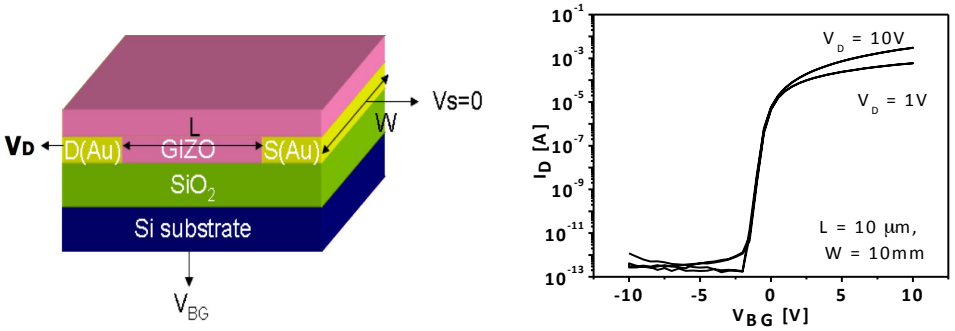
(a) Optical microscope image (b) AFM image

Figure 5.4: Imprinted P(VDF-TrFe) on top to GIZO FET, where $L = 5$ µm, and $W = 5$ mm. The RMS value of the thin layer is 2.1 nm, and the layer thickness is 2.4 nm.

5.3 Results and Discussion

5.3.1 Morphology of imprinted transistors

In Chapter 4, it was proved that multi-bit capacitors with a grating structure line: 20 µm / space: 10 µm show the best memory performance. Thus, the work in this chapter focuses on ferroelectric transistors using P(VDF-TrFE) with the same imprinting pattern.



(a) (b)

Figure 5.5: (a) schematic of bottom contact FETs, with SiO_2 as the gate insulator, and Si substrate as the gate. (b) I_D-V_{BG} transfer curves for an a-GIZO FET.

5.3.2 Characterization of a-GIZO FETs and non-imprinted FeFETs

The field-effect properties of n type a-GIZO were first characterized in bottom contact FET. Transfer curves are shown in Figure 5.5. In FETs, the drain current follows the equations:

$$(I_D)_{lin} = \frac{W}{L}\mu(V_G - V_{th} - \frac{V_D}{2})V_D, \tag{5.3}$$

and

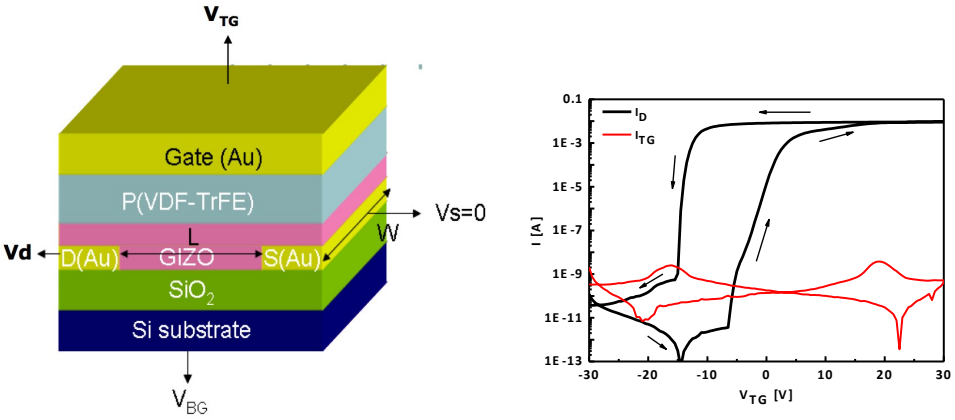
$$(I_D)_{sat} = \frac{W}{2L}\mu C_i(V_G - V_{th})^2, \tag{5.4}$$

where C_i is the capacitance of the dielectric material and V_{th} is the threshold voltage defined as the voltage necessary to induce mobile charges, at which the square root of the saturation I_D begins to increase substantially. It is clear that the transfer curves of the a-GIZO FET are identical for V_G sweeping from -10 to 10 V and from 10 to -10 V.

In contrast, FeFETs using P(VDF-TrFE) show a typical hysteresis property obtained by the top gate measurement, see Figure 5.6. The counter-clockwise hysteresis in the drain current can be explained by polarization switching of the gate dielectric and its influence on the channel charge. The maximum ON/OFF ratio I_{ON}/I_{OFF} = 10^6 is at $V_{TG} = -5$ V. The I_{ON}/I_{OFF} ratio should preferably be high. This value is among the highest reported values for FeFETs and results from high field-effect mobility in the channel in the ON state and (close to) full depletion of the channel area in the OFF state. The memory window of this transfer curve is about 15 V.

5.3.3 Characterization of imprinted a-GIZO FeFETs

Figure 5.7 shows typical transfer characteristics of an imprinted FeFET. Steep current variations as a result of polarization reversal occur at gate biases close to the values of the coercive voltages determined in the capacitors with corresponding P(VDF-TrFE) thicknesses.



(a) (b)

Figure 5.6: (a) The schematic of top contact FeFETs, with P(VDF-TrFE) as the gate insulator, and Au as the gate. (b) The I_D-V_{TG}, I_{TG}-V_{TG} curves for an a-GIZO FET. Device dimension is $L = 5$ µm, $W = 5$ mm. The arrows indicate the sweeping directions of V_G.

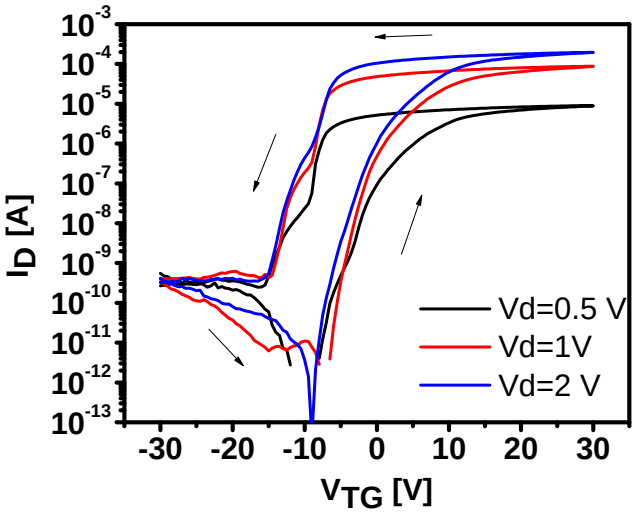


Figure 5.7: I_D-V_{TG} transfer curves for an a-GIZO FeFET with imprinted P(VDF-TrFE) film. Device dimensions: $L = 5$ µm, $W = 20$ mm. The arrows indicate the sweeping directions.

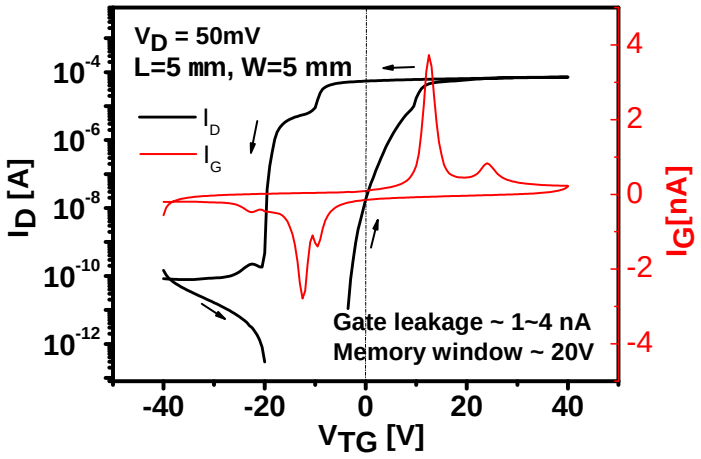


Figure 5.8: I_D vs V_{TG} and I_G vs V_{TG} transfer curves in an imprinted FeFET. The arrows indicate the sweeping directions.

This shows that like imprinted capacitors, these devices can achieve multi-bit functionality. Further evidence for this comes from the observation of four sharp, well-resolved switching peaks superimposed on the gate current when the thick or thin ferroelectric film regions switch their polarization state. These are plotted more clearly in Figure 5.8.

The peaks at ± 13 V and ± 25 V correspond to the polarization reversal in the thin and thick layer, respectively. The difference of the peak voltage between the capacitor and the transistor stems from slight differences in the P(VDF-TrFE) thickness. The initial P(VDF-TrFE) film thickness in the transistor is 320 nm, which after imprinting with Si stamp with 270 nm protrusions results in a thick layer of 430 nm and a thin layer of 150 nm. Values for the capacitor were 466 nm and 187 nm respectively.

5.3.4 I_G-V_{TG} sub-loops for imprinted FeFETs

I_G response of sub-loops operation, explained in Figure 5.9, is an example for data writing in an imprinted FeFET. For instance, V_G sweeping from -40 to 20 V is a process to write "10". Correspondingly, I_D-V_G transfer curves are shown in Figure 5.10. The drain current of four states "11", "01", "10", "00" are $(4 \sim 8) \times 10^{-8}$, 5×10^{-7}, 4.5×10^{-5}, $(2 \sim 3) \times 10^{-5}$A respectively.

From these results it is obvious that, with a good control of the operating voltage, the ferroelectric transistor can read and write multiple data.

5.3.5 Retention test

The retention test shows that it is possible to program the four individual states separately. It furthermore demonstrates the non-volatility of the four states. The slight variation in I_D with

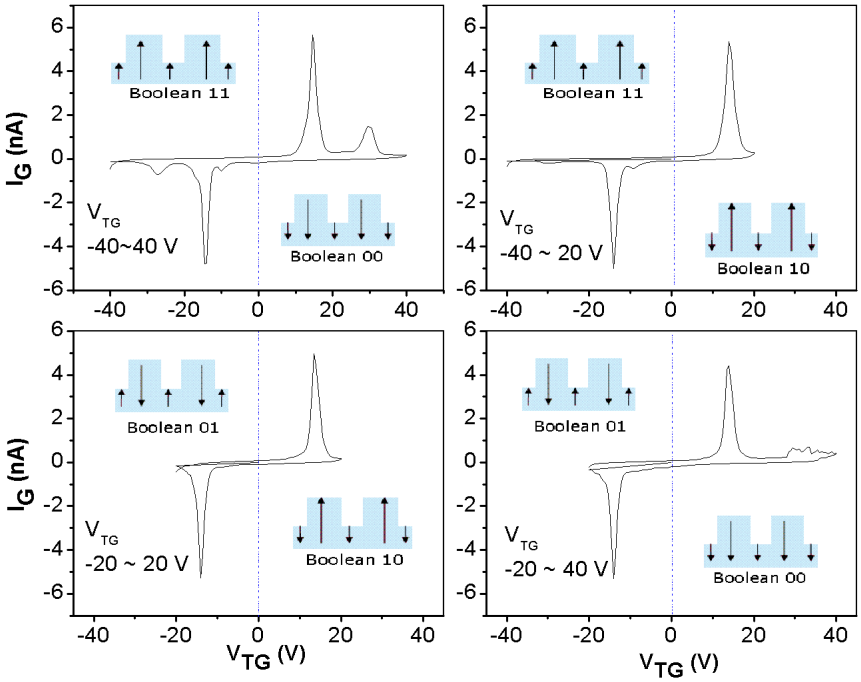


Figure 5.9: I_G-V_{TG} response of sub-loops operation in the imprinted FeFETs

time may be the result of ferroelectric depolarization and/or charge trapping in the device. This is a topic of further investigation. For this work, it is important to note that there is no difference between the data volatility of the four bits, and also that the measured data retention time (>10 000 s) is comparable to previous reported data retention times [23].

Theoretically, the use of a multi-level stamp can result in 2^n-bit storage per cell with n the number of levels of the stamp. There is however a limit to the minimum thickness variation below which switching of two regions of neighboring thickness becomes too difficult to detect individually. The shape of the hysteretic D-V polarization of the ferroelectric can be used as a first indication. Because of their square-like hysteretic polarization loops, P(VDF-TrFE) polymers have in this respect a clear advantage over ferroelectric ceramic materials that typically exhibit a more skewed hysteretic loop [48]. As long as the switching current peaks are well resolved, it should in principle be possible to fully program and read-out the logic content in ferroelectric capacitors and transistors. Of course, in a practical device the switching voltage of the thickest film region should not be higher than the breakdown voltage of the thinnest part.

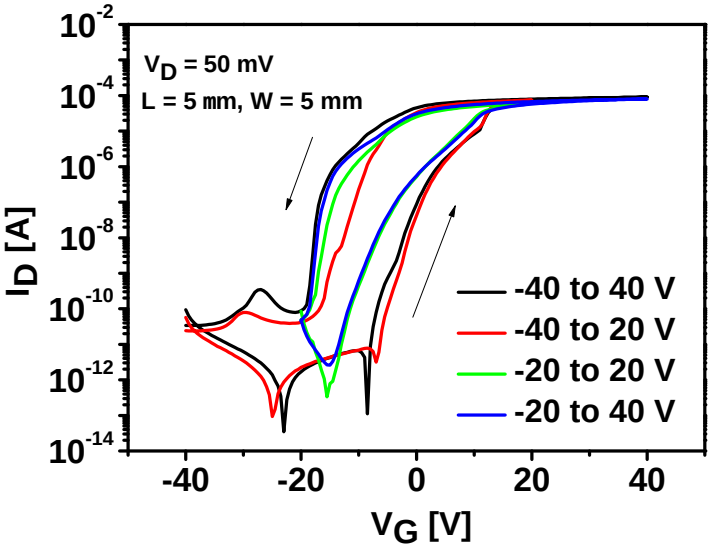
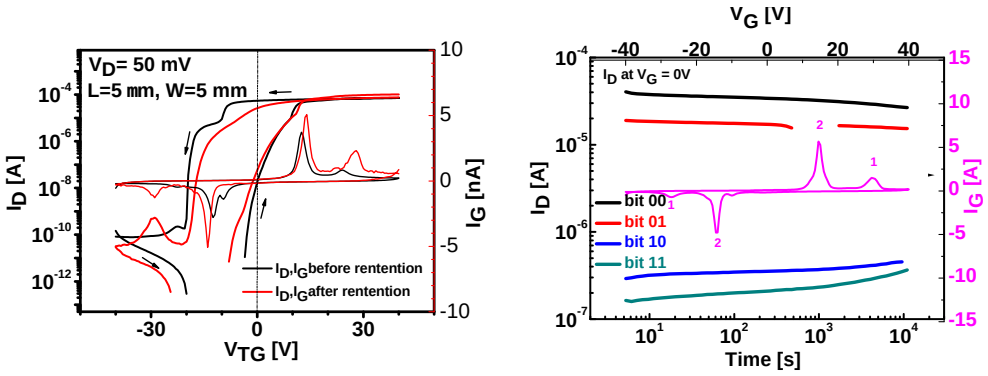


Figure 5.10: I_G-V_{TG} response of sub-loops operation in the imprinted FeFETs. The arrows indicate the sweeping directions.



(a) (b)

Figure 5.11: (a) Retention result of an imprinted FeFET after 10^4 s and (b) the comparison of memory of imprinted FeFET before and after the retention test

5.4 Conclusion

Multi-bit FeFETs have been successfully fabricated utilizing thermal imprinting lithography by patterning grating structure in P(VDF-TrFE) film. The FeFETs use P(VDF-TrFE) as the insulator and amorphous a-GIZO as the semiconductor. The fabricated devices show good data retention. It is shown that it is possible to program and read four states of information in a single memory cell. When using multi-level imprinted structures, it is possible to increase the maximum number of bits stored per memory cell even further.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

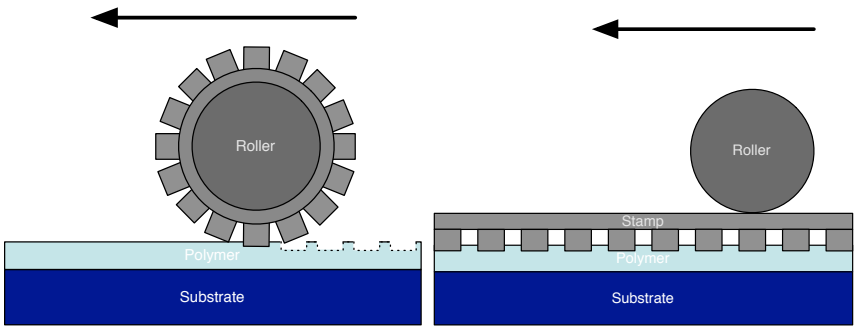
Successful pattern transfer of grating line/space features in P(VDF-TrFE) has been achieved by thermal imprinting lithography. Utilizing structured P(VDF-TrFE), multi-bit ferroelectric memory can be achieved in both capacitors and transistors.

In the first part of the thesis work, a good replication of P(VDF-TrFE) microstructures was done via a fine tuning of the imprinting conditions. It has been proved that thermal imprinting lithography is an effective way to pattern P(VDF-TrFE). Imprinting micro grating structures is helpful to produce a thin uniform P(VDF-TrFE) layer below 200 nm which is capable to be driven with a lower operation voltage.

Utilizing the imprinted ferroelectric P(VDF-TrFE) film, two non-volatile multi-bit memory devices were fabricated. The first application is ferroelectric capacitor. The performance of the capacitors indicated that a property combination of the initial P(VDF-TrFE) layer thickness and the protrusion height of the stamps are very critical for the multi-bit memory functionality. In order to have good multi-bit memory functionality, a thinner initial layer and bigger height difference in the grating structure are preferred. And the bottom line is that the operation voltage for the thick layer should not cause breakdown of the thin layer. The results proved that the imprinted grating pattern with a structure of line: 20 μm / space: 10 μm is better than other patterns for multiple data recording. The multi-bit ferroelectric capacitor fabricated in our experiment exhibits a good retention performance.

The second application is FeFET, which is better than ferroelectric capacitors in terms of scaling down and having a non-destructive readout. Generally, one challenge for FeFET devices is to overcome the low values of data retention time. One of the reasons is the charge trapping in the interface between the ferroelectric film and the semiconductor. To fabricate defect-free P(VDF-TrFE) film by imprinting lithography, is necessary to reduce the charge trapping phenomenon.

As the conclusion, the feasibility study of using thermal NIL has demonstrated that this technology is a good solution for patterning functional polymer materials. However, as a new technology, issues such as defects, yields, process reliability, costs, etc. must all be clearly defined in order to be considered a production-worthy solution.



(a) (b)

Figure 6.1: Imprinting in roll-to-roll line with (a) a cylinder stamp and (b) a flat stamp.

6.2 Future Work

Future development work will encompass some issues for imprinting on flexible electronic devices and design imprinting stamps with smaller features and more levels. A continuation to further understand the limitations of nano-imprinting technology as applied to producing and testing devices will be done during this development.

It should be noted that in order to imprint in a roll-to-roll line for fabrication of flexible electronic devices, the stamp material needs to be taken into account, as well as the anti-adhesive issue. Since Si has a poor mechanical strength, Ni is usually used as the stamp material in a roll-to-roll line. The oxide layer on the Ni surface deteriorates the anti-adhesive property of SAM-deposited Ni stamps. However, it is not easy to carry out the pretreatment to reduce the oxide layer on the Ni stamp. In some studies, an electrochemical pretreatment was used to reduce the oxide layer on Ni and make molecules of SAM adsorbed on the surface orderly. However, with repeated imprinting, the SAM is prone to degradation due to process parameters. This degradation requires the periodic reapplication of the SAM, which is inefficient for Ni stamps. Besides, if there is some organic contamination on the stamps, oxygen plasma cleaning treatment can not be used as normal for the Si stamp. This process might destroy the SAM on top of Ni and produce a thick oxide layer that is strongly hydrophilic.

So far, most of the approaches for making hydrophobic Ni stamp are coating the stamp with Si [9], SiO_2 [41] or Au. Therefore, a silane-based SAM layer can be formed on the Si or SiO_2 surface, while a thiol-based SAM layer can be formed on Au surface. In our trial experiments for study of the anti-adhesive issue for Ni stamps, the first approach has been tested. The coated layer is 5 nm Ti and 20 nm SiO_2, in which Ti is inserted to improve the adhesion between Ni and Si.

In order to increase data capacity, it is very helpful to design imprinting stamps with smaller features and more levels. However it should be noted that as the device area scales down, the size effect will become more apparent and critical. The future work will focus on performance optimization of the imprinted devices and on the study of device performance while scaling down the size of the imprinting patterns.

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Appendix A

Glossary

In this appendix we give an overview of frequently used terms and abbreviations.

a-GIZO amorphous Gallium Indium Zinc Oxide

DSC: Differential Scanning Calorimetry

EUV: Extreme ultraviolet

FDTS: (1H,1H,2H,2H-Perfluorodecyltrichlorosilane, 97% ($C_{10}H_4Cl_3F_17Si$))

FWHM: Full width at half maximum

NIL: Nano-imprinting Lithography.

OLED: Organic Light Emitting Diode.

P(VDF): Poly(Vinylidene Fluoride).

P(VDF-TrFE): Poly(Vinylidene Fluoride-Trifluoroethylene).

PZT: Pb(Zr,Ti) O_3

RMS: Root-mean-square

SAM: Self-Assembled Monolayer

SEM: Scanning electron microscope

SPM: Scanning Probe Microscopy lithography

TFTs: Thin Film Transistors