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A Synchronized Switch Harvesting Rectifier With Reusable Storage Capacitors for Piezoelectric Energy Harvesting

Xinling Yue, *Graduate Student Member, IEEE*, and Sijun Du, *Senior Member, IEEE*

***Abstract*— Synchronized ac–dc rectifiers are widely used for energy rectification in piezoelectric energy harvesting (PEH), which have to employ a bulky inductor or some dedicated flying capacitors for high energy conversion efficiency. This article proposes a synchronized switch harvesting on shared capacitors (SSHSC) rectifier achieving synchronized voltage flipping without inductors or dedicated flying capacitors for PEH. The proposed SSHSC rectifier employs only three energy-storage capacitors with a specific capacitance ratio (3:3:1). These three capacitors mainly serve as storage capacitors; they can also be reused as flying capacitors for bias-flip operations. Thanks to the capacitor-sharing technique, this SSHSC rectifier takes a small volume and fewer I/O pads compared to prior SSHC rectifiers. This design was fabricated in a 180-nm BCD process, and the measured results show 78% voltage flipping efficiency and 7.58× power enhancement.**

***Index Terms*— Bias-flip rectifier, energy harvesting, inductorless, miniaturization, piezoelectric transducers (PTs), rectifier, synchronized switch harvesting on capacitors (SSHC).**

I. Introduction

ENERGY harvesting has emerged as an alternative solution to traditional batteries, which are often bulky and difficult to replace in wireless applications in the Internet-of-Things (IoT) [1], [2], [3], [4], [5]. Among energy-harvesting systems, piezoelectric energy harvesting (PEH) has been widely used in recent years due to its high power density and compatibility with CMOS technologies [1], [6], [7], [8], [9], [10]. It harvests vibration energy from environments and converts it into electrical energy with a piezoelectric transducer (PT). When the PEH electromechanical coupling is relatively weak, it can be approximately modeled as an ac current source, I_P, in parallel with a capacitor, C_P, and a resistor, R_P, as shown in Fig. 1. As the output power from the PT is ac power, rectifiers are typically required for energy extraction and rectification [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21].

Full bridge rectifiers (FBR) are widely employed due to their easy implementations, simplicity, and stability. However, the output power efficiency of a passive FBR is low since

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The authors are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: sijun.du@tudelft.nl).

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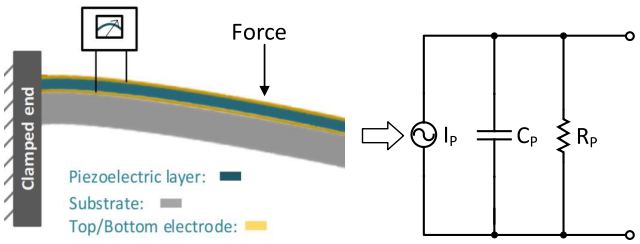

Fig. 1. PT and its equivalent electrical model.

the PT voltage (V_{PT}) has to be flipped slowly by its generated charge. To improve the output efficiency, some active rectifiers were studied to assist V_{PT} to flip the PT voltage [9], [22], [23], [24], [25]. The synchronized switch harvesting on the inductor (SSHI) rectifier employs a discrete inductor to synchronously flip the voltage across the PT [1]. To have good performance, the external inductor is typically large, which is counter to system miniaturization in space-limited application scenarios. To eliminate the large inductor in SSHI rectifiers, synchronized switch harvesting on capacitors (SSHC) rectifiers were proposed by using multiple flying capacitors to flip the PT voltage in multiple phases [2], [3]. The SSHC rectifier largely reduces the system volume and cost since the volume and cost of the capacitors are much lower than a bulky off-chip inductor. Typical SSHC rectifiers require a large number of dedicated off-chip flying capacitors for good performance, for example, eight capacitors for voltage flipping and one capacitor for energy storage [2], [3]. These capacitors dominate the system volume. Though a fully integrated SSHC rectifier was proposed by implementing all the flying capacitors on-chip [4], it can only work with tiny PTs fabricated in MEMS technology, which has small internal capacitors (C_P) of sub-nF level, resulting in lower output power. The general commercial PT usually has a very large intrinsic capacitance that is several tens of nF. When employing the general PT for higher harvested power, the flying capacitors cannot be integrated on-chip anymore and hence they can only be implemented off-chip. Therefore, reducing the number of off-chip components is crucial in reducing the overall form factor and cost.

To reduce the system volume, this article proposes a synchronized switch harvesting on shared capacitors (SSHSC) rectifier achieving synchronized voltage flipping without an inductor or dedicated flying capacitors. In a typical SSHC rectifier, eight flying capacitors and one energy storage capacitor

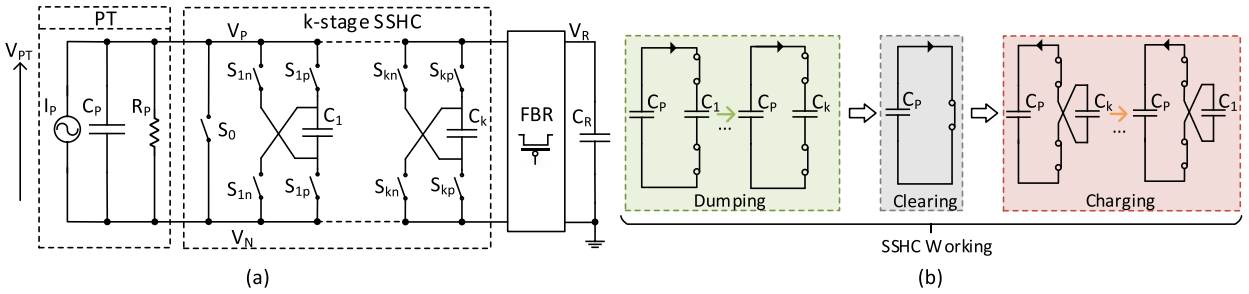

Fig. 2. (a) Topology of the typical k-stage SSHC rectifier. (b) SSHC rectifier working process during the flipping moment.

TABLE I
OFF-CHIP COMPONENTS FOR ACTIVE RECTIFIERS

Different Rectifier Types	Total Off-Chip Components
SSHI	1 Inductor + 1 Capacitor
SSHC	9 Capacitors
Proposed SSHSC	3 Capacitors

are required for good energy-extraction performance. In the proposed SSHSC rectifier, no dedicated flying capacitor is present; instead, the energy storage capacitors are temporarily borrowed as flying capacitors to flip the PT voltage. To properly and efficiently flip the voltage, three storage capacitors are employed and connected in series with a capacitance ratio of 3:3:1. Due to the absence of dedicated flying capacitors, the off-chip components only include three energy-storage capacitors, which take a smaller volume and less I/O connections compared to conventional SSHC rectifiers. Table I compares the off-chip components of popular active rectifiers with the proposed rectifier. The proposed SSHSC rectifier does not require any inductor and employs the least off-chip capacitors.

II. THEORETICAL ANALYSIS

A. Flying Capacitors Used in a Typical SSHC Rectifier

Fig. 2(a) shows a typical k-stage SSHC rectifier [2]. There are k flying capacitors dedicated for voltage flipping: C_1 to C_k, and each flying capacitor is controlled by four switches. The FBR block represents the FBR composed of four cross-connected MOSFETs and an active diode. V_R is the output rectified voltage across the storage capacitor C_R. The k flying capacitors require $4k + 1$ switches to flip the voltage across the PT (V_{PT}). When V_{PT} is being flipped, the working process of the SSHC rectifier consists of three major steps, as shown in Fig. 2(b): (dumping) the charge is dumped from C_P to $C_1, \ldots, C_k$, in k phases; (clearing) the remaining charge in C_P is cleared in one phase; (charging) C_P is charged from $C_k, \ldots, C_1$ in a reversed order and polarity to finalize the flipping process in k phases. The ratio of the absolute voltage $|V_{\mathrm{PT}}|$ after and before the flipping is the voltage flipping efficiency (η_F). To let the rectifier extract more energy from the PT, η_F needs to be as high as possible [26]. When employing the SSHC rectifier, there is an intrinsic relation between η_F and the capacitors. Assuming that all flying capacitors are equal ($C_1 = C_2 = \cdots = C_k$), the relation can be written as follows [27]:

$$\eta_F = \frac{kC_k}{C_P + (k+1)C_k} \tag{1}$$

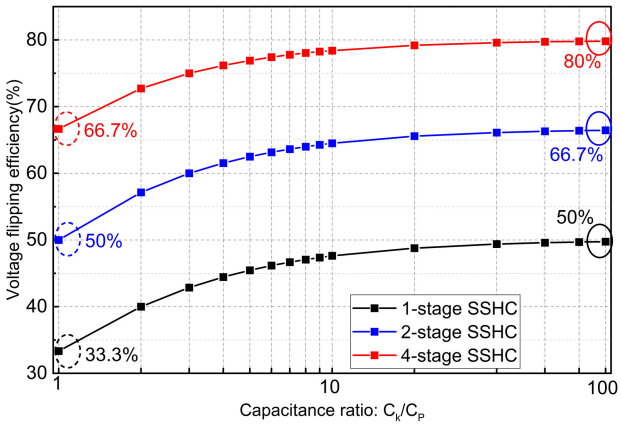

Fig. 3. Voltage flipping efficiency of one-, two-, and four-stage SSHC rectifiers with different flying capacitor to C_P ratios.

where k is the number of flying capacitors used in an SSHC rectifier, C_k is the capacitance of each flying capacitor, and C_P is the capacitor of the PT. From (1), it can be seen that the more and larger flying capacitors are employed, the higher the flipping efficiency is. Fig. 3 shows η_F for one-, two-, and four-stage SSHC rectifiers with varying capacitance ratios of C_k/C_P. When C_k is selected as equal capacitance to C_P, the corresponding η_F of one-, two-, and four-stage SSHC rectifiers is 33.3%, 50%, and 66.7%, respectively.

The SSHC rectifier in [2] uses eight flying capacitors to achieve 80% flipping efficiency, where the capacitance of C_k equals C_P. According to (1), increasing the capacitance of C_k results in a higher flipping efficiency, according to (1). However, the relationship is nonlinear. The growth trend is shown in Fig. 3. The flipping efficiency increases a lot when the capacitance ratio C_K/C_P grows from 1× to 10×. However, from 90× to 100×, the flipping efficiency has very limited increment, which means that the flipping efficiency is already in saturation when flying capacitance is 90×–100× larger than C_P. In Fig. 3, the maximum flipping efficiency is 50%, 66.7%, and 80%, respectively, when flying capacitors use 100× larger capacitance than C_P. Therefore, using larger capacitors for voltage flipping can reduce the number of off-chip capacitors. And when the capacitance is large enough (over 100×), the flipping efficiency is already in saturation and would not be higher with a larger capacitance.

Considering the circuit complexity and the output power efficiency, using four flying capacitors with a much larger

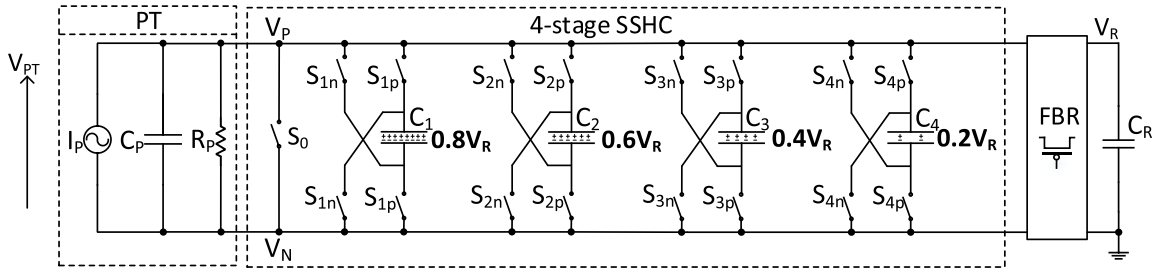

Fig. 4. Voltage levels across the large flying capacitors of a typical four-stage SSHC rectifier.

capacitance than C_P is preferred for both system miniaturization and output performance. If four flying capacitors are employed in a typical SSHC rectifier, there are 17 switches in total, as shown in Fig. 4. Assuming that the employed flying capacitors are much higher than C_P, after sufficient flipping cycles, the voltage across C_1, C_2, C_3, and C_4 is maintained at $0.8V_R$, $0.6V_R$, $0.4V_R$, and $0.2V_R$, respectively.

B. Storage Capacitors Shared in the Proposed SSHSC Rectifier

1) Storage Capacitor Sharing Possibility Analysis for Flipping: In a typical SSHC rectifier, during the flipping period, the dedicated flying capacitors, C_1–C_k, are used to store the charge in C_P in a short time and dump the charge back to C_P in sequence. Therefore, the flying capacitors in typical SSHC rectifiers work as temporary charge reservoirs. From Fig. 3, it is shown that by using large flying capacitors, the voltage flipping efficiency can be greatly enhanced. For all the bias-flip rectifiers, including the SSHC rectifiers, the storage capacitors are the largest energy reservoirs which are usually hundreds or thousands of times larger than the flying capacitors. These storage capacitors are used to store harvested energy when the bridge rectifier is conducting, and they are not used when the rectifier is cut-off. This indicates that these storage capacitors can be reused as flying capacitors to flip the voltage across the PT, which happens exactly when the rectifier is cut-off. Therefore, two nonconflict operations of using the storage capacitors guarantee the possibility of sharing them for storing energy and flipping voltage purposes, without employing a group of dedicated flying capacitors.

2) Voltage Levels Generated by Different Combinations of the Storage Capacitors: As temporary flying capacitors, the flipping operation should not change the voltage across the storage capacitor before and after flipping, which raises a specific requirement for the storage capacitance ratio. When a typical SSHC rectifier is implemented with four flying capacitors much larger than C_P, as shown in Fig. 4, the voltage levels across the flying capacitors C_1, C_2, C_3, and C_4 are $0.8V_R$, $0.6V_R$, $0.4V_R$, and $0.2V_R$, respectively. Therefore, the storage capacitors are also required to provide these voltage levels for flipping as typical SSHC rectifiers do. To achieve this, the proposed SSHSC rectifier employs three storage capacitors connected in series with the specific capacitance ratio: C_{R1}:C_{R2}:C_{R3} = 3:3:1 as shown in Fig. 5. There are two connection configurations for the three storage capacitors: Con. (I) (following the sequence from the top V_R to $C_{R1} \rightarrow C_{R2} \rightarrow C_{R3}$ to ground) and Con. (II) (following the sequence from the top V_R to $C_{R3} \rightarrow C_{R1} \rightarrow C_{R2}$ to ground). Con. (I) is the default configuration when they are used as energy storage capacitors. Starting from the cold state, the voltages across C_{R1}, C_{R2}, and C_{R3} are $0.2V_R$, $0.2V_R$, and $0.6V_R$, respectively, due to the specific ratio of C_{R1}, C_{R2}, and C_{R3} (3:3:1). Therefore, in Con. (I), V_{R2P} and V_{R3P}, the voltage at the positive plates of C_{R2} and C_{R3}, provide the voltage levels of $0.8V_R$ and $0.6V_R$ for the one- and two-stage flipping, respectively. While in Con. (II), V_{R1P} and V_{R2P}, the positive plate of C_{R1} and C_{R2}, provide the voltage levels $0.4V_R$ and $0.2V_R$ for the three- and four-stage flipping, respectively. Therefore, the four virtual flying capacitors used in the four-stage SSHSC rectifier are C_{Fly1} (C_{R2} and C_{R3} in series), C_{Fly2} (C_{R3} only), C_{Fly3} (C_{R1} and C_{R2} in series), and C_{Fly4} (C_{R2} only).

The four voltage levels V_{Fly1}, V_{Fly2}, V_{Fly3}, and V_{Fly4} provided by the virtual flying capacitors C_{Fly1}, C_{Fly2}, C_{Fly3}, and C_{Fly4} are $0.8V_R$, $0.6V_R$, $0.4V_R$, and $0.2V_R$, respectively, which are the same values as generated by dedicated flying capacitors in a typical SSHC rectifier shown in Fig. 4.

3) Theoretical Analysis on Shared Capacitors: The voltage flipping includes four stages and is divided into three phases: dumping, clearing, and charging as the same as in Fig. 2(b). After each phase, the PT voltage V_{PT}, V_{Fly1}, V_{Fly2}, V_{Fly3}, and V_{Fly4} are updated to new values. To guarantee the proper flipping operations and no energy stolen from the three storage capacitors to C_P to help flipping, the voltage across each of the storage capacitors should maintain the same value before and after each flipping operation. Hence, a detailed theoretical analysis is performed in this section to prove this assumption, which will also be verified in the measurement section later.

First, the voltages across PT (V_{PT}) in the first stage with virtual capacitor, C_{Fly1}, can be calculated as follows:

before dumping

$$V_{\text{PT}} = V_R, \quad V_{\text{Fly1}} = 0.8 \times V_R$$

after dumping

$$V_{\text{PT}} = V_{\text{Fly1}} = \frac{V_R \times C_P + 0.8 \times V_R \times C_{\text{Fly1}}}{C_{\text{Fly1}} + C_P} = 0.8 \times V_R + \frac{0.2 \times V_R \times C_P}{C_P + C_{\text{Fly1}}} = 0.8 \times V_R + \alpha_1 \quad (2)$$

where $\alpha_1 = ((0.2 \times V_R \times C_P)/(C_P + C_{\text{Fly1}}))$. Since C_{Fly1} is built of storage capacitors, which are significantly larger than

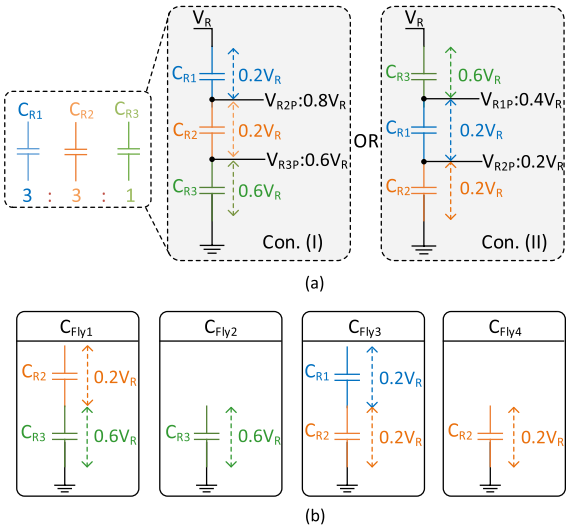

Fig. 5. Configurations and combinations of three storage capacitors to form four virtual flying capacitors to be used in a four-stage SSHSC rectifier. (a) Voltage levels generated by the storage capacitors. (b) Four virtual flying capacitors for voltage flipping.

C_P, the voltage increment, α_1, is extremely small. The next phase is to dump the charge from C_P to C_{Fly2}. The PT voltage (V_{PT}) variations in this phase are

before dumping

$$V_{\text{PT}} = 0.8 \times V_R + \alpha_1, \quad V_{E2} = 0.6 \times V_R$$

after dumping

$$\begin{aligned} V_{\text{PT}} = V_{\text{Fly2}} &= \frac{(0.8 \times V_R + \alpha_1) \times C_P + 0.6 \times V_R \times C_{\text{Fly2}}}{C_{\text{Fly2}} + C_P} \\ &= 0.6 \times V_R + \frac{0.2 \times V_R \times C_P}{C_P + C_{\text{Fly2}}} + \frac{\alpha_1 \times C_P}{C_P + C_{\text{Fly2}}} \\ &= 0.6 \times V_R + \alpha_2 + \frac{\alpha_1 \times C_P}{C_P + C_{\text{Fly2}}} \end{aligned} \tag{3}$$

where $\alpha_2 = ((0.2 \times V_R \times C_P)/(C_P + C_{\text{Fly2}}))$. Similarly, due to $C_{\text{Fly2}} \gg C_P$, α_2 is an extremely small value, and the third term in (3) becomes even much smaller due to the existence of α_1. Hence, the third term can be ignored in front of the first and the second terms for easier calculations. Therefore, (3) becomes

$$V_{\text{PT}} = V_{\text{Fly2}} \approx 0.6 \times V_R + \alpha_2. \tag{4}$$

Similarly, after the dumping in the third and fourth phases, the voltages can be expressed as follows:

$$\begin{aligned} V_{\text{PT}} = V_{\text{Fly3}} &= \frac{(0.6 \times V_R + \alpha_2) \times C_P + 0.4 \times V_R \times C_{\text{Fly3}}}{C_{\text{Fly3}} + C_P} \\ &= 0.4 \times V_R + \frac{0.2 \times V_R \times C_P}{C_P + C_{\text{Fly3}}} + \frac{\alpha_2 \times C_P}{C_P + C_{\text{Fly3}}} \\ &= 0.4 \times V_R + \alpha_3 + \frac{\alpha_2 \times C_P}{C_P + C_{\text{Fly3}}} \approx 0.4 \times V_R + \alpha_3 \end{aligned} \tag{5}$$

$$\begin{aligned} V_{\text{PT}} = V_{\text{Fly4}} &= \frac{(0.4 \times V_R + \alpha_3) \times C_P + 0.2 \times V_R C_{\text{Fly4}}}{C_{\text{Fly4}} + C_P} \\ &= 0.2 \times V_R + \frac{0.2 \times V_R \times C_P}{C_P + C_{\text{Fly4}}} + \frac{\alpha_3 \times C_P}{C_P + C_{\text{Fly4}}} \\ &= 0.2 \times V_R + \alpha_4 + \frac{\alpha_3 \times C_P}{C_P + C_{\text{Fly4}}} \approx 0.2 \times V_R + \alpha_4 \end{aligned} \tag{6}$$

where $\alpha_3 = ((0.2 \times V_R \times C_P)/(C_P + C_{\text{Fly3}}))$ and $\alpha_4 = ((0.2 \times V_R \times C_P)/(C_P + C_{\text{Fly4}}))$. Therefore, after dumping charge from C_P to the four virtual flying capacitors, the voltage changes in the four virtual flying capacitors are approximately α_1, α_2, α_3, and α_4, respectively. They are all very small values. After dumping, the remaining charge in C_P is cleared to zero in the following phase, resulting in $V_{\text{PT}} = 0$. The sequence of the charge charging back to C_P follows the reverse sequence compared with the dumping. The voltage across PT and effective capacitor after the first phase of charging is expressed as follows:

$$\begin{aligned} -V_{\text{PT}} = V_{\text{Fly4}} &= \frac{0.2 \times V_R \times C_{\text{Fly4}} + \alpha_4 \times C_{\text{Fly4}}}{C_{\text{Fly4}} + C_P} \\ &= 0.2 \times V_R - \alpha_4 + \frac{\alpha_4 \times C_{\text{Fly4}}}{C_{\text{Fly4}} + C_P} \approx 0.2 \times V_R. \end{aligned} \tag{7}$$

The approximation in last derivation step in (7) is because $C_{\text{Fly4}} \gg C_P$, and the two α_4 cancel. Therefore, after this charging phase, the voltage across PT and C_{Fly4} go back $0.2V_R$, which is the voltage before C_{Fly4} was used in the fourth dumping phase. This explains that the voltage across the C_{Fly4} does not change before and after the voltage flipping process. Similarly, the voltage of the second, third, and fourth flipping phases can be written as follows:

$$\begin{aligned} -V_{\text{PT}} &= V_{\text{Fly3}} \\ &= 0.4 \times V_R - \alpha_3 + \frac{\alpha_3 \times C_{\text{Fly3}}}{C_{\text{Fly3}} + C_P} \approx 0.4 \times V_R \end{aligned} \tag{8}$$

$$\begin{aligned} -V_{\text{PT}} &= V_{\text{Fly2}} \\ &= 0.6 \times V_R - \alpha_2 + \frac{\alpha_2 \times C_{\text{Fly2}}}{C_{\text{Fly2}} + C_P} \approx 0.6 \times V_R \end{aligned} \tag{9}$$

$$\begin{aligned} -V_{\text{PT}} &= V_{\text{Fly1}} \\ &= 0.8 \times V_R - \alpha_1 + \frac{\alpha_1 \times C_{\text{Fly1}}}{C_{\text{Fly1}} + C_P} \approx 0.8 \times V_R. \end{aligned} \tag{10}$$

According to the analysis, the voltage across all the four virtual flying capacitors after the flipping process, as given in (7)–(10), are the same as their voltage before the flipping process, as given in (2)–(5). Furthermore, the analysis also shows that the voltage flipping efficiency for V_{PT} is 80%, according to V_{PT} before and after flipping, as given in (10). The analysis shows that the proposed SSHSC rectifier can achieve a promising voltage flipping efficiency at 80%, while keeping the voltage across the storage capacitors unchanged. These two results theoretically prove our assumption in building the SSHSC rectifier without using any dedicated flying capacitors.

III. System Architecture

The detailed flipping process of the proposed SSHSC rectifier is shown in Fig. 6. When the bridge rectifier is conducting, the three storage capacitors follow the connection Con. (I) in Fig. 5, as shown in Fig. 6 (top left). When the bridge rectifier is cut off, and V_{PT} needs to be flipped, the three storage capacitors form the four virtual flying capacitors with different combinations and configurations. Fig. 6 shows the nine phases

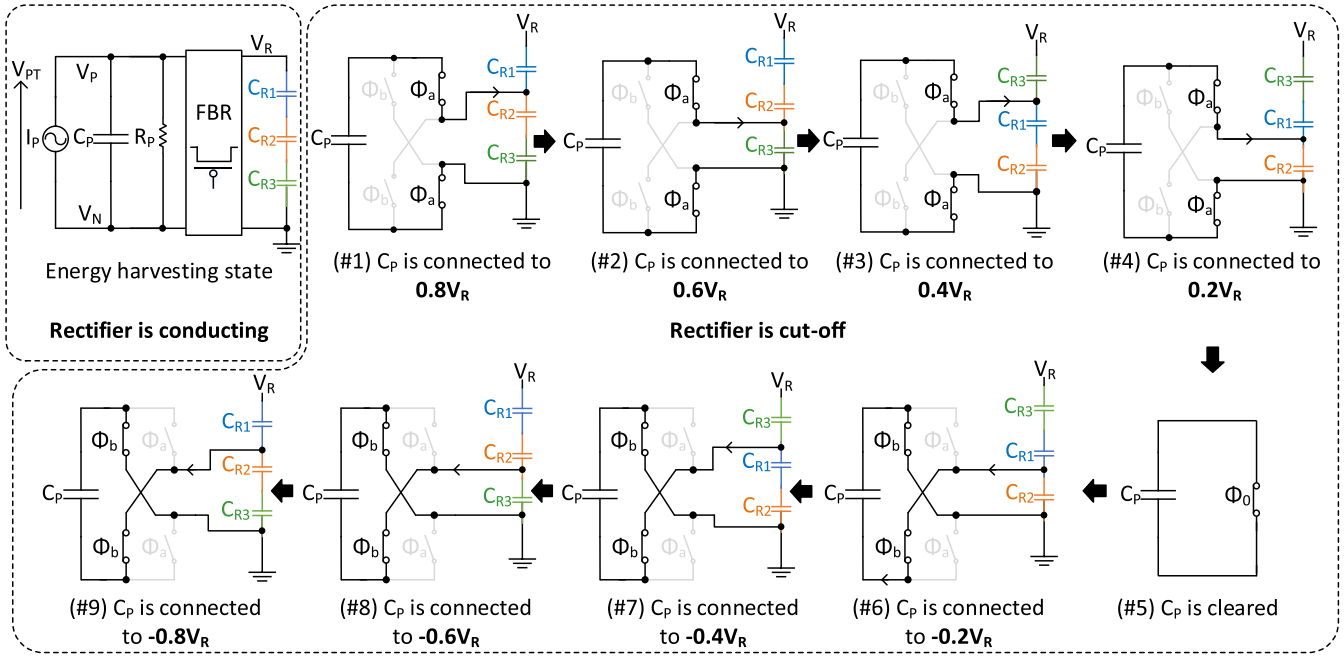

Fig. 6. Working flow of the proposed SSHSC rectifier: rectifier is conducting for energy extraction; rectifier is cut-off for flipping V_{PT} in nine phases.

(#1–#9) to flip V_{PT} from positive to negative. If V_{PT} needs to be flipped from negative to positive, the phase order simply starts from #9 and ends at #1. In phase #1, by closing ϕ_a, C_P is connected in series with C_{R2} and C_{R3} ($C_{R2}+C_{R3}$) which provide the $0.8V_R$ voltage level, so the charge in C_P dumps to C_{R2} and C_{R3}. After first dumping, the voltage across C_P and $C_{R2}+C_{R3}$ are both very close to $0.8V_R$, thanks to their large capacitance. Then, C_{R3} provides $0.6V_R$ for the second stage dumping as shown in Fig. 6 (#2) and C_P dumps the charge to C_{R3} and V_{PT} is finally stabilized at $0.6V_R$. To generate $0.4V_R$ and $0.2V_R$ for three- and four-stage flipping, the connection of the three storage capacitors is changed from Con. (I) to Con. (II) in Fig. 6 (#3) and (#4), respectively. The C_P is connected and dumped charge to C_{R1} and C_{R2} in Fig. 6 (#3) and C_{R2} in Fig. 6 (#4), respectively, and stabilized at $0.4V_R$ and $0.2V_R$ eventually. After dumping, ϕ_0 is turned on, and the remaining charge in C_P is cleared. After clearing C_P, the charging begins and follows the inverse sequence of dumping: from (#6) to (#9). From (#6) to (#9) in Fig. 6, the charge is flipped back from $C_{R2} \rightarrow C_{R1}+C_{R2} \rightarrow C_{R3} \rightarrow C_{R2}+C_{R3}$ to C_P, where the storage capacitors provide $-0.2V_R$, $-0.4V_R$, $-0.6V_R$, and $-0.8V_R$, respectively, for charging C_P.

Fig. 7 shows the system architecture of the proposed SSHSC rectifier. It includes five main parts: an FBR, a "switch I" block and its associated control block, as well as a "switch II" block and its associated control block. The "switch I" block performs the voltage flipping process in nine phases, while the "switch II" block creates virtual flying capacitors with three storage capacitors corresponding to the nine flipping phases. When it is time to flip the PT voltage, the FBR block will generate a synchronized signal (SYN). As an indicator, the SYN is fed to the "switch II control" block, which will generate S_{R1} and S_{R2} to decide the configurations of the storage capacitors as the same as in Fig. 5. After the configuration is fixed, the SYN is fed to the "switch I control" block to generate the switch control signals for the switches in the "switch I" block. Through the pulse generation (PG), pulse sequencing (PS) block, and some OR gates, the control signals are prepared. Through the level shifters (LSs), the signals Φ_a, Φ_b, Φ_0, S_{R3P}, S_{R2P}, and S_{R1P} are used to drive the switches in the "switch I" block.

Unlike typical SSHC rectifiers, the synchronized switches ϕ_a and ϕ_b in "switch I," are used repeatedly in every flipping stage, reducing the chip's dimension for large switches. The circuit details of the LS, PS cell, delay cell, and transmission gate are also presented in Fig. 7.

The V_{PT} flipping moment from positive to negative and the corresponding switch control signals are shown in Fig. 8. It has nine flipping phases from (#1) to (#9) and follows the voltage levels from $0.8V_R \rightarrow 0.6V_R \rightarrow 0.4V_R \rightarrow 0.2V_R \rightarrow 0 \rightarrow -0.2V_R \rightarrow -0.4V_R \rightarrow -0.6V_R \rightarrow -0.8V_R$. S_{R1} and S_{R2} are used to decide if Con. (I) or Con. (II), shown in Fig. 5(a), is used. S_{R1} is high during (#3)–(#7), which is exactly in three- and four-stage flipping and PT voltage clearing periods; otherwise, S_{R2} always keeps high. S_{R1P}, S_{R2P}, and S_{R3P} are used to decide which positive plates of C_{R1}, C_{R2}, and C_{R3} are connected to V_P to generate four voltage levels for charging, as the same as introduced in Fig. 5. ϕ_a, ϕ_b, and ϕ_c are used to drive only one group of synchronized switches to connect the effective capacitors to C_P for flipping instead of dedicated switches for every flying capacitor.

IV. Circuit Implementations

In this section, the implementations of the FBR, PG block, and switch bulk regulation block are presented. To reduce the

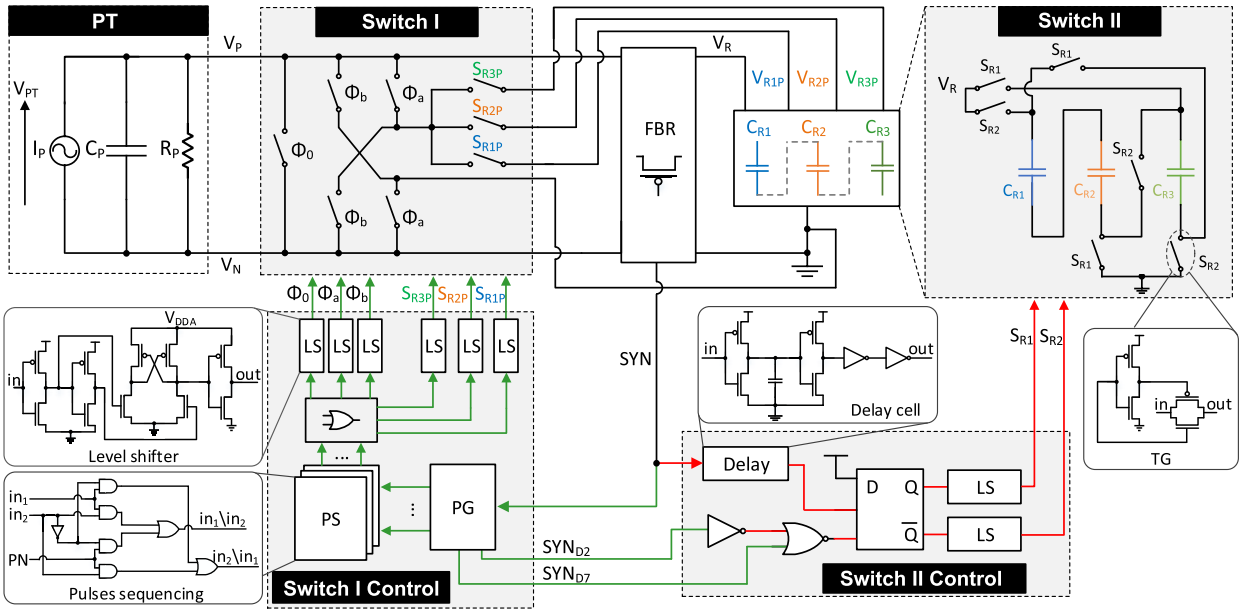

Fig. 7. System architecture of the proposed SSHSC rectifier.

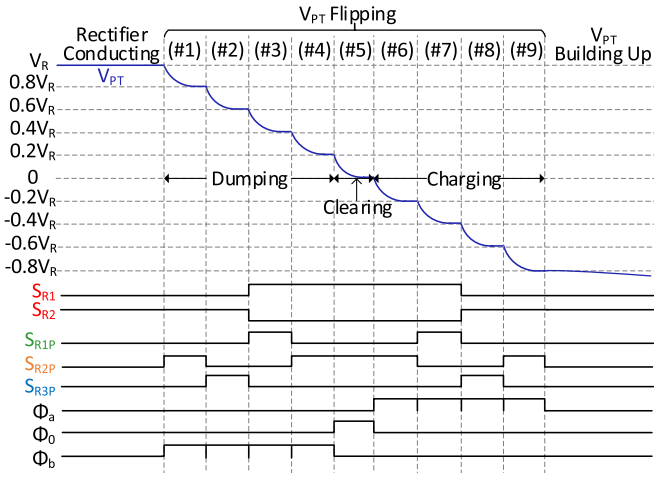

Fig. 8. PT voltage flipping moment and the associated control signals for switches.

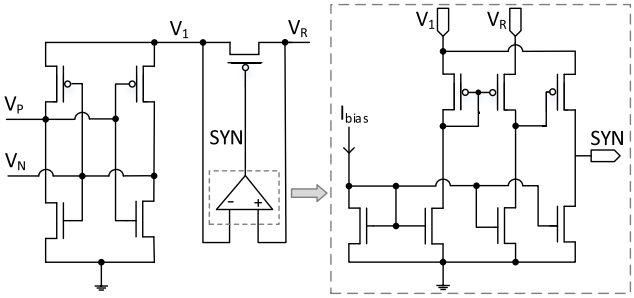

Fig. 9. Four cross-connected MOSFETs and active diode in the FBR block.

voltage drop of the diodes in the FBR block, the FBR consists of four cross-connected MOSFETs, and an active diode [8], as shown in Fig. 9. When the current of I_P is zero, the FBR becomes nonconductive and V_1 becomes lower than V_R; the comparator is triggered, and a rising edge in the synchronized signal, SYN, is generated, which indicates the starting time for flipping. The offset in the comparator caused by random mismatch at the zero-cross moment of I_P is about 7 mV, resulting in an acceptable delay in SYN signal due to the low (130 Hz) vibration frequency.

The SYN signal is fed to the PG, as shown in Fig. 10(a). Through a PG cell, the switch control signals $\phi_1 \rightarrow \phi_9$ and their corresponding delayed SYN_D are generated, where the PG cell is composed of two weak inverters and an adjustable capacitor array C_D. The generated output control signals $\phi_1 \rightarrow \phi_9$ are fed to a PS block where the sequence of the pulses is decided by the PN generated in Fig. 10(b), which indicates the flipping sequence (from positive to negative or vice versa). Because only one group switches are shared between different stages, after sequencing, the output control signals Φ_1 to Φ_9 are fed to some OR gates to generate Φ_a, Φ_b, S_{R1P}, S_{R2P}, and S_{R3P} as shown in Fig. 10(b).

Fig. 11 shows the supply voltage selector for the transmission gate switches used in the "Switch I" and "Switch II" blocks, to achieve $V_{\text{DDA}} = \max(V_{\text{DD}}, V_R)$. This is important to make sure that the switches are fully turned on or off for proper operations. In this circuit, there are two large power switches, M_1 and M_2, whose gates are controlled by the output of a comparator, as shown on the right. When $V_{\text{DD}} > V_R$, the output of the comparator is high, resulting in M_1 and M_3 in the open state and M_2 in the OFF state. Therefore, $V_{\text{DDA}} = V_{\text{DD}}$. Similarly, when $V_{\text{DD}} < V_R$, V_{DDA} is connected to V_R.

V. Experiment Result Analysis

The proposed SSHSC rectifier was fabricated in a 180-nm BCD process, which occupies 0.18-mm^2 active area. Fig. 12 shows the measurement setup (left) and the chip micrograph (left). A commercial PT (S129-H5FR-1803YB) was employed in the experiment with the resonant frequency of 130 Hz and

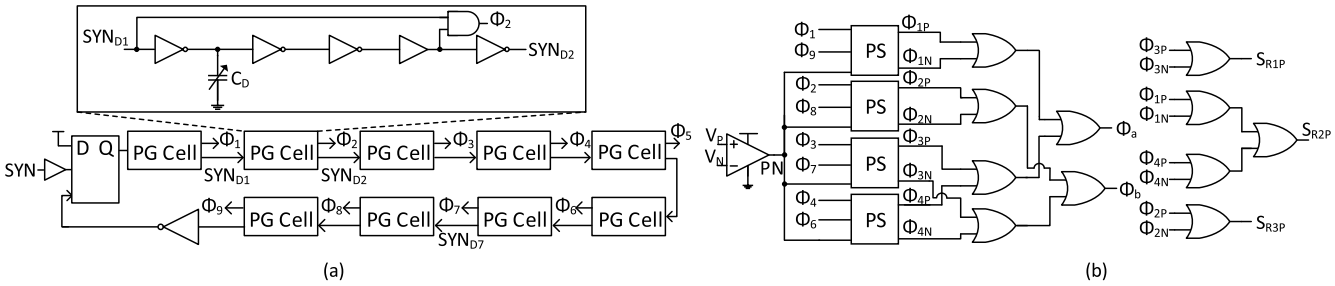

Fig. 10. PG block in "switch I control". (a) PG for each switch control in every stage during flipping. (b) PG for one group shared switch.

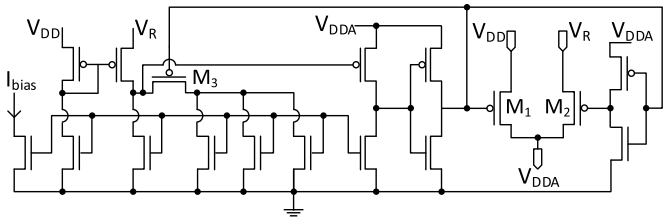

Fig. 11. Supply voltage selector for switches of SSHSC rectifier.

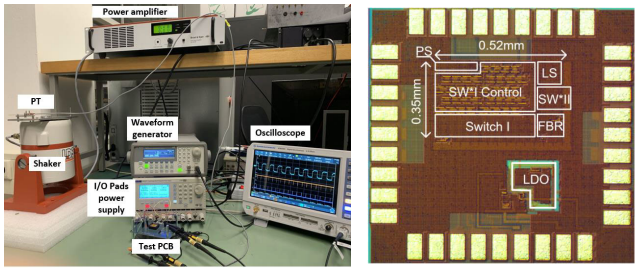

Fig. 12. Measurement setup and chip micrograph.

the intrinsic capacitance C_P of 22 nF. Fig. 13 (top) shows the measured waveform of $V_{\rm PT}$, S_{R1}, and S_{R2} and their zoomed-in versions during voltage flipping. The V_R is flipped from −4.7 to 3.65 V, indicating 78% voltage flip efficiency (η_F). The voltage flipping is performed in nine phases with ϕ_a, ϕ_0, and ϕ_b switching signals as shown in Fig. 13(d) where the flipping moment for each phase is around 9 μs. S_{R1} (S_{R2}) switches from low to high (high to low) at the end of #2.

Fig. 13(c) shows the three voltages, V_{R1P}, V_{R2P}, and V_{R3P}, which are the voltage at the positive plates of the three storage capacitors, C_{R1}, C_{R2}, and C_{R3}, respectively. Due to the limited number of oscilloscope probes, the three switch controlling signal, Φ_a, Φ_0, and Φ_b, are ORed and shown as the fourth signal at the bottom. When $V_{\rm PT}$ is not being flipped, the connection follows Con. I in Fig. 5 and the measured voltage of V_{R1P}, V_{R2P}, and V_{R3P} are 4, 3.2, and 2.4 V, respectively, as shown in Fig. 13(c). They indicate that the voltage across the three storage capacitors C_{R1}, C_{R2}, and C_{R3} are 0.8, 0.8, and 2.4 V, with a voltage ratio of 1:1:3, which accurately matches their designed capacitance ratio of 3:3:1.

The zoomed-in voltage flipping moment is shown in Fig. 13(d), where the phases #1–#9 correspond to the phases #1–#9 in Fig. 6. During phases #1, #2, #8, and #9, the storage capacitors follow the same connection as in the energy harvesting state, which is Con. I in Fig. 5(a). Therefore, the voltage levels at the positive plates of V_{R1P}, V_{R2P}, and V_{R3P} are 4, 3.2, and 2.4 V, respectively, same as in the rectifier conducting state. During phases #3–#7, the connection of three storage capacitors is reconfigured from Con. I to Con. II [Fig. 5(a)]. Thus, the positive plate voltages V_{R1P}, V_{R2P}, and V_{R3P} are changed to 1.6, 0.8, and 4 V correspondingly, since the ground is now temporarily connected to the bottom plate of C_{R2}, instead of C_{R3}. However, the voltage across C_{R1}, C_{R2}, and C_{R3} keep the same value: 0.8, 0.8, and 2.4 V.

Fig. 14 presents the rectified output voltage, V_R, with 3-V open-circuit voltage amplitude from the PT ($V_{\rm OC}$) and 78% flip efficiency (η_F). To verify that the proposed SSHSC rectifier can adopt storage capacitors with different sizes and the voltage ratio is not affected by the inevitable inherent leakage in the capacitors over a long time of operation, two sets of storage capacitors are chosen as C_{R1}, C_{R2}, and C_{R3}: 1) 10, 10, and 3.3 μF and 2) 100, 100, and 33 μF. All the capacitors have the same surface-mounted device (SMD) package, 0805 (2012 Metric). For some SMD packages, a smaller package has a smaller maximum capacitance available. Therefore, given the optimal C_R, which varies depending on the applications, the proposed technique may require higher overall capacitance, which may lead to the use of a bigger SMD package, increasing the area. Fig. 14(a) shows the output voltage for the capacitor set (1), and V_R is charged from 0 to 4.7 V. During the cold startup period, V_R has some fluctuations due to the weak gate-driving voltage of the switches controlled by S_{R1} and S_{R2}. After startup, the SSHSC rectifier is engaged, and the V_R starts increasing faster. The spikes of V_R are caused by the switching moment of S_{R1} and S_{R2} due to the temporary disconnection to the ground, which will be fully recovered in 1–2 ns. Since the three storage capacitors are off-chip implemented, the bottom-plate effect is negligible. When the capacitance of the storage capacitors is increased by 10× larger with the capacitor set (2), the measured rectified voltage, V_R, is shown in Fig. 14(b). It has a similar waveform as Fig. 14(a), indicating that the rectified voltage and flipping operation are affected as long as the three storage capacitors have the ratio of 3:3:1. However, with the larger capacitor set, longer time is needed to build up V_R.

The measured output power from the proposed SSHSC rectifier and FBR is shown in Fig. 15(a). It shows that the proposed SSHSC rectifier achieves the maximum rectified power at 72 and 130 μW with $V_{\rm OC}$ = 2 V and $V_{\rm OC}$ = 3 V,

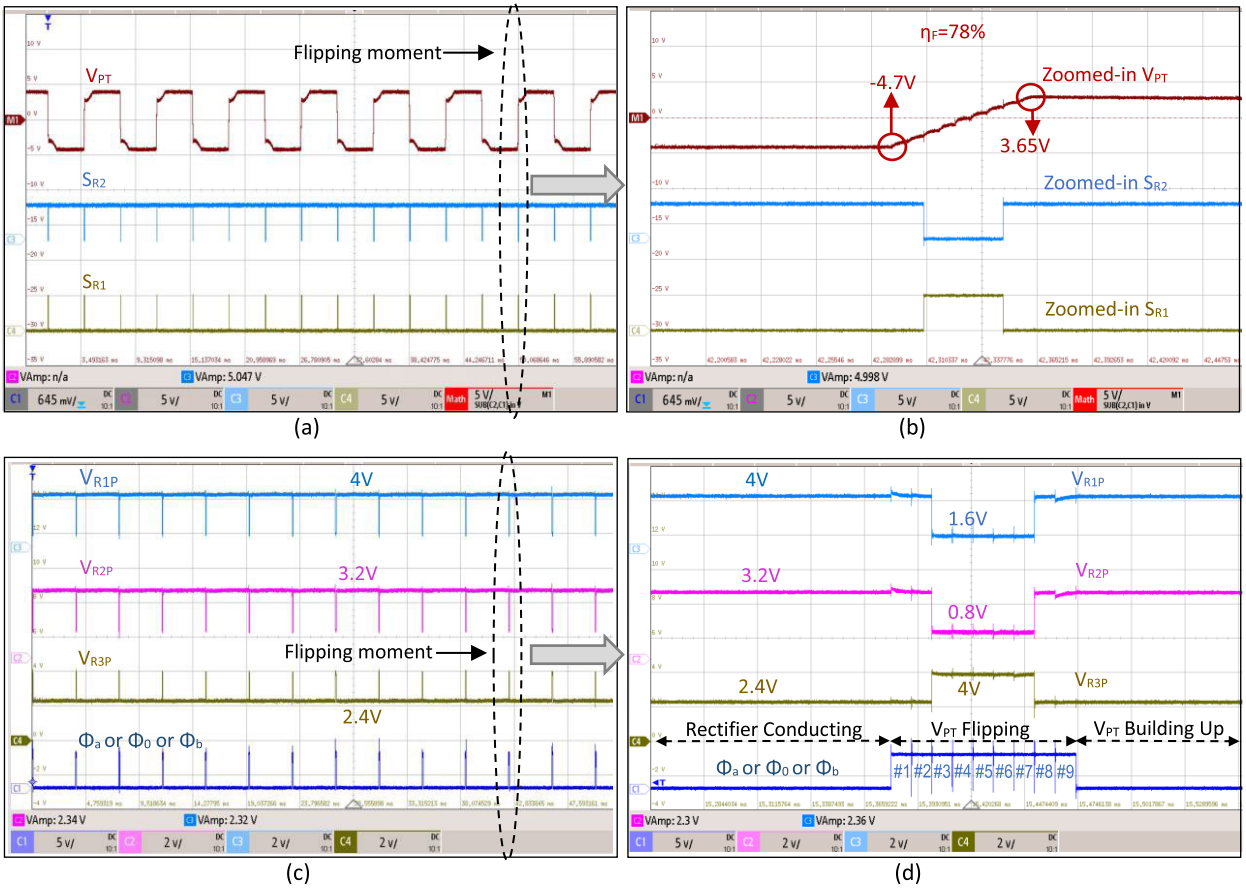

Fig. 13. Measured waveform: (a) V_{PT} and switch control signals S_{R2} and S_{R1}, and (b) their zoomed-in versions during the flipping moment, (c) voltage at positive plates of three storage capacitors, V_{R1P}, V_{R2P}, V_{R3P}, and ORed version of flipping signals, OR(Φ_a, Φ_b, and Φ_a), and (d) their zoomed-in versions during the flipping moment.

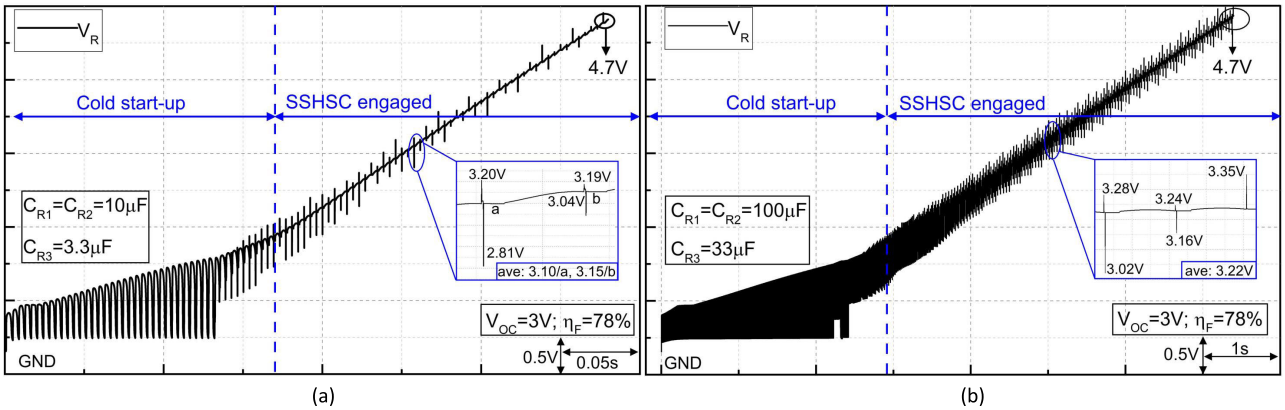

Fig. 14. Measured output voltage, V_R, with different storage capacitor sets: (a) $C_{R1} = C_{R2} = 10$ μF and $C_{R3} = 3.3$ μF and (b) $C_{R1} = C_{R2} = 100$ μF and $C_{R3} = 33$ μF.

respectively, while the FBR can only generate 9.5 μW power. The proposed SSHSC rectifier achieves 7.58× maximum power enhancement compared to an FBR with the same input condition at $V_{OC} = 2$ V. The rectified power in a range of V_{OC} is presented in Fig. 15(b). The measured maximum power from the proposed SSHSC rectifier is 289.5 μW when V_{OC} is 6 V.

The comparisons between the proposed SSHSC rectifier and state-of-the-art works are presented in Table II. For a large commercial PT with a 22 nF-C_P, the proposed SSHSC rectifier borrows three off-chip storage capacitors for voltage flipping rather than dedicated flying inductors or capacitors. The proposed SSHSC technique achieves the smallest active rectifier with a compact area of 0.18 mm^2. The measured power consumption of the chip is 0.57 μW. The SSHSC rectifier has the highest output power enhancement of 7.58× compared to a conventional FBR. This work also has the smallest volume for the off-chip components compared with

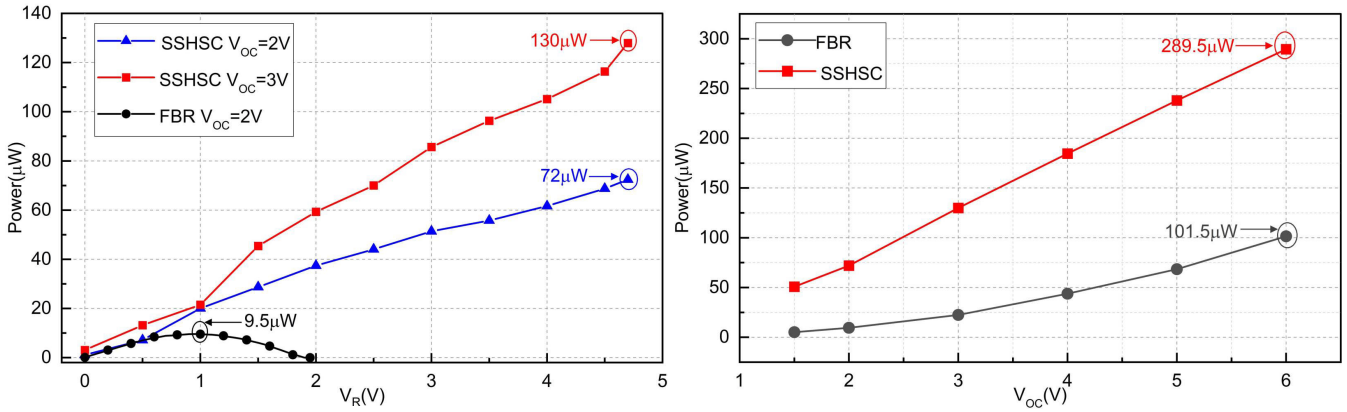

Fig. 15. Measured output power of the proposed SSHSC rectifier and an FBR for output voltage V_R varying between 0 and 4.75 V (left) and open-circuit voltage V_{OC} varying between 1.5 and 6 V (right) with load capacitors 10, 10, and 3.3 μF.

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUS WORK

	ISSCC'16 [5]	JSSC'17 [2]	JSSC'17 [10]	ISSCC'19 [3]	JSSC'19 [11]	JSSC'22 [6]	**This work**
Technology (μm)	0.35	0.35	0.18	0.18	0.18	0.18	**0.18**
Technique	P-SSHI	SSHC	FCR	SPFCR	SSHI	Inductive	**SSHSC**
PT type	Mide-V21BL	Mide-V21BL	P5A4E	PPA1021	PPA1021/1022	PPA1021	**Piezo-1803YB**
C_P	26nF	45nF	80pF	22nF	14/22	19nF	**22nF**
$V_{OC}(V)$	2.45	2.5	1*	-	1.5	1	**2-3**
Frequency(Hz)	134-229	92	110k	200	441/432	146	**130**
Dimension (mm^2)	1.3	2.9	1.73	0.2	0.54	1-3.3	**0.18**
Power consumption (μW)	-	1.7	8.5	4	2	0.75	**0.57**
Flipping efficiency	89%	80%	85%	84%	89.5%	69%	**78%**
Output power(μW)@V_{OC}(V)	21.4@1.25	161.8@2.5	50.2@1	64@0.19g	100-120@2	10.2@1	**130@3**
P_{IC}/P_{FBR}	4.4×	2.7×-9.7×	4.83×	6.5×	4.48×	3.68×	**7.58×**
Flipping efficiency	89%	78.5%	85%	89%	89.5%	-	**78%**
Off-chip components	1Ind+2Cap+2Res	9Cap	1Cap	5Cap	1Ind+1Cap	1Ind+1Cap	**3Cap**

*Estimated value; -Not reported.

other SSHI or typical SSHC rectifiers, thanks to the proposed capacitor-sharing technique.

VI. CONCLUSION

Typical SSHI or SSHC rectifiers require an off-chip inductor or at least eight off-chip capacitors for PT voltage flipping when large-sized PTs are employed. Some fully integrated SSHC rectifiers are achieved using customized MEMS PTs with very small C_P at the sub-nF level, which does not provide sufficient power for IoT applications. This article proposes an SSHSC rectifier for general PT with large intrinsic capacitance. To eliminate the flying capacitors, the proposed rectifier employs three storage capacitors with a specific capacitance ratio (3:3:1), which are temporarily borrowed by the rectifier as flying capacitors for voltage-flipping operations. With the proposed capacitor-sharing technique, the measured voltage flipping efficiency achieves 78%, and the maximum output power is 289.5 μW with 7.58× maximum power enhancement. To regulate the output voltage for ultralow-power load devices, a switched-capacitor converter can be employed for voltage regulation in future work.

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Xinling Yue (Graduate Student Member, IEEE) is pursuing the Ph.D. degree in microelectronics with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands.

She joined the Electronic Instrumentation Laboratory, Delft University of Technology, in December 2020. Her current research interests are energy-efficient power management integrated circuits and systems, which include energy harvesting, ac/dc rectifiers, dc/dc converters, and maximum power point tracking techniques.

Ms. Yue received the Best Student Paper Award at the 2022 IEEE International Conference on Electronics Circuits and Systems (ICECS), Student Travel Grant Awards at the 2022 IEEE International Symposium on Circuits and Systems (ISCAS), and 2023 International Solid-State Circuits Conference (ISSCC).

Sijun Du (Senior Member, IEEE) received the B.Eng. degree (Hons.) in electrical engineering from University Pierre and Marie Curie (UPMC), Paris, France, in 2011, and the M.Sc. degree (Hons.) in electrical and electronics engineering from Imperial College, London, U.K., in 2012, and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in January 2018.

He worked at the Laboratoire d'Informatique de Paris 6 (LIP6), University Pierre and Marie Curie, Paris, and then worked as a Digital IC Engineer in Shanghai, China, from 2012 to 2014. He was a Summer Engineer Intern at Qualcomm Technology Inc., San Diego, CA, USA, in 2016. He was a Visiting Scholar at the Department of Microelectronics, Fudan University, Shanghai, in 2018. He was a Postdoctoral Researcher at the Berkeley Wireless Research Center (BWRC), Department of Electrical Engineering and Computer Sciences (EECS), University of California, Berkeley, CA, USA, from 2018 to 2020. In 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, where he is currently an Assistant Professor. His current research is focused on energy-efficient integrated circuits and systems, including power management integrated circuits (PMIC), energy harvesting, wireless power transfer, and dc/dc converters used in the Internet-of-Things (IoT) wireless sensors, wearable electronics, biomedical devices, and microrobots.

Dr. Du received the Dutch Research Council (NWO) Talent Program-VENI grant in the 2021 round. He was a co-recipient of the Best Student Paper Award in IEEE ICECS 2022. He is a Technical Committee Member of the IEEE Power Electronics Society (PELS) and IEEE Circuits and Systems Society (CASS). He served as a Sub-Committee Chair of IEEE ICECS 2022, a Review Committee Member of IEEE ISCAS from 2021 to 2023, and a Committee Member of the 2023 IEEE ISSCC Student Research Preview (SRP).