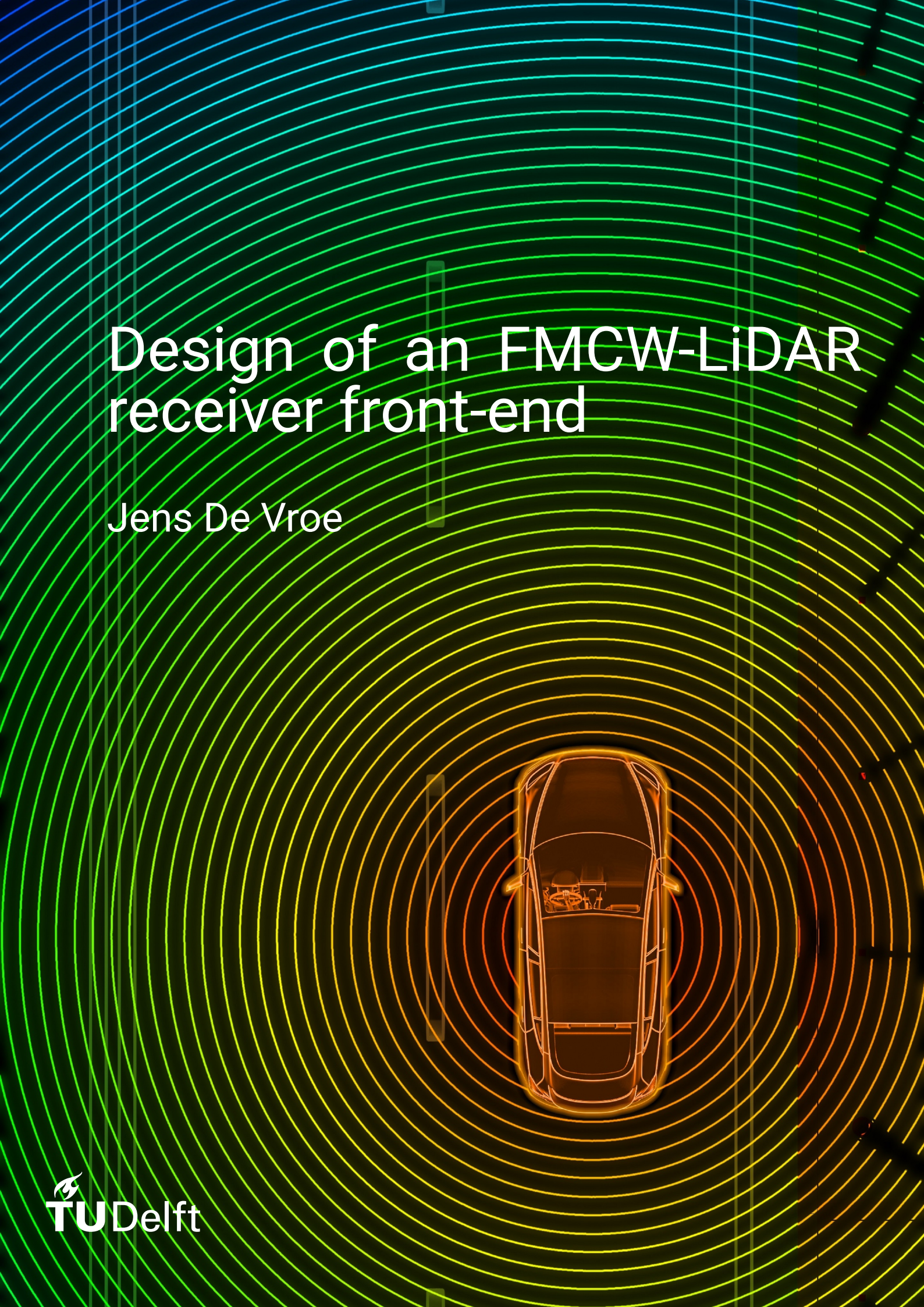
Design of an FMCW-LiDAR receiver front-end

Jens De Vroe



TU Delft

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by

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English Abstract

This work presents an analog front-end (AFE) signal processing chain for automotive FMCW LiDAR. The AFE consists of a high-gain transimpedance amplifier (TIA) followed by a gain-stage. The gain of the AFE is 103.2$dB\Omega$ at a bandwidth of 505MHz. Since the noise of FMCW-LiDAR systems is dominated by the shot noise of the local oscillator (LO), the AFE is noise matched to the optical system. It has an input-referred noise of 13$pA/\sqrt{Hz}$ which is lower than the 16$pA/\sqrt{Hz}$ generated by the optical system. The signal chain is designed to amplify the small single-ended photo current and convert it into a differential output voltage between 7mVpk and 125mVpk that is adequate for digitisation by an ADC. An SFDR=46.4dB is maintained to mitigate the generation of spurious tones, which will cause false object detections. The AFE circuits are sufficiently linear to ensure that such tones are below the noise floor. The signal path is AC-coupled to ensure that the balanced photodetector does not compromise the bias currents of the input stage. An external coupling capacitor defines a 1MHz high pass corner. The AFE was implemented in 0.13m CMOS technology and occupies 1160 m x 585 m including all supporting circuitry. With a 1.5V power supply, the total power dissipation is 250mW including the ADC-driver. The project was finalised by integrating the AFE with an ADC and the required support circuitry into a full ASIC for use as a building block in LiDAR systems.

Nederlands Abstract

Het onderwerp van deze thesis is een analoge front-end (AFE) voor automotive FMCW-LiDAR toepassingen. De AFE bestaat uit een transimpedantievoorversterker (TIA) gevolgd door een extra versterkerstrap. De versterkers hebben een totale versterking van 103.2$dB\Omega$ met een bandbreedte van 505MHz. In FMCW-LiDAR systemen is de shot noise van de local oscillator (LO) dominant, de AFE is ontworpen zodat een noise match met het optische systeem wordt verkregen. De AFE behaalt een maximale equivalente ingangsruis van 13$pA/\sqrt{Hz}$ hetgeen lager is dan de 16$pA/\sqrt{Hz}$ die gegenereerd wordt vanuit het optische gedeelte. Het totale signaalverwerkingspad van de AFE versterkt de kleine fotostromen afkomstig van de photodetector tot een signaal tussen 7mV_{pk} en 125mV_{pk}. De amplitude van deze signalen is voldoende groot om gedigitaliseerd te kunnen worden door een ADC. De AFE heeft een SFDR=46.4dB, dit vermijdt dat het signaalverwerkingspad spectrale onzuiverheden zou vertonen die bijdragen tot een foutieve objectdetectie. De circuits zijn voldoende lineair zodat spectrale onzuiverheden voldoende onderdrukt worden en deze verdwijnen in de ruisvloer. Het systeem heeft een AC-gekoppeld signaalpad zodat de bias van de ingangstrap niet wordt verstoord door offset stromen van de gebalanceerde photodiodes. Een externe koppelcondensator is aangewezen zodat een hoogdoorlaatkarakteristiek met een kantelfrequentie van 1MHz wordt verkregen. Alle circuits zijn geïmplementeerd in 0.13 μm CMOS technologie. In combinatie met alle ondersteunende schakelingen meet de AFE 1160 μm x 585 μm. De circuits worden van een 1.5V voeding voorzien en dissiperen 250mW, inclusief een ADC-driver. Naderhand is de AFE geïntegreerd in een ASIC samen met een ADC en de nodige ondersteunende circuits zodat het geheel kan gebruikt worden als bouwsteen in LiDAR systemen.

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Chapter 1

Introduction

In this introductory chapter, the background and a brief history and overview of autonomous driving is given. Furthermore the LiDAR as a sensor is situated within the concept of self-driving vehicles. Finally the project goal and research question are addressed.

1.1 Introduction & background

Ever since the invention of the automobile around the turn of the 19th century engineers have been looking for solutions to automate driving by replacing the driver with a machine. Throughout the 20th century efforts took place towards remote controlled or self-driving cars. The first big leap in self driving vehicles was taken in the 1980's when Ernst Dickmanns and his team at the Bundeswehr University Munich developed a robotic van equipped with cameras which was capable of autonomous driving by means of computer vision [10]. At the same time the United States had a DARPA-funded project developing an ALV (Autonomous Land Vehicle) accomplishing the same goals [36]. Through the 1990's further research was conducted on these technologies. During the 2000's the 2005 DARPA Grand Challenge boosted developments in autonomous driving significantly [46] [38]. From 2005 onwards car manufacturers have shown increasing interest in the development of autonomous vehicles. Additionally, companies typically involved in electronics and computing technology have taken an interest in the topic. The combination of these industry interests has caused an exponential increase in advancements in the field of autonomous driving over the last decade.

The self-driving cars that are being developed these days require a combination of a broad set of technologies. These technologies enable the vehicle to perceive its environment or 'see', process the sensed data and compute the desired course of action or 'think' and finally actuate the vehicle controls or 'drive' in a similar way humans would. Figure 1.1 shows the general overview of the autonomous vehicle data pipeline. The advancements in semiconductor technologies and microelectronics have played a significant role in the development of this new era of motoring [37].

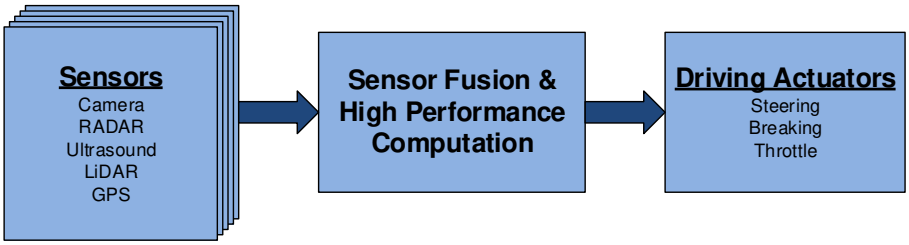


Figure 1.1: Autonomous vehicle information pipeline

In order to make self-driving or autonomous vehicles possible, the first step is to develop a reliable set of sensors such that the vehicle can perceive its environment. The accuracy and precision of these sensors is vital for the creation of reliable data. This data will in turn be used as input to the self-driving algorithms. Figure 1.1 shows that multiple sensors are used to capture the required data. Each of these different types of sensors uses different underlying technologies and therefore comes with its own set of advantages and disadvantages. Table 1.1 shows a qualitative comparison between 3 major technologies. From this table it becomes clear that the different sensors are

	Camera	**RADAR**	**LiDAR**	**Autonomous Requirement**
Object Detection	M	H	H	H
Object Classification	H	M	L	H
Close-Proximity Detection	M	H	L	H
Speed Detection	L	H	M	H
Lane Detection	H	L	L	H
Traffic Sign Recognition	H	L	L	H
Range	H	H	M	Full Range
Work in Rain/Fog/Snow	L	H	M	H
Work in Bright light	M	H	H	H
Work in Low light	L	H	H	H
Size	Small	Small	Medium	Mix
Cost	L	M	H	Mix

Table 1.1: Qualitative comparison of different ADAS sensors [5] (H = High, M = Medium, L = Low)

complementary rather than competing technologies. In self-driving environments these sensors will for example be responsible for detecting obstacles. As it can be seen from table 1.1 according to lighting and weather conditions not every sensor performs equally well. To compensate for the individual shortcomings data from multiple sensors will be combined. This way obstacles not detected by one sensor can still be 'seen' by the other sensors.

The LiDAR sensor bridges the gap between cameras and RADARs. For example, Cameras are able to image the environment at close distances and the data collected can be used for object detection and recognition. RADARs have the capability to detect objects at further distances but the acquired data cannot easily be used for object recognition. However, LiDAR would be able to acquire a 3D image of the environment and perform object detection and recognition at distances shorter than the RADAR but longer than the camera. A second advantage is that each sensor type degrades in different ways and under different conditions. For example, in dark environments the camera might suffer performance degradation while LiDAR and RADAR do not suffer from this. In adverse weather conditions (rain, snow) visibility is limited, as a result cameras and LiDAR's are affected more than RADAR, which will provide the best source of data for the situation. It is clear that LiDAR has its place as a robust imaging tool to make autonomous driving possible.

1.2 Goal & Research question

The goal of this project is to develop a custom designed analog front-end (AFE) for an automotive FMCW-LiDAR. The project starts with the extraction of the requirements from the mathematical models given by the system design team. To accomplish this, the study, simulation and extension of the existing system models with the electrical building blocks is required. Once the requirements are known, the appropriate circuit architectures can be chosen. With the architecture fixed, the circuits can be implemented and simulated. The finalisation of the project is the integration of the

AFE with an ADC design and a top-level simulation and verification as a collaborative effort. The ADC-design is not included in the scope of this project. A concise formulation of the research question is as follows:

Given a system level FMCW-LiDAR specification,
how can a custom AFE be designed ?

1.3 Structure of the Thesis

In Chapter 2 a short overview of the important principles of LiDAR for this work is given including the illumination and detection schemes. Furthermore, the LiDAR range equation and the related SNR are discussed. Chapter 3 gives an overview of the optical LiDAR system used, the specifications and the measurement principles. Using these system level specifications, the electrical specifications are derived. Chapter 4 uses the specifications of chapter 3 to develop a signal chain architecture for the electrical system. In this chapter specifications of each of the circuit blocks are derived. Chapter 5 implements the signal chain architecture. Chapter 6 discusses the integration of the AFE into a larger ASIC that includes an ADC and other support circuitry. The design of the ADC is not a part of this work. Finally Chapter 7 concludes this work with a summary and conclusions of this work.

Chapter 2

LiDAR

In this chapter, the concept of LiDAR is explained along with background information on the types of LiDAR classified by their illumination scheme and detection method. In a third section, the LiDAR-range equation is discussed along with the assumptions made for the application at hand. A fourth section compares the expected SNR for a direct detection system versus a coherent detection system. Lastly, the key performance metrics for the application at hand are discussed.

2.1 What is LiDAR

LiDAR is the acronym for **Li**ght **D**etection **A**nd **R**anging. Similar to RADAR or SONAR, LiDAR is a method used to measure distances to a certain object by means of LASER light. Where RADAR uses radio waves and SONAR uses sound waves, LiDAR uses light. Figure 2.1 shows the main LiDAR principle. A LASER light source (for example a LASER diode) transmits a laser beam towards an object, the object reflects the light and an optical receiver (for example a photodiode) captures the reflected light. By measuring the time the light needs to travel $(t_3 - t_1)$ to the object and reflect, the distance (r) to the object can be determined [7] [31]. The round trip time $(t_3 - t_1)$ is called the time of flight (TOF).

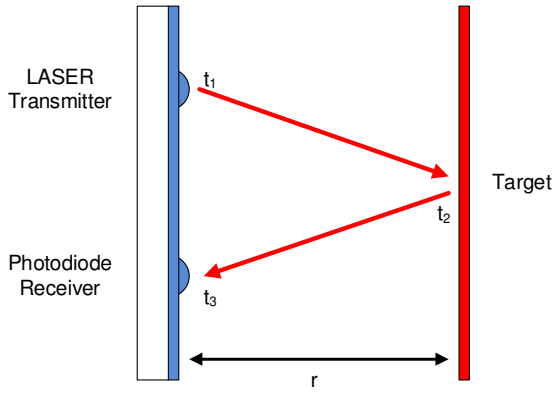


Figure 2.1: LiDAR basic Principle

Since the speed of light is a known constant, the distance can be calculated by measuring the time of flight. Equation 2.1 describes this relationship [7] [6] [28].

$$r = \frac{c \cdot \Delta t}{2} \qquad \text{where} \qquad \Delta t = (t_3 - t_1) \tag{2.1}$$

In formula 2.1, r is the distance to be measured and is the distance between the LiDAR and the target. c denotes the speed of light, Δt the time of flight.

2.2 The LiDAR range equation & reflected power

The LiDAR range equation describes the relation between the transmitted power and the received reflected power. This equation makes it possible to estimate the input power to the LiDAR receiver. In the following sections, the LiDAR range equation is discussed. First in its standard form and afterwards simplifications and non-idealities for the application at hand are implemented and the power vs. distance characteristic is simulated.

In any LiDAR system the power received by the photodetector is a fuction of a multitude of factors depending on optical and environmental parameters. Equation 2.2 shows what is known as the general form of the LiDAR range equation [15] [28] [9].

$$P_r = \left[\frac{4P_t K L_{A-tx-o} L_{tx}}{\pi\varphi^2 r_{tx-o}^2}\right] \cdot \left[\Gamma\right] \cdot \left[\frac{A L_{A-o-rx} L_{rx}}{4\pi r_{o-rx}^2}\right] \tag{2.2}$$

where:

P_r = Received signal power $[W]$
P_t = Transmitted power, LASER power $[W]$
K = Beam profile function
L_{A-tx-o} = Atmospheric loss from LASER to object/target $[\%]$
L_{tx} = Transmitter optical efficiency $[\%]$
φ = Transmitter Beamwidth $[radians]$
r_{tx-o} = Distance from transmitter to object $[m]$
Γ = LiDAR Cross Section (LCS) $[m^2]$
A = Receiver aperture $[m^2]$
L_{A-o-rx} = Atmospheric loss from object/target to receiver $[\%]$
L_{rx} = Receiver optical efficiency $[\%]$
r_{o-rx} = Distance from object/target to receiver$[m]$

This equation consists of three factors. The first factor describes the propagation of the LASER light from source to destination including losses. The second factor is the LiDAR Cross Section (LCS) [16] which models how the LASER light is reflected from the object. The third factor describes the propagation and collection of the reflected light.

In automotive applications it can be assumed that the LiDAR system is monostatic. In other words the transmitter and receiver are in the same location[14] [28]. Two simplifications are possible. Firstly the atmospheric losses are equal $L_{A-tx-o} = L_{A-o-rx} = L_A$ since the transmitted and reflected power travel though the same channel. Secondly, the distances from the transmitter to the object and vice-versa are equal ($r_{tx-o} = r_{o-tx} = r$).

The LiDAR cross section (LCS) describes how the light is reflected from the object. It is considered as $\Gamma = \rho_\pi \pi \varphi^2 r^2$ [16] (appendix A) and reveals the dependence on the target reflectivity ρ_π.

The non-idealities caused by the optical beam properties are included as the beam profile K. These non-idealities cause the flattening of the received power as shwon in figure 2.2 when objects are located close to the LiDAR. This is an effect that follows from beam optics and is caused by the fact that the laser beam does not have a constant power across its diameter. The LASER is assumed to have a Gaussian beam profile [14] [42], (appendix B).

Using the assumptions above, equation 2.2 can be simplified to the particular form presented in equation 2.3 [15]. In this function, the first factor models the power returned, the second factor models the losses and the third factor models the close range or Rayleigh range effects.

$$P_r = \left[P_t \rho_\pi \frac{A}{4\pi r^2}\right] \cdot \left[L_A^2 L_{tx} L_{rx}\right] \cdot \left[\frac{1}{1+\left[\frac{\pi w_0^2}{\lambda r}\right]^2}\right] \tag{2.3}$$

In equation 2.3 ρ_π denotes the reflection coefficient of the object, w_0 indicates the beam waist, defined as the radius of the beam at the aperture [42]. Furthermore λ denotes the wavelength of the LASER used.

The derived range equation is plotted in figure 2.2. The range equation with close range effects (blue) and without close range effects (orange) is plotted on a log-log scale to demonstrate the flattening effect. In figure 2.2 z_r denotes the Rayleigh length of the beam [42], appendix B.

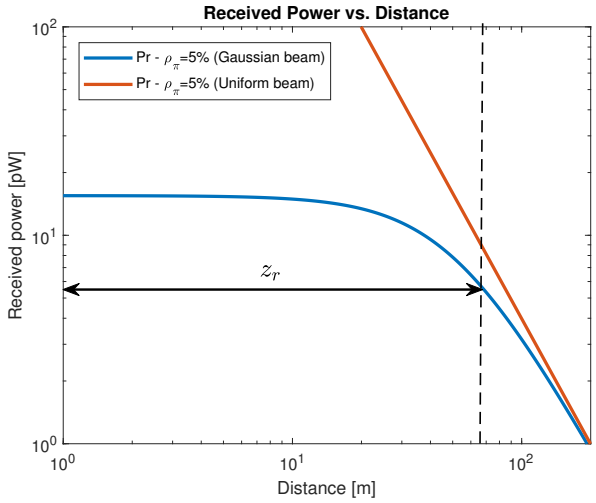


Figure 2.2: LiDAR Received power (P_r) vs. distance (r) with ($\rho_\pi = 5\%, P_t = 100mW, L_A = L_{tx} = L_{rx} = 1, w_0 = 5mm, \lambda = 1550nm$)

Figure 2.2 shows that for an idealised beam (orange) the r^2 dependence is clearly visible. The plot using non-ideal beam properties (blue), shows a flat curve, up to the Rayleigh length before the r^2 behaviour becomes dominant. Flattening of the reflected power as a consequence of the Rayleigh range effects will cause the reflected signal to have a limited dynamic range.

2.3 LiDAR properties

LiDAR's can be classified in a multitude of ways. They can be classified by, but not limited to, the type of measurement made, the type of LASER and wavelength used, the used illumination technique of the target, the detection technique, the modulation used, the functions performed etc. [14]. Classifying LiDAR according to one of its properties hardly provides a complete description, therefore in this section only the illumination and modulation scheme used in this application of the LiDAR system at hand are mentioned. For a more complete overview the reader is referred to the existing literature [14] [9] [27] [28].

2.3.1 Illumination

The intended use of the system is a scanning LiDAR shown in figure 2.3b. In this system the LASER beam is physically moved from point to point within the Field Of View (FOV). Contrary to the simpler Flash LiDAR, shown in figure 2.3a, where the full FOV is illuminated at once, similar to the operating principle of a visible light camera. In a scanning system the LASER is coupled to a beam steering mechanism which is typically mechanical or more recently using solid state beamforming techniques [52] [48]. This has the capability to deflect the beam in the horizontal and vertical directions. In such a setup each point is illuminated separately, the reflected light is then captured by a single photosensitive element. The drawback of this technique is that positioning the beam takes time, as a result the framerate will be lower. However, it is capable of providing higher SNR [20] compared to a flash LiDAR setup.

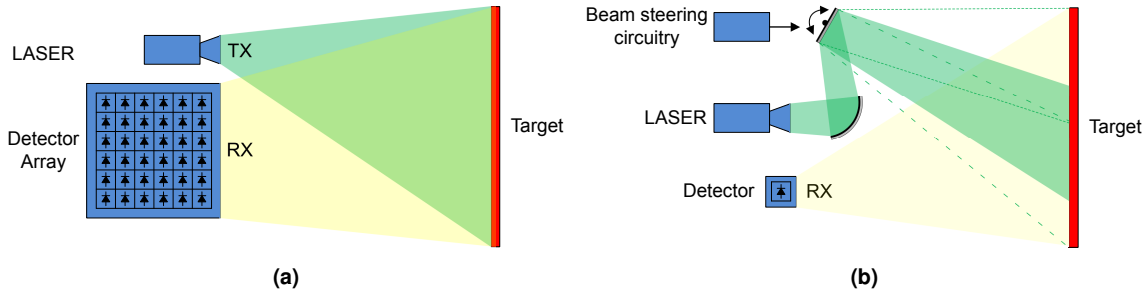


Figure 2.3: (a) Flash LiDAR, (b) Scanning LiDAR

2.3.2 Modulation

The scanning LiDAR illumination scheme is combined with a coherent detection modulator/demodulator scheme. Coherent LiDAR systems modulate the LASER's frequency or phase. The intensity of the LASER beam is kept constant. In this case the oscillation frequency of the LASER is modulated to create a frequency chirp, as shown in figure 2.4a. A Frequency Modulated Continues Wave (FMCW) system is obtained. The coherent detection is performed by using an interferometer which mixes the reflected waveform with the transmitted wave. The reflected wave experiences a delay with respect to the transmitted wave and when mixed, in the optical domain, it creates a beat frequency which is proportional to the ToF [20] [7]. Figure 2.4 shows such an FMCW-LiDAR receiver. The optical beat frequency is very low frequency compared to the LASER's oscillation frequency and falls within the bandwidth of standard CMOS processes.

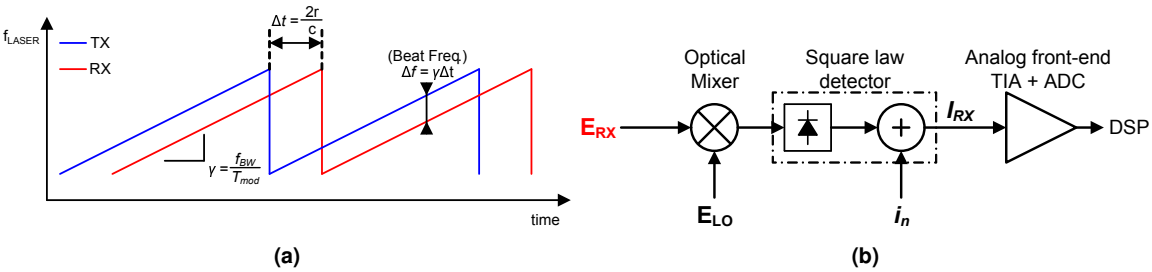


Figure 2.4: (a) FMCW-LiDAR frequency vs. time waveform, (b) high-level overview of a LiDAR employing coherent detection

In figure 2.4a Δt indicates the ToF, r indicates the distance to the target and c the speed of light. Furthermore γ represents the frequency slope and Δf indicates the beat frequency formed. In figure 2.4b E_{RX} represents the electric field of the received optical wave, E_{LO} represents the electric

field of the local oscillator (transmitted) optical wave. The noise added to the electrical system by the square-law detector is represented by i_n, I_{RX} represents the combination of signal and noise current at the input of the electrical signal chain.

The FMCW modulation is able to obtain better range resolution and precision compared to amplitude modulated (AMCW [30] or Pulsed LiDAR [7]). Because mixing happens in the optical domain, lower bandwidth electrical circuits can be used compared to the bandwidths needed for amplitude modulated or pulsed systems [7].

A second advantage of FMCW based systems is that the optical power of the LASER signal is kept constant which is preferable when silicon-photonic-based beam-steering mechanisms are used for scanning LiDARs such as in this application. For example, the large optical power used in pulsed LiDARs could exercise non-linear effects in the silicon photonics [7].

A third important advantage of an FMCW system is that it is more robust to environment conditions. The coherence of the transmitted and received signals through the mixing makes the system more selective for the reflected signal while rejecting background or ambient light. Additionally the optical mixing gain of the receiver obtains a better SNR.

2.4 LiDAR SNR

In the previous sections, the LiDAR principle, the range equation and the illumination and modulation/demodulation properties have been discussed. Using the range equation the reflected power can be calculated. In combination with the knowledge of the illumination and modulation schemes the equation for the system's SNR can be derived.

Using coherent detection, the reflected received signal power (P_r) is mixed with the local oscillator (P_{LO}) signal in the optical domain. Similar to mixing in the electrical domain, the signals created are the sum and difference frequencies. However at optical wavelengths the oscillations of the LASER and sum-frequencies are beyond the bandwidth of the photodetectors and only its magnitude will be detected, this shows up as a DC component. The difference frequency is however designed to fall within the photodetector's bandwidth and is detectable. The amplitude of this signal is $i_{out} = \rho_d \sqrt{2P_{LO}P_r}$ [27] [9] [28] [14]. The received signal power P_r experiences a gain by the LO power P_{LO}, an advantage over a direct detection system yielding a better SNR, described by equation 2.4 [27].

$$\begin{aligned} SNR &= \frac{i_{out}^2}{\sigma_n^2} = \frac{i_{out}^2}{\sigma_{ns}^2 + \sigma_{n-BG}^2 + \sigma_{n-DK}^2 + \sigma_{n-TH}^2} \\ &= \frac{2\rho_d^2 P_r P_{LO}}{2qB_w\left[\rho_d P_{LO} + \rho_d P_r + \rho_d P_{BG}\right] + 2qB_w i_{DK} + 4kTB_w/R_{TH}} \end{aligned} \tag{2.4}$$

where:

P_r = Received signal power $[W]$
P_L = Power of the local oscillator $[W]$
ρ_d = Photodetector responsivity $[A/W]$
σ_{ns}^2 = Shot noise caused by the incident light power $[A^2]$
σ_{n-BG}^2 = Shot noise caused by the background light power $[A^2]$
σ_{n-DK}^2 = Shot noise caused by the dark current of the detector $[A^2]$
σ_{n-TH}^2 = Thermal noise of the detector $[A^2]$
q = Unit charge of an electron $[C]$
k = Boltzmann's constant $[JK^{-1}]$
B_w = Bandwidth $[Hz]$

P_{BG} = Background light power $[W]$
i_{DK} = Photodetector dark current $[A]$
R_{TH} = Photodetector equivalent thermal noise resistance $[\Omega]$

Equation 2.4 formulates the SNR of the coherent detection system. The signal i_{out} is previously defined and is dependent on the modulation scheme. The noise consists of 4 terms where the first 2 terms, σ^2_{ns} and σ^2_{n-BG} indicate the shot noise induced by the incident light and the background light respectively. A well-designed coherent detection system is designed such that the LO-power causes sufficiently high signal gain and ensures that its shot noise becomes dominant [27]. This renders effect of background light negligible and causes the system's SNR to be fixed. The result is an independence from environmental parameters like background light, which is not the case for direct detection systems where a varying background light causes a varying SNR (under the assumption that the shot noise of the reflected power is non-dominant). The last 2 terms of the noise are σ^2_{n-DK} and σ^2_{n-TH} and indicate the dark current shot noise and thermal noise, respectively. These parameters are inherent to the physics of the photo detector and cannot easily be changed.
Considering an LO shot noise dominated system as described earlier, simplifications to equation 2.4 can be made by neglecting σ^2_{n-BG}, σ^2_{n-DK} and σ^2_{n-TH}. This yields equation 2.5.

$$SNR = \frac{\rho_d P_r P_{LO}}{qB_w \left[P_{LO} + P_r\right]} \tag{2.5}$$

In equation 2.5 it can be estimated that $\left[P_{LO} + P_r\right] \approx P_r$ because $P_{LO} \gg P_r$. The result is shown in equation 2.6 [27] [20]. This simplification reveals the fundamental lower limit of the SNR for a shot noise dominated system.

$$SNR_{ns-limit} = \frac{\rho_d P_r}{qB_w} \tag{2.6}$$

The SNR of such a system is only dependent on the reflected power and the bandwidth. The minimum SNR can be determined given the smallest reflected power through the range equation. Conversely given a certain SNR detection threshold, the minimum reflected power, and through the range equation the required LASER power.

2.5 LiDAR Summary

In this chapter the principles of LiDAR were described focussed on FMCW-LiDAR. First the main LiDAR principle is introduced, next the LiDAR range equation was described relating the transmitted and received power. Furthermore the LiDAR illumination and modulation techniques were introduced. In the last section, the 3 topics were combined to determine the SNR and illustrate the improvement in SNR over direct detection LiDAR. In the next chapter these concepts will be used to analyse the operation of a Coherent Detection FMCW (Frequency Modulated Continuous Wave) LiDAR system more closely.

Chapter 3

FMCW-LiDAR

In this chapter, the design of an FMCW-LiDAR (Frequency Modulated Continuous Wave LiDAR) system will be discussed. First, the optical system and its waveforms are discussed, as well as how they are converted into electrical signals. In the second part, an explanation is given of how the measurements are performed together with a discussion of experimental limitations. In the third part, knowledge about the system is combined with the knowledge about the measurements, and with this information the complete system is modelled and the electrical specifications of the FMCW-system are determined.

3.1 FMCW-LiDAR system operation

In the following sections the specific FMCW-LiDAR system used is introduced and its interferometric operation is analysed. The output current of the system is derived by setting up the equations for the optical waves and combining them according to the path of the optical wave. Following that the balanced detection and advantages/disadvantages are discussed.

3.1.1 FMCW-LiDAR system

The LiDAR system as intended for use in automotive applications is illustrated as a block diagram in figure 3.1. The optical system will be implemented on a silicon photonics chip, whereas the electrical system will be implemented in CMOS technology. The system will be part of a scanning LiDAR, the beam-steering is out of the scope of this document. In the following paragraphs the analysis of the optical system is done in order to derive the relevant electrical signal properties.

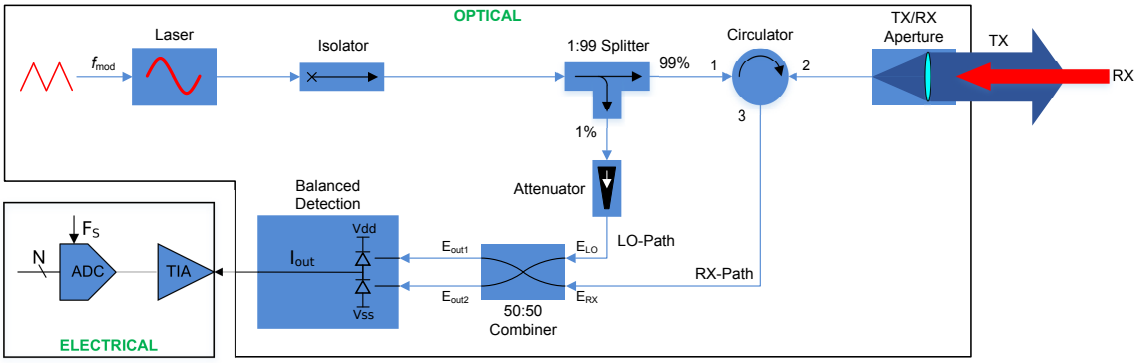


Figure 3.1: FMCW-LiDAR opto-electrical setup

The opto-electrical system is shown in figure 3.1. In order to create FMCW waveforms, a frequency

tunable LASER source is required. The modulated light wave is sent through an isolator in order to avoid reflections from back-propagating into the LASER. The signal is then carried into a 1:99 splitter. This transmits 99% of the power, while 1% is sent to the LO-branch for coherent detection. The majority of the power is sent out of the optical system via a circulator, and then transmitted into free space. The circulator's isolating properties [32] make it possible to use the same aperture to transmit and receive. The received beam is diverted into a separate path without the risk of it back-propagating into the transmit optics. The LO-wave and received wave are fed into a 50:50 combiner which combines both waveforms into a balanced optical signal that in turn is converted to an electrical current by a balanced photodiode detector.

The system can be seen as a Mach Zehnder interferometer (MZI) [51]. The 1:99 splitter and the 50:50 combiner fulfill the same function as the semi-reflective mirrors of a MZI. The LO-branch acts as the reference branch of the MZI and does not experience any time delay, the TX-branch is the measurement branch in which the waves experience a ToF due to the distance of the target object. The ToF experienced causes a phase shift in the received wave, and combining it with the reference wave of the LO results in interfering light patterns projected onto the balanced photodiodes. Each photodiode receives 50% of the power and waves $\vec{E_{out2}}$ and $\vec{E_{out3}}$ are 180° out of phase.

The interfering light patterns perform optical down conversion and create a measurable difference frequency within the bandwidth of the photodetectors. The balanced detector combines the signals measured by both photodiodes into a single output current. By using an appropriate transimpedance amplifier (TIA) and analog to digital converter (ADC) the signals can be digitised and used to perform object detection.

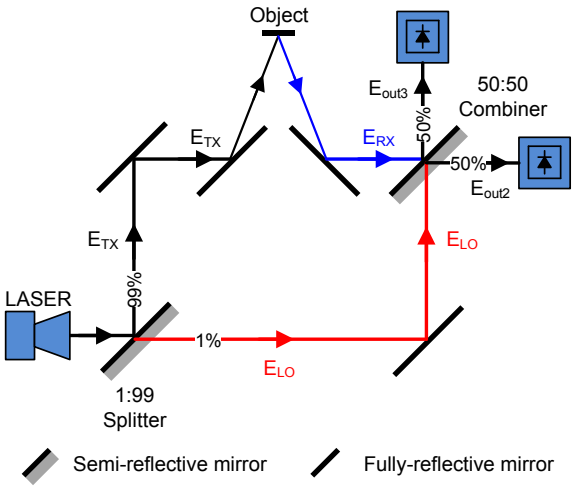


Figure 3.2: FMCW-LiDAR Mach Zehnder interferometer equivalent

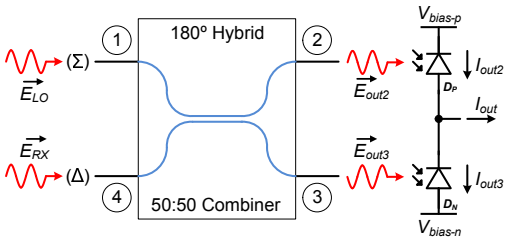
3.1.2 FMCW-LiDAR output signal

The output signal properties determine the specifications for the subsequent electronics. To obtain these, the opto-electrical receiver chain is modeled. The transmitted signal is a frequency modulated optical wave, the received reflected signal is an attenuated and time-delayed copy. The magnitude is determined by the LiDAR range equation while the time delay is equal to the ToF. These waves are described in equation 3.1.

$$\begin{aligned} \vec{E_{RX}} &= E_R cos(\omega_R t) \\ \vec{E_{LO}} &= E_L cos(\omega_{LO} t) \end{aligned} \tag{3.1}$$

In equation 3.1, $\vec{E_{RX}}$ and $\vec{E_{LO}}$ describe the reflected and transmitted waves respectively. E_R and E_R indicate the electrical field magnitudes and ω_R and ω_{LO} the angular velocities.

Both waves are applied to the 50:50 optical combiner as shown in figure 3.3. This component passively combines both waves and performs the same function as a 2x2 coupler or a 180° hybrid as is commonly used in RF-electronics [32]. Applying signals to input ports 1 and 2 will result in $1/2$ of each of the input powers combined at ports 2 and 3, where port 2 contains the sum of the inputs and port 3 the difference as described by equation 3.2.



$$\vec{E_{out2}} = \frac{-j}{\sqrt{2}}\left[\vec{E_{RX}} + \vec{E_{LO}}\right]$$
$$\vec{E_{out3}} = \frac{-j}{\sqrt{2}}\left[\vec{E_{RX}} - \vec{E_{LO}}\right] \tag{3.2}$$

Figure 3.3: 50:50 coupler and balanced detector

The outputs of the combiner form a balanced light wave which is incident to the balanced photodetector. By substituting 3.1 into 3.2 these waves can be derived. The photodiodes are sensitive to incident optical power, the power is related to its electric field by $P = |\vec{E}|^2$ or $P = E^2/2$. The optical power is converted into current over diode's responsivity ρ_d. Applying these conditions yields photocurrents I_{out2} and I_{out3} as described by equations 3.3 and 3.4.

$$\begin{aligned} I_{out2}(t) &= \rho_D \frac{1}{2}\left[\vec{E_{RX}} + \vec{E_{LO}}\right]^2 = \rho_D \frac{1}{2}\left[\vec{E_{RX}}^2 + 2E_R E_L cos(\omega_r t)cos(\omega_l t) + \vec{E_{LO}}^2\right] \\ &= \rho_D \frac{1}{2}\left[P_R + 2\sqrt{P_R P_L}\left[cos\left[(\omega_r - \omega_l)t\right] + cos\left[(\omega_r + \omega_l)t\right]\right] + P_L\right] \end{aligned} \tag{3.3}$$

$$\begin{aligned} I_{out3}(t) &= \rho_D \frac{1}{2}\left[\vec{E_{RX}} - \vec{E_{LO}}\right]^2 = \rho_D \frac{1}{2}\left[\vec{E_{RX}}^2 + 2E_R E_L cos(\omega_r t)cos(\omega_l t) + \vec{E_{LO}}^2\right] \\ &= \rho_D \frac{1}{2}\left[P_R - 2\sqrt{P_R P_L}\left[cos\left[(\omega_r - \omega_l)t\right] + cos\left[(\omega_r + \omega_l)t\right]\right] + P_L\right] \end{aligned} \tag{3.4}$$

In equation 3.3 and 3.4 the light waves $\vec{E_{RX}}^2$ and $\vec{E_{LO}}^2$ as well as the resulting sum terms are at or beyond the LASER frequency, well beyond the bandwidth of the photodiodes. These will result in a common mode DC-current and cancel in the balanced detector due to having opposite signs. The difference frequency is designed to fall within the photodiode's bandwidth and carries ToF or distance information in the form of a beat frequency Δf. Substituting I_{out2} and I_{out3} into equation 3.5 yields the final output current of the balanced detector.

$$\begin{aligned} I_{out}(t) &= I_{out2}(t) - I_{out3}(t) \\ I_{out}(t) &= 2\rho_d \sqrt{P_R P_L} cos\left[(\omega_r - \omega_l)t\right] \end{aligned} \tag{3.5}$$

3.1.3 PiN Photodiode & Balanced detector

The conversion from optical to electrical signals is facilitated by a balanced photodetector implemented on the silicon photonics chip. The diodes used are germanium PiN diodes, part of the integrated photonics process library. Table 3.1 shows the typical specifications for these devices.

Parameter	Value	Unit	Description
ρ_{d-min}	0.8	$[A/W]$	Minimum responsivity at $1550nm$
B_{w-min}	25	$[GHz]$	Minimum Bandwidth ($V_R = 1V$)
B_{w-min}	30	$[GHz]$	Minimum Bandwidth ($V_R = 2V$)
I_{dark}	20	$[nA]$	Dark current for $V_R = 1V$
I_{dark}	200	$[nA]$	Dark current for $V_R = 2V$

Table 3.1: Specifications for the PiN Photodiodes germanium photodiode for operation at a 1550nm wavelength

An important parameter is the photodiode's responsivity ρ_d, which determines the response of the detector to an incident light wave. It is a process parameter and is function of the light's wavelength and the diode's quantum efficiency [47]. For the application at hand only the responsivity at the LASER wavelength was taken into account. A second parameter is the parasitic capacitance C_{pd}, it is an important parameter for the design of the subsequent circuitry. Although this parameter is not given in the device's datasheet, it is estimated to be 0.5pF.

The balanced detector used in previous derivations is considered to be ideal. However mismatches in responsivity between D_p and D_n or in the optical chain might exist. This will cause an imbalance with limited common mode rejection and offset output currents as a result. Typical mismatches between detectors are in the range of 0.5-1dB [13]. Equation 3.6 calculates a mismatch current based on these typical values.

$$I_{mb} = 10log\left[\frac{\rho_d(1+\alpha)}{\rho_d(1-\alpha)}\right] = \mathbf{1dB} \rightarrow \alpha \approx 11.5\% \tag{3.6}$$

$$I_{offset} = \alpha\rho_d P_L \approx 100\mu A$$

In equation 3.6 Imb is the photodiode mismatch in dB and α is the mismatch as a percentage. In this example pertaining to the system at hand only responsivity mismatch is considered because details on the optical system are not yet available. In equation a typical $1dB$ mismatch and $1mW$ LO-power is assumed.

3.2 FMCW-LiDAR measurements

Using the system as pictured in figure 3.1, the FMCW-LiDAR principles and measurement objectives are explained in this section. First the range detection will be discussed, afterwards the velocity measurement is added. Furthermore the spectral measurement of the beat frequency is discussed.

3.2.1 Range measurement

FMCW LiDAR waveforms are created by linearly modulating the LASER frequency in function of time. Figure 3.4 illustrates this and displays the frequencies of the local oscillator waveform E_{LO} (copy of the transmitted waveform) and reflected waveform E_{RX} in function of time.

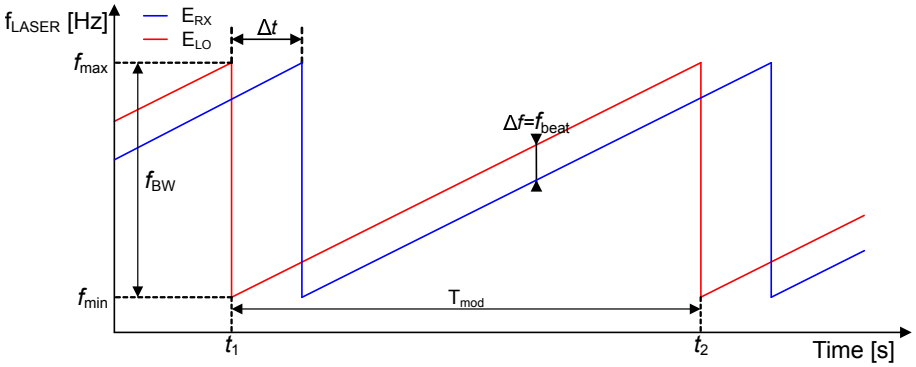


Figure 3.4: FMCW-LiDAR frequency vs. time

In figure 3.4 the transmitted light reaches the receiver after a round trip delay (ToF) indicated by Δt. The linear modulation causes the instantaneous frequency difference Δf to be proportional to

the time delay, $\Delta f = \gamma \cdot \Delta t$. The slope of the modulation is a constant defined by $\gamma = f_{BW}/T_{mod}$, where f_{BW} is the modulation bandwidth of the LASER and T_{mod} the chirp rate. Combining these constants with the ToF from equation 2.1 in section 2.1 yields a distance measurement based on the difference or beat frequency:

$$r = \Delta f \cdot \frac{c}{2\gamma} = \Delta f \cdot \frac{cT_{mod}}{2f_{BW}} \tag{3.7}$$

In equation 3.7 r is the distance measured, c is the speed of light. The other parameters are defined previously. Given the modulation parameters and maximum distance r_{max} the equation can be used to determine the maximum frequency difference $\Delta f_{max} = BW_{electrical-range}$ that can be present in the system. This also defines the upper limit for the system's bandwidth:

$$BW_{electrical-range} = \frac{2r_{max}}{c} \cdot \frac{f_{BW}}{T_{mod}} \tag{3.8}$$

3.2.2 Velocity Measurement

The advantages of using coherent LiDAR is that it is possible to simultaneously measure the range and velocity of an object. This is of interest in automotive LiDAR. The relative movement of LiDAR and object causes a Doppler shift ($\Delta f_{doppler}$) in the frequency of the received signal. The frequency shift is reflected in the beat frequency and can be measured together with the range information. When the LiDAR and the object are moving towards each other, the received frequency is increased, when they move away from each other the frequency decreases.

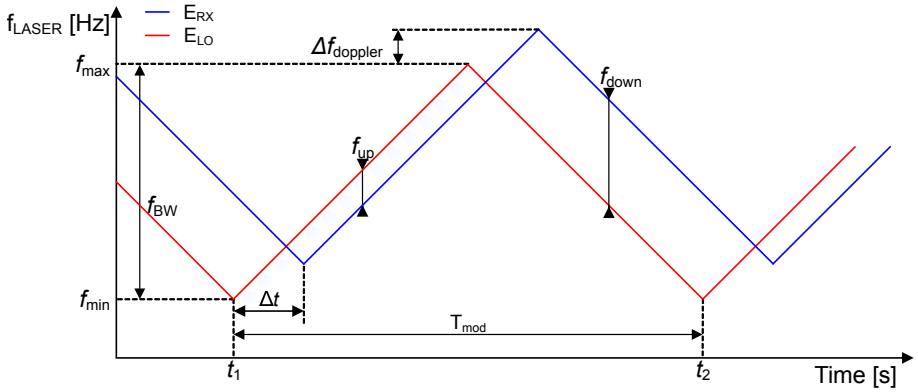


Figure 3.5: FMCW-LiDAR frequency vs. time, using a triangular modulation wave for velocity sensing using the Doppler effect, object and LiDAR moving towards each other

To accomplish range and velocity measurements the modulation shape must change to a triangular chirp as shown in figure 3.5. The modulation parameter γ is adjusted accordingly. With this new modulation shape two beat frequency measurements are performed, one during the up-ramp and one during the down-ramp. Considering an example where the LiDAR and object are moving towards each other, a decreasing beat frequency is measured during the up-ramp. Conversely an increasing beat frequency is measured during the down-ramp. The opposite is true when the LiDAR and the object move away from each other.

Untangling the range and velocity component can be accomplished by making the sum and difference of the frequency measured during the up-ramp and the down ramp. This is shown in equation 3.9.

$$\begin{aligned} f_{down} &= f_{beat} + \Delta f_{doppler} \\ f_{up} &= f_{beat} - \Delta f_{doppler} \end{aligned} \tag{3.9}$$

$$\begin{aligned} f_{down} + f_{up} &= 2f_{beat} && \text{(range frequency component)} \\ f_{down} - f_{up} &= 2\Delta f_{dopper} && \text{(velocity frequency component)} \end{aligned}$$

In equation 3.8 it was demonstrated how the LiDAR's system bandwidth relates to the required bandwidth for the receiving electronics. However with a Doppler shift present, the doppler frequency will be added or subtracted from the beat frequency due to the range, hence a higher bandwidth is needed. The worst case bandwidth requirement can be determined by adding the maximum obtainable Doppler component to equation 3.8, this is shown in equation 3.10.

$$BW_{electrical-doppler} = \frac{2r_{max}}{c} \cdot \frac{2f_{BW}}{T_{mod}} + \frac{|\Delta v_{max}|}{\lambda_{LASER}} \tag{3.10}$$

In equation 3.10 all parameters are previously defined. A clear separation between the contribution of the range and the velocity is visible. $|\Delta v_{max}|$ represents the absolute value of the maximum relative velocity between LiDAR and object, $|\Delta v_{max}| = |v_{LiDAR} - v_{object}|$. Negative velocities indicate a movement in the direction opposite to the LiDAR.

3.2.3 Measurement of the beat frequency

The beat frequency generated by the distance and velocity measurements can now be analysed by the subsequent DSP-system(s). Object detection algorithms make use the frequency spectrum to interpret the measurement data. The balanced photodetector output current is described by equation 3.5. Performing a Fourier transform yields equation 3.11.

$$I_{out}(\omega) = \frac{\rho_d \sqrt{2P_R P_L}}{2} \left[T_{meas} sinc\left(\frac{(\omega - \omega_{beat}) T_{meas}}{2} \right) + T_{meas} sinc\left(\frac{(\omega + \omega_{beat}) T_{meas}}{2} \right) \right] \tag{3.11}$$

In equation 3.11, $\omega_{beat} = \omega_r - \omega_t$ is the beat frequency to be measured. $T_{meas} = T_{mod}$ is the measurement time over which the FFT is taken. A fixed relation between the N-points in the FFT, T_{meas} and $f_s = 2BW_{electrical-doppler}$ exists. It will determine the FFT's frequency resolution (equation 3.12).

$$\Delta f_{FFT-bin} = \frac{2BW_{electrical-doppler}}{N} \tag{3.12}$$

The frequency resolution implies distance resolution. The range resolution Δr can be found by substituting $\Delta f_{FFT-bin}$ into equation 3.8. However for the LiDAR system the LASER modulation bandwidth is the limiting factor determining the resolution and precision. The maximum obtainable range resolution [7] Δr and precision [7] δr are determined as:

$$\Delta r_{min} = \frac{c}{2f_{BW}} \qquad \delta r \approx \frac{\Delta r_{min}}{\sqrt{SNR}} \tag{3.13}$$

Implementing an FFT frequency resolution that yields a larger range resolution than the system limitation is a waste of processing power. The LiDAR system has a tunable resolution [20] by tuning the chirp. Speed, resolution and precision trade-offs can be made without the need to change the system/electronics design.

The FFT analysis has the advantage of suppressing broadband signals by its processing gain (PG). Noise is present as a broadband signal and therefore the processing gain lowers the noise floor [41]. An FFT analysis can alternatively be seen as a bank of N-filters, where N is the number

of points in the FFT. Each of the filters has a bandwidth equal to the FFT binwidth $\Delta f_{FFT-bin}$. In the case of noise, the total noise power is divided over all the frequency bins resulting in a lower noise power per bin. The PG is described in equation 3.14.

$$PG[dB] = 10log\left(\frac{N}{2}\right) \tag{3.14}$$

In further analysis the PG is taken into account by considering $\Delta f_{FFT-bin}$ as the bandwidth for the determination of the SNR (equation 2.5). The lower noise floor in the FFT is beneficial for the algorithm that interprets the objects from the spectrum. The baseline algorithm used for this is CA-CFAR, its operating principle is analysed in appendix C. The algorithm requires a minimum SNR threshold for detection (SNR_{Th}) that corresponds with a certain probability of detection. A SNR value below the threshold will degrade the reliability of the system.

3.3 FMCW-LiDAR system specifications

The LiDAR system specifications are given in table 3.2. These represent the typical requirements for automotive LiDAR. Combined with the principles discussed in section 3.2 the electrical system specifications and LiDAR properties are derived.

Parameter	Value	Unit	Description
r_{min}	0.5	$[m]$	Minimum object distance
r_{max}	200	$[m]$	Maximum object distance
$\rho_{\pi-min}$	5	$[\%]$	Minimum object reflectivity
$\rho_{\pi-max}$	100	$[\%]$	Maximum object reflectivity
A	10	$[mm^2]$	Aperture cross sectional area
$v_{obj/LiDAR}$	200	$[km/h]$	Maximum relative speed at which any object or the LiDAR can be moving
f_{BW}	1.5	$[GHz]$	LASER modulation bandwidth - bandwidth over which the LASER is chirped
T_{mod}	10	$[\mu s]$	LASER modulation period - Period over which the laser frequency is chirped over its bandwidth f_{BW} - upramp and downramp
T_{up}	5	$[\mu s]$	LASER modulation period upramp
T_{down}	5	$[\mu s]$	LASER modulation period downramp
P_{LASER}	100	$[mW]$	LASER output power
λ_{LASER}	1550	$[nm]$	LASER wavelength
Detection Algorithm	-	-	CA-CFAR algorithm ($SNR_{th} \approx 15dB$)
Electronics tech.	-	-	TSMC - 0.13μm

Table 3.2: LiDAR system specifications

3.3.1 Electrical bandwidth

The bandwidth composition of the electrical system is determined by equation 3.8 and 3.10. Plugging in the minimum distance of $0.5m$ and maximum distance of $200m$ yields a bandwidth from $1MHz$ to $400MHz$ respectively. However this only takes into account the range, additional bandwidth is provisioned for the Doppler shift. The worst case scenario was considered where the LiDAR and target approach each other at the maximum speed and hence $\Delta v_{max} = 2v_{obj/LiDAR} = 400km/h$. This results in an additional $72MHz$ required for velocity measurements yielding a full $472MHz$ bandwidth. As a result the electronic bandwidth is set to $500MHz$.

3.3.2 Resolution, precision and samplerate

Using the given specifications equations 3.12 and 3.13, the frequency and range resolution are determined. The system specifications are chosen such that the LASER bandwidth, the measurement time, and the samplerate yield the smallest obtainable resolution. Using Nyquist conversion a samplerate of $f_s = 1Gs/s$ is chosen. The given ramptimes and modulation parameters determine a $5k$-point FFT yielding a $200kHz$ binwidth and frequency resolution. For the given system specifications and CA-CFAR detection parameters this yields:

$$\Delta f_{FFT-bin} = 200kHz \qquad \Delta r \approx 10cm \qquad \delta r \approx 4cm \tag{3.15}$$

3.3.3 Received Signal, Noise and SNR

The optical system discussed in figure 3.2 is modeled and simulated by describing the optical waves propagating through the optical components, through free space by modeling the LiDAR range equation and through the receiver and the conversion into an electrical signal. The full electro-optical simulation takes all the parameters from table 3.2 as an input. Figure 3.6 shows the simulation results of the output signal current and the noise of the system in function of the distance to the object from 0m to 200m over multiple object reflectivities from 5% to 100%. The integrated noise is indicated when integrated over the FFT-binwidth and when integrated over the full system bandwidth to indicate the SNR improvement due to the FFT properties.

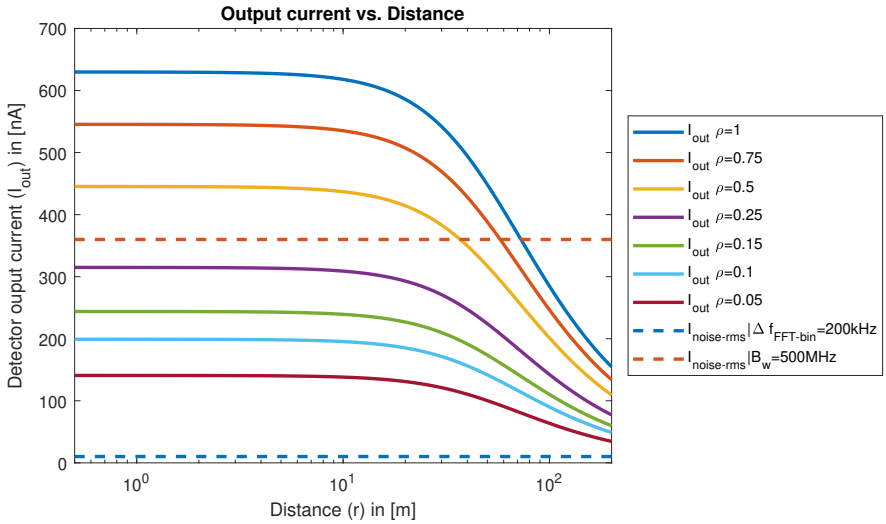


Figure 3.6: Signal output currents & integrated noise currents vs. distance to target for a set of different reflectances

Reading the graph from figure 3.6 or using hand calculations with equations 2.3 and 3.5 for the corner cases, the minimum and maximum signals can be found. These occur, respectively, when the distance to an object is minimum while having 100% reflectivity and at the maximum distance with 5% reflectivity. This yields the results shown in equation 3.16.

$$\begin{array}{lllllll} r_{max} \approx 200m & \rho_{\pi-min} & \approx 0.05 & \rightarrow & P_{r-min} & \approx 0.93pW & I_{out-min} \approx 34nA \\ r_{min} \approx 0.5m & \rho_{\pi-max} & \approx 1 & \rightarrow & P_{r-max} & \approx 309pW & I_{out-max} \approx 630nA \end{array} \tag{3.16}$$

From a noise perspective the system is designed to be shot noise dominated by the LO-power. The following SNR estimations discard the other noise components since they will not significantly

affect the SNR. The noise caused by the LO shown in equation 3.17 where both the FFT-binwidth and full system bandwidth are considered.

$$\begin{aligned} I_n \approx \sqrt{2q\rho_d P_L} &= \mathbf{16}pA/\sqrt{Hz} \\ I_{n-rms-bin} = I_n\sqrt{200kHz} &= \mathbf{7}nA \quad \text{(per FFT bin)} \\ I_{n-rms-full} = I_n\sqrt{500MHz} &= \mathbf{357}nA \quad \text{(total bandwidth)} \end{aligned} \tag{3.17}$$

With the minimum and maximum signal levels and noise known, the SNR can now be estimated. The worst case for the SNR occurs at the lowest signal level because the shot noise is dependent on the LO power only. Using equation 2.4 and its signal and components already calculated in equations 3.16 and 3.17 from the previous chapter, the minimum SNR is estimated to be:

$$SNR_{worst-case} = \frac{\rho_d^2 P_r P_L}{q\Delta f_{FFT-bin}\rho_d\left[P_L + P_r\right]} \approx \frac{34nA}{7nA} \approx \mathbf{14}\boldsymbol{dB} \tag{3.18}$$

The worst-case SNR $\approx 14dB$ as calculated in equation 3.18 is approximately equal to the minimum SNR threshold $\approx 15dB$ [35][25][4] required by the CA-CFAR algorithm. Alternatively plugging in the SNR threshold of the algorithm in the shot-noise limit equation 2.6 shows that the lower limit is $P_r \approx 1pW$. This shows that the system at hand is optimally designed to reach the limits of the technology at hand.

3.3.4 Linearity

The opto-electrical signal chain cannot tolerate non-linearities because they create ghost targets. A ghost target is a false-positive detection of an object. Degraded linearity will generate harmonic or spurious tones. Upon algorithmic analysis of such a frequency spectrum these tones are falsely labelled as a tone corresponding to an object while in the real world no object is present at the detected distance. Linearity of the signal chain must be maintained such that spurious tones remain indistinguishable from the noise.

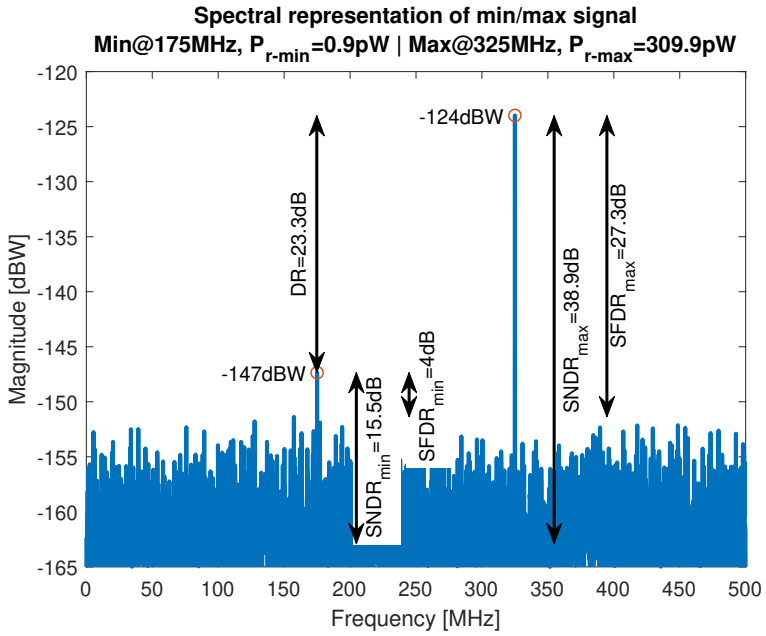


Figure 3.7: Spectral analysis of minimum and maximum received signals from the balanced photodetector

Non-linear effects occur for objects with high reflectivity at close range since they will cause the largest signals in the system. Figure 3.7 shows a side-by-side comparison of the 2 extreme cases that can occur in the frequency spectrum annotated with their DR, SNDR and SFDR parameters.

The SFDR is chosen as a parameter to define the linearity. The simulation of figure 3.7 indicates the maximum SFDR$\approx 27dB$ at the output of the balanced photodetector. The calculated requirement sets an SFDR is $\approx 29dB$ under the assumption that spurs must be suppressed such that they have an amplitude smaller then $\approx 3\sigma$ of the noise. Designing for this specification ensures that spurious tones become indistinguishable from noise avoiding ghost detections in the spectral analysis.

3.4 Conclusion & electrical specification summary

In this chapter the FMCW-LiDAR system was presented, analysed, modelled and simulated. The FMCW-LiDAR principles are combined with the general LiDAR principles from chapter 2. Using these principles the specifications, constraints and requirements for the electronics were determined, a summary is given in table 3.3.

Parameter	Value	Unit	Description
$I_{out-min-rms}$	34	$[nA]$	Minimum signal level
$I_{out-max-rms}$	630	$[nA]$	Maximum signal level
$I_{n-input-referred}$	16	$[pA/\sqrt{(Hz)}]$	Maximum input referred noise density
$I_{out-offset}$	100	$[\mu A]$	Balanced detector maximum offset current
C_{pd}	1	$[pF]$	Balanced detector parasitic capacitance
$f_{low-corner}$	1	$[MHz]$	Low frequency cut-off corner
$f_{high-corner}$	500	$[MHz]$	High frequency cut-off corner
DR	25	$[dB]$	Dynamic range
$SFDR$	29	$[dB]$	Linearity, suppression of harmonics
f_s	1	$[Gs/s]$	ADC samplerate $f_s = 2f_{high-corner}$

Table 3.3: Derived electrical specification summary

Chapter 4

Signal chain architecture

In the previous chapter, the LiDAR system was discussed, the relevant parameters of the system were derived, and the limits of the system were explored based on the given requirements. Using these requirements, the electrical specifications were derived. In this chapter these specifications will be used to design an analogue front-end that forms the signal path from the photodiode to the ADC input. First a general problem statement is formulated. Then the electrical specifications, as given in the previous chapter, are used to derive the signal chain architecture and requirements. Following that the signal chain architecture is presented and the requirements and feasibility of each of the sub-blocks is studied. Finally the complete signal chain with the requirements per block is presented.

4.1 Signal chain requirements

The electrical specifications are summarised in table 3.3. These can be translated into a high level signal chain architecture as shown in figure 4.1. The signal will be designed to capture the weak current of the balanced detector, amplify it to appropriate voltage levels before converting it into a digital signal for further analysis in the digital domain.

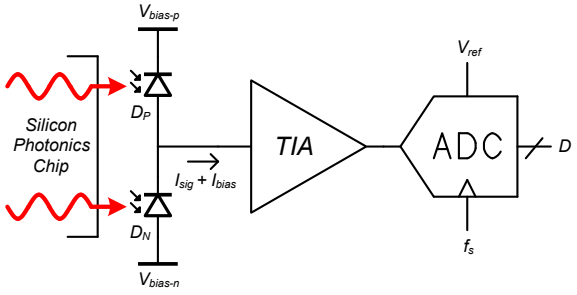


Figure 4.1: High level signal chain processing overview

Using a conventional architecture, the first stage is a current-to-voltage conversion by using a transimpedance amplifier (TIA) boosting the weak current up to appropriate voltage levels. This front-end is followed by an analogue-to-digital converter translating the signals to the digital domain, however this is not part of this work but it is shown for completeness. In the following sections, the requirements and feasibility of the front-end signal chain are determined.

4.1.1 Front-end requirements

The electrical specifications from table 3.3 are directly applicable to the transimpedance front-end. The missing parameter is the transimpedance gain, so an optimisation of the gain is needed. For the smallest input signals it is advantageous to employ a gain as large as possible such that the ADC design can be relaxed by maximising the LSB step size, this in turn will relax the offset requirements. Conversely, for the largest input signals it is important to limit the gain because the signal should not clip. Additionally since a significant amount of noise is present, it is important to provide additional headroom for the noise. Any clipping of the output signal will cause non-linearities which will corrupt the measurement. Equation 4.1 shows how the input-referred clip level of the signal can be set. The factor a is called the noise clipfactor and determines the contribution of the noise, or, at which level noise can be clipped.

$$I_{clip} \geq I_{out-max-pk} + a \cdot \sigma_{noise} \qquad with \qquad \sigma_{noise} = I_{n-input-referred}\sqrt{f_{high-corner}} \tag{4.1}$$

The effect of partly clipping the noise by using factor a from equation 4.1 is simulated, the results are shown in figure 4.2. Figure 4.2a shows the signal behaviour with and without the effects of noise and the clipped noise. After clipping, the noise distribution is no longer Gaussian. The frequency analysis of such a signal would show unwanted frequency spurs. Figure 4.2b shows a simulation where the spectral parameters SFDR, HD2 and HD3 are simulated as a function of the clipfactor (a).

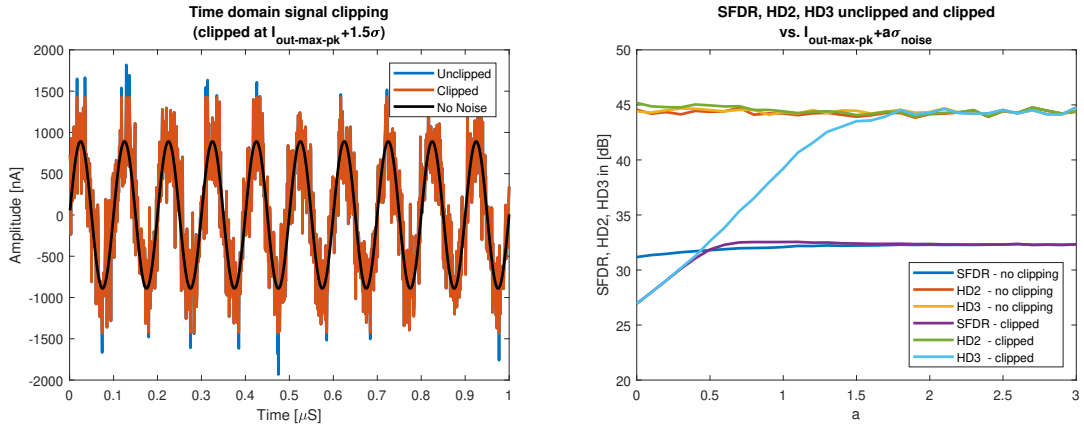


Figure 4.2: (a) Time domain waveform of the unclipped and clipped signals, (b) SFDR, HD2 and HD3 performance vs. a $a\sigma_{noise}$ clipping level.

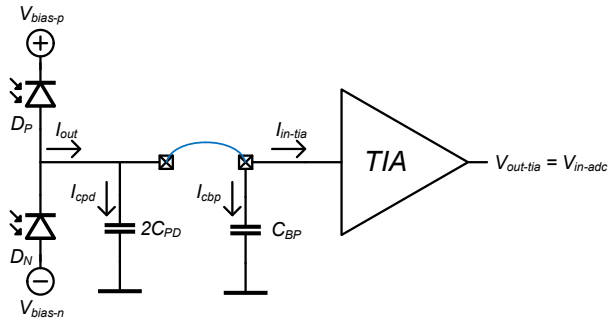
From the simulation results of figure 4.2b, it can be observed that clipping the noise at $(a < 0.5)$ causes the SFDR and HD3 performance to be severely degraded. Values of $1.5 > a$ allow for the full HD3 and SFDR performance. Using $a = 1.5$ the input signal amplitude can swing to $I_{clip} = 1.42\mu A$. The maximum output amplitude is determined to be $\approx 250mV$. Considering a power supply rail of 1.5V fixed by the technology and a baseline amplifier as a differential pair with a tail current source and active load. All transistors are assumed to be biased in saturation with $V_{ds} \approx 250mV$. The maximum gain can now be determined to be:

$$A_{TIA} = R_{TIA} = \frac{V_{out-pk-max}}{I_{clip}} \approx 160k\Omega \approx \mathbf{104}\boldsymbol{dB}\Omega \tag{4.2}$$

The gain shown in equation 4.2 is the nominal gain configuration. Additionally, 3 more gain ranges will be implemented, $102dB\Omega$, $106dB\Omega$, $109dB\Omega$. The electro-optical system will suffer from

losses, for example sub-optimal fiber-optic coupling or mismatches in the balanced detection. The implementation of multiple gains provides finetuning capabilities to the overall system.

The last parameter is the total input capacitance. A good estimate is required since it will affect the bandwidth and stability of the TIA. The capacitance will short the input current, this effect worsens with increasing frequency causing less input current for the TIA. Figure 4.3 illustrates the current path from the balanced detector, the most significant contributors are shown.



$$\begin{array}{lll} & 2C_{PD} & 2 \cdot 0.5pF \\ + & C_{BP} & 0.6pF \\ \hline & C_{in-tot} & \mathbf{1.6 \approx 2pF} \end{array}$$

Figure 4.3: Worst-case input capacitance estimation

The main contributors are the balanced photodetector's parasitic capacitance and the bondpad parasitic capacitance. Each photodiode has a capacitance of $\approx 500fF$ estimated from the silicon photonics technology manual. The bondpad capacitance is specified by the TSMC 0.13 I/O manual and is determined to be $C_{BP} = 100fF - 600fF$ depending on the ESD-structures used. The full input capacitance is estimated to be $C_{in-tot} \approx 2pF$ considering that $\approx 400fF$ is available for wiring capacitance should it be needed.

4.2 Signal chain architecture

In the previous section the requirements of the signal chain were established. In the following sections these requirements will be assessed for their feasibility by checking the literature. First, the different TIA architectures are discussed, afterwards an overview of existing designs is given.

4.2.1 Literature survey

In order to evaluate the feasibility of the literature is studied, a comparison of different publications is made. The study is focused on optical receiver front-ends since they deal with similar properties as LiDAR front-ends. The literature found has 4 commonly used architectures. These are shortly discussed and a comparison table is shown in table 4.1.

A first architecture is the shunt-feedback transimpedance amplifier [43] as shown in figure 4.4a. The transimpedance gain is set by the feedback resistance (R_f), combined with the input capacitance (C_{in}) the bandwidth is fixed, considering an amplifier with a fixed gain-bandwidth. In a well balanced design the noise is dominated by the contribution of the feedback resistance. In optical transceivers the input capacitance is fixed by the photodiode and as a result, the choice of the feedback resistance constrains transimpedance gain, bandwidth and noise.

A second topology is the common gate TIA as shown in figure 4.4b [43]. A common gate stage serves as a current buffer, whose input impedance is inversely proportional to the CG transconductance ($Z_{in} = 1/g_{m-CG}$). Combined with the input capacitance (C_{in}) this sets the dominant pole and determines bandwidth considering that the output pole is non-dominant. The CG transistor also acts as an isolator between the input and output. As a result, the transimpedance can be set independently by the load (R_L). This implies that, given a fixed input capacitance, the circuit can be designed with a higher bandwidth or larger transimpedance gain compared to the shunt-feedback topology [34] [39]. The CG-stage acts as a current buffer, as a result any noise generated by the load, CG or current sources directly contribute to the input referred noise. Reducing noise

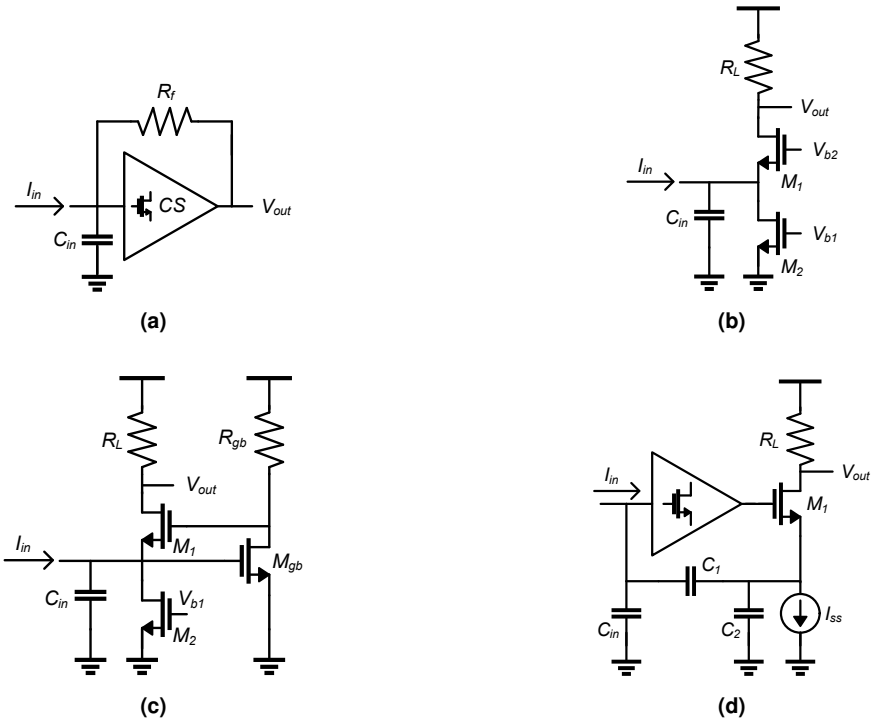


Figure 4.4: (a) Shunt-feedback TIA, (b) CG-TIA, (c) RCG-TIA, (d) Capacitive-feedback TIA

can be done by reducing the current but it will impact the obtainable transconductance and hence bandwidth and transimpedance gain.

A third topology is the regulated common-gate (RCG) as shown in figure 4.4c. The RCG tries to solve the CG amplifier's noise issue by adding a gain-booster [43] [44] [49] [23] [29] [22]. In figure 4.4c a gain-booster amplifier, consisting of M_{gb} and R_{gb}, is added to a CG-stage. The current in the CG transistor can now be decreased while maintaining the same effective transconductance and bandwidth. The noise contribution of the CG-branch is decreased but additional noise is added by gain-booster and an optimal noise configuration can be found. With the reduction in current, a larger load resistance can be chosen to yield a larger transimpedance.

A fourth topology is the capacitive feedback transimpedance amplifier [39][18][43]. This architecture is shown in figure 4.4d. The gain is set by the ratio of capacitors in combination with the output resistor $(1+C_2/C_1)R_L$. Since the feedback network is capacitive, it will not add any noise, therefore this topology is well suited for a low noise design [33] [40], more so than the topologies previously mentioned.

Table 4.1 compares the performance of different publications and their specifications. In order to evaluate the performance of a TIA design, the transimpedance-bandwidth product ($ZB_w = Z_{tia-DC} \cdot B_{w-tia}$) can be calculated for each of the designs. It is defined as the transimpedance gain multiplied by the -3dB bandwidth of the amplifier [18]. This FoM [18] is analogous to the well-known gain-bandwidth (GB_W) used for voltage-to-voltage amplifiers.

A typical optical front-end architecture is presented in [29]. This design makes use of a common gate followed by a resistive feedback TIA. In [43] a similar architecture is used however a RCG is used to obtain a smaller input impedance and a higher bandwidth. The addition of a CG or RCG stage is useful in shielding the parasitic capacitance from subsequent stages. This architecture is also demonstrated in [43], in [44] a differential implementation is shown, in [22] the CS gain-booster transistor is preceded by a CG transistor used as a level shifter to allow operation in technologies with lower supplies. In [49] and [23] fully integrated front-ends for optical receivers are presented. Both publications discuss a TIA cascaded with additional amplification and limiting stages. The

	JSSC '10 [23]	JSSC '05 [49]	JSSC '04 [44]	ISSCC '00 [33]	CICC '09 [40]
Technology	0.13μm CMOS	0.18μm CMOS	0.25μm CMOS	0.6μm CMOS	0.18μm CMOS
Bandwidth	6.4GHz	8GHz	670MHz	550MHz	1.8MHz
TIA-gain	75$dB\Omega$	53$dB\Omega$	80$dB\Omega$	79$dB\Omega$	155$dB\Omega$
Noise	32$pA/\sqrt{Hz}$	-	20$pA/\sqrt{Hz}$	4.5$pA/\sqrt{Hz}$	65$fA/\sqrt{Hz}$
C_{pd}	3pF	0.15pF	1pF	-	-
Power	47mW	210mW	27mW	30mW	436μW
ZB_w	36$THz\Omega$	3.6$THz\Omega$	6.7$THz\Omega$	4.7$THz\Omega$	100$THz\Omega$
Architecture	*a + c*	*a + c*	*a + c*	*d*	*d*

Table 4.1: Transimpedance amplifier comparison (architecture as referenced in figure 4.4)

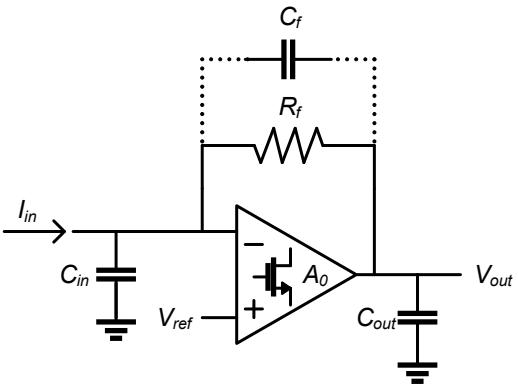
front-end is based on an RCG input stage cascaded with a resistive feedback TIA. Inductive peaking and equalisation techniques are used to extend the bandwidth. Lastly [33] and [40] make use of the capacitive feedback architecture. These show superior noise performance and power consumption compared to the other architectures.
Using the study from the foregoing paragraphs and table 4.1 shows that there are two possible candidates, it can be concluded that there are 2 possible candidates, the RCG and the capacitive feedback architecture. The final architecture chosen consists of a combination of an RCG stage followed by a shunt-feedback stage. The transimpedance gain of this architecture is similar to the capacitive feedback architecture but it can reach higher bandwidths. However to reach the gain specification of $104dB$, it is clear that an additional gain-stage is required. The RCG stage as well as the additional gain stage are designed with sufficiently high bandwidth such that, when cascading the stages, the bandwidth reduction is limited and the overall bandwidth specification is reached. The capacitive feedback architecture has superior noise performance, due to the direct contribution of the transistor's channel noise to the input-referred noise. However the RCG is capable of reaching the noise requirement of $16pA/\sqrt{Hz}$ set forward for the application.

4.2.2 Feasibility study

The feasibility of the transimpedance amplifier, shown in figure 4.6, is assessed by considering a simple shunt-feedback TIA as a baseline. Considering the topology without an input capacitance ($C_{in} = 0$), it is clear that it is a first order system and the bandwidth is only determined by the amplifier. The input capacitance (C_{in}) adds an additional pole in combination with the feedback resistance (R_{fb}) yielding a second order system. The TIA bandwidth (f_n) is the geometric mean of both poles, the gain-bandwidth (GB_W) can be determined by equation 4.3:

$$GB_W = 2\pi f_n^2 C_{in} R_f \quad = 500GHz \quad \text{with} \quad GB_W = \frac{\omega_0(1+A_0)}{2\pi} \approx \frac{\omega_0 A_0}{2\pi} \tag{4.3}$$

Equations 4.4 to 4.6 are derived from the circuit's transfer function and can be used as design equations. The quality factor is set to $Q = 1/\sqrt{2}$ to obtain a Butterworth response [39], this entails that $f_n = f_{-3dB}$. The input capacitance (C_i) and the feedback resistance (R_f) are known by equation 4.6 and a fixed ratio between A_0 and ω_0 exists.



$$G_{TIA} = R_f \frac{A_0}{A_0 + 1} \tag{4.4}$$

$$f_n = \frac{1}{2\pi}\sqrt{\frac{\omega_0(1+A_0)}{C_{in}R_f}} \tag{4.5}$$

$$Q = \frac{\sqrt{\omega_0(1+A_0)C_{in}R_f}}{C_{in}R_f\omega_0 + 1} \tag{4.6}$$

Figure 4.5: Baseline shunt-feedback TIA

Using the equations and the derived specifications ($f_n = f_{high-corner} = 500MHz$, $C_i = C_{pd} = 2pF$ and $R_f = 160k\Omega$) yields a gain-bandwidth requirement of 500GHz. It is clear that such a high gain-bandwidth will be difficult to achieve, using a different architecture this can be mitigated.
In equations 4.3 to 4.6, G_{TIA} represents the transimpedance gain, R_f represents the feedback resistance, A_0 describes the open loop gain of the amplifier and $\omega_0 = 2\pi f_0$ is related to its cut-off frequency. Furthermore f_n is the pulsation frequency of the second order system and is related to the bandwidth through the Q factor. C_f is an optional capacitor for frequency compensation.

Gain-bandwidth assessment

The gain-bandwidth of the core amplifier is a key parameter in tuning the transfer function of the TIA. A simulation driven assessment was taken, as a baseline an architecture using a differential pair with a current mirror load was chosen (figure 4.6). Simulation results show the technology has a typical $f_t \approx 80GHz$ ($W/L = 16/0.13\mu m$, $I_d \approx 1mA$, $V_{gs} - V_{th} \approx 0.2V$). In an amplifier as shown in figure 4.6, biasing at the same operating point reaches maximum gain-bandwidths as presented table 4.7. This ensures maximum bandwidth with $g_{m1/2} = 8.6mS$ and $A_0 = 5.9x \approx 15dB$.

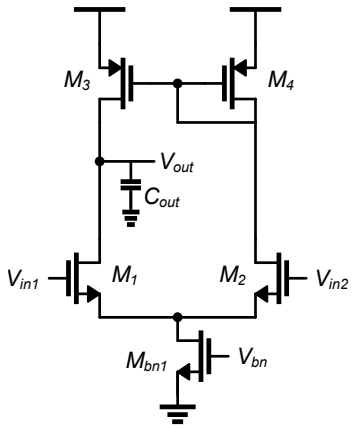


Figure 4.6: Baseline TIA 5T-amplifier core

Corner	Slow $125°C$	Nominal $27°C$	Fast $-40°C$
GB_W	$\approx$10GHz	$\approx$16GHz	$\approx$22GHz

Figure 4.7: Simulated GB_w a differential pair with a current mirror load ($A_0 = 5.9x$)

With a load capacitance estimated to be $C_{out} \approx 100fF$ (estimated wiring and subsequent stage's gate capacitance) with a gain-bandwidth to $10GHz$ in the worst-case corner. With the given specifications a maximum of $R_f \approx 3k\Omega$ can be reached.

Stability

The stability of the TIA depends on the pole placement. The assessment of the stability can be done by analysing the loopgain as shown in equation 4.7. A first pole is caused by the amplifier

represented in the first factor, a second pole is formed by the capacitance C_{in} and R_f shown in the second factor.

$$A_{LP} = \frac{-A_0}{\frac{s}{\omega_0}+1} \cdot \frac{1}{C_{in}R_f+1} \tag{4.7}$$

There are two distinct pole placement possibilities: closely spaced poles will cause instability, poles spaced far apart will reduce the bandwidth. High Q-factors result in small phase margins and instability. Targeting $Q = 1/\sqrt{2}$ corresponds to a stable system with a $\approx 65^\circ$ phase margin and uses the bandwidth most efficiently.
The bode diagram of the two pole placement cases are shown in figure 4.8. These plots show the resulting transimpedance gain (blue), the amplifier open-loop gain (black), the loop-gain (red) and the noise-gain (green). The noise gain is defined as the inverse transfer function of the feedback network [39]. Dashed representations indicate the uncompensated case (C_f not present).

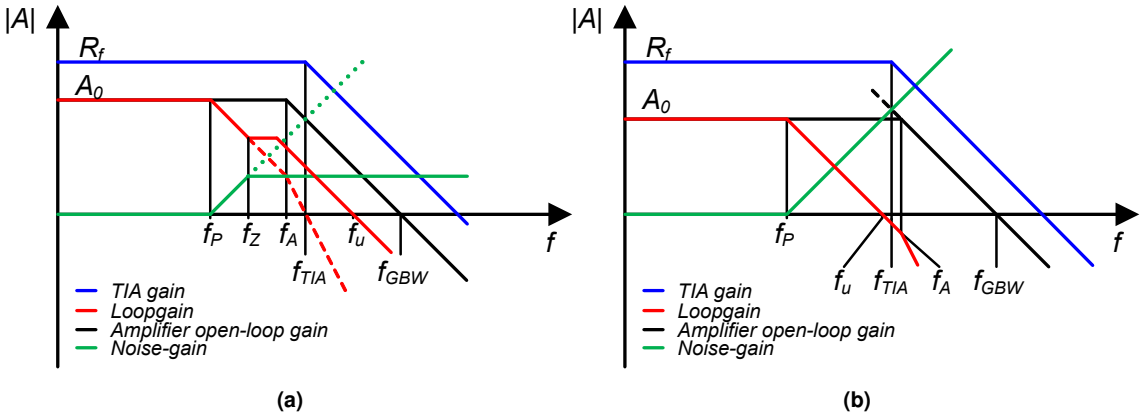


Figure 4.8: (a) C_f compensated TIA Loop-gain (uncompensated cases showed in dashed lines) (b) Loop-gain for a feedback-capacitor compensated TIA

The case for high Q-factors is shown in figure 4.8a. Both the pole of the amplifier at (f_A) and of the feedback network (f_P) occur in a constellation such that the loopgain crosses unity with a slope of -40dB/dec indicating instability. Alternatively each pole causes a -90° phase shift, combined with an inverting amplifier, this yields a positive feedback loop while the gain is unity or higher. To ensure stability a feedback capacitor C_f is employed, this introduces a zero (f_Z) in the feedback network and causes pole splitting. As a result Q-factor reduces due to one pole moving lower in frequency while the other moves up. The bandwidth is slightly reduced but more phase margin is created. The zero adds a +90° phase shift. Alternatively in the bode diagram, the zero compensates a pole and causes a -20dB/dec roll-off and zero crossing.
The low Q-factor pole constellation is shown in figure 4.8b. The amplifier's pole (f_A) is at a much higher frequency then (f_P). The loopgain shows that, the pole of the feedback network (f_P) becomes the dominant. The amplifier's pole (f_A) only occurs after the loopgain already crossed unity. An inherently stable situation is the result. The drawback of this configuration is that the bandwidth is not optimally used. The amplifier will require more power to push its pole to a higher frequency. The configuration of figure 4.8a with closely spaced poles is more energy efficient.

Noise

The noise analysis of the circuit in figure 4.6 is shown in equation 4.8. $I^2_{n,TIA}$ represents the total input referred noise density, k represents the Boltzmann constant, T the absolute temperature, V_n^2 the input-referred voltage noise of the amplifier.

$$I^2_{n-TIA} = \frac{4kT}{R_f} + V_n^2\left[\frac{1}{R_f} + s(C_{in}+C_f)\right]^2 \tag{4.8}$$

The amplifier's input referred noise V_n^2 experiences a noise gain with increasing frequencies due to the input capacitance. This effect worsens with increasing C_{in}, by changing the design to push V_n^2 lower a noise balance with the effects of R_f can be found. However for the large R_f and C_f the amplifier's input referred noise becomes dominant. An input referred noise of $V_n \approx 2.5nV/\sqrt{Hz}$ is required to reach the specification.

Gain-boosted common-gate input stage (RCG)

The presented shunt feedback architecture has a fixed relation between bandwidth, transimpedance gain. Given the specifications, the system has 2 degrees of freedom, the feedback resistance and the amplifier's gain-bandwidth. The transimpedance bandwidth is a given while the parasitic capacitance is fixed by the photodiode. To overcome these limitations, the proposed architecture places an RCG stage in front of the shunt feedback stage, shown in figure 4.9. This stage acts as a current buffer and shields the large C_{in} from R_f, the capacitance at the virtual ground is now determined only by parasitic capacitances. The feedback resistor can now be increased to create higher transconductance gain for the same bandwidth. The shunt-feedback stage transimpedance gain is now limited by any offset current flowing through R_f rather than a bandwidth limitation. This can be mitigated by reducing the current through CG-transistor (M_{mgc}) the resulting reduction in transconductance can be compensated by increasing the gain-booster's gain.

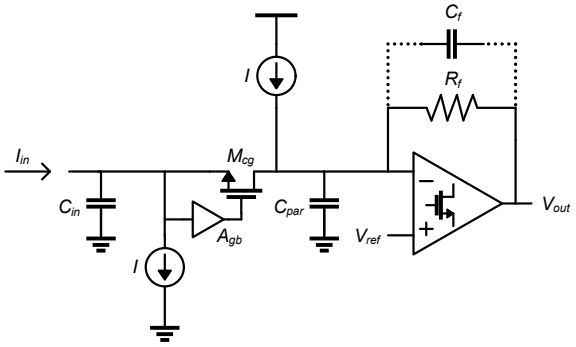


Figure 4.9: Shunt-feedback TIA with a gain-boosted CG-current buffer

Gain and bandwidth

The RCG stage does not add gain, and further analysis reveals that the input impedance and bandwidth can be approximated by equation 4.9. Considering a CG-stage, its input impedance looking into the source terminal is the inverse of the transconductance. Implementing gain boosting multiplies this transconductance by the gain of the booster amplifier. The bandwidth is then set by the input impedance and capacitance, considering it is the dominant pole for the stage.

$$Z_{in} = \frac{1}{g_{m-cg}(A_{gb}+1)} \qquad f_{bw} = \frac{g_{m-cg}(A_{gb}+1)}{2\pi C_{in}} \tag{4.9}$$

In the equation 4.9 g_{m-cg} is the transconductance of the CG-transistor and A_{gb} describes the gain of the gain-booster. Z_{in} and f_{bw} describe the input impedance and bandwidth of the RCG-stage.

Noise

The RCG noise and bandwidth can be designed orthogonally. To maintain a total input-referred noise of $16pA/\sqrt{Hz}$ an equal division between the contributing components: the shunt-feedback stage, high (PMOS) and low (NMOS) side current sources, the CG-transistor and its gain-booster. For the circuit shown in figure 4.9 a high level noise analysis is given in equation 4.10:

$$I_{in-tot}^2 = I_{n-Mp}^2 + I_{n-Mn}^2 + I_{n-GB-Cin}^2 + I_{n-Mcg}^2 + I_{n-TIA}^2 \tag{4.10}$$

In equation 4.10, I_{n-TIA}^2 indicates the noise contribution of the shunt-feedback amplifier. I_{n-Mp}^2 and I_{n-Mn}^2 represent the channel noise of the high (NMOS) and low (PMOS) side current sources. I_{n-Mcg}^2 is the channel noise of the CG-transistor and $I_{n-GB-Cpd}^2$ is the the gain-booster's input-referred voltage noise converted into an input-referred noise current over the input capacitance.

Stability

The stability of the RCG stage must be ensured since the booster amplifier and the CG-transistor form a loop which inherently has 2 poles. A first, dominant, pole is formed by the CG's input impedance and C_{in} while a second pole is caused by the gain-booster amplifier [19]. Depending on the pole position the system can become unstable, an in-depth analysis follows in the next chapter.

Baseline implementation

Using the previous analysis a baseline design implementation of the architecture can be made. Designing the circuit bandwidth with an equal division of $707MHz$ for each of the stages yields an overall $500MHz$ bandwidth. This is accomplished with a CG transconductance of $g_{m-CG} \approx 1.5mS$ and the gain of the booster set to $A_{gb} \approx 5$. This is obtainable considering the assessment of the 5T-amplifer core of figure 4.6. The shunt-feedback resistance, with an estimated $C_{par} \approx 100fF$, can reach $R_f \approx 30k\Omega$. However offsets generated in the CG-branch will manifest an offset voltage over R_f. With a nominal current of $150\mu A$ through the CG-transistor and current sources, a worst-case 10% offset current was simulated. This requires the feedback resistance to be limited, and hence the gain, to $R_f = 20k\Omega$ to keep the shunt-feedback amplifier biased correctly. The noise specification of $\leq 16pA/\sqrt{Hz}$ can be reached by choosing an equal division of $\leq 7pA/\sqrt{Hz}$ per contributor. Table 4.2 shows the estimates of the feasibility of the architecture.

Parameter	Value	Unit
R_{TIA}	≈84	$[dB\Omega]$
$f_{high-corner}$	≈500	$[MHz]$
$f_{RCG-stage}$	≈707	$[MHz]$
$f_{TIA-stage}$	≈707	$[MHz]$
$I_{in-noise}$	≈16	$[pA/\sqrt{Hz}]$
$I_{n-RCG-stage}$	≈14	$[pA/\sqrt{Hz}]$
$I_{n-Mp/n}$	≈7	$[pA/\sqrt{Hz}]$
I_{n-Mcg}	≈7	$[pA/\sqrt{Hz}]$
v_{n-GB}	≈1	$[nV/\sqrt{Hz}]$
$I_{n-TIA-stage}$	≈7	$[pA/\sqrt{Hz}]$

Table 4.2: TIA requirements

4.2.3 Gain stage requirements

The architecture shown in figure 4.9 has the potential of reaching the bandwidth and noise requirements, however it does not cover the full gain required. A gain stage is added to reach the full $104dB$ gain. Using table 4.2 an additional $20dB$ of gain is required. However adding a gain-stage will decrease the system's overall $3dB$-bandwidth as shown in equation 4.11 [18].

$$f_{-3dB-tot} = \left[\sqrt{{f_{-3dB-TIA}}^{-2} + {f_{-3dB-GainStage}}^{-2}}\right]^{-1} \tag{4.11}$$

In equation 4.11, $f_{-3dB-tot}$ represents the bandwidth of the system, $f_{-3dB-TIA}$ and $f_{-3dB-GainStage}$ represent the transimpedance stage and gain stage bandwidth respectively.
To mitigate the bandwidth reduction, the transimpedance gain is reduced by $1dB$ and the gain-stage's gain is set to $21dB$ so that the TIA bandwidth can be increased. This is accomplished by reducing the feedback resistance to $18k\Omega$, this results in an increase in TIA bandwidth from $500MHz$ to $560MHz$. The gain-stage bandwidth requirement is now set to $f_{-3dB-GainStage} \approx 1.2GHz$ to reach the $500MHz$ system bandwidth. The adjusted TIA specifications are shown in table 4.10.

Parameter	Value	Unit
R_{TIA}	≈83	$[dB\Omega]$
$f_{high-corner}$	≈560	$[MHz]$
$I^2_{in-noise}$	≈11.3	$[pA/\sqrt{Hz}]$

Figure 4.10: Adjusted TIA-specifications

Parameter	Value	Unit
$A_{gain-stage}$	≈21	$[dB]$
f_{Bw}	≈1.2	$[GHz]$
$V^2_{n-gain-stage}$	<160	$[nV/\sqrt{Hz}]$
C_L	1	$[pF]$

Figure 4.11: Gain-stage specifications

The gain of the TIA stage is kept high to reduce any noise contribution of subsequent stages to the input, as a result there is an unequal bandwidth distribution between the TIA and gain-stage. The input referred noise of the TIA is lowered by $\sqrt{2}$ and budgeted to the gain-stage. Considering the TIA gain this yields a maximum input referred noise specification of $160nV/\sqrt{Hz}$ for the gain stage. The gain-stage specifications are summarised in table 4.11. The output of the gain stage must be foreseen such that it can drive the subsequent ADC's input capacitance. The input capacitance is estimated to be $\approx 1pF$ and therefore forms the load of the gain stage.

4.2.4 Literature survey

With the established gain-stage requirements, an architecture can be chosen. High bandwidth amplification stages are required to reach the specifications. However conventional opamp feedback amplifiers are ill suited for this purpose because the multi-transistor topologies typically reduce the available gain-bandwidth. Therefore open loop solutions are chosen as a solution to create the required gain while maintaining bandwidth.
A typical open-loop topology using a differential pair with a resistive or diode load is shown in figure 4.12a and 4.12b. The gain of such an amplifier topology is governed by $A_0 \approx g_{m1/2}R_L$, the bandwidth is defined by $B_w \approx 1/C_{out}R_L$ and gain bandwidth $GB_w \approx g_{m1/2}/C_{out}R_L$. When a diode load is chosen, the output resistance can be replaced by $1/g_{m-pd1/2}$. This architecture can reach a relatively wide bandwidth and a low gain. The disadvantage of the resistive loads is that they exhibit poor PSRR. Diode connected loads add more parasitic capacitance reducing bandwidth. Additionally the circuit is heavily subject to PVT variations. These variations can be minimized by implementing the circuit in figure 4.12b using only P-type or N-type devices.
A second possible candidate is the Cherry-Hooper architecture [8] as shown in figure 4.12. The architecture is commonly used in high bandwidth applications for optical communications [18] [39] [49]. An input transconductance stage is formed by transistors M_1 and M_2. A second stage is a transimpedance stage formed by M_3, M_4 and the feedback resistances R_f and R_d. The DC-gain of the circuit is determined by $A_0 \approx g_{m1}R_f$ considering $R_f << R_d$. A first pole is located at node x caused by the parasitic capacitances. The transconductance stage is loaded with a TIA as active load, its input impedance is $R_i \approx R_f/A$, in parallel with the impedance at node x it lowers the total impedance and pushes the pole to higher frequencies. A second pole is located at the output of the TIA and defined by C_{out}. Additionally, the 2-pole system can potentially employ peaking to extend bandwidth [18]. The disadvantage is that the gain is limited and resistive loads cause bad PSRR.
Inductive peaking [18] is a bandwidth enhancement technique that can be applied to the differential

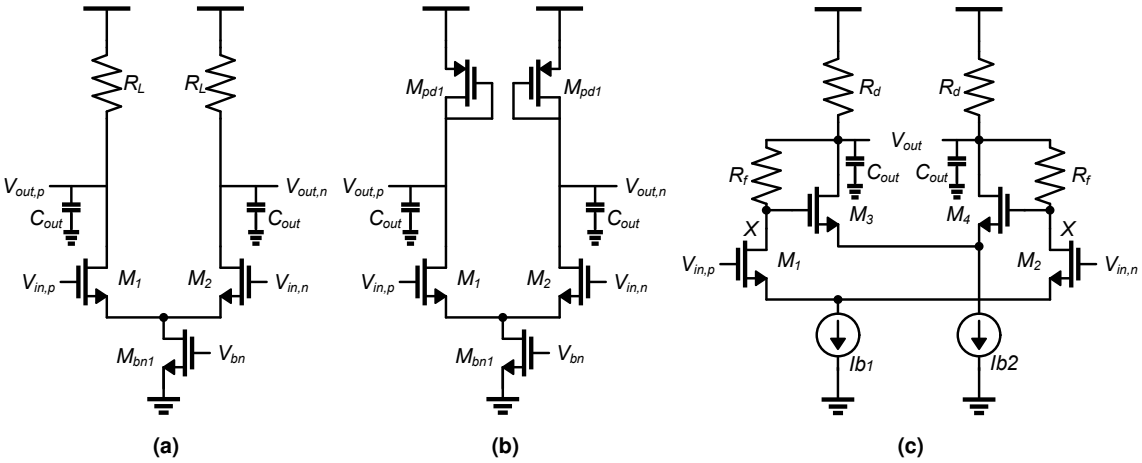
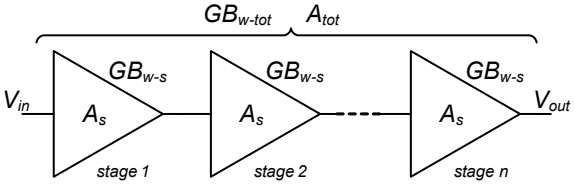


Figure 4.12: (a) Diff. pair, resistive load, (b) Diff. pair, diode load, (c) CH-architecture

pair or CH-architecture. Resistors can be replaced or inductors can be placed in series with the load resistances [49]. However on-chip inductors are cumbersome to design, as an alternative negative resistance circuits [23] can be used.
Open loop architectures run into issues where DC-offsets can cause the amplifier to pull towards one of the supply rails, especially when cascading multiple stages. A first solution is to use coupling capacitors to isolate the DC-bias. A second solution is to use DC-offset compensation loop [39] [18] [23] and [49]. Both solutions will, however, introduce a low-frequency high-pass corner.
The chosen baseline amplifier core architecture is a modified version of the differential pair with a diode connected load as shown in figure 4.12b. All devices are implemented as N-type MOSFET's to minimise the effect of PVT variations. The amplifier core can be AC coupled and cascaded in case a multi stage approach is needed to reach the gain. Bandwidth is mainly determined by the transconductance of M_1 and M_2 considering a fixed load capacitance. The high TIA gain of the preceding stage makes the noise of the amplifier a less significant input-referred noise contributor.

4.2.5 Gain stage feasibility

With the considered architectures and the specifications, listed in table 4.11, a baseline amplifier stage can be designed. With the required gain and bandwidth a $GB_w \approx 13.5GHz$ is required. Considering the earlier GB_w performance benchmarks from figure 4.6 and table 4.7, a cascaded amplifier approach was taken. Using this approach, the gain bandwidth of multiple identical cascaded stages can be extended beyond what can be obtained by a single stage[39][18]. The gain-bandwidth extension B_{w-tot}/B_{w-s} is explained in figure 4.13 and equation 4.12.



$$\frac{B_{w-tot}}{B_{w-s}} = A_{tot}^{1-1/n}\sqrt{2^{1/n}-1} \tag{4.12}$$

Figure 4.13: Cascaded amplifier chain

Considering this bandwidth enhancement technique, an optimum number of stages $n \approx 2 \cdot ln(A_{tot})$ exists[39]. For the given specifications of table 4.11, this yields a 5-stage amplifier with a total bandwidth extension of $\approx 2.7x$. Each stage has a gain of $4.2dB$ and a bandwidth of $2.7GHz$. The chosen architecture deviates from this optimum, the amplifier consists of 2 gain-stages delivering a bandwidth extension of $\approx 2.2x$. The gain per stage is set to $10.5dB$ and a bandwidth of

$1.7GHz$. This reduces design complexity, area usage and power consumption while meeting all the requirements.
The total input-referred noise of the cascaded gain stages is a gain weighted sum of the input-referred noise of the identical stages as described in equation 4.13. For a 2 stage the equation is straightforward and yields a maximum allowable input-referred noise per stage $153nV/\sqrt{Hz}$.

$$V_{in-tot}^2 = \sum_{i=0}^{n-1} \frac{V_{in-n}^2}{(A_{s-n}^i)^2} \tag{4.13}$$

In equation 4.13, n is the number of stages, V_{in-tot} and V_{in-n} represent the total and single amplifier input-referred noise and A_{s-n} the gain of a single stage.
Considering a 2 stage amplifier, table 4.3 summarises the specification for a single gain stage element. The final architecture is illustrated by figure 4.14. Because open loop stages were chosen as building blocks, AC coupling capacitors were chosen as a solution to battle DC offsets. The capacitors need to be chosen such that the application's high pass corner requirement is satisfied.

Parameter	Value	Unit
$A_{gain-stage}$	≈10.5	$[dB]$
f_{Bw}	≈1.7	$[GHz]$
V_{in-tot}^2	≈153	$[nV/\sqrt{Hz}]$

Table 4.3: Specifications for a single gain-core element

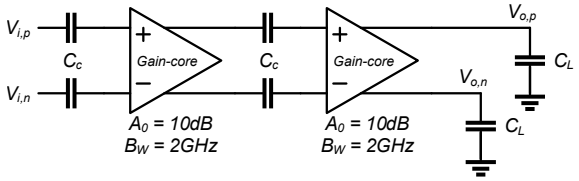


Figure 4.14: Architecture of the gain-stage

Chapter 5

Circuit Design

In the previous chapter the architecture of the signal-chain is fixed. This chapter gives a more detailed description of each of the circuit blocks. For each block the transistor design is shown, the analysis, simulations and optimisations are discussed as well as the final post-layout simulation results.

5.1 Transimpedance amplifier design

The detailed implementation of the RCG transimpedance architecture is shown in figure 5.1. The current sources of the CG-branch are implemented by PMOS and NMOS transistors M_n and M_p respectively.

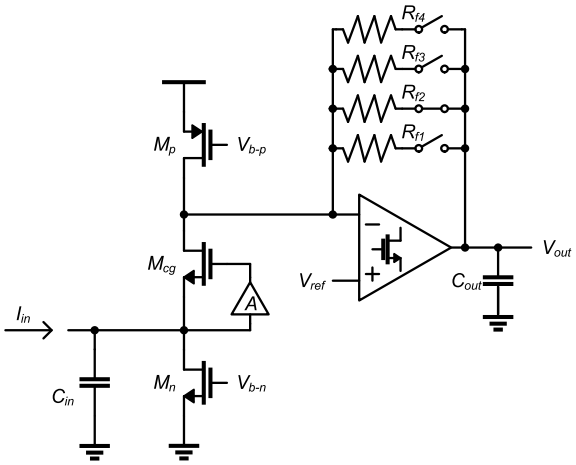


Figure 5.1: TIA architecture, Gain-boosted common-gate input stage combined with a variable gain shunt-feedback amplifier

In the following paragraphs, the implementation details of the CG-stage with its gain-booster was discussed first. Secondly the shunt feedback implementation is discussed. This portion of the signal chain has the 4 selectable gains implemented by using different selectable feedback resistances.

5.1.1 Gain-boosted common-gate input stage (RCG)

The RCG input stage, as shown in figure 5.1, is implemented from a bandwidth and noise perspective. Taking a structured approach to the design the first parameter considered is the bandwidth. Once the bandwidth is fixed, the gain-booster amplifier design can be completed. The noise per-

formance can be adjusted afterwards, it can be optimised by a proper scaling of the CG transistor and the gain-booster.

Gain & Bandwidth

The RCG's bandwidth is determined by the effective transconductance as described earlier in equation 4.9. For a proposed bandwidth of $707MHz$ an effective transconductance of $g_{m-cg}(A_{gb}+1) \geq 9mS$ in combination with the input capacitance $C_{in} = 2pF$. This effective transconductance is split up in a CG transcoductance $g_{m-cg} \geq 1.8mS$ and a gain-booster gain of $A_{gb} \geq 5x$ (table 4.2).

Gain-booster

The gain-booster's gain is set at $14dB$ $(5x)$, however the bandwidth is to be determined. To obtain an RCG closed-loop bandwidth of $707MHz$ the gain-booster requires a larger bandwidth. At this frequency its gain will already be reduced by $\approx 30\%$. A larger bandwidth is required such that the gain at the closed loop bandwidth ensures sufficient gain-boosting. Modeling the RCG through equation 4.9 and considering a first order roll-off for the gain-booster yields a $\approx 1.4GHz$ bandwidth requirement, as shown in table 5.1. Lastly the noise specification was copied from the TIA specifications as established in table 5.1 of the previous chapter.

Parameter	Value	Unit
A_{gb}	≈14	$[dB]$
f_{Bw-gb}	≈1.4	$[GHz]$
V^2_{n-gb}	≈1	$[nV/\sqrt{Hz}]$

Table 5.1: Specifications for the gain-booster

To determine the architecture for the gain-booster the DC-bias considerations are used as a starting point. The CG-transistor has a $V_{th} \approx 0.4V$ (low threshold devices), the overdrive voltage is set to $V_{ov} = 0.2V$. The low side NMOS current source (M_n) is designed with $V_{ds} \geq 0.2V$. This means that the minimum CG gate voltage of M_{cg} must be $V_{g-cg} \geq 0.8V$. The gain-booster candidates are shown in figure 5.2. A first candidate is simple CS stage as proposed in [43] and shown in figure 5.2a. However, since an NMOS (M_n) current source is used rather than a resistor, the CS-transistor cannot be biased correctly because a minimum voltage of $V_{g-Mgb} \approx 0.6V$ is required. With $V_{ds-Mn} \approx 0.2V$ it is too low to bias the CS gain-booster. Increasing this V_{ds} also increases the required CG's gate voltage but decreases the available headroom for R_{gb} and a lower resistance must be chosen with a drop in the gain, and gain-boosting capability as a result. A second candidate is a differential pair as shown in figure 5.2b. However, similar issues arise, biasing the amplifier requires a $V_{ds-Mn} \approx V_{ds-Mtail} + V_{th-Mgb1} + V_{vov-Mgb1} \approx 0.8V$. The CG gate must now be biased at $V_{g-Mcg} \approx 1.4V$ leaving no headroom for the loads. When switching to a PMOS topology, the low side output is too low to bias the CG-transistor. A more robust topology is shown in figure 5.2c. It makes use of a folded cascode with a PMOS input which provides a low-side input and a high-side output. The input and output ranges are large enough to cover the biasing requirement for the CG transistor, the circuit's output or CG bias voltage, can go up to $V_{g-Mcg} \approx V_{dd} - V_{ov-Mcsp} \approx 1.3V$, while the input is allowed to go up to $V_{ds-Mn} \approx V_{dd} - V_{ds-Mtail} - V_{th} - V_{ov-Mgb1/2} \approx 0.7V$. The input of the circuit employs an additional PMOS device (M_{gb2}) to accomplish the regulation of the input voltage. The additional PMOS gate is connected to a $\approx 0.3V$ reference keeping the input and V_{ds-Mn} at this voltage. For the reasons above, this last topology (figure 5.2c is the chosen implementation.

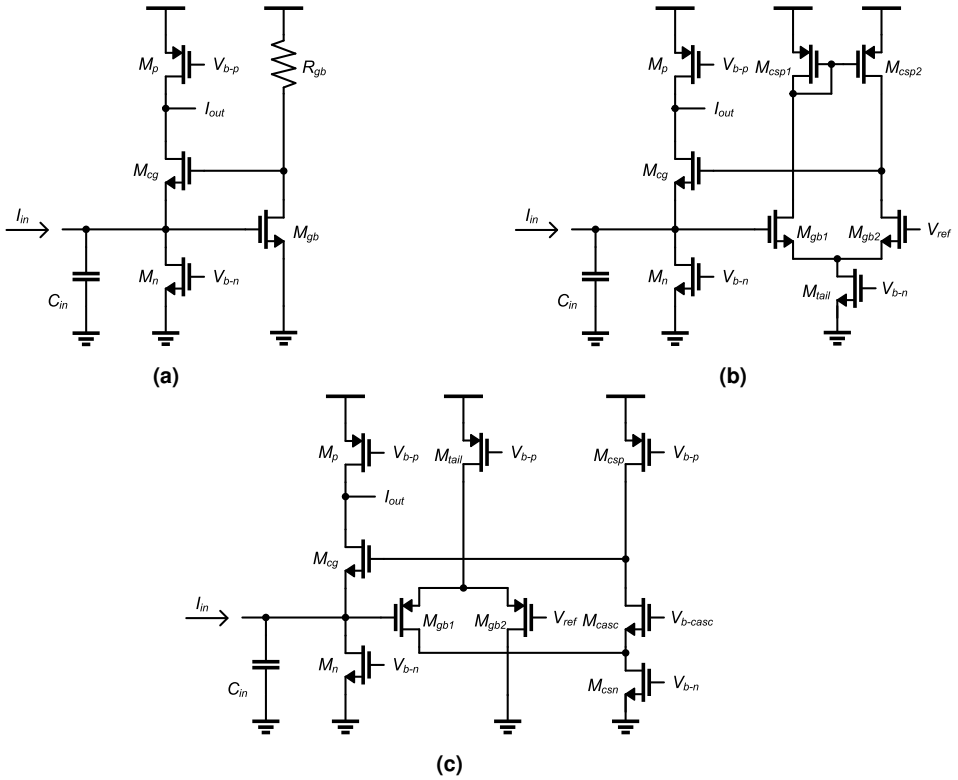


Figure 5.2: Considered gain-booster configurations: (a) Common source, (b) Differential pair, (c) Folded cascode

Noise

The RCG-stage exists out of 2 distinct circuit parts, the GC-branch and the gain-booster. These circuit elements will both contribute to the input-referred noise of the amplifier and an optimum noise performance can be found. This can be done by scaling the CG-branch and gain-booster against each other. The noise analysis of the front-end from figure 5.2c is shown in equation 5.1. The contribution of the shunt-feedback amplifier was left out and will be discussed later. The 1/f noise was neglected in this model because the system has a high pass corner at $1MHz$, causing its contribution to be outside the band of interest.

$$\begin{aligned} I_{in-tot}^2 &= I_{n-Mp}^2 + I_{n-Mn}^2 + I_{n-Mcg-GB-Cpd}^2 + I_{n-Mcg}^2 \\ I_{in-tot}^2 &\approx 4kT\gamma g_{m-Mp} \\ &\quad + 4kT\gamma g_{m-Mn} \\ &\quad + \frac{4kT\gamma(g_{m-Mgb1} + g_{m-Mcsp})}{(g_{m-Mgb1} + g_{m-Mcsp})^2}\left[g_{m-Mn} + s(C_{in} + C_{gs-Mgb1})\right]^2 \\ &\quad + \frac{4kT\gamma(g_{m-Mcg} + g_{m-Mp})}{g_{m-Mcg}^2}\left[s(C_{gs-Mcg} + C_{gs-Mgb1})\right]^2 \end{aligned} \tag{5.1}$$

In equation 5.1 the first and second terms denote the noise contributions of the CG-branch current sources. These directly add to the input-referred noise, the PMOS-source directly adds because the RCG acts as a current buffer. The third term is the gain-booster's input-referred noise contribution. High values of C_{in} will gain up the noise towards higher frequencies. The large input capacitance will cause this term to become the dominant contributor. The fourth term is the contribution of M_{cg}, the relevant capacitances also introduce a noise gain towards higher frequencies. However the noise gain is limited because the total capacitance is significantly lower then C_{in}. Figure 5.3b

shows and example of this. The input-referred noise is plotted in function of frequency. Each noise contribution is shown, the impact of the noise gain is clearly visible at higher frequencies.
The result of the noise optimisation is shown in figure 5.3. Within the CG-branch g_{m-cg} is scaled by M, in the gain-booster $g_{m-gb1/2}$ and its cascode g_{m-casc} are scaled by M^{-1}, for both branches the NMOS and PMOS current sources are adjusted accordingly. In figure 5.3a the total input-referred noise at the bandwidth of $500MHz$ is shown in function of M. At low M-values the CG-stage has a small transconductance and a large noise contribution, the gain-booster on the other hand has large transconductances and its contribution is low, the CG dominates the noise. For increasing M the CG becomes stronger and conversely, the gain-booster weaker. As the multiplier increases, $I^2_{n-Mcg-GB-Cpd}$ increases more rapidly compared to I^2_{n-Mcg} and at high multiplier values the gain-booster will become dominant.

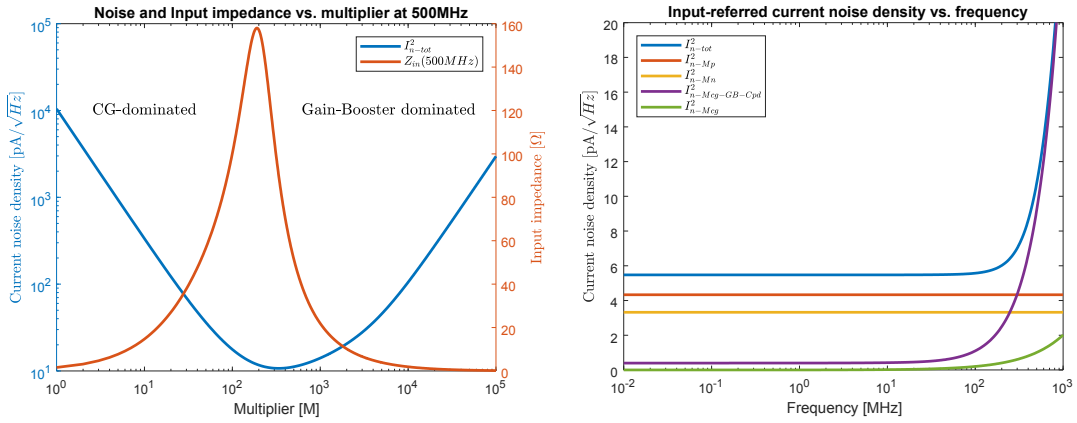


Figure 5.3: (a) CG-stage & Gain-booster scaling vs. noise, (b) Current noise spectral density vs. frequency (M=295)

Figure 5.3a shows the noise and input impedance as a result of a sweep of the scaling parameter M. An optimum is found at $M = 295$ where the combination of the CG-stage and gain-booster reach a minimum while maintaining the required gain and bandwidth. Figure 5.3b shows the contributions and total input-referred noise in function of frequency at the optimum. A final optimised input-referred noise of $12.17pA/\sqrt{Hz}$ at the bandwidth of $500MHz$ is reached in post-layout simulations. The optimised design, from figure 5.2c, with the respective scaling factor is simulated. The final simulated transconductances, parasitic capacitance and output resistances are shown in table 5.2 and 5.3 respectively.

Parameter	Value
g_{m-cg}	$\approx 2mS$
g_{m-p}	$\approx 1.5mS$
g_{m-n}	$\approx 1.5mS$
$g_{m-gb1/2}$	$\approx 50mS$
$r_{o-gb1/2}$	$\approx 45\Omega$
g_{m-casc}	$\approx 50mS$
r_{o-casc}	$\approx 45\Omega$

Table 5.2: Gain-boosted CG-stage designed transconductances

Parameter	Value
C_{d-Mcg}	$\approx 7fF$
C_{gs-Mcg}	$\approx 10fF$
C_{db-p}	$\approx 30fF$
$C_{gs-Mgb1/2}$	$\approx 300fF$
$C_{gs-Mcasc}$	$\approx 200fF$
$C_{d-Mcasc} = C_{gd-Mcasc} + C_{db-Mcasc}$	$\approx 300fF$
$C_{d-Mcsn} = C_{gd-Mcsn} + C_{db-Mcsn}$	$\approx 2.4pF$
$C_{d-Mcsp} = C_{gd-Mcsp} + C_{db-Mcsp}$	$\approx 2.4pF$

Table 5.3: Gain-boosted CG-stage parasitic capacitances

Stability

The RCG-input stage has 3 poles, meaning care must be taken not to create an unstable feedback system. The gain-boosting loopgain is described by equation 5.2, 3 poles are present in the denominator:

$$A_{LP} = \frac{-A_{gb}}{\left(\frac{s(C_{in}+C_{gs-Mgb1})}{g_{m-Mcg}}+1\right)\left(\frac{s(C_{gs-Mcasc}+C_{d-Mcsn})}{g_{m-Mcasc}}+1\right)\left(s(C_{d-Mcasc}+C_{d-Mcsp})r_{o-Mcasc}+1\right)} \quad (5.2)$$

The first, dominant pole (f_d) is caused by the total input capacitance and CG transconductance. A second, non-dominant pole (f_{nd1}) is caused at the output node of booster amplifier caused by the drain-bulk capacitances of load (M_{csp}) and cascode (M_{casc}) in combination with the output resistance. A third, non-dominant pole (f_{nd2}) is located at the folding node caused by its parasitic capacitances and the cascode transconductance (M_{casc}). Figure 5.4 shows the asymptotic loopgain.

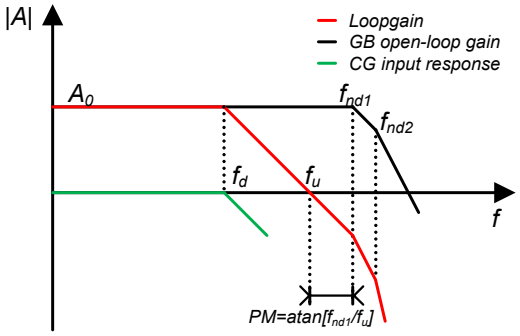


Figure 5.4: Gain-boosted common-gate stage loopgain

$$f_u \approx \frac{A_{gb}g_{m-Mcg}}{2\pi(C_{in}+C_{gs})} \quad (5.3)$$

$$PM = arctan\left[\frac{f_{nd1}}{f_u}\right] \approx 63^\circ \quad (5.4)$$

Using the designed transconductances and parasitic capacitances as defined in table 5.2 and 5.3 an estimate of the phase margin of the loop can be made. The dominant pole is located at a frequency of $f_d \approx 140MHz$, the first non-dominant pole $f_{nd1} \approx 1.36GHz$ and the second non-dominant pole is at $f_{nd2} \approx 3.06GHz$. With $A_{gb} \approx 5x$, this yields a unity gain frequency $f_u \approx 700MHz$ which is spaced sufficiently far away from f_{nd1} yielding a phase margin of $\approx 63^\circ$ (equation 5.4).

5.1.2 Shunt-feedback stage

The shunt-feedback stage is implemented as shown in figure 5.1. Due to the shielding form the RCG, the feedback resistance and hence transimpedance gain can be maximised. The design is implemented according to the specifications, additionally the feedback resistance is made selectable such that the TIA gain is programmable. The drawback is that the selection switches will contribute some parasitic capacitances. Therefore the switches are designed with low capacitance $C_{switch} \approx 10fF$ at the drain or source, the trade-off is that a higher on resistance ($\approx 500\Omega$) must be tolerated. The gain ranges are implemented with a $2dB$ step, using 4 selectable resistors a total tuning range of $6dB$ is available.

Gain & Bandwidth

The circuit design is based upon the 5T amplifier as shown in the feasibility study with a nominal feedback resistor $R_f = 18k\Omega$. Designing for the desired bandwidth, the capacitance of the virtual ground must be estimated:

$$C_{vg} = C_{gs-M1} + C_{d-Mcg} + C_{d-p} + 4C_{switch} \approx 100fF \quad (5.5)$$

Where C_{gs-M1} is the 5T's amplifier input capacitance, C_{d-Mcg} and C_{d-Mcg} constitute the RCG output capacitance seen at the drain and consisting of the gate-drain and drain-bulk capacitances, C_{switch} is the capacitance of the switch. An estimate is made using the values of table 5.3.
The output capacitance will set the second pole in the system, the main contributors consist of the drain capacitances of M_1 & M_3 of the 5T amplifier, the capacitance of the switches (C_{switch}) and the load capacitance formed by the next stage ($C_{load} \approx 100fF$):

$$C_{out} = C_{load} + C_{d-M1} + C_{d-M3} + 4C_{switch} \approx 200fF \tag{5.6}$$

The implementation of the amplifier as shown in figure 4.6. The transconductances of the differential pair transistors was chosen $g_{m1/2} \approx 12mS$, the current source load was designed accordingly yielding a large gain-bandwidth of $\approx 10GHz$ with a gain of $\approx 15dB$.
The design was carried out for the nominal gain range first, additional resistances were added and tuned to result in the $2dB$ steps; table 5.4 shows the results. Due to the changing resistance, the bandwidth will change accordingly however since the damping-factor is not exactly $1/\sqrt{2}$ bandwidths are verified using simulations.

Gain	R_f	Z_{TIA}	B_w
Gain 1	$15k\Omega$	$82dB\Omega$	646MHz
Gain 2 (Nom.)	$18k\Omega$	$84dB\Omega$	590MHz
Gain 3	$24k\Omega$	$86dB\Omega$	511MHz
Gain 4	$32k\Omega$	$88dB\Omega$	442MHz

Table 5.4: RCG + Shunt-feedback TIA with selectable feedback resistance values (R_f) and their resulting transimpedance gain

Linearity

In the design no specific linearity precautions were taken because the maximum signal amplitude at the output will only be $\approx 14mV_{pk}$. Combined with the slightly larger overdrive voltage used ($V_{gs} - V_{th} \approx 250mV$) linearity degradation is minimal and in nominal conditions an $SFDR \approx 44dB$ is reached. However as offset currents generated in the RCG flow through the feedback resistance, degradation occurs when selecting the highest gain range, but the SFDR does not degrade below $40dB$.

Noise

The shunt-feedback TIA and its feedback resistance add noise directly to the front-end input because the RCG has a current gain that is unity. Equation 5.7 shows input-referred noise of the shunt-feedback stage.

$$I^2_{in-TIA} = I^2_{n-Rf} + I^2_{n-amp} \approx \frac{4kT}{R_f} + \frac{8kT\gamma g_{m-M1}}{g^2_{m-M1}} \cdot \left[sC_{vg}\right]^2 \tag{5.7}$$

Using the circuit's nominal settings and parameters as determined above, the noise $I^2_{in-TIA} \approx 1.2pA/\sqrt{Hz}$, at a bandwidth of $500MHz$. With the RCG noise contribution of $\approx 12.17pA/\sqrt{Hz}$, the noise of shunt-feedback stage is negligible.

Stability

The last parameter of the shunt-TIA is its stability. The feasibility study showed 2 possible pole placement possibilities. The implemented shunt-feedback TIA makes use of a pole placement

where the feedback network causes a first dominant pole (f_d) and the amplifier a second non-dominant pole (f_{nd}) as described by equations 5.8 and 5.9.

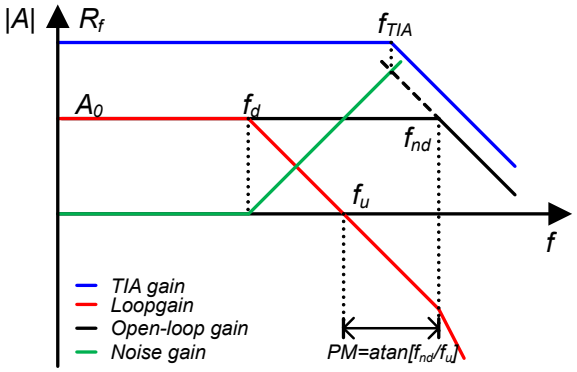


Figure 5.5: Asymptotic transimpedance gain and loopgain

$$f_d \approx \frac{1}{2\pi C_{in} R_f} \tag{5.8}$$

$$f_{nd} \approx \frac{1}{2\pi C_{out} r_{o1} || r_{o3}} = \frac{g_{m1/2}}{2\pi C_{out} A_0} \tag{5.9}$$

$$f_u \approx \frac{A_0}{2\pi C_{in} R_f} \tag{5.10}$$

$$PM = arctan\left[\frac{f_{nd}}{f_u}\right] \qquad PM \approx 74^\circ \tag{5.11}$$

The stability is guaranteed by shifting the amplifier's pole (f_{nd}) towards higher frequency such that both poles are sufficiently spaced apart. This approach is shown in figure 5.5. It is chosen over the feedback capacitor approach because its capacitance value becomes too small ($\approx 7fF - 15fF$) for high bandwidth applications. This causes it to become indistinguishable from parasitic capacitances and as a result it complicates the design in lay-out.
The stability is assessed using the phase margin. Using the parameters as determined before and applying equations 5.8 to 5.11 yields a phase margin $PM \approx 74^\circ$. The first pole of the loopgain is located at $f_d \approx 88MHz$, the non dominant pole caused by the amplifier is located at $f_{nd} \approx 1.8GHz$. The dominant pole shifts depending on the feedback resistance, as a result the phase margin also changes. The worst case occurs at the lowest gain yielding a minimum phase margin of $PM \approx 71^\circ$.

5.1.3 Design summary & results

The RCG and the shunt-feedback stages are designed, optimised and implemented as explained in the previous sections. The design is thoroughly simulated for each of the categories, gain, bandwidth, noise, linearity and stability over all process corners and the full temperature range $-40^\circ C - 125^\circ C$. Figure 5.6 shows the post-layout simulation results for the transfer function (5.11a), input impedance (5.11b) and noise (5.11c) in the nominal process corner over the full temperature range.
Detailed post-layout simulation results are shown in table 5.5. In this table the column indicated with 'Typ' indicates the results for nominal operating conditions at room temperature (27°) in the nominal corner. The 'Min' and 'Max' values indicate the lowermost and uppermost extreme value that occurs over the different corners and the temperature range. Under nominal conditions the TIA reaches a transimpedance of $82dB\Omega$ with a bandwidth of $578MHz$, the noise performance reaches $12.8pA/\sqrt{Hz}$ at $500MHz$. Alternatively the effective input-referred noise is $I_{n-eff} = I_{n-rms}/\sqrt{B_w} \approx 10pA/\sqrt{Hz}$. These results closely match the targeted requirements. The linearity shows and SFDR in excess of $40dB$ for signals $\approx 2I_{in-max-pk}$.
The characteristics as shown in figure 5.6 are as expected. The TIA transfer function from figure 5.11a shows a flat response with limited peaking near the bandwidth. The peaking does not increase the dc gain more than $0.2dB$ from the DC-gain. The input-referred noise, as shown in figure 5.11c, matches the simulations from figure 5.3b. Towards higher frequencies the noise increases as expected, at lower frequencies the effect of the flicker noise becomes apparent. Flicker noise was not included in the model used to obtain the results shown in figure 5.3b. However in this application, lower frequencies also coincide with a sufficiently high SNR values such that the

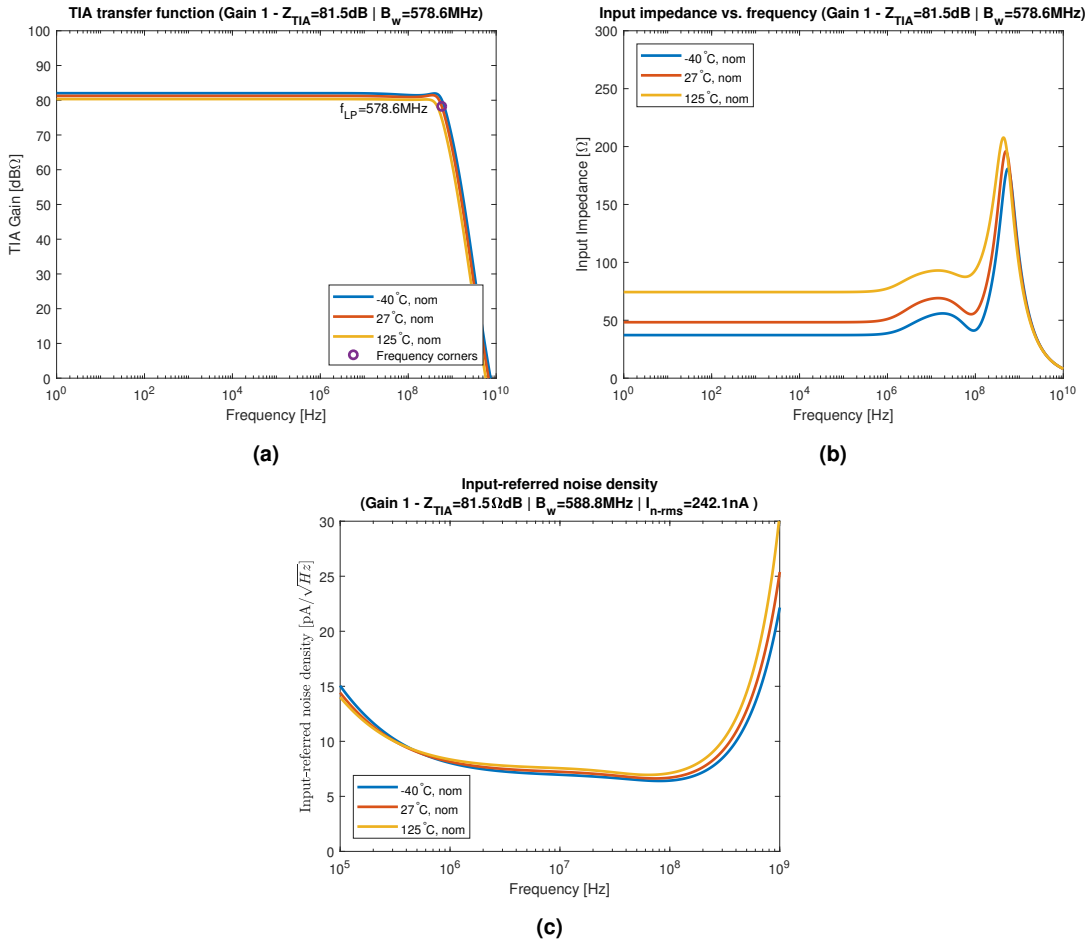


Figure 5.6: Nominal operation: (a) TIA transfer function, (b) Input impedance vs. frequency, (c) Input-referred noise current vs. frequency

performance is not affected. Figure 5.11b shows the input impedance in function of frequency. The impedance shows peaking around $578MHz$ (the bandwidth of the circuit), this is caused by the roll-off of the gain-boosting loop as described by equation 5.2 and figure 5.4. As the dominant pole takes effect, the gain rolls off and the circuit loses its ability to perform gain boosting. When the loopgain reaches unity, the input impedance reaches $1/g_{m-cg}$. However the bandwidth of the circuit is reached before the impedance can settle to this value and the roll-off of the full TIA causes the input impedance to reduce again.

AC-Properties

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
B_w	-3dB bandwidth	Gain0, T=-40°C-125°C, $C_{in} = 2pF$, $C_{out} = 1pF$	493	**605**	694	MHz
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $C_{out} = 1pF$	440	**578**	648	MHz
		Gain2, T=-40°C-125°C, $C_{in} = 2pF$, $C_{out} = 1pF$	450	**504**	540	MHz
		Gain3, T=-40°C-125°C, $C_{in} = 2pF$, $C_{out} = 1pF$	327	**411**	440	MHz
Z_{TIA}	Transimpedance	Gain0, T=-40°C-125°C, $C_{in} = 2pF$, $C_{out} = 1pF$	76	**80**	83	dBΩ
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $C_{out} = 1pF$	78	**82**	84	dBΩ
		Gain2, T=-40°C-125°C, $C_{in} = 2pF$, $C_{out} = 1pF$	80	**84**	85	dBΩ
		Gain3, T=-40°C-125°C, $C_{in} = 2pF$, $C_{out} = 1pF$	79	**85**	87	dBΩ
Z_{in}	Input Impedance	Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 1MHz$	20	**51**	98	Ω
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 10MHz$	44	**69**	72	Ω
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 100MHz$	37	**57**	111	Ω
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 200MHz$	67	**89**	143	Ω
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 300MHz$	100	**134**	181	Ω
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 400MHz$	138	**179**	190	Ω
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 500MHz$	166	**196**	202	Ω
I_n	Input-referred current noise density	Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 1MHz$	7.7	**8.1**	9.9	$pA/\sqrt{Hz}$
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 10MHz$	7.0	**7.2**	7.8	$pA/\sqrt{Hz}$
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 100MHz$	6.3	**6.7**	7.3	$pA/\sqrt{Hz}$
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 200MHz$	7.2	**7.6**	8.4	$pA/\sqrt{Hz}$
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 300MHz$	8.5	**9.1**	10.3	$pA/\sqrt{Hz}$
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 400MHz$	10.0	**10.8**	12.4	$pA/\sqrt{Hz}$
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $f = 500MHz$	11.7	**12.8**	15.1	$pA/\sqrt{Hz}$
I_{n-rms}	Integrated Input-referred noise	Gain0, T=-40°C-125°C, $C_{in} = 2pF$	227	**255**	269	$nArms$
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$	200	**242**	285	$nArms$
		Gain2, T=-40°C-125°C, $C_{in} = 2pF$	94	**204**	211	$nArms$
		Gain3, T=-40°C-125°C, $C_{in} = 2pF$	74	**167**	175	$nArms$
I_{n-eff}	Effective input-referred noise $I_{n-eff} = I_{n-rms}/\sqrt{B_w}$	Gain0, T=-40°C-125°C, $C_{in} = 2pF$	9.8	**10.3**	10.6	$pA/\sqrt{Hz}$
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$	9.4	**10.0**	10.3	$pA/\sqrt{Hz}$
		Gain2, T=-40°C-125°C, $C_{in} = 2pF$	7.5	**9.1**	9.5	$pA/\sqrt{Hz}$
		Gain3, T=-40°C-125°C, $C_{in} = 2pF$	7.5	**8.3**	8.7	$pA/\sqrt{Hz}$
$SFDR$	Spurious free Dynamic range (no-noise, $f = 35MHz$)	Gain0, T=-40°C-125°C, $C_{in} = 2pF$, $1.7\mu Apk$	42	**45**	55	dB
		Gain1, T=-40°C-125°C, $C_{in} = 2pF$, $1.7\mu Apk$	40	**44**	58	dB
		Gain2, T=-40°C-125°C, $C_{in} = 2pF$, $1.7\mu Apk$	42	**42**	55	dB
		Gain3, T=-40°C-125°C, $C_{in} = 2pF$, $1.7\mu Apk$	40	**41**	58	dB

DC-Properties

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ib}	Input bias voltage	T= 27°C, (nom)		**251**		mV
		T=-40°-125°C	222		500	mV
V_{out}	Output DC voltage	Gain0, T= 27°C, (nom)		**936**		mV
		Gain0, T=-40° - 125°C	686		936	mV
		Gain1, T= 27°C, (nom)		**925**		mV
		Gain1, T=-40° - 125°C	650		925	mV
		Gain2, T= 27°C, (nom)		**903**		mV
		Gain2, T=-40° - 125°C	686		944	mV
		Gain3, T= 27°C, (nom)		**883**		mV
		Gain3, T=-40° - 125°C	732		938	mV

Table 5.5: TIA post-layout simulation results

5.2 Gain-Stage

The gain stage is implemented as envisaged in the architecture study and features 2 open-loop stages each with a gain of $\approx 10.5dB$ and a bandwidth of $\approx 1.7GHz$. In the following sections only a single gain-core amplifier implementation is shown. The simulation results presented consider the 2 stage amplifier.

5.2.1 Gain core implementation

The full circuit implementation for a single gain-core is shown in figure 5.7. The stage consists of an NMOS differential pair with diode connected NMOS loads. Using NMOS for the high and low side devices mitigates the effects of PVT variations. Both the $M_{1/2}$ and $M_{nd1/2}$ devices are impacted equally and as a result the variability of the gain is reduced. Additionally current sources are used to inject additional current into M_1 and M_2 to boost higher transconductance and achieve higher gain and bandwidth.

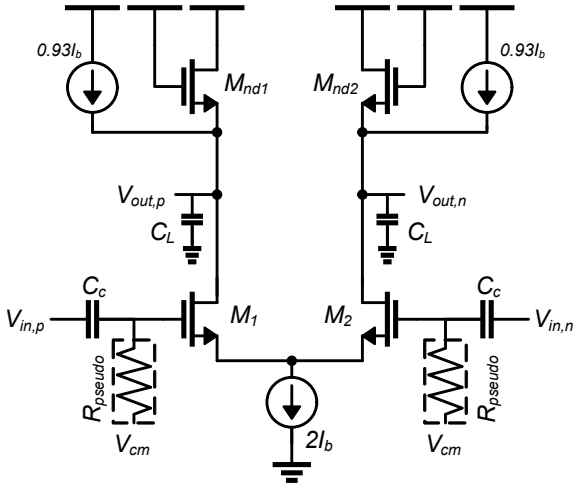


Figure 5.7: Gain-core differential amplifier implemented with NMOS over NMOS transistors and parallel current sources

Gain & Bandwidth

The gain of the amplifier is determined by the transconductance ratio's of the NMOS pair and their NMOS diode loads, hence $A_0 \approx g_{m1}/g_{m-nd1}$. By injecting current into the drains of $M_{1/2}$ bigger ratio's and higher gains can be accomplished. The output resistances will cause the gain to deteriorate, however they are neglected in this approximation. With an output capacitance of $C_L \approx 1pF$ the required gain-bandwidth ($G_{bw} \approx 6GHz$) is reached with a transconductance of $g_{m1/2} \approx 40mS$. To reach the $10.5dB$ gain, a $g_{m-nd1} \approx 12mS$ is needed with $\approx 7\%$ of the drain current of $M_{1/2}$ used for the diode while the remaining $\approx 93\%$ is injected by PMOS current sources.
The first drawback is the bulk-effect of the diodes ($M_{nd1/2}$) which increases the effective transconductance but degrades the gain. Further degradation is caused by the finite output resistances of the diodes, current sources and the input pair ($M_{1/2}$). However, the physical design showed additional series resistances in the source and drain contacts of $M_{nd1/2}$ and $M_{1/2}$ which in turn increase the gain. A second drawback is the insertion loss, a $\approx 1dB$ attenuation is caused by the AC-coupling and biasing. To overcome these drawbacks the circuit was optimised using an iterative approach by designing a layout and adjusting the schematics accordingly to reach the required performance in post-layout simulations. The current sources have a high output impedance and the transconductance $g_{m1/2}$ is tuned to compensate for parasitic capacitance and gain degradation.

This results in an over-design compared the initial estimation yielding $g_{m1/2} \approx 63mS$. This results in a higher gain of $\approx 12dB$ compensating for the mentioned non- idealities.

Linearity

The linearity of the circuits was ensured by biasing the input transistors using an overdrive $V_{gs} - V_{th} \approx 300mV$. The gain-stage's worst-case input amplitude is $V_{in-pk} \approx 100mV$, using a higher overdrive voltage keeps the devices in saturation under all circumstances. The loads are biased ensuring a minimum $V_{gs} = V_{ds} \approx 450mV$. These bias conditions set the operating point to a flat, more linear, part in the output characteristic compared to lower overdrive voltages. The output common mode voltage was set to be $\approx 750mV$ to accommodate a maximum output amplitude of $\approx 300mV$. The result is that the full signal swing and the noise can propagate through the chain while maintaining the required linearity.

Noise

The input-referred voltage noise of the amplifier is dominated by the channel noise of the input transistors $M_{1/2}$ and the loads $M_{nd1/0}$ with their current sources as described by equation 5.12:

$$V_n^2 = 8kT\gamma\Big[\frac{1}{g_{m1}} + \frac{g_{cs} + g_{nd1}}{g_{m1}^2}\Big] \leq 1nV/\sqrt{Hz} \tag{5.12}$$

In equation 5.12 g_{m1}, g_{m-nd1} and g_{m-cs} respectively represent the transconductances of the input devices, the diode loads and current sources. With the transconductances fixed by the gain and bandwidth, by design, the noise is below the required $1nV/\sqrt{Hz}$.

5.2.2 Gain core biasing

The amplifier core is part of a 2-stage AC-coupled amplifier as shown in the architecture study. Each stage is biased at the common-mode voltage $V_{cm} \approx 1V$ which is generated by a diode connected NMOS device. The bias voltage is connected to the amplifier inputs by means of the resistance R_{psuedo}. In combination with the coupling capacitance C_c it will set the high-pass corner. The resistors are designed to reach $R_{pseudo} \approx 1M\Omega$ such that in combined with $C_c = 1pF$ a high-pass corner of $f_{HP} \approx 160kHz$ is reached.

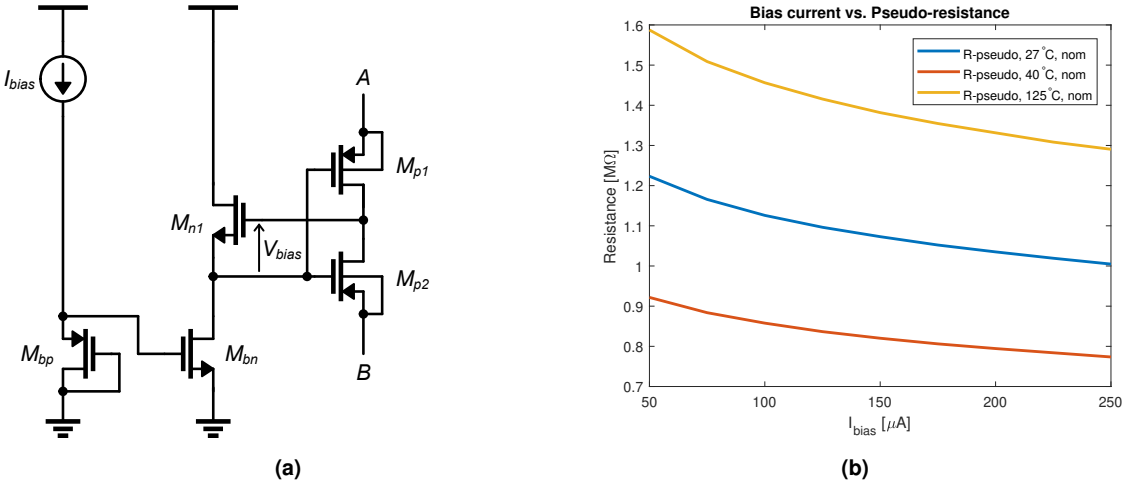


Figure 5.8: (a) Implementation of the pseudo-resistor (b) Simulation of a bias current vs. the pseudo-resistance.

The resistance is implemented as a pseudo resistance consisting of PMOS-devices operating in their ohmic region. Implementing the required $1M\Omega$ using conventional poly resistors would result in a large area usage $\approx 32\%$ of the gain-stage cell. The implemented circuit is shown in figure 5.8a, these structures are typically applied in biomedical applications[24] and discussed in [45] and [11]. The pseudo-resistor as shown in figure 5.8a is a set of back-to-back PMOS devices between A and B, operated in their ohmic/triode region as introduced by [12]. PMOS devices are used because they are located within an N-well such that a floating structure is formed. Since this resistor is used to bias the gate of an NMOS device it carries very low currents ($< 1nA$) causing a $V_{ds-p1/2} \approx 0V$. With nodes A and B biased at $V_{A/B} \approx 1V$ the drains of $M_{p1/2}$ can be assumed to have the same voltage. As a result also $V_{g-Mn1} \approx 1V$, a drain current through M_{n1} maintains a positive bias voltage $V_{bias} = V_{gs-Mn1}$. Since $V_{g-Mp1/2} < V_{A/B}$, the $M_{p1/2}$ structure is in its ohmic region. By varying I_{ds-Mn1}, the bias voltage V_{bias} is controlled, in turn it controls the biasing of $M_{p1/2}$ and hence the pseudo-resistance. The pseudo current-mirror consisting of M_{bn} and M_{bp} offers a first order compensation for process variations.

5.2.3 Design summary & results

Simulations are obtained by cascading 2 gain-cores as depicted in figure 5.7 with a load capacitance $C_L = 1pF$. Figure 5.9 shows the performance for both a single gain-core and the total gain-stage. Performance numbers over process and temperature corners of the gain-stage are shown in table 5.6.

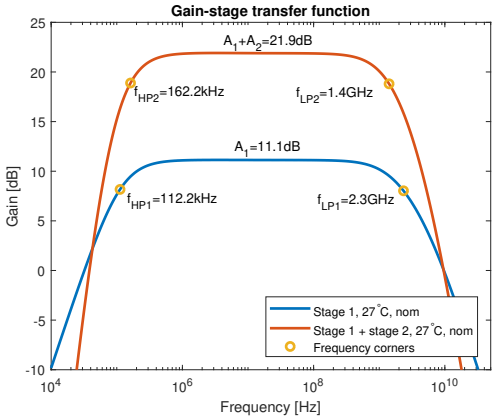


Figure 5.9: Gain-stage, post-layout transfer function ($C_L = 1pF$)

The design has a bandwidth of $1.4GHz$ and a gain of $21.9dB$, slightly higher than the specifications. It can be seen that the gain of the circuit only varies $\approx 0.3dB$ nominally over temperature and $\approx 3dB$ over all corners, bandwidth and cut-off frequencies vary accordingly. This is the drawback of the parallel current injection since the PMOS current sources do not vary with the NMOS loads.
The noise of the gain-stage is not determined separately as, by design, it is within the specifications. With a calculated input-referred noise of $\approx 1nV/\sqrt{Hz}$ per gain-core it will not contribute significantly to the overall system. Additionally the input-referred offset of a single amplifier stage is measured to be $8.40mV$.

AC-Properties

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
A_{DC}	Voltage gain	T=-40°C, $C_c = 1pF, C_L = 1pF$	20.8	**22.0**	23.9	dB
		T= 27°C, $C_c = 1pF, C_L = 1pF$	20.6	**21.9**	23.7	dB
		T=125°C, $C_c = 1pF, C_L = 1pF$	20.4	**22.1**	23.5	dB
f_{LP}	High-frequency low-pass corner	T=-40°C, $C_c = 1pF, C_L = 1pF$	1.38	**1.62**	1.82	GHz
		T= 27°C, $C_c = 1pF, C_L = 1pF$	1.23	**1.41**	1.62	GHz
		T=125°C, $C_c = 1pF, C_L = 1pF$	1.05	**1.18**	1.38	GHz
f_{HP}	Low-frequency high-pass corner	T=-40°C, $C_c = 1pF, C_L = 1pF$	170	**219**	257	kHz
		T= 27°C, $C_c = 1pF, C_L = 1pF$	126	**162**	200	kHz
		T=125°C, $C_c = 1pF, C_L = 1pF$	93	**120**	145	kHz

DC-Properties

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{i-cm}	Input common mode voltage	T= 27°C, (nom)		**1.02**		V
		T=-40°C	0.98	1.08	1.20	V
		T= 27°C	0.91	1.02	1.13	V
		T=125°C	0.82	0.92	1.04	V
V_{o-cm}	Output common mode voltage	T= 27°C, (nom)		**0.78**		V
		T=-40°C	0.65	0.74	0.84	V
		T= 27°C	0.67	0.78	0.87	V
		T=125°C	0.74	0.85	0.95	V
$V_{i,os}$	Input-referred offset	T= 27°C, (nom)		**8.40**		mV

Table 5.6: Gain-stage post-layout simulation results

5.3 Output buffer

The final stage in the signal chain is an output buffer. The purpose of this buffer is to drive the output signal off-chip onto the PCB. Because routing signals off-chip typically introduces a significant amount of capacitance, a stronger driver is needed. The preceding gain-stage is only intended to drive the on-chip $\approx 1pF$ load presented by the initial estimate for the ADC input capacitance. The output buffer was also re-used as a stronger ADC driver. The final ADC implementation showed higher input capacitance than initially estimated. After the consolidation of the AFE and ADC designs a significant amount of kick-back noise was present in the system. The use of the buffer as an ADC driver mitigates the performance degradation. Additionally, the buffer adjusts the DC level to the required $750mV$ and $1V$ DC-bias level for the ADC input.

5.3.1 Specifications

The capacitive load along with the bandwidth specification are the most important specifications, it is the starting point of the buffer design such that cascading the buffer does not significantly reduce the overall bandwidth. To estimate the final capacitive load, typical PCB design parameters and properties are applied. This is summarised in table 5.7.

Param.	Description	8-layer	4-layer
ε_r	Relative permittivity	4.6	
W	Track width	$0.15\mu m$	$0.25\mu m$
t	Track thickness	$35\mu m$	
h	Layer-to-layer spacing	$0.19\mu m$	$0.465\mu m$
C_0	PCB-track capacitance	$\approx$**0.45**pF/cm	$\approx$**0.92**pF/cm
C_L	Load cap. probe or buffer	$\approx 1pF$	
C_{ESD}	ESD-structure capacitance	$\approx 0.6pF$	
C_{L-tot}	Load cap. + PCB-track (3.5cm)	$\approx$**3**pF	$\approx$**5**pF

Table 5.7: PCB estimated track capacitance

The typical PCB technology parameters are available from manufacturers e.g. [2]. The load capacitance of the differential track is approximated to be $\approx 1pF$ which is a typical value for a probe or buffer [1] [3]. The capacitance due to the ESD structure is taken from the foundry specification. Estimates are made for a 8 or 6 layer PCB, using a differential track spacing rule of $S = 1.5W$. Using Hammerstad and Jensen[17], the capacitance per unit length is estimated. An adequate fan-out length of $\approx 3.5cm$ yields a worst-case capacitance of $5pF$.
The bandwidth requirement is set by the combination of the TIA and gain-stage bandwidths from table5.5 and 5.6. This dictates that a buffer bandwidth larger than $f_{-3dB-buffer} > 1.5GHz$ is required such that the full signal chain bandwidth is not degraded below $500MHz$.

5.3.2 Implementation

Initially source follower circuits were considered, however with the large input signal amplitude ($V_{in} \approx 300mV$) this circuit offers limited performance. The source follower should be designed with a large overdrive $V_{ov} \approx 400mV$ such that the signal does not push the device out of saturation. For an NMOS source follower, assuming $V_t \approx 0.4V$ and an output voltage of $\approx 0.75V$ the gate bias should be $V_{g-n} \approx 1.55V$. Using a PMOS device and assuming an output voltage of $\approx 1V$ yields a gate bias of $V_{g-p} \approx 200mV$. In both cases the source follower input bias is close to, or exceeds the supply. Biasing with a lower overdrive would alleviate this issue but at the cost of linearity.
The buffer is implemented as a pseudo-differential architecture, shown in figure 5.10. Each single-ended buffer is implemented as a differential pair with current source load. The input biasing of the buffer is done using pseudo-resistor and the signal is coupled using a capacitor. The bias voltage is set at $V_{cm} \approx 1V$, with $V_t \approx 400mV$, $V_{ds-Mb1} \approx 200mV$ and $V_{ov} \approx 0.4V$ the unity gain yields an output bias at $1V$. The buffer's output is DC-coupled to ADC inputs such that proper biasing is established. However, the buffer's output offset will corrupt the LSB's. To mitigate this issue, a copy of the output buffer is implemented such that its output voltage can be sensed and the ADC reference can be adjusted to eliminate this effect.

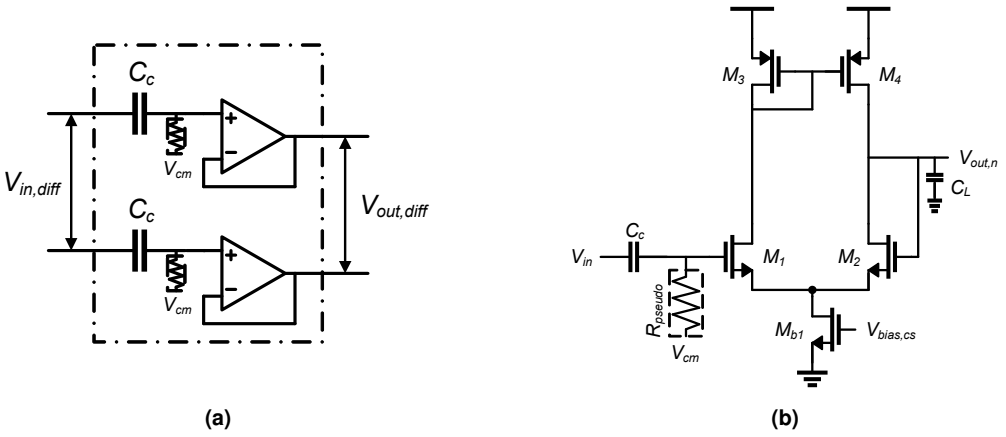


Figure 5.10: (a) Implementation of the pseudo-differential buffer (b) Single-ended (half-circuit) of the pseudo differential buffer

Gain & bandwidth

The final implementation was implemented such that a $\approx 2GHz$ bandwidth is reached when considering a $\approx 10pF$ single ended load or a $5pF$ differential load. Designing for double of the estimated output capacitance foresees sufficient overhead/flexibility to cope with different loading conditions. A transconductance of $g_{m1/2} \approx 125mS$ is needed to reach the specifications with a tail current of $25mA$, yielding a total power consumption of $75mW$. A minimum transistor length was chosen in

order to maximise the bandwidth however as a result the circuit of figure 5.10b only has limited open loop yielding in a slight a $\approx -0.8dB$ attenuation.

5.3.3 Design summary & results

The bandwidth and attenuation of the buffer are not separately simulated, rather they are verified within the full signal chain. Separate verification of the offset was performed. The worst-case post-layout results are presented in table 5.8. The differential offset is well controlled and lower than the ADC's $V_{LSB} \approx 8mV$. The systematic single-ended offset however is much larger.

Param.	Description	Value
$V_{os,diff}$	Differential input-referred offset voltage (1σ)	1.62mV
$V_{os,cm}$	Single-ended input-referred common mode offset (1σ of $V_{ocm} - V_{icm}$)	-31mV

Table 5.8: Post-layout offset voltage measurements

5.4 Full signal chain results & summary

The final performance characteristics of the full signal chain, the cascade of the TIA with the gain-stage and the output buffer, are summarised in table 5.9 and figure 5.11. The simulations are performed on post-layout extracted results of the full front-end layout including the pad-ring periphery with its ESD-protections, bond wires, photodiode capacitance and output capacitances. Table 5.9 shows the typical values with a performance under nominal supply, temperature and process corner conditions. The minimum and maximum values indicate the worst-case values over temperature and process corner variations.
The emphasised nominal performance parameters being the total transimpedance gain, the bandwidth, noise and linearity are within the set specifications. A combined gain of $\approx 103dB$ is reached, the addition of the output buffer drops the expected gain by $\approx 1dB$. The bandwidth reaches $\approx 505Mhz$, figure 5.11a illustrates the variation of both the gain and bandwidth over temperature.
The noise response in figure 5.11c as and reported in table 5.9 is meeting the specification. The spectral noise density is shown at specific frequency intervals at the bandwidth of $500MHz$ is nominally $13pA/\sqrt{Hz}$ and a worst case of $\approx 15pA/\sqrt{Hz}$ over the corner and temperature. This yields a good noise match to the balanced photodiode. Additionally the integrated input referred noise and effective input referred noise (I_{n-eff}) are reported.
The linearity is simulated using an input amplitude of $1.7\mu Apk$, $\approx 2x$ the maximum input current. This amplitude operates the signal chain at the onset of clipping (approximately the 1dB gain compression point). The performance numbers in table 5.9 are simulation results without noise in nominal operating conditions, with its nominal gain range (Gain1) the SFDR $\approx 46dB$, as predicted by the model of figure 4.2 in chapter4. Figure 5.11d shows that the SFDR drops to the simulated $\approx 30dB$ in the presence of noise. The worst-case SFDR is $\approx 16.9dB$ and occurs if, over corners and temperature, the signal chain obtains its largest gain. The clipping of the output signal then results in the degraded SFDR. For the Gain1-range, lowering the input amplitude to $890nApk$ show an SFDR improvement of $\approx 6dB$. This brings the linearity within the set specification, similar improvements are expected for the other gain-ranges.

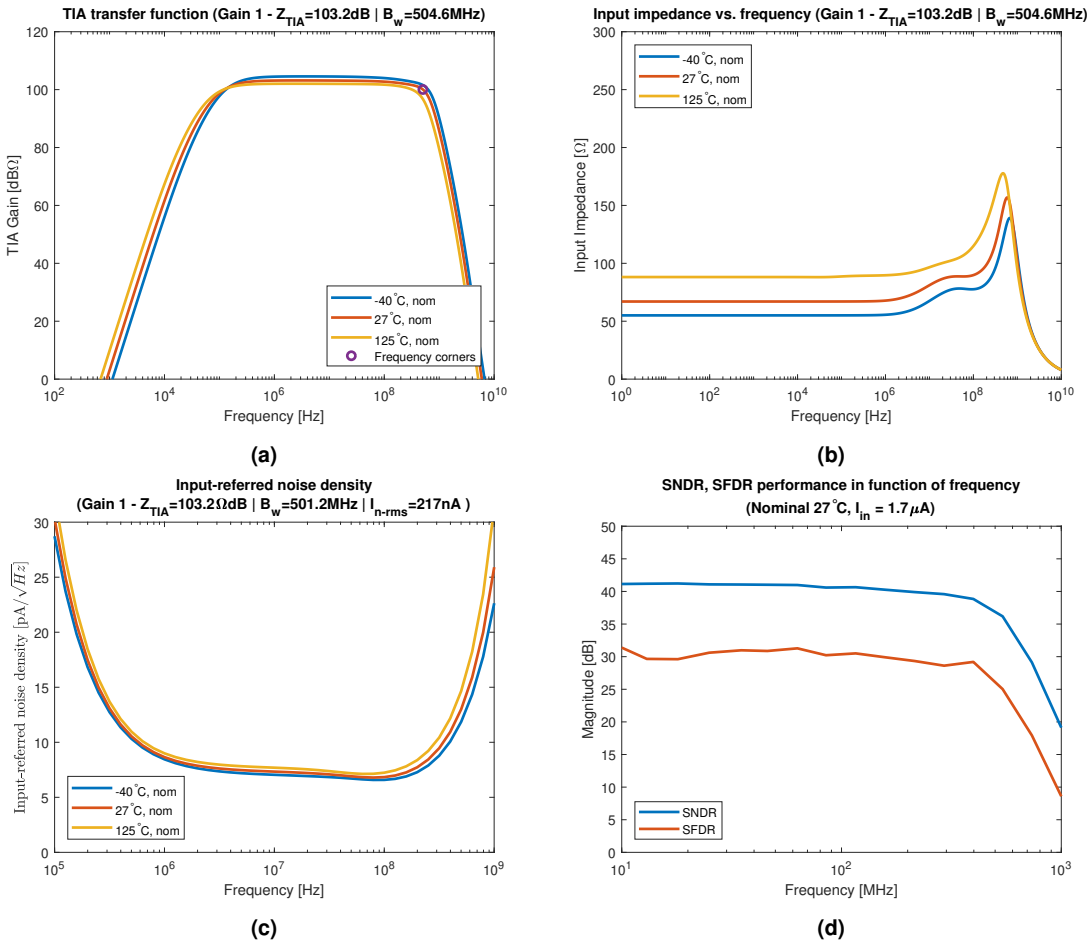


Figure 5.11: Nominal operation: (a) AFE transfer function, (b) Input impedance vs. frequency, (c) Input-referred noise current vs. frequency, (d) Spectral performance

AC-Properties

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
B_w	-3dB bandwidth ($B_w \approx f_{lp}$)	Gain0, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	411	**579**	634	MHz
		Gain1, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	267	**505**	528	MHz
		Gain2, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	110	**335**	324	MHz
		Gain3, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	98	**243**	255	MHz
f_{hp}	High-pass corner	Gain0, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	92	**126**	144	kHz
		Gain1, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	77	**128**	147	kHz
		Gain2, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	74	**126**	202	kHz
		Gain3, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	76	**128**	198	kHz
Z_{TIA}	Transimpedance	Gain0, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	95	**101**	105	dBΩ
		Gain1, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	97	**103**	107	dBΩ
		Gain2, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	99	**105**	109	dBΩ
		Gain3, T=-40°-125°, $C_{in} = 2pF, C_{out} = 5pF$	99	**107**	111	dBΩ
Z_{in}	Input Impedance	Gain1, T=-40°-125°, $C_{in} = 2pF, f = 1MHz$	52	**68**	108	Ω
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 10MHz$	66	**81**	119	Ω
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 100MHz$	74	**90**	135	Ω
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 200MHz$	78	**99**	174	Ω
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 300MHz$	110	**114**	162	Ω
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 400MHz$	152	**109**	139	Ω
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 500MHz$	125	**151**	193	Ω
I_n	Input-referred current noise density	Gain1, T=-40°-125°, $C_{in} = 2pF, f = 1MHz$	8.1	**8.7**	11.9	$pA/\sqrt{Hz}$
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 10MHz$	6.8	**7.3**	7.4	$pA/\sqrt{Hz}$
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 100MHz$	7.2	**6.8**	8.5	$pA/\sqrt{Hz}$
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 200MHz$	8.8	**7.7**	10.7	$pA/\sqrt{Hz}$
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 300MHz$	10.1	**9.5**	12.6	$pA/\sqrt{Hz}$
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 400MHz$	11.8	**10.9**	15.3	$pA/\sqrt{Hz}$
		Gain1, T=-40°-125°, $C_{in} = 2pF, f = 500MHz$	11.7	**13.0**	15.1	$pA/\sqrt{Hz}$
I_{n-rms}	Integrated Input-referred noise	Gain0, T=-40°-125°, $C_{in} = 2pF$	188	**218**	260	$nArms$
		Gain1, T=-40°-125°, $C_{in} = 2pF$	174	**217**	220	$nArms$
		Gain2, T=-40°-125°, $C_{in} = 2pF$	76	**141**	173	$nArms$
		Gain3, T=-40°-125°, $C_{in} = 2pF$	70	**118**	126	$nArms$
I_{n-eff}	Effective integrated input-referred noise $I_{n-eff} = I_{n-rms}/\sqrt{B_w}$	Gain0, T=-40°-125°, $C_{in} = 2pF$	9.1	**9.7**	10.7	$pA/\sqrt{Hz}$
		Gain1, T=-40°-125°, $C_{in} = 2pF$	8.1	**9.7**	9.8	$pA/\sqrt{Hz}$
		Gain2, T=-40°-125°, $C_{in} = 2pF$	7.0	**7.9**	8.7	$pA/\sqrt{Hz}$
		Gain3, T=-40°-125°, $C_{in} = 2pF$	6.7	**7.4**	7.2	$pA/\sqrt{Hz}$
$SFDR$	Spurious free Dynamic range (no-noise, $f = 35MHz$)	Gain0, T=-40°-125°, $C_{in} = 2pF, 1.7\mu Apk$	27.8	**49.9**	62.3	dB
		Gain1, T=-40°-125°, $C_{in} = 2pF, 1.7\mu Apk$	22.1	**46.4**	57.8	dB
		Gain2, T=-40°-125°, $C_{in} = 2pF, 1.7\mu Apk$	18.8	**37.5**	55.1	dB
		Gain3, T=-40°-125°, $C_{in} = 2pF, 1.7\mu Apk$	16.9	**35.4**	53.7	dB

DC-Properties

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ib}	Input bias voltage	T= 27°C, (nom)		**311**		mV
		T=-40°-125°C	181		419	mV
V_{out}	Output DC voltage	Gain0, T= 27°C, (nom)		**1.04**		V
		Gain0, T=-40° - 125°C	0.883		1.16	V
		Gain1, T= 27°C, (nom)		**1.03**		V
		Gain1, T=-40° - 125°C	0.873		1.16	V
		Gain2, T= 27°C, (nom)		**1.04**		V
		Gain2, T=-40° - 125°C	0.874		1.16	V
		Gain3, T= 27°C, (nom)		**1.04**		V
		Gain3, T=-40° - 125°C	0.874		1.16	V
V_{os}	Differential output offset voltage (1σ)	Gain1, T= 27°C, (nom)		1.62		mV
$V_{o,cm}$	Differential output common mode offset ($V_{ocm} - V_{icm}$)	Gain1, T= 27°C, (nom)		-31		mV
P_d	Dissipated power	Transimpedance stage		126		mW
		Gain stage		48		mW
		Output buffer		75		mW
		Total		250		mW

Table 5.9: Full chain post-layout simulation results

Chapter 6

Implementation

This chapter briefly discusses the layout of the AFE design. Secondly the top-level of the full chip is shown and the integration between the AFE and the ADC is discussed.
The front-end designed is integrated into a full chip together with an ADC. The ADC design is not part of this work, however for completeness, it is mentioned as part of the top-level design.

6.1 AFE-Layout

The annotated layout of the complete AFE is shown in figure 6.1. The AFE was implemented in an area of 1160μm x 585μm such that it fits within the pattern of the ADC layout. The various circuit blocks are implemented with a standard height, this makes interconnecting stages and supply routing straightforward. Power supplies are distributed using a metal mesh on layers 5 down to 2 limiting the voltage drop to 5mV. On-chip bypass capacitors are implemented using arrays of MOS-capacitors forming a 100pF capacitor. These capacitors are placed between the supply rails close to the circuitry. The coupling capacitors are implemented using MIM-capacitors unlike MOS-capacitors their capacitance is independent of bias conditions.

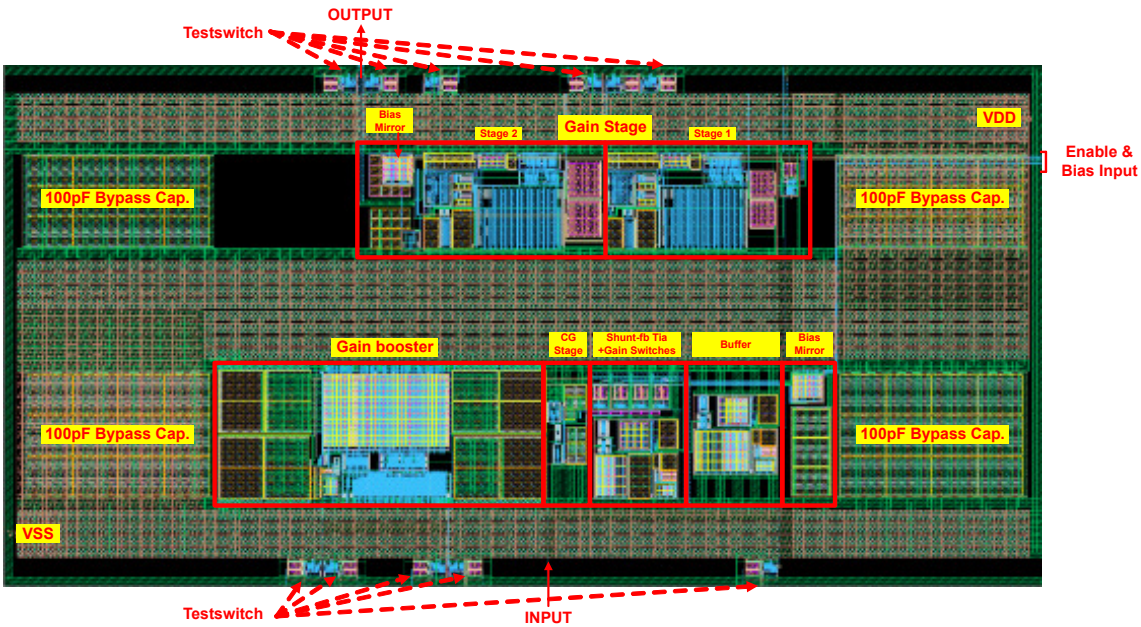


Figure 6.1: AFE-layout

The layout contains additional analogue multiplexers (DFT-MUX) to bring out internal nodes for debugging/testing purposes, should it be needed. Test switches are placed along the outside of

the AFE with their appropriate control signals. The drawback is that the test signals cross over the supply distribution lines. The inter-metal capacitance is minimised by retracting the supplies by $5\mu m$ from test signal lines.
The layout is designed carefully using a back-and-forth approach between layout and schematic optimisation ensuring the intended performance is maintained with the capacitances added by the layout. All performance characteristics shown in previous chapters are simulation results of post-layout circuits with the test infrastructure disabled.

6.2 Chip top-level design

6.2.1 Division of work

The final top level implementation combines the AFE and ADC in a single chip. The design is a collaborative effort between 2 designers. The top-level architecture and schematic implementation was realised as a part of this work and a brief overview is given in the following paragraphs. The layout was realised as a division between the chip-core and the padring. The padring is part of this work.

6.2.2 Top-level architecture

The simplified chip top-level schematic is shown in figure 6.2. A simplified representation of the AFE is shown in the bottom left. Above it, custom designed analogue multiplexing infrastructure is implemented. The bottom right shows the ADC's block schematic along with the required peripheral logic. Connecting the AFE and ADC is a buffered switching mechanism. The register interface, PLL and SerDes are implemented as black-box components available from silicon-proven standard IP-blocks.
The register interface consists of a 256-bit shift register controlled by 5 bondpads. Using such interface reduces the amount of bondpads needed to configure the chip. Individual register bits are distributed across the chip to configure the separate blocks.
The ADC and calibration are integrated as shown in figure 6.2. The ADC is an improved 6-bit, 1Gsps flash architecture with a reference of 0.5V. The ADC design is beyond the scope of this document. However the integration in the chip top-level is part of this work and integration was carried out according to the guidelines by the ADC designer. The calibration controls are originally intended to be controlled by bondpads. However due a shortage of bondpads, it was decided that the calibration logic is controlled by the register interface.
The buffer architecture consists of the output buffer connected to the input of the ADC and the input of a switch. This allows separate access to the AFE's output and ADC inputs. The AFE outputs can be accessed by simultaneously enabling the buffer and the switch. Decoupling the ADC is possible by permanently enabling its calibration mode (asserting the CAL-pin). Conversely by simultaneously disabling the output buffer and enabling the switch an external input signal can be provided to the ADC.
In the previous chapter it was noted that the output buffer has an output offset of $Vos \approx 31mV$ causing corruption of ≈ 4LSB's. To mitigate this, an identical copy of the buffer is employed and the offset can be measured on the VCM_OUT-bondpad. The measured value can then be used to build an external control loop to adjust the ADC's reference voltage ($VREF < P:N >$).
The serialisers and LVDS-driver IP-blocks send out the 6Gbps datatstream. To handle this datastream a total of 24 parallel LVDS drivers clocked at 250MHz are used. Additionally 2 LVDS source clocks are distributed along with the data to ease clock and data recovery on the receiving end.
The chip is clocked by a 10MHz reference clock. The on chip PLL IP-block generates the required 1GHz sampling clock as well as the multi-phase 250MHz required to clock the serialisers. The PLL

is auto-configured on start-up, however the registers can be used to change the settings should it be needed.

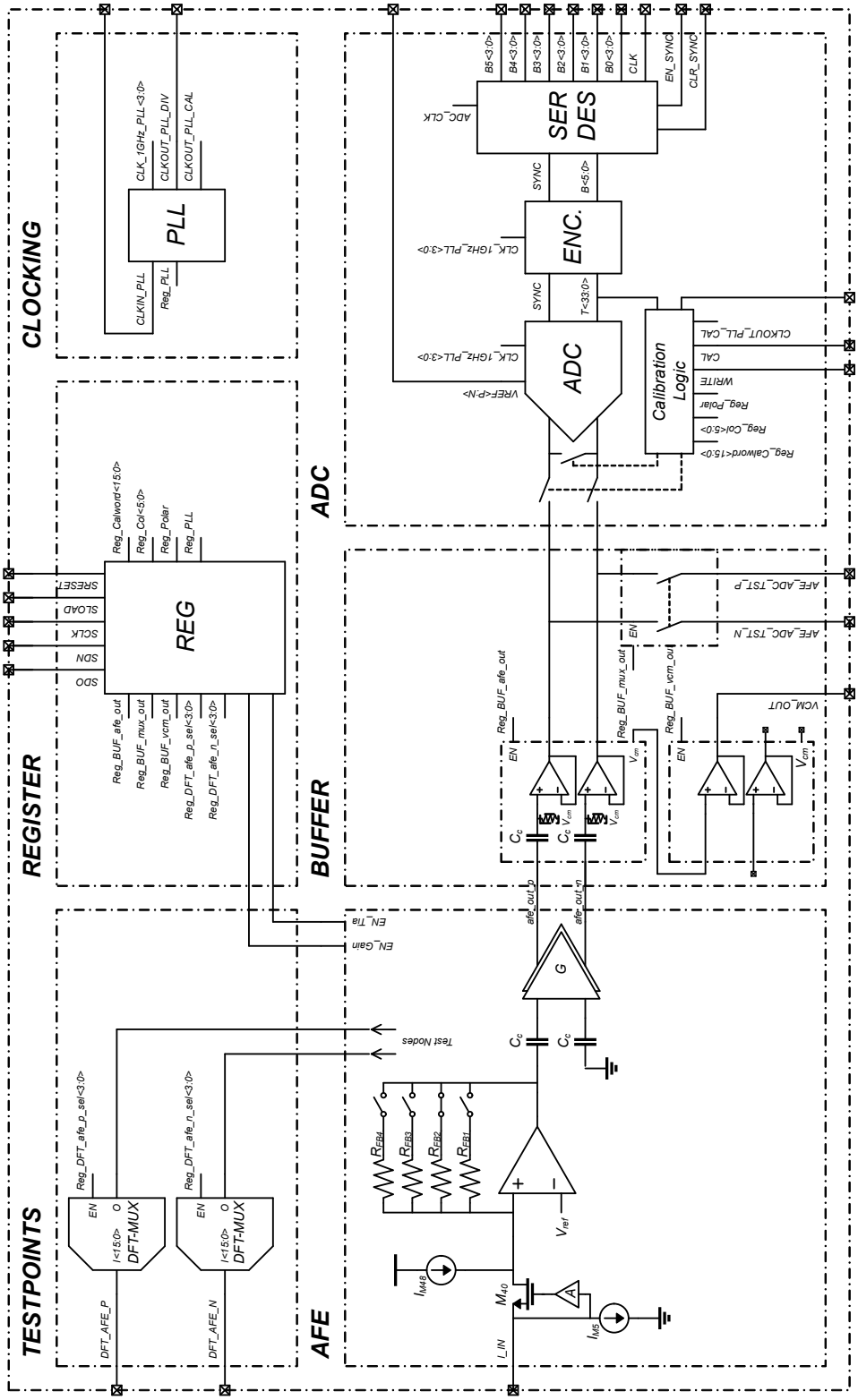


Figure 6.2: Chip top-level schematic

The chip has its power supply split in 5 different domains. The padring is powered by separate 3.3V and 1.5V supplies powering the ESD-protection structures, the LVDS drivers and the foundry

provided I/O. The PLL receives a separate 1.5V supply. Lastly the AFE, and ADC circuits receive separate analogue and digital 1.5V supplies.

6.2.3 Top-level implementation

Figure 6.3 shows the implementation of the full chip including the padring with the previously discussed blocks indicated. The chip core occupies 3.5x3.5mm, about 60% of the core area is used. The complete design including the padring is 5x5mm. The design is implemented using the TSMC 0.13μm technology using 5 metal layers. The chip has a total of 96 bondpads intended for packaging in a QFN-100 package.

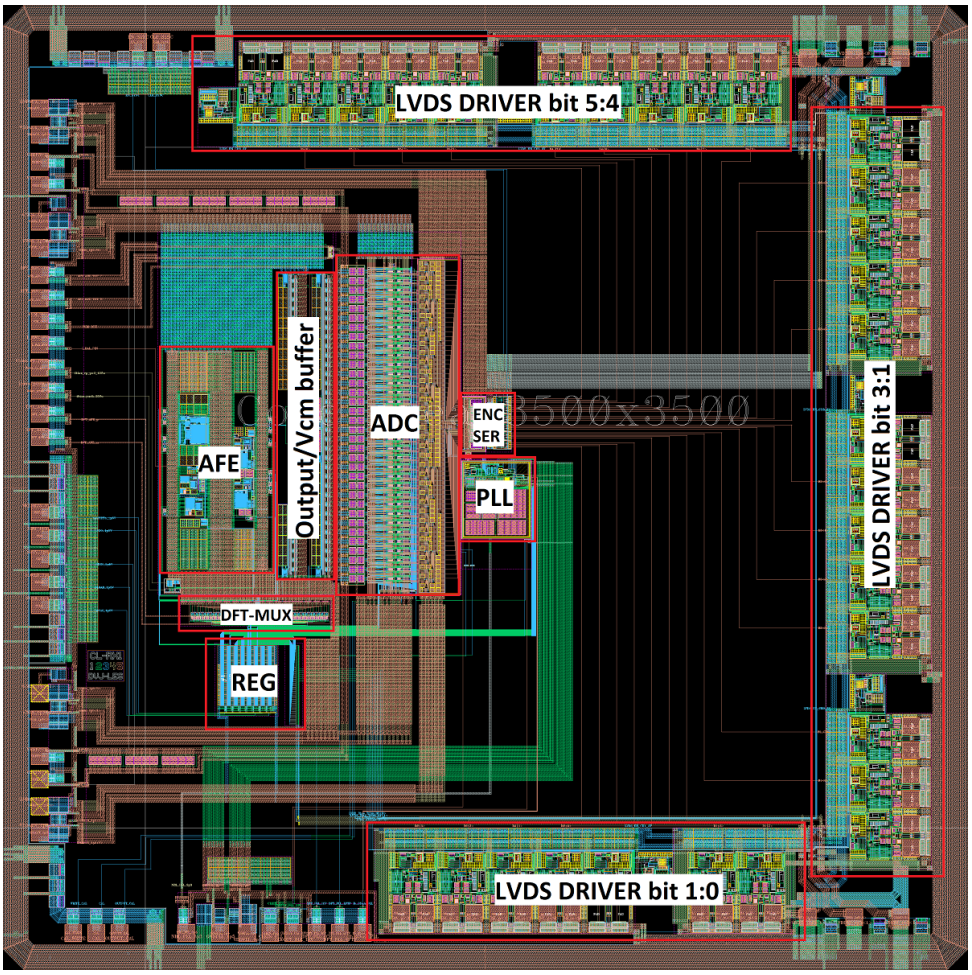


Figure 6.3: Chip top-level implementation

6.3 Status of completion

The complete chip is implemented and top-level simulation and its functionality is verified. Rough performance estimates are acquired as a sanity check by configuring the simulator in its fastest mode with reduced accuracy. The design is delivered as shown in figure 6.3. The last step is to place the sealring and run foundry-provided scripting to complete the tape-out process.

Chapter 7

Conclusion

7.1 Conclusion

In this work an analogue front-end for FMCW-LiDAR applications is presented. A top-down approach was taken starting from the optical system. Using the given LiDAR and optical parameters and models the full electro-optical signal chain was modelled with its non-idealities. Additionally a baseline digital signal processing and tone (object) detection algorithm was implemented because its limitations dictate the required spectral performance. Analysis of the system simulation results was used to determine the system's optical properties, and then to derive the requirements for the electrical front-end and ADC. Using these requirements the application specific circuitry was implemented. Extensive transistor level simulations were performed including simulations over process corners and the automotive temperature range ($-40°C - 125°C$). The circuits were implemented in TSMC 130nm CMOS technology. Post-layout simulations are preformed and the circuits are adjusted to maintain performance including all parasitics. Finally the AFE and ADC were consolidated with existing IP-blocks to form a full chip. Final functional verification and performance evaluations showed a fully functional design with the targeted performance. The project was delivered as a full design ready for tape-out.
The developed chip allows the LiDAR system to detect targets with reflectivities down to 5% at a distance of 200m whilst travelling at speeds up to 200km/h. This is achieved by transmitting an optical FMCW wave and downmixing the reflected wave, the beat frequency is detected using a balanced square-law detector. The balanced detector's picoampere-level outputs are amplified by $103dB\Omega$ while a bandwidth of $500MHz$ is maintained. The input-referred noise is maximally $13pA/\sqrt{Hz}$ and is matched to the noise of the detector. The noise is amplified without clipping because it causes significant generation of frequency spurs in the spectrum that can be identified as an object. The foremost linearity metric is the SFDR for which $46dB$ is reached. Using the 6-bit ADC, the SNDR of the detector is matched to that of the ADC, the SFDR is large enough such that any unwanted spurs are suppressed below the quantisation noise.

7.2 Future work

The design of the complete chip is done and ready for tape-out. To complete the project additional efforts to perform tape-out and packaging of the device are needed. The final project phase is test and measurement, this requires a custom-built test system.
The AFE is an analogue block and can be tested standalone but requires careful design of the power supply, a biasing current, the digital SPI-interface and the test signal generation hardware. The test signal can be provided by custom circuitry emulating the photodiode's behaviour. Conversely a full electro-optical LiDAR setup with appropriate photodiodes can be used. In the case that a full-chip characterisation needs to be performed including both the AFE and ADC a more

advanced FPGA-based test system will be needed to offer 6Gbps interfacing capabilities for the LVDS outputs.
The AFE design presented is proven to reach the specifications set forward. However in the following paragraphs, improvements for a second design iteration of the system are formulated.
A first improvement for the AFE is the addition of offset compensation circuitry compensate for the offset currents generated by the balanced photodiode detector. This eliminates the external AC-coupling capacitor. An approach to accomplish this is to build a compensation loop which measures the offset voltage at the output of the transimpedance stage and extracts or injects a current to the input node similar as shown in [50].
A second improvement regarding noise and power can be accomplished by replacing the TIA RCG-input stage by a capacitive feedback TIA. This topology accomplishes a similar shielding action as the RCG, but with the added benefit that it provides a gain greater than unity, while also offering very good noise performance. This in-turn relieves the gain requirement of the shunt-feedback stage.
A third possible improvement is lowering the offset of the output buffer. It would eliminate the need for the ADC-reference compensation loop. This can be accomplished by applying auto-zeroing techniques. However due to the amplifier's large bandwidth and to avoid the need for high frequency switching a continues time auto zeroing is recommended. This can be done by measuring the output, low-pass filtering it and injecting a current into the input to drive the output offset to zero. To reach a sufficiently low corner in the low-pass filter, a switched capacitor filter or external capacitor might need to be applied to avoid large on-chip capacitors.

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Appendix A

LiDAR Cross Section (LCS)

The LiDAR range equation as presented in equation 2.2 of chapter 2 contains the LCS parameter Γ. The LCS determines how the light of an object is reflected. It is defined as a fictional surface area in $[m^2]$ and represents the cross section of a reflecting sphere that would cause the equivalent amount of light power to be reflected towards the receiver as the real world target/object would, when illuminated by the same source [16]. The LCS is equivalent to the RADAR cross section (RCS) for RADAR applications [21]. The LCS or RCS are parameters that are difficult to determine. For simple objects these can be determined by solving a set of equations for simple objects like spheres and disks for example. However for more complex objects reaching an exact solution is difficult. In RADAR applications the RCS this is often measured [32].

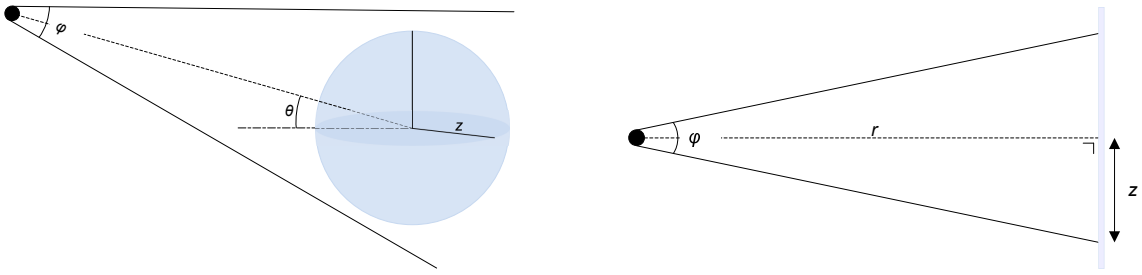


Figure A.1: (a) Lambertian scattering for a sphere, (b) Lambertian scattering simplified for object far away with a size larger than the beamwidth

The complexity of the LCS makes it difficult to model it mathematically. Therefore the following assumptions will be made. The object/target is assumed to have a Lambertian surface and thus exhibits Lambertian scattering properties (1). The object/target is larger than the beamwidth of the transmitted light (2). Lambert's cosine law is defined as $I_R = I_0 \rho_\pi cos(\theta)$ where I_R is the reflected irradiance under angle θ from the normal, I_0 the irradiance perpendicular to the object's surface. For a sphere which exhibits Lambertian reflection equation A.1 [16] describes the LCS, the equation applies to figure A.1a.

$$\Gamma = 4\pi\rho_\pi z^2 cos(\theta) \tag{A.1}$$

where:

ρ_π = Target reflection coefficient $[\%]$
z = Radius of the sphere $[m]$
θ = Angle of incidence of the light to the sphere for Lambertian reflection [radians]

Equation A.1 can be further simplified by applying some assumptions. Since the object/target is far away it can be assumed that the incident angle θ is small and therefore $cos(\theta) \approx 1$. Furthermore considering the object/target to be much larger than the LASER beam, the illuminated surface can be approximated by using the tangent and neglecting the curvature. Since a high quality LASER beam is assumed, the beamwidth (φ) is small and the tangent can thus be approximated by assuming it to be equal to the angle in radians. This is shown in equation A.2 [16].

$$\begin{aligned} \Gamma &= \rho_\pi 4\pi \left[tan\left(\frac{\varphi}{2}\right) r \right]^2 \qquad \text{with} \quad tan\left(\frac{\varphi}{2}\right) \approx \frac{\varphi}{2} \quad \text{for small angles} \\ \Gamma &= \rho_\pi \pi \varphi^2 r^2 \end{aligned} \tag{A.2}$$

where:

ρ_π = Target reflection coefficient $[\%]$
r = Distance between LiDAR and object/target $[m]$
φ = Transmitter beamwidth [radians]

Equation A.2 summarises the assumed LiDAR cross section under the assumption that light is indicent under a small angle and that the light beam has a small divergence angle compared to the distance to the target. Equation A.2 can now be substituted into the LiDAR range equation and will reveal its dependence on the target reflectivity.

Appendix B

Beam profile & Rayleigh range

The LiDAR range equation as described by equation 2.2 in chapter 2 contains a beam profile function K. The beam is transmitted into the optical system or into free space through a lens or aperture. This causes the collimated beam to assume a Gaussian [14] profile, Gaussian beam properties apply. The result is that a diverging beam is obtained [42] as a result of the lens used.

An important property of a Gaussian beam is the Rayleigh length or range (z_r), this a measure of distance along the beam's z-axis from the beam waist (w_0) (position where the beam spot size is minimal) to the position where the beam starts diverging significantly. At this position the radius has increased to $w_0\sqrt{2}$ and the cross sectional area has doubled [42]. To understand the significance of this parameter an analogy with RADAR systems can be made. LiDAR makes use of an aperture or lens to transmit the light into free space similar to how RADAR uses an antenna. Like RADAR, LiDAR also experiences the different field regions. The Rayleigh length denotes the division between the near-field and far-field regions. Equation B.1 indicates how the Rayleigh length (z_r) is defined for LiDAR.

$$z_r = \frac{\pi w_0^2}{\lambda} \tag{B.1}$$

In equation B.1 is z_r the Rayleigh length, λ the wavelength of the LASER and w_0 represents the radius of the beam at the beam waist. The profile of a Gaussian beam is shown in figure B.1, the Rayleigh lengths, half convergence angle and beam radii are indicated. One can now imagine a

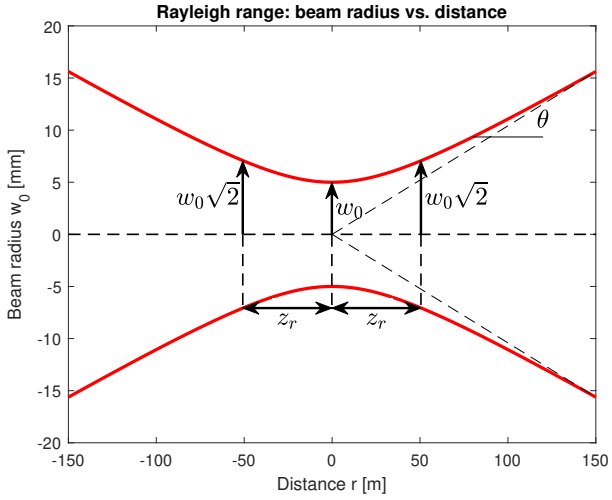


Figure B.1: example of a Gaussian beam profile ($w_0 = 5mm$, $\lambda = 1550nm$)

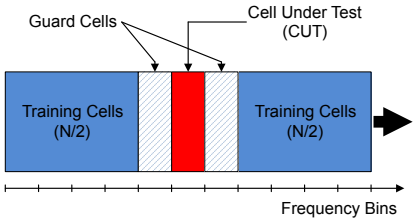
$$P(r) = P_0 \frac{1}{1 + \left[\frac{\pi w_0^2}{\lambda r}\right]^2}$$
$$K = \frac{P(r)}{P_0} = \frac{1}{1 + \left[\frac{\pi w_0^2}{\lambda r}\right]^2} \tag{B.2}$$

receiving aperture with a radius of w_0 illuminated by the beam. Placing the aperture at a distance $r < z_r$ will causes the aperture to capture 86.5% of the light power in the worst-case. When operating the LiDAR at short distances, below the Rayleigh range, the light to remains collimated and maintains a quasi-flat received power vs. distance characteristic. When the aperture is placed at distances $r > z_r$, the beam starts to diverge significantly and the received power drops proportional to $1/r^2$. The receiver is now located in the LiDAR's far-field. This phenomenon is described by equation B.2 and can be derived from Gaussian beam optics [42].

Appendix C

CA-CFAR detection algorithm

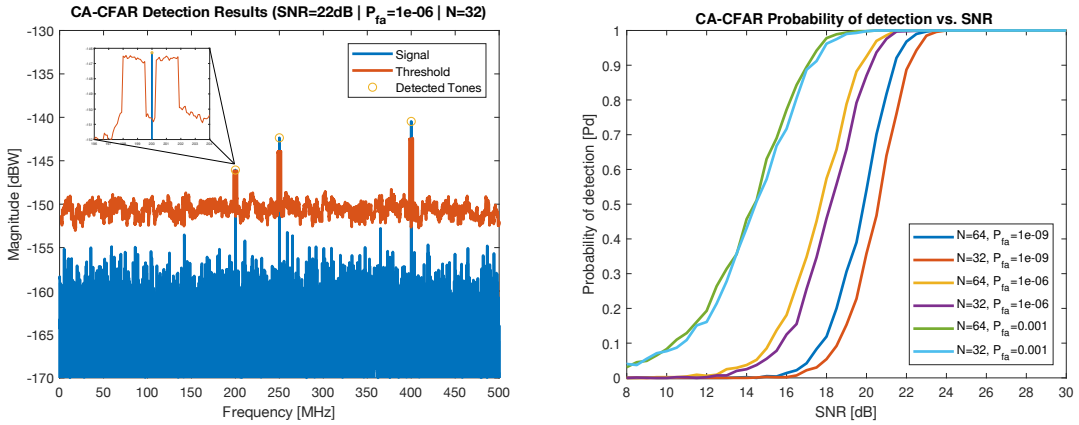
The tone detection algorithm is part of the downstream DSP processing. After the signals have been processed in the analogue domain and digitised, an FFT algorithm is used to get the spectrum. The properties of the tone detection algorithm will determine the minimum SNR threshold (SNR_{th}) required in order to maintain reliable detection.



$$
\begin{aligned}
T &= \alpha P_n \\
\alpha &= N\left(P_{pfa}^{-\frac{1}{N}} - 1\right) \\
P_n &= \frac{1}{N}\sum_{N}^{m=1} x_m
\end{aligned}
\tag{C.1}
$$

Figure C.1: CA-CFAR sliding window

The baseline algorithm selected is the CA-CFAR (Cell Averaging - Constant False Alarm Rate) [35][26]. The algorithm uses a sliding window approach, this window with training and guard cells centred around the CUT (Cell Under Test) slides over the frequency spectrum and the threshold for detection for the CUT is dynamically calculated. This is illustrated by figure C.1.



(a) **(b)**

Figure C.2: (a) Example of CA-CFAR: spectrum, threshold and tones, (b) Performance of the CA-CFAR across multiple P_{fa} values and window sizes N

In equation C.1 N is the number of training cells. For the training cells an average power level P_n is calculated, guard cells are discarded. The detection threshold (T) for the CUT is calculated and based on a threshold scaling factor α and the calculated average power level P_n. Factor α depends on the desired false alarm rate (P_{fa}) and the number of training cells N.

The simulations performed in figure C.2 are representative for the LiDAR application. A measurement time $T_{meas} = 10\mu S$ and an $10k$-point FFT were maintained to perform the measurements shown.
The performance of the algorithm is tested by measuring its probability of detection (P_d) versus SNR, shown in figure C.2b. A monte-carlo simulation was performed on the whole system the SNR of the input signal is swept. This was done for multiple window sizes and false-alarm rates. Figure C.2b shows that lower false alarm rates require to maintain a higher SNR. A bigger window size allows a lower SNR for the same detection probability. From plot C.2b it can be determined that to maintain a 1^{-3} false alarm rate a minimum SNR of $SNR_{min} = 15dB$ SNR is required [35][25][4] this number is assumed as the required threshold for detection (SNR_{th}).