# Silicon/silicon-germanium heterostructures for spin-qubit quantum processors

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# SILICON/SILICON-GERMANIUM HETEROSTRUCTURES FOR SPIN-QUBIT QUANTUM PROCESSORS

# SILICON/SILICON-GERMANIUM HETEROSTRUCTURES FOR SPIN-QUBIT QUANTUM PROCESSORS

## Proefschrift

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# CONTENTS

# SUMMARY

Spin qubits in silicon have emerged as a promising candidate for a scalable quantum computer due to their small footprint, long coherence times, and their compatibility with advanced semiconductor manufacturing. However, all known spin qubit material hosts come with specific challenges, that limit the performance of quantum information processing. In this thesis we study Si/SiGe heterostructures, comprising a strained silicon (Si) quantum well which is sandwiched between two silicon-germanium (SiGe) barriers. Si/SiGe heterostructures designed to act as solid-state matrix to host spin qubits have three intrinsic material challenges that limit performance: hyperfine interaction, valley splitting, and charge noise. Therefore, to realize a scalable quantum computer in Si/SiGe heterostructures we first quantify the performance limiting parameters and subsequently, we improve them systematically with statistical significance.

Acquiring data with statistical significance, however proves challenging for quantum devices in Si/SiGe heterostructures due to complicated and time-consuming fabrication schemes for device manufacturing, and the need of using dilution refrigerators that cool samples down to sub-Kelvin temperatures with only a limited amount of wires for electrical characterization of devices. Therefore, in this thesis we demonstrate fast growth-fabrication-measurement feedback cycles to accelerate our understanding on the materials and devices.

We realize such fast feedback cycles by first establishing a unique workflow at TU Delft, allowing 100 mm wafer growth and fabrication. Subsequently in our first experiment, we overcome the wiring bottleneck by presenting a cryogenic multiplexing platform that multiplies DC wires inside of a dilution refrigerator. This cryogenic multiplexer platform uses commercially available CMOS components, is compatible with any dilution refrigerator, and allows us to measure thirteen chips in the same cooldown at a temperature of 50 mK and at magnetic fields of up to 10 T. We confirm these extreme measurement conditions by showing statistically significant quantum transport properties of industrially grown 300 mm $^{nat}$Si/SiGe wafers.

In the following experimental chapters we then leverage the cryogenic multiplexer to successively tackle the performance limiting parameters of spin qubit processors in Si/SiGe heterostructures. In the second experiment we first analyze valley splitting in two dimensional electron gases and observe that valley splitting increases linearly with the electric field at the quantum Hall edge states of the device at a rate consistent with theoretical predictions. In turn, this observation allows us to evaluate valley splitting on a micron length scale with relatively simple Hall-bar measurements.

In the third experiment we show two major improvements in our heterostructures. First, we measure valley splitting in quantum dots with varying quantum well interface sharpness with statistical significance. We then proceed to analyze the atomic composition of the quantum well interfaces in several samples using atom probe tomography and show that Ge atoms are distributed randomly in each atomic layer. Subsequently

using the atom probe tomography results as input, we simulate valley splitting and show that valley splitting depends on the atomistic details of the interface and needs to be treated as a statistical distribution. We then propose a strategy to increase valley splitting on average above a chosen threshold by introducing a small concentration of Ge atoms into the quantum well. Second, all electrical measurements in this experiment are performed in isotopically purified $^{28}$Si quantum wells, which reduces the hyperfine interaction and hence increases qubit coherence times. While we do not explicitly discuss this improvement in this chapter, it is a crucial baseline for all following experiments in this thesis and for all qubit experiments using Delft grown $^{28}$Si/SiGe heterostructures.

We then move to show wafer-scale improvements of the disorder landscape of Si quantum wells in our fourth experiment. There, we challenge the common approach of growing an epitaxial Si cap on the $^{28}$Si/SiGe heterostructure, by replacing the Si cap with an amorphous Si-rich layer. We compare these two heterostructues by monitoring the statistical performance of mobility, percolation density, maximum electric field before hysteresis, and single particle relaxation time and observe a statistical performance increase of the mean value and the standard deviation.

In the fifth experiment we study a heterostructure with a thin quantum well and compare its statistical performance of mobility, percolation density, and charge noise with the performance of the heterostructures from the preceding experiment. Importantly, we find that misfit dislocation arising from strain relaxation are significantly reduced in thin quantum wells as confirmed by geometrical phase analysis of transmission-electron microscope images. In consequence, we observe a statistical performance increase of all key metrics in the novel heterostructure, only possible by our approach of engineering the critical material layers. Finally, we see promising simulated qubit coherence times and qubit error rates when using our charge noise results as simulation input, hinting at a practical advantage of our novel $^{28}$Si/SiGe heterostructures for quantum processors.

In the last experimental chapter we demonstrate how our improved $^{28}$Si/SiGe heterostructures have enabled two key experiments in the field of spin-based quantum computing. First, we show that our purified heterostrucures may host high-quality qubits, that in turn serve as a testbed for demonstrating CMOS-based cryogenic control of silicon quantum circuits. Second, we show how our isotopically purified, low-disorder heterostructures host a 6-qubit quantum processor with high-fidelity initialization, high-fidelity gate operation, and high-fidelity readout.

We conclude this thesis by highlighting key improvements of our $^{28}$Si/SiGe heterostructures that have contributed to state-of-the-art spin qubit experiments. However, our heterostructures still require further improvements if we want to achieve error rates around $10^{-6}$ and scale to large spin qubit arrays with more than a million qubits. Therefore, we discuss additional material changes that could further lower spin qubit error rates and we consider how to assess the uniformity of the material over different length scales, relevant when striving for larger qubit arrays.

# SAMENVATTING

Spin-qubits in silicium zijn naar voren gekomen als een veelbelovende kandidaat voor een schaalbare kwantumcomputer vanwege hun kleine voetafdruk, lange coherentietijd, en hun compatibiliteit met de geavanceerde halfgeleiderindustrie. Echter, alle bekende spin-qubit materiaalgastheren hebben hun eigen specifieke uitdagingen, die de prestaties van kwantuminformatieprocessors limiteren. In dit proefschrift onderzoeken we Si/SiGe heterostructuren, bestaande uit een opgespannen silicium (Si) kwantumput die is ingeklemd tussen twee silicium-germanium (SiGe) barrièrelagen. Si/SiGe heterostructuren, een vaste stof matrix ontworpen om te fungeren als gastheer voor spin-qubits, hebben drie intrinsieke materiële uitdagingen die prestaties beperken: de hyperfijninteractie, valleisplitsing, en ladingsruis. Daarom, om een schaalbare kwantumcomputer in Si/SiGe heterostructuren te realiseren, kwantificeren we eerst de prestatiebeperkende parameters om deze vervolgens met statistische significantie systematisch te verbeteren.

Het verkrijgen van data met statistische significantie blijkt echter een uitdaging voor kwantumapparaten in Si/SiGe heterostructuren vanwege gecompliceerde en tijdrovende fabricatieschema's voor de productie van kwantumapparaten en de noodzaak om verdunningskoelkasten te gebruiken die de apparaten afkoelen naar sub-Kelvin temperaturen met slechts een beperkt aantal draden beschikbaar voor de elektrische karakterisering van de apparaten. Daarom demonstreren we in dit proefschrift snelle groei-fabricage-meting feedbackcycli om ons begrip van de materialen en apparaten te versnellen.

We realiseren zulke snelle feedbackcycli door eerst een unieke workflow bij de TU Delft op te zetten waarbij de kweek en fabricatie op 100 mm wafers mogelijk wordt gemaakt. Vervolgens hebben we in ons eerste experiment het probleem van beperkte bedrading opgelost door een cryogeen multiplexerplatform te presenteren dat de DC-draden in een verdunningskoelkast vermenigvuldigt. Dit cryogene multiplexerplatform maakt gebruik van in de handel verkrijgbare CMOS-componenten, is compatibel met iedere verdunningskoelkast, en stelt ons in staat om tot dertien chips tegelijkertijd af te koelen en te meten bij een temperatuur van 50 mK en bij magnetische velden tot 10 T. We verifiëren deze extreme meetomstandigheden door statistisch significante kwantumtransporteigenschappen te laten zien van industrieel gekweekte 300 mm $^{nat}$Si/SiGe wafers.

In de volgende experimentele hoofdstukken maken we gebruik van de cryogene multiplexer om achtereenvolgens de prestatiebeperkende parameters van spin-qubit processors in Si/SiGe heterostructuren aan te pakken. In het tweede experiment analyseren we eerst valleisplitsing in tweedimensionale electrongassen en observeren we dat valleisplitsing lineair toeneemt met het elektrisch veld bij de kwantum-Hall randtoestanden van een apparaat op een manier dat overeenkomstig is met theoretische voorspellingen. Deze waarneming stelt ons op haar beurt in staat om valleisplitsing te evalueren op een micron-lengteschaal met relatief eenvoudige Hall-bar metingen.

In het derde experiment laten we twee belangrijke verbeteringen in onze heterostructuren zien. Eerst meten we met statistische significantie de valleisplitsing in kwantumdots, die verschillend van scherpte zijn in de overgangszones van de kwantumput. We gaan verder met het analyseren van de atomaire samenstelling van de kwantumput-overgangszones in verschillende apparaten door gebruik te maken van atoomsondetomografie en laten we zien dat Ge-atomen willekeurig verdeeld zijn in elke atoomlaag. Vervolgens, door de resultaten van de atoomsondetomografie als invoer te gebruiken, simuleren we valleisplitsing en tonen we aan dat valleisplitsing afhangt van de atomaire details van de overgangszone en derhalve behandeld moet worden als een statistische verdeling. Hierna stellen we een strategie voor om de valleisplitsing gemiddeld boven een gekozen drempel te verhogen door een kleine concentratie van Ge-atomen te introduceren in de kwantumput. Ten tweede zijn in dit experiment volledig elektrische metingen uitgevoerd in isotopisch gezuiverde $^{28}$Si kwantumputten, wat de hyperfijninteractie vermindert en daarmee de qubit-coherentietijden verhoogt. Hoewel we in dit hoofdstuk deze verbetering niet expliciet bespreken, is het een cruciale basis voor alle volgende experimenten in dit proefschrift en voor alle qubit-experimenten met de in Delft gekweekte $^{28}$Si/SiGe heterostructuren.

We gaan vervolgens over op het tonen van verbeteringen op de schaal van een wafer van het wanordelandschap van Si kwantumputten in ons vierde experiment. Hier dagen we de gebruikelijke aanpak van het kweken van een epitaxiale Si cap op de $^{28}$Si/SiGe heterostructuur uit door de Si cap te vervangen met een amorfe Si-rijke laag. We vergelijken deze twee heterostructuren door het monitoren van statistische prestaties van mobiliteit, percolatiedichtheid, maximaal elektrisch veld voor hysterese, en relaxatietijd van één deeltje en we observeren een statistische prestatiestijging in de gemiddelde waarde en de standaarddeviatie.

In het vijfde experiment bestuderen we een heterostructuur met een dunne kwantumput en vergelijken we zijn statistische prestaties van de mobiliteit, percolatiedichtheid, en ladingsruis met de prestaties van de heterostructuren uit het voorgaande experiment. Belangrijker wijze vinden we dat misfit-dislocaties als gevolg van spanningsrelaxatie significant verminderd zijn in dunne kwantumputten zoals bevestigd door geometrische faseanalyse van transmissie-elektronenscopie afbeeldingen. Als gevolg hiervan zien we een statistische prestatiestijging in alle sleutelparameters in de nieuwe heterostructuur, alleen mogelijk gemaakt door onze aanpak in het engineeren van de kritische materiaallagen. Ten slotte observeren we veelbelovende gesimuleerde qubitcoherentietijden en qubit-foutpercentages bij gebruik van onze ladingsruisresultaten als simulatieinvoer, een hint naar een praktisch voordeel van onze nieuwe $^{28}$Si/SiGe heterostructuren voor kwantumprocessors.

In het laatste experimentele hoofdstuk tonen we hoe onze verbeterde $^{28}$Si/SiGe heterostructuren twee belangrijke experimenten mogelijk hebben gemaakt op het gebied van spin-gebaseerde kwantumcomputing. Ten eerste laten we zien dat onze gezuiverde heterostructuren qubits van hoge kwaliteit kunnen herbergen, die op hun beurt dienen als een proefbank voor het demonstreren van op CMOS-gebaseerde cryogene controle van silicium kwantumcircuits. Ten tweede tonen we aan hoe onze isotopisch gezuiverde heterostructuren met een lage stoornis een platform vormt voor een 6-qubit kwantumprocessor die in de initialisatie, poortoperatie, en uitlezing een hoge betrouwbaarheid

heeft.

We sluiten dit proefschrift af met het benadrukken van de belangrijkste verbeteringen van onze $^{28}$Si/SiGe heterostructuren die hebben bijgedragen aan state-of-the-art spin-qubit experimenten. Onze heterostructuren vereisen echter nog verdere verbeteringen als we foutpercentages van $10^{-6}$ willen bereiken en willen opschalen naar grote spin-qubit roosters bestaande uit meer dan een miljoen qubits. Daarom bespreken we aanvullende materiële veranderingen die fouten in spin-qubits verder zouden kunnen verminderen en we overwegen hoe we de uniformiteit van het materiaal over verschillende lengteschalen, relevant bij het streven naar grote qubit roosters, kunnen beoordelen.

# 1

# INTRODUCTION

*I don't think we've even seen the tip of the iceberg. I think the potential of what the internet is going to do to society, both good and bad, is unimaginable.*

David Bowie

1

## 1.1. THE HUMAN DRIVE FOR INNOVATION

Ever since Homo Sapiens emerged on earth approximately 230.000 years ago [1], the evolutionary advantage was the ability to outperform predators and prey in mental tasks [2]. In the beginning these tasks were restricted to hiding, hunting, and gathering food, but with time, the mental exercises and the resulting ideas became more complex as humans started to bent and control fire, invent tools, domesticate wheat and animals, and develop concepts that would first allow us to organize ourselves in bigger groups, then in cities, and ultimately in countries, which up to nowadays are the prevalent form of government. With the increasing challenges of humanities' societal progress, the tools needed to support this progress, also grew in complexity. Starting with innovations such as the wheel, humans proceeded to invent plows, steam engines, or analog computing machines, which accompanied the progress over time. Nowadays, we have an almost unbelievably large toolset comprising, telecommunication, transport vehicles, and automated assembly lines among many others and many more are yet to be discovered.

One of the inventions that turned our societies upside-down is the transistor. A transistor is a semiconductor device used to switch electrical signals and represents the building block of any computer. In turn, the use of computers enabled growth in any possible aspect of human society, ranging from technological advances, such as personal computers or Moore's law, to societal advances containing the modeling of economics or climate change. In 1947 the ground-breaking demonstration of the transistor (awarded with the Nobel prize in physics in 1956 [3]) was performed by William Shockley, John Bardeen, and Walter Brattain, using germanium (Ge) as the host material. The succeeding journey of the transistor is history: in 1960 the first integrated circuit was developed, in 1971 the Intel 4004 became the first commercial single-chip microprocessor [4], in 1997 the IBM deep blue became better in chess than humans [5], and in 2022 the transistor is unarguably the most reproduced object in the history of humanity, manufactured over 20.000.000.000.000 times per second [6].

Modern day transistor manufacturing companies however, have predominantly used silicon (Si) over Ge as their material choice for decades, mainly because of the emergence of Si with a chemical purity of 99.9999999 % also called electronic-grade Si. Electronic-grade Si has several practical advantages over other material choices to host transistor technologies: First Si is the second most abundant element in the earth crust, second there are very effective ways to grow monocrystalline Si using the Czochralski process [7], third the purification of Si is relatively easy, and last the interface between Si and the thermal oxide is of higher quality compared to its Ge counterpart [8]. Because electronic-grade Si comprises all these requirements it has prevailed as the material choice for classical analog computing.

## 1.2. QUANTUM COMPUTING

While (Si) transistor technology continues to write its success story, another technology is arising on the horizon: quantum technology. The origin of quantum technology is intertwined with observations of odd behaviour of matter at small length scales in the early 20th century. However, it took humanity over a hundred years to develop tools on the basis of quantum physics, partly because we lacked the technology (e.g. nanofabrication,

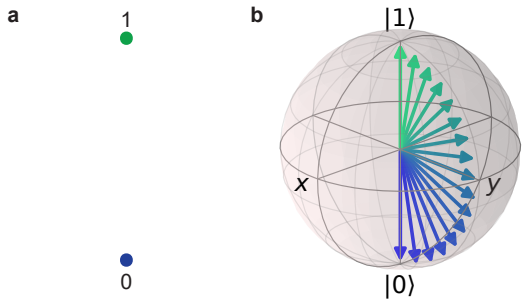


Figure 1.1: **a** classical bit containing a true (1) and false (0) statement. **b** Visualization of a Pauli-X-gate operation on a Bloch sphere. The arrows represent the state evolution going from $|1\rangle$ to $|0\rangle$.

cryogenic refrigerators with sub-Kelvin temerpatures, etc.) to controllably manipulate quantum effects. The promises that come along with this technology are immense and give rise to several fields. Quantum computing promises usage of the Shor and Grover algorithm for prime number factorization and efficient database search, respectively [9, 10], exponential calculation power with linearly growing system size [11], and the usage of quantum simulations to enhance drug research or material simulations [12]. Next, quantum communication promises secure information transmission [13]. Lastly, quantum metrology [14, 15] promises a new generation of ultra-sensitive sensors starting with for example the widely-known MRI-scans.

The original idea of using a quantum computing machine instead of a classical computer to simulate the world of quantum mechanics is often associated with the Feynman lectures, where he famously noted:" *Nature isn't classical, dammit, and if you want to make a simulation of nature, you'd better make it quantum mechanical, and by golly it's a wonderful problem, because it doesn't look so easy.* [16]."

Similar to the bits in classical computers, quantum computers rely on unit cells called the quantum bits or qubits. However, instead of holding information in the classical 0 or 1 state, qubits encode information as a combination of the 0 and 1 states, called superposition. This allows for the qubit to represent the ground state of the system as:

$$|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle \tag{1.1}$$

where $\alpha$ and $\beta$ are complex valued coefficients normalized to 1. Because $\alpha$ and $\beta$ are complex any representation of the two vectors $|0\rangle$ and $|1\rangle$ are mapped on the so-called Bloch sphere. This Bloch sphere is visualized in figure 1.1b and represents the center piece of quantum information science and any operation on a qubit will move its state around the surface of the Bloch sphere. For instance, we initialize a state into $|1\rangle$ where the state is pointing straight upwards. If we then apply a so called Pauli-X-gate, a rotation around the x-axis of 180°, we move the qubit into $|0\rangle$-state, which is analogous to the classical NOT-operation. Another crucial operation is the so-called Hadamard gate. Again, we initialize the qubit into the $|1\rangle$-state, then the Hadamard gate converts the $|1\rangle$-state into $\frac{|1\rangle+|0\rangle}{\sqrt{2}}$, which brings the qubit into an equal superposition state in the equatorial plane of the Bloch sphere. Both, the Pauli-X-gate and the Hadamard gate,

are applied onto a single qubit, the true power of quantum computing, however, reveals itself when we start using entanglement and two-qubit gates.

Entanglement means that global states of a composite system cannot be written as a product of the states of individual subsystems [17]. In practice this means, if we manipulate one particular quantum state within the group, we are effectively manipulating all quantum states within the group of entangled states. In a quantum computer we achieve entanglement for example by applying a Hadamard gate on two qubits. We initialize the system into a $|00\rangle$ ground state and apply the Hadamard gate $H$:

$$H|00\rangle = \frac{1}{\sqrt{2}}(|01\rangle + |00\rangle) \tag{1.2}$$

On the right side of the equation we see what is defined as the symmetric superposition state. This operation on two individual qubits manipulates the states into superposition.

Exploiting that we have a superposition state we now use two-qubit gates, which change the state of one qubit, the target qubit, depending on the state of another qubit, the control qubit. One example for a two-qubit gate is the CZ-gate, which applies a phase $\phi = \pi$ onto the target qubit, only if both the target and control qubit are in a $|1\rangle$-state. Such multi qubit operations can be expanded to n-qubit gates, where the manipulation of one target qubit depends on the state of many other control qubits. It is possible to decompose such manifold conditional qubit gates using a set of one- and two-qubit gates. A set of qubit gates that can reproduce any arbitrary multi-qubit gate is also called a set of universal quantum gates.

## 1.3. REQUIREMENTS FOR A QUANTUM COMPUTER

The demonstration of quantum supremacy —the proof that a programmable quantum computer is able to solve a problem faster than the most powerful classical computer —has leveraged the field of quantum computation [18, 19]. However, qubits still experience errors from their environment or from imperfect implementations of quantum gates and therefore the implementation of fault tolerant quantum computers —quantum computers where the encoded quantum information are protected from these errors [20] —remains a challenge. In 2000 David DiVincenzo formulated 5 criteria that any quantum computing architecture needs to fulfill [21]:

1. A scalable physical system with well characterized qubits
2. The ability to initialize well-defined qubit states
3. A high decoherence time vs. gate operation time ratio
4. A universal set of quantum gates
5. High fidelity qubit readout

Physicists have been experimenting with several available platforms to fulfill these requirements and realize a quantum computer, containing qubits based on superconductors [22, 18, 23], ion traps [24, 25, 26], NMR [27, 28, 29], topologically protected states

[30, 31, 32], NV centers in diamonds [33, 34, 35], neutral atoms [36, 37], photons [19, 38, 39], and spins [40, 41, 42, 43], each of them with their own advantages, disadvantages, and material challenges.

Spin qubits in particular use the spin degree of freedom of electrons or holes to encode information [44, 45, 46, 43] and represent a promising quantum computing platform because they hold the promise to meet the DiVincenzo criteria, have small footprints of ≤100 nm, and since they use semiconducting materials for their realization, they can in principle leverage CMOS-technology for scaling. However, there are caveats: Ultimately qubit initialization, decoherence, and readout fidelity are limited through enhanced relaxation, charge defect motion, ill-defined ground states or magnetic noise arising from the interaction with nuclear spins in the solid state matrix. In addition, the scalability of the system will demand a small device-to-device variability [47, 48], which implies uniform material properties such as sharp material interfaces, low and uniform defect densities, and isotopic enrichment on a wafer-scale. As a consequence, the underlying material used for spin qubit quantum computation needs to meet all these requirements and fulfill, in analogy to the classical electronic-grade counterpart, the quantum-grade condition.

## 1.4. DEVELOPMENT CYCLE OF SEMICONDUCTOR MATERIALS FOR QUANTUM PROCESSORS

One of the most promising platforms to realize spin qubits are Si/SiGe heterostructures, thin layers of semiconductor Si stretched and sandwiched between layers of SiGe. To implement spin qubits in Si/SiGe heterostructures we use gate-defined quantum dots to isolate and control the spin of a single electron (we will take a deeper look in section 2.3.2). This qubit encoding is known as the Loss-and-DiVincenzo-qubit [41]. In figure 1.2**a** and 1.2**b** we see a schematic side and top view of a gate defined quantum dot in Si/SiGe heterostructures. Ideally, the gates shape the electrical landscape such that spin qubits form in the Si quantum well (see figure 1.2**b**). However, spin qubits in such a system will either decohere or experience ambiguous initialization and readout because of noise sources such as ill-defined ground states, noise through material impurities causing electrical charges moving in the solid-state matrix, or noise through the spontaneous relaxation of the magnetic momentum in the nucleus of the atoms nearby the qubit.

In figure 1.2**c** we see a schematic of a Si/SiGe heterostructure emphasizing the most common realizations of noise sources comprising: ill-defined ground states, magnetic impurities, crystalline defects, diffused interfaces, background impurities and charged impurities, where the last four contribute to a deviation from a perfect crystal, called disorder. It is crucial to quantify which of these noise sources is limiting the performance of a quantum processor and subsequently we need to address these material issues in a systematic manner. For example Si in nature occurs in 3 isotopes: $^{28}$Si, $^{29}$Si, and $^{30}$Si. Therefore when we use natural silicon ($^{nat}$Si) to grow our materials these three isotopes are present in the quantum well. In this case the $^{29}$Si isotope is problematic for spin qubit coherence because it has a non-zero nuclear spin and therefore contributes to the magnetic noise in the system (see also figure 1.2**c**) [49]. A solution is to grow quantum wells exclusively with zero nuclear spins for example through isotopical enrichment of

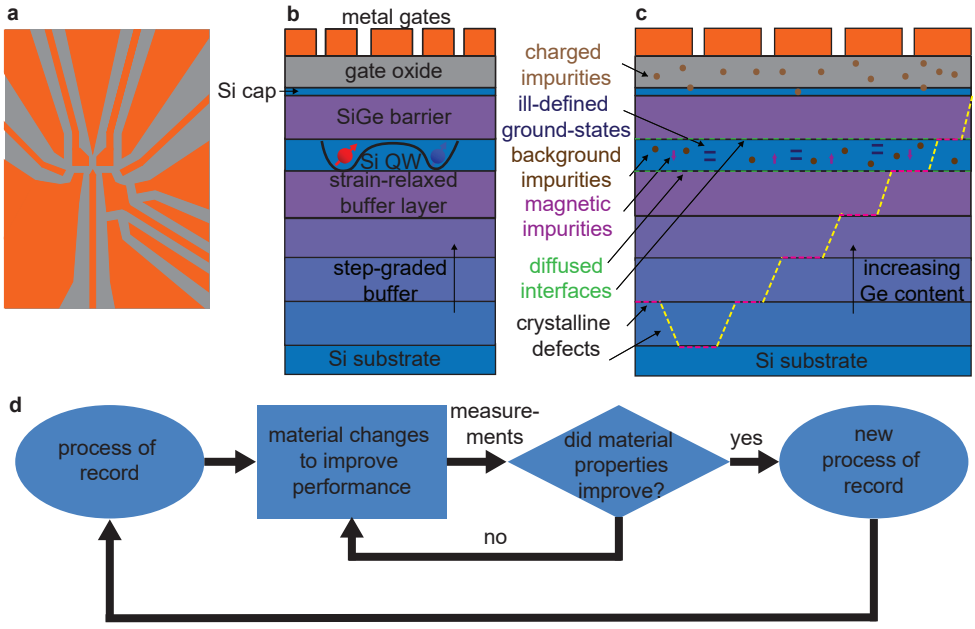


Figure 1.2: **a** Top view schematic of gate defined quantum dots. **b** Side view schematic of a Si/SiGe heterostructure with gate defined quantum dots. In the Si quantum well we see two schematic spin qubits trapped in an electrostatical potential. **c** Side view schematic of a Si/SiGe heterostructure with gate defined quantum dots and performance limiting noise sources: crystaline defects (pink and yellow dashed lines), diffused interfaces (green dashed line), magnetic impurities (purple arrows), background impurities (dark brown circles), ill-defined ground states (short blue parallel lines), and charged impurities (light brown circles). **d** Flow chart of a material feedback cycle.

the $^{28}$Si-isotope.

In order to validate the performance of the materials upon process variations we need to implement feedback cycles. A typical material feedback cycle is illustrated in figure 1.2**d**. Starting from the process of record —the currently known recipe for yielding our best performing material —we design changes in the material, implement these variations by growing splits of semiconductor heterostructures, and fabricate appropriate devices to test a suite of electrical properties. Then we measure the material performance at cryogenic temperatures and with statistical significance, and decide whether the material performance improved. The response determines what is the next step: If the answer is no, we go back to device and material changes, and if the answer is yes, we have a new process of record. The new process of record then becomes the new baseline for all following experiments. It is important that these feedback cycles are fast and accurate, since a short response time ultimately accelerates the development of quantum processors. Therefore, we have to define metrics that indicate performance improvements for spin qubit processors, and we want to use measurements that require a reasonable amount of time for their execution to repeat them on many devices and gain statistical relevance.

For example, we use Hall-bar devices to probe the electrical performance of a Si/SiGe heterostructure. Hall-bar devices are transistors with additional voltage probes, which allow us to quantify the charge carrier mobility $\mu$ and the percolation density $n_p$. $\mu$ measures how fast charge carriers move in a semiconductor when subject to an electric field and therefore informs us about charge scattering from disorder in the system, and $n_p$ measures the minumum charge density to form a conductive channel. Both, $\mu$ and $n_p$ help us to understand and quantify the dominating disorder sources in the system.

## 1.5. SI/SIGE HETEROSTRUCTURES FOR SPIN-QUBIT QUANTUM PROCESSORS

In this thesis we show how we advance Si/SiGe heterostructures for spin qubits by implementing fast material feedback cycles. The following chapters guide the reader through the progress over the last years and demonstrate the improvements of the underlying material platform, ultimately leading to high performing quantum processors.

**Chapter 2** provides the theoretical framework relevant to the work in this thesis. We discuss the electronic band structure of bulk Si, study the effects of strain and confinement on the band structure properties, and look at the performance limiting mechanisms of spin qubits in Si. We focus on valley splitting, electrical noise, and magnetic noise. We then examine a suite of devices that allow us to quantify the performance of Si/SiGe heterostructures as a host material for spin-qubit processors.

**Chapter 3** discusses the experimental methods. We study the growth of 100 mm wafers, material characterization techniques, the fabrication processes of micro- and nano-devices, dilution refrigerators, and the instrumentation, enabling wafer-scale analysis of the material and devices.

The results section successively shows the reproducible material improvements, transitioning from experiments in $^{nat}$Si/SiGe heterostructures provided from Intel within the Intel-QuTech partnership, to isotopically enriched $^{28}$Si/SiGe heterostructures developed by the Scappucci group in Delft.

In **Chapter 4** we demonstrate a cryogenic multiplexer platform that overcomes the input/output (I/O) interconnect bottleneck present in cryostats operating at sub-kelvin temperatures. We statistically measure key metrics of Si/SiGe Hall-bar heterostructure field effect transistors, accelerating the feedback loop of industrially grown $^{nat}$Si/SiGe 300 mm wafers.

In **Chapter 5** we use high quality industrial $^{nat}$Si/SiGe heterostructures to perform valley splitting measurements in low-disorder silicon quantum wells in the quantum Hall regime. We observe, that valley splitting increases with electric field at the edge of the device at a rate consistent with theoretical predictions.

In **Chapter 6** we exploit the cryo-multiplexing platform and show statistical measurements of valley splitting in quantum dots with varying quantum well interface sharpness in $^{28}$Si/SiGe heterostructures. We determine the atomic composition of the quantum well interfaces with atom probe tomography and show that Ge atoms are distributed randomly in each atomic layer. Subsequently, we simulate valley splitting and show that valley splitting needs to be treated as a statistical distribution. We propose a strategy to increase valley splitting on average above a chosen threshold by introducing a small

concentration of Ge atoms into the quantum well.

The study of the electrical environment of the $^{28}$Si/SiGe heterostructures comprises two chapters. In **Chapter 7** we challenge the mainstream approach to deposit an epitaxial Si cap on 28Si/SiGe heterostructures and, instead, we terminate the SiGe barrier with an amorphous Si-rich layer. We observe a statistical performance increase of mean value and spread of mobility, percolation density, maximum electric field before hysteresis, and single particle relaxation time. These results form the basis for the wafer scale analysis of charge noise measurements in **Chapter 8**. We show wafer-scale low charge noise achieved through targeted engineering of the critical material layers responsible for charge noise.

**Chapter 9** shows how our $^{28}$Si/SiGe heterostructure have enabled two key experiments in the field of quantum computing [50, 51]. First, we show that our purified heterostrucures may host high-quality qubits, that serve as a testbed for demonstrating CMOS-based cryogenic control of silicon quantum circuits. Second, we show how our isotopically purified, low-disorder heterostructures host a 6-qubit quantum processor with high-fidelity initialization, high-fidelity gate operation, and high-fidelity readout.

In **Chapter 10** we conclude this thesis by discussing key results, speculating on future material developments, and considering uniformity on the relevant disorder length scales to improve quantum processors in Si.

# 2

# THEORY

*The interface is the device.*

Horst Störmer

## 2.1. SI/SIGE HETEROSTRUCTURES

Two layers of different semiconductors adjadcent to each other are called a heterojunction. In turn, two or more heterojunctions together form a heterostructure. Heterostructures have been a vivid research topic for decades and the pioneering work of Zhores Alferov and Herbert Kroemer was awarded the Nobel prize in 2000 [52]. Heterostructures form quantum wells in the conduction and valence band, which allows the confinement of electrons or holes, respectively. In particular, heterostructures comprising the group-IV semiconductors Si and Ge are of great scientific and technological interest because they can host spin qubits, which in turn could be the building block of a fault tolerant quantum computer [41].

### 2.1.1. BAND STRUCTURE OF SILICON

Silicon and germanium as well as their compounds crystallize in the zincblende structure. zincblende structures follow a face-centered-cubic (FCC) Bravais lattice with a two-atom basis, so that we describe them as two interpenetrating FCC lattices (figure 2.1**a**). The primitve cell of an FCC lattice is described using the three translational vectors:

$$v_1 = \frac{a}{2}(0,1,1),\ v_2 = \frac{a}{2}(1,0,1),\ v_3 = \frac{a}{2}(1,1,0) \tag{2.1}$$

where $a$ is the lattice parameter of the unit cell. In the Zincblende structure the two atoms in the primitive cell are placed at the origin $d_1 = (0,0,0)$, and at one fourth of the diagonal of the cube: $d_2 = \frac{a}{4}(1,1,1)$.

Using the translation, $g_k = \frac{2\pi}{V} v_i \times v_j$, where V is the Volume of the unit cell, $g_k$ is the vector in the reciprocal lattice, $v_i$ and $v_j$ are the primitive vectors of the FCC lattice, and the indices k,i, and j permutate between the values 1,2,3, we map out the real space FCC vectors onto its corresponding reciprocal space vectors:

$$g_1 = \frac{2\pi}{a} a(-1,1,1),\ g_2 = \frac{2\pi}{a}(1,-1,1),\ g_3 = \frac{2\pi}{a}(1,1,-1), \tag{2.2}$$

which form a BCC lattice. In a crystal there is an infinite amount of these reciprocal unit cells next to each other and we can define a volume around each atom, which is closest to only one atom in the reciprocal lattice compared to any other atoms in the reciprocal lattice. This volume is called the Brillouin zone, which for an FCC lattice is a truncated octahedron. In figure 2.1**b** we show such an Octahedron alongside some high symmetry points that are found in a BCC lattice.

The Brillouin zone is the center piece of any analysis of electronic band structures in solid states. Using theoretical tools such as the tight binding model, we can understand the energy dispersion of an electron within the Brillouin zone[1]. These energy dispersions are usually illustrated following a path going from one high symmetry point to the next one. In figure 2.1**c** we see the band structure diagram of silicon starting from center point of the hexagonal face in (1,1,1)-direction L, to the center point of the Brillouin

[1] To understand how to get from the Brillouin zone to eletronic band structures the interested reader is referred to Ref. [53]

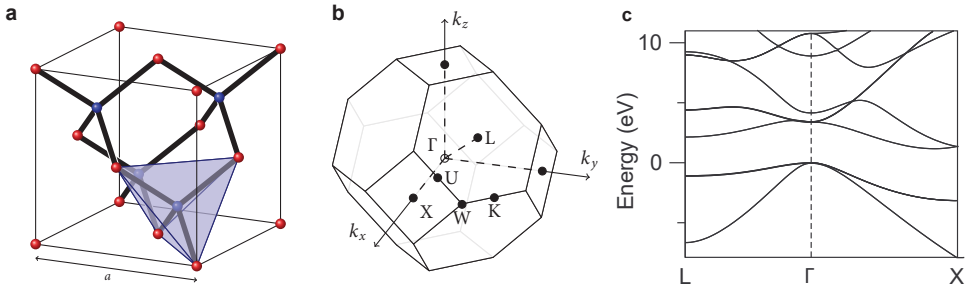


Figure 2.1: a) unit cell of the zincblende structure including nearest-neighbor bonds. Both, the blue and the red atoms form FCC lattices, displaced by one fourth of the diagonal of the unit cells. The blue tetrahedron highlights, that each atom in zincblende structure has the opposite atom as its four nearest neighbors. If both atoms are the same we get the diamond structure. b) Brillouin zone of an FCC lattice, as found in silicon. Some high symmetry points at the center, at edges, and on the faces are highlighted. c) Band structure diagram of silicon following the path L-Γ-X. We see the top most conduction band in the Γ-point, and the bottom-most conduction band at the Δ-point equal to 0.82 of the distance betweeen Γ and X. All panels adapted and modified from Ref [55]

zone Γ, and finally to the center of the quadratic face along the (1,0,0)-direction, the X-point. We find the maximum of the valence band at the Γ-point and the minimum of the conduction band at 82 % of the distance to the X-point, also called the Δ-point. Since there are six different X-points, we also get a six-fold degeneracy of the conduction band minimum at the six different Δ-points. Therefore, on top of the spin degree of freedom that we want to exploit in Si/SiGe heterostructures to build a quantum computer, the conduction band minimum, the valley, adds another degree freedom which can cause decoherence of spin qubits [54].

### 2.1.2. STRAINED SI QUANTUM WELLS

This valley degeneracy poses a serious limitation to Si/SiGe as material choice for spin based quantum computation. But what if the symmetry of the Brillouin zone could be broken and subsequently the valleys at the Δ-points would move? We achieve this by applying strain. In figure 2.2**a** we first illustrate materials free of strain, also called relaxed materials, with their respective lattice constants $a_1$, $a_2$, $b_1$, and $b_2$. In the upper panel of figure 2.2**a** we then see the effect of two materials with lattice constant $a_1$ and $a_2$ merging. Since $a_2 > a-1$ the upper layer is under tensile strain, which increases the lattice constant in x- and y-direction and reduces the lattice constant in z-direction. In consequence, tensile strain moves the in-plane valleys in $k_x$- and $k_y$-direction, the $\Delta_4$-valleys further away, and the out-of-plane in $k_z$-direction closer to the center of the Brillouin zone, leaving two degenerate $k_z$-valleys, the $\Delta_2$-valleys, energetically more favorable. In contrast, compressive strain changes the lattice constants vice versa and consequently would move the valleys in the opposite directions, with the difference, that there would be four energy degenerate valleys in $k_x$ and $k_y$ direction available.

Tensile strain is realized by a heterostructure where Si is sandwiched between two semiconductors with a larger lattice constant compared to Si. The lattice parameters $a$ of Si and Ge are $a_{Si}$ = 0.5431 nm and $a_{Ge}$ = 0.5658 nm, respectively. In addition, Si

and Ge are fully miscible so any alloy comprising the two elements can be used for heterostructures. In particular, we use the following formula for the relaxed lattice constant $a_x$ of any $Si_{1-x}Ge_x$ alloy [56, 57]:

$$a_x = a_{Si} + 0.200326x(1-x) + [a_{Ge} - a_{Si}]x \tag{2.3}$$

where the factor 0.200326x is a correction factor, introduced to match the experimental deviation from Vegard's law in $Si_{1-x}Ge_x$ alloys (see Ref. [56, 58] for a more rigorous discussion). When designing the strain of $Si_{1-x}Ge_x$ alloys, it is crucial that the crystalline integrity of the heterostructure stays intact. But if the top layer starts relaxing and therefore its lattice constant in $x$- and $y$-direction does not adjust to the bottom layer, misfit dislocations form at the interface between the top and bottom layer (see figure 2.2**b**) [59]. These dislocations strongly influence the electrical quality of the Si quantum well because they act as efficient recombination-generation sites for charge carriers [60, 61].

Defects form during the growth of the virtual substrate which comprises a step-graded-

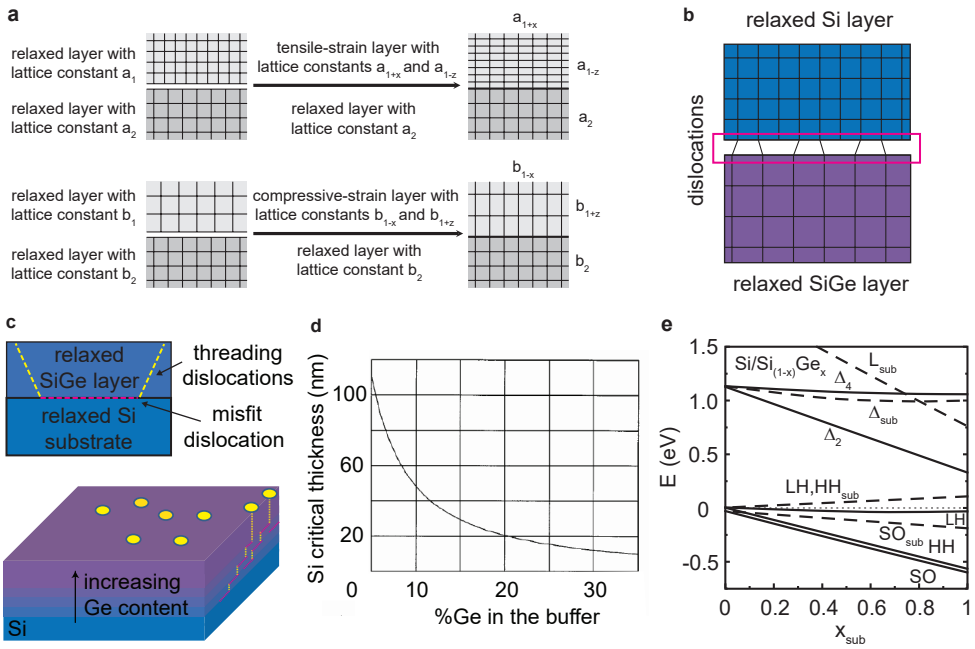


Figure 2.2: **a** Difference between compressive and tensile strain. In the tensile case we have two relaxed lattices with lattice constants $a_1$ and $a_2$ where $a_1 < a_2$. Consequently, the in-plane lattice constant of the upper layer adapts to the lattice constant of the lower layer. In consequence, the lattice constant in z-direction decreases. For compressive strain this process works vice versa. Adapted from Ref. [55]. **b** Formation of dislocations when a relaxed Si top layer is grown on top of a relaxed SiGe substrate. **c** Schematic image of the directions of misfit and threading dislocations in Si/SiGe heterostructures. **d** Critical thickness of a strained silicon layer as a function of the germanium concentration of a fully relaxed virtual substrate. **b**-**d** adapted from Ref. [62]. **e** Variation of the relevant conduction and valence band edges of a $Si/Si_{1-x}Ge_x$ heterostructure as a function of the substrate composition $x$. Adapted from Ref. [8].

buffer with several SiGe layers of different Ge concentration, and a strain-relaxed buffer layer with the final Ge concentration. For example in the top panel of figure 2.2**c** we see a schematic illustration of a relaxed SiGe layer on top of a relaxed Si substrate. Because the SiGe layer is relaxed, a misfit dislocation forms (pink dashed line) at the Si/SiGe interface and at each end of the misfit dislocation a threading dislocation (yellow dashed line) propagates at a 60° angle through the SiGe layer. In the bottom panel of figure 2.2**c** we see how misfit and threading dislocations propagate through the step-graded SiGe layers. At each interface misfit dislocations go along the interface and threading dislocations move through the adjacent layers. Additionally, new misfit dislocations form at each interface. However, when dislocations reach the edge of material there is no further propagation in z-direction, which makes the growth of virtual substrates with several μm thickness beneficial in the context of defect elimination.

To avoid the formation of additional misfit and threading dislocations in the Si quantum well, we have to prevent strain-relaxation in the quantum well layer. We prevent strain-relaxation when the quantum well thickness is below the critical thickness $t_c$, with $t_c$ being the thickness where the elastic energy stored in the crystal for an additional layer is higher than the energy required for the formation of defects [59]. In figure. 2.2**d** we see $t_c$ of a Si layer as a function of the Ge concentration in the $Si_{1-x}Ge_x$-matrix. In this graph we distinguish two different regions. First, the unstable region above the curve shows the parameters where the Si layer starts to relax, which effectively reduces the splitting of the $\Delta_2$ and $\Delta_4$ valleys and compromises the crystalline quality through the formation of dislocations [59]. Second, the stable region below the curve shows the parameters where the strain in the thin silicon layer does not relax. Ultimately, it is desirable to grow quantum wells thinner than the critical thickness because the critical thickness is a statistical value that locally varies depending on the nucleation sites in the underlying substrate [61].

The resulting energy evolution of the most important valence and conduction bands in Si/SiGe heterostructures are shown in figure 2.2**e** [8]. Here, the solid curves represent the energy of bands in the Si quantum well and dashed lines the bands in the $Si_{1-x}Ge_x$-matrix. As expected the $\Delta_2$ and $\Delta_4$ valleys are degenerate at $x = 0$ and split further as x is increased. Since the splitting is in the order of tens to hundreds of meV, much larger than any other relevant energy for quantum computation, we have achieved a two-fold degeneracy. Interestingly, the light and heavy-hole bands in the substrate are energetically favorable over the entire substrate composition, therefore it is only possible to accumulate electrons in the Si layer.

## 2.2. MATERIAL CHALLENGES RELEVANT FOR SPIN QUBITS

To improve the performance of quantum processors, the decoherence sources in the qubit host environment need to be removed (at best) or, more pragmatically, mitigated. Magnetic noise [63], electrical noise [64, 65] and valley splitting [66, 54] are, among others, three main factors in Si/SiGe heterostructures that limit spin qubit coherence times, and hence performance. By material engineering, these factors may be addressed in turns, starting from the one that has the most dominant effect. For example, if spin qubit coherence is mainly limited by magnetic noise, the focus should be on isotopic purification of the Si quantum well before improving charge noise by developing a bet-

ter semiconductor-oxide interface. Every time we improve on one limiting factor, the material will support qubits with an increased baseline for coherence time until a new limiting mechanism has become relevant. This way of working leads to a never-ending material-fabrication-measurement feedback cycle, where new, creative ideas are necessary to provide everlasting qubit performance improvements.



### 2.2.1. VALLEY SPLITTING

In section 2.1.2 we have analyzed how to split the 6-fold degeneracy into $\Delta_4$ and $\Delta_2$ valleys. To realize a spin-based quantum computer in Si, however, we need to remove the energy degeneracy of the $\Delta_2$-valleys and achieve a large energy splitting (see figure 2.3**a**). The energy splitting of the $\Delta_2$-valleys, also called valley splitting, naturally occurs as a result of the broken symmetry at the interfaces of the thin Si layer and the SiGe matrix.

A first understanding of valley splitting is provided by effective mass theory (EM). EM approximates the solutions of the dispersion relation of the conduction band minima using the effective mass. In strained silicon we write the electron wavefunction $\Psi(\vec{r})$ as:

$$\Psi(\vec{r}) = \sum_{j=\pm z} \alpha_j e^{ik_j z} u_{\vec{k_j}}(\vec{r}) F_j(\vec{r}) \tag{2.4}$$

where $\alpha_j$ is the relative phase between the valleys in $k_z$ direction (analogous to the $\Delta_2$ valleys) with a normalization of $|\alpha_j| = 1/\sqrt{2}$, $e^{ik_j z} u_{\vec{k_j}}$ is a Bloch wave describing fast atomic scale oscillations, and $F_j(\vec{r})$ is an envelope functions for the two valleys. From this equation we see that EM captures both atomic scale and several nanometer scale behaviour with the Bloch waves and envelope functions, respectively. EM however, is valid only in a slowly varying confinement potential, which imprecise problematic at the abrupt and sharp potential barriers at the Si/SiGe interfaces. To circumvent this limitation we introduce a valley coupling potential [67]:

$$V_v = v_v \delta(z - z_i) \tag{2.5}$$

where $v_v$ is the valley coupling parameter and $\delta(z-z_i)$ is the vertical position coordinate of the Si/SiGe heterostructure interface. The parameter $v_v$ allows the computationally light EM-formalism to simulate valley splitting values while considering non-trivial Si/SiGe heterostucture interfaces. Unfortunately, EM does not provide a solution for $v_v$ (with the recent exception of Ref [68]) and therefore we need experiments or tightbinding methods to quantify $v_v$.

The tight-binding method to formalize valley splitting assumes a chain of identical atoms with neareast neighbour and next-nearest neighbor interactions (see figure 2.3**b**) [69]. The atoms are characterized by an onsite energy $\epsilon$, nearest neighbor hopping coefficient $t_1$ and next-nearest neighbor hopping coefficient $t_2$. We write the wavevector for such a chain as:

$$|\Psi\rangle = \sum_z \phi_n |n\rangle \tag{2.6}$$

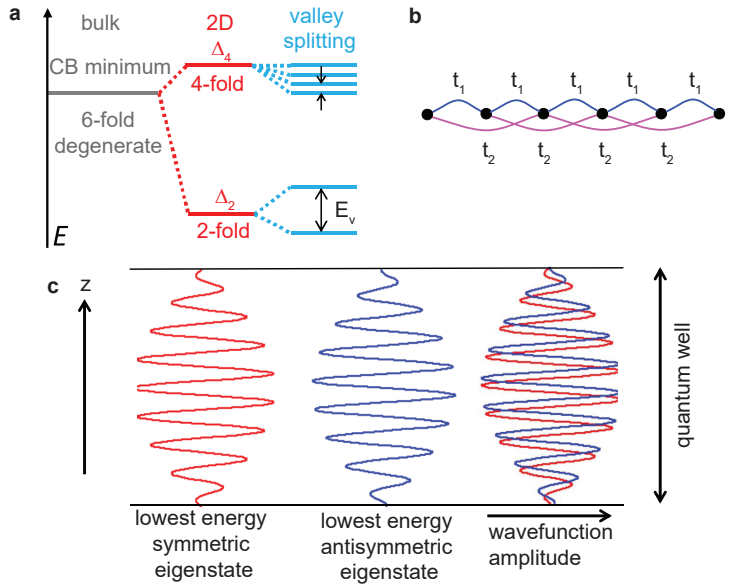


Figure 2.3: **a** Valley splitting in Si/SiGe heterostructure. The sixfold valley degeneracy of bulk silicon is broken by the large in-plane tensile strain in the quantum well so that the $\Delta_4$ and $\Delta_2$-valleys split and the energetic separation of the $\Delta_2$ split bands is called valley splitting ($E_v$). **b** Representation of a one-dimensional chain of atoms with nearest neighbor interaction $t_1$ and next-nearest neighbor interaction $t_2$. **c** Illustration of the two lowest-lying energy eigenstates in an infinite square well [42]. Both eigenstates have similar envelope wave function for the symmetric and antisymmetric state. The valley degeneracy causes the fast oscillations with a phase shift, depending on the details of the quantum well interface. This sensitive dependance on the quantum well interface disorder causes large valley splitting fluctutations across wafers and devices. All panels adapted and modified from [42].

where $\phi_n$ is the state of the n-th atom in a chain of atoms of length $2N+1$, and $|n\rangle$ is the orthogonal basis. Subsequently, we use a Hamiltonian that incorporates nearest and next-nearest neighbor interactions of form:

$$H|\Psi\rangle = \sum_n \phi_n(\epsilon|n\rangle + t_1|n-1\rangle + t_1|n+1\rangle + t_2|n-2\rangle + t_2|n+2\rangle) \tag{2.7}$$

where we extract the eigenenergies of the system with $\langle\Psi|H|\Psi\rangle$:

$$\epsilon\phi_n + t_1(\phi_{n+1} + \phi_{n-1}) + t_2(\phi_{n+2} + \phi_{n-2}) = E\phi_n \tag{2.8}$$

Using the Ansatz $\phi_n = \phi_0 e^{ikna}$ with $k$ as the spatial index ($k = p\frac{2\pi}{L}$ and $p \in \mathbb{Z}$ ) and $a$ as the lattice constant, and periodic boundary conditions we write the dispersion relation $E(k)$:

$$E(k) = \epsilon + 2t_1\cos(ka) + 2t_2\cos(2ka) \tag{2.9}$$

This model assumes a chain of one atom per unit cell, however, silicon though contains two atoms in the unit cell and therefore it necessary to adapt the model to a lattice with a two-atom-basis [69]. Using a modified wavevector $|\Psi\rangle = \sum_n (\phi_n |n,1\rangle + \psi_n |n,2\rangle$ and then applying the Hamiltonian from equation 2.7 we get:

$$\begin{aligned} H|\Psi\rangle = \sum_n & (\epsilon\phi_n |n,1\rangle + \epsilon\psi |n,1\rangle \\ & + t_1\psi_n |n,1\rangle + t_1\psi_{n-1} |n,1\rangle + t_2\phi_{n+1} |n,1\rangle + t_2\phi_{n-1} |n,1\rangle \\ & + t_1\phi_n |n,2\rangle + t_1\phi_{n+1} |n,2\rangle + t_2\psi_{n+1} |n,2\rangle + t_2\psi_{n-1} |n,2\rangle \end{aligned} \tag{2.10}$$

and the subsequent dispersion relation then reads:

$$E_{\pm}(k) = \epsilon \pm 2t_1 \cos(ka) + 2t_2 \cos(2ka) \tag{2.11}$$

With $t_1 = 0.683$ eV and $t_2 = 0.612$ eV we set the twofold degenerate minimum of the lowest band to a minimum at $\pm k = \pm 0.82(2\pi/a)$. We achieve the splitting of these degenerate states by introducing hard-wall boundary conditions at the edges of the chain:

$$\phi_{-n-2} = \phi_{-n-1} = \phi_{-n+1} = \phi_{-n+2} = 0 \tag{2.12}$$

and we get a symmetric and an antisymmetric eigenstate. Again we see fast oscillations with a phase shift that share the same envelope, which in turn give a different result of the energy eigenvalues, representing the valley splitting.

Both EM and tight binding have their (dis-)advantages, where EM is computationally much lighter than tight binding, but tight binding can simulate valley splitting *ab initio*. Furthermore tight-binding approaches allow to accurately simulate the interactions of a Si/SiGe heterostrucutre with several million atoms or more atoms using NEMO software [70, 71, 72]. These approaches give numerically more accurate results than EM, but ultimately reveal the same physics.

The theoretical models are powerful to understand valley physics and give good estimates of the valley splitting. On the other hand valley splitting in an experiment depends on the atomic details of the Si/SiGe interfaces, because Si/SiGe interfaces extend over several atomic layers [73, 74], contain atomic steps [75, 70, 76], and are non-uniform due to surface roughness, which makes it difficult to have large and consistent valley splitting over a large qubit array [77]. In consequence we need to understand how valley splitting can be influenced and what parameters we can vary to increase the valley splitting.

The two main parameters that we vary to increase the valley splitting $E_v$ are the quantum well width $d$ and the external, vertical, electric field $E_z$. As we derived with the EM and tight binding approaches, the energy splitting of the two lowest lying valley energy $E_v$ oscillates with a phase shift, which is a direct consequence of the alignment of the valley states at the quantum well interfaces. In figure 2.4**a** we see the lowest lying states in red and blue with the characteristic phase shift. The phase shift at quantum well interface (dotted line at $x \approx 5$ nm) is then the valley splitting. In figure 2.4**b** we see that the

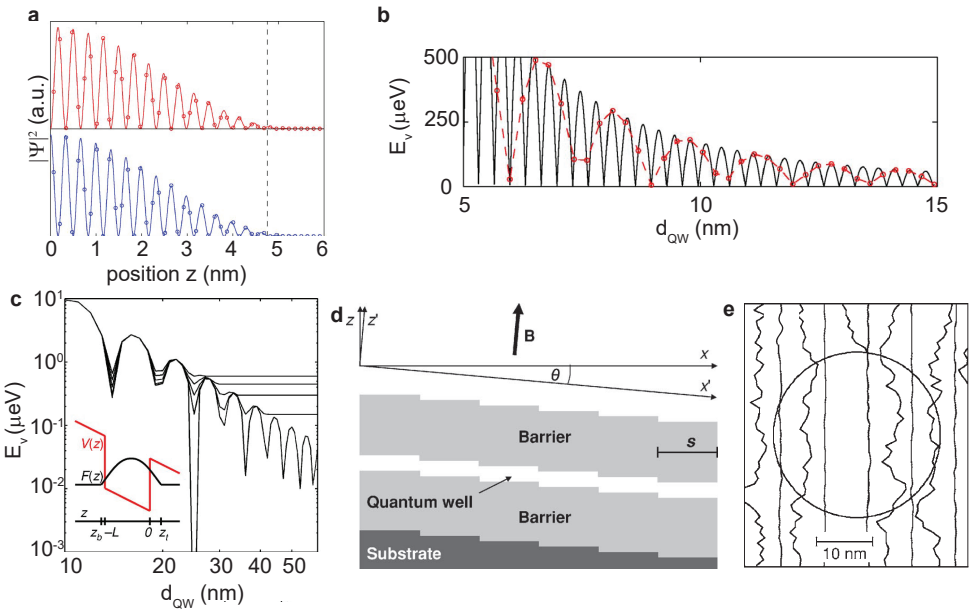


Figure 2.4: **a** Comparison of effective mass and tight binding results for the two lowest eigenstates in a $Si_{0.7}Ge_{0.3}/Si/Si_{0.7}Ge_{0.3}$ heterostructure with quantum well width of 9.5 nm. Only half the eigenfunctions are shown [67]. Top: solutions of the valley excited state. Bottom: ground state. Solid lines represent effective mass theory, circles tight-binding theory, and the dashed line the quantum well boundary. **b** Results of tight binding (red dot) and effective mass calculations (black line) of valley splitting in a finite square well with a well potential of 160 meV. The red dashed line is a guide for the eye. **c** Effective mass results for the valley splitting in an electric field $E$, as a function of the quantum well width, for five different $E$-fields. Inset: E-field geometry, with confinement potential $V(z) = V_{QW}(z) + V_\phi(z)$ and wave function $F(z)$, where $V_{QW}(z)$ is the quantum well potential and $V_\phi(z)$ is the electrostatic potential energy. **a**-**c** adapted from Ref. [67]. **d** Tilted quantum well with step size s. The crystallographic axes (x, y, z) are rotated by an angle $\theta$ to map the rotational axes (x', y', z'), assuming y = y'. **e** Randomly generated step edge profile, with smooth and rough step edges. The circle shows the radius of an electron wavefunction with $r = 15$ nm. **d** and **e** adapted from Ref. [75].

valley splitting overall increases with decreasing well width, since the alignment of the two valley states changes.

It is now interesting to understand how the electric field influences $E_v$. The inset in figure 2.4**c** shows how the electric field tilts the band structure and consequently, we have two different possibilities of realizing a quantum well. Either the lowest lying energy states are manifested in the standard square well or in a triangular well that is defined by the strength of $E_z$. The main panel of figure 2.4**c** shows how $E_z$ influences $E_v$ at different quantum well width. We again observe a general increase of $E_v$ with decreasing quantum well width regardless of electric field. For large quantum wells however, we see a saturation of $E_v$ at high $E_z$. This this saturation applies when the lowest lying states move from probing squared well barriers to probing triangular well barriers. We conclude the electric field will only increase $E_v$ if $E_z$ is high enough for the lowest lying states to experience a triangular well configuration.

Experimental quantum wells however, do not have ideal interfaces and are charac-

terized by atomic scale disorder [69, 67], finite interfacial widths [73, 74], and, possibly, atomic steps [73, 75, 70]. Especially atomic steps have a dramatic influence on $E_v$. Figure. 2.4**d** illustrates a simple model of atomic steps with length $s$ and step height $h$. $h$ is usually on the order of 1 mono-atomic layer, which in silicon is $h_{Si} = 0.136$ nm. At such a step the two lowest lying valley wavefunctions differ with a phase of $0.85\pi$, effectively causing destructive interference between the two states. In figure 2.4**e** we see an electron with a wavefunction radius $r = 15$ nm that covers several atomic steps and to further enhance valley splitting we can either increase the $s$ or confine $r$. Finally, we conclude that both, strong vertical confinement through $d$ and $E_z$ and lateral confinement through $s$ and $r$ can increase the valley splitting.

### 2.2.2. ELECTRICAL NOISE

The content in the following paragraphs have been rigorously discussed in Refs. [65, 78, 79, 80, 81, 82, 83] and is rephrased here for an overview of the mechanisms giving rise to electric noise. Electric noise or charge noise poses a limitation to the coherence of qubits through small changes in the electric and magnetic field in the qubit environment. The origin of the low-frequency changes is commonly attributed to so-called two-level fluctuators (TLF), found in an abundance of solid-state material platforms [84, 81, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96]. TLF are dynamic defects that switch at random between two states (1 and 2) with switching rates $\gamma_{1\to2}$ and $\gamma_{2\to1}$ for the transitions $1 \to 2$ and $2 \to 1$, respectively [97, 98, 99]. This switching ultimately leads to random telegraph noise (RTN), which manifests itself in form of current fluctuations in a resistor (see figure 2.5**a**). In Si/SiGe heterostructures TLF will only contribute to decoherence of qubits if the TLF energy splitting $E$ is less than a few $k_B T$ (with $k_B$ the Boltzman constant and $T$ the temperature), because higher energy splittings lead to a frozen ground state. For $E < k_B T$ we assume that the two switching rates $\gamma_{1\to2}$ and $\gamma_{2\to1}$ are equal and we write $\gamma_{1\to2} = \gamma_{2\to1} \equiv \gamma$. A set of TLF causing RTN with exponentially broad distribution of relaxation rates $\gamma$ produces a 1/f power spectrum in the frequency range $\gamma_{min} < \omega = 2\pi f < \gamma_{max}$, where $\gamma_{min}$ is the lowest switching rate of a TLF in the system, $\gamma_{max}$ is the highest switching rate of a TLF in the system with $E \approx k_B T$, and $\omega$ and $f$ represent the frequency range between $\gamma_{min}$ and $\gamma_{max}$ [65].

In the simplest case, $1/f$-like charge noise spectra are a quadratic function of the applied voltage onto an Ohmic resistor, which in turn means that the current fluctuates as a direct consequence of the fluctuation in the Ohmic resistance. The kinetics of such Ohmic resistance fluctuations on the microscopic scale have several origins.

When the kinetics of the fluctuations are characterized by one relaxation rate $\gamma$, the correlation function of the fluctuating quantity $x(t)$ is proportional to $e^{\gamma|t|}$ [65]. The spectral density then is a Lorentzian function of form

$$S_x(\omega) \propto \frac{1}{\pi} \frac{\gamma}{\omega^2 + \gamma^2} \equiv \mathscr{L}_x. \tag{2.13}$$

In a realistic solid state matrix however, there are usually several or even many TLF with varying relaxation rate, with a relaxation rate distribution $\mathscr{P}_x(\gamma)$. In this case the power spectral density becomes:

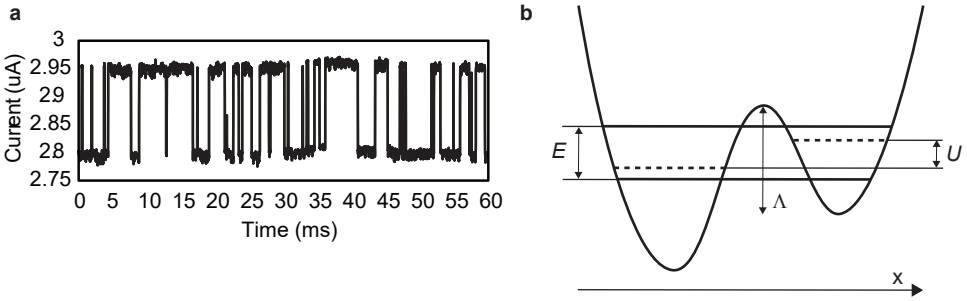


Figure 2.5: a) Example of random telegraphic noise caused by changes in the resistance of a Si field effect transistor caused by a nearby two-level fluctuator. The TLF originates from a single dominating trap within the measured device. Adapted from Ref. [101]. b) Schematic diagram of the potential energy of a two-level tunneling system against a spatial coordinate $x$ with a barrier of strength $\Lambda$. $U$ is the asymmetry of the energy levels in the two individual potential wells. In contrast E is the difference in energy of the two lowest lying energy of the TLF, which depends on $U$ and $\Lambda$. Adapted from Ref. [65].

$$S_x(\omega) \propto \int_0^\infty d\gamma \mathscr{P}_x(\gamma) \mathscr{L}_x \tag{2.14}$$

If $\mathscr{P}_x(\gamma) \propto \gamma^{-1}$ in a window $\gamma \gg \gamma_{min}$ the spectral density is $S(\omega) \propto \omega^{-1}$ following an 1/f-behaviour. A typical process that leads to such a behaviour, is a switching process $\gamma = \gamma_0 e^{-E/k_B T}$ with temperature activation $E/k_B T$.

The kinetics of the fluctuations can also depend on tunneling processes, where $\gamma$ then depends on the tunneling barrier width and height. In the case that the distribution of the tunnel barrier and height parameters is almost constant over a large range, then we get $\mathscr{P}_x(\gamma) \propto \gamma^{-1}$ again. It has been suggested that such fluctuations in semiconducting devices could arise from the exchange of electrons from semiconducting layer to the oxide layer through tunneling. The following characteristic relaxation rate then is $\gamma = \gamma_0 e^{-x/x_0}$, where x is the distance between the semiconductor interface and the TLF and $x_0$ is the characteristic decay length in the length scale of 1 Å [100]. This model has been extensively used to interpret $1/f$-noise in field-effect transistors [65].

Next, atoms (or in some cases groups of atoms) can occupy two positions in a crystal and their energy can be plotted as a double well potential (see figure 2.5**b**). The underlying assumption of this model is that certain atoms (or the groups of atoms) of mass $m$ can tunnel a distance $x$ through the potential $U$. The according TLF model [80, 78] consists of the asymmetry of $U$ and the tunnel matrix element $\lambda$, which characterizes the strength of the barrier. The tunnel amplitude between the two wells can then be written:

$$\Lambda = \hbar\omega_0 e^{-\lambda} \tag{2.15}$$

where $\omega_0$ is the frequency of the intra-well vibrations and $\hbar$ is the Planck constant. In turn, the excitation energy $E$ of a TLF is given by

$$E = \sqrt{\Lambda^2 + U^2} \tag{2.16}$$



Disorder directly influences $U$ and $\lambda$ of the TLF with probability distribution $\mathscr{P}(U,\lambda)$. In the region $\lambda \gg 1$ and $U \ll \hbar\omega$, the probability distribution is $\mathscr{P}(U,\lambda) = P_0$, where $P_0$ is a constant that is extracted from experiments [65, 82, 83].

The two-level transition rate of TLF is determined either by interactions with phonons (for insulating solids) or with electrons (in metals). Under the assumption that the diagonal splittings $U$ are dominant, we can write the interaction between the environment and a TLF as:

$$\mathscr{H}_{TLF-env} = g' \hat{c} \tau_z \tag{2.17}$$

where $\hat{c}$ is an operator in the Hilbert space depending on the specific interaction mechanism (phonons in insulators and electrons in metals), $\tau_z$ is the Pauli-z matrix acting on the TLS, and $g'$ is the matrix element arising from the overlap between the wavefunctions of the two wells. The TLF Hamiltonian is:

$$\mathscr{H}_{TLF} = \frac{1}{2}(U\tau_z + \Lambda\tau_x) \tag{2.18}$$

where $\tau_x$ is the Pauli-x matrix. By rotating the Hilbert space we can diagonalize the Hamiltonian from equation 2.18:

$$\mathscr{H}_{TLF} = (E/2)\tau_z \tag{2.19}$$

$$\mathscr{H}_{TLF-env} = g' \hat{c} (\frac{U}{E}\tau_z + \frac{\Lambda}{E}\tau_x) \tag{2.20}$$

The second term describes the interlevel transitions of the TLF-environment interactions. In consequence $\gamma$ for the deviation of the occupancy numbers of the levels from the equilibrium ones is proportional to $(\Lambda/E)^2$ [65, 81, 79] and the relaxation rate between the two levels is given by:

$$\gamma = \gamma_0(E)(\frac{\Lambda}{E})^2,\ \gamma_0 \propto E^a \coth(\frac{E}{2k_B T}) \tag{2.21}$$

where $\gamma_0(E)$ is the maximal relaxation rate for the TLF with the interlevel spacing $E$, $a$ in the exponent of $E^a$ is a scaling factor depending on the interaction mechanism (phonon or electrons). The following distribution of the relaxation rates is then written as:

$$\mathscr{P}(\gamma, E) = \frac{E}{2U\gamma}\mathscr{P}(U,\Lambda) = \frac{P_0}{2\gamma\sqrt{1-\gamma/\gamma_0}} \approx \frac{P_0}{2\gamma} \tag{2.22}$$

The proportionality of the distribution and the inverse of the relaxation rate, can be explained with the exponential term $\gamma \propto e^{-2\lambda}$ and the approximately uniform distribution of $\lambda$ in an exponentially broad interval [65].

To conclude this section we emphasize that charge noise arises through various physical mechanisms and poses a serious limitation for achieving ubiquitous high-fidelity operation of quantum gates required for a large spin-qubit systems. For Si/SiGe heterostructures in particular the TLF causing charge noise have been linked to remote impurities in the dielectric layers above the quantum well[48, 102] and to impurities nearby or within the quantum well, for example background impurities [103, 104, 105, 106] or crystalline defects such as threading or misfit dislocations [107, 108, 109]. The spatial distribution of these impurities is random, which limits the scalability of spin qubits due to a large device-to-device variability [47, 48]. Therefore, to achieve Si/SiGe heterostructures suitable for spin qubits we need to reduce all possible charge noise sources by reducing the underlying impurity densities, which will consequently lead to longer coherence times of spin qubits.



### 2.2.3. MAGNETIC NOISE

Magnetic noise, caused by the hyperfine interaction, describes the interactions of electrons with the atomic nucleus. Odd mass nuclei have a non-zero nuclear spin and in consequence carry a magnetic moment, leading to dramatically shortened decoherence times of spin qubits [63, 110]. The most dominant hyperfine-interaction term for electrons is the contact hyperfine interaction, arising from the overlap of the s-type Bloch wave functions with the nuclear sites,

$$H_{HF} \propto \mu_0 g_0 \mu_B \gamma_n \hbar \sum_{i=1}^{N} |\Psi(r)|^2 I_i \dot{S}. \tag{2.23}$$

Here $g_0$ is the free electron gyromagnetic ratio, $\gamma_N$ the nuclear gyromagnetic ratio, $I_i$ the nuclear spin at location $r_i$ in the crystal lattice and $|\Psi(r)|^2$ the magnitude of the electron wave function at the position of the nucleus [63]. It is possible to rewrite equation 2.23 as

$$H_{HF} \propto \sum_{i=1}^{N} A_i I_i \dot{S} \equiv g \mu_B B_N S \tag{2.24}$$

which defines $B_N$, the so called Overhauser field, which can be approximated as a random classical field acting on the electron spin. The most abundant isotopes in silicon have zero nuclear spin and in consequence are magnetically quiet. The only naturally occurring silicon isotope with spin 1/2 is $^{29}$Si and represents 4.7% or 47000 ppm of total natural amount of Si atoms. Furthermore, it is possible to isotopically enrich $^{28}$Si isotopes with a remaining $^{29}$Si-concentration of 60 ppm [111], allowing long coherence times [111], and ultimately high fidelity single- and two-qubit operations [112, 113, 114, 115].

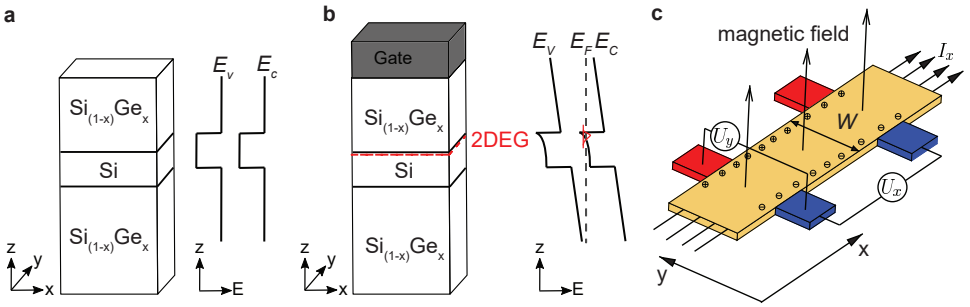


Figure 2.6: **a** Schematic of a Si/SiGe heterostructure with corresponding conduction band minima and valence band maxima. The bands align to form a type II quantum well. The depth of the quantum well depends on the concentration x. **b** Band diagram of a Si/SiGe heterostructure with an externally applied electric field. The conduction and valence bands tilt linearly until the Fermi level $E_F$ and electron start accumulating at the top interface of the quantum well to form a two-dimensional electron gas (2DEG). **a** and **b** adapted from Ref. [116]. **c** Schematic of a Hall-experiment with 4 voltage probes. Along the device we measure the current $I_x$ and the voltage drop $U_x$ When we apply an external magnetic field the Lorentz force pushes electrons one edge of the device. The following voltage drop is measured using $U_y$. Adapted from Ref. [117].

## 2.3. ELECTRICAL DEVICES FOR MATERIALS CHARACTERIZATION

For experiments concerning material performance we use two type of devices, Hall-bar heterostructure field effect transistors and gate-defined quantum dots. Both type of devices enable a variety of techniques, consequently allowing us to measure valley splitting, charge noise, and decoherence in the Si/SiGe platform.

### 2.3.1. HALL-BAR HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

The key elements of an H-FET in Si/SiGe heterostrucutres comprise a metal gate, an insulating layer consisting of a gate oxide and the SiGe barrier, and the semiconducting Si quantum well (see figure 2.6**a**). In these undoped heterostructures, electrons are accumulated in the quantum well by field effect upon biasing the top-gate.

We use the gate on top of the heterostructure to apply an external, vertical electric field $E_g$ to change the alignment of the bands (see figure 2.6**b**). When we apply such an electric field the Fermi level $E_F$ (the energy needed to add an electron to the conduction band) will move up or down depending on the sign of the applied potential. By applying a positive gate voltage $V_g$ we move $E_F$ upwards and start accumulating a two-dimensional electron gas (2DEG), once $E_F$ crosses the conduction band (see figure 2.6**b**). Since the 2DEG is quantized in the z-direction we write the time independent Schrödinger equation:

$$(-\frac{\hbar^2}{2}(\frac{1}{m_x^*}\frac{\partial}{\partial x^2}+\frac{1}{m_y^*}\frac{\partial}{\partial y^2}+\frac{1}{m_z^*}\frac{\partial}{\partial z^2}-eV(z)))\Psi(\vec{r})=E\psi(\vec{r}) \tag{2.25}$$

where, $m_x^*$,$m_y^*$, and $m_z^*$ are the effective mass of the electron in x-,y-, and z- direction respectively, $e$ is the electron charge, $V(z)$ is the potential coming from $E_g$, $\vec{r}$ is the position vector, and $\hbar$ is Planck's constant divided by $2\pi$. With the ansatz

$$\Psi(\vec{r}) = \phi(z)\Psi(x,y) = \phi(z)e^{i(k_x x + k_y y)} \tag{2.26}$$

where $k_x$ and $k_y$ the wave number in x- and y-direction respectively, we solve the Schrödinger equation and get the energy levels for the system:

$$E = E_{xy} + E_j = \frac{\hbar^2}{2}(\frac{k_x^2}{k_y^2} + \epsilon_j) \tag{2.27}$$

where $\epsilon$ is the quantization of the energy in z-direction with a known potential $V(z)$.

For measuring the electrical properties of the accumulated 2Deg, the gate electrodes of H-FETs is shaped as a Hall-bar (see figure 2.6**c**). We add voltage and current probes along the H-FET-channel and measure the current $I_{SD}$, the Voltage drop $U_x$ along the longitudinal channel direction, and $U_y$ along the transverse channel direction, for example as function of the gate voltage, magnetic field, or temperature.

### 2.3.2. GATE-DEFINED QUANTUM DOTS

Gate-defined quantum dots are the second kind of device that we use. In contrast to two-dimensional systems (such as 2DEGs), quantum dots are further confined in both lateral directions by using additional depletion and accumulation gates. Figure 2.7**a** shows a simple quantum dot architecture with two accumulation gates (S and D), two barrier gates (BL and BR), and a plunger gate P. Underneath the accumulation gates and the plunger we accumulate electron, where accumulation gates acts as electron reservoirs for the quantum dot underneath P. The barriers are designed to be depletion regions, that create tunnel barrier for electrons. The plunger gate is used to tune the chemical potential $\mu_c$. By applying a source-drain-bias to the device, there is potential between the source and the drain contact. Since the states in the quantum dot are quantized there is a ladder of states that moves with the plunger gate voltage $V_P$ (see figure 2.7**b**). If the there is no state underneath $P$ inside of the bias window we will not see conduction through the device. In turn, if a state is within the bias window we see a current going through the device (see figure 2.7**c**). A schematic graph of the current as a function of the plunger gate voltage is illustrated in figure 2.7**d**, where we see Coulomb peaks whenever current flows, and Coulomb-blockade when the current is 0.

In quantum dots the energy scales of $E_v$ and the orbital state splitting $\Delta E$ play a significant role. In the cases $E_v \gg \Delta E$ and $E_v \ll \Delta E$ the valley and orbital states are well defined (see figure 2.7**e**-**f**). If $E_v \approx \Delta E$ however, the valley and orbital states hybridize to valley-orbit-states [77]. The splitting between the two lowest lying valley-orbit states $V_{O1}$ and $V_{O2}$ form the ground-state splitting, which is the relevant energy splitting for spin qubits.

## 2.4. PHYSICAL CONCEPTS OF ELECTRICAL CHARACTERIZATION TECHNIQUES

We measure Hall-bar shaped H-FETs and quantum dots to probe the material environment in terms of valley splitting, electric noise, and magnetic noise. These measure-

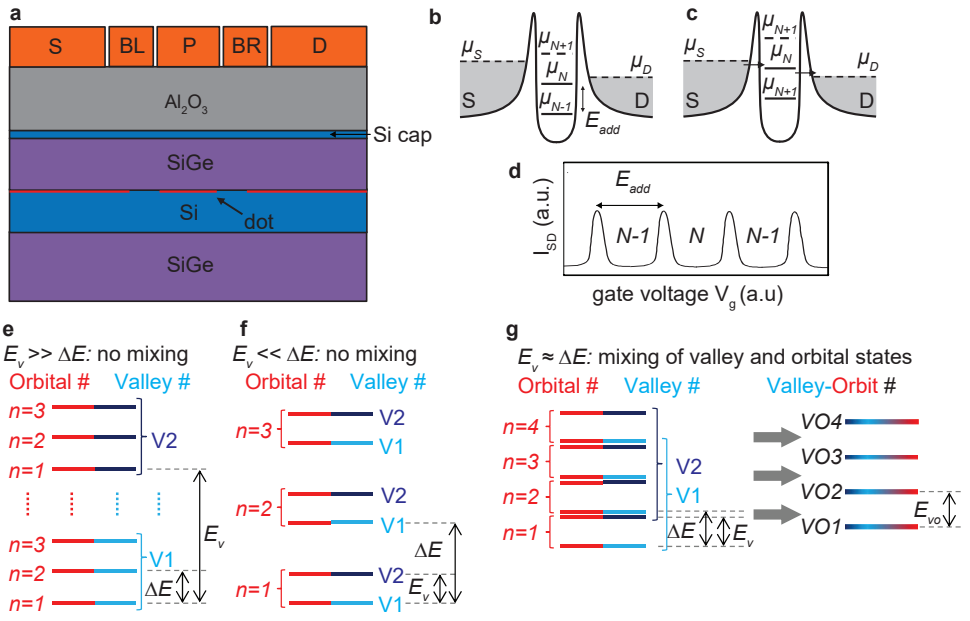


Figure 2.7: **a** shows a schematic of a quantum dot device in an undoped Si/SiGe heterostructure. The gates are sperated by an $Al_2O_3$-oxide layer and are divided into accumulation gates (S,P,D) and depletion gates (LB, RB). We accumulate electron reservoirs underneath S and D, and an electron island below P. LB and RB tune the tunnel barrier potential. Adapted from Ref. [116]. **b** shows a schematic diagram of the electrochemical potential of a single-electron transistor in absence of an available state in the bias window between $\mu_S$ and $\mu_D$. We call this configuration Coulomb blockade. **c** shows a schematic diagram of the electrochemical potential of a quantum dot with an available state in the bias window between $\mu_S$ and $\mu_D$. The N state is in the bias window, therefore one electron first hops from S to N, and then from N to D, resulting in a single-electron tunneling current. **d** shows current through a quantum dot as a function of the gate voltage $V_g$. Each time when an enery state is in the bias window, we see a sharp rise and decrease of the current, called a Coulomb peak. **e** and **f** show schematics of the energy states if the valley splitting $E_V$ is much luch larger and much lower than the orbital splitting $\Delta E$. In both cases the two energetic states will be well separated. **g** shows the schematics of the energy states if $E_V \approx \Delta E$. In this case the valley and orbit energy levels hybridize to valley-orbit energy states with the valley-orbit splitting $E_{vo}$. **b**-**f** are adapted from Ref. [42].

ments feed into the materials development cycle, to ultimately achieve high-performance qubits. These experiments serve two purposes: We first want to understand first the single device performance on a macro- or nanometer-scale and second we want to ensure wafer-scale reproducibility of devices.

### 2.4.1. THE CLASSICAL HALL EFFECT

When sending a current through a conductor (such as an H-FET) with an external, magnetic field $B = 0$ the current density $J$ is:

$$J = -nev = \sigma_{xx} E_g \tag{2.28}$$

where $n$ is the charge carrier density, $e$ is the electron charge, v is the velocity $\sigma_{xx}$ is conductivity term along the longitudinal direction of the current, and $E_{SD}$ is the ap-

plied electric field along the conductor. If the conductor is in a magnetic field however, the current also experiences the Lorentz force, causing a transverse conductivity $\sigma_{xy}$, called the Hall-conductivity. Together $\sigma_{xx}$ and $\sigma_{xy}$ form the conductivity tensor $\sigma$ in a 2D system:

$$\hat{\sigma} = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} \\ -\sigma_{xy} & \sigma_{xx} \end{pmatrix} \tag{2.29}$$

The corresponding equation of motion of an electron in such conditions is:

$$m^* \frac{dv}{dt} = -eE - ev \times B - m^* \frac{v}{\tau} \tag{2.30}$$

where, $m^*$ is the effective electron mass, $\frac{dv}{dt}$ is the velocity of the electron, the term $m^* \frac{v}{\tau}$ comes from the Drude model [118], and $\tau$ is the mean free time between momentum-relaxing-collisions of the electron. Solving equation 2.28 for $v$ and inserting it into equation 2.30 we get:

$$\begin{pmatrix} 1 & \omega_c\tau \\ -\omega_c\tau & 1 \end{pmatrix} J = \frac{e^2 n \tau E}{m^*} \tag{2.31}$$

where $\omega_c = eB/m^*$ is the cyclotron frequency. Here we define the conductivity as:

$$\sigma = \frac{ne^2\tau}{m^*} \tag{2.32}$$

and finally the conductivity and the resistivity $\hat{\rho}$ tensors follow the relation:

$$\frac{1}{\sigma}\begin{pmatrix} 1 & -\omega_c\tau \\ \omega_c\tau & 1 \end{pmatrix} = \sigma^{-1} = \rho = \begin{pmatrix} \rho_{xx} & \rho_{xy} \\ -\rho_{xy} & \rho_{xx} \end{pmatrix} \tag{2.33}$$

where $\rho_{xx}$ is the longitudinal resistivity, and $\rho_{xy}$ is the transverse resistivity. In practice we use the off-diagonal element $\rho_{xy} = \frac{B}{ne}$ to determine the electron density and the diagonal element $\rho_{xx} = \frac{m^*}{ne^2\tau}$ (at zero magnetic field) to calculate the mobility $\mu$, where we use $\mu = \frac{e\tau}{m^*}$.

### 2.4.2. SCATTERING MECHANISMS IN TWO DIMENSIONAL ELECTRON GASES

The electron mobility $\mu$ is a direct measure of the momentum relaxation an electron experiences while propagating through a resistor. In most cases, $\mu$ is a non-trivial function of the electron density $n$ and gives important insights on the dominant scattering mechanisms in the conductor, where several scattering mechanisms contribute to the resistivity. Their individual contributions to the measured mobility can be summed up using Matthiessen's rule [120]:

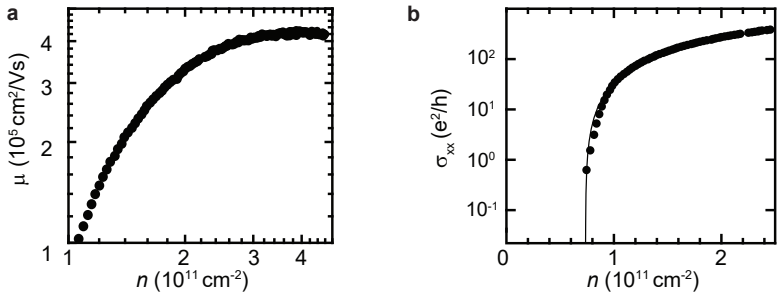


Figure 2.8: **a** Mobility $\mu$ as a function of density $n$ illustrating the typical steep rise at low density, and the flattening out of the curve at high density. **b** Conductivity $\sigma_{xx}$ as a function of $n$. The black line in **b** is a fit to percolation theory (see main text). Both panels adapted from Ref. [119].

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{remote}} + \frac{1}{\mu_{bgnd}} + \frac{1}{\mu_{RMS}} + \frac{1}{\mu_{MDD}} ... \tag{2.34}$$

where $\mu_{total}$ is the measured mobility, $\mu_{remote}$, $\mu_{bgnd}$, $\mu_{MDD}$, and $\mu_{RMS}$, are the mobilities of the remote impurities, background impurities, misfit dislocations and surface roughness scattering, respectively, that the material would have if there was no other scattering source. For Si/SiGe heterostructures treated by scattering theory within the Born approximation, Monroe *et al* [121] conclude that three relevant mechanisms limit the mobility in Si/SiGe heterostuctures at practical densities up to about $10^{12}\text{cm}^{-2}$:

$$\mu_{remote} = \frac{16\pi^{1/2} g_v^{1/2} g_z^{1/2} e n^{3/2} h^3}{\hbar N_{\square}} \tag{2.35}$$

$$\mu_{bgnd} = \frac{g_v^{3/2} g_z^{3/2} e n^{1/2}}{4\pi^{1/2} \hbar n_{bgnd}} \tag{2.36}$$

$$\mu_{RMS} = \frac{e^5 g_v^3 g_z^3}{192\pi^3 \hbar \epsilon^2 \epsilon_0^2 \pi \Lambda^2 \Delta^2 E^2 n} \tag{2.37}$$

where, $g_v$ is the valley degeneracy, $g_z$ the is the spin degeneracy, $\hbar$ the Planck constant, $D_{IT}$ is interface trap density, $n$ is the electron density, $n_{bgnd}$ is the background impurity concentration in the quantum well, $\epsilon_0$ is the dielectric permittivity in vacuum, $\epsilon$ it the dielectric constant of the gate stack, $\Lambda$ is the charateristic length of the Si/SiGe interface roughness, $\Delta$ is the RMS roughness of the Si/SiGe interface, and $E$ is the external electric field. The only difference here is that for scattering from remote impurities Monroe *et al* [121] assume a modulation doped heterostructure, which defers from our case. For our undoped Si/SiGe heterostructures however, we have trapped charges at the semiconductor/dielectric interface and in the gate oxide which we approximate as a 2D charge density. For a formal derivation of formulas 2.35, 2.36, 2.37 and the derivation of four other possible mechanisms $\mu_{threading}$, $\mu_{alloy}$, $\mu_{strain}$, and $\mu_{vicinal}$ see Ref.

[121]. In figure 2.8**a** we see a typical mobility-density curve. Due to the different power dependence each of the scattering mechanisms, each density regime is dominated by a different scattering mechanism. At low density for example, we see a typical steep rise of the mobility due to the screening of remote impurities, therefore $\mu_{remote}$ is dominant and the curve follows $n^{1.5}$. At higher densities several mechanisms can be dominant e.g. $\mu_{bgnd}$ is dominant in the density regime between 2-3*$10^{11}$ cm$^{-2}$, where the curve follows a power law dependence of $\approx n^{0.5}$. At densities $n > 4 * 10^{11}$ cm$^{-2}$ the curve first flattens out until the slope becomes negative. Dominating mechanisms in this regime need to behave $\alpha < 0$, e.g. scattering from the surface roughness between the Si quantum well and the SiGe barrier [122, 121, 123, 124].

Another metric that we obtain from classical transport measurements is the percolation transition density $n_p$, which is the lowest density, that allows a continuous conduction path in a field effect transistor. $n_p$ is particularly interesting because it indicates material quality in the low-density regime of a Hall-bar shaped H-FET at electron densities that are comparable to the number of electrons in a two-dimensional quantum dot array. For example, if we assume a quantum dot with dimensions of 50 nm×50 nm loaded with one electron the electron density is $n_{QD} = 4 * 10^{10}$ cm$^{-2}$. If $n_p > n_{QD}$ it implies that, likely, disorder in the system will make it challenging to reproducibly achieve the single electron regime for spin-qubit manipulation. Therefore we are interested in providing heterostructures where $n_p \leq n_{QD}$.

$n_p$ originates from the locally-varying conduction band minimum in the metal-to-insulator transition (MIT), where an inhomogeneous distribution of accumulation sites in the FET manifests itself in the accumulation of localized charge puddles. With increasing gate voltage, and therefore a larger overlap of the Fermi level and the conduction band minimum, the puddles grow in size and number until electrons percolate through the entire channel. We extract $n_p$ using a fit to the function $\sigma_{xx} = A(n - n_p)^{1.31}$, where A is a fitting parameter, $n$ is the electron density, and 1.31 is the power law dependence of a percolation transition in two dimensions [125]. It is important to note, that this relationship only holds in the low-density regime of the conductivity-density relationship (see figure 2.8**b**), where we observe a nonlinear failure of screening of the remote impurities [125].

### 2.4.3. THE QUANTUM HALL EFFECT

The quantum Hall effect (QHE, Nobel prizes for the integer QHE [129] in 1985 and the fractional QHE in 1998 [126]) arises at low temperatures and strong magnetic field and is characterized by quantization of $\rho_{xy}$ in a two-dimensional electron gas in a semiconductor:

$$\rho_{xy} = \frac{2\pi\hbar}{e^2\nu} = \frac{R_K}{\nu} \approx \frac{25.8}{\nu} k\Omega \tag{2.38}$$

where $\nu$ is an integer number of quantized Landau levels also called filling factor, and $R_K$ is the von-Klitzing constant. In figure 2.9**a** we see the resistivities $\rho_{xx}$ and $\rho_{xy}$ in the quantum Hall effect as measured by Klaus von Klitzing [129]. In contrast to the classical Hall effect $\rho_{xy}$ will increase from resistivity plateau to the next one in step-wise

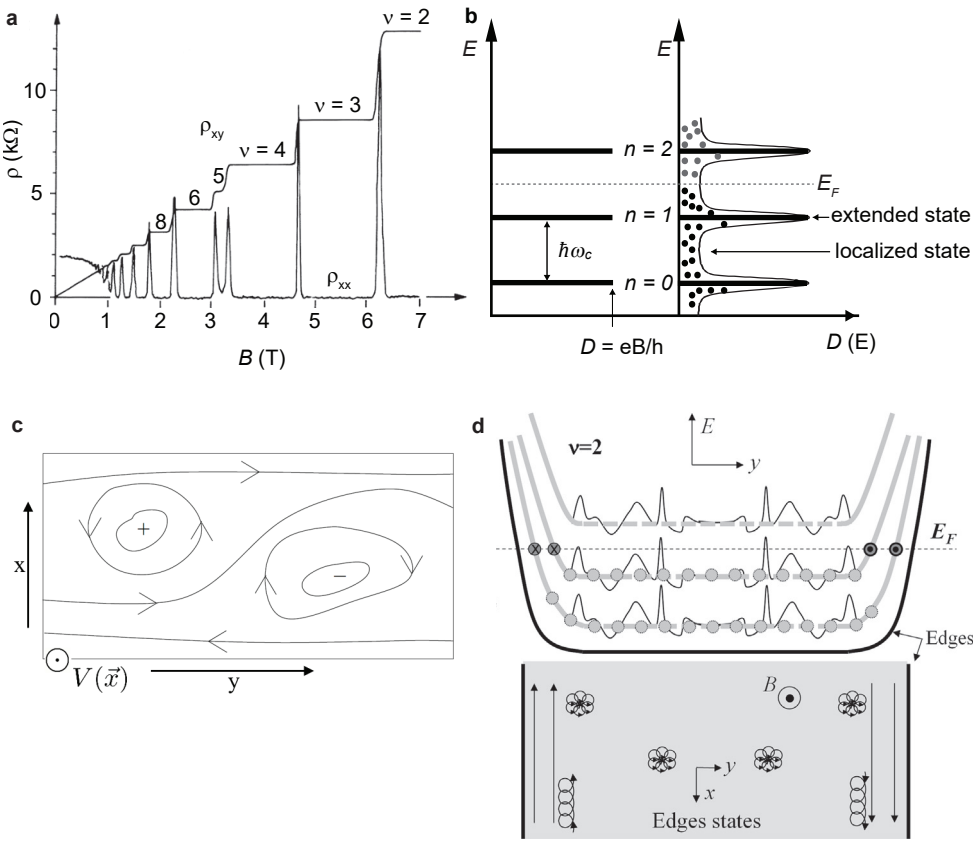


Figure 2.9: **a** Quantum Hall effect measurement by Klaus von Klitzing. Adapted from Ref. [126]. **b** Schematic of ideal Landau levels (left) and broadened Landau levels (right) with the Fermi energy lying in between the second and third Landau level. **c** Schematic drawing of a potential landscape in a 2DEG from a top-view. The lines are equipotential lines, the "+" sign denotes a potential peak and the "-" sign a potential dip. Taken from [127]. **d** Landau levels bent by the confining potential (top). Schematic of two edge states and localized states in real space (bottom). **b**, and **d** taken from Ref. [128].

$1/\nu$-intervals. Similarly, $\rho_{xx}$ oscillates with magnetic field and the oscillations are called Shubnikov-de Haas oscillations (SdH). Whenever there is a plateau in $\rho_{xy}$, $\rho_{xx}$ will be zero. This alignment of $\rho_{xy}$ and $\rho_{xx}$ always occurs when the magnetic field is:

$$B = \frac{2\pi\hbar n}{e\nu} = \frac{n}{\nu}\Phi_0 \tag{2.39}$$

where $\Phi_0$ is the flux quantum, and $n$ is the density. From this relationship we are able to extract $n$ just from the periodicity of the filling factors in $1/B$.

The observation that the resistivity of the SdH oscillations becomes 0 is remarkable since this behaviour suggests, that we have a perfect conductor in this regime. However, if we calculate the longitudinal conductivity $\sigma_{xx}$ through matrix inversion of equation 2.33:

$$\sigma_{xx} = \frac{\rho_{xx}}{\rho_{xx}^2 + \rho_{xy}^2} \tag{2.40}$$

we also see that the conductivity is 0 if $\rho_{xy} \neq 0$ and $\rho_{xx} = 0$, which means that the system is a perfect insulator. At first glance having a perfect conductor and a perfect insulator simultaneously, seems contradictory. However, both statements are true since in the QHE we have no current flowing in the longitudinal direction of the Hall-bar ($\sigma_{xx} = 0$), and $\rho_{xx} = 0$ implies that there is no dissipation of energy due to the absence of scattering.



LANDAU LEVELS

To obtain a deeper understanding of the QHE we examine the quantum-mechanical picture of electrons in a magnetic field. We use a Hamiltonian to describe the eigenstates and eigenvalues of electrons moving in the $xy$-plane in a magnetic field oriented along the z-axis:

$$H = \frac{1}{2m}(p + eA)^2 = \hbar\omega_c(a^+ a + 1/2) \tag{2.41}$$

where p is the canonical momentum and A is the vector potential, $\omega_c = eB/h$ is the cyclotron frequency, and $a$ is a scaling operator obeying $[a^+, a] = 1$. This Hamiltonian, yields the energy spectrum of a harmonic oscillator with highly degenerate energy values [128] where each energy eigenstate $\epsilon_n$ is a Landau level (Fig. 2.9**b**) with an energy separation of (for a detailed derivation the reader is referred to Ref. [130]):

$$\epsilon_n = \hbar\omega_c(n + 1/2) \tag{2.42}$$

where n is an integer. It results, that the cyclotron frequency is quantized (figure 2.9**b**) with a density of states for each Landau level of $eB/h$ [128].

In the right panel of figure 2.9**b**, however, we see a more realistic picture of the Landau levels, where the degeneracy within each Landau level is lifted. The reason for this lifting of the degeneracy is that disorder creates a spatially varying potential that is much smaller than the energy spacing of the Landau levels, which causes the Landau levels to broaden and creates extended states in narrow energy bands centered around each Landau level, as well as localized states at energies in between Landau levels [128] (see figure 2.9**b**). Localized states are spatially pinned because they sit on equipotential lines (see figure 2.9**c**) in peaks or dips of the potential and therefore do not carry current. Extended states, however, arise at the edge of the device geometry where the potential rises steeply. Figure 2.9**d** shows a schematic drawing of a device with edges in the QHE regime (bottom) with the confinement potential of such a device (top) where the Fermi level $E_F$ lies between the second and third Landau level. The relative position of $E_F$ is tuned by varying the Landau level (by sweeping either $n$ or $B$). When $E_F$ is located in between two Landau levels there is a range of energies where no conduction is possible since $E_F$ either crosses no states or exclusively localized states, which explains the plateaux in

both $\rho_{xx}$ and $\rho_{xy}$ in figure 2.9**a**. Whenever the $E_F$ comes close to Landau level however, there is conduction through the extended states at the edge of the channel. It is worth to note, that at finite Temperatures electrons are allowed to hop between equipotential lines through activation from the thermal energy and additionally contribute to the resistivity changes around each Landau level.

Lastly we want to understand the origin of the von Klitzing constant $R_H$. At the edges of the device shown in figure 2.9**d** $E_F$ crosses a finite number of extended states, which corresponds to $\nu$. Each of these extended states is one-dimensional and at opposite sides of the device the group velocity of is reversed due to the cyclotron motion induced by the external magnetic field. Thus, all states with opposite momentum are spatially separated on opposite sites of the samples, which forbids electron backscattering [128]. In consequence, the conductance through these edge states is ballistic (there is no dissipation of energy) and scattering theory of electronic transport [131, 132] shows that the conductance of a 1D ballistic state is $h/e^2 = R_H$.

We use the quantum Hall effect to quantify the energy separation of two neighbouring Landau levels. Under the influence of temperature the longitudinal resistivity $\rho_{xx}$ can be described using an Arrhenius relationship:

$$\rho_{xx} = \rho_0 * exp(\Delta/2k_BT) \tag{2.43}$$

where $\Delta$ is the activation energy, $k_B$ is the Boltzmann constant, $T$ is the temperature, and $\rho_0$ is the resistivity of the sample when the Temperature exceeds the activation energy.

### 2.4.4. CHARGE SENSING WITH QUANTUM DOTS

Quantum dots in Si/SiGe may host spin qubits, but in the context of materials developement we use them mainly as a local probe for valley splitting and charge noise. A quantum dot operated on the flank of a Coulomb peak is sensitive to small current displacements in the surrounding environment e.g. a change in the charge state $N$ of another quantum dot. Figure 2.10**a** shows a double-quantum-dot system with a nearby charge sensor formed of a quantum dot. In this architecture we use the sensing-quantum dot (SD) underneath the gate SDP to understand the behaviour of the target-quantum dots (TD) underneath the gates RP and LP.

The lower panel of figure 2.10**b** illustrates the current underneath the gate $LP$ $I_{LP}$ as a function of the gate voltage $V_{LP}$, with schematically drawn Coulomb peaks. Each time we add an electron to the quantum dot we see that the signal-to-noise ratio of the Coulomb peaks gets larger. In contrast, in the upper panel of figure 2.10**b**, we see current underneath SDP $I_{SDP}$ also as a function of $V_{LP}$. $I_{SDP}$ changes because $LP$ and $SDP$ are capacitively coupled. Each time that a charge state becomes available, $I_{SDP}$ jumps. Using this technique we see charge transitions, that are not detectable by solely monitoring $I_{LP}$, such as the first jump in the upper panel of figure 2.10**b**. Charge-transitions are mapped in figure 2.10**c** as a function of the gate voltages $V_{RP}$ and $V_{LP}$ in a charge-stability diagram. With (X,Y) we indicate how many electron are in the left dot (X) and in the right dot (Y). In this case the charge transitions are ideal, meaning there is no

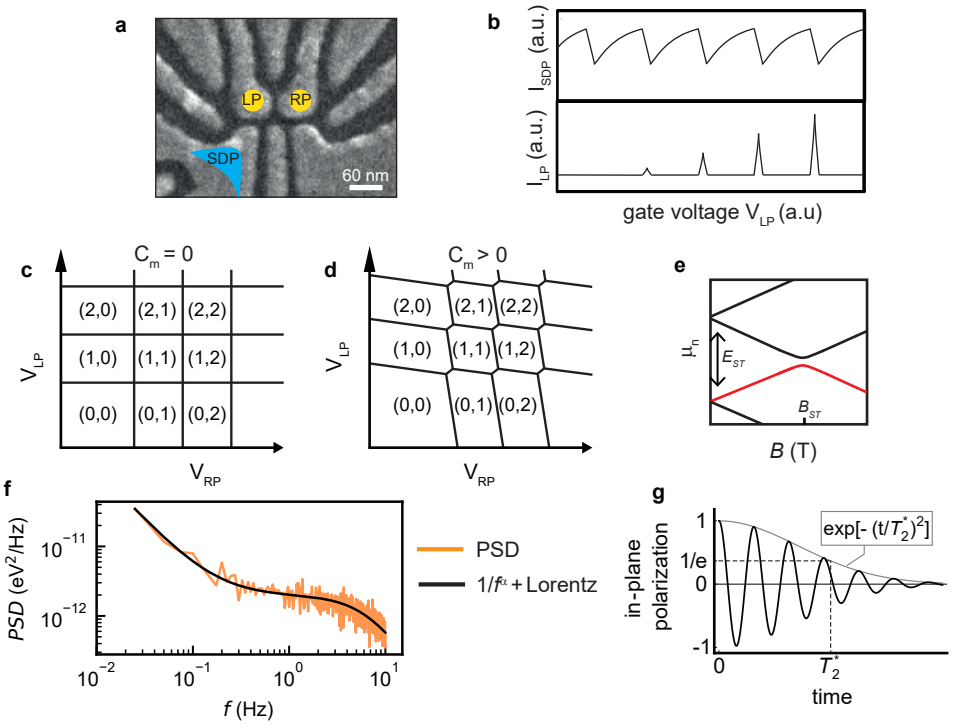


Figure 2.10: **a** False-coloured scanning electron microscope image of a double quantum. Quantum dots are formed underneath LP and RP. SDP functions as a charge sensor [73]. **b** Schematic of noninvasive charge sensing of the LP-quantum dot using the quantum dot underneath SDP. The transport current $I_{LP}$ shows Coulomb peaks as a function of the quantum dot plunger gate voltage $V_{LP}$. The sensing current $I_{LP}$ shows the cahracteristic jumps that occur whenever a state bcomes available underneath the gate $LP$. **c** Schematic stability diagram for a double dot system without interdot tunneling. **d** Schematic stability diagram for a double dot system with interdot tunneling. Adapted from Ref. [63]. **e** Energy evolution of the ground state and first excited state in a single quantum dot as a function of the magnetic field. The red line shows the expected spin filling for the charge transition $N = 1 \rightarrow 2$. At $B = B_{ST}$ the typical kink is observed, where the Zeeman energy $E_Z$ is equal to the singlet-triplet splitting energy $E_{ST}$ [73]. **f** Power spectral density of current fluctuations (orange line) from a 40 second measurement, revealing a significant deviation from $1/f^{\alpha}$-noise due to one strong TLF with a switching frequency $\gamma \approx 6.5$ Hz. **g** Schematic of a typical Ramsey experiment, showing oscillations of the in-plane polarization of a qubit as a function of time. The oscillations follow a Gaussian decay envelope that allows us to extract $T_2^{\star}$ [133].

capacitive coupling $C_m$ between $V_{RP}$ and the left dot and $V_{LP}$ and the right dot. In reality however, there is capacitve coupling between the quantum dots and all surrounding gates. Therefore the transition lines in the charge-stability diagram become tilted (see figure 2.10**d**).

We are interested in using these double quantum dots with a charge sensor as a probe to measure for example charge noise or the singlet-triplet energy splitting $E_{ST}$, where $E_{ST}$ usually gives a lower bound on the valley splitting $E_v \geq E_{ST}$ [134, 135]. We measure $E_{ST}$ by varying the parallel magnetic field and monitoring either the (0,1)→(0,2)-charge transition. By varying the magnetic field the transition line moves upwards, because we

add a spin ↑ to form the singlet ground state $S_0$. The slope will move upwards until the $S_0$ is energy degenerate with the next available $T_-$ state at a magnetic field $B_{ST}$, where we observe a characteristic kink. After the kink the $T_-$-state becomes the new ground state of the two-electron system and the slope moves downwards. $E_{ST}$ is determined from the position of the kink with $E_{ST} = g\mu_B B_{ST}$, where g is the electron gyromagnetic ratio (g-factor) in silicon, and $\mu_B$ is the Bohr magneton.

Next, we measure low-frequency charge noise by monitoring the current as a function of time and extracting the current noise spectrum $S_I$ using a Fourier transform in a regime where current fluctuations are most pronounced. In quantum dots the flank of a Coulomb peak is the most sensitive region where the derivative of the current $|dI/dV|$ is highest, indicating that the current fluctuations are dominated by fluctuations in the electrochemical potential [136, 84]. In this case small current fluctuations $\delta I$ can be expressed as:

$$\delta I = \frac{dI}{dV}\frac{\delta_\epsilon}{\alpha} \tag{2.44}$$

where $\delta_\epsilon$ represents the fluctuations in the electrochemical potential and $\alpha$ is the lever arm. To convert the current noise spectrum to a charge noise spectrum $S_\epsilon$ we use:

$$S_\epsilon = \frac{\alpha^2 S_I}{|dI/dV|^2} \tag{2.45}$$

In chapter 2.2.2. we theoretically discussed, that these charge-noise spectra follow either a power-law frequency dependence or in some cases the sum of a power law and a Lorentzian. In figure 2.10**f** we show a charge noise spectrum representative of the power law plus Lorentzian case. Here, the spectrum deviates from $1/f$ due to a strong TLF with switching frequency $\gamma \approx 6.5Hz$.

### 2.4.5. COHERENCE TIMES IN SPIN QUBITS

In the previous section we examined how to use a quantum dot as a charge sensor to probe the performance of other, nearby quantum dots. On the other hand we can use spin qubits in the measurement dots themselves as sensors as well. The coherence times of spin qubits are sensitive to the host environment and can be seen as the ultimate metric to benchmark material performance.

Qualitatively, the coherence time describes the time a phase oscillation of a superposition state is coherent. To measure a coherence time we use a Ramsey experiment where a qubit is initialized to a state in the equatorial plane of the Bloch sphere. We then measure the in-plate polarization of the state as a function of time, by changing the monitoring time of the experiment. For low frequency noise the resulting time trace approximately follows a cosine with a Gaussian decay envelope [137]:

$$P_x(t) = exp((-t/T_2^\star)^2)\frac{1+cos(\omega t)}{2} \tag{2.46}$$

A typical curve from a Ramsey experiment is found in figure 2.10**g**. Nevertheless, there are caveats in using $T_2^\star$ as a metric: First, tuning a device into a regime where we can measure $T_2^\star$, is non-trivial and often requires longer time periods in the order of days to weeks compared to Hall-bar or quantum dot measurements which take minutes to hours, second, $T_2^\star$ is a non-trivial function of the electric environment of the qubits, where small changes can already change $T_2^\star$ significantly [138, 115, 133], third, because $T_2^\star$ is non-trivial it is challenging to define a set of experimental conditions that make $T_2^\star$ comparable across devices. These caveats should not be seen as an obstacle, in fact they should encourage the improvement of materials, devices, and measurement equipment in quality and reproducibility, such that $T_2^\star$ will become a more central metric in the evaluation of Si/SiGe heterostructures. An initial study of statistical coherence time performance in spin qubits and a guide for future studies on $T_2^\star$ is given in Ref. [133].

# 3

# EXPERIMENTAL METHODS AND SETUPS

*He who is good with a hammer thinks of everything as a nail.*

Abraham Maslov

## 3.1. SI/SIGE HETEROSTRUCTURES

In this thesis we consider two different streams of Si/SiGe heterostructures. The first stream of heterostructures is provided by Intel within the context of the Intel-Qutech partnership. These heterostrucutres are deposited on industrial 300 mm substrates in an advanced semiconductor fabrication facility. Our role has been to fabricate and electrically characterize H-FETs on these wafers to advance the material development cycle at Intel. The second stream of heterostructures is developed locally in Delft by the Scappucci group. We grow our own $^{28}$Si/SiGe heterostructure at Else Kooi laboratories (EKL) at the Technical University Delft, using the same crystal growth techniques used by industry. This allows us to implement fast feedback cycles on the material and to port the learnings from our own heterostructures to an industrial fab.



### 3.1.1. $^{NAT}$SI/SIGE HETEROSTRUCTURES ON INDUSTRIAL 300MM SI WAFERS

$^{nat}$Si/SiGe heterostructures are grown on 300 mm <100> silicon wafers. These heterostructures comprise a $Si_{0.7}Ge_{0.3}$ strained relaxed buffer obtained by step grading of the germanium content, a 10-nm-thick strained Si quantum well, a 30-nm-thick $Si_{0.7}Ge_{0.3}$ barrier and a 1-nm-thick Si cap. Before fabrication, these wafers are laser-cut by an external supplier into five 100 mm wafers so we can further process them to H-FETs using the 100 mm wafer processing tools in the clean room facilities at EKL.

### 3.1.2. $^{28}$SI/SIGE HETEROSTRUCTURES ON A 100 MM WAFER AT TU DELFT

$^{28}$Si/SiGe heterostructures are grown at EKL using chemical vapor deposition (CVD). CVD is the mainstream crystal-growth method used by the semiconductor industry to deposit epitaxial layers for tailoring the electronic properties of semiconductor stacks for electronic devices. In figure 3.1**a** we see a schematic of a CVD growth process. One or more precursor gases react with a heated solid-state substrate, where the precursor gas deposits the desired atoms at the surface and the byproducts of the reaction remain in the gas phase.

In our case we use reduced pressure CVD, an industry compatible process, that operates in the pressure regime between 0.01 and 1000 mbar. To grow our heterostructures we use an ASMI Epsilon 2000 CVD system consisting of a quartz chamber, a rotating graphite susceptor, integrated heat lamps that can heat the chamber up to 1200 °C, and gas inlets for the precursors. Before the gas inlets there is an additional part, the precursor injection zone, where the precursor gases are injected with proper flow alongside the carrier gas ($H_2$). From there the gases move into a single line, the main manifold, where the precursors are then mixed. Once the gases reach the quartz chamber through the gas inlets their flow through the chamber is laminar and steady, ensuring that the gas uniformly reaches the rotating graphite susceptor hosting the target substrate.

We use 100 mm <100> silicon wafers with a resistivity of 1-5 Ωcm as a the substrate for the hetero-epitaxial growth of Si/SiGe heterostructures. To grow the different layers of Si/SiGe heterostructures we use three precursor gases: natural dicholorsilane ($SiCl_2H_2$) 100 %, germane ($GeH_4$) diluted 2 % in $H_2$, and isotopically enriched silane ($^{28}SiH_4$) with a purifcation of 800 ppm diluted 1 % in $H_2$. These precursors lead to three thermally activated reactions for the growth of Ge, $^{nat}$Si, and $^{28}$Si:

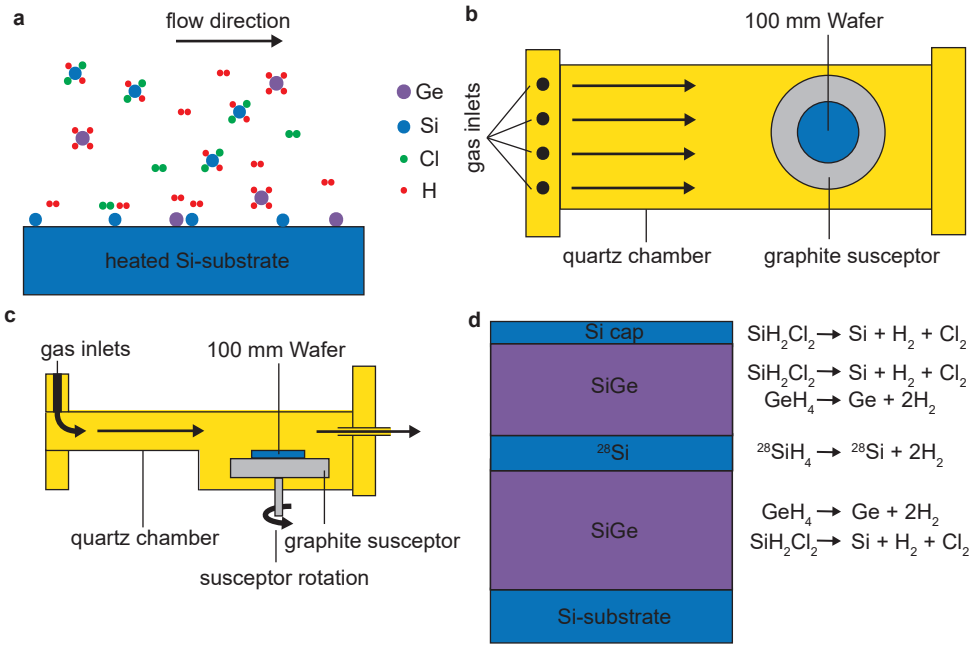


Figure 3.1: **a** Schematic diagram of SiGe growth using CVD. Dichlorosilane and germane react with the heated surface, where Si and Ge adhere to the substrate and $H_2$ and $Cl_2$ from in the gas phase. **b** Schematic top view of the ASMI Epsilon 2000 CVD system. **c** Schematic side view of the ASMI Epsilon 2000 CVD system. **b** and **c** adapted from [139]. **d** Schematic of a typical Si/SiGe heterostructure with the chemical reactions that grow the respective layer.

$$GeH_4 \rightarrow Ge + 2H_2 \tag{3.1}$$

$$SiH_2Cl_2 \rightarrow Si + H_2 + Cl_2 \tag{3.2}$$

$$^{28}SiH_4 \rightarrow ^{28}Si + 2H_2 \tag{3.3}$$

In figure 3.1**d** we see which reactions are responsible for the growth of each individual layer of the Si/SiGe heterostructures. Reaction 3.1 and 3.2 grow the virtual substrate and the barriers of the heterostructure, reaction 3.3 grows the isotopically purified quantum well, and reaction 3.2 by itself is used for the Si-cap growth. Since growth parameters vary between chapters in this work, the specific growth details are found in the respective supplementary sections.

Growing the material at EKL is crucial to accelerate the development of the heterostructures for several reasons. First, $^{nat}$Si quantum wells are usually grown with DCS due to the lower temperature range [140]. $^{28}$Si quantum wells however, are grown with silane because silane is the final product of isotopical enrichment of $^{28}$Si precursors [141]. As a consequence, the thermal budget difference requires to reengineer the entire material stack when moving from $^{nat}$Si to $^{28}$Si. Second, a 100 mm wafer tolerates thicker virtual substrates compared to a 300 mm wafer, where thick virtual substrates

decrease the threading dislocation density [142] and also increase the distance between existing dislocations in the deeper layers of the heterostructure and the quantum well therefore, thick virtual substrates introduce less disorder into the system.

### 3.1.3. STRUCTURAL CHARACTERIZATION OF THE MATERIAL STACK

In chapter 2.1 we have analyzed how electrical properties are used to determine performance. However, prior to electrical analysis of the heterostructures we use material characterization methods to get chemical and structural insights into our growth process. In this thesis three characterization techniques are of significant relevance: transmission-electron-microscopy (TEM), secondary-ion-mass-spectroscopy (SIMS), and atom probe tomography (APT).

TEM is based on the same principles as light microscopy, but because of the much shorter wavelength of electron in comparison to light, the diffraction limit is in the sub-

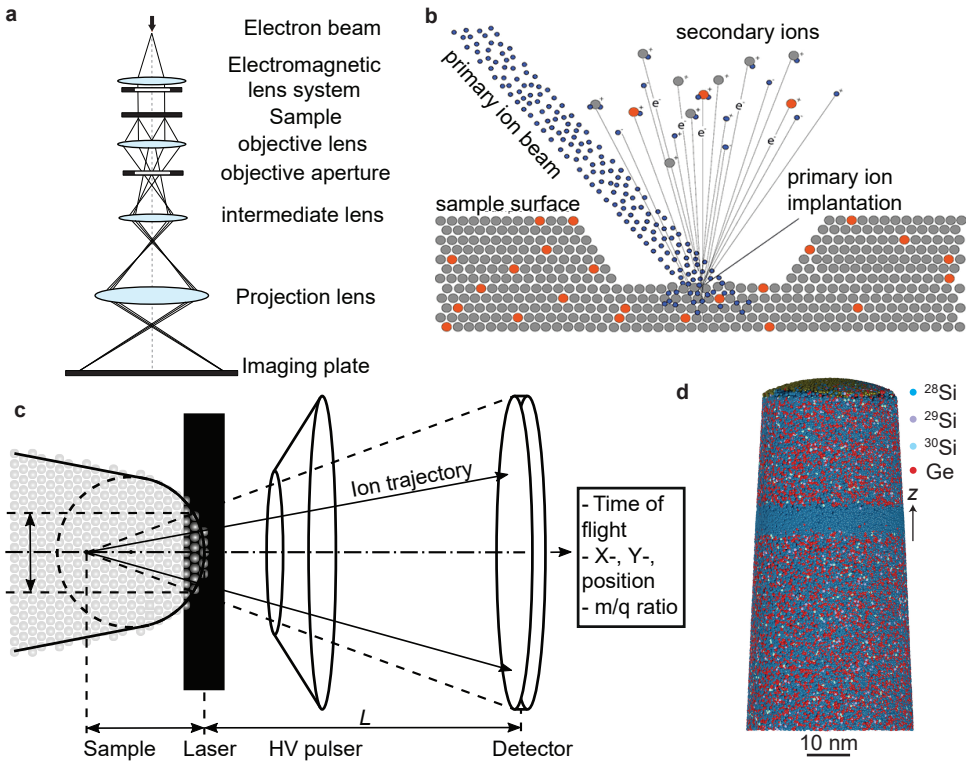


Figure 3.2: **a** Schematic overview of a transmission electron microscope. A complex system of electromagnetic lenses and apertures focuses the electron beam onto the imaging plate. Picture adapted from [143]. **b** Zoom into the sample surface during secondary ion mass spectrometry. Secondary ions fly through vacuum and are eventually collected by an ion mass analyzer. Picture adapted from [144]. **c** Working principle of atom probe tomography. Atoms are ionized by a laser and an HV pulser and the detector records the time of flight, the X and Y position as well as charge to mass ratio. Adapted from [116]. **d** Atom probe tomography reconstruction of a $^{28}$Si/SiGe heterostructure. Adapted from [73].

nm regime. In particular, TEM uses a complex system of electromagnetic lenses (see figure 3.2**a**) to focus a beam of electrons onto a sample to create an image. The electrons are transmitted through a thin piece of the sample, also called the lamella, and collected by a detector, revealing details of the morphology, composition, and crystalline structure of the material. The contrast of a TEM is sensitive to the atomic weights, allowing to distinguish between different elements in the lamella. In our case, we use TEM to determine the quantum well and barrier thicknesses, the interface quality at the top and bottom of the quantum well, as well as the structural quality of the semiconductor/dielectric interface.



SIMS is a key analytical technique for research, development, and process control of compound semiconductor epitaxy and devices. In particular, SIMS is a destructive technique to detect atom and isotope concentrations in thin films with nm-depth and µm-lateral resolution. The first step of SIMS is to place a thin film sample into a vacuum and focus a beam of primary ions onto the sample. This process etches away particles from the target material ((see figure 3.2**b**)) where the etched particles are called secondary ions. Secondary ions freely move through the vacuum after their removal and are eventually collected by a mass spectrometer which assigns the mass of an incoming secondary ion to the respective atom/isotope. SIMS has an accurate elemental detection limit in the order of $10^{12}$ cm$^{-2}$ - $10^{16}$ cm$^{-2}$ and because we measure the mass of the incoming ions, we are able to distinguish the isotopic composition in the sample. In our case, we use SIMS to first quantify the amount of remaining $^{29}$Si isotopes in the quantum well, so we are able confirm reduced magnetic noise from hyperfine interaction and second to determine the concentration of background impurities in the heterostructure introduced during the growth, such as oxygen or carbon.

APT is the only available technique offering extensive capabilities for both, 3D imaging and chemical composition measurements at the atomic scale (depth 0.1 nm; lateral 0.3-0.5 nm). APT samples are prepared to form a truncuated cone with a hemispherical cap. Under the influence of high DC voltages (5-25 kV), and high electric field (10 V/nm) at the tip surface atoms are ionised and evaporated individually at each pulse towards a position sensitive detector a distance L away from the sample (see figure 3.2**c**). The detector then measures the time of flight of ions, the $m/q$-ratio (where $m$ is the mass and $q$ the electric charge), the X,Y position where the ions hit the detector and the order of arrival of the atoms. Repeating this sequence for many atoms and taking all the measurements into account, a dedicated software is able to reconstruct the original position of the ions at the tip and allows to achieve a 3 D image of the material (see figure 3.2**d**). In our case we use APT to determine the quantum well width, the quantum well/barriers interface sharpness and roughness over the size of a quantum dot, as well as to investigate the presence of atomic steps or other correlated chemical disorder at the quantum well/barrier interface.

We refer the interested reader to Ref. [145] (TEM), Ref. [146] (SIMS), and Ref. [147] (APT) for a more rigorous and exhaustive description. Additionally, we have used also other characterization techniques such as electron energy loss spectroscopy (EELS, chapter 7) to assess chemical composition, or geometric phase analysis (GPA, chapter 8) to infer local strain variations. Since we have used these techniques occasionally, they are described in the respective chapters and the interested reader is referred to Ref. [148]

(EELS), and Ref. [149] (GPA) for a more rigorous description.

## 3.2. FABRICATION PROCESSES

Device fabrication on 100 mm wafers comprises two steps. First we perform a pre-fabrication for micron-scale devices and structures such as Hall-bars, bonding pads, and ohmic contacts, and subsequently a nano-fabrication process to fabricate quantum dot devices.



### 3.2.1. PRE-FABRICATION OF MICRON-SCALE TEMPLATES

The pre-fabrication is performed using tooling for 100 mm wafers at EKL. A schematic of the pre-fabrication process is illustrated in figure 3.3**a**. First the Si/SiGe heterostructures go through a standard photo-lithography step consisting of: spin coating with SPR 3012 positive photoresist, optical lithography with an ASML PAS 5500/80, and development with MF322 developer. A subsequent dry etching process with HBr + Cl plasma using a Trikon Omega 201 produces the mesa for physical isolation of the quantum well and the optical markers for mask alignment. The remaining photoresist is then removed by oxygen plasma using a Tepla Plasma 300.

A standard wet cleaning process is performed consisting of a 99% $HNO_3$-solution-bath to remove organic particles, a 69.5% $HNO_3$-solution-bath at 100 °C to remove inorganic particles, rinsing, and drying. Another standard photo-lithography step is performed to prepare the wafer for ion implantation. Then phosphorous ions are implanted using a TLC Varian E500HP. After implantation there is another plasma cleaning and another standard wet cleaning. Implants are activated through a 15 seconds rapid thermal annealing at 700 °C using an SSI Solaris 100. The temperature is chosen to stay below the Si quantum well growth Temperature of 750 °C, to avoid diffusion of Ge atoms into the Si quantum well and strain relaxation.

Another standard cleaning process is performed and then a 10 nm thick $Al_2O_3$ is deposited through atomic layer deposition using a Picosun R-200 Advanced at a temperature of 300 °C. Afterwards there is an additional standard photo-lithography step. A standard HF dip is performed using BHF 1:7 solution with subsequent rinsing and drying opening windows through the AlO layer to the ohmics. To finish this part of the process a final wet etch with acetone is performed to remove organic residuals.

The wafer is again cleaned using the standard cleaning process. Before deposition of the Al-gate photo-lithography is performed: Two spin-coating processes with diluted positive SPR3012 photoresist and negative AZ nLOF 2000 photoresist positive resist, optical lithography,with an ASML PAS 5500/80, and development with MF322 developer. A subsequent oxygen plasma using Trikon Omega 201 removes the positive SPR3012 from the opened windows. A 200 nm aluminum film is sputtered and a lift-off process removes the remaining thin film from the wafer. Afterwards the wafer is cleaned with $HNO_3$.

The wafer is once more cleaned using the standard cleaning process. Before deposition of the Ohmic contacts there is another standard HF-dip step and another photo-lithography step with negative AZ nLOF 2000 photoresist, and MF322 developer. Subsequently, the Ohmic contacts of 2 nm titanium and 20 nm platinum are deposited through physical vapor deposition. A lift-off process removes the remaining remaining thin film

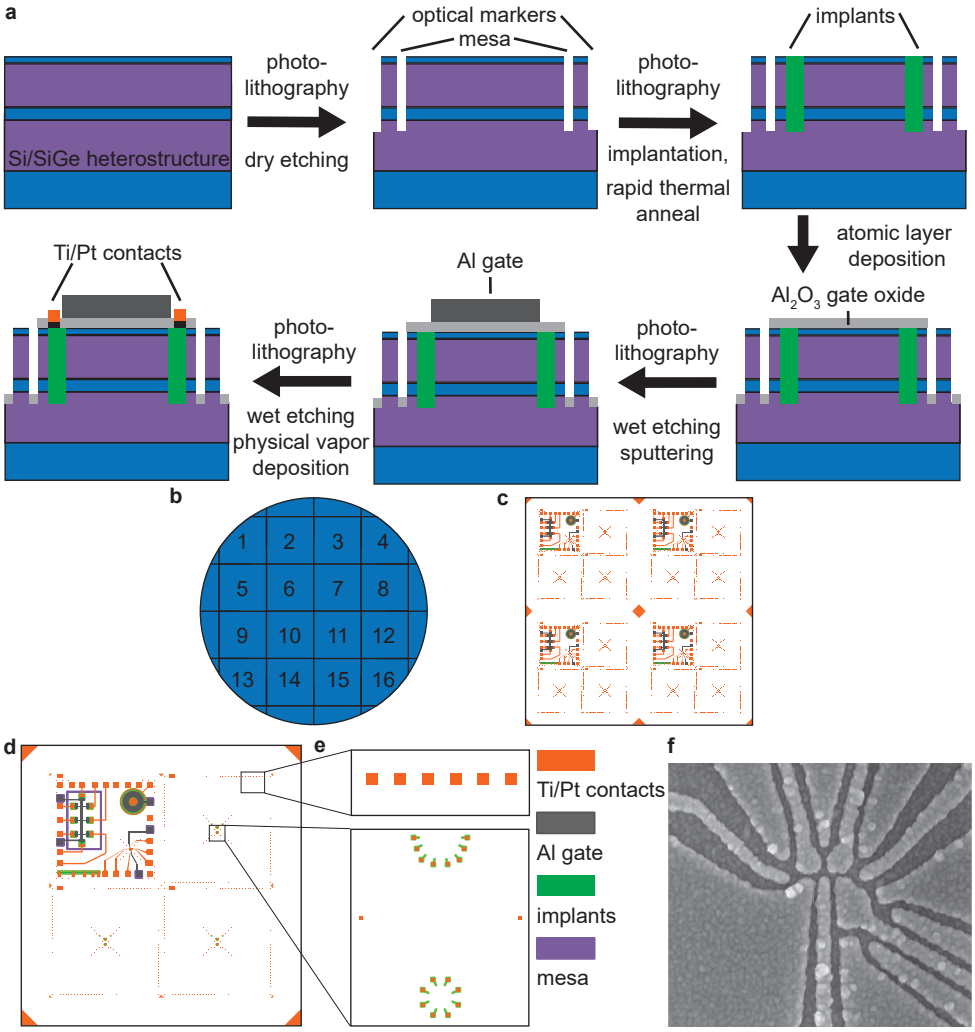


Figure 3.3: **a** Schematic illustration of the 100 mm-wafer fabrication process. Each step also contains a cleaning process, which is omitted in the graph but described in the main text. **b** Wafer diced into sixteen 2 cm×2 cm coupons. **c** Zoom into a coupons with four 10 mm × 10 mm duplicate cells. **d** Zoom into a cell, further divided into four identical chips. The top left chip hosts large-scale structures such as Hall-bars, a Corbino disk, and a transmission line. The other three are identical to each other and host bondpads and ohmic contact for subsequent nano-fabrication. **e** Zoom into an ohmic contact and implant region for nano-fabrication. **f** Scanning-electron-microscope image of a nano-fabricated double quantum dot device.

from the wafer, patterning the Aluminum gates.

As the last step the wafers are diced into sixteen 2 cm×2 cm coupons (see figure 3.3**b**), where the four corner coupons have only three corners. Each coupon hosts four 10 mm × 10 mm duplicate cells, shown in 3.3**c** and each cell hosts four quadrants (see figure 3.3**d**). The top left quadrant illustrates the large structures that are used to mea-

sure material performance, containing a large Hall-bar H-FET (top left), a Corbino disk (top right), a transmission line (bottom left), and a small Hall-bar H-FET (bottom right). The other three quadrants are identical to each other and are used for nano-fabrication where Ohmic contacts and implants are illustrated in 3.3**e**. Each chip is labelled with a unique number, which allows to track the position of every device coming from a wafer, such that it is possible to locate possible differences in device performance, for example we can compare devices that originate from the center with devices from the edge of the wafer.



### 3.2.2. FABRICATION OF NANO-SCALE TEMPLATES

Nano fabrication is performed at the van Leeuwenhoek laboratories (VLL) in the Applied Science faculty of the Technical University Delft. Nano-fabrication is performed on a single coupon. Fabrication of double quantum dot devices begins with a wet cleaning step using isopropanol and acetone. Subsequently, a lithography process is performed consisting of spin-coating, baking at 150 °C, electron-beam lithography, and development with pentylacetate and isopropanol. Then the thin-film metal gates consisting of 3 nm titanium and 17 nm paladium are evaporated thorugh physical vapr deposition and a lift-off process removes the remaining lacquer thin-film from the wafer.

Finally, the coupons are diced into sixteen cells, where twelve cells host the nano-fabricated devices, and the other four host the previously described, micron-scale structures. In figure 3.3**f** we see a typical double quantum dot device that went through both fabrication processes. More complicated fabrication schemes are described in chapters 6, 8, and 9 where devices with multilayer gate stacks are integrated.

## 3.3. EXPERIMENTAL SETUPS FOR CRYOGENIC MEASUREMENTS

The relevant energy scales of the quantum Hall effect and quantum dots are much smaller than the thermal energy at room temperature, therefore samples need to be cooled down in cryogenic systems where the thermal energy is in the range of $\simeq$ 4 μeV (50 mK) to $\simeq$ 340 μeV (4 K). To characterize samples at such low temperatures the cryogenic systems are then connected to control and measurement electronics at room temperature. The first system we use for device characterization at cryogenic temperatures is an attoDRY2100 pulse tube refrigerator which reaches a base temperature of 1.6 K and is equipped with a superconducting magnet reaching magnetic field of up to 9 T. The second system is a Leiden MCK50-400 dilution refrigerator which reaches a base temperature of 50 mK and is equipped with a superconducting magnet reaching magnetic field of up to 12 T. Both refrigerators are top-loading systems with thermal cycle times shorter than 12 hours, which benefits our goal to achieve fast material-device-measurement feedback cycles. These top-loading systems are constrained in space and therefore can only host a limited number of DC wires. We circumvent this constraint using cryogenic multiplexers, which in turn enable high throughput measurements of our devices with statistically relevant feedback.

### 3.3.1. ATTODRY2100 PULSE TUBE REFRIGERATOR

The attoDRY2100 is a cryogenic refrigerator operating in the temperature range between 1.6 K - 300 K, without supply of external cryogenic liquids. The cryogenic refrigerator consists of a main unit, a support unit, a helium gas storage vessel, scroll pump and a compressor. The main unit contains the cryostat with a superconducting magnet inside, also called the isolation volume. The support unit contains the control electronics, a pulse tube cooler valve, and a pulse tube cooler buffer reservoir [150].

The cooling part of the refrigerator comprises, a compressor, three heat exchangers, a regenerator, two helium pressure lines, an orifice, a reservoir volume and a pulse tube (see figure 3.4**a**). We also call the cooling part a pulse tube cryocooler, even though the pulse tube is only a single part of the cooling apparatus. The compressor moves He gas back and forth at room temperature, therefore the pressure within the system decreases and increases. When the compressor increases the pressure, gas enters the regenerator - a periodic flow heat exchanger usually consisting of a porous medium with large specific heat - and the regenerator will absorb heat from the gas. The cold gas then flows through the heat exchanger cold plate and the orifice to the reservoir, where the gas again transmits heat to its surroundings. When the compressor decreases the pressure the gas moves back through the entire circuit towards the compressor and removes heat from the regenerator.

The pulse tube has the function to separate the cold and warm ends. Therefore it is necessary that gas is only able to travel a fraction of the tube length, such that the gas in the middle of the tube can act as an insulating barrier between the cold and warm end.

Besides the cooling apparatus the Attocube system is equipped with a thermometer,

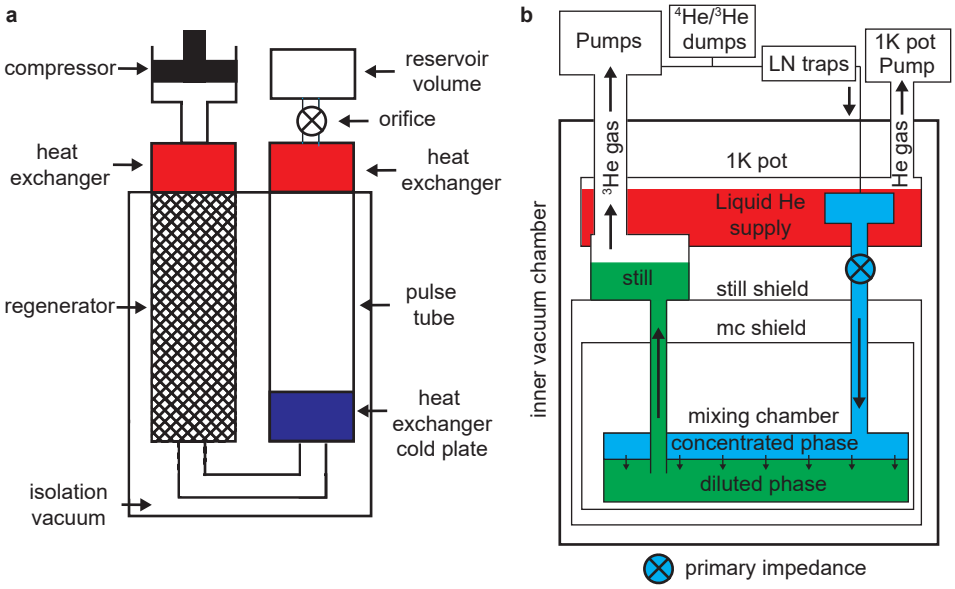


Figure 3.4: **a** Schematic overview of the pulse tube used in the attocube. Picture adapted from [150]. **b** Schematic overview of a dilution refrigerator. Picture adapted from [151].

a heater, wiring to room temperature, and a cryogenic multiplexer printed-circuit board (PCB) supporting 13 samples and 8 direct current (DC) connections. The PCB is connected first through the wiring and then through a Fischer 24-pin coaxial cable to the control and measurement electronics.

### 3.3.2. LEIDEN MCK50-400 DILUTION REFRIGERATOR

The Leiden MCK50-400 refrigerator is a wet cryogenic refrigerator system that consists of a cryogenic liquid vessel, a 1 K-pot, a mixing chamber, a still, a circulation system, nitrogen cold traps, and a gas handling system, schematically drawn in figure 3.4**b**. During operation the cryogenic liquid vessel is filled with liquid helium with a temperature of 4.2 K. The liquid helium bath is connected to the 1 K-pot, where an external scroll pump can reduce the temperature of the helium in the 1 K-pot to 1.6 K through evaporative cooling.

Once the 1 K-pot has reached its base temperature of 1.6 K the gas handling system will induce $^4$He to the circulation system. First the $^4$He flows through liquid nitrogen traps (LN traps) to trap residual gas atoms (e.g. oxygen). Afterwards the $^4$He pipe goes through the 1K point where the $^4$He gas liquefies. The $^4$He then flows through a primary impedance filling the mixing chamber with liquid $^4$He. A turbo pump attached to the far end of the still then evaporatively cools the mixing chamber to 800 mK. As soon as all $^4$He gas is condensed, the gas handling system starts inserting $^3$He into the circulation system, which will liquefy in the mixing chamber. Below 870 mK the mixture of $^4$He and $^3$He undergoes a spontaneous phase separation in the mixing chamber, where a concentrated phase (100% $^3$He) and a dilute phase (6.6% $^3$He) are in equilibrium. Inside of the mixing chamber $^3$He flows from the concentrated phase through the phase boundary into the dilute phase. This diluting process is endothermic and removes energy in form of heat from the mixing chamber. The $^3$He then moves towards the still where it evaporates due to its lower boiling point. In consequence, there is a steady $^3$He-flow in the circulation system. Here, the still can be heated to increase the flow in the mixing chamber, which ultimately allows to reach a base temperature of 50 mK. The additional mc and still shields ensure further thermal isolation of the mixing chamber from its environment.

Besides the cooling apparatus the Leiden system is equipped with three thermometers (1K-pot, still, and mixing chamber), two heaters (still and mixing chamber), wiring to room temperature, a superconducting magnet, and an exchangeable cryogenic multiplexer printed-circuit board (PCB) supporting either 13 samples and 8 DC wires or 5 samples with 22 DC wires, depending if the devices under test (DUT) are Hall-bar shaped H-FETs or quantum dots. The PCB is connected first to the wiring and then through two Fischer 24-pin coaxial cables to the control and measurement electronics.

### 3.3.3. CONTROL AND MEASUREMENT ELECTRONICS

Both the Attocube and the Leiden systems use the same type of instrumentation to quantify sample properties. In both cases the coaxial cables leaving the fridge are connected to an isolated matrix module, which is equipped with internal $\pi$-filters that filter and suppress interference up to >10 GHz. The matrix module allows micro coaxial connectors (MCX) to connect to an IVVI-rack and a serial peripheral interface (SPI)-rack, where

both racks are powered by isolated batteries and are also galvanically isolated from all other instrumentation to avoid coupling of signals from the 50 Hz power grid.

The two racks host 16-bit digitial-to-analog converters (DAC), as well as a series of exchangeable, custom-built measurement modules [152, 153]. DACs operate with a range of ±2 V, centered around -2 V, 0 V, or 2 V. The measurement modules are isolated input modules for DC and alternate current (AC) voltages, voltage amplifiers, current-to-voltage (IV) converter modules, and isolated output modules for DC and AC voltages.

The output modules are connected to two types of measurement instruments. First, an SR830 lock-in amplifier is used for low-frequency AC-signaling and detection. The output and inputs of the lock-in amplifier are connected to the measurement modules via coaxial cables. Second, a Keithley DMM6500 digital multimeter is used for DC detection. This type of multimeter is equipped with a 16-bit digitizer card with a maximum sample rate of 1 M samples/s.



All instrumentation is connected to a computer where the DACs in the IVVI-rack are connected through an optical fiber, the SPI-rack through an in-series connection of a C2-microcontroller box [153] and a USB connection, the multimeter is connected through a USB port, and the lock-ins are connected through GPIB-connectors. With the computer we have full software control over the measurement instruments, the SPI-rack, and the IVVI rack through QCoDeS, a Python-based data acquisition framework developed by the Copenhagen/ Delft/ Sydney/ Microsoft quantum computing consortium [154].

Hall-bars are operated by applying a AC voltage of typically 100 μV with a frequency of 7.777 Hz to the source contact and a DC voltage to the gate. The drain contact is connected to a current-to-voltage converter module converting and amplifying the AC current to an AC voltage. The amplified AC voltage is then detected by the lock-in. In addition, potential differences on the Hall-bar are amplified with amplifier modules and then detected with the lock-ins. Quantum dots are operated by applying a DC voltage of typically 100 μV to the source contact of the quantum dot and DC voltages applied to the gates. The drain contact is connected to a current-to-voltage converter module converting and amplifying the DC current to a DC voltage. The amplified DC voltage is then detected by the multimeter.

# 4

# MULTIPLEXED QUANTUM TRANSPORT USING COMMERCIAL OFF-THE-SHELF CMOS AT SUB-KELVIN TEMPERATURES

*Continuing advancements in quantum information processing have caused a paradigm shift from research mainly focused on testing the reality of quantum mechanics to engineering qubit devices with numbers required for practical quantum computation. One of the major challenges in scaling toward large-scale solid-state systems is the limited input/output (I/O) connectors present in cryostats operating at sub-kelvin temperatures required to execute quantum logic with high-fidelity. This interconnect bottleneck is equally present in the device fabrication-measurement cycle, which requires high-throughput and cryogenic characterization to develop quantum processors. Here we multiplex quantum transport of two-dimensional electron gases at sub-kelvin temperatures. We use commercial off-the-shelf CMOS multiplexers to achieve an order of magnitude increase in the number of wires. Exploiting this technology we accelerate the development of 300 mm epitaxial wafers manufactured in an industrial CMOS fab and report a remarkable electron mobility of* $(3.9\pm0.6)\times10^5$ $cm^2/Vs$ *and percolation density of* $(6.9\pm0.4)\times10^{10}$ $cm^{-2}$*, representing a key step toward large silicon qubit arrays. We envision that the demonstration will inspire the development of cryogenic electronics for quantum information and because of the simplicity of assembly and versatility, we foresee widespread use of similar cryo-CMOS circuits for high-throughput quantum measurements and control of quantum engineered systems.*

This chapter has been published in B. Paquelet Wuetz*, P. L. Bavdaz*, L. A. Yeoh, R. Schouten, H. van der Does, M. Tiggelman, D. Sabbagh, A. Sammak, C. G. Almudever, F. Sebastiano, J. S. Clarke, M. Veldhorst and G. Scappucci, Multiplexed quantum transport using commercial off-the-shelf CMOS at sub-kelvin temperatures, NPJ quantum information **6**, 43 (2019) [155]
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## 4.1. INTRODUCTION

With quantum computing technology advancing at a fast pace, noisy intermediate-scale quantum (NISQ) technology with 50-100 qubits are predicted to be realized in the near future [156, 157]. Solid-state quantum processors in the NISQ era and beyond will be realized by mass-fabrication on wafers including 300 mm technology . Optimization and validation approaches for quantum materials and devices are therefore required that can rely on an increasingly fast-feedback cycle. Since quantum technology operates at sub-kelvin temperatures, cryogenic solutions for fast testing will have to be developed.

The decades of advancement in classical technology following Moore's law has been made possible by approaches dictated by Rent's rule $T = tg^p$, where the Rent exponent $p$ relates the total number of control lines $T$ and proportionality factor $t$ with the number of internal components $g$ [158, 159]. This same rule has been predicted to be required for practical quantum processors [160], but we also envision that this rule will determine the progress in fabrication and validation, with the Rent factor crucially determining how many devices can be tested simultaneously.



One pursuit toward scalable testing is to adapt room temperature wafer-scale probing at cryogenic temperatures. Indeed, a cryogenic wafer prober has recently been developed to establish a high-volume 300 mm test-line for quantum devices [161]. The measurement temperature in probe-based systems, however, is limited to a few kelvin. Furthermore, integration of magnets required for material characterization is challenging to achieve on large-size probe systems. Alternatively, cryogenic on-chip multiplexers have been developed in GaAs/AlGaAs [162, 163, 164, 165] and Si/SiGe [166] heterostructures, operating at a temperature of 1.6 K and 0.2 K, respectively. With this approach the number of quantum devices measured in one cooldown on a single chip is increased without the need to alter existing cryostat setups. However, the design and implementation of on-chip multiplexers is specific to the materials and device under test (DUT). Furthermore, an architecture that works at base temperature of a dilution refrigerator, high magnetic fields, and is independent of the number and type of DUT has yet to be developed.

In this Article we deploy digital CMOS logic at $T$ = 50 mK to increase the number of wires available at cryogenic temperature by an order of magnitude while keeping the overhead number of I/O wires at room temperature fixed (Fig. 4.1). Our cryogenic platform is based on general-purpose commercial off-the-shelf multiplexers driven by a nearby shift-register, is operated under the extreme temperature and magnetic fields achieved in dilution refrigerators, and can be readily integrated in any kind of cryostat. We have specifically designed the cryo-CMOS circuit to act as a switch and allow for high-throughput quantum transport measurements. Multiple devices can be screened for relevant metrics in the same cooldown either individually or at once by time-division multiplexing (TDM) without introduction of any artifacts.

To prove the value of this architecture for accelerating the fabrication-measurement cycle of quantum devices, we focus on an archetypal measurement in condensed matter physics: magnetotransport of 2DEGs in the classical and quantum Hall regime. These measurements are used to evaluate statistically key metrics of high-mobility Si/SiGe heterostructures field effect transistors, relevant for spin-qubits in Si [167, 168], currently leading the field of quantum computation with quantum dots [41]. We exploit the cryo-

multiplexing platform to accelerate the development of 300 mm epitaxial wafers manufactured in an industrial CMOS fab and report record values of electron mobility and percolation density at sub-kelvin temperatures, relevant for large silicon spin-qubit arrays.

## 4.2. CRYOGENIC MULTIPLEXER PLATFORM

Figure 4.2 shows schematics of our experimental setup. At the heart of the architecture is a printed circuit board (cryo-MUX PCB; Fig. 4.2**c**) operating at 50 mK. The cryo-MUX PCB comprises cascaded serial-input parallel-output (SIPO) shift registers which provide $N$ outputs lines, each of them controlling $M$ outputs lines of multiplexer components. Few input/output (I/O) wires connect the cryo-MUX PCB to room temperature



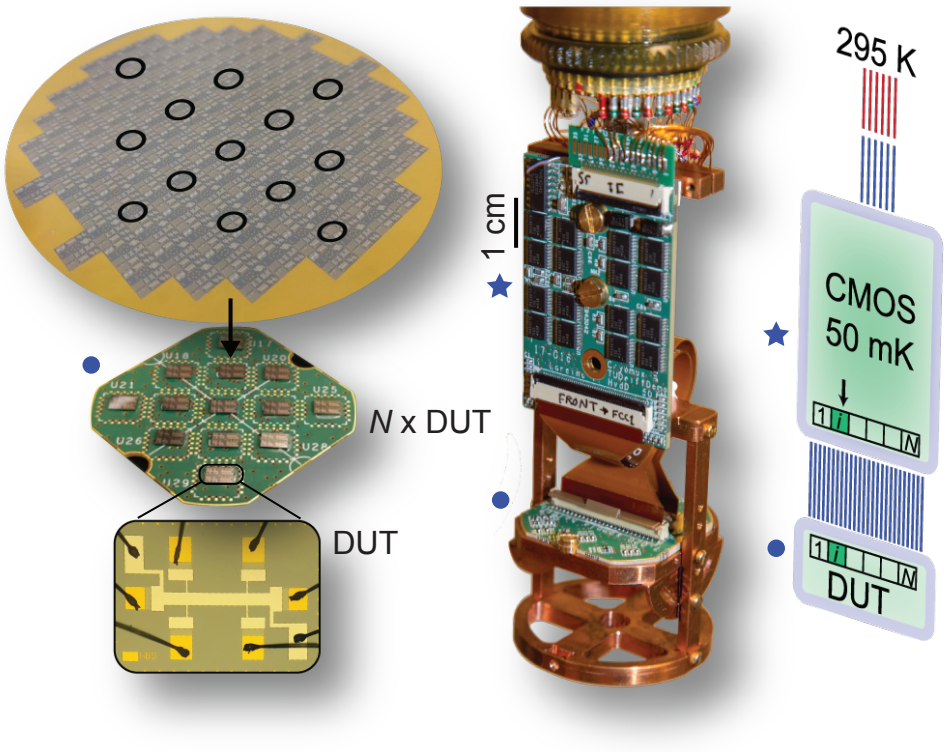


Figure 4.1: **Setup for accelerated cryo-testing of quantum materials and devices.** Left panel: a number $N$ of dies, each containing a device under test (DUT) are selected from a wafer and wire bonded onto a printed circuit board (DUT-PCB; blue circle). Middle panel: the DUT-PCB is mounted to the cold finger of a dilution refrigerator (MCK 50-400 by Leiden Cryogenics) connected by flat ribbon cables to a printed circuit board containing CMOS components (cryo-MUX PCB; blue star). The DUT-PCB and cryo-MUX PCB are operated at $T$ = 50 mK. Right panel: schematics of the cold finger showing how the use of cryo-CMOS allows cold-wires multiplication on the DUT-PCB with a fixed overhead of wires to room temperature. Devices may be selected for single measurements or time division multiplexing

electronics (Fig. 4.2**a**) with the following purpose: i) provide supply voltages and digital logic levels to the board components; ii) connect the multiplexers to current/voltage supplies and equipment for performing measurements of the devices. Each of the DUT has $M$ ($S$) multiplexed (shared) terminals and are bonded to a printed circuit board (DUT-PCB; Fig. 4.2**d**). The DUT-PCB, also operating at 50 mK, is connected to the multiplexers on the cryo-MUX PCB by flat ribbon I/O cables supporting more than $NM+S$ wires.

Table 4.1 presents an overview of the scaling properties of the number of lines between the different parts of the cryogenic architecture in our experimental setup. The system can be scaled by either adding more devices or by adding more lines per device, i.e increasing $N$ or $M$, respectively. When devices are added, additional shift registers are required to select these devices. When the number of lines per device is increased, ad-



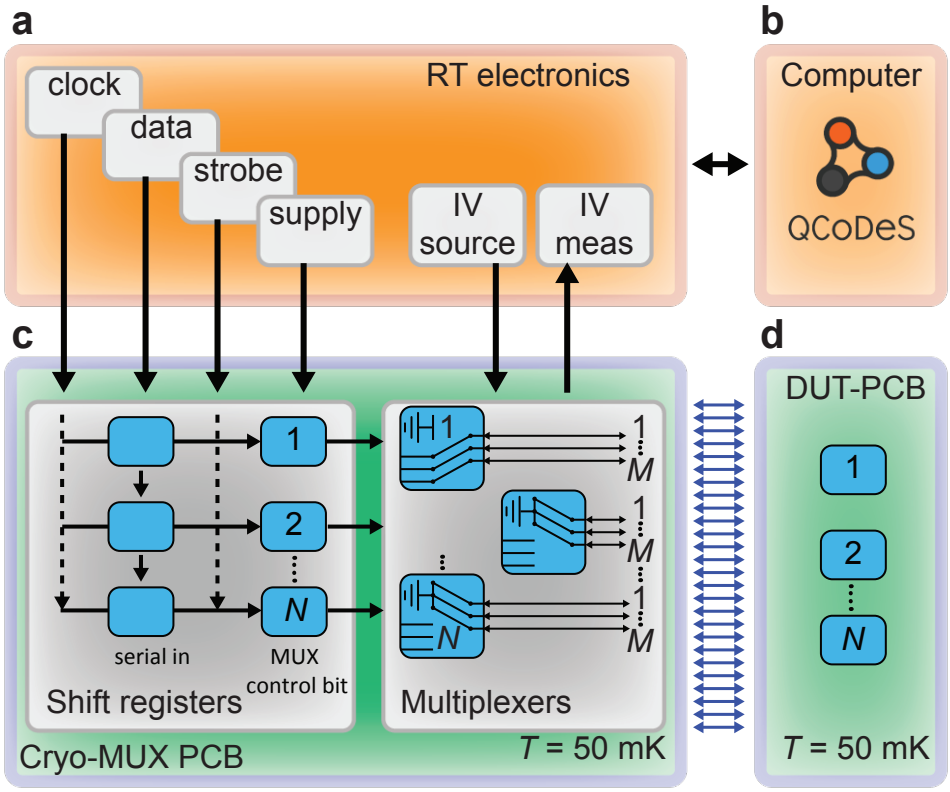


Figure 4.2: **Cryo-multiplexing platform setup.** **a** Electronics operated at room temperature is controlled by a computer **b** using the QCoDeS framework and supplies voltages to the components located on the cryo-MUX PCB **c**. The serial-input parallel-output shift registers receive a string of bits from the room temperature electronics to control the multiplexers. Each bit corresponds to all multiplexers associated with one device under test, located on the DUT-PCB **d**. The multiplexed lines of select devices can be switched either to the supply and measurement equipment or to ground.

| | RT electronics | Shift registers | Mutliplexers | DUT |
|---|---|---|---|---|
| RT electronics | | $C_1$ | M+$C_2$ | S |
| Shift registers | $C_1$ | | N | |
| Mutliplexers | M+$C_2$ | N | | NM |
| DUT | S | | NM | |

Table 4.1: **Number of lines between parts of the cryo-multiplexer platform.** A constant number is indicated with *C*, whereas *N* is the number of DUT and *M* (*S*) is the number of multiplexed (shared) lines per DUT. The first row indicates that the lines between room temperature and cryogenic temperatures are not dependent on *N*. On the other hand, scaling the system will increase the lines between the multiplexers and DUT.



ditional multiplexers and room temperature measurement equipment are needed. Crucially, this protocol requires a constant number of lines between room temperature and cryogenic components, regardless how large *N* is. This approach yields an optimal Rent exponent at room temperature $p_{RT}$=0, however the time necessary to perform a measurement cycle through all DUT scales linearly with *N*.

The whole system is controlled by sending commands to the electronics through a software environment built on QCoDeS [154] (Fig. 4.2**b**), while timing is done using an internal hardware clock for increased precision. Three signals generated from custom digital to analog converters are sent to the SIPO shift registers to perform switching between DUT. All signals are produced by low-noise equipment to avoid any coupling of noise and interference to the multiplexers, since additional line filters were not present due to space constraints in our dilution refrigerator. Firstly, a sequence of data bits is sent that defines which DUT will be selected. Secondly, a clocking signal is sent while loading each bit. Thirdly, a strobe signal is supplied, indicating when the shift register is fully loaded and the outputs can be sent to the multiplexers.

To achieve switching between lines, each line in the DUT is connected to a multiplexer consisting of a CMOS analog integrated circuit configured as a single-pole/double-throw switch. The input terminal of the switch is connected to the DUT, while the output terminals are connected to room temperature equipment and ground. All switches associated with a DUT are controlled through logic inputs connected to the same shift register output. All possible $2^N$ combinations of DUT can be selected since the multiplexers are driven by the parallel output of the shift register.

In all the experiments presented here, the cryo-MUX PCB comprises two cascaded shift registers with eight parallel output each (Texas Instruments 74HC4094; specifications in Ref. [169]), allowing, in principle to measure up to *N*=16 DUT. Each of the *N* parallel outputs of the shift registers control *M*=6 multiplexed lines, separated over two components, each containing three single-pole/double-throw switches (Maxim MAX4619; specifications in Ref. [170]). These components show an on-resistance of 28 Ω and an off-leakage current ≤ 1 fA at $T \leq 80$ mK (see section 4.6.6). The shift registers and multiplexer components are powered with positive and negative supply voltages of 1.1 V and -3.9 V, respectively. The same values define the digital logic levels. In total, the 16 available channels and 6 multiplexed lines result in 96 wires available at the base temperature of the dilution refrigerator. Up to 13 devices are bonded on the DUT-PCB, less than *N*=16

due to the specific die-size chosen for the DUT and the limited sample space. A complete circuit diagram of the cryo-MUX PCB and DUT-PCB is provided in section 4.6.3.

We are able to discriminate whether correct switching has occurred, and consequently whether an intended DUT has been selected, by monitoring the resistance of $N$ control resistors, each connected to one of the $M = 6$ multiplexed lines. We send commands to switch more than $10^3$ times between randomly selected control resistors at a strobe frequency $f_{strobe}$. We then verify that the measured resistance is matching the expected value of the control resistors. We obtain a switching success rate of 100% at $T \leq 80$ mK, while loading the shift register at a clock signal frequency of 4.4 MHz and while switching between resistors at a frequency $f_{strobe} = 1$ KHz, much larger than $f_{strobe} = 8$ Hz used in the experiments reported below. By increasing $f_{strobe}$ to 8 KHz, we observe that the steady temperature of the dilution refrigerator stage has increased to 130 mK, signalling that the power dissipation in the MUX-PCB has exceeded the cooling power of our dilution refrigerator at base temperature (see section 4.6.5).



## 4.3. TIME-DIVISION MULTIPLEXING OF CONTROL RESISTORS

Thirteen metal thin film resistors ($N$=13) are bonded to the DUT-PCB in a four-probe configuration (Fig. 4.3**a**) to validate multiplexed electrical transport under different control sequences and conditions of external parameters, such as source-drain voltage applied to the resistors ($V_{SD}$), magnetic field ($B$), and temperature ($T$). The four-probe setup eliminates the series resistance originating from fridge wiring and electrical contacts and is a test-bed for quantum devices characterization. At room temperature the resistance of the chosen components ranges from 100 Ω to 8.2 kΩ and is expected to be temperature independent, minimizing device unpredictability.

We investigate two measurements protocols. Firstly, the cryo-MUX PCB may act as a simple DUT-selector by keeping a single device connected to the measurement equipment whilst sweeping the relevant parameter. This allows for a traditional single device measurement, with $N$ devices measured one after the other. Alternatively, TDM is achieved by sequentially selecting for measurement all resistors at each point in the parameter sweep, allowing all $N$ measurements to be completed within a single parameter sweep. In addition to benefiting from measurement speedup, this protocol allows for an better comparison between devices since differences in time-dependent factors are minimized.

In Fig. 4.3**b** we compare the dc voltage-current characteristics of the resistors obtained by sweeping the source-drain voltage $V_{SD}$ following the two methodologies (sequential sweeps vs TDM). For all resistors the curves obtained with the two methodologies are matching, with fitted resistance values differing by 0.7% at most, limited by measurement resolution. Having established the validity of the TDM methodology, we further test its applicability to $V_{SD}$, $B$, or $T$ sweeps, to emulate typical quantum transport measurements. For these measurements we use four-terminal low-frequency lock-in techniques by applying constant AC source-drain voltages of 100 $\mu$V. As seen in Fig. 4.3**c**-**e**, the resistance values remain constant for all $N$ devices while sweeping $V_{SD}$, $B$, or $T$. Overall, this characterisation indicates that TDM does not introduce non-linearity in the four terminal measurements and that the whole architecture works properly under

high magnetic fields and different temperature conditions.

## 4.4. MULTIPLEXED QUANTUM TRANSPORT OF INDUSTRIAL SI/SIGE FIELD EFFECT TRANSISTORS

We now harness the power of the multiplexing platform to measure quantum transport of buried-channel semiconductor heterostructures, an archetype material platform for the fabrication of gated semiconductor quantum devices. In Si/SiGe heterostructures a type II band alignment promotes electron confinement at the interface between a strained Si quantum well and a SiGe barrier [8]. Si/SiGe heterostructures fabricated in academic environments have proven a successful material platform for obtaining long-lived high-fidelity electron spin-qubits in silicon [113], and demonstrating strong spin-photon coupling [171, 172]. Furthermore, the advanced level of quantum control in these qubits allows to run quantum algorithms on two qubit processors [173, 168].

By investigating quantum transport in Hall-bar shaped heterostructures field effect transistors (H-FETs) [122, 123, 174], key material metrics such as maximum mobility and percolation density are extracted. Electron mobility is a straightforward figure of merit to asses the overall quality of the 2DEG in the high density regime, where screening of

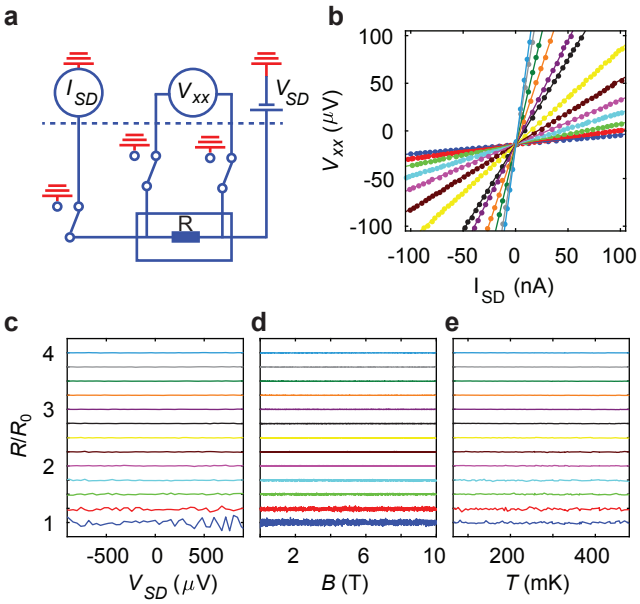


Figure 4.3: **Multiplexed measurements of known resistors. a** Four-probe setup for multiplexed measurements of known resistors. **b** Dc voltage-current characteristics of thirteen resistors measured individually (dots) or all at once (lines) by time division multiplexing. Different colors correspond to different resistors. **c**-**e** Multiplexed resistance measurements while sweeping source-drain voltage ($V_{SD}$), magnetic field ($B$), and temperature ($T$). On the vertical axis, the AC resistance $R = dV_{xx}/dI_{SD}$ is normalized to the resistance value $R_0$ measured at zero dc source-drain voltage, zero magnetic field, and $T = 50$ mK. For clarity, curves are offset by an amount $0.25j$, with $j$ being an integer from 0 (bottom curve) to 12 (top curve).

impurity scattering is relevant [175, 125]. On the other hand, the percolation density indicates the minimum density necessary to establish a metallic conduction channel and is a gauge for disorder at low density, where quantum devices operate.

In this work we take advantage of the cryo-multiplexer platform to reduce the total time required to characterize in detail multiple devices at sub-kelvin temperatures, thereby accelerating the process development for Si/SiGe heterostructures on 300 mm Si substrates in an industrial manufacturing CMOS fab. Si/SiGe H-FETs are fabricated in an academic clean room on 100 mm wafers laser-cut from the original 300 mm Si/SiGe industrial wafer (see details in section 4.6.2).

Ten dies ($N$=10) are randomly selected from different locations of the 100 mm wafer (Fig. 4.4**a**), bonded onto the DUT-PCB, and cooled down to 50 mK for measurements. Fig. 4.4**b** and c show a cross-section of the H-FETs and a schematic of the multiple connecting lines, respectively. Each device has 8 terminals. Five ohmic contacts (O1-O3, O5, O6) are multiplexed, whereas the source contact (O4) and the gate contacts (G1, G2) are shared by all $N$ devices ($M$=5, $S$=3). Using these connections we perform magneto-transport measurements on all DUT by standard low frequency lock-in techniques (see "Methods" section).

Figure 4.4**d** shows the conductivity ($\sigma_{xx}$) and the electron density ($n$) of the devices measured by time division multiplexing as a function of gate voltage (upper and lower panel, respectively) Above a threshold voltage $V_0$, electrons accumulate in the quantum well, current flows in the transistor channel and $\sigma_{xx}$ increases monotonically with $V_0$. Correspondingly, in all devices, the electron density increases linearly as $V_G$ sweeps more positive, consistent with a parallel-plate capacitor model where dielectric between the 2DEG and metallic top-gate comprises the $Si_{0.7}Ge_{0.3}$ barrier and the $Al_2O_3$ layer.

Figure 4.4**e** shows the density-dependent mobility ($\mu$) and conductivity (upper and lower panel respectively). Excluding the purple and red curves, all the other devices follow a similar trend. The mobility increases steeply at small densities ($n \leq 1.4\times10^{11}\,\mathrm{cm}^{-2}$), before slowing down and eventually saturating at higher densities ($n \geq 2\times10^{11}\,\mathrm{cm}^{-2}$). This behaviour is indicative of a high quality Si/SiGe 2DEG. The mobility is limited at low density by scattering from remote charged impurities, likely at the oxide interface, whereas at higher density saturation is given by short-range scattering from impurities within or nearby the quantum well. Remarkably, four devices (black, green, yellow, brown) stand out for exhibiting overlapping mobility density curves over the entire density range, indicating a uniform disorder landscape across the wafer [176]. This is beneficial for future development of large Si qubit arrays with shared control lines [177].

By analyzing the data sets in Fig. 4.4**d**,**e** we perform statistical analysis of key metrics of the 2DEG. Threshold voltage, capacitance ($C$), maximum mobility ($\mu_{max}$), and percolation density ($n_p$) are reported as box plots in Fig. 4.4**f**-**i**. The threshold voltage $V_0$ (Fig. 4.4**f**) is extrapolated from the linear density-gate voltage dependence to zero density, whereas the capacitance (Fig. 4.4**g**) is given by the relationship $C = \frac{dn}{dV_g}e$. We observe small variations in both $V_0$ (2.75%) and $C$ (1.34%) indicating that the dielectric stack comprising a 30-nm-thick $Si_{0.7}Ge_{0.3}$ barrier and the $Al_2O_3$ layer are uniform across the wafer. A record high $\mu_{max}$ (Fig. 4.4**h**) of $4.2\times10^5$ cm$^2$/VS is achieved for these industrially manufactured Si 2DEGs, with an average value of $(3.9\pm 0.6)\times10^5$ cm$^2$/Vs, corresponding to a standard deviation below 20%. Our maximum mobility is less than

the value of 6.5 $\times 10^5$ cm$^2$/Vs obtained previously in Si/SiGe [178] possibly because the dielectric interface in our samples is much closer to the channel (30 nm compared to 50 – 60 nm in Ref. [178]).

As expected from the density-dependent mobility curves, the box plot of $\mu_{max}$ re-

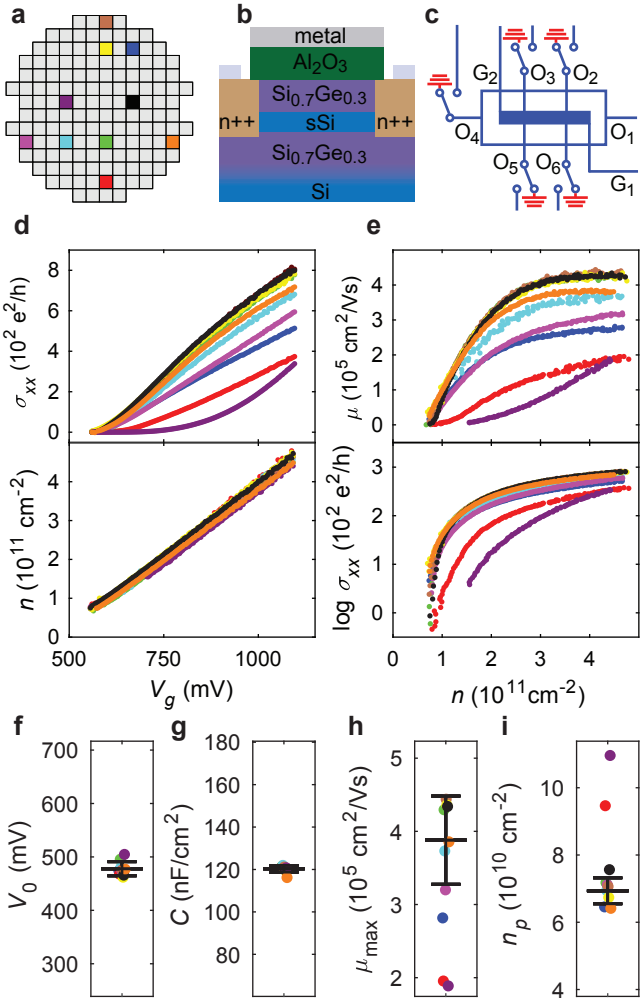


Figure 4.4: **Multiplexed quantum transport in the classical Hall regime at $T$ = 50 mK. a** Dicing scheme of the wafer. Each die and associated measurements throughout the figure have assigned a unique color. **b** Cross-section schematic of the DUT, a Si/SiGe heterostructure field effect transistor and **c** contact schematics. **d** Conductivity $\sigma_{xx}$ (upper panel) and density $n$ (lower panel) as a function of gate voltage $V_g$. **e** Mobility $\mu$ (upper panel) and conductivity $\sigma_{xx}$ (lower panel) as a function of density $n$. Statistical analysis of data-sets in **d** and **e** yield box plots of **f** threshold voltage $V_0$, **g** capacitance $C$, **h** maximum mobility $\mu_{max}$, and **i** percolation density $n_p$ with mean and standard deviation (black crosses). To draw a meaningful comparison between variations in **f-i** the range of each vertical axis is chosen to equal the mean value of the plotted variable. All measurements are taken in a single cooldown.

veals the outliers (purple and red), with values outside of the standard deviation. The percolation density $n_p$ (Fig. 4.4**i**) is obtained by fitting the density-dependent conductivity to a 2D percolation transition model $\sigma_{xx} \sim (n - n_p)^{1.31}$ [125]. We obtain an average $n_p$ of $(6.9 \pm 0.4) \times 10^{10}$ cm$^{-2}$, corresponding to a standard deviation below 6%. The percolation density has a minimum value of $6.4 \times 10^{10}$ cm$^{-2}$, on par with the best values reported in the literature [178, 123]. Overall these results support the use of 300 mm epitaxial Si/SiGe as a promising material platform to manufacture industrial spin qubits.

We now examine magnetotransport at high magnetic field, where quantum effects are dominant. Figure 4.5**a** shows $\rho_{xx}$ and $\rho_{xy}$ of the black device measured either in mul-

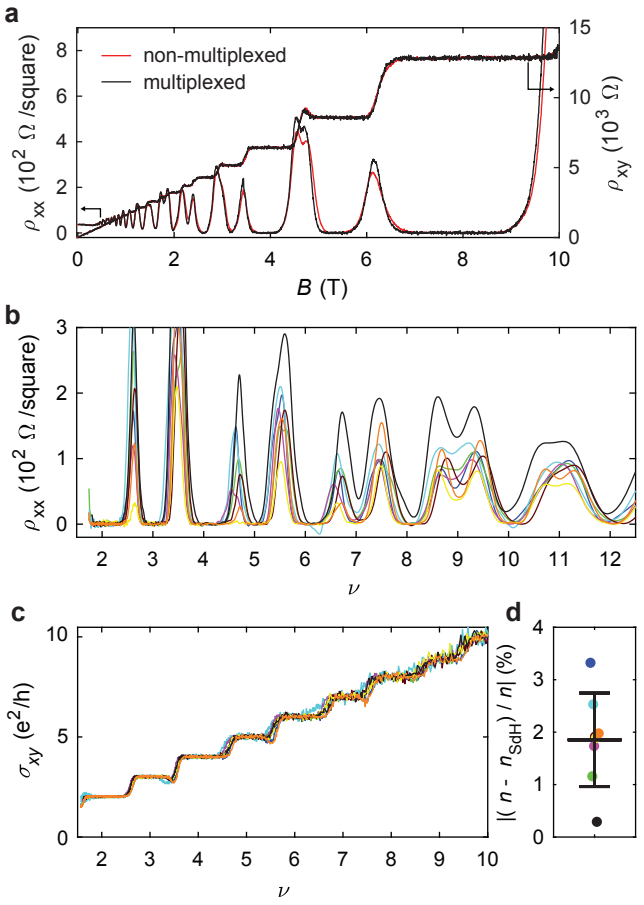


Figure 4.5: **Multiplexed quantum transport in the quantum Hall regime at $T$ = 50 mK. a** Resistivity $\rho_{xx}$ and Hall resistivity $\rho_{xy}$ of a Si/SiGe heterostructure field effect transistor at $T$ 50 mK measured individually (red curves) or by multiplexing (black curves) through all other devices. **b** Multiplexed resistivity $\rho_{xx}$ and **c** Hall conductivity $\sigma_{xy}$ as a function of filling factor $\nu$ for eight devices. Color coding as described in Fig. 4.4**a**. **d** Box plot of the percentage difference between Hall density $n$ and density $n_{SdH}$, with average and standard deviation (cross), extracted by analysis of the Shubnikov de-Haas oscillation periodicity.

tiplexed or non-multiplexed conditions. The overlap between the two curves is excellent, confirming the robustness of the setup against magnetic field sweeps. Clear Shubnikov–de Haas oscillations with zero-resistivity minima are observed in the longitudinal resistance $\rho_{xx}$ as a function of the magnetic field $B$. Correspondingly, flat quantum Hall effect plateaus are visible in $\rho_{xy}$. The oscillations structure is typical of a Si/SiGe structure. The first oscillations at low fields correspond to integer filling factors $\nu = 4k$ due to the spin and valley degeneracy. At higher fields, opening of the Zeeman gap and increased valley splitting leads to lifting of spin and valley degeneracy and observation of the associated even ($\nu = 4k$-2) and odd ($\nu = 2k$-1) filling factors. The QHE plateaus values are quantized as expected at values of $h/e^2\nu$, where $h$ is Planck's constant and $e$ the elementary charge.

Figure 4.5**b** shows the multiplexed $\rho_{xx}$ measurements for all devices. We exclude the purple and red device because analysis of the Shubnikov -de Haas oscillations reveals for these devices the presence of a spurious conduction channel in parallel to the quantum well, possibly due to leakage from the gate. This spurious channel is likely cause of the reduced mobility compared to the other devices at similar density. The measurement are taken at a fixed $V_G$, corresponding to $n \sim 4.3\times10^{11}$ cm$^{-2}$. For clarity, the curves are plotted against filling factor $\nu$. All devices show clearly the spin and valley split levels, however differences in the values of $\rho_{xx}$ are seen, possibly due to the different Landau level broadening and/or different energy splittings across devices. Similar considerations apply to the minor difference observed in quantum Hall measurements reported in Fig. 4.5**c**. As a final statistical analysis, we show in Fig. 4.5**d** a box plot of the percentage difference between Hall density and Shubnikov-de Haas density $n_{SdH}$, obtained by the periodicity of the oscillations as a function of $1/B$. The discrepancy is less than 3%, indicating that population of only one high-mobility subband is achieved uniformly across the wafer.



## 4.5. DISCUSSION

In conclusion, we investigate a cryo-CMOS architecture that uses general-purpose discrete components at 50 mK to increase the number of wires available at cryogenic temperature by an order of magnitude. This is obtained while keeping the overhead number of I/O wires at room temperature fixed. As a proof of principle, we develop and operate a cryo-MUX PCB with 16 selectable channels and 6 multiplexed lines, resulting in 96 wires available at the base temperature of the dilution refrigerator. This solution, implemented in a dilution refrigerator insert with a small sample space, can be further expanded and readily applied to virtually any cryostat.

We show control experiments where we perform time-division multiplexed measurements of known resistors to demonstrate robustness of the setup with respect to applied voltages, magnetic field, and temperature sweeps. We harness the power of the multiplexing architecture to measure quantum transport of numerous Si/SiGe H-FETs in one cooldown, accelerating the development of 300 mm Si/SiGe wafers fabricated in an industrial CMOS fab. We report record values of maximum mobility and percolation density and further improvements of these two metrics are expected by processing the entire gate stack in the high volume manufacturing environment, due to the better semiconductor/oxide interface attainable with an advanced process control. Mul-

tiplexed measurements of Shubnikov de-Haas oscillations and quantum Hall effect are performed successfully. These capabilities provide scope for future high-volume measurements of valley splitting in Si 2DEGs based on thermal activation measurements in the QHE regime [179].

We show a path forward for high-throughput quantum transport at cryogenic temperatures which will help to accelerate the fabrication-measurement cycle of quantum devices in industrial settings. The cryogenic multiplexing demonstrated here may be used already to set the potential landscape of large quantum dot arrays [177, 180, 181]. Moreover, the recent demonstration of universal quantum logic above one kelvin with silicon qubits [182] provides avenue for switching rates exceeding MHz frequencies, thus enabling full control over quantum circuits with only a few room temperature control lines. We envisage that investigations of different components with smaller footprints, circuits, and architectures at cryogenic temperatures [183], including custom fully integrated CMOS solutions, will help to satisfy the ever growing need for scalable wiring solutions to control large quantum systems.

## 4.6. SUPPLEMENTARY INFORMATION

### 4.6.1. GROWTH AND FABRICATION

The Si/SiGe heterostructure comprises a $Si_{0.7}Ge_{0.3}$ strained relaxed buffer obtained by step grading of the germanium content, a 10-nm-thick strained Si quantum well, a 30-nm-thick $Si_{0.7}Ge_{0.3}$ barrier and a 1-nm-thick Si cap. The fabrication process for H-FETs involves: mesa-trench for device isolation; P ion implantation and anneal at $T$ = 750 °C for contacting the 2DEG; atomic layer deposition of a 30-nm-thick $Al_2O_3$ dielectric layer to isolate the 2DEG from the Hall-bar shaped metallic top-gate; metallization for gate, ohmic contacts, and bonding pads.

### 4.6.2. QUANTUM TRANSPORT MEASUREMENTS

We apply a source-drain bias of 0.1 mV and measure $I_{SD}$, the longitudinal voltage $V_{xx}$, and the transverse Hall voltage $V_{xy}$ as a function of gate voltage $V_G$ and $B$. These measurements are carried out by sequential selection or time division multiplexing. As for the control resistance measurements discussed previously, the data-sets obtained with the two methodology agree within less than 1%, indicating that time division multiplexing does not perturb the measurements. The longitudinal resistivity $\rho_{xx}$ and transverse Hall resistivity $\rho_{xy}$ are then calculated. The longitudinal ($\sigma_{xx}$) and transverse ($\sigma_{xy}$) conductivity are obtained via tensor inversion. The Hall electron density $n$ is obtained from the linear dependence $\rho_{xy} = B/en$ at low magnetic fields. The carrier mobility $\mu$ is extracted from the relationship $\sigma_{xx} = ne\mu$, where $e$ is the electron charge.

### 4.6.3. ELECTRICAL CIRCUITS

Figures 4.6 and 4.7 show the schematic circuits of all electrical components used for the cryo-MUX PCB (corresponding to Fig. 4.2**c**). Small labels e.g. "47n" next to a capacitor are representations of 47 nF (e.g. as seen in Fig. 4.6**b**. Red labels with the same name are connected together (e.g. O1_x in Fig. 4.6a is connected to O1_x in Fig. 4.7**a**. Free standing numbers represent the pin connection of an in-/outgoing wire. The ground connection is the same for all components and is connected to a ground at room temperature.

Figure 4.6a shows the connectors that connect wires in the fridge to the cryo-MUX PCB. Connections 1 and 35 on both connectors are grounded to protect from electrostatical discharge (ESD). Connections 22 to 34 on connector 1 are not connected since they are not needed in this configuration. The second connector in Fig. 4.6a has the purpose to attach an additional cryo-MUX PCB for achieving higher yield of measurable samples per thermal cycle.

The cryo-MUX PCB is supplied with $V_{1,2}+$ = +1.1 V and $V_{1,2}-$ = -3.9 V. $V_1\pm$ is used as power supply for the multiplexers and $V_2\pm$ as power supply for the shift registers. In principle these power supplies could be connected together, since we found that both shift registers and multiplexers may share the same supply voltages at $T \leq 80$ mK. Decoupling capacitors C85-C102[1] in Fig. 4.6b and C81-C83[1] in Fig. 4.6c stabilize the power supply, where C85-C102 and C81-C83 combine to a total value of ≈ 37 pF and ≈ 33 pF respectively. Diodes D3[2] (Fig. 4.6**b** and D1[2] (Fig. 4.6**c** are used for reverse bias protec-

[1] Kemet C0805C473J3GACTU and Kemet C0603C153J3GACTU
[2] ON SS16

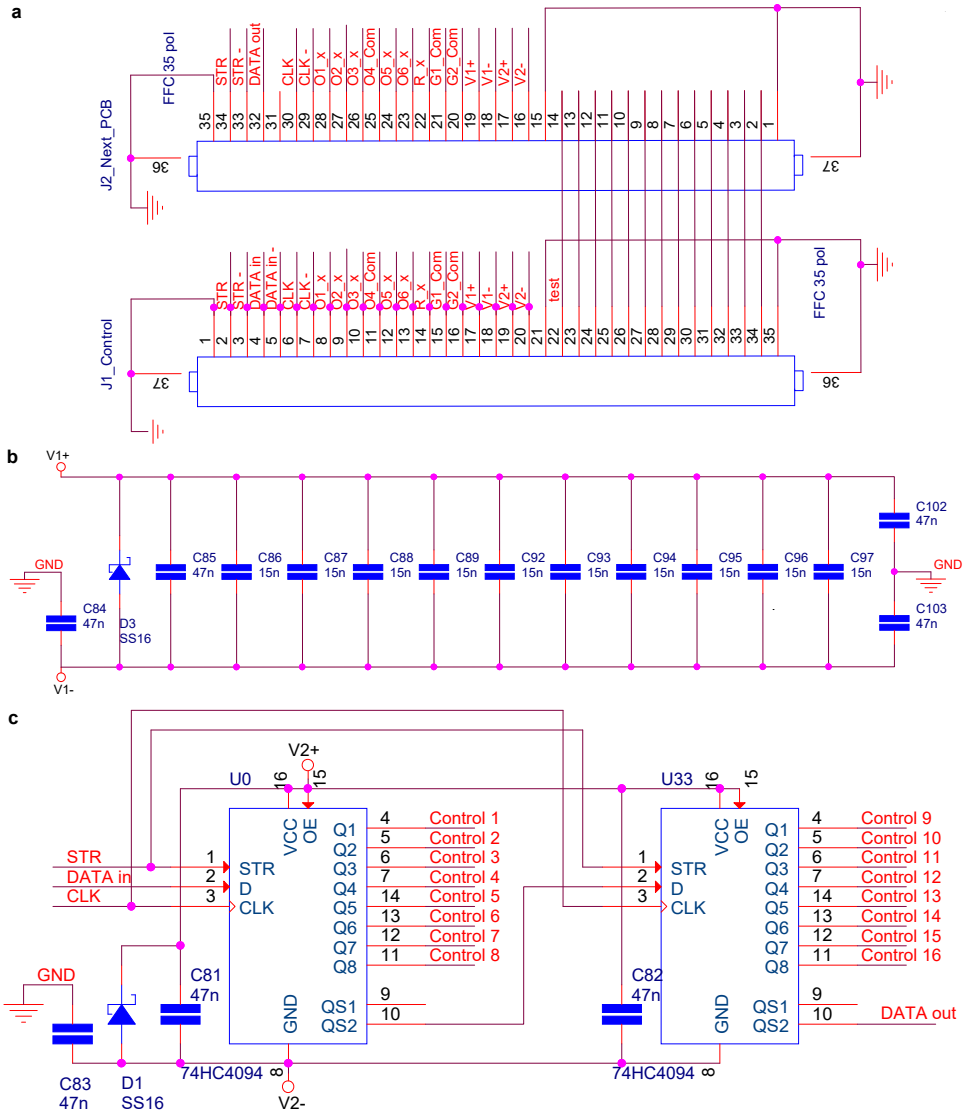


Figure 4.6: Schematics of implementation of **a** connectors from room temperature electronics to the cryo-MUX PCB with ground connections to protect from ESD. **b** a protective diode and a series of decoupling capacitors. **c** shift register with output wires to connect to follow up components.

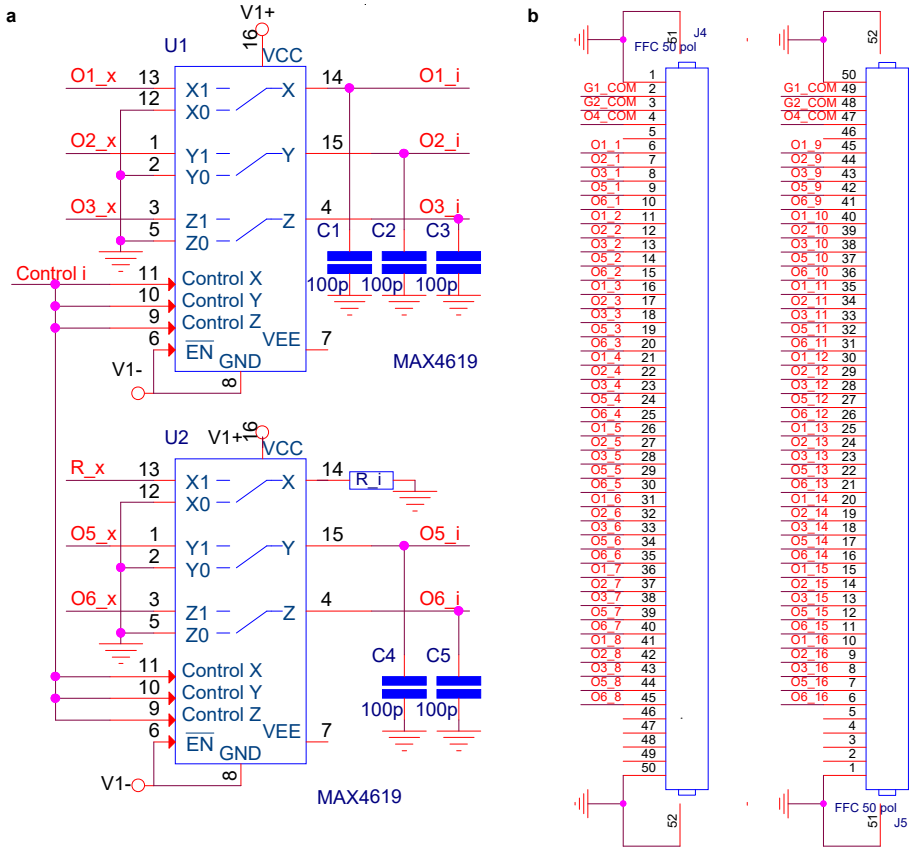


Figure 4.7: Schematics of implementation of **a** the multiplexer components with one control wire i and 6 outgoing wires O1_i, O2_i, O3_i, O5_i, O6_i and R_i. R_i is used to verify correct switching. **b** Connectors hosting outgoing wires from the cryo-MUX PCB with ground connections to protect from ESD.

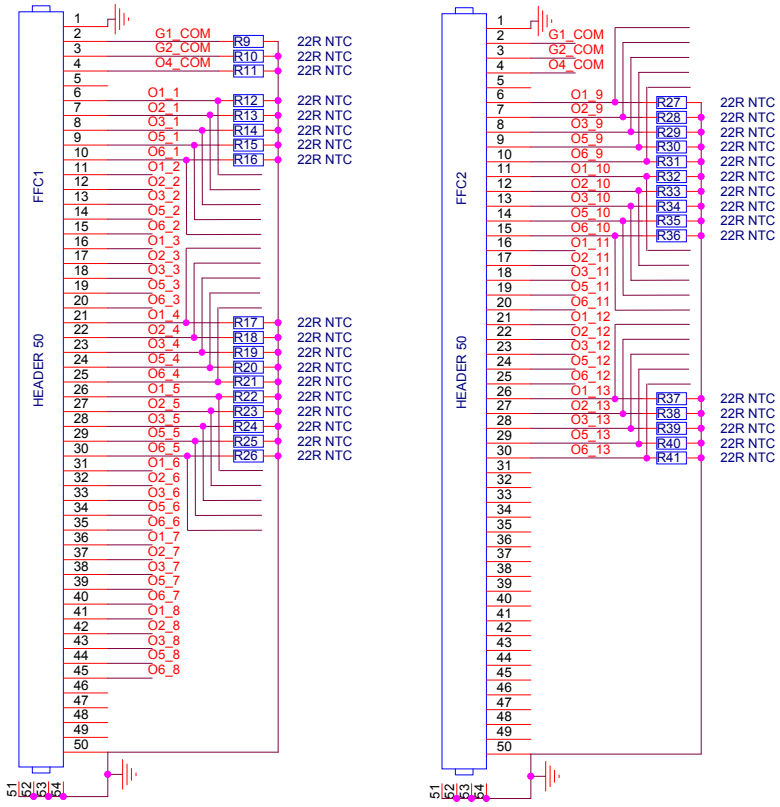


Figure 4.8: Schematics of the connectors on the DUT-PCB with ground connections to protect from ESD and showing all connected wires. Samples 1, 4, 5, 9, 10 and 13 are protected against ESD with NTC resistors.

tion. On the left part of Fig. 4.6c the clock (CLK), data (DATA in) and strobe (STR) wires are connected to the shift register to load data into the registers. Clock and strobe are universal for all shift registers and the output QS2 of shift register 1 is connected to the data input of shift register 2. Additional registers can be cascaded via DATA out on shift register 2.

Each control line (control $i$ 1-16; Fig. 4.6**c** is attached to two sets of three single pole double throw multiplexers (see Fig. 4.7**a**. If a logic low voltage is applied, the multiplexers (i.e. $X$, $Y$ and $Z$) are routed to ground; if a logic high voltage is applied the multiplexers establish a connection between the measurement wires (i.e. O1_i, O2_i, O3_i, O5_i, O6_i and R_i to O1_x, O2_x, O3_x, O5_x, O6_x and R_x). The control lines $X$,$Y$ and $Z$ are connected to the same input signal, enabling all switches ($X$, $Y$, $Z$) at the same time if the control signal is set to logic high. The lines O1_i, O2_i, O3_i, O5_i and O6_i are used to connect to sample $i$. Capacitors of 100 pF [3] reduce the effect of charge injection

[3] Kemet C0402C101J5GACTU

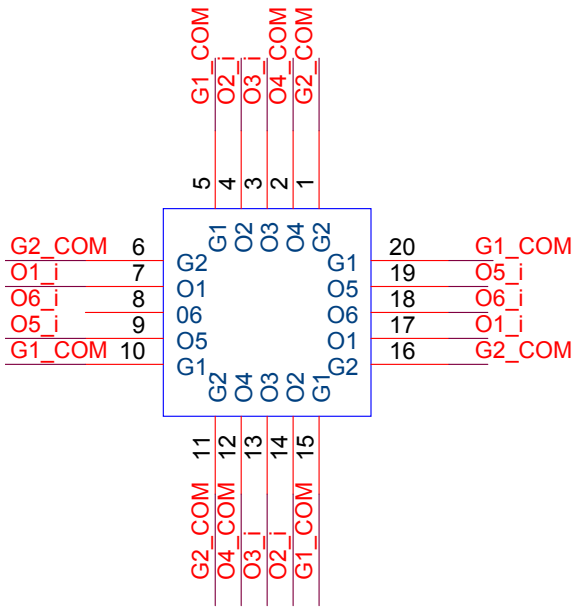


Figure 4.9: Electrical schematic of a cell within the DUT-PCB where an individual DUT is bonded.

from the switches to the samples. $R\_i$ is a unique resistor for each MUX pair (ranging in value from 100 Ω to 8.2 $k\Omega$). Measurements of $R\_i$ confirm if the switching protocol is executed correctly.

Finally, 86 wires in total are routed from the cryo-MUX PCB to the DUT-PCB via connectors (Fig. 4.7**b** with grounding connections present for protection against ESD. In addition, three common lines are connected to pins 2,3 and 4 (connector 1) and pins 47, 48 and 49 (connector 2). These lines do not go through any of the described components. All other lines are attached to the multiplexed outputs described in Fig. 4.7a. Flexible cables connect all outgoing wires of the cryo-MUX PCB to the connectors on the DUT-PCB (see Fig. 4.1).

Figures 4.8 and 4.9 show the components used for the DUT-PCB (corresponding to Fig. 4.2**d**). The DUT-PCB connectors are shown in Fig. 4.8 and are equipped with two ground connections. Wires going to samples 1, 4, 5, 9, 10 and 13 protect the samples against ESD via negative temperature coefficent (NTC) resistors in parallel. NTC resistors have a low resistance at room temperature enabling a path to ground for a current. NTCs have, instead, a high resistance at cryogenic temperature blocking the electrical path to ground and forcing current to go through the DUT.

Finally, Fig. 4.9 shows electrical schematic of a cell within the DUT-PCB where an individual DUT is bonded. Each cell has two complete sets of bond pads to facilitate wire-bonding to the DUT.

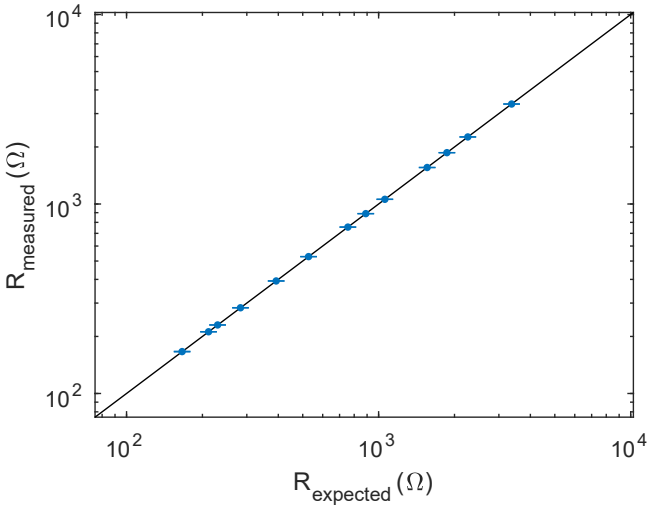


Figure 4.10: Measured resistance compared to expected resistance for determining successful switching. Each measurement is preceded by 3900 random switches, using a clock frequency of 4.4 MHz and strobe frequency of 1 kHz. The line $R_{measured} = R_{expected}$ is added for clarity.

### 4.6.4. SWITCHING SUCCESS RATE

To determine the switching success rate at $T < 80$ mK we adopt the following procedure: load the shift register at a clock rate of 4.4 MHz; switch 3900 times at a strobe frequency $f_{strobe}$ = 1 kHz to a randomly selected control resistor; measure the selected resistor ($R_{measured}$) and compare to the expected result ($R_{expected}$) based on the final switch in the sequence. This procedure is repeated 1000 times. Figure 4.10 shows $R_{measured}$ as a function of $R_{expected}$. The observed linear dependence with unity gradient indicates that 100% switching success rate is achieved.

### 4.6.5. POWER DISSIPATION OF THE CRYO-MUX PCB AND OF A SINGLE MULTIPLEXER

The same experiment is repeated at different strobe frequencies and we always achieve 100% switching success rate. Figure 4.11**a** reports the temperature of the mixing chamber $T_{MC}$ as a function of time to assess power dissipation while switching at different strobe frequencies. At $f_{strobe}$ = 8 kHz (red curve), $T_{MC}$ increases to 130 mK, indicating that power dissipation in the cryo-MUX PCB has exceeded the cooling power of our dilution refrigerator (≤ 400 $\mu$W at 100 mK).

In a separate experiment, we measure the power dissipation while switching a single multiplexer component (MAX4619) to gain further insights into the power dissipation of the circuit. For this purpose, a RIGOL DG4102 arbitrary waveform generator is used to toggle between the high and low logic state of MAX4619. The incoming current and voltage to the power supply are measured with a Keithley 2700 multimeter as a function of toggling frequency. Data points shown in Fig. 4.11**b** are taken at $T \leq 80$ mK and a

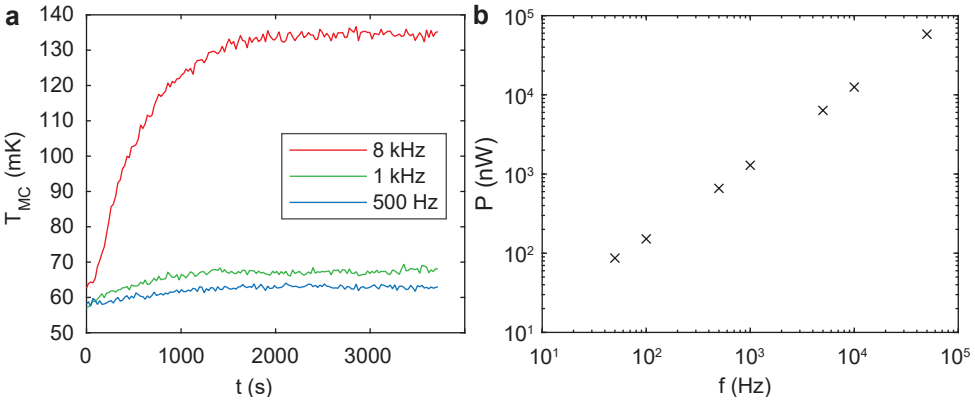


Figure 4.11: **a** Temperature of the mixing chamber $T_{MC}$ over time while switching. Different colors correspond to different strobe frequencies. Switching at 8 kHz overcomes the cooling power of the dilution refrigerator at base temperature. For switching frequencies of 1 kHz and 500 Hz (green and blue curves) heating is limited and $T_{MC}$ is less than 80 mK. **b** Measurements of power vs. frequency to determine the power dissipation for MAX4619.



double logarithmic scale is used for clarity. As expected the power dissipation increases linearly with the switching frequency resulting in a dissipation of 1.165 ± 0.2 nW/Hz. We observe heating of the system ($T_{MC} \geq 80$ mK) for switching frequencies above 1 MHz, with $T_{MC}$ reaching 130 mK at a frequency of 4 MHz.

### 4.6.6. ON-RESISTANCE AND OFF-LEAKAGE CURRENT

Two key specifications of a non-ideal switch are the on-resistance and off-leakage current. We determine the on-resistance by applying a current and measuring both the current and voltage across the multiplexer using lock-in amplifiers. We then subtract the series resistance that arises from the fridge wiring and that was measured previously using a similar setup. We obtain a on-resistance of 28 Ω at $T \leq 80$ mK, above the 10 Ω room temperature maximum reported in the component data sheet.

The off-leakage current affects the current through unselected devices and is an additional undesired current through the disconnected terminal of the selected device. This current is estimated by charging a capacitor connected to the switch and measuring at known time intervals the voltage decrease that occurs while the switch is in the off-state. A schematic of the procedure is shown in Fig. 4.12. First (Fig. 4.12**a**) both capacitors in the circuit are charged. Next (Fig. 4.12**b**), the switch is flipped, disconnecting the cryogenic capacitor $C_c$ from the rest of the circuit. The room temperature capacitor $C_r$ is then discharged (Fig. 4.12**c**) to prevent leakage through the room temperature capacitor. After a known time interval during which charge leaks from capacitor $C_c$, a voltmeter is connected to the circuit (Fig. 4.12**d**), the switch is flipped, and the voltage is measured (Fig. 4.12**e**). The discharge of the room temperature capacitor induces a voltage drop of $V_0 C_r/(C_r + C_c)$, in addition to the voltage drop caused by the leakage through the cryogenic multiplexer. Afterwards, the procedure can be repeated by switching (Fig. 4.12**d**) and grounding (Fig. 4.12**c**) or by recharging the capacitor (Fig. 4.12**a**). A measure-

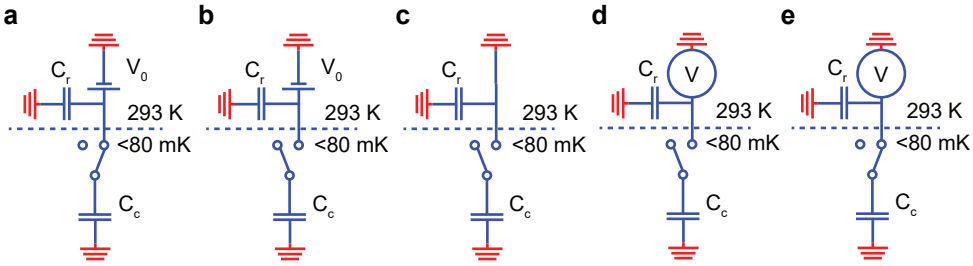


Figure 4.12: The procedure for determining the leakage current. First, the capacitors are charged **a**, then the switch is flipped **b** and the room temperature capacitor is discharged **c**. After waiting, the voltage is measured by connecting a voltage meter **d** and flipping the switch **e**.



ment with minimal waiting time is performed to determine the voltage drop due to the intentional discharge. The N7R capacitors used in the experiment have a room temperature capacitance of $C_r$=1.5 nF and $C_c$= 47 nF. After subtracting the charge drop due to the room temperature discharge, losses of 0.6 mV and 0.1 mV were measured after charging the capacitor to 1V and -1V respectively and waiting for 16 hours. These results correspond to average leakage currents below 1 fA, which is in line with the extrapolation of the off-leakage temperature dependence documented in the data sheet (see Ref. [170]).

# 5

# THE EFFECT OF QUANTUM HALL EDGE STRIPS ON VALLEY SPLITTING IN SI/SIGE HETEROSTRUCTURES

*We determine the splitting of the conduction-band valleys in two-dimensional electrons confined to low-disorder Si quantum wells. We probe the valley splitting dependence on both perpendicular magnetic field $B$ and Hall density by performing activation energy measurements in the quantum Hall regime over a large range of filling factors. The mobility gap of the valley split levels increases linearly with $B$ and is strikingly independent on Hall density. Valley splitting rather depends on the universal incremental changes in density $eB/h$ across quantum Hall edge strips, as our transport model matching the data suggests. With this hindsight, we estimate that valley splitting increases with density at a rate of $116\,\mu eV/10^{11}\ cm^{-2}$, in agreement with previous theories for a near-perfect quantum well top interface.*

This chapter has been published in B. Paquelet Wuetz, M. P. Losert, A. Tosato, M. Lodari, P. L. Bavdaz, L. Stehouwer, P. Amin, J. S. Clarke, S. N. Coppersmith, A. Sammak, M. Veldhorst, M. Friesen, and G. Scappucci, Effect of Quantum Hall Edge Strips on Valley Splitting in Silicon Quantum Wells, Phys. Rev. Lett. **125**, 186801 (2020). [119].

## 5.1. INTRODUCTION

Silicon has proven to be a successful material platform for obtaining high-fidelity electron spin-qubits in quantum dots[184, 113, 185]. The advanced level of quantum control in these qubits makes it possible to execute two-qubit logic gates and rudimentary quantum algorithms[186, 168, 173]. In particular Si/SiGe heterostructures are promising for scalable qubit tiles[181, 177] and the presence of low disorder has already made it possible to define a nine quantum dot array[167]. However, spin qubits in silicon suffer from a two-fold degeneracy of the conduction-band valleys[187, 42, 54], complicating quantum operation. While the valley splitting energy can be large in silicon metal-oxide-semiconductor devices[188], even allowing for qubit operation above one Kelvin[189, 182], atomic-scale disorder in Si/SiGe heterostructures at the Si quantum well top-interface yields a valley splitting energy that is typically modest and poorly controlled, with values ranging from 10 to 200 μeV in quantum dots[168, 134, 190, 191, 192, 193, 194, 195, 196, 197]. While Si/SiGe heterostructures may provide a superior host for scalable qubit arrays due to the low disorder, a key challenge is thus to increase the valley splitting energy for scalable quantum information.



The dependence of valley splitting on quantum confinement yields information about the disorder realization at the critical quantum well top-interface and hence provides tools to improve the Si/SiGe platform. The two-dimensional electron gas (2DEG) is confined laterally over the magnetic length scale $l_B = \sqrt{\hbar e/B}$, where $B$ is the perpendicular magnetic field, which can be precisely controlled. The 2DEG is confined vertically by the quantum well heterostructure, with a confinement energy determined by the vertical electric field $E_z$ (perpendicular to the plane of the 2DEG), which pulls the electrons against the top interface. According to the conventional theory, the valley degeneracy is lifted by the broken translational symmetry of the quantum well barriers, and is therefore proportional to the penetration of the wavefunction into the top barrier. This penetration is proportional to $E_z$ and the two-dimensional electron density [67] $n = \epsilon E_z/e$, which is easily measured in a Hall bar geometry. However, valley splitting in Si/SiGe 2DEGs is usually probed by activation energy measurements in the quantum Hall regime[198, 199, 200, 179]. In this regime, drawing the correct relationship between valley splitting and electric field is challenging since the presence of quantum Hall edge states adds complexity to the electrostatics of the system compared to the simple electrostatics of an infinite 2DEG. Furthermore, the dependence of valley splitting upon both $B$ and $n$ requires activation energy measurements over many filling factors $\nu$ because of the quantum Hall relationship $\nu = hn/eB$. This has challenged experiments so far, since measurements over many filling factors are possible in heterostructure field effect transistors (H-FETs) only if the mobility is high and the critical density for establishing metallic conduction in the channel (percolation density) is low.

In this Letter we overcome this hurdle and we study valley splitting of 2D electrons as a function of both magnetic field and density in Si/SiGe H-FETs. Benefiting from the high mobility and low percolation density achieved in industrially grown heterostructures[155], we resolve Shubnikov–de Haas (SdH) oscillations at small magnetic fields over a large range of densities and we measure activation energies in the quantum Hall regime over an unprecedented range of filling factors. We find that valley splitting increases linearly with magnetic field and is independent of Hall density. Such behavior is

inconsistent with bulk transport models; we therefore present a model in which the valley splitting depends on the incremental changes in density $\Delta n = eB/h$ across quantum Hall edge strips. With this critical new insight, the experimental dependence of valley splitting upon $\Delta n$ is in agreement with previous calculations for a near-ideal Si quantum well top-interface[67].

## 5.2. HIGH QUALITY SI/SIGE HETEROSTRUCTURES

Figure 5.1 shows the basic structural and magnetotransport characterization of the Si/SiGe H-FETs. The heterostructures were grown by reduced-pressure chemical vapor deposition in an industrial manufacturing CMOS fab on top of a 300 mm Si wafer. The layer sequence (Fig. 5.1**a**) comprises a step-graded $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer, an 8 nm strained Si quantum well, a 34 nm $Si_{0.7}Ge_{0.3}$ barrier, and a sacrificial 3 nm Si cap. Hall-bar shaped H-FETs are fabricated with ion implanted ohmic contacts and an $Al_2O_3$/Ti/Pt gate stack. Magnetotransport characterization of the H-FETs is performed over a tem-

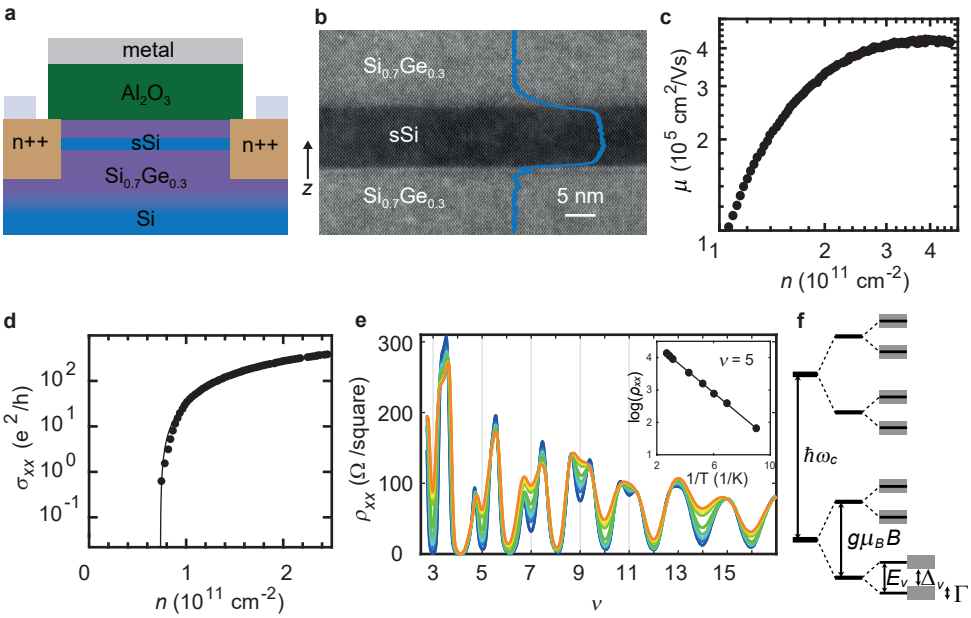


Figure 5.1: **a** Cross-section schematic of a Si/SiGe heterostructure field effect transistor. **b** High angle annular dark field scanning transmission electron (HAADF-STEM) image of the strained Si quantum well and nearby $Si_{0.7}Ge_{0.3}$ with superimposed HAADF-STEM intensity profile (blue line). The heterostructure growth direction $z$ is indicated by a black arrow. **c** Mobility $\mu$ and **d** conductivity $\sigma_{xx}$ as a function of density $n$ at a temperature of 110 mK, measured at the cold finger of the dilution refrigerator. The black line in **d** is a fit to percolation theory. **e** Resistivity $\rho_{xx}$ as a function of filling factor $\nu$ measured at $n = 4.0\times10^{11}\,\mathrm{cm}^{-2}$. Different colors correspond to different temperatures from 110 mK (dark blue) to 450 mK (orange). The inset reports the Arrhenius plot and fit to extract $\Delta_\nu$ for $\nu = 5$. **f** Single particle Landau level energy diagram. Valley split levels correspond to odd integer filling factors $\nu$, Zeeman split levels to $\nu = (4k\text{-}2)$ ($k$ = 1,2,3...), whereas spin and valley degenerate Landau levels correspond to $\nu = 4k$. The shaded areas represent the single-particle level broadening $\Gamma$ due to disorder.

perature range $T$ = 50–500 mK in a dilution refrigerator using standard four-probe low-frequency lock-in techniques. Positive bias applied to the gate induces a 2DEG and controls $n$ in the quantum well (see Ref. [155] for details of the heterostructure growth, device fabrication, and magnetotransport characterization).

Figure 5.1**b** shows a cross-section image of the heterostructure obtained by high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) to highlight the different chemistry in the layers. By fitting the HAADF-STEM intensity profile in Fig. 5.1**b** with an error function[201], we infer that the transition between Si and SiGe at the top interface of the quantum well is characterized by a distance $\lambda \approx 1$ nm[1]. Figure 5.1**c** shows the density-dependent mobility. At high density, the mobility is limited by short-range scattering from impurities within or near the quantum well and reaches a maximum value of $4.2\times10^5$ cm$^2$/Vs at $n = 4.0\times10^{11}$cm$^{-2}$. A low percolation density of $7.3\times10^{10}$cm$^{-2}$ is extracted by fitting the density-dependent conductivity (see Fig. 5.1**d**) to percolation theory[125]. Overall, high mobilities are observed over a wide range of densities, making these H-FETs well suited for quantum Hall measurements over many filling factors.

5

## 5.3. VALLEY SPLITTING AS A FUNCTION OF MAGNETIC FIELD AND DENSITY

Figure 5.1**e** shows typical temperature-dependent measurements of the longitudinal resistivity ($\rho_{xx}$), plotted for clarity against filling factor $\nu$. These measurements are performed at fixed $n$, by keeping the gate voltage constant while sweeping the magnetic field. We observe clear SdH oscillations that are related to the valley splitting $E_v$, the Zeeman splitting $g\mu_B B$, and the cyclotron gap $\hbar\omega_c$ (Fig. 5.1**f**). The inset in Fig. 5.1**e** shows a typical temperature dependence of the SdH oscillation minimum for a valley-split level ($\nu = 5$). We observe a thermally activated dependence $\rho_{xx} \propto \exp(-\Delta_v/2k_BT)$, from which the mobility gap $\Delta_v$ is determined at a specific pair of $B$ and $n$ values satisfying the quantum Hall relationship $\nu = hn/eB$ when $\nu$ is an integer. As indicated in Fig. 5.1**f**, the mobility gap $\Delta_v$ measures the valley splitting $E_v$ reduced by $\Gamma$, the Landau level broadening induced by disorder.

Figure 5.2 shows $\Delta_v$ as a function of $B$ and $n$ on a three-dimensional (3D) plot. The data points in this graph are obtained by repeating temperature dependent $\rho_{xx}$ measurements at different $n$ and by extracting $\Delta_v$ for the odd-numbered filling factors resolved at each iteration. The 3D plot shows that $\Delta_v$ increases linearly with $B$ and—at fixed $B$—is independent of $n$. These observations are quantified by fitting the data in Fig. 5.2 to the plane $\Delta_v = c_B B + c_n n - \Gamma$ with coefficient $c_B = 28.1 \pm 1.2$ μeV/T, $c_n = 0.1 \pm 2.5$ μeV/$10^{11}$cm$^{-2}$, and $\Gamma = 37.5 \pm 10.2$ μeV. Our main experimental result, $E_v(B,n) = c_B B$, follows by considering $c_n$ negligible and correcting for $\Gamma$[2]. Under similar experimental conditions we measure a $g$-factor $\approx 1.8$, close to the expected value of 2[3]. This observation suggests that the measured quantum Hall gaps are not enhanced by electron-

[1] See chapter 5.6.2 for the analysis of the HAADF-STEM intensity profile along the heterostructure growth direction

[2] See chapter 5.6.3 for theoretical justification of this fitting form

[3] See chapter 5.6.3 for $g$-factor analysis

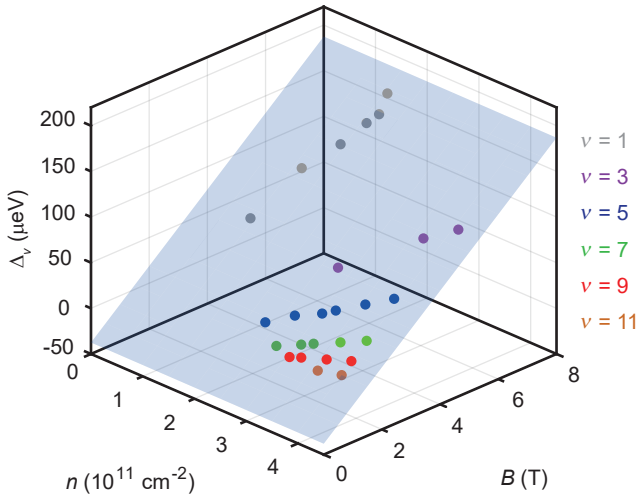


Figure 5.2: Activation energy $\Delta_\nu$ for odd-integer filling factors $\nu$ measured as a function of magnetic field $B$ and Hall density $n$ (filled circles). The blue plane defined by the equation $\Delta_\nu = c_B B + c_n n - \Gamma$ with $c_B = 28.1$ μeV/T, $c_n = 0.1$ μeV/$10^{11}$cm$^{-2}$, and $\Gamma = 37.5$ μeV is a fit to the experimental data points with coefficient of determination $R^2 = 0.993$.



electron interactions[179] and that they represent the single particle valley splitting relevant for silicon qubits.

## 5.4. QUANTUM HALL EDGE STATES AND THEIR EFFECT ON TEMPERATURE ACTIVATED MEASUREMENTS OF VALLEY SPLITTING

The conventional theory of valley splitting in a silicon quantum well predicts that $E_\nu$ depends on the penetration of the electron wavefunction into the quantum well barrier, with $E_\nu \propto E_z$ [67]. If we assume that the 2DEG screens out electric fields from the top gate, then we should find $E_z = 0$ at the bottom of the 2DEG and $E_z = en/\epsilon$ at the top, so that $E_\nu \propto n$, where $n$ is the locally varying electron density in the 2DEG. The proportionality constant is obtained, self-consistently, in Ref. [67]. It is therefore surprising that $E_\nu$ does not appear to depend on $n$ in the Hall data reported in Fig. 5.2.

Previous experiments on quantum Hall devices were unable to separately determine the dependence of valley splitting on $n$ and $B$. In particular, there was no indication of behavior inconsistent with conventional "bulk" behavior. We must therefore modify previous theories of bulk behavior [202] to account for the fact that valley splitting varies systematically across the device. Specifically, we propose that the activation energy is determined near the edges of the 2DEG, giving rise to the observed independence of $E_\nu$ on $n$, as we now explain.

In the quantum Hall regime, the 2DEG forms alternating strips of compressible (blue) and incompressible (pink) liquid [203], as sketched in Fig. 5.3**a**. The density increases by $n_B = eB/h$ in consecutive incompressible strips, where $n_B$ is the quantized density of a

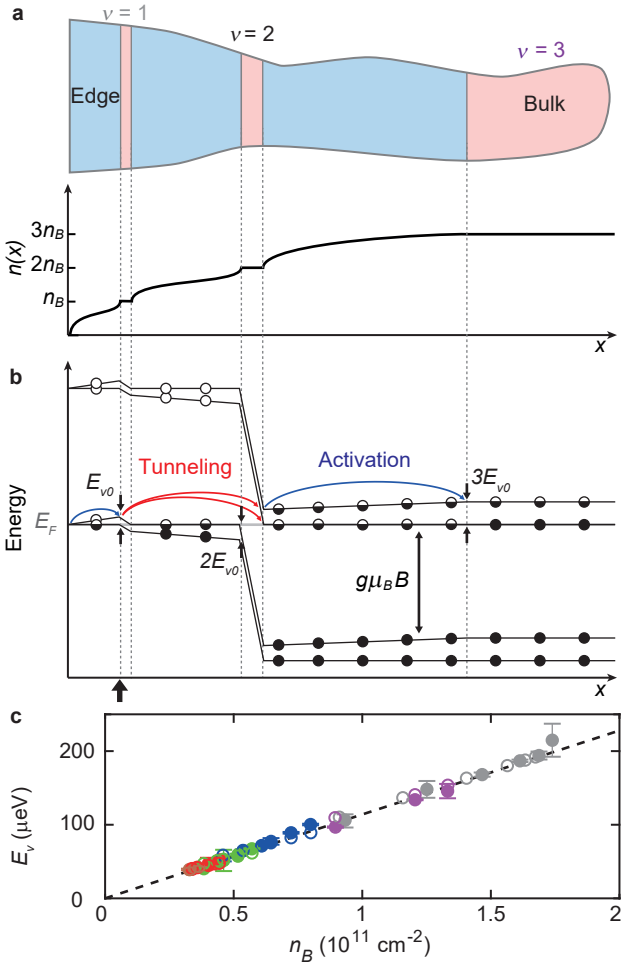


Figure 5.3: **a** Schematic representation of the charge density profile $n(x)$ on the left-hand side of a Hall bar shaped H-FET for the case of $\nu = 3$, in units of the density $n_B = eB/h$ corresponding to one completely filled Landau level. The edge of the Hall bar is at $x = 0$. The 2DEG is divided into compressible (blue) and incompressible (pink) strips. **b** Energy-level diagram, including valley and Zeeman splittings. Landau-level splittings are not present for the case of $\nu_{\text{bulk}} = 3$ shown here, but would occur for larger $\nu_{\text{bulk}}$ values. Valley splittings are assumed to be proportional to the local value of $n$. Filled, partially filled, and empty Landau levels are indicated by filled, half-filled, and empty circles, respectively. Our model of activated transport incorporates activation and tunneling processes across the alternating compressible and incompressible strips. The thick black arrow indicates the location where the valley splitting takes its characteristic value, $E_{\nu 0}$. The valley splitting increases by an amount $E_{\nu 0}$ in each of the compressible strips. **c** Agreement between experimental (filled circles) and simulated (open circles) data points of valley splitting $E_\nu$ as a function of density $n_B = eB/h$. The dashed line is the expected valley splitting dependence on density for a disorder-free quantum well top-interface as calculated in Ref. [67].

filled Landau level, until reaching the bulk value $n = \nu_{\text{bulk}} n_B$, measured by the Hall effect. In the compressible strips, the density varies monotonically between these quantized values, with a charge distribution that screens out electric fields parallel to the plane of the 2DEG. In this way, $n$ varies from zero at the edge of the Hall bar to its bulk value in the center. Figure 5.3**b** is a sketch of the corresponding energy levels, assuming that $E_\nu$ is proportional to the local value of $n$. Note that in the compressible strips and in the bulk, the highest filled levels are pinned at the Fermi level $E_F$ [204].

To observe nonzero longitudinal resistance in our activation energy experiments, electrons must transit across the transverse width of the Hall bar. However, since all the states in the incompressible strip in the center of the Hall bar are filled for integer filling factors, this requires exciting electrons to a state above the Fermi level. Our proposed model incorporates alternating activation and tunneling processes across successive compressible strips.

Each of the activation steps involves climbing "uphill" by an energy $\sim E_{\nu 0}$, which is the change in valley splitting associated with the density change $\Delta n = n_B$. The tunneling process results in the occupation of two valley states, as indicated, since the valley quantum number is not preserved in the presence of atomic-scale roughness at the quantum-well interface[205]. This process leads to conduction across the bulk because the valley-state lifetimes are long, so electrons can travel long distances before decaying. In this model, the characteristic energy $E_{\nu 0}$ is the valley splitting obtained at the position indicated by a thick black arrow in Fig. 5.3**b**.

In Fig. 5.3**c** we demonstrate the consistency of this model with our experimental results and compare our results with previous effective mass theories for valley splitting in Si/SiGe[67]. Here, the experimental results from Fig. 5.2 are reported as solid circles as a function of density $n_B = eB/h$. The data points lie on a single line, irrespective of $\nu$, as expected from the discussion of Fig. 5.2. We also report theoretical results for the valley splitting obtained from Thomas-Fermi simulations of the Hall-bar H-FET (open circles[4]).

In each simulation, we adjust the top-gate voltage to obtain the desired filling factor in the bulk region.The values of $n$ are chosen to match those used in the experiments (see Fig. 5.2). Although magnetic field does not enter the simulations explicitly, its value is determined from $n$ and $\nu$ through the quantization relation $B = hn_{\text{bulk}}/e\nu$. We then evaluate $E_z$ at the location of the thick black arrow in Fig. 5.3**c**. Valley splitting is assumed to be proportional to $E_z$ at the top interface of the quantum well, as described above, and we use a single fitting parameter $\beta = 134.77$ μeV·m/MV to match the simulations with the experimental results, through the relation $E_\nu = \beta E_z$, correcting for the offset of the experimental data at zero electric field due to Γ.

The agreement between the experimental and simulated data points indicates that the proposed activation energy model agrees very well with the experimental measurements of quantum Hall gaps. Additionally, we report in Fig. 5.3**c** as a dashed line the expected value of valley splitting in Si/SiGe according to Eq. 48 of Ref. [67], which is valid for a near-ideal Si quantum well top-interface. Again, the experimental data matches the theoretical expectations. This result suggests that the atomic-scale disorder associated with the diffused SiGe barrier in Fig. 5.1**b** does not significantly suppress valley splitting,

[4] see Supplemental Material of Ref[119] for theoretical methods, which includes Ref. [206]

at least over lateral length scales less than the largest magnetic confinement length for electrons $\sim 4l_B = 70$ nm in our experiments.

## 5.5. DISCUSSION

In summary, we have measured the valley splitting in low-disorder silicon quantum wells over a large range of odd-numbered filling factors in the quantum Hall regime. Supported by a transport model that incorporates the electrostatics of quantum Hall edge states, we demonstrate that valley splitting depends linearly upon the density $eB/h$ rather than on the Hall density. We estimate the ratio $E_v/E_z \sim 135$ μeV·m/MV, which can be compared directly to valley splitting measurements in quantum dots.

## 5.6. SUPPLEMENTARY INFORMATION

### 5.6.1. EXPERIMENTAL METHODS

We apply a source-drain bias of 100 µV and measure $I_{SD}$, the longitudinal voltage $V_{xx}$, and the transverse Hall voltage $V_{xy}$ as a function of gate voltage $V_G$ and $B$. The longitudinal resistivity $\rho_{xx}$ and transverse Hall resistivity $\rho_{xy}$ are then calculated. The longitudinal ($\sigma_{xx}$) and transverse ($\sigma_{xy}$) conductivity are obtained via tensor inversion. The Hall electron density $n$ is obtained from the linear dependence $\rho_{xy} = B/en$ at low magnetic fields. The carrier mobility $\mu$ is extracted from the relationship $\sigma_{xx} = ne\mu$, where $e$ is the electron charge.

### 5.6.2. ANALYSIS OF HIGH-ANGLE ANNULAR DARK FIELD SCANNING TRANSMISSION ELECTRON MICROSCOPY INTENSITY PROFILE

In Fig. 5.4**a** we show the intensity profile from high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) along $z$, the heterostructure growth direction, and a theoretical fit to the function $erf(\frac{z-z_0}{\sqrt{2}\lambda})$. Erf is the error function, $z_0$ is the center of the quantum well top-interface, where the HAADF-STEM intensity signal is midway in between the value measured at the quantum well and at the SiGe barrier, and $\lambda$ is the characteristic distance. The HAADF-STEM intensity signal is shown after a linear background subtraction and normalization to the value measured in the quantum well. We extract $\lambda = 1.04 \pm 0.03$ nm from the fit.



### 5.6.3. G-FACTOR ANALYSIS

We determine the $g$-factor from the thermally activated dependence of the Shubnikov de Haas (SdH) oscillation minimum for spin split levels[179]. Figure 5.4**b** shows the mobility gaps for Zeeman spin split levels ($\Delta_Z$, blue circles) and valley split levels ($\Delta_v$, red cirles) as a function of magnetic field. Similarly to the procedure described in the main text, these data points are obtained by fitting the temperature dependent magnetoresistance oscillation minima in the density range of (0.9–4) $\times 10^{11}$ cm$^{-2}$ to an Arrhenius law $\rho_{xx} \propto \exp(-\Delta_Z/2k_BT)$ and $\rho_{xx} \propto \exp(-\Delta_v/2k_BT)$ for spin and valley states, respectively. Both $\Delta_Z$ and $\Delta_v$ increase linearly with magnetic field. Taking into account the reduction of the Zeeman energy gap $g\mu_B B$ due to valley splitting $E_v = c_B B$ and Landau level broadening $\Gamma$ (see inset in Fig. 5.4**b**), the linear increase of $\Delta_Z$ and $\Delta_v$ with magnetic field is described by the following two equations:

$$\Delta_Z = g\mu_B B - c_B B - \Gamma \tag{5.1}$$

$$\Delta_v = c_B B - \Gamma \tag{5.2}$$

We fit the experimental points $\Delta_Z$ and $\Delta_v$ in Fig.5.4**b** to Eq 5.1. and 5.2. using $g$, $c_B$ and $\Gamma$ as fitting parameters. We extract: $g = 1.8 \pm 0.05$, $c_B = 27.5 \pm 0.9$ µeV/T and $\Gamma = 35.3 \pm 3.3$ µeV. The obtained values of $c_B$ and $\Gamma$ are compatible with the analysis in the main text. The solid lines in Fig 5.4**b** correspond to the Zeeman energy $g^*\mu_B B$ and valley splitting energy $E_v = c_B B$, taking into account $\Gamma$. The $g$-factor $\approx 1.8$ is close and not greater than the single particle value $g = 2$, suggesting that the measured quantum

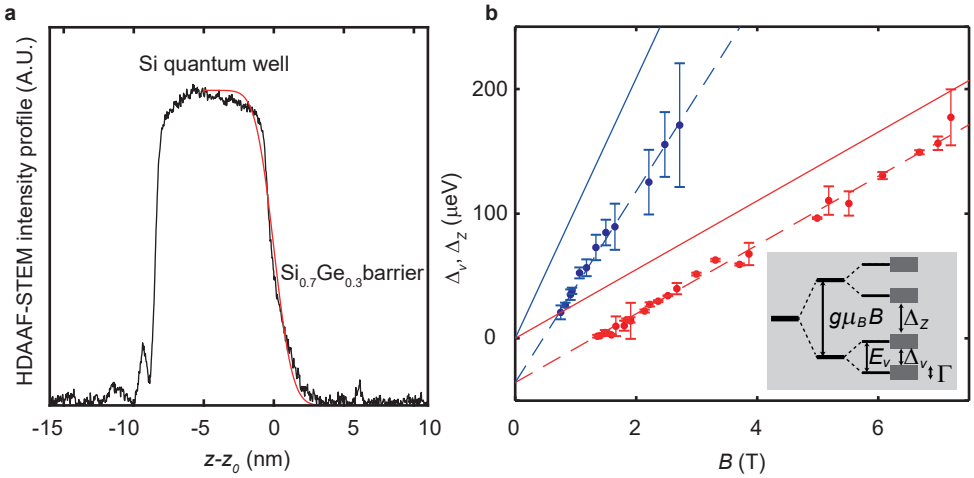


Figure 5.4: **a** HAADF-STEM intensity profile (black line) along the $z$, the heterostructure growth direction. The red line is a theoretical fit of the data in the region corresponding to the top interface between the Si quantum well and the SiGe barrier (see text for details). For clarity, the horizontal axis is offset by $z_0$, the coordinate of the center of the quantum well top interface. **b** Mobility gaps obtained from thermal activation of Shubnkiov de Haas oscillation minima for $2n$ - 1 fillings factors ($\Delta_v$, red circles) and $4n$ - 2 filling factors ($\Delta_Z$, blue circles), corresponding to valley and Zeeman split levels, respectively. The blue and red dashed lines are theoretical fits to the experimental data using equations (5.1) and (5.2), respectively. The blue and red solid lines correspond to the estimated Zeeman and valley energy gaps, respectively. The inset shows splitting of a Landau level due to Zeeman spin splitting and valley splitting. Shaded areas represent the single-particle level broadening $\Gamma$ due to disorder.

Hall gaps in the main text are not enhanced by electron-electron interaction and thus represent single-particle energy gaps.

### 5.6.4. RESIDUALS FOR THE PLANAR FIT OF $\Delta_v$ AS A FUNCTION OF MAGNETIC FIELD AND HALL DENSITY

In Fig. 5.5 we show the residuals to highlight the agreement between experimental data points and theoretical fit in Fig. 2 of the main text. For clarity, the residuals are plotted against magnetic field $B$ (Fig. 5.5**a**), Hall density (Fig. 5.5**b**), and activation energy $\Delta_v$ (Fig. 5.5**c**). Overall we observe small residuals with random distributions around zero, indicating a good fit.

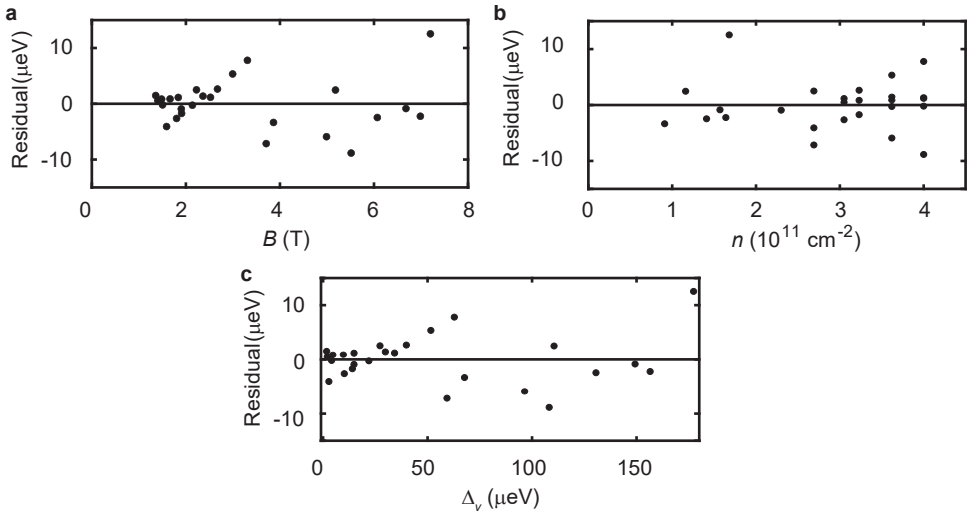


Figure 5.5: Residual plot of the activation energy $\Delta_\nu$ reported in Fig. 2 to the plane defined by the equation $\Delta_\nu = c_B B + c_n n - \Gamma$ with $c_B = 28.1$ μeV/T, $c_n = 0.1$ μeV/$10^{11}$cm$^{-2}$, and $\Gamma = 37.5$ μeV. Residuals are plotted as a function of **a** magnetic field $B$, **b** Hall density $n$, **c** activation energy $\Delta_\nu$.

# 6

# ATOMIC FLUCTUATIONS LIFTING THE ENERGY DEGENERACY IN SI/SIGE QUANTUM DOTS

*Electron spins in Si/SiGe quantum wells suffer from nearly degenerate conduction band valleys, which compete with the spin degree of freedom in the formation of qubits. Despite attempts to enhance the valley energy splitting deterministically, by engineering a sharp interface, valley splitting fluctuations remain a serious problem for qubit uniformity, needed to scale up to large quantum processors. Here, we elucidate and predict the valley splitting by the holistic integration of 3D atomic-level properties, theory and transport. We find that the concentration fluctuations of Si and Ge atoms within the 3D landscape of Si/SiGe interfaces can explain the observed large spread of valley splitting from measurements on many quantum dot devices. Against the prevailing belief, we propose to boost these random alloy composition fluctuations by incorporating Ge atoms in the Si quantum well to statistically enhance valley splitting.*

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*These authors have contributed equally

## 6.1. INTRODUCTION

Advanced semiconductor manufacturing is capable of integrating billions of transistors onto a single silicon chip. The promise of leveraging the same technology for large-scale integration of qubits into a fault-tolerant quantum processing unit is a key driver for developing electron spin qubits in silicon quantum dots[207]. Although these devices bear many similarities to transistors[208], qubits operate in the single electron regime[41], making them more sensitive to electrostatic disorder and noise arising from the surrounding environment. In strained silicon quantum wells, the electronically active part of the device is separated by an epitaxial SiGe barrier from the electronically noisy interface at the gate-stack, offering a quiet system with high mobility and low leakage between the gate and the quantum dots[209]. These properties make strained Si/SiGe heterostructures promising for scalable qubit tiles[181, 177] and have made it possible to define nine quantum dot arrays[167], run quantum algorithms[168] and entangle three-spin states[210] in natural silicon structures, and achieve two-qubit gate fidelity above 99%[115, 114] in isotopically purified silicon structures.

However, spin-qubits in silicon suffer from a two-fold degeneracy of the conduction band minima (valleys) that creates several non-computational states that act as leakage channels for quantum information[42]. These leakage channels increase exponentially with the qubit count[211], complicating qubit operation and inducing errors during spin transfers. Despite attempts to enhance the valley energy splitting, the resulting valley splittings are modest in Si/SiGe heterostructures, with typical values in the range of 20 to 100 μeV [168, 191, 192, 193, 194, 178, 196, 172] and only in a few instances in the range of 100 to 300 μeV [134, 190, 212]. Such variability in realistic silicon quantum dots remains an open challenge for scaling to large qubit systems. In particular, the probability of thermally occupying the excited valley state presents a challenge for spin initialization, and, in some cases, intervalley scattering may limit the spin coherence[213]. Furthermore, small valley splitting may affect Pauli spin blockade readout[66], which is considered in large-scale quantum computing proposals[181, 177]. Therefore, scaling up to larger systems of single-electron spin qubits requires that the valley splitting of all qubits in the system should be much larger than the typical operation temperatures (20 – 100 mK).

It has been known for some time that valley splitting depends sensitively on the interface between the quantum well and the SiGe barrier[67]. Past theoretical studies have considered disorder arising from the quantum well miscut angle[77] and steps in the interface[75, 70, 205, 214, 215] demonstrating that disorder of this kind can greatly decrease valley splitting in quantum dots. However, a definitive connection to experiments has proven challenging for a number of reasons. At the device level, a systematic characterization of valley splitting in Si/SiGe quantum dots has been limited because of poor device yield associated with heterostructure quality and/or device processing. At the materials level, atomic-scale disorder in buried interfaces[216] may be revealed by atom-probe tomography (APT) in three-dimensions (3D) over the nanoscale dimensions comparable to electrically defined quantum dots. However, the current models employed to reconstruct in 3D the APT data can be fraught with large uncertainties due to the assumptions made to generate the three-dimensional representation of the tomographic data[217]. This results in limited accuracy when mapping heterointerfaces[218]

and quantum wells[219, 220, 74]. These limitations prevent linking the valley splitting in quantum dots to the relevant atomic-scale material properties and hinder the development of accurate and predictive theoretical models.

Herein we solve this outstanding challenge and establish comprehensive insights into the atomic-level origin of valley splitting in realistic silicon quantum dots. Firstly, we measure valley splitting systematically across many quantum dots, enabled by high-quality heterostructures with a low disorder potential landscape and by improved fabrication processes. Secondly, we establish a new method to analyse APT data leading to accurate 3D evaluation of the atomic-level properties of the Si/SiGe buried interfaces. Thirdly, incorporating the 3D atomic-level details obtained from APT, we simulate valley splitting distributions that consider the role of random fluctuations in the concentration of Si and Ge atoms at each layer of the Si/SiGe interfaces. By comparing theory with experiments, we find that the measured random distribution of Si and Ge atoms at the Si/SiGe interface is enough to account for the measured valley splitting spread in real quantum dots. Based on these atomistic insights, we conclude by proposing a practical strategy to statistically enhance valley splitting above a specified threshold as a route to making spin-qubit quantum processors more reliable — and consequently — more scalable.

## 6.2. STATISTICAL GROUND STATE SPLITTING MEASUREMENTS IN QUANTUM DOTS



Figure 6.1 overviews the material stack, quantum dot devices, and measurements of valley splitting. To increase statistics, we consider two isotopically purified $^{28}Si/Si_{0.7}Ge_{0.3}$ heterostructures (quantum wells A and B) designed with the same quantum well width and top-interface sharpness (see section 6.6.1), which are important parameters determining valley splitting[67, 212]. As shown in high angle annular dark field scanning transmission electron microscopy (HAADF-STEM), quantum well A (Fig. 6.1**a**) has a sharp $^{28}Si \rightarrow$ Si-Ge heterointerface at the top and a diffused Si-Ge $\rightarrow$ $^{28}Si$ heterointerface at the bottom, whereas in quantum well B (Fig. 6.1**b**) the growth process was optimized to achieve sharp interfaces at both ends of the quantum well. These heterostructures support a two-dimensional electron gas with high mobility and low percolation density (Figs. 6.5 and 6.6), indicating a low dissorder potential landscape, and high-performance qubits[51, 115] with single- and two-qubit gates fidelity above 99%[115].

We define double-quantum dots electrostatically using gate layers insulated by dielectrics (see section 6.6.4). A positive gate voltage applied to plunger gates P1 and P2 (Fig. 6.1**c**) accumulates electrons in the buried quantum well, while a negative bias applied to other gates tunes the confinement and the tunnel coupling between the quantum dots Q1 and Q2. All quantum dots in this work have plunger gate diameters in the range of 40-50 nm (Fig. 6.1**d** and Supplementary Table 6.1), setting the relevant lateral length scale for atomic-scale disorder probed by the electron wave function.

We perform magnetospectroscopy measurements of valley splitting $E_v$ in dilution refrigerators with electron temperatures of about 100 mK (see section see section 6.6.4). Figure 6.1**e** shows a typical charge stability diagram of a double quantum dot with DC gate voltages tuned to achieve the few electron regime, highlighted in Fig. 6.1**f**. We deter-

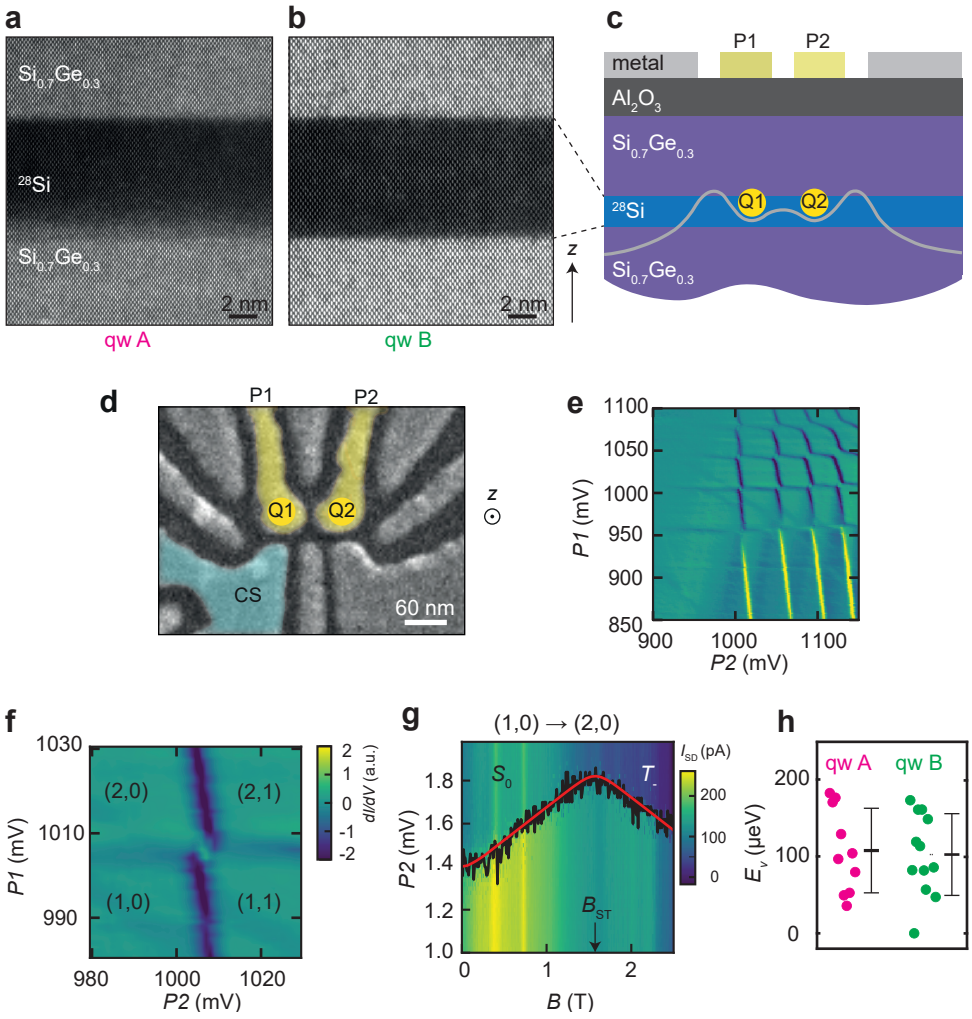


Figure 6.1: **Material stack, devices, and valley splitting measurements a,b** High-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) of $^{28}$Si/SiGe quantum wells A and B, respectively. **c,d** Schematic cross-section of a heterostructure with gate layout and false-coloured scanning electron microscope image of a double quantum dot, respectively. Q1 and Q2 are the quantum dots defined through confinement potentials (schematic, grey line) formed below plunger gates P1 and P2. CS is a nearby quantum dot used as a charge sensor. **e** Typical stability diagram of a double quantum dot formed by plunger gates P1 and P2 and measured by a nearby charge sensor (CS in **d**). **f** Close-up of the stability diagram in the few-electron regime. **g** Typical magnetospectroscopy of the (1,0)→(2,0) transition, used to measure singlet-triplet splittings. An offset of 1082 mV is subtracted for clarity from the gate voltage applied to P2. Black lines show the location of the maximum of the differentiated charge-sensor signal ($dI_{SD}/dP2$) of the electron charging transition. Red lines show a fit to the data, from which we extract the kink position $B_{ST}$. The valley splitting $E_v$ is given by $g\mu_B B_{ST}$, where $g = 2$ is the gyromagnetic ratio and $\mu_B$ is the Bohr magneton. **h** Experimental scatter plots of the valley splittings for quantum wells A (magenta) and B (green), with thick and thin horizontal black lines denoting the mean and two-sigma error bars.

mine the 2-electron singlet-triplet energy splitting ($E_{ST}$) by measuring the gate-voltage dependence as a function of parallel magnetic field $B$ along the (0,1) → (0,2) transition (Fig. 6.1**g**) and along the (1,1) → (0,2) transition (Supplementary Fig. 6.8). In Fig. 6.1**g**, the transition line (black line) slopes upward, because a spin ↑ electron is added to form a singlet ground state $S_0$. Alternatively, a spin down electron can be added to form a $T_-$-state, with a downward slope. A kink occurs when the $S_0$-state is energetically degenerate with the $T_-$-state, becoming the new ground state of the two-electron-system. From the position of the kink ($B_{ST}$ = 1.57 T) along the theoretical fit (red line) and the relation $E_{ST} = g\mu_B B_{ST}$, where $g = 2$ is the electron gyromagnetic ratio and $\mu_B$ is the Bohr magneton, we determine $E_{ST}$ = 182.3 μeV for this quantum dot. $E_{ST}$ sets a lower bound on the valley splitting, $E_v \geq E_{ST}$[134, 135]. Due to small size, our dots are strongly confined with orbital energy much larger than $E_{ST}$ (Supplementary Fig. 6.7), similar to other Si/SiGe quantum dots[191, 178, 190]. Therefore, we expect exchange corrections to have negligible effects[135] and here take $E_v \approx E_{ST}$.

Here we report measurements of $E_v$ in 10 quantum dots in quantum well A and 12 quantum dots in quantum well B (Figures. 6.9-6.12) and compare the measured values in Fig. 6.1**h**. We observe a rather large spread in valley splittings, however we obtain remarkably similar mean values and two-standard-deviation error bars $\overline{E_v} \pm 2\sigma$ of 108 ± 55 μeV and 106±58 μeV for quantum wells A and B, respectively[1]. We argue that quantum wells A and B have similar $\overline{E_v} \pm 2\sigma$ because the electronic ground state is confined against the top interface, which is very similar in the two quantum wells.



## 6.3. ATOM PROBE TOMOGRAPHY

We now characterize the atomic-scale concentration fluctuations at the quantum well interfaces to explain the wide range of measured valley splittings with informed theoretical and statistical models. To probe the concentrations over the dimensions relevant for quantum dots across the wafer, we perform APT on five samples each from quantum wells A and B, with a field of view of approximately 50 nm at the location of the quantum well (see section 6.6.2). First, we show how to reliably reconstruct the buried quantum well interfaces, then we use this methodology to characterise their broadening and roughness.

Figure 6.2**a** shows a typical point-cloud reconstruction of an APT specimen from quantum well B. Each point represents the estimated position of an ionized atom detected during the experiment[217]. Qualitatively, we observe an isotopically enriched $^{28}$Si quantum well, essentially free of $^{29}$Si, cladded in a SiGe alloy. To probe the interface properties with the highest possible resolution allowed by APT and differently from previous APT studies on Si/SiGe[74], we represent the atom positions in the acquired data sets in form of a Voronoi tessellation[221, 222] and generate profiles on an $x-y$ grid of the tessellated data, as described in Supplementary Discussion Section 6.7.2**C**. A sigmoid function $[1+\exp(z-z_0)/\tau]^{-1}$[74] is used to fit the profiles of each tile in the $x-y$ grid. Here, $z_0$ is the inflection point of the interface and $4\tau$ is the interface width. As the Voronoi tessellation of the data set does not sacrifice any spatial information, the

[1] The quantum dots all have a similar design and hence are expected to have similar electric fields across the devices with a small influence on valley splitting under our experimental conditions

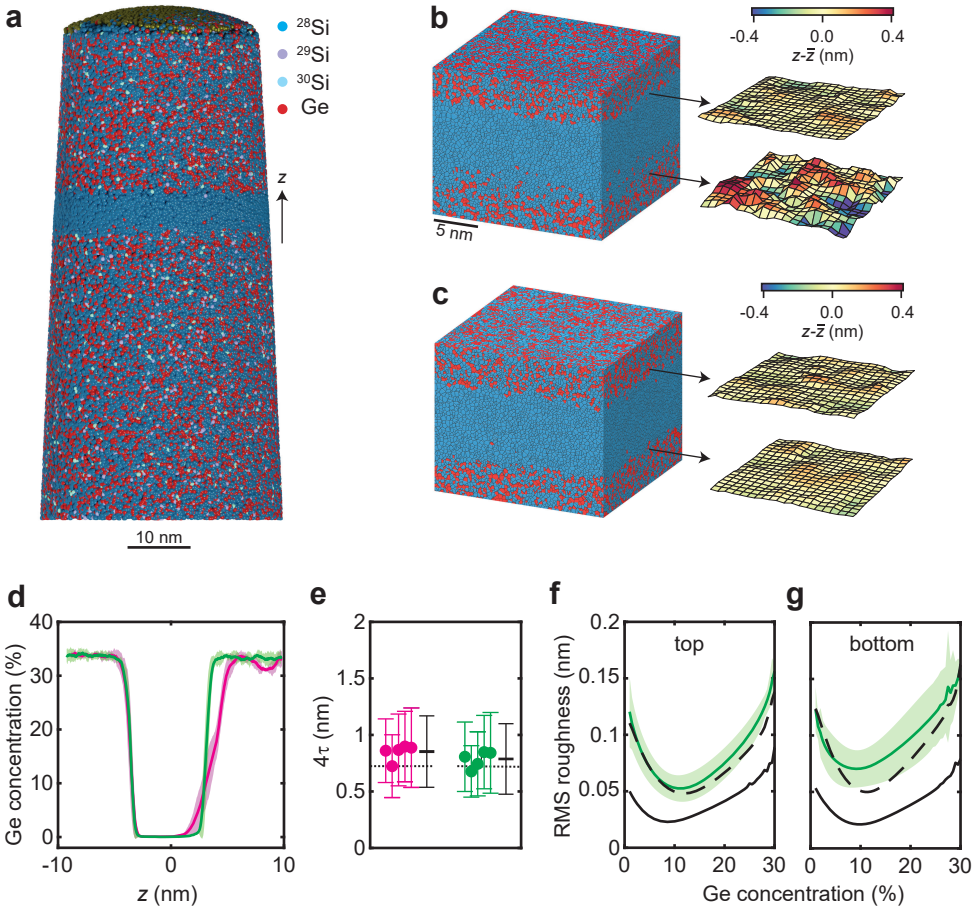


Figure 6.2: **Atom probe tomography of $^{28}$Si/SiGe heterostructures. a** Point-cloud APT reconstruction of quantum well B, showing the $^{28}$Si quantum well and surrounding SiGe barriers. Isotopic purification is confirmed by secondary ion mass spectroscopy (Supplementary Fig. 6.20). **b**, **c** Voronoi tessellation of the APT reconstructions for quantum wells A and B, respectively, and extracted isosurfaces corresponding to 8% Ge concentration. $\bar{z}$ is the average position of the 8% Ge concentration across these particular samples. We limit the lateral size of the analysis to $\approx 30$ nm $\times$ 30 nm, reflecting the typical lateral size of a quantum dot (Fig. 6.1**d**). **d** Average germanium concentration depth profiles across quantum wells A (magenta) and B (green). Shaded areas mark the 95% confidence interval over each of the sets of five APT samples. **e** Statistical analysis of the top interface width $4\tau$ determined by fitting the data for quantum wells A (magenta) and B (green) to sigmoid functions. Thick and thin horizontal black lines denote the mean and two-standard-deviation error bars for the different APT samples. Dotted black lines show $4\tau$ results from the HAADF-STEM measurements (Supplementary Fig 6.19). **f**,**g** Root mean square (RMS) roughness of the concentration isosurfaces as a function of germanium concentration at the top and bottom interfaces of quantum well B (green line). Shaded areas indicate the 95% confidence interval, averaged over each set of five APT samples. The experimental data are compared to the RMS roughness of a simulated quantum well with the interface properties of **d** (dashed black line) vs. an atomically sharp quantum well (solid black line).

tiling in the $x-y$ plane represents the smallest lateral length scale over which we characterise the measured disorder at the interface. Note that we do not average at all over the $z$ axis and hence maintain the inherent depth resolution of APT. We find that for tiles as small as 3 nm × 3 nm the numerical fitting of sigmoid functions to the profiles converges reliably. Although each tile contains many atoms, their size is still much smaller than the quantum dot diameter, and may therefore be considered to be microscopic. We use the sigmoid fits for each tile stack to visualise and further characterise the interfaces (Supplementary Figs. 6.14–6.16). Importantly, Ge concentration isosurfaces as shown in Fig. 6.2**b**,**c** are constructed by determining the vertical position for which each of the sigmoids reaches a specific concentration. Note, that we oversample the interface to improve the lateral resolution by making the 3 nm × 3 nm tiles partially overlap (Supplementary Discussion Section 6.7.2**C**).

In Fig. 6.2**d**, we show the average Ge concentration profile and measurement to measurement variations from the tessellated volumes (Supplementary Discussion Section 6.7.2 **B**,**C**) of all samples for both quantum wells A and B. APT confirms HAADF-STEM results in Fig. 6.1**a**,**b**: quantum wells A and B have an identical sharp top interface and quantum well A has a broader bottom interface. Furthermore, the shaded colored areas in Fig. 6.2**d** reveal narrow 95% confidence levels, pointing to highly uniform concentration profiles when averaged across the wafer. Strong disorder fluctuations emerge at the much smaller tile length scale. In Fig. 6.2**e** we show for all samples of a given quantum well the interface width mean value with two standard deviations $\overline{4\tau} \pm 2\sigma$, obtained by averaging over all the tiles in a given sample. The results indicate uniformity of $\overline{4\tau}$, and further averaging across all samples of a given heterostructure ($\mu_{\overline{4\tau}}$, black crosses) yields similar values of $\mu_{\overline{4\tau}} = 0.85 \pm 0.32$ nm and $0.79 \pm 0.31$ nm for quantum wells A and B, consistent with our $4\tau$ analysis from HAADF-STEM measurements (black dotted lines). However, the two-standard-deviation errors ($2\sigma$) of each data point can be up to 30% of the mean value $\overline{4\tau}$.

To pinpoint the root cause of atomic-scale fluctuations at the interface, in Fig. 6.2**f**,**g** we utilize the 3D nature of the APT data sets, calculate, and compare the root mean square (RMS) roughness of the interfaces (solid green lines) as measured by APT on quantum well B to two 3D models (Fig. 6.2**f**,**g**) mimicking the dimensions of an APT data set. Both models are generated with random distributions of Si and Ge in each atomic plane (see section 6.7.2**D**). The first model (solid black lines) corresponds to an atomically abrupt interface where the Ge concentration drops from ~33.5% to 0% in a single atomic layer. It hence represents the minimum roughness achievable at each isoconcentration surface given the in-plane randomness of SiGe and the method to construct the interface. The second model (dashed black lines) is generated with the experimentally determined Ge concentration profile along the depth axis (Supplementary Fig. 6.17). As shown in Fig. 6.2**f**,**g**, the roughness extracted from the second model fits well to the measured data, suggesting that the RMS roughness measured by APT is fully explained by the interface width and shape along the depth axis. Furthermore, as the deviation of each isosurface tile position from the isosurface's average position also matches that of the measured interfaces from the second model (Supplementary Movie 1 in Ref. [73]) the APT data are consistent with a random in-plane distribution of Ge perpendicular to the interface in all data sets of quantum well B. For 2 out of 5 samples on quantum well

A that we analyzed, we observe features that are compatible with correlated disorder from atomic steps (Fig. 6.19). In the following, the alloy disorder observed in the APT concentration interfaces is incorporated into a theoretical model. As shown below, the calculations of valley splitting distributions associated with the 3D landscape of Si/SiGe interfaces can be further simplified into a 1D model that incorporates the in-plane random distribution of Si and Ge atoms.

## 6.4. VALLEY SPLITTING SIMULATIONS

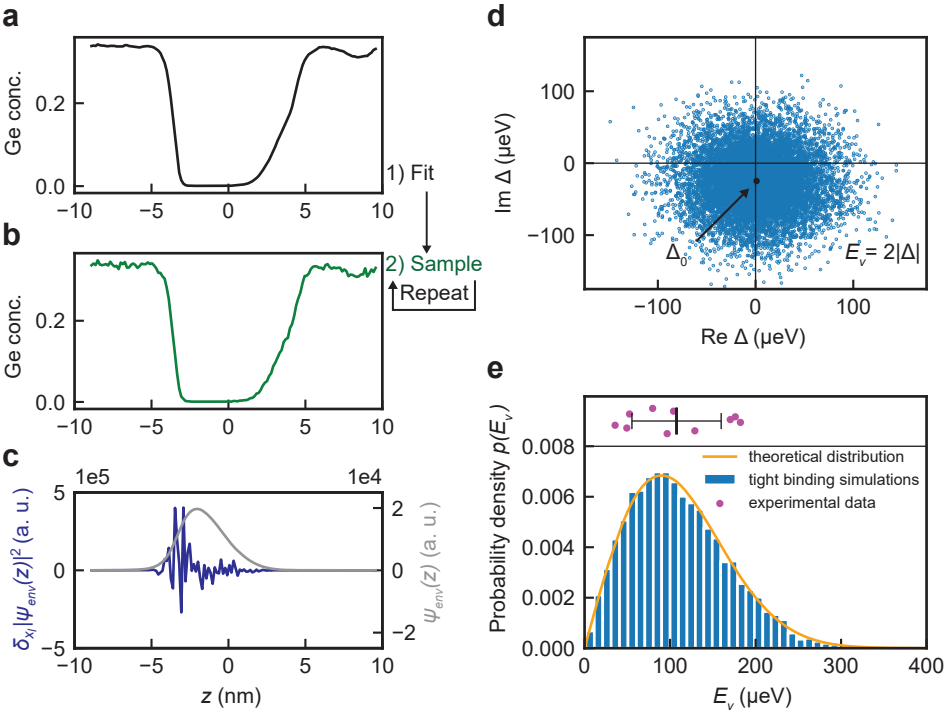


Figure 6.3: **Valley-splitting simulations.** **a** Average concentration profile obtained from APT data (quantum well A). **b**, Typical, randomized Ge concentration profile, derived from **a**. **c** Envelope function $\psi_{\mathrm{env}}(z)$, obtained for the randomized profile in **b** (grey curve), and the corresponding concentration fluctuations weighted by the envelope function squared: $\delta_{x_l}|\psi_{\mathrm{env}}(z_l)|^2$ (blue). Here, the wavefunction is concentrated near the top interface where the concentration fluctuations are also large; the weighted fluctuations are therefore largest in this regime. **d** Distribution of the intervalley matrix element $\Delta$ in the complex plane, as computed using an effective-mass approach, for 2,000 randomized concentration profiles. The black marker indicates the deterministic value of the matrix element $\Delta_0$, obtained for the experimental profile in **a**. **e**, Histogram of the valley splittings from tight-binding simulations with 10,000 randomized profiles. The same profiles may be used to compute valley splittings using effective-mass methods; the orange curve shows a Rice distribution whose parameters are obtained from such effective-mass calculations (see section 6.6.5).

We begin by considering an ideal laterally infinite heterostructure with no concentration fluctuations, and we denote the average Si concentration at layer $l$ by $\bar{x}_l$. Due to the finite size of a quantum dot and the randomness in atomic deposition, there will be

dot-to-dot concentration fluctuations. We therefore model the actual Si concentration at layer $l$ by averaging the random alloy distribution weighted by the lateral charge density in the quantum dot, giving $x_l^d = \bar{x}_l + \delta_{x_l}$, as described in Supplementary Discussion Section 3c in Ref. [73]. Here, the random variation $\delta_{x_l}$ is computed assuming a binomial distribution of Si and Ge atoms. We find that these fluctuations can have a significant impact on the valley splitting.

We explore these effects numerically using 1D tight-binding simulations. We begin with the averaged fitted concentration profiles obtained from the APT analysis in Fig **??**d, which enable us to directly measure the average Ge concentration in a given layer $\bar{x}_l$ (Fig. 6.3**a**). The variance of the concentration fluctuations is determined by the size of the quantum dot, which we assume has an orbital excitation energy of $\hbar\omega = 2$ meV and corresponding radius $\sqrt{\hbar/m^*\omega}$, as well as the average Si concentration $\bar{x}_l$. Here, $m^*$ is the effective mass of Si. Together, $\bar{x}_l$ and the variance determine the probability distribution of weighted Si and Ge concentrations. Concentration profiles are sampled repeatedly from this distribution, with a typical example shown in Fig. 6.3**b**. The valley splitting is then determined from a 1D tight-binding model [69]. The envelope of the effective mass wavefunction $\psi_{\text{env}}(z)$ is shown in Fig. 6.3c (grey curve) for an electron confined in the quantum well of Fig. 6.3**b**. The procedure is repeated for 10,000 profile samples, obtaining the histogram of valley splittings shown in Fig. 6.3**e**. These results agree very well with calculations obtained using a more sophisticated three-dimensional 20-band $sp^3d^5s^*$ NEMO tight-binding model[71] (Supplementary Discussion Section 3b in Ref. [73]) and confirm that concentration fluctuations can produce a wide range of valley splittings. For comparison, at the top of Fig. 6.3**e**, we also plot the same experimental valley splittings shown in Fig. 6.1**h**, demonstrating good agreement in both the average value and the statistical spread. These observations support our claim that the valley splitting is strongly affected by composition fluctuations due to random distributions of Si and Ge atoms near the quantum well interfaces, even though the experiments cannot exclude the presence of correlated disorder from atomic steps in quantum dots.

Analytical methods using effective mass theory may also be used to characterise the distribution of valley splittings. First, we model the intervalley coupling matrix element [67] as $\Delta = \int e^{-2ik_0z_l} U(z)|\psi_{\text{env}}(z)|^2 dz$, where $k_0 = 0.82 \cdot 2\pi/a_0$ is the position of the valley minimum in the Si Brillouin zone, $a_0 = 0.543$ nm is length of the Si cubic unit cell, $\psi_{\text{env}}(z)$ is a 1D envelope function, and $U(z)$ is the quantum well confinement potential. The intervalley coupling $\Delta$ describes how sharp features in the confinement potential couple the two valley states, which would otherwise be degenerate. In general, $\Delta$ is a complex number that can be viewed as the sum of two distinct components: a deterministic piece $\Delta_0$, arising from the average interface concentration profile, and a random piece $\delta\Delta$, arising from concentration fluctuations. The latter can be expressed as a sum of contributions from individual atomic layers: $\delta\Delta = \sum_l \delta\Delta_l$, where $\delta\Delta_l$ is proportional to $\delta_{x_l}|\psi_{\text{env}}(z_l)|^2$ (see section 6.6.5). To visualize the effects of concentration fluctuations in Fig. 6.3**c**, we compute $\delta\Delta_l$ using the randomized density profile of Fig. 6.3**b** (blue curve). We see that most significant fluctuations occur near the top interface, where $|\psi_{\text{env}}(z_l)|$ and the Ge content of the quantum well are both large. In Fig. 6.3**d** we plot $\Delta$ values obtained for 2,000 quantum-well realizations using this effective mass approach. The deterministic contribution to the valley splitting $\Delta_0$ (black dot) is seen to be located

near the center of the distribution in the complex plane, as expected. However, the vast majority of $\Delta$ values are much larger than $\Delta_0$, demonstrating that concentration fluctuations typically provide the dominant contribution to intervalley coupling.

The total valley splitting is closely related to the intervalley coupling via $E_v = 2|\Delta|$, and therefore exhibits the same statistical behavior. In Fig. 6.3**e**, the orange curve shows the Rice distribution whose parameters are derived from effective-mass calculations of the valley splitting (see section 6.6.5), using the same concentration profiles as the histogram data. The excellent agreement between these different approaches confirms the accuracy of our theoretical techniques (Supplementary Discussion Section 3d in Ref. [73]).

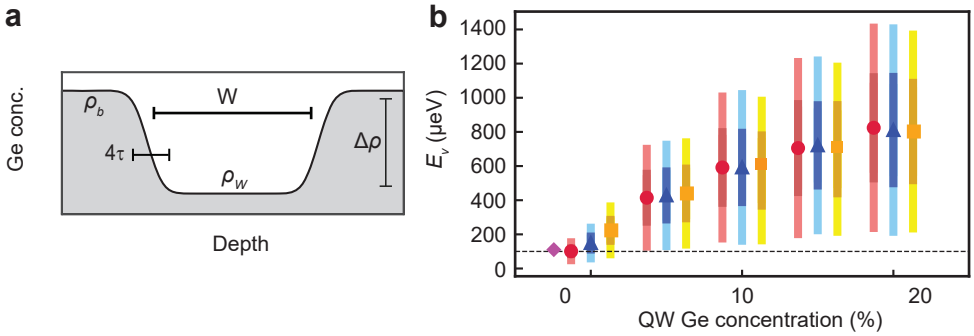


Figure 6.4: **Valley-splitting simulations. a**, Schematic Si/SiGe quantum well with Ge concentrations $\rho_W$ (in the well) and $\rho_b = \rho_W + \Delta\rho$ (in the barriers), with a fixed concentration difference of $\Delta\rho = 25\%$. **b**, Distribution of valley splittings obtained from simulations with variable Ge concentrations, corresponding to $\rho_W$ ranging from 0 to 20%, and interface widths $4\tau = 5$ ML (red circles), 10 ML (blue triangles), or 20 ML (orange squares), where ML refers to atomic monolayers. Here, the marker describes the mean valley splitting, while the darker bars represent the 25-75 percentile range and the lighter bars represent the 5-95 percentile range. Each bar reflects 2,000 randomized tight-binding simulations of a quantum well of width $W = 120$ ML. The magenta diamond at zero Ge concentration shows the average measured valley splitting of quantum well A. In all simulations reported here, we assume an electric field of $E = 0.0125$ V/nm and a parabolic single-electron quantum-dot confinement potential with orbital excitation energy $\hbar\omega = 2$ meV and corresponding dot radius $\sqrt{\hbar/m^*\omega}$.

## 6.5. DISCUSSION

Based on the results obtained above, we now propose two related methods for achieving large valley splittings (on average), with high yields. Both methods are derived from the key insight of Fig. 6.3**c**: due to random-alloy fluctuations, the valley splitting is almost always enhanced when the electronic wavefunction overlaps with more Ge atoms. In the first method, we therefore propose to increase the width of the interface ($4\tau$) as shown in Fig. 6.3**f**, since this enhances the wavefunction overlap with Ge atoms at the top of the quantum well. This approach is nonintuitive because it conflicts with the conventional deterministic approach of engineering sharp interfaces. The second method, also shown in Fig. 6.4**a**, involves intentionally introducing a low concentration of Ge inside the quantum well. The latter method is likely more robust because it can incorporate both deterministic enhancement of the valley splitting from a sharp interface, and

fluctuation-enhanced valley splitting.

We test these predictions using simulations, as reported in Fig. 6.4**g**, where different colors represent different interface widths and the horizontal axis describes the addition of Ge to the quantum well. For no Ge in the quantum well, as consistent with our experiments, we observe significant increases in the valley splitting with increasing interface width. Here, the narrowest interface appears most consistent with our experimental results (green marker), attesting to the sharp interfaces achieved in our devices. As the Ge concentration increases in the quantum well, this advantage is largely overwhelmed by concentration fluctuations throughout the well. A very substantial increase in valley splitting is observed for all concentration enhancements, even at the low, 5% level. Here, the light error bars represent 5-95 percentiles while dark bars represent 25-75 percentiles. At the 5% concentration level, our simulations indicate that >95% of devices should achieve valley splittings >100 μeV. This value is more than an order of magnitude larger than the typical operation temperature of spin-qubits and is predicted to yield a 99% readout fidelity[66]. This would represent a significant improvement in qubit yield for Si quantum dots. A recent report of SiGe quantum wells with oscillating Ge concentrations provides the first experimental evidence that intentionally placing Ge in the quantum well leads to significant variability and some of the highest recorded values of valley splitting[223].

In conclusion, we argue for the atomic-level origin of valley splitting distributions in realistic Si/SiGe quantum dots, providing key insights on the inherent variability of Si/SiGe qubits and thereby solving a longstanding problem facing their scaling. We relate 3D atom-by-atom measurements of the heterointerfaces to the statistical electrical characterization of devices, and ultimately to underlying theoretical models. We observe qualitative and quantitative agreement between simulated valley splitting distributions and measurements from several quantum dots, supporting our theoretical framework. Crucially, we learn that atomic concentration fluctuations of the $^{28}$Si → Si-Ge heterointerface are enough to account for the valley splitting spread and that these fluctuations are largest when the envelope of the wavefunction overlaps with more Ge atoms. Moreover, while we have only incorporated random alloy disorder into our theoretical framework so far, we foresee that APT datasets including correlated disorder, such as steps, will be used to further refine our theoretical understanding of valley splitting statistics. Since atomic concentration fluctuations are always present in Si/SiGe devices due to the intrinsic random nature of the SiGe alloy, we propose to boost these fluctuations to achieve on average large valley splittings in realistic silicon quantum dots, as required for scaling the size of quantum processors. Our proposed approaches are counter-intuitive yet very pragmatic. The interface broadening approach seems viable for hybrid qubits, which require valley splitting to be large enough to be usable but not so large as to be inaccessible. For single-electron spin qubits, which don't use the valley degree of freedom, the direct introduction of Ge in the quantum well appears better suited for targeting the largest possible valley splitting. By adding Ge to the Si quantum well in small concentrations we expect to achieve on average valley splitting in excess of 100 μeV. Based on results from scattering theories[121], we speculate that the added scattering from random alloy disorder will not be the limiting factor for mobility in current $^{28}$Si/SiGe heterostructures and therefore should not compromise the low-disorder potential environment, which is

important for scaling to large qubit systems. We believe that our results will inspire a new generation of Si/SiGe material stacks that rely on atomic-scale randomness of the SiGe as a new dimension for the heterostructure design.

## 6.6. METHODS

### 6.6.1. SI/SIGE HETEROSTRUCTURE GROWTH

The $^{28}$Si/SiGe heterostructures are grown on a 100-mm n-type Si(001) substrate using an Epsilon 2000 (ASMI) reduced pressure chemical vapor deposition reactor equipped with a $^{28}SiH_4$ gas cylinder (1% dilution in $H_2$) for the growth of isotopically enriched $^{28}$Si. The $^{28}SiH_4$ gas was obtained by reducing $^{28}SiF_4$ with a residual $^{29}$Si concentration of 0.08%[141]. Starting from the Si substrate, the layer sequence for quantum well A comprises a 900 nm layer of $Si_{1-x}Ge_x$ graded linearly from $x = 0$ to 0.3, followed by a 300 nm $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer, an 8 nm tensily strained $^{28}$Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a sacrificial Si cap. The layer sequence for quantum well B comprises a 1.4 µm step-graded $Si_{(1-x)}Ge_x$ layer with a final Ge concentration of $x = 0.3$ achieved in four grading steps ($x = 0.07$, 0.14, 0.21, and 0.3), followed by a 0.45 µm $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer, an 8 nm tensily strained $^{28}$Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a sacrificial Si cap. In quantum well A, the $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer and the Si quantum well are grown at 750 °C without growth interruption. In quantum well B the $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer below the quantum well is grown at a temperature of 625 °C, followed by growth interruption and quantum well growth at 750 °C. This modified temperature profile yields a sharper bottom interface for quantum well B as compared to quantum well A.



### 6.6.2. ATOM PROBE TOMOGRAPHY

Samples for APT were prepared in a FEI Helios Nanolab 660 dual-beam scanning electron microscope using a gallium focused ion beam at 30, 16 and 5 kV and using a procedure described in detail in ref. [224]. Before preparation, a 150-200 nm thick chromium capping layer was deposited on the sample via thermal evaporation to minimize the implantation of gallium ions into the sample. All APT analyses were started inside this chromium cap with the stack fully intact underneath. APT was carried out using a LEAP 5000XS tool from Cameca. The system is equipped with a laser to generate picosecond pulses at a wavelength of 355 nm. For the analysis, all samples were cooled to a temperature of 25 K. The experimental data are collected at a laser pulse rate of 200-500 kHz at a laser power of 8-10 pJ. APT data are reconstructed using IVAS 3.8.5a34 software and visualized using the AtomBlend addon to Blender 2.79b and Blender 2.92 software. For the Voronoi tessellation the reconstructed data sets were exported to Python 3.9.2 and then tessellated using the scipy.spatial.Voronoi class of SciPy 1.6.2. Note that in these analyses the interfaces are represented as an array of sigmoid functions generated perpendicular to the respective interface on 3 nm × 3 nm tiles that are 1 nm apart. This sacrifices lateral resolution to allow for statistical sampling of the elemental concentrations but preserves the atomic resolution along the depth axis that APT is known to provide upon constructing the interface as shown in Fig. 6.2**a**.

### 6.6.3. DEVICE FABRICATION

The fabrication process for Hall-bar shaped heterostructure field effect transistors (H-FETs) involves: reactive ion etching of mesa-trench to isolate the two-dimensional electron gas (2DEG); P-ion implantation and activation by rapid thermal annealing at 700 °C; atomic layer deposition of a 10-nm-thick $Al_2O_3$ gate oxide; deposition of thick dielectric pads to protect gate oxide during subsequent wire bonding step; sputtering of Al gate; electron beam evaporation of Ti:Pt to create ohmic contacts to the 2DEG via doped areas. All patterning is done by optical lithography. Quantum dot devices are fabricated on wafer coupons from the same H-FET fabrication run and share the process steps listed above. Double-quantum dot devices feature a single layer gate metallization and further require electron beam lithography, evaporation of Al (27 nm) or Ti:Pd (3:27 nm) thin film metal gate, and lift-off. For linear quantum dot arrays the gate stack consists of 3 layers of Ti:Pd metallic gates (3:17, 3:27, 3:27 nm) isolated from each other by 5 nm $Al_2O_3$ dielectric interlayers. The fabrication processes for quantum dot devices are further detailed in ref. [225].

### 6.6.4. ELECTRICAL CHARACTERIZATION OF DEVICES

Hall-bar measurement are performed in a Leiden cryogenic dilution refrigerator with a mixing chamber base temperature $T_{\mathrm{MC}} = 50$mK[155]. We apply a source-drain bias of 100 μV and measure the source-drain current $I_{\mathrm{SD}}$, the longitudinal voltage $V_{xx}$, and the transverse Hall voltage $V_{xy}$ as function of the top gate voltage $V_g$ and the external perpendicular magnetic field $B$. From here we calculate the longitudinal resistivity $\rho_{xx}$ and transverse Hall resistivity $\rho_{xy}$. The Hall electron density $n$ is obtained from the linear relationship $\rho_{xy} = B/en$ at low magnetic fields. The carrier mobility $\mu$ is extracted from the relationship $\sigma_{xx} = ne\mu$, where $e$ is the electron charge. The percolation density $n_p$ is extracted by fitting the longitudinal conductivity $\sigma_{xx}$ to the relation $\sigma_{xx} \propto (n - n_p)^{1.31}$. Here $\sigma_{xx}$ is obtained via tensor inversion of $\rho_{xx}$ at $B = 0$. Quantum dot measurements are performed in Oxford and Leiden cryogenic refrigerators with base temperatures ranging from 10–50 mK. Quantum dot devices are operated in the few-electron regime. Further details of the 2DEG and quantum dot measurements are provided in section 6.7.1.

### 6.6.5. THEORY AND SIMULATIONS

The quantum-well potential at vertical position $z_l$ is simply defined here as a linear interpolation of the conduction-band offset at the quantum-well interface: $U(z_l) = \frac{x_l^d - x_s}{x_w - x_s}\Delta E_c$, where $x_l^d$ is the average Si concentration in layer $l$, $x_s$ is the average Si concentration in the strain-relaxed SiGe barriers, $x_w$ is the average Si concentration in the strained quantum well, and $\Delta E_c$ is the conduction band offset in the absence of fluctuations. In the effective-mass theory, the intervalley coupling matrix element can then be approximated by the sum

$$\Delta = \frac{a_0}{4} \sum_l e^{-2ik_0 z_l} \frac{x_l^d - x_s}{x_w - x_s} \Delta E_c |\psi_{\mathrm{env}}(z_l)|^2. \tag{6.1}$$

Defining the local concentration fluctuations as $x_l^d = \bar{x}_l + \delta_l$, the matrix element can then be split into its deterministic and fluctuating contributions $\Delta = \Delta_0 + \delta\Delta$, where the

fluctuating term $\delta\Delta$ contains all dependence on $\delta_l$:

$$\delta\Delta = \frac{a_0}{4}\frac{\Delta E_c}{x_w - x_s}\sum_l e^{-2ik_0 z_l}\delta_l|\psi_{\text{env}}(z_l)|^2. \tag{6.2}$$

The deterministic term $\Delta_0$ represents the matrix element of the ideal, smooth concentration profile, while $\delta\Delta$ describes the fluctuations about this value. For concentration fluctuations $\delta_l$ defined by binomial distributions of Ge and Si atoms, the resulting valley splitting $E_v = 2|\Delta_0+\delta\Delta|$ corresponds to a Rice distribution with parameters $\nu = 2|\Delta_0|$ and $\sigma = \sqrt{2}\sqrt{\text{Var}[\delta\Delta]}$ [226]. For additional details, see the Supplementary Discussion Section 3 in Ref [73]. All simulations and numerical calculations reported in this work were performed using Python 3.7.10 with the open-source libraries NumPy, SciPy, and Matplotlib. The 3D atomistic simulations were done using the large-scale Slater-Koster tight-binding solver NEMO3D. A spin resolved 20 band sp3d5s* nearest neighbour model was used. Strain optimization was done using a valence force field Keating model.

# 6.7. SUPPLEMENTARY INFORMATION

## 6.7.1. ELECTRICAL CHARACTERIZATION

### A. MAGNETOTRANSPORT CHARACTERIZATION OF HALL-BAR SHAPED HETEROSTRUCTURE FIELD EFFECT TRANSISTORS

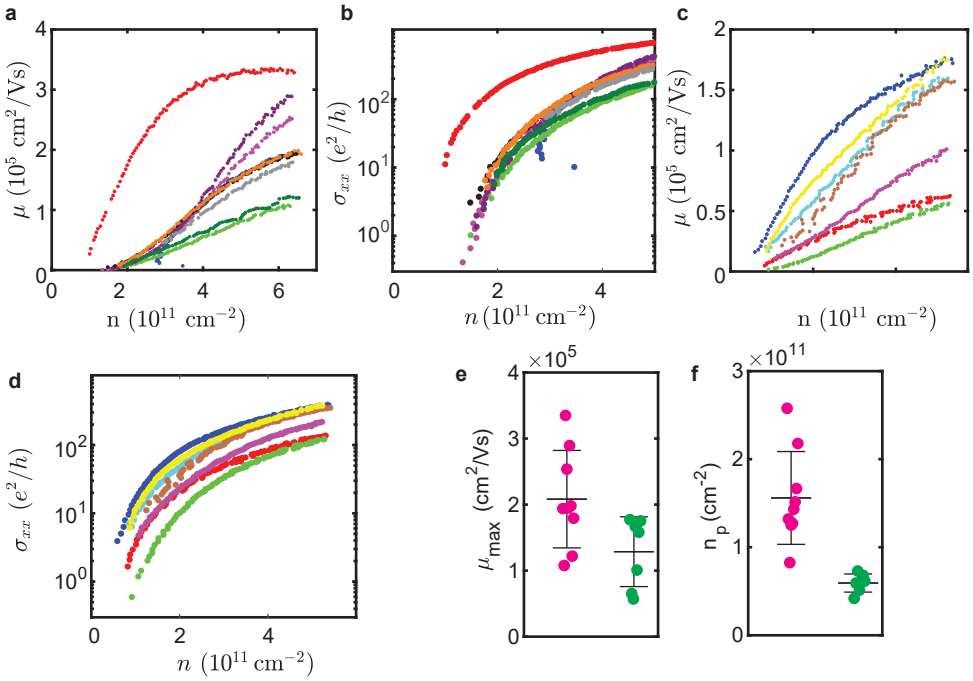


Figure 6.5: **a**,**b**. Mobility $\mu$ and conductivity $\sigma_{xx}$ as a function of Hall density $n$ measured for quantum well A. **c**, **d** Mobility $\mu$ and conductivity $\sigma_{xx}$ as a function of Hall density $n$ measured for quantum well B. **e** Maximum mobility $\mu_{max}$ for quantum well A (magenta) and quantum well B (green) extracted from **a** and **c**. Black crosses are the mean and standard deviation. For quantum well A we find $\overline{\mu_{max}} = 129.000 \pm 53.000$ cm$^2$/Vs and for quantum well B we find $\overline{\mu_{max}} = 208.000 \pm 74.000$ cm$^2$/Vs. **f** Percolation density $n_p$ for quantum well A (magenta) and quantum well B (green) extracted by fitting the conductivity-density curves in **b** and **d** to the relationship $\sigma_{xx} \propto (n - n_p)^{1.31}$ [125]. Since this percolation theory is valid only at low densities, for each sample we chose a fitting range that goes from the lowest measured density $n_{min}$ to a density $n_{max,fit}$ that yields the best fitting results. For the devices from quantum well A in **b** we have $n_{max,fit} = 3.2{\times}10^{11}$ cm$^{-2}$, $2.2{\times}10^{11}$ cm$^{-2}$, $2{\times}10^{11}$ cm$^{-2}$, $2{\times}10^{11}$ cm$^{-2}$, $2.2{\times}10^{11}$ cm$^{-2}$, $2.2{\times}10^{11}$ cm$^{-2}$, $2.5{\times}10^{11}$ cm$^{-2}$, $4{\times}10^{11}$ cm$^{-2}$, $5.8{\times}10^{11}$ cm$^{-2}$. For the devices from quantum well B in **d** we have $n_{max,fit} = 1.35{\times}10^{11}$ cm$^{-2}$, $1.35{\times}10^{11}$ cm$^{-2}$, $1.6{\times}10^{11}$ cm$^{-2}$, $1.6{\times}10^{11}$ cm$^{-2}$, $1.6{\times}10^{11}$ cm$^{-2}$, $1.8{\times}10^{11}$ cm$^{-2}$, $1.35{\times}10^{11}$ cm$^{-2}$ Black crosses are the mean and standard deviation of the percolation density. For quantum well A we find $\overline{n_p} = 1.56 \pm 0.53{\times}10^{11}$ cm$^{-2}$ and for quantum well B we find $\overline{n_p} = 0.59 \pm 0.1{\times}10^{11}$ cm$^{-2}$.

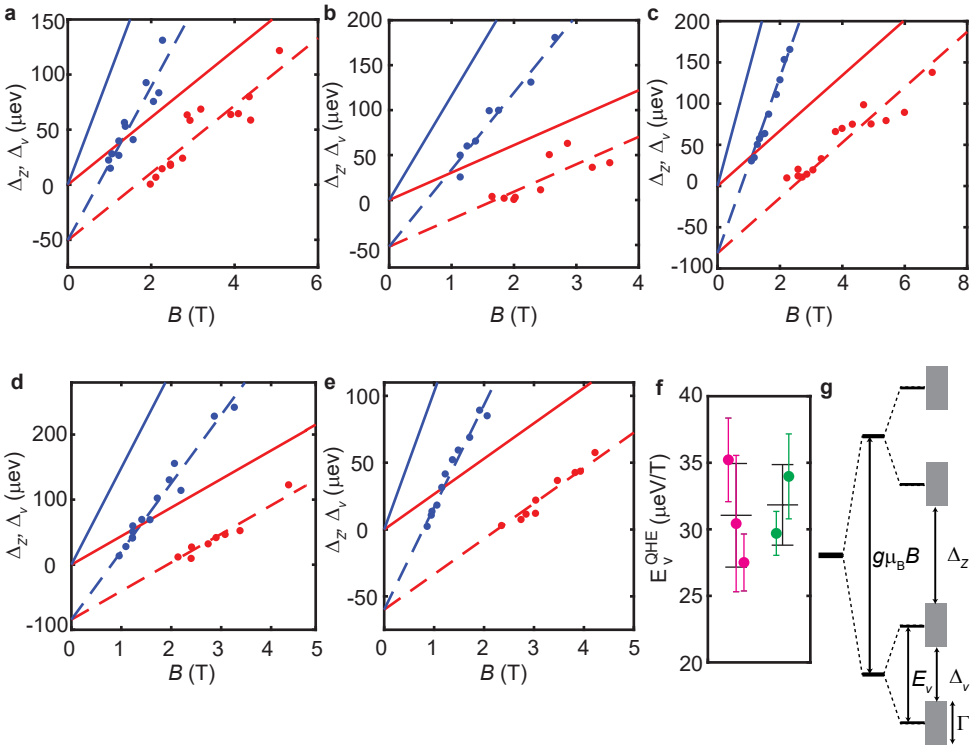


Figure 6.6: **a**-**c** Activation energy measurements of the valley gap $\Delta_v$ (red circles) and Zeeman gap $\Delta_Z$ (blue circles) as a function of the magnetic field $B$ for three different devices from quantum well A. $\Delta_v$ is measured at the $2n-1$ quantum Hall filling factors and $\Delta_Z$ is measured at the $4n-2$ filling factors. We follow the same methodology as in Ref. [119]. The blue and red dashed lines are theoretical fits to the experimental data using the equations $\Delta_Z = g^*\mu_B B - c_B B - \Gamma$ and $\Delta_v = c_B B - \Gamma$, where $g^*$ is the effective Landé-g-factor, $\mu_B$ is the Bohr magneton, $c_B$ is the proportionality factor of the valley splitting with $B$, and $\Gamma$ is the Landau level broadening induced by disorder. We obtain $c_B = 30.64 \pm 3.14$μeV/T, $30.43 \pm 5.12$ μeV/T, $32.46 \pm 2.14$ μeV/T, and $g^* = 1.74 \pm 0.16,\ 2 \pm 0.21,\ 2.36 \pm 0.12$ respectively. The blue and red solid lines correspond to the estimated Zeeman and valley energy gaps, respectively. **d**, **e** Activation energy measurements and fits of the valley gap and Zeeman gap as in **a**-**c** for two devices from quantum well B. We obtain $c_B = 26.28 \pm 1.65$ μeV/T, $43.15 \pm 3.19$ μeV/T, and $g^* = 1.77 \pm 0.13,\ 2.54 \pm 0.17$ respectively. **f** Rate of increase of valley splitting with magnetic field $E_V^{QHE}$ for quantum well A (magenta) and quantum well B (green) extracted from the fitting analysis of **a**-**e**. We calculate $E_V^{QHE}$ by setting $E_V^{QHE} = c_B g/g^*$, thereby scaling $c_B$ with a coefficient $g/g^*$ that normalizes the fitted $g^*$ to the value $g = 2$ in silicon. This normalization is a way to take into account the modest electron-electron interaction present in different devices, allowing for a comparison across different quantum wells. Black crosses are the mean and standard deviation of $E_V^{QHE}$. For quantum well A we find $\overline{E_V^{QHE}} = 31.1 \pm 3.9$ μeV/T and for quantum well B we find $\overline{E_V^{QHE}} = 31.8 \pm 3$ μeV/T. **g**, Schematic drawing of a Landau level split into Zeeman and valley energy levels, showing all relevant energy separations. Shaded areas represent the single-particle Landau level broadening $\Gamma$ due to disorder [119].

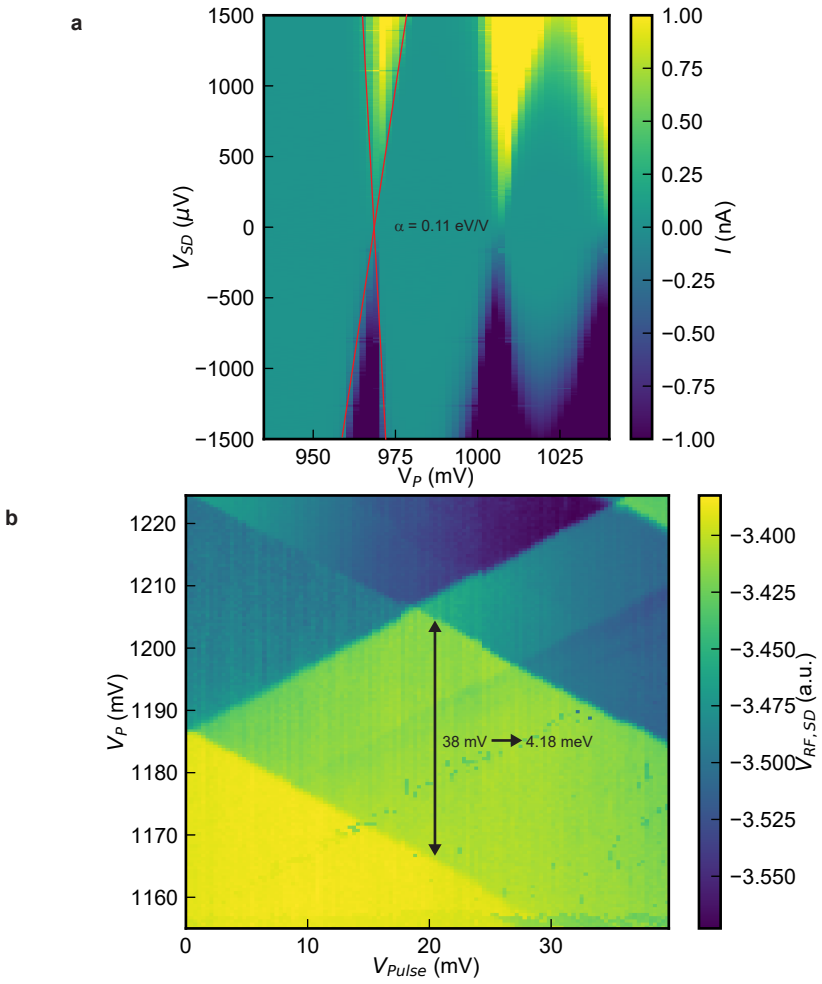


Figure 6.7: **a** Coulomb blockade measurements of QD1, device 5 (see Table S1). The current through the QD is monitored while scanning the gate voltage and the bias voltage applied between the source and the drain, resulting in Coulomb diamonds. From the leftmost Coulomb diamond (indicated by the red lines) we extract a leverarm $\alpha = 0.11$ eV/V using the method described in the supplementary information of Ref. [48]. **b** Pulsed gate spectroscopy for the same quantum dot. The time-averaged RF reflectometry signal/sensing dot response is plotted as a function of the dc gate voltage $V_P$ and the square pulse amplitude $V_{pulse}$ with a pulse frequency of 25 kHz, both applied to the same gate. The arrow indicates the orbital splitting, which we extract as $E_{orb} = \alpha V_{orb} = 4.18$ meV, consitent with other values reported in literature [190, 191, 195]

### B. SINGLET-TRIPLET ENERGY SPLITTING IN QUANTUM DOTS

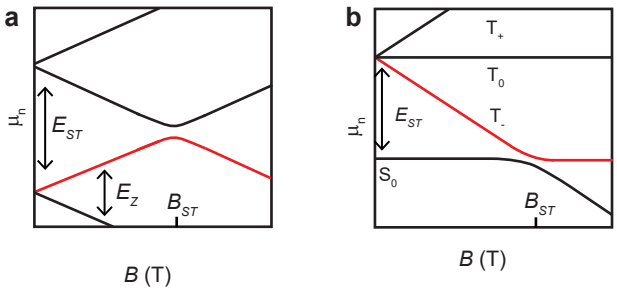


Figure 6.8: **a**, Energy evolution of the ground state and first excited state in a single quantum dot as a function of the magnetic field. The red line shows the expected spin filling for the charge transition $N = 1 \rightarrow 2$. At $B = B_{ST}$ the typical kink can be observed, where the Zeeman energy $E_Z$ is equal to the singlet-triplet splitting energy $E_{ST}$. **b**, Energy evolution of the four lowest lying energy states in a double quantum dot as a function of the magnetic field with fixed electron number $N = 2$. The red line represents the $T_-$ energy state measured along the (1,1) →(2,0) transition. At $B = B_{ST}$ the singlet state $S_0$ and the triplet state $T_-$ are equal in energy, resulting in an anticrossing.

The singlet-triplet energy splitting is computed according to the configurations in Fig. 6.8. In the configuration in Fig. 6.8**a** the red line can be fitted to compute $E_{ST}$ with the formula[215]:

$$V_P = \frac{1}{\alpha\beta_e} \ln \frac{e^{\frac{1}{2}\kappa B + \beta_e E_{ST}}(e^{\kappa B}+1)}{e^{\kappa B} + e^{2\kappa B} + e^{\kappa B + \beta_e E_{ST}} + 1}, \tag{6.3}$$

where $\alpha$ is the lever arm converting gate voltage to energy, $V_P$ is the gate voltage, $\kappa = g\mu_B\beta_e$ where $\beta_e = 1/k_B T_e$, $g$ is the Lande-g-factor in silicon, $\mu_B$ is the Bohr magneton, $B$ is the magnetic field, $k_B$ is Boltzmann's constant, and $T_e$ is the electron temperature[215].

In the configuration in Fig. 6.8**b** the Hamiltonian of the T− state is given by:

$$\hat{H} = \begin{pmatrix} \mathrm{E_{S0}} & \mathrm{t}_c \\ \mathrm{t}_c & \mathrm{E}_{T-} \end{pmatrix} \tag{6.4}$$

where $E_{S0}$ is the energy evolution of the singlet state, $E_{T-}$ is the energy evolution of the triplet minus-state, and the off-diagonal element $t_c$ is the tunnel coupling between the (1,1)-state and the the (2,0)-state in the double quantum dot. Diagonalization of the Hamiltonian yields:

$$\mu_n(T-) = \frac{1}{2}(E_{S0} + E_{T-} + \sqrt{(E_{S0} - E_{T-})^2 + 4t_c^2}) \tag{6.5}$$

To fit the red line from Fig. 6.8**b** we use $E_{S0} = 0$ and $E_{T-} = \alpha(g\mu_B B + E_{ST})$, where $\alpha$ is the lever arm, $g$ is the single particle g-factor, $B$ is the magnetic field, and $E_{ST}$ is the singlet-triplet splitting.

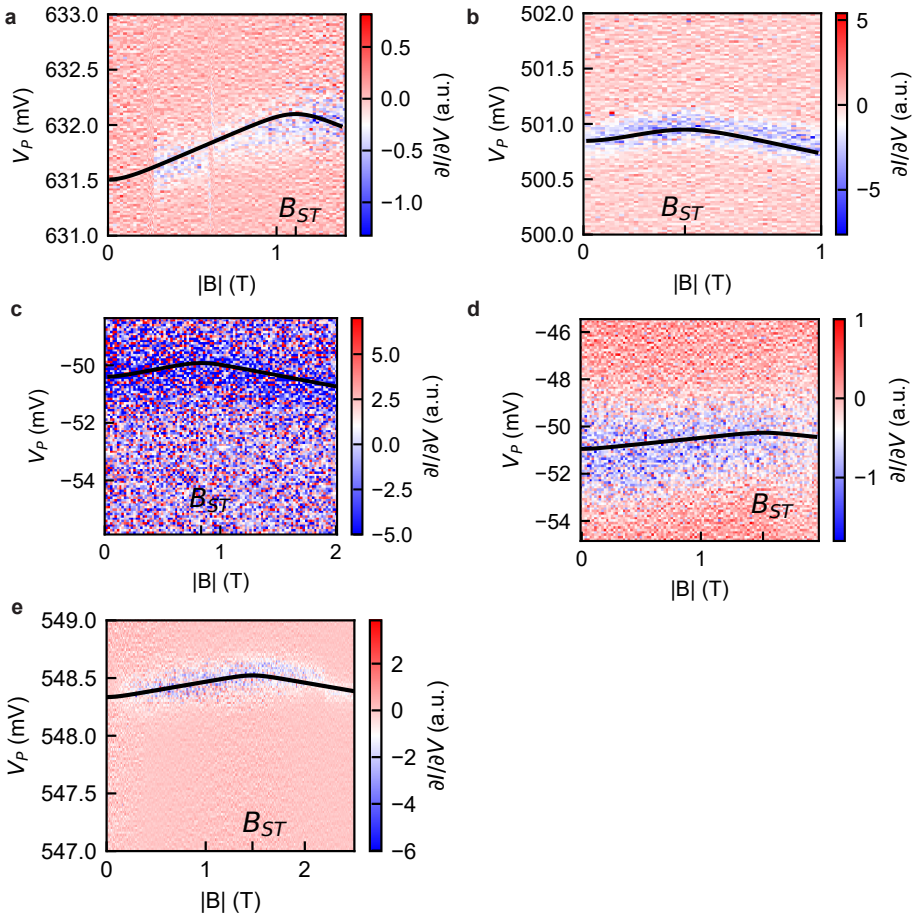


Figure 6.9: Magnetospectroscopy of quantum dots fabricated on quantum well A. $V_P$ is the gate voltage applied to the plunger gate forming the quantum dot. **a** - **e** Magnetospectroscopy data measured along the $N = 1 \rightarrow 2$ transition of five different quantum dots on three different samples in quantum well A. The signal is measured by monitoring the derivative of the current through a nearby charge sensor. a), A charge fluctuation occurred during the measurement and to optimize the fitting routine, we shifted the data in the range 0.3-0.6 T upwards by 1 mV. **a** - **e**, Due to low tunnel rates, for each gate Voltage sweep at the different magnetic fields, we determine the points with the highest derivative of the current $\frac{\partial I}{\partial V}$ through the charge sensor as the $N = 1 \rightarrow 2$ charge transition. We then use these points as the input of eq. 6.3. With this equation we can fit the charge transition as a function of the magnetic field (black curve).

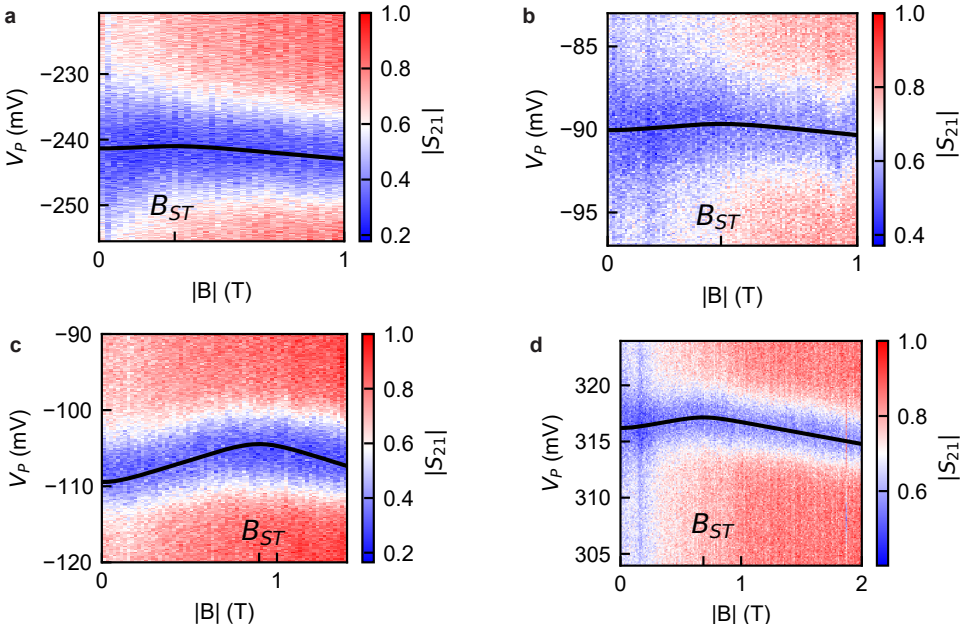


Figure 6.10: Magnetospectroscopy of quantum dots fabricated on quantum well A. $V_P$ is the gate voltage applied to the plunger gate forming the quantum dot. **a** - **d** Magnetospectroscopy data measured along the $N = 1 \rightarrow 2$ transition of four different quantum dots on two different samples in quantum well A. The quantum dot is probed via gate-based sensing using an on-chip superconducting resonator in these measurements [171]. The magnitude of the transmitted microwave signal $S_{21}$ through a feed line that is capacitively coupled to the resonator is plotted here. For each gate Voltage sweep at the different magnetic fields, we use a Lorentzian function to find the resonance peak of the signal. The resonance peaks then are used as input of eq. 6.3. With this equation we can fit the charge transition as a function of the magnetic field (black curve).

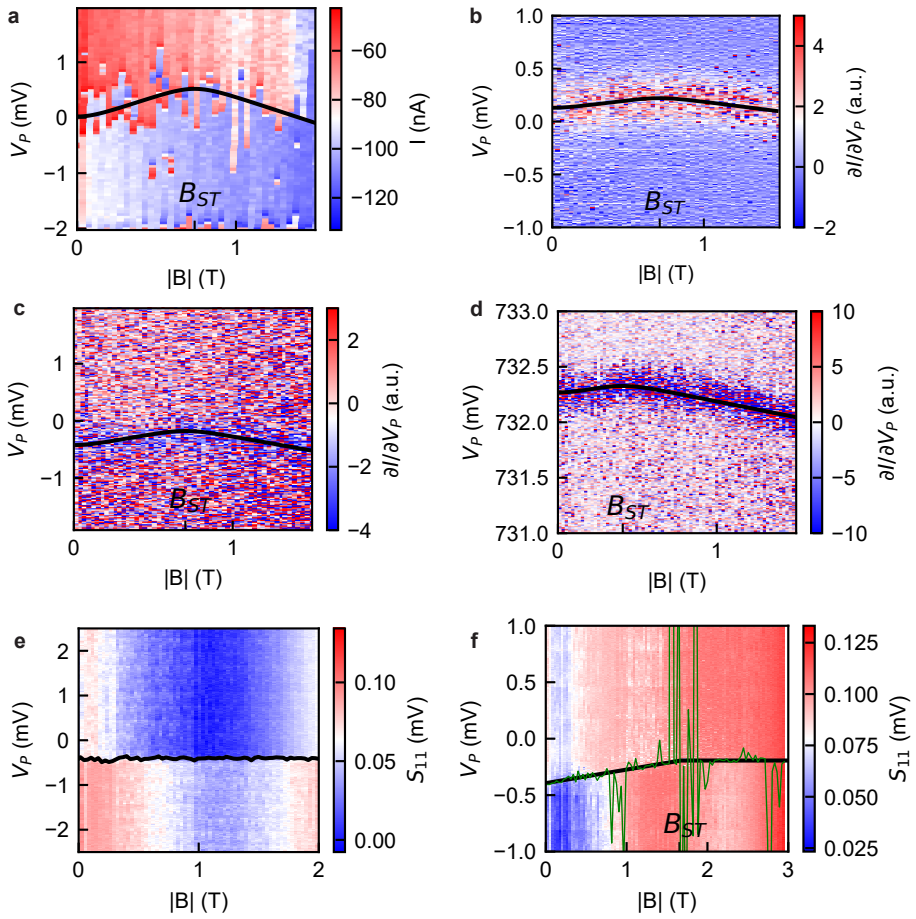


Figure 6.11: Magnetospectroscopy of quantum dots fabricated on quantum well B. $V_P$ is the gate voltage applied to the plunger gate forming the quantum dot. For clarity, we subtract from $V_P$ in panels **a**, **b** **c**, **e**, and **f** an offset that depends is on the quantum dot being measured. **a** - **d** Magnetospectroscopy data measured along the $N = 1 \rightarrow 2$ transition of four different quantum dots on two different samples in quantum well B. The signal is measured by monitoring **a**, the current $I$ through a nearby charge sensor, or **b** - **d** by monitoring the derivative of the current $\frac{\partial I}{\partial V}$ through a nearby charge sensor. **a** - **d**, To extract the inflection point of the electron charge transition, we fit the signal of the detuning for every magnetic field to eq. (2) from Ref. [227]. The inflection points then are used as input of eq. 6.3. With this equation we can fit the charge transition as a function of the magnetic field (black curve). **e** - **f** Magnetospectroscopy data measured along the $N = (1,1) \rightarrow (2,0)$ transition of eight different quantum dots on two different samples in quantum well B. The signal is measured by monitoring the reflected amplitude of the rf readout signal through a nearby charge sensor. To extract the inflection point of the electron charge transition, we fit the signal of the detuning for every magnetic field to eq. (2) from Ref. [227]. Here we superimpose the inflection points as green curves, to help the reader to follow the charge transitions. To extract $B_{ST}$ we use the crossing point of two linear fits (black solid lines) along the $T_-$ and $S_0$-state. On top of these samples there is a micromagnet lowering the magnetic field strength at the center of the sample by up to 0.2 T corresponding to 23 μeV which is taken as a lower bound for measurable $E_{ST}$.

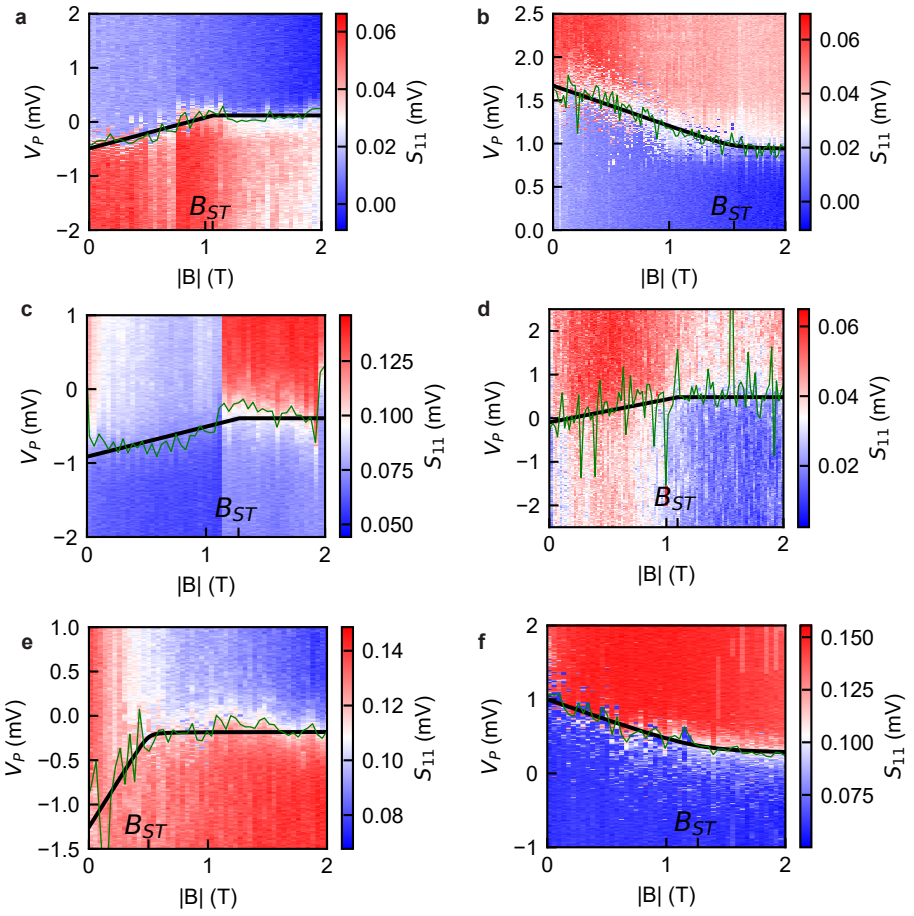


Figure 6.12: Magnetospectroscopy of quantum dots fabricated on quantum well B. $V_P$ is the gate voltage applied to the plunger gate forming the quantum dot. For clarity, we subtract from $V_P$ in panels **a** - **f** an offset that depends is on the quantum dot being measured. **a** - **f** Magnetospectroscopy data measured along the $N = (1,1) \rightarrow (2,0)$ transition of six different quantum dots on one sample in quantum well B. The signal is measured by monitoring the reflected amplitude of the rf readout signal through a nearby charge sensor. To extract the inflection point of the electron charge transition, we fit the signal of the detuning for every magnetic field to eq. (2) from Ref. [227]. Here we superimpose the inflection points as green curves, to help the reader to follow the charge transitions. To extract $B_{ST}$ we use the crossing point of two linear fits (black solid lines) along the $T_-$ and $S_0$-state. On top of these samples there is a micromagnet lowering the magnetic field strength at the center of the sample by up to 0.2 T corresponding to 23 µeV which is taken as a lower bound for measurable $E_{ST}$.

| Stack | Wafer ID | database processing ID | Figure | device ID | transition | $B_S T$ (T) | $E_S T$ μeV | $d_P$ (nm) |
|---|---|---|---|---|---|---|---|---|
| QW A | QT428 | DEMO 13 | 6.9**a** | D1 2-dot, P2 | (0,1) → (0,2) | 1.11 | 129±1.1 | 50 |
| QW A | QT428 | DEMO 13 | 6.9**b** | D1 2-dot, P1 | (0,1) → (0,2) | 0.42 | 49.4±2.2 | 50 |
| QW A | QT428 | DEMO 21 | 6.9**c** | D2 2-dot, P1 | (0,1) → (0,2) | 0.83 | 96.6±6.3 | 50 |
| QW A | QT428 | DEMO 21 | 6.9**d** | D2 2-dot, P2 | (0,1) → (0,2) | 1.47 | 170.4±9.0 | 50 |
| QW A | QT428 | DEMO 15 | 6.9**e** | D3 2-dot, P1 | (0,1) → (0,2) | 1.52 | 176.3±13.4 | 50 |
| QW A | QT428 | DEMO 15 | 6.1**f**, | D3 2-dot, P2 | (0,1) → (0,2) | 1.57 | 182.3±5.8 | 50 |
| QW A | QT539 | SQ19-193-1-3-03 | 6.10**a** | D4 2-dot, P1 | (0,1) → (0,2) | 0.31 | 35.7±5.9 | 50 |
| QW A | QT539 | SQ19-193-1-3-03 | 6.10**b** | D4 2-dot, P2 | (0,1) → (0,2) | 0.45 | 52.6±0.8 | 50 |
| QW A | QT539 | SQ19-193-1-3-04 | 6.10**c** | D5 2-dot, P1 | (0,1) → (0,2) | 0.9 | 104±1.6 | 50 |
| QW A | QT539 | SQ19-193-1-3-04 | 6.10**d** | D5 2-dot, P2 | (0,1) → (0,2) | 0.69 | 79.6±2.0 | 50 |
| QW B | QT592 | SQ20-20-5-25-2 | 6.11**a** | D1 5-dot, P4 | (0,1) → (0,2) | 0.74 | 85.7±2.0 | 40 |
| QW B | QT592 | SQ20-20-5-25-2 | 6.11**b** | D1 5-dot, P1 | (0,1) → (0,2) | 0.71 | 82.1±3.7 | 40 |
| QW B | QT592 | SQ20-20-5-25-2 | 6.11**c** | D1 5-dot, P2 | (0,1) → (0,2) | 0.7 | 81.7±10.1 | 40 |
| QW B | QT553 | SQ19-228-2-44-2 | 6.11**d** | D6 2-dot, P2 | (0,1) → (0,2) | 0.41 | 47.2±3.68 | 50 |
| QW B | QT592 | SQ20-20-5-18-4 | 6.11**e** | D1 6-dot, P3 | (1,1) → (0,2) | 0 | 0±0 | 50 |
| QW B | QT592 | SQ20-20-5-18-4 | 6.11**f** | D1 6-dot, P4 | (1,1) → (0,2) | 1.73 | 191.5±13.2 | 50 |
| QW B | QT637 | SQ20-205-2-12 | 6.12**a** | D2 6-dot, P1 | (1,1) → (0,2) | 1.06 | 123.1±8.9 | 40 |
| QW B | QT637 | SQ20-205-2-12 | 6.12**b** | D2 6-dot, P2 | (1,1) → (0,2) | 1.56 | 180.5±9.7 | 40 |
| QW B | QT637 | SQ20-205-2-12 | 6.12**c** | D2 6-dot, P3 | (1,1) → (0,2) | 1.1 | 126.8±33.6 | 40 |
| QW B | QT637 | SQ20-205-2-12 | 6.12**d** | D2 6-dot, P4 | (1,1) → (0,2) | 1.27 | 147.3±15.7 | 40 |
| QW B | QT637 | SQ20-205-2-12 | 6.12**e** | D2 6-dot, P5 | (1,1) → (0,2) | 0.5 | 57.9±13.5 | 40 |
| QW B | QT637 | SQ20-205-2-12 | 6.12**f** | D2 6-dot, P6 | (1,1) → (0,2) | 1.25 | 144.6±19.1 | 40 |

Table 6.1: Summary of quantum dot valley splitting measurements. Among all devices measured, in one case (data point $E_{ST} = 0$ μeV) we did not observe in magnetospectroscopy the signature kink associated with valley splitting. This indicates a very small valley splitting, below the lower bound of about 23 μeV set by our experimental measurement conditions. While very small valley splitting values are within the predicted theoretical distributions in the main text, previous theories[67] suggest that they could also originate from the presence of an atomic step within the quantum dot.

### 6.7.2. MATERIAL CHARACTERIZATION

#### A. ATOM PROBE TOMOGRAPHY ANALYSIS OF INTERFACES

Atom Probe analysis (APT) of the interfaces is done in 5 steps. All of them explained in detail below. First, the entire measurement is reconstructed using the standard reconstruction algorithms [217]. Second, a cube approximately representing the size of an electrical defined quantum in the x,y-plane and comfortably comprising the entire quantum well in the z-direction/depth-direction is extracted from the reconstructed data. This is done to have comparable sizes for each measurement, to limit the known reconstruction artefacts of APT [218] and to enable a direct comparison to simulations in step 5. Third, the three-dimensional point cloud created in the usual APT reconstruction [217] is tessellated using a Voronoi tessellation [221, 222]. The Voronoi tessellation is used for all subsequent steps. It can be viewed as a smoothing operation that "spreads out" the detected ions/atoms to a finite volume rather than representing them as zero-dimensional points. Forth, a x,y-grid is defined on the cube and for each cell of the grid a profile based on the Voronoi tessellation along the z-axis is created that is than fitted



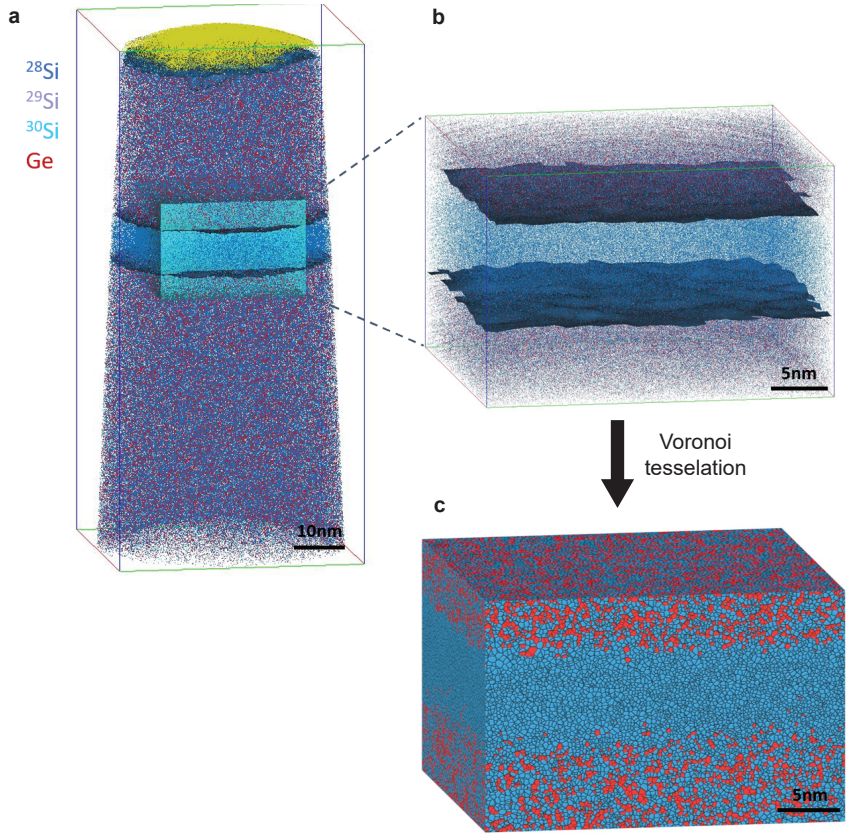


Figure 6.13: Visualization of the extraction of the cube **b** from the full data set **a** and Voronoi tessellation of the cube **c**.

with a sigmoid function. The collection of sigmoid functions is then used to represent the interface and calculate the interface positions as well as the isoconcentration surfaces. Fifth, the profile extracted from the Voronoi grid of the entire cube is used to create a model structure with the known crystal structure of SiGe and a pseudo-random distribution of Si and Ge atoms in the x-y plane, enforcing the same profile along the depths direction as given by the Voronoi grid and the same percentage of atoms in the volume as expected from the detection efficiency of the Atom Probe (here: 80 % detection efficiency of the LEAP 5000XS). These model structures interface are then compared to the measurement results. All data treatment is done in Python 3.9 using numpy 1.20.3 and scipy 1.6.3.

### B. EXTRACTION OF THE CUBES AND VORONOI TESSELLATION

The cubes are manually extracted from the reconstructed volume as exemplary shown in Fig. 6.13 **a**-**b**). After a cube containing the quantum well with the approximate size of an electrically defined quantum dot (~ 30x30x20 nm) is extracted a Voronoi tessellation is performed on the point cloud representing APT data inside the cube. A result of such a tessellation in exemplary shown in Fig. 6.13 **c**).

### C. CONSTRUCTION OF THE INTERFACE

Interfaces are constructed based on the Voronoi tessellated data sets. The process is depicted in Fig. 6.14. A grid is created in the x,y-plane of the tessellated data set (Fig. 6.14 **a**-**b**). For each cell of the grid a one-dimensional profile along the z-axis is generated using the tessellation. As opposed to "regular" APT data [217] where profiles are created utilizing small bins along the z-axis and concentrations are then calculated from the ions/atoms within the bin (Ref. [228] Chapter 7), the profiles on the tessellated data are created by a set of cutting planes. The process works by cutting the tessellation at each depth and use every ion/atom whose volume is cut as part of the plane and hence have it contribute to the concentration measured within that plane and at that depth.This can be viewed as a smoothing operation that spreads out the detected ions/atoms to a finite volume.

Each x,y-cell (typically 3x3 nm wide spaced 1 nm apart and hence partially overlapping) generates a profile and is then fitted using sigmoid function [74] as shown in Fig. 6.14 **c**). The sigmoid functions are then used to represent the interface in the following way:

- The inflection point of the sigmoid represents the position of the interface in each cell (Fig. 6.14 **d**)
- Isoconcentration surfaces (Ref. [228] Chapter 6.3.2) are created by plotting the position where the sigmoid of each cell reaches the respective concentration

Fig. 6.15 and 6.16 show examples of the interface positions maps and isoconcentration surface maps generated in this way for the top and bottom interfaces of a QW A and a QW B sample. Note, that the data can now readily be used to calculate the average roughness and root mean square roughness in the usual way [229].

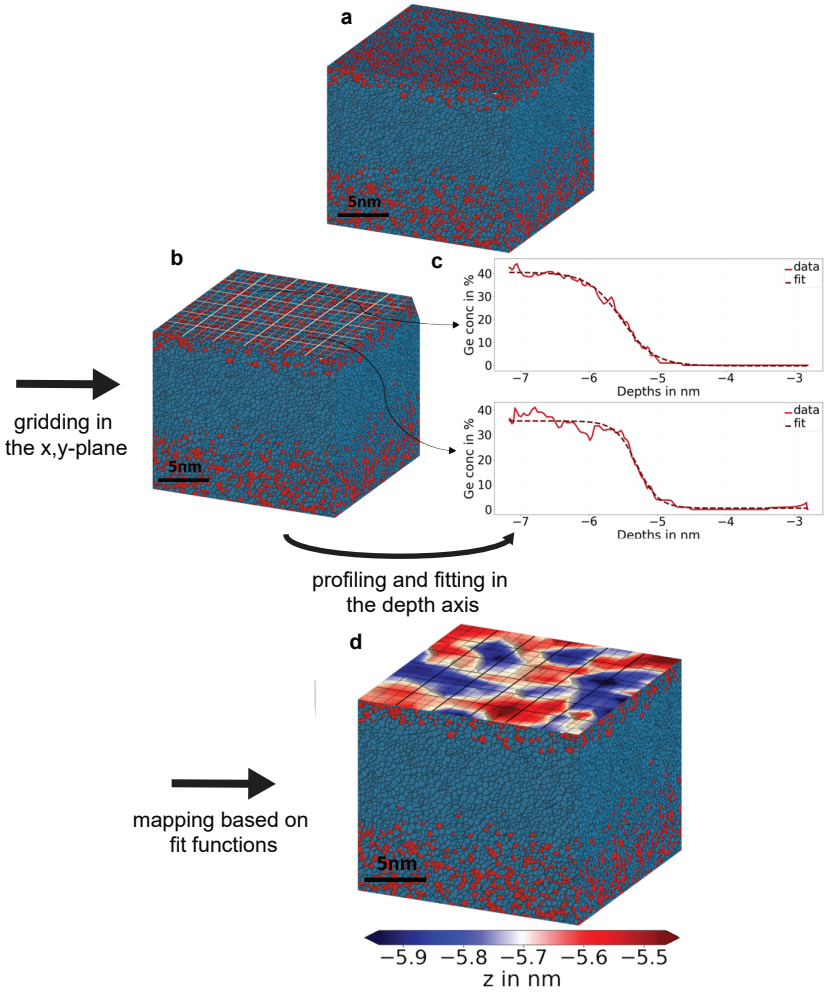


Figure 6.14: Creation of a map from the Voronoi tessellated cube (**a**) by applying an x,y-grid (**b**) and fitting of profiles along z-axis with a sigmoid function in each cell **(c)**. The profiles can then be used to calculate the position of e.g. the 25 % Germanium isoconcentration surface **(d)**.

### D. GENERATING MODEL DATA

Model data are generated based on the known crystal properties of $Si_{66.5}Ge_{33.5}$. A crystal of the same size as the cubes extracted from the data (~ 30x30x20 nm) is generated digitally and then 20 % of the atoms in the crystal are pseudo-randomly removed to account for the detection efficiency of the LEAP5000XS system used in the APT analysis.

Along the depth axis of the cube the average measured APT profile of the Si and Ge concentration of QW A and QW B as shown in Fig. 6.2**c** is enforced. The result of the generation of such a cube for QW A and the comparison of the depth profile extracted from a cube of QWA and QW B to the average profile of QW A and QW B respectively

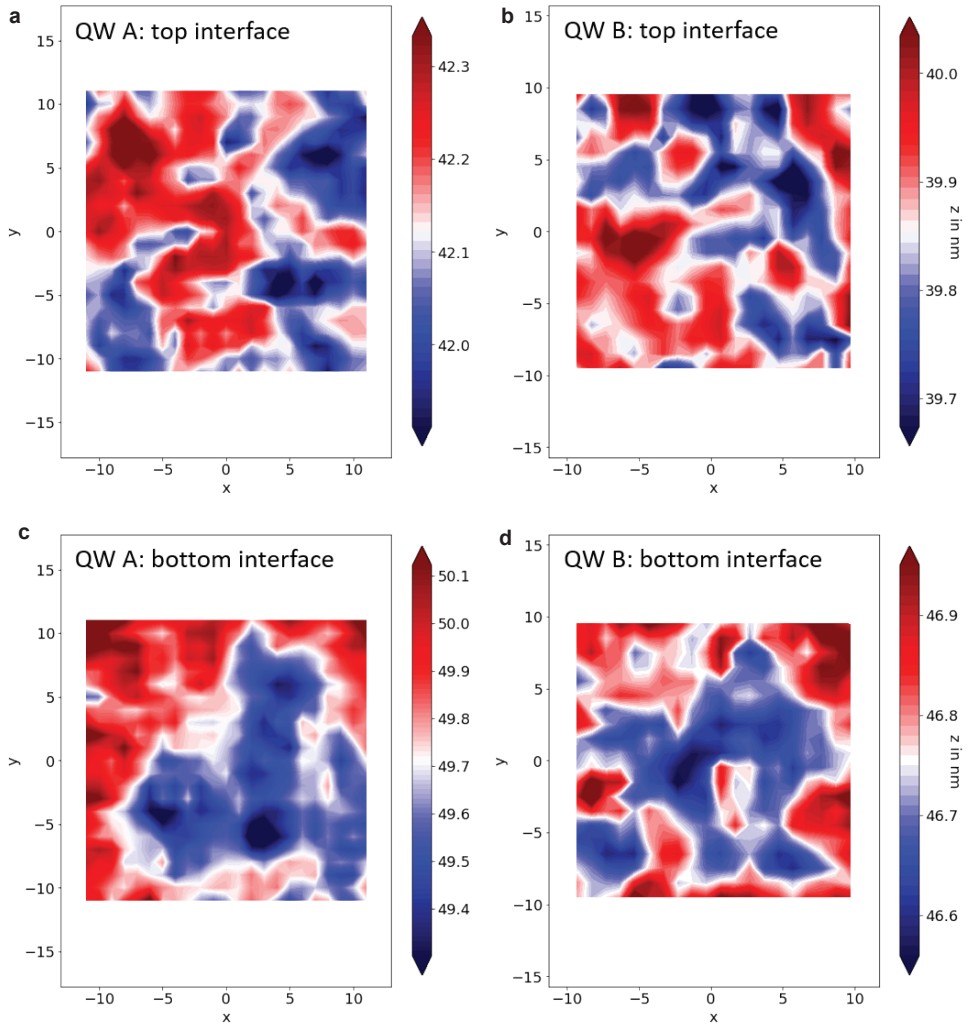


Figure 6.15: Examples of position maps of top (**a**, **b**) and bottom (**c**, **d**) Germanium interfaces for both Quantum wells A and B. For each cell the depth plotted on the map is extracted from inflection point the sigmoid fit to the profile extracted from the cell (Fig. 6.14 **b**-**c**).

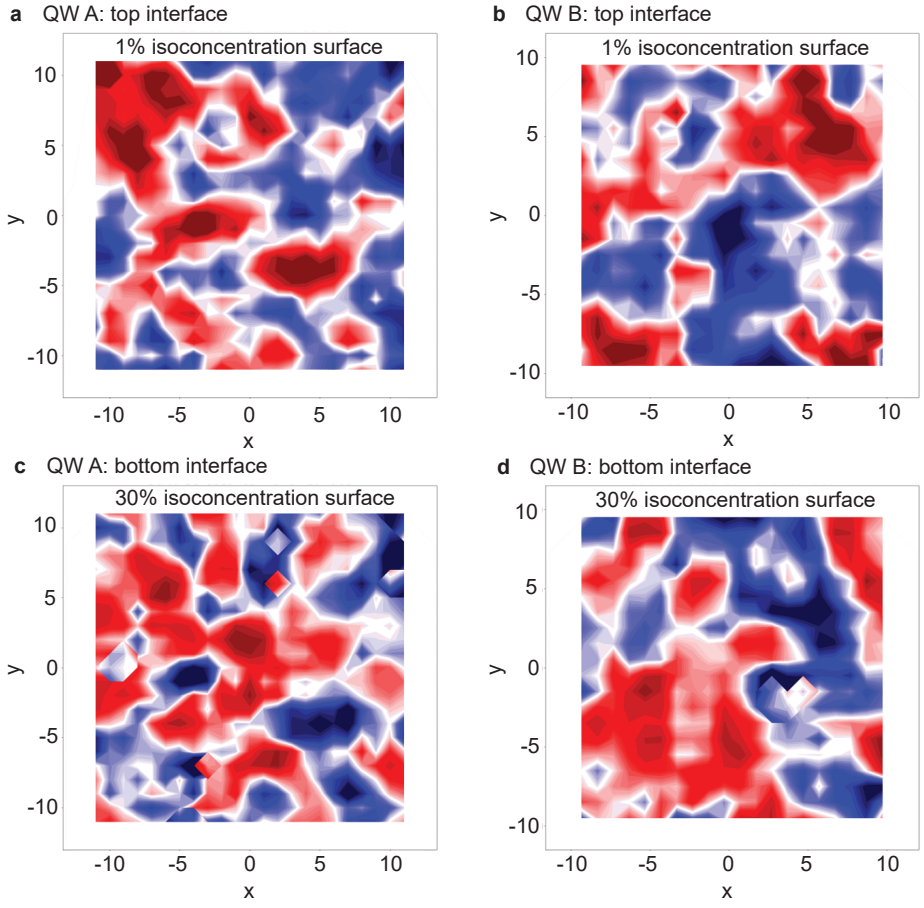


Figure 6.16: Example of Germanium isoconcentration surfaces or the top (**a**, **b**) and bottom (**c**, **d**) interfaces of both Quantum Wells a and B. The plots reported here show one particular isosurface, 1% in **a**, **b** and 30% in c,d. Animated short clips provided as Supplementary Movies in Ref [73] show the evolution across the interfaces of each isoconcentration surfaces, from 1-30 % Ge. As before the depth for each map can be extracted from the sigmoid fits to the profile in each cell.

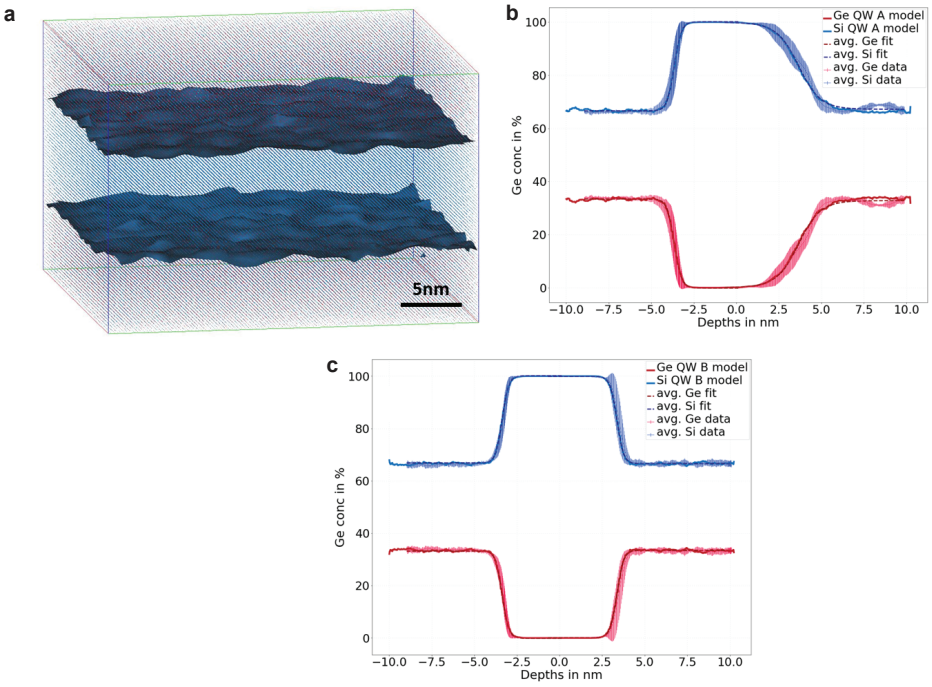


Figure 6.17: Example of a crystalline cube of QW ( **a**) and a comparison of the average profiles of the measured quantum wells (see Fig. 6.2**c**) and profiles from a generated cube of Quantum Well A (**b**) and Quantum Well B (**c**).

are shown in Fig. 6.17. In Fig. 6.18 interface position maps of these model structures are shown. They should be compared to Fig. 6.15 where the same maps are extracted from measured data sets. The root mean square roughness as measured from the model is compared to the data measured from the APT data in Fig. 6.2.

Note: there is an animation in the file Supplementary_ Movie_1.m4v in Ref. [73] which shows for the top interface of quantum well B (for increasing Ge concentration) the deviation of each isosurface tile position from the isosurface's average position. There we benchmark the experimental data from our APT analysis (at each frame of the animation) against average and min-max range covered by 100 random models.

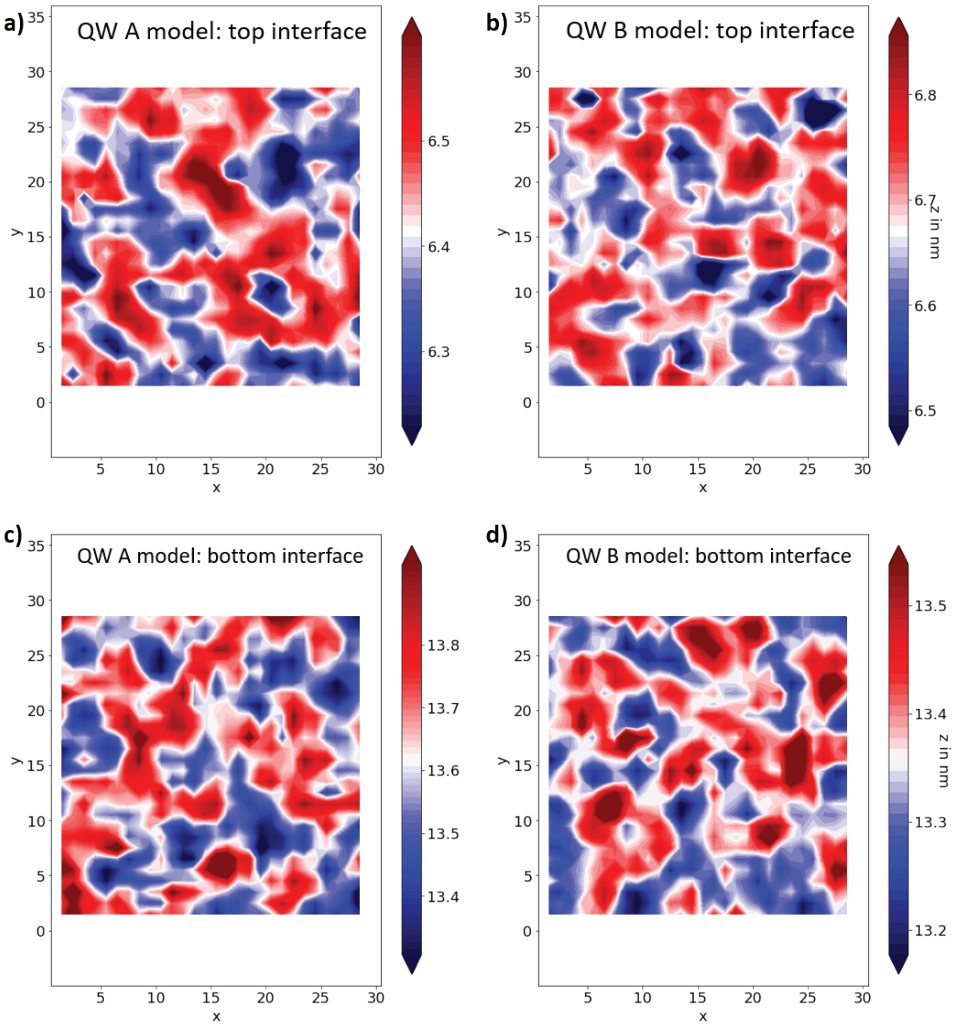


Figure 6.18: Examples of position maps of top (**a**, **b**) and bottom (**c**, **d**) Germanium interfaces for model data sets of both Quantum wells A and B. As in Fig. 6.15 the depth plotted on the map is extracted from the inflection point of the sigmoid fit for the profile along the depth axis generated in each cell (Fig. 6.14 **b**-**c**).

### E. ATOMIC STEPS, QUANTUM WELL WIDTH, AND BOTTOM INTERFACES

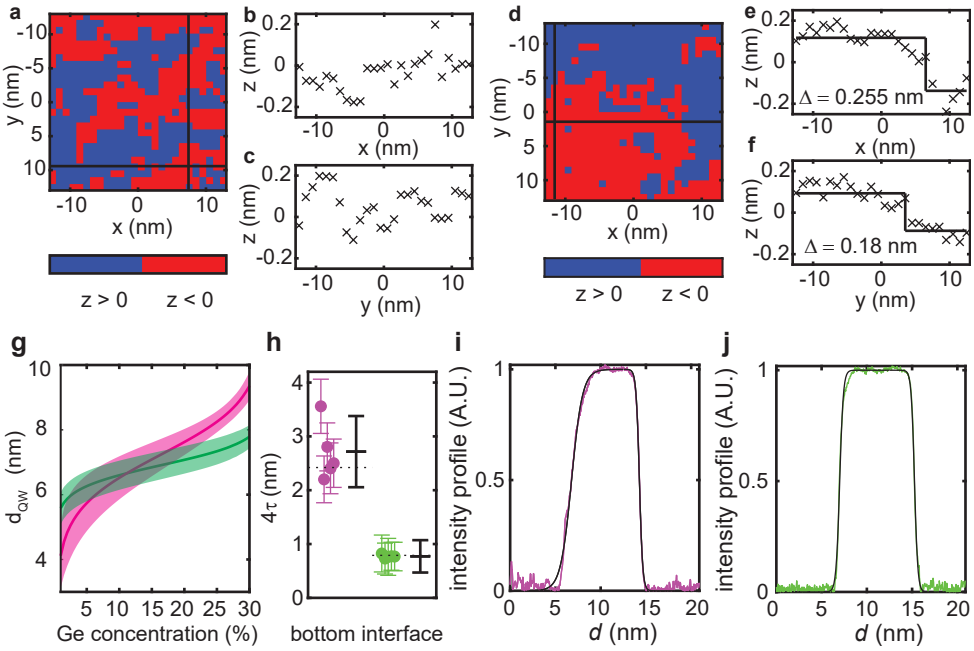


Figure 6.19: **a** 10% isoconcentration surface from a Stack A sample without step. Blue areas are below and red areas above the average height (defined as $z = 0$) of the isoconcentration surface. The black lines are the positions of the line cuts in **b** and **c**. **b** line cut along the x direction of the isoconcentration surface. in **a**. **c** line cut along the y-direction of the isoconcentration surface. The z-position randomly oscillates around the mean value. **d** 10% isoconcentration surface from a Stack A sample with clear spatial division of the blue and red areas. The black lines are the positions of the line cuts in **e** and **f**. **e** line cut along the x-direction of **d**. A step with height $\Delta = 0.255$ nm occurs at $x = 7$ nm, corresponding to approximately 2 monoatomic layers. The black line represents the Heavyside step function with the highest $C$ and the step height is determined by taking average z-position of the line cut before and after the step. **f** line cut along the y-direction of **c**. A step with $\Delta = 0.18$ nm occurs at $x = 3$ nm, corresponding to approximately 1.5 monoatomic layers. The black line represents the average z-position before and after the step. **g**, Average width of quantum well A (magenta line) and B (green line) as a function of the Ge concentration of the isoconcentration surfaces. Shaded areas represent the standard deviation of the quantum wells. **h**, Statistical analysis of the bottom $4\tau$ interface widths derived from the fitting the data for quantum well A (magenta) and quantum well B (green). Black crosses are the mean and standard deviation for data from the different APT samples, highlighting the uniformity of the interfaces. **i**, **j**, HAADF-STEM intensity profile for stack A and B (magenta and green line, respectively) along the heterostructure growth direction (see TEMs in the main section). The black lines are fits of the data in the interface regions, using a sigmoid function.

To evaluate the presence of atomic steps from isoconcentration surfaces, we consider one-dimensional line cuts along the x- and y-axis of an isosurface. If a line cut crosses an atomic step along the isosurface, the line cut should resemble a Heavyside step function $H$:

$$H(x - x_s) = h_0 + \begin{cases} -a/2, & \text{for } x < x_s. \\ a/2, & \text{for } x \geq x_s. \end{cases} \tag{6.6}$$

where $a$ is the step height, $x_s$ is the step position and the offset $h_0$. To quantify the resem-

blance between a line cut and the step function, we determine the correlation coefficient $C$ between the two with:

$$C = \frac{\sum_k (z_k - \bar{z})(h_k - \bar{h})}{\sqrt{\sum_k (z_k - \bar{z})^2}\sqrt{\sum_k (h_k - \bar{h})^2}} \tag{6.7}$$

where $z_k$ are the z-values of the line cut, $\bar{z}$ is the mean value of the line cut, k is the index of the, $h_k$ are the values of the step function, and $\bar{h}$ the mean value of the step function. If $C \geq 0.75$ we consider the linecut to represent a step. We subsequently can determine $a$ by taking the difference between the two plateaux $\Delta = \bar{z}_{k+} - \bar{z}_{k-}$, where $\bar{z}_{k+}$ and $\bar{z}_{k-}$ are the average z-position before and after $x_s$, respectively.

### F. SIMS AND CROSSHATCH PATTERN

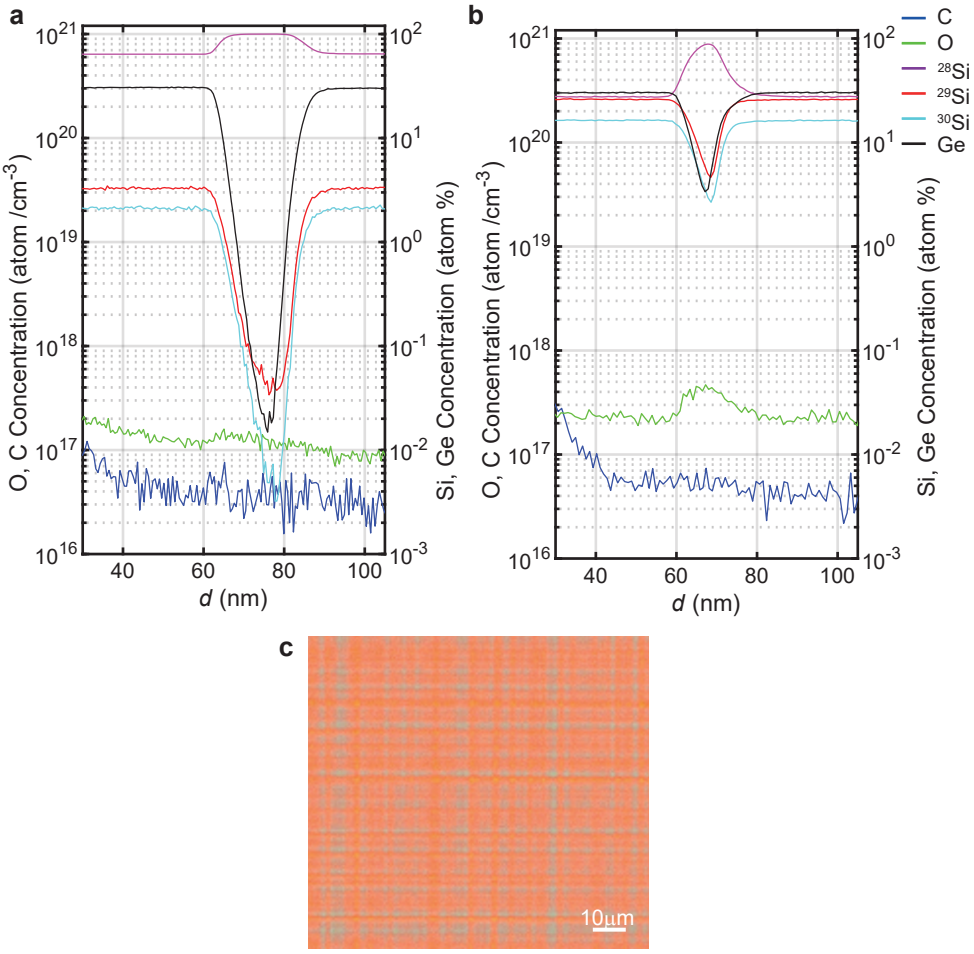


Figure 6.20: **a**, **b**, Depth concentration SIMS profile of quantum well A and quantum well B respectively. Analyzed elements are $^{28}$Si (red), $^{29}$Si (blue), $^{30}$Si (purple), Ge (black), oxygen (green) and carbon (blue). In quantum well A both carbon and oxygen concentrations are below their respective detection limits of $3 \times 10^{16}$ cm$^{-3}$ and $1 \times 10^{17}$ cm$^{-3}$. In quantum well A only carbon is below the detection limits, while there is a residual oxygen content of $4 \times 10^{17}$ cm$^{-3}$ in the quantum well. **c** typical cross-hatch pattern from the surface of the wafers.

# 7

# WAFER-SCALE LOW-DISORDER 2DEG IN $^{28}$SI/SIGE WITHOUT AN EPITAXIAL SI CAP

*We grow $^{28}$Si/SiGe heterostructures by reduced-pressure chemical vapor deposition and terminate the stack without an epitaxial Si cap but with an amorphous Si-rich layer obtained by exposing the SiGe barrier to dichlorosilane at 500 °C. As a result, $^{28}$Si/SiGe heterostructure field-effect transistors feature a sharp semiconductor/dielectric interface and support a two-dimensional electron gas with enhanced and more uniform transport properties across a 100 mm wafer. At $T = 1.7$ K we measure a high mean mobility of $(1.8 \pm 0.5) \times 10^5$ cm$^2$/Vs and a low mean percolation density of $(9 \pm 1) \times 10^{10}$ cm$^{-2}$. From the analysis of Shubnikov–de Haas oscillations at $T = 190$ mK we obtain a long mean single particle relaxation time of $(8.1 \pm 0.5)$ ps, corresponding to a mean quantum mobility and quantum level broadening of $(7.5 \pm 0.6) \times 10^4$ cm$^2$/Vs and $(40 \pm 3)$ μeV, respectively, and a small mean Dingle ratio of $(2.3 \pm 0.2)$, indicating reduced scattering from long range impurities and a low-disorder environment for hosting high-performance spin-qubits.*

This chapter has been published in Davide Degli Esposti, Brian Paquelet Wuetz, Viviana Fezzi, Mario Lodari, Amir Sammak, and Giordano Scappucci, Wafer-scale low-disorder 2DEG in $^{28}$Si/SiGe without an epitaxial Si cap, Appl. Phys. Lett. **120**, 184003 (2022) [230]

## 7.1. INTRODUCTION

Strained $^{28}$Si/SiGe heterostructures are a compelling platform for scalable qubit tiles based on gate-defined quantum dots.[181, 177] In these $^{28}$Si buried quantum wells, electron spins experience a quiet electrical and magnetic environment. The electronically noisy semiconductor/dielectric interface is far away, separated from the quantum well by a SiGe epitaxial barrier, and the nuclear spins have been removed by isotopic enrichment. Continuous advances in the material science of $^{28}$Si/SiGe and improved device fabrication have enabled quantum logic with spin qubits crossing the surface code threshold,[115, 114, 231] coherent coupling of two electron spins at a distance via virtual microwave photons,[232] and CMOS-based cryogenic control of quantum circuits[51]. In the mainstream approach to quantum dot fabrication, the last step in the heterostructure growth cycle comprises the heteroepitaxial deposition of a thin epitaxial Si cap on the SiGe barrier [225]. This is to avoid the formation of low-quality Ge-based oxides upon exposure of SiGe to air. After the Si cap deposition, a high-$\kappa$ dielectric is deposited *ex-situ* and at low-temperature ($\approx 300\,^{\circ}$C) to insulate the gate from the buried and undoped quantum well. This low-temperature process preserves the strain in the quantum well but induces large concentrations of impurities at the critical semiconductor/dielectric interface. These impurities can influence the electrostatic confining potential landscape induced by the gates, leading to the formation of unintentional quantum dots,[233] and are a source of charge noise limiting qubit performance.[48, 111] While efforts have focused on achieving uniform and high-purity $^{28}$Si quantum wells with sharp interfaces,[73, 212, 190] now more attention is needed to optimize the step which terminates the heterostructure deposition cycle and has a critical role in defining the semiconductor/dielectric interface.



In this letter, we explore $^{28}$Si/SiGe heterostructures terminated by exposure to dichlorosilane (DCS) gas at a temperature well below the threshold for epitaxial growth of Si. By avoiding the growth of an epitaxial Si cap altogether, we obtain $^{28}$Si/SiGe heterostructure field effect transistors (H-FETs) with a sharp semiconductor/dielectric interface. We show that the $^{28}$Si quantum well supports a two-dimensional electron gas with less disorder and improved quantum transport properties compared to heterostructures with an epitaxial Si cap.

## 7.2. HETEROSTRUCTURE

Figure 7.1**a** illustrates the workflow to fabricate $^{28}$Si/SiGe H-FETs. We grow $^{28}$Si/SiGe heterostructures on 100 mm Si(001) wafers using an Epsilon 2000 (ASMI) reduced-pressure chemical vapor deposition reactor. We use isotopically-enriched $^{28}SiH_4$ for growing the $^{28}$Si quantum well (residual $^{29}$Si concentration of 0.08%[141, 51, 115]) and DCS ($H_2SiCl_2$) and $GeH_4$ for all other layers. The heterostructure comprises a 3 µm step-graded $Si_{1-x}Ge_x$ layer (final $x \simeq 0.3$), a 2.5 µm $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer, a 8 nm tensile-strained $^{28}$Si quantum well and a 30 nm $Si_{0.7}Ge_{0.3}$ barrier[1] and in the SiGe barrier is $\simeq 4\times10^{17}$ cm$^{-3}$. To achieve sharp interfaces and minimize Si/Ge interdiffusion at the quantum well-barrier interface[73], the temperature is decreased from 750 °C for growing the quantum well to

[1] A typical secondary ions mass spectrometry of our heterostructures is reported in Fig. S13 of Ref. [73]. The oxygen concentration in the $^{28}$Si quantum well is $\simeq 4\times10^{17}$ cm$^{-3}$

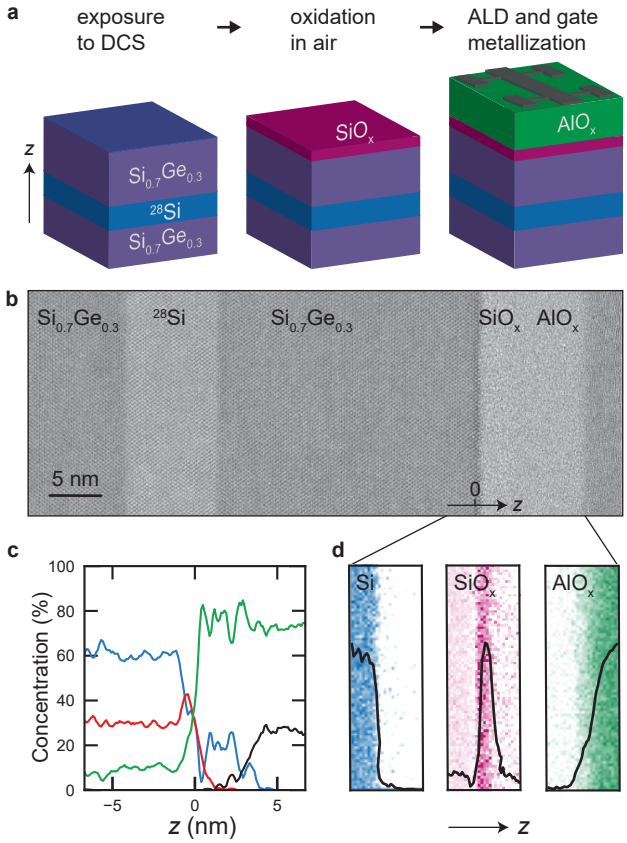


Figure 7.1: **a** Schematics of the $^{28}$Si/SiGe heterostructure and formation of the dielectric interface in a Hall-bar heterostructure field effect transistor. $z$ indicates the heterostructure growth direction. The heterostructure is terminated by exposure to dichlorosilane (DCS) gas at a temperature below the threshold for growing an epitaxial Si cap and the dielectric stack comprises a $SiO_x$ layer formed by exposure of the heterostructure to air at room temperature and an $AlO_x$ layer formed by atomic layer deposition (ALD). **b** BF-STEM image of the active layers of the $^{28}$Si/SiGe heterostructure field effect transistor showing, from left to right, the $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer layer, the tensile-strained $^{28}$Si quantum well, the $Si_{0.7}Ge_{0.3}$ barrier, followed by the $SiO_x/AlO_x$ dielectric stack. **c** Electron energy loss spectroscopy (EELS) semi-quantitative concentration depth profiles across the semiconductor/dielectric interface for Si (blue), Ge (red), O (green), and Al (black). **d** 15 nm×45 nm wide 2D maps by EELS using low-energy edges to recognize differences between the different bonding states: Si (blue), $SiO_x$ (magenta), and $AlO_x$ (green). We do not detect any Cl or H signal above the background noise in our EELS data.

625 °C for the barrier. We now introduce a major difference compared to our previous experiments. In Refs. [171, 51, 115, 73]) we deposited a thin epitaxial Si cap at 675 °C using DCS. Here we reduce the substrate temperature to 500 °C, below the desorption temperature of chlorine from the surface (600–650 °C),[234, 235] under the same conditions of DCS flow and pressure. According to literature[236, 237, 238, 239, 240, 241, 242], we expect that exposure to DCS at 500 °C essentially suppresses crystalline growth but creates an amorphous Si-rich layer on $Si_{0.7}Ge_{0.3}$. After terminating the deposition cycle

with this step, the heterostructure is removed from the growth reactor and a native oxide is formed upon exposure to air at room temperature. We identify the native oxide as $SiO_x$ based on the chemical analysis in Fig. 7.1**c**,**d**. Then, we fabricate Hall-bar shaped H-FETs using the process described in Ref. [73]. In short, the process comprises the implantation of ohmic contacts and rapid thermal annealing at 700 °C, the atomic layer deposition at 300 °C of a 10 nm $Al_2O_3$ dielectric layer on the $SiO_x$, and the final deposition of a Hall-bar shaped metallic gate, electrically insulated from the heterostructure by the $SiO_x/Al_2O_3$ dielectric stack.

Figure 7.1**b** shows a bright-field scanning transmission electron microscopy (BF-STEM) image of the heterostructure and of the dielectric stack under the gate stack at the end of the H-FET fabrication process. The Si quantum well is uniform, without extended defects, and is characterized by sharp top and bottom interfaces to the $Si_{0.7}Ge_{0.3}$ layers, in agreement with our previous reports [51, 115, 73]. The semiconductor/dielectric interface is similarly sharp, highlighted by the perfect atomically sharp semiconductor surface as imaged by BF-STEM. Two distinct amorphous layers, which we identify as the $SiO_x$ and $AlO_x$ layers, appear on the dielectric side of the interface. We gain insights over the nature of the semiconductor/dielectric interface and of the dielectric stack by performing electron energy loss spectroscopy (EELS). In Fig. 7.1**c** we show the semi-quantitative concentration profiles using the Si-K (1839-2084 eV), Al-K (1560-1700 eV), O-L (532-660 eV), and Ge-L (1220-1400 eV) high energy edge. The Si (blue) and Ge (red) concentration profiles decrease together whilst the oxygen (green) signal is increasing. We deduce that oxidation of the $Si_{0.7}Ge_{0.3}$ barrier with on top an amorphous Si-rich layer results in a sharp $SiGe/SiO_x$ semiconductor/dielectric interface. This is confirmed by the minor Ge pile-up on the semiconductor side of the interface,[243, 244] which appears as a dark line in BF-STEM [Fig. 7.1**b**] and suggests that the top of the single crystalline $Si_0.7Ge_{0.3}$ barrier has been oxidized and that Ge oxides at the interface are absent[245, 246]. Furthermore, the Al signal (black line) rises after the Si signal from $SiO_x$ has trailed, indicating that the dielectric stack retains the two distinct $SiO_x$ and $AlO_x$ layers.

In Fig. 7.1**d** we show the chemical mapping by EELS of Si (blue), $SiO_x$ (magenta), and $AlO_x$ (green) along and across the semiconductor/dielectric interface, together with the intensity profiles. To recognize differences between the different bonding states, we use the low-energy Si-L edge (96.3-100.8 eV) for the semiconductor phase and a shifted Si-L edge (101.4-107.1 eV) for the oxide phase, and Al-L (73.8-79.5 eV) for the oxided Al phase. The $SiGe/SiO_x$ interface is sharp throughout the image, whereas the $SiO_x/AlO_x$ interface shows some interdiffusion. By fitting the intensity profiles with exponential functions[247] we characterize the size of the interfaces with the leading (towards the surface) and trailing (from the surface) exponential slopes $\lambda_L$ and $\lambda_T$. We find $\lambda_L^{\mathrm{Si}} = (1.0 \pm 0.1)$ nm and $\lambda_T^{\mathrm{SiO_x}} = (0.8 \pm 0.1)$ nm. Conversely, we find $\lambda_L^{\mathrm{SiO_x}} = (1.9 \pm 0.1)$ nm and $\lambda_T^{\mathrm{AlO_x}} = (3.1 \pm 0.2)$ nm. Overall, the transition from epitaxial SiGe to amorphous $SiO_x$ interface is sharper than the transition between $SiO_x$ and $AlO_x$, pointing to a degree of intermixing at the latter interface.

## 7.3. HALL CHARACTERIZATION AT 1.7 K

We characterize the H-FETs by magnetotransport measurements at a temperature of 1.7 K and 190 mK[2] in refrigerators equipped with cryo-multiplexers.[155] With this approach, we measure multiple devices from a wafer in the same cool-down. The devices are operated in accumulation mode, in which electrons populate the undoped $^{28}$Si quantum well by applying a positive DC gate voltage ($V_G$). We measure the longitudinal and transverse components of the resistivity tensor, $\rho_{xx}$ and $\rho_{xy}$, by using standard four-probe lock-in techniques at fixed AC source-drain bias of 100 μV. We calculate the longitudinal $\sigma_{xx}$ and transverse $\sigma_{xy}$ conductivity via tensor inversion. We measure electron density ($n$) and mobility ($\mu$) with the classical Hall effect at low perpendicular magnetic field $B$.

Figure 7.2**a** shows for a typical device the turn-on and pinch-off source-drain current $I_{SD}$ as a function of increasing and decreasing $V_G$, respectively. Above a threshold voltage ($V_G$ = 350 mV), the current starts flowing in the channel and increases monotonically. If the gate voltage is operated within the operational gate voltage range $\Delta V_G$ (red curve), $I_{SD}$ is stable and the threshold and pinch-off voltages overlap. At higher $V_G$, $I_{SD}$ saturates due to charge build-up at the semiconductor/dielectric interface, triggering hysteresis and, consequently, a shift in pinch-off voltage. As shown in Fig. 7.2**b**, if $V_G$ is swept within the operational gate voltage range, $n$ increases linearly with $V_G$ up to $6 \times 10^{11}$ cm$^{-2}$. From the slope $\frac{dn}{dV_G}$ we derive an effective capacitance per unit area $C \simeq 205$ nF/cm$^2$ using the relationship $C = e\frac{dn}{dV_G}$.[155]. This capacitance characterizes the parallel-plate capacitor where the 2DEG in the $^{28}$Si quantum well and the metallic top gate are insulated by a SiGe/$SiO_x$/$AlO_x$ dielectric stack. Figure 7.2**c** shows the density-dependent mobility measured in the same density range as in Fig. 7.2**b**.

In the low density regime ($n \leq 3 \times 10^{11}$ cm$^{-2}$), the mobility rises steeply due to the increasing screening of Coulomb scattering from remote charged impurities located at semiconductor/dielectric interface.[121] At higher density ($n \geq 5 \times 10^{11}$ cm$^{-2}$), the mobility approaches saturation at a value above $2.5 \times 10^5$ cm$^2$/Vs. This weaker density-dependence is typical of a high-quality 2DEG, where the maximum mobility is limited by short-range scattering from impurities within or near the quantum well.[123, 122, 155]

In Fig. 7.2**d**–**f** we plot the distributions of the maximum electric field ($E_z^{max}$), the percolation density ($n_p$), and the mobility at high density for heterostructures terminated with an amorphous Si-rich layer (blue) and, as a benchmark, for heterostructures with an epitaxial Si cap (red). These three metrics are obtained from the analysis of measurements in Fig. 7.2**a**–**c**, repeated on multiple H-FETs on dies that are randomly selected from different locations across the 100 mm wafer. $E_z^{max}$, calculated as $C\Delta V_G/\epsilon_0\epsilon_r$, where $\epsilon_r = 11.68$ is the dielectric constant of Si, indicates the maximum electric field that we can apply to the quantum well in the H-FETs before hysteresis. Large $E_z^{max}$ are desirable for device stability, increased tunability, and large valley splitting.[67, 119, 190, 73] $n_p$ characterizes disorder in low density regime, relevant for quantum dot operation, and

[2] $T$ = 190 mK is the electron temperature obtained by fitting Coulomb blockade peaks (see figure 7.5) measured on quantum dot devices[51] fabricated on a similar heterostructure. The electron temperature is higher than the temperature of 70 mK measured by a thermometer located on the mixing chamber of the dilution refrigerator

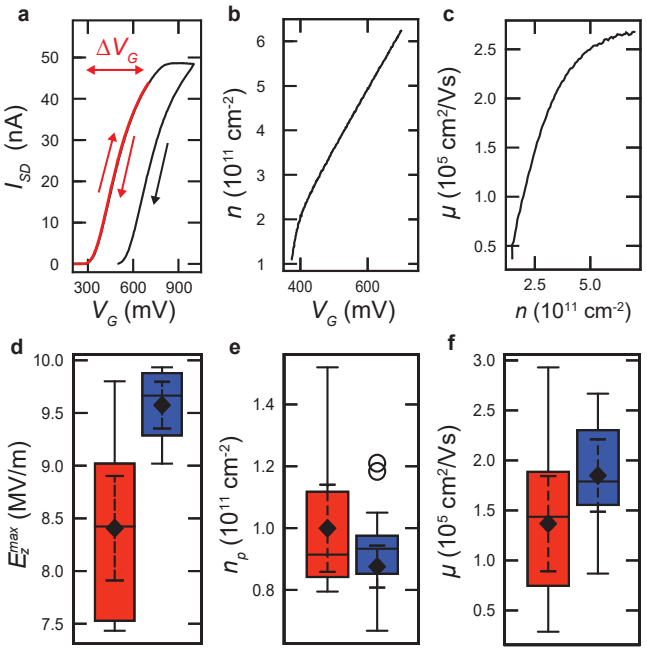


Figure 7.2: **a** Source-drain current $I_{SD}$ measured at $T = 1.7$ K as a function of gate voltage $V_G$ for a typical Hall bar heterostructure field effect transistor (H-FET). The operational gate voltage range $\Delta V_G$ indicates the range over which an $I_{SD}$-$V_G$ curve (red line) can be measured repeatedly without hysteresis and drift. **b** Density $n$ as a function of gate voltage $V_G$ and **c** electron mobility $\mu$ as a function of $n$ measured within the operational gate voltage range. **d**, **e**, **f** Distributions of maximum electric field applicable before hysteresis $E_z^{max}$, percolation density $n_p$, and $\mu$ measured at $n = 6\times10^{11}$ cm$^{-2}$ for heterostructures terminated by a Si-rich amorphous layer obtained exposure to DCS at 500 °C (blue, 14 H-FETs measured) and for heterostructures with an epitaxial Si cap grown by exposure to DCS at 675 °C (red, 16 H-FETs measured). Quartile box plots, mode (horizontal line), means (diamonds), outliers (circles), and 99% confidence intervals of the mean (dashed whiskers) are shown.



is obtained by fitting the density-dependent $\sigma_{xx}$ to percolation theory.[125] Finally, the mobility at high density is a probe for disorder arising from within or nearby the quantum well.[121, 122, 123] Overall, H-FETs perform better when the SiGe barrier is terminated with an amorphous Si-rich layer. We measure a 9% increase in mean $E_z^{max}$, 7% decrease in mean percolation density, and a 40% increase in mean mobility. Most importantly, we observe a reduction in the spread of $E_z^{max}$, $n_p$, and $\mu$ of $\simeq$ 300%, $\simeq$ 200%, and $\simeq$ 30% respectively, pointing to an increased uniformity on a 100 mm wafer scale.

We further characterize disorder in the $^{28}$Si/SiGe heterostructure at 190 mK by measuring the single-particle relaxation time $\tau_q$[248] in the quantum Hall regime. From $\tau_q$ we derive the quantum mobility $\mu_q = e\tau_q/m^*$, where $e$ is the elementary charge and $m^*$ is the effective mass, and the quantum level broadening of the momentum eigenstates $\Gamma = \hbar/2\tau_q$, here $\hbar$ is the reduced Planck constant. $\mu_q$, associated with $\tau_q$, is influenced by all scattering events and is different from the mobility $\mu = e\tau_t/m^*$, where the scattering time $\tau_t$ is unaffected by forward scattering. Therefore $\tau_q$ and $\mu_q$ qualify the disorder in the heterostructure more comprehensively than $\tau_t$ and $\mu$.

Figure 7.3**a** shows for the H-FET with the highest mobility a measurement of $\rho_{xx}$ plotted for clarity against the Landau level filling factor $\nu = hn/eB$, where $h$ is the Plank constant. This measurement was performed at fixed density $n = 4.75 \times 10^{11}$ cm$^{-2}$ by keeping $V_G$ constant and sweeping $B$. Onset of Shubnikov–de Haas oscillation, Zeeman splitting, and valley splitting occurs at 0.125, 0.43, and 1.15 T, respectively, corresponding to $\nu = 152$, 42 and 17. The observation of Shubnikov–de Haas oscillations, Zeeman and valley splitting at these high filling factors indicates a very low level of disorder.[249] Figure 7.3**b** shows the normalized oscillation amplitude $\Delta\rho_{xx}/\rho_0 = (\rho_{xx} - \rho_0)/\rho_0$ in the low magnetic field regime after polynomial background subtraction. $\rho_0 \simeq 63\ \Omega$/square is the longitudinal resistivity at zero magnetic field from which we extract a mobility of $2.7\times10^5$ cm$^2$/Vs. We estimate $\tau_q = (7.4\pm0.1)$ ps from a fit of the Shubnikov-de Haas oscillation envelope to the function $\Delta\rho_{xx} = 4\rho_0\chi(T)\exp(-\pi/\omega_c\tau_q)$, where $\chi(T) = (2\pi^2 k_B T/\hbar\omega_c)/\sinh(2\pi^2 k_B T/\hbar\omega_c)$. Here $T = 190$ mK, $k_B$ is the Boltzmann constant, and $\omega_c$ is the cyclotron frequency calculated using a fixed $m^* = 0.19\, m_e$ [250, 249]. From $\tau_q$ we derive $\mu_q = (6.8 \pm 0.1) \times 10^4$ cm$^2$/Vs, $\Gamma = (44 \pm 1)$ μeV, and find a Dingle ratio

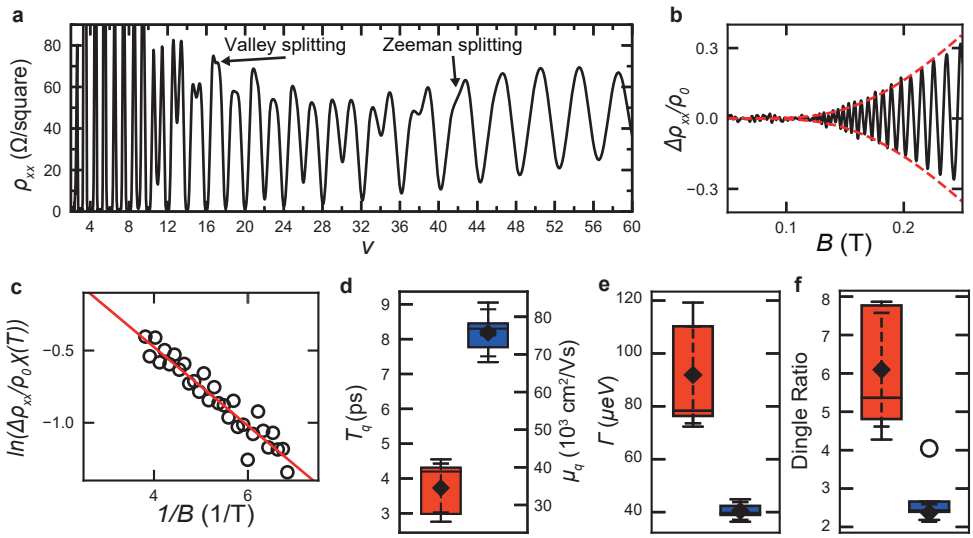


Figure 7.3: **a** Longitudinal resistivity $\rho_{xx}$ measured at $T = 190$ mK as a function of Landau level filling factor $\nu$. These measurements are performed at fixed $n = 4.75 \times 10^{11}$ cm$^{-2}$ while sweeping the perpendicular magnetic field $B$. Spin and valley degenerate Landau levels correspond to $\nu = 4k$ ($k$ = 1,2,3...), Zeeman split levels to $\nu = (4k\text{-}2)$, whereas valley split levels correspond to odd integer filling factors $\nu$. Arrows indicate the filling factors at which Zeeman spin splitting and valley splitting are resolved. **b** Normalized resistivity oscillation amplitude (black curve) as a function of $B$ after polynomial background subtraction. The arrow indicates the magnetic field at which Shubnikov–de Haas oscillations are resolved. The red dashed line is the theoretical fit of the oscillations envelope from which we extract $\tau_q$. **c** Dingle plot (open circles) from the first twenty most resolved resistivity oscillation maxima and minima and theoretical curve (solid red line) computed using $\tau_q$ from the analysis in **b**. **d**, **e**, **f** Distributions of $\tau_q$, $\mu_q$, Γ, and Dingle ratio measured at $n = (5-6) \times 10^{11}$ cm$^{-2}$ for heterostructures terminated by a Si-rich amorphous layer obtained exposure to DCS at 500 °C (blue, 5 H-FETs measured) and for heterostructures with an epitaxial Si cap grown by exposure to DCS at 675 °C (red, 7 H-FETs measured). Quartile box plots, mode (horizontal line), means (diamonds), outliers (circles), and 99% confidence intervals of the mean (dashed whiskers) are shown.

$\tau_t/\tau_q \simeq 3.8$. The Dingle plot of Fig. 7.3**c** highlights the high number of oscillation maxima and minima used in the fitting procedure.

In Fig. 7.3**d–f** we plot the distributions for $\tau_q$ (and $\mu_q$), $\Gamma$, and the Dingle ratio $\tau_t/\tau_q$, measured in the high density regime ($n = (5-6) \times 10^{11}$) cm$^{-2}$). As in Fig. 7.2**d–f**, we consider heterostructures terminated with an amorphous Si-rich layer (blue, 5 H-FETs measured) and heterostructures with an epitaxial Si cap (red, 7 H-FETs measured). Heterostructures with an amorphous Si-rich layer have a mean $\tau_q$ of $(8.1 \pm 0.5)$ ps, and consequently a mean $\mu_q$ of $(7.5 \pm 0.6) \times 10^4$ cm$^2$/Vs and $\Gamma$ of $(40 \pm 3)$ μeV, representing a $\simeq 2\times$ improvement compared to heterostructures with an epitaxial Si cap. Consistent with the trend in Fig. 7.2**d–f**, we find a significant reduction in spread for $\tau_q$ (30%), and consequently for $\mu_q$, $\Gamma$. Furthermore, in heterostructures with an amorphous Si-rich layer we find a mean Dingle ratio of $(2.3 \pm 0.2)$. This mean value is $\simeq 300\%$ smaller and has an 80% reduction in spread compared to heterostructures with an epitaxial Si cap. This low value of the Dingle ratio indicates that short-range scattering from impurities within or near the quantum well is the dominant scattering mechanism[121], in agreement with the analysis of the mobility-density curve. Scattering from remote impurities is reduced thanks to a better semiconductor/dielectric interface. Our mean value for $\tau_q$ in $^{28}$Si/SiGe is also on par with the best value reported in Ref. [123] from H-FETs in Si/SiGe heterostructures featuring an epitaxial Si cap. However, in our samples, the semiconductor/dielectric interface is much closer to the channel (30 nm compared to 50 nm in Ref. [123]). Therefore, this comparison confirms that scattering from remote impurities is limited in our devices as a consequence of a high-quality and uniform semiconductor/dielectric interface associated with the termination process at 500 °C.

## 7.4. DISCUSSION

In summary, we challenged the mainstream approach to deposit an epitaxial Si cap on $^{28}$Si/SiGe heterostructures and, instead, we terminated the SiGe barrier with an amorphous Si-rich layer, obtained by exposure to DCS at 500 °C. Compared to previous heterostructures that feature an epitaxial Si cap and that have already produced high performance spin qubits [51, 115], we demonstrate an improvement in performance of H-FETs in terms of mean value and spread of mobility, percolation density, maximum electric field before hysteresis, and single particle relaxation time (and hence quantum mobility). We speculate that performance improves because the amorphous Si-rich layer gets completely oxidized compared to the epitaxial Si cap (see figure. 7.4), thereby creating a more uniform $SiO_x$ layer with less scattering centers. By having a better semiconductor/dielectric interface and wafer-scale uniformity, we expect that this material stack may lead to Si spin qubits with improved yield and performance. In this direction, charge noise measured in quantum dots on these heterostructures will be very informative as these measurements probe the dynamics of charge fluctuations that transport experiments are not very sensitive to. These results motivate new studies, for example by varying the temperature and/or time of exposure to DCS to understand in detail the nature of the amorphous Si-rich layer on the SiGe barrier, the role of Cl and H upon oxidation in air, and to use this knowledge as a tool for further optimizing the semiconductor/dielectric interface.

## 7.5. SUPPLEMENTARY INFORMATION

### 7.5.1. STRUCTURAL AND CHEMICAL PROPERTIES OF THE SEMICONDUCTOR/DIELECTRIC INTERFACE

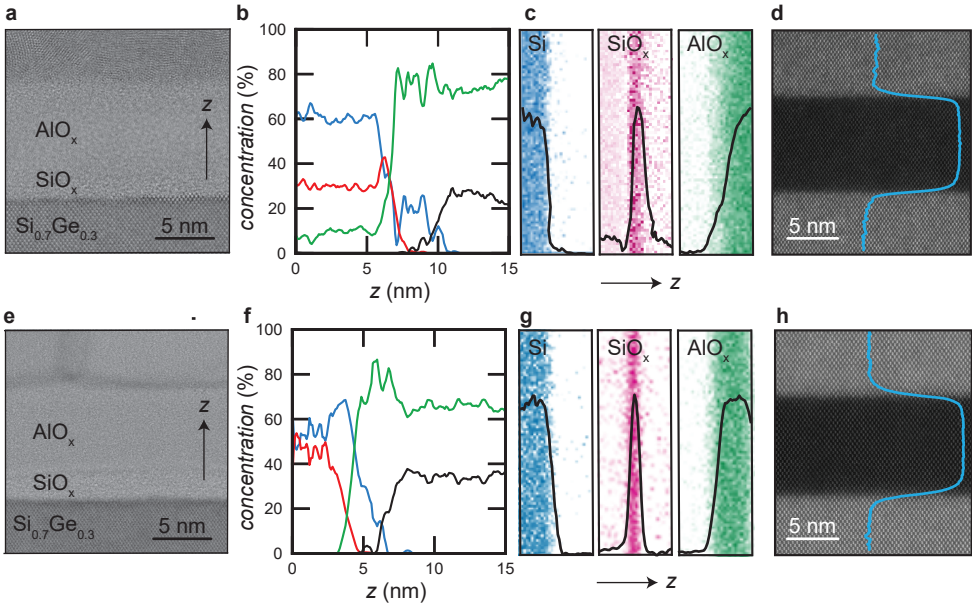


Figure 7.4: Data comparing the structural and chemical properties of the semiconductor/dielectric interface for heterostructures terminated by a Si-rich amorphous layer obtained by exposure to DCS at 500 °C (first row) and for heterostructures with an epitaxial Si cap grown at 675 °C (second row). **a**, **e** Bright Field-STEM zoom-in images of the dielectric and gate metal stack **b**, **f** Electron energy loss spectroscopy (EELS) semiquantitative concentration depth profiles across the semiconductor/dielectric interface for Si (blue), Ge (red), O (green), and Al (black). **c**, **g** 15 nm×45 nm wide 2D maps by EELS using low-energy edges to recognize the different bonding states: Si (blue), $SiO_x$ (magenta) and $AlO_x$ (green). **d**, **h** Z Contrast-STEM zoom images of the $^{28}$Si QW with superimposed intensity profiles. QW thickness and interface sharpness remain similar in the two heterostructures.

### 7.5.2. ELECTRON TEMPERATURE

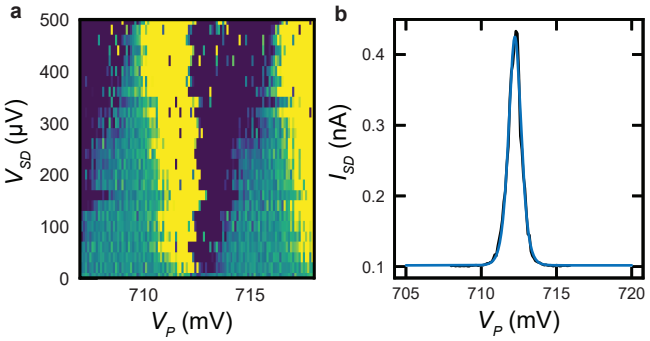


Figure 7.5: **a** Differential conductance ($dI/dV$) showing representative Coulomb blockade diamonds as a function of the source-drain voltage ($V_{SD}$) and plunger gate voltage ($V_P$). The measurements are performed using the sensing dot on single-layer quantum dot devices in transport regime [115]. From the shape of the Coulomb diamond, we derive an effective lever arm via the equation $\alpha = \frac{m_S m_D}{m_S - m_D} = 0.06$ (eV/V), where $m_S$ and $m_D$ are the slopes of the Coulomb diamond from source and drain. **b** Coulomb peak with superimposed fit to the function $I(V_P) = A + B\cosh^{-2}(\frac{\alpha(V_0 - V)}{2k_B T})$ where $A$, $B$, $V_0$, and $T_e$ are fitting parameter [251]. From the fit we derive an electron temperature of $T_e = 190(10)$ mK. The Coulomb peak is measured using a source-drain voltage of $V_{SD} = 100\ \mu$V.

# 8

# REDUCING CHARGE NOISE IN QUANTUM DOTS BY USING THIN SILICON QUANTUM WELLS

*Charge noise in the host semiconductor degrades the performance of spin-qubits and poses an obstacle to control large quantum processors. However, it is challenging to engineer the heterogeneous material stack of gate-defined quantum dots to improve charge noise systematically. Here, we address the semiconductor-dielectric interface and the buried quantum well of a $^{28}$Si/SiGe heterostructure and show the connection between charge noise, measured locally in quantum dots, and global disorder in the host semiconductor, measured with macroscopic Hall bars. In 5 nm thick $^{28}$Si quantum wells, we find that improvements in the scattering properties and uniformity of the two-dimensional electron gas over a 100 mm wafer correspond to a significant reduction in charge noise, with a minimum value of $0.29 \pm 0.02$ $\mu eV/\sqrt{Hz}$ at 1 Hz averaged over several quantum dots. We extrapolate the measured charge noise to simulated dephasing times to* CZ*-gate fidelities that improve nearly one order of magnitude. These results point to a clean and quiet crystalline environment for integrating long-lived and high-fidelity spin qubits into a larger system.*

This chapter has been published in Brian Paquelet Wuetz, Davide Degli Esposti, Anne-Marije J. Zwerver, Sergey V. Amitonov, Marc Botifoll, Jordi Arbiol, Amir Sammak, Lieven M. K. Vandersypen, Maximilian Russ, Giordano Scappucci, Reducing charge noise in quantum dots by using thin silicon quantum wells, arXiv:2209.07242 (2022) [252]

## 8.1. INTRODUCTION

Spin-qubits in silicon quantum dots are a promising platform for building a scalable quantum processor because they have a small footprint[207], long coherence times[186, 133], and are compatible with advanced semiconductor manufacturing[208]. Furthermore, rudimentary quantum algorithms have been executed[168] and quantum logic at high-fidelity performed[115, 114, 253, 231]. As the qubit count is increasing, with a six-qubit processor demonstrated[50], significant steps have been taken to couple silicon spin qubits at a distance, via microwave photons or spin shuttling[171, 173, 254, 232, 255, 256], towards networked spin-qubit tiles[181]. However, electrical fluctuations associated with charge noise in the host semiconductor can decrease qubit readout and control fidelity[113]. Reducing charge noise independently of the device location on a wafer is pivotal to achieving the ubiquitous high-fidelity of quantum operations, within and across qubit tiles, necessary to execute more complex quantum algorithms.

Charge noise is commonly associated with two-level fluctuators (TLF)[65] in the semiconductor host. In gated heterostructures with buried quantum wells, TLF may arise from impurities in several locations: within the quantum well, the semiconductor barrier, the semiconductor/dielectric interface, and the dielectrics layers above[48, 257, 102, 103, 104, 105, 106]. Furthermore, previous work on strained-Si MOSFETs[107, 108, 109], with strained-Si channels deposited on SiGe strain relaxed buffers, has associated charge noise with dislocations arising from strain relaxation, either deep in the SiGe buffer or at the quantum well/buffer interface. Since these impurities and dislocations are randomly distributed over the wafer and are also a main scattering source for electron transport in buried quantum wells[121], a holistic approach to materials engineering should be taken to address disorder in two-dimensional electron gases and charge noise in quantum dots.

In this work, we demonstrate thin quantum wells in $^{28}$Si/SiGe heterostructures with low and uniform charge noise, measured over several gate-defined quantum dot devices. By linking charge noise measurements to the scattering properties of the two-dimensional electron gas, we show that a quiet environment for quantum dots is obtained by improving the semiconductor/dielectric interface and the crystalline quality of the quantum well. We feed the measured charge noise into a theoretical model, benchmark the model against recent experimental results [115, 50], and predict that these optimized heterostructures may support long-lived and high-fidelity spin qubits.



## 8.2. DESCRIPTION OF SI/SIGE HETEROSTRUCTURES

Figure 8.1**a** illustrates the undoped $^{28}$Si/SiGe heterostructures, grown by reduced-pressure chemical vapour deposition, and the gate-stack above. From bottom to top, the material stack comprises a 100 mm Si substrate, a strain-relaxed SiGe buffer layer, a strained $^{28}$Si quantum well, a 30 nm thick SiGe barrier, a Si cap oxidized in air to form a $SiO_x$ layer, an $AlO_x$ layer formed by atomic layer deposition, and metallic gates. The SiGe layers above and below the quantum well have a Ge concentration of $\simeq 0.3$ (Methods).

We consider three $^{28}$Si/SiGe heterostructures (A, B, C) to improve, in sequence, the semiconductor/dielectric interface (from A to B) and the crystalline quality of the quantum well (from B to C). Heterostructure A has an $\simeq 9$ nm thick quantum well and is termi-

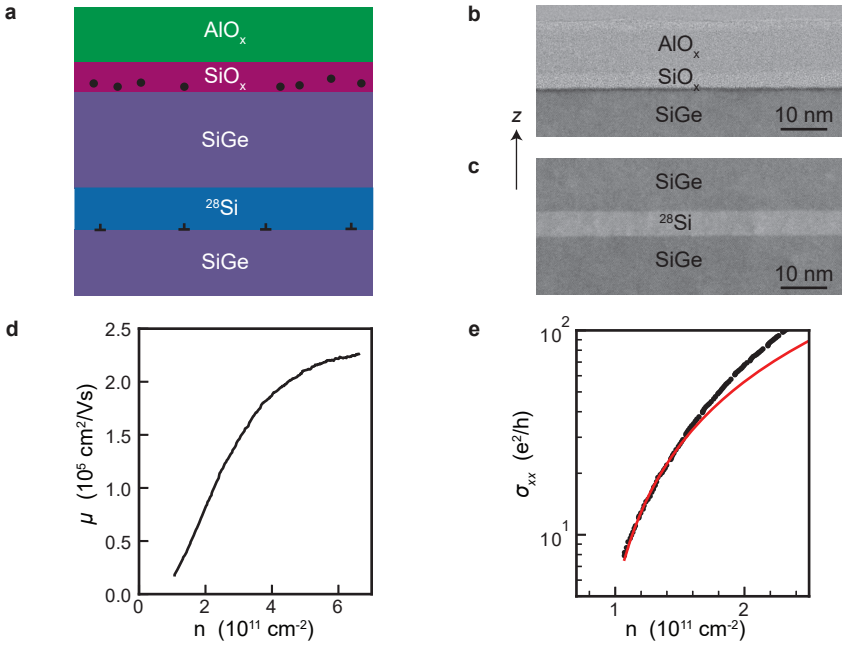


Figure 8.1: **a** Schematics of the $^{28}$Si/SiGe heterostructure and dielectric stack above. $z$ indicates the heterostructure growth direction. Circles represent remote impurities at the semiconductor/dielectric interface and perpendicular symbols represent misfit dislocations that might arise at the quantum well/buffer interface due to strain relaxation. **b**, **c** BF-STEM images from heterostructure C highlighting the semiconductor/dielectric interface and the 5 nm thick $^{28}$Si quantum well, respectively. **d** Mobility $\mu$ and **e** conductivity $\sigma_{xx}$ measured as a function of density $n$ at a temperature of 1.6 K in a Hall bar H-FET from heterostructure C. The red curve in **e** is a fit to percolation theory.

nated with an epitaxial Si cap grown by dichlorosilane at 675 °C. This kind of heterostructure has already produced high performance spin-qubits[51, 115, 50]. Heterostructure B misses a final epitaxial Si cap but features an amorphous Si-rich layer obtained by exposing the SiGe barrier to dichlorosilane at 500 °C. Compared to A, heterostructure B supports a two-dimensional electron gas with enhanced and more uniform transport properties across a 100 mm wafer, owing to a more uniform $SiO_x$ layer with less scattering centers[230]. Finally, we introduce here heterostructure C, having the same amorphous Si-rich termination as in heterostructure B, but a thinner quantum well of $\simeq 5$ nm (Supplementary Fig. 1). This is much thinner than the Matthews-Blakeslee critical thickness [59, 258], which is $\simeq 10$ nm[142] for the relaxation of tensile Si on $Si_{0.7}Ge_{0.3}$ via the formation of misfit dislocation at the bottom interface of the quantum well.

Figures 8.1**b**, c show bright-field scanning transmission electron microscopy (BF-STEM) images from heterostructure C after fabrication of a Hall bar shaped heterostructure field effect transistors (H-FET). We observe a sharp SiGe/$SiO_x$ semiconductor/dielectric interface (Fig. 8.1**b**), characterised by a minor Ge pile up (dark line) in line with Ref. [230]. The $\simeq 5$ nm thick quantum well (Fig. 8.1**c**) is uniform and has sharp interfaces to the nearby SiGe. No structural defects such as misfit dislocations are visible, suggesting they

are, at most, scarce. By analysing Raman spectra (Supplementary Fig. 2), we estimate a tensile strain for the $^{28}$Si quantum wells in heterostrucure B and C of $(0.93 \pm 0.02)$% and $(1.22 \pm 0.02)$%, respectively, compared the expected strain of 1.2% for the given stoichiometry of the heterostructures. These measurements point to significant strain relaxation in heterostructure B compared to C. In heterostructure B, the quantum wells approach the Matthews-Blakeslee critical thickness and therefore misfit dislocation segments are expected, in light of recent morphological characterization of Si/SiGe heterostructures with similar quantum well thickness and SiGe chemical composition[**liu_role_2022**]. Due to the $\sim 2\times$ thinner quantum well, instead, heterostructure C adapts the epitaxial planes to the SiGe buffer much better than heterostructure B, meaning that misfit dislocations arising from strain-relaxation are, in principle, suppressed.

### 8.2.1. ELECTRICAL CHARACTERIZATION OF H-FETS

We evaluate the scattering properties of the two-dimensional electron gases by wafer-scale electrical transport measured on Hall-bar shaped H-FETs operated in accumulation mode (Methods). For each heterostructure, multiple H-FETs over a wafer are measured in the same cool-down at a temperature of 1.7 K in refrigerators equipped with cryo-multiplexers[155]. Figures 8.1**d**, e show typical mobility-density and conductivity-density curves for heterostructure C, from which we extract the mobility measured at high density ($n = 6\times10^{11}$ cm$^{-2}$) and the percolation density ($n_p$)[125]. The mobility rises steeply at low density due to progressive screening of scattering from remote impurities and flattens at higher density ($n > 5\times10^{11}$ cm$^{-2}$), limited by scattering from impurities within or nearby the quantum well, for example uniform background charges, surface roughness, or crystalline defects such as threading or misfit dislocations[121, 61].

## 8.3. CHARGE NOISE MEASUREMENTS IN QUANTUM DOTS

For charge noise measurements, we use devices comprising a double quantum dot and a charge sensor quantum dot nearby, illustrated in Fig. 8.2**a**. Using the same device design, two-qubit gates with fidelity above 99% were demonstrated[115], silicon quantum circuits were controlled by CMOS-based cryogenic electronics[51], and energy splittings in $^{28}$Si/SiGe heterostructures were studied with statistical significance[73].

Here, we electrostatically define a multi-electron quantum dot in the charge sensor by applying gate voltages to the accumulation gates SDRAcc and SDLAcc, the barriers SDLB and SDRB, and the plunger gate P. All other gates (red in Fig. 8.2**a**) are set to 0 V for measurements of heterostructure B and C, whereas they are positively biased in heterostructure A to facilitate charge accumulation in the sensor (Methods). Figure 8.2**b** shows typical Coulomb blockade oscillations of the source-drain current $I_{SD}$ for a charge sensor from heterostructure C measured at a dilution refrigerator base temperature of 50 mK. We follow the same tune-up procedure (Methods) consistently for all devices and we measure charge noise at the flank of each Coulomb peak within the $V_P$ range defined by the first peak observable in transport and the last one before onset of a background channel (Supplementary Figs. 3,4). For example, in Figure 8.2**b** we consider Coulomb peaks within the $V_P$ range from 260 mV to 370 mV. The data collected in this systematic way is taken as a basis for comparison between the three different heterostructures in

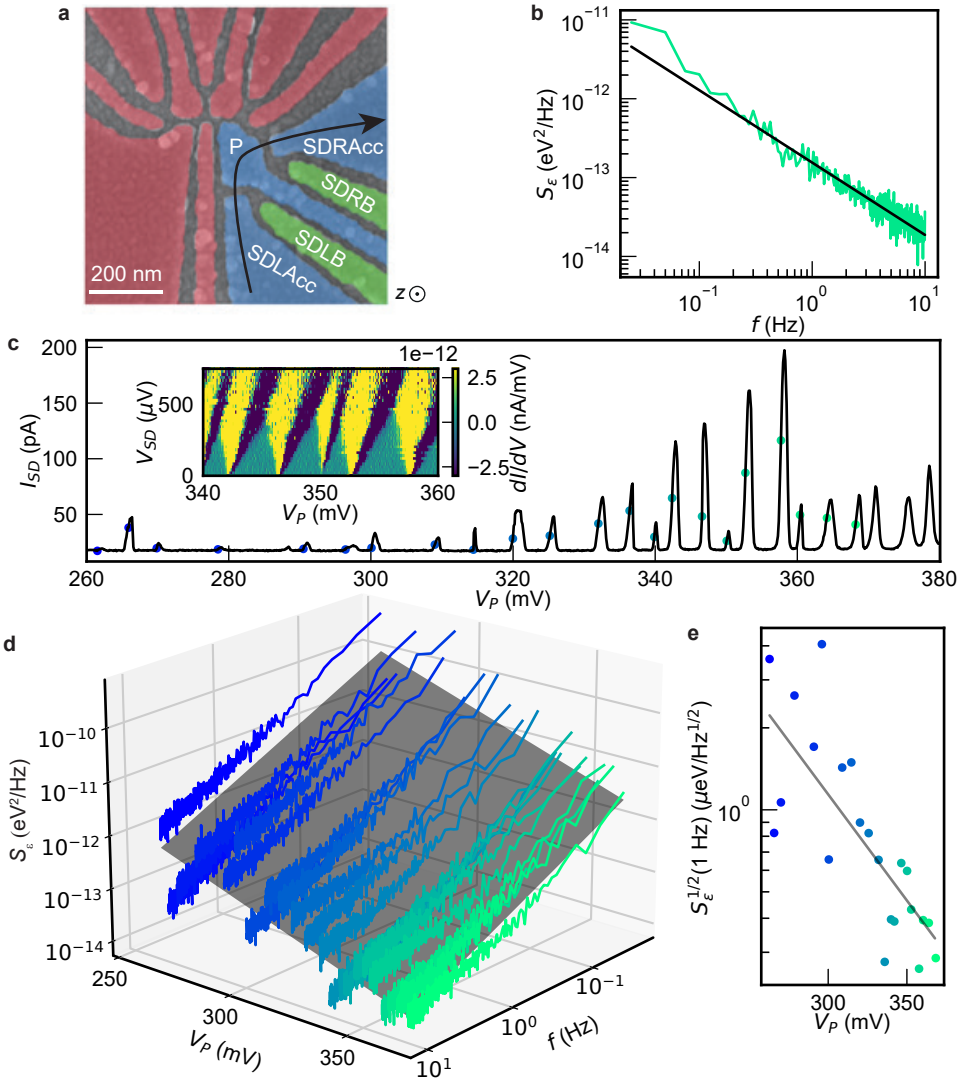


Figure 8.2: **a** False colored SEM-image of a double quantum dot system with a nearby charge sensor. Charge noise is measured in the multi-electron quantum dot defined by accumulation gates SDLAcc and SDRAcc (blue), plunger P (blue), with the current going along the black arrow. In these experiments, the gates defining the double quantum dot (red) are used as screening gates. There is an additional global top gate (not shown) to facilitate charge accumulation when needed. **b** Source-drain current $I_{SD}$ through a charge sensor device fabricated on heterostructure C against the plunger gate voltage $V_P$. Colored dots mark the position of the flank of the Coulomb peak where charge noise measurements are performed. The inset shows Coulomb diamonds from the same device, plotted as the differential of the current $dI/dV$ as a function of $V_P$ and the source drain bias $V_{SD}$. **c** Charge noise spectrum $S_\epsilon$ measured at the Coulomb peak at $V_P \simeq 345$ mV in **b** and extracted using lever arms from Coulomb diamonds. **d** Charge noise spectrum $S_\epsilon$ for the same device in **b**, plotted in 3D as a function of $V_P$ and $f$. The dark gray plane is a fit through the datasets. **e** Charge noise at $f = 1$ Hz obtained from data in **d**. The grey line is a line cut through the plane in **i** at $f = 1$ Hz.

this study.

For each charge noise measurement at a given $V_P$ we acquire 60 s (heterostructure A) or 600 s (heterostructures B, C) long traces of $I_{SD}$ and split them into 10 (heterostructure A) or 15 windows (heterostructures B, C). We obtain the current noise spectrum $S_I$ by averaging over the 10 (15) windows the discrete Fourier transform of the segments (Methods). We convert $S_I$ to a charge noise spectrum $S_\epsilon$ using lever arms from Coulomb diamond measurements and the slope of the Coulomb peaks(inset Fig. 8.2**b**, Methods, and Supplementary Fig.5). A representative charge noise spectrum $S_\epsilon$ measured at $V_P$ = 360.3 mV is shown in Fig. 8.2**c**. We observe an approximate $1/f$ trend at low frequency, pointing towards an ensemble of TLF with a broad range of activation energies affecting charge noise around the charge sensor [99, 64]. Figure 8.2**e** shows the charge noise $S_\epsilon^{1/2}$ at 1 Hz as a function of $V_P$. The charge noise decreases, with a linear trend, with increasing $V_P$, suggesting that, similar to scattering in 2D, screening by an increased electron density shields the electronically active region from noise arising from the heterostructure and the gate stack[138]. From this measurement we extract, for a given device, the minimum measured charge noise at 1 Hz ($S_{\epsilon,min}^{1/2}$) upon variation of $V_P$ in our experimental range. We use $S_{\epsilon,min}^{1/2}$, as an informative metric to compare charge noise levels from device to device in a given heterostructure. For a given device, all charge noise spectra $S_\epsilon$ are plotted in 3D as a function of $f$ and $V_P$ (Fig. 8.2**d**). To quantify our observations, we fit the data to the plane $\log S_\epsilon = -\alpha \log f + \beta V_P + \gamma$ with coefficient $\alpha = 0.84 \pm 0.01$ indicating the spectrum power law exponent and coefficient $\beta = -15.6 \pm 0.1$ $\mu eV^2/VHz$ quantifying the change in noise spectrum with increasing plunger gate and, consequently, the susceptibility of charge noise to the increasing electron number in the sensor.

## 8.4. DISTRIBUTION OF TRANSPORT PROPERTIES AND CHARGE NOISE

We have introduced key metrics for 2D electrical transport ($\mu$, $n_p$) and charge noise ($\alpha$, $\beta$ and $S_{\epsilon,min}^{1/2}$) from Hall bar and quantum dot measurements, respectively. In Figs. 8.3**a**-**e** we compare the distributions of all these metrics for the three heterostructures A, B, C. Each box-plot is obtained from the analysis of measurements in Figs. 8.1**d**,**e**, and Fig. 8.2**d** repeated on multiple H-FETs or quantum dots, on dies randomly selected from different locations across the 100 mm wafers (Methods). As reported earlier in Ref. [230], the improvement in both mean values and spread for $\mu$ and $n_p$ was associated with a reduction of remote impurities when replacing the epitaxial Si cap in heterostructure A with a Si-rich passivation layer in heterostructure B. Moving to heterostructure C, we measure a high mean mobility of $(2.10 \pm 0.08) \times 10^5$ $cm^2/Vs$ and a low mean percolation density of $(7.68 \pm 0.37) \times 10^{10}$ $cm^{-2}$, representing an improvement by a factor $\simeq 1.4$ and $\simeq 1.3$, respectively (compared to heterostructure A). Most strikingly, the 99% confidence intervals of the mean for $\mu$ and $n_p$ are drastically reduced by a factor $\simeq 9.8$ and $\simeq 4.8$, respectively. We speculate that these improvements in heterostructure C are associated with the suppression of misfit dislocations at the quantum well/buffer interface, thereby reducing short range scattering and increasing uniformity on a wafer-scale. This interpretation is supported by the strain characterization discussed above and by previous studies of mobility limiting mechanisms as a function of the quantum well thickness in strained

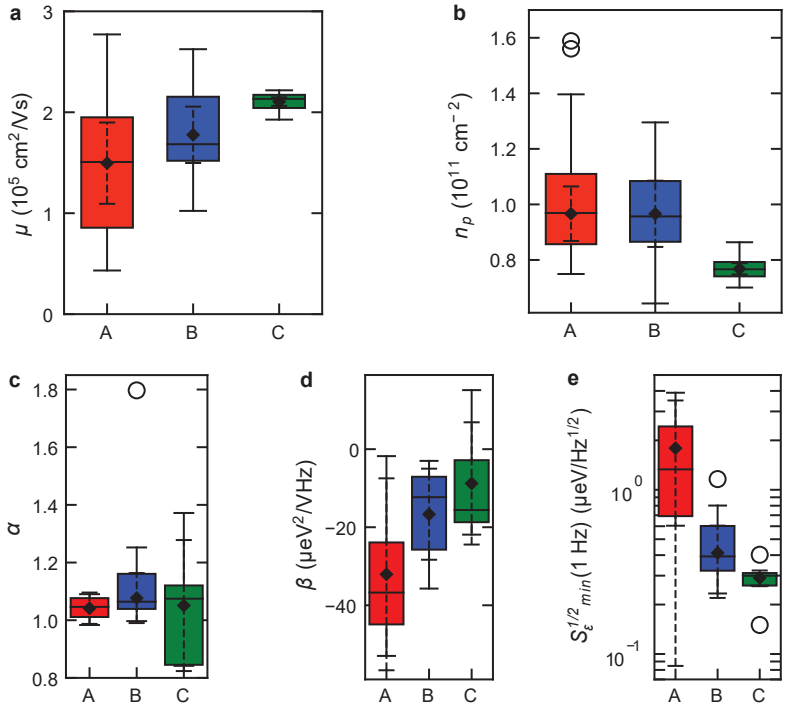


Figure 8.3: **a**, **b** Distributions of mobility $\mu$ measured at $n = 6 \times 10^{11}$ cm$^{-2}$ and percolation density $n_p$ for heterostructure A (red, 20 H-FETs measured, of which 16 reported in Ref. [230]), B (blue, 16 H-FETs measured of which 14 reported in Ref. [230]), and C (green, 22 H-FETs measured). **c**- **e** Distributions of noise spectrum power law exponent $\alpha$, coefficient $\beta$ indicating the change in noise spectrum with increasing $V_P$, and minimum charge noise $S^{1/2}_{\epsilon,min}$ within the range of $V_P$ investigated for heterostructure A (red, 4 devices measured), B (blue, 7 devices measured), and C (green, 5 devices measured). Quartile box plots, mode (horizontal line), means (diamonds), 99% confidence intervals of the mean (dashed whiskers), and outliers (circles) are shown.



Si/SiGe heterostructures[61].

We now shift our attention to the results of charge noise measurements. First, the power law exponent $\alpha$ (Fig. 8.3**c**) shows a mean value $\simeq 1$, however the 99% confidence interval and interquartile range increase when moving from heterostructure A to B and C. Next, we observe a decreasing trend for the absolute mean value of coefficient $\beta$ (Fig. 8.3**d**), meaning that the noise spectrum is less susceptible to changes in $V_P$. Finally, we plot in Fig. 8.3**e** the distributions for $S^{1/2}_{\epsilon,min}$, the minimum charge noise at 1 Hz upon varying $V_P$. We find in heterostructure C an almost order of magnitude reduction in mean $S^{1/2}_{\epsilon,min}$ to $0.29 \pm 0.02$ μeV/$\sqrt{\text{Hz}}$. Furthermore, within the distribution of $S^{1/2}_{\epsilon,min}$ for heterostructure C, the minimum value of the measured charge noise as a function of $V_P$ and across quantum dots is 0.15 μeV/$\sqrt{\text{Hz}}$. These charge noise values are on par or compare favourably to the best values reported previously at 1 Hz in gate defined quantum dots. In multi-electron quantum dots, charge noise of 0.47 μeV/$\sqrt{\text{Hz}}$ was reported for Si/SiGe[111], 0.6 μeV/$\sqrt{\text{Hz}}$ (average value, with a minimum of $\leq$ 0.2 μeV/$\sqrt{\text{Hz}}$) for Ge/SiGe[89], $0.49 \pm 0.1$ μeV/$\sqrt{\text{Hz}}$ for Si/$SiO_2$[136], and 1 μeV/$\sqrt{\text{Hz}}$ for InSb[92]. In single-

electron quantum dots, charge noise of 0.33 μeV/$\sqrt{\text{Hz}}$ was reported for Si/SiGe[197] and 7.5 μeV/$\sqrt{\text{Hz}}$ for GaAs[259].

We understand the charge noise trends in Figs. 8.3**c**–**e** by relating them to the evolution of the disorder landscape moving from heterostructures A to B and C, as inferred by the electrical transport measurements in Figs. 8.3**a**,**b**. The narrow distribution of $\alpha$ in heterostructure A points to charge noise from many TLFs possibly located at the low quality semiconductor/dielectric interface and above. Instead, the larger spread in $\alpha$ in heterostructure B and C implies that deviations from $1/f$ behaviour become more frequent, possibly originating from a non-uniform distribution of TLF or from one low frequency TLF in the surrounding environment of the quantum dot that dominates the power spectrum in the measured interval. The electrical transport measurements support this interpretation: scattering from many remote impurities is dominant in heterostructure A, whereas with a better semiconductor/dielectric interface remote scattering has less impact in the transport metrics of heterostructures B and C.

The decreasing trend in $|\beta|$ is in line with the observation from electrical transport. As the impurity density decreases from heterostructure A to B and C, charge noise is less affected by an increasing $V_P$, since screening of electrical noise through adding electrons to the charge sensor becomes less effective, possibly due to a smaller TLF-per-volume ratio. While we are not able to measure directly the electron number in the charge sensor, we deem unlikely the hypothesis that charge sensors in heterostructure A are operated with considerably fewer electrons than in heterostructure C. This is because all operation gate voltages in heterostructure A are consistently larger than in heterostructure C (Supplementary Fig. 4), due to the higher disorder.

Finally, the drastic reduction in mean value and spread of $S_{\epsilon,min}^{1/2}$ mirrors the evolution of mean value and spread of $n_p$ and $\mu$. From heterostructure A to B, a reduction in scattering from remote impurities is likely to result in less charge noise from long-range TLFs. From heterostructure B to C, the larger strain, and consequently the reduction in the possible number of dislocations at the quantum well/buffer interface, further reduces the charge noise picked up by quantum dots. This explanation is based on earlier studies of charge noise in strained Si-MOSFETs[107, 108, 109], which showed a correlation between low-frequency noise spectral density and static device parameters. Dislocations at the bottom of the strained channel may act as scattering centers that degrade mobility and as traps for the capture and release of carriers, which causes noise similarly to traps at the dielectric interface.

8

## 8.5. CALCULATED DEPHASING TIME AND INFIDELITY

To emphasize the improvement of the electrical environment in the semiconductor host, we calculate the dephasing time $T_2^\star$ of charge and spin qubits assuming these qubits experience the same fluctuations as our $^{28}$Si/SiGe quantum dots. The dephasing time of a qubit (in the quasistatic limit and far-off from a sweet spot) is given by [137]

$$T_2^\star = \frac{h}{\sqrt{2}\pi\sigma} \tag{8.1}$$

with the Planck constant $h$ and the standard deviation

$$\sigma^2 = \left|\frac{\partial \mathscr{E}}{\partial \mu}\right|^2 \times 2 \int_{f_{\text{low}}}^{f_{\text{high}}} \frac{S_\epsilon^2}{f^\alpha} df. \tag{8.2}$$

Importantly, both the charge noise amplitude $S_\epsilon^2(f)$ and the noise exponent $\alpha$ have a strong impact on the dephasing time while the low and high frequency cut-off, $f_{\text{low}}$ and $f_{\text{high}}$, given by the duration of the experiment have a weaker impact. The prefactor $\left|\frac{\partial \mathscr{E}}{\partial \mu}\right|$ translates shifts in chemical potential of the charge sensor into energy shifts of the qubit and depends on many parameters such as the type of qubit and the device itself. We find $\left|\frac{\partial \mathscr{E}}{\partial \mu}\right| = 1$ for a charge qubit [260] and $\left|\frac{\partial \mathscr{E}}{\partial \mu}\right| \approx 10^{-5}$ for an uncoupled spin- qubit [111] (see Supplementary Information for a derivation of these numbers and the used frequency bandwidths).

Figure 8.4**a** shows the computed dephasing times of charge qubits (circle) and spin qubits (star) for all three heterostructures. The improvements in our material can be best seen by investigating $T_2^\star$ of the charge qubit since it is directly affected by charge noise. Our theoretical extrapolation shows two orders of magnitude improvement in $T_2^\star$ by switching from heterostructures A to heterostructures B and C [1]. Note, that the integration regimes differ for spin and charge qubits due to the different experimental setups and operation speeds [260, 111]. For potential spin qubits in heterostructure A the calculated $T_2^\star$ shows an average $\overline{T}_2^\star = 8.4 \pm 5.6$ µs. This distribution compares well with the distribution $\overline{T}_2^\star = 6.7 \pm 5.6$ µs of experimental $T_2^\star$ data from state-of-the-art semiconductor spin qubits in materials with similar stacks as in heterostructure A[115, 50]. Note that while such comparisons oversimplify actual semiconductor spin-qubit devices by reducing them to a single number, they fulfill two aims. They allow us to benchmark the computed performance of heterostructure A to past experiments and provide a prognosis on the qubit quality in novel material stacks. Heterostructures B and C, in this case, may support average dephasing times of $\overline{T}_2^\star = 24.3 \pm 12.5$ µs and $\overline{T}_2^\star = 36.7 \pm 18$ µs, respectively. The highest values $T_2^\star = 70.1$ µs hints towards a long spin qubit dephasing times previously only reported in Ref. [186].

Figure 8.4**b** shows the simulated infidelity, a metric to measure the closeness to the ideal operation, of a universal CZ-gate between two spin qubits following Ref. [115] and Section 5 in the Supplementary Information. Note, that the device used in Ref. [115] has the same architecture as our test devices. In the CZ-gate simulation noise dominantly couples in via barrier voltage fluctuations which affects the interaction between the electron spins. Again, we assume the charge noise amplitude and exponents measured in our quantum dot experiments as input for the simulations. The simulations show an averaged average gate infidelity $1 - \overline{F}_{\text{CZ}} = 0.02 \pm 0.01$ % which means on average a single error every 5000 runs. We also observe a saturation value close to $1 - F = 10^{-4}$ which arises from single-qubit dephasing $T_2^\star = 20$ µs used in the simulations estimated from nuclear spin noise due to a 800 ppm concentration of the $^{29}$Si silicon isotope which has a non-zero nuclear spin [111].

[1] One order is gained from the reduced charge noise amplitude and another order is gained through a more beneficial noise exponent $\alpha > 1$.

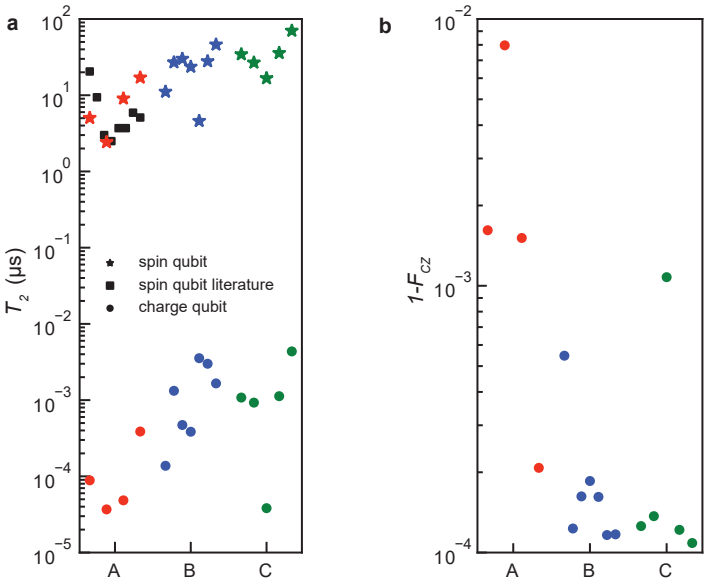


Figure 8.4: **a** Computed dephasing times $T_2^\star$ of a charge qubit (circle) and a spin-qubit (star) using $S_{\epsilon,min}$ from heterostructure A (red), B (blue), C (green). Eq. (8.1) was used to compute $T_2^\star$ as a function of $S_\epsilon$ and $\alpha$ from Fig. 8.3. Literature values (squares) are taken from Refs. [115, 50]. **b** Simulated infidelity of a CZ-gate between two spin qubits following the Ref. [115] using $S_\epsilon$ and $\alpha$ from heterostructure A (red), B (blue), C (green) in Fig. 8.3 as input for barrier fluctuations.

## 8.6. DISCUSSION

In summary, we have measured electron transport and charge noise in $^{28}$Si/SiGe heterostructures where we improve the semiconductor/dielectric interface, by adopting an amorphous Si-rich passivation, and the structural quality of the quantum well, by reducing the quantum well thickness significantly below the Matthew-Blakeslee critical thickness for strain relaxation. We relate disorder in 2D to charge noise in quantum dots by following a statistical approach to measurements. A reduction of remote impurities and dislocations nearby the quantum well is connected with the key improvements in the scattering properties of the 2D electron gas, such as mobility and percolation density, and their uniformity across a 100 mm wafer. The trend observed from electron transport in 2D is compatible with the observations from measurements of charge noise in quantum dots. As remote impurities are reduced, charge noise becomes more sensitive to local fluctuators nearby the quantum well and less subject to screening by an increased number of electrons in the dot. Furthermore, with this materials optimization, we achieve a statistical improvement of nearly one order of magnitude in the charge noise supported by quantum dots. Using the charge noise distribution as input parameter and benchmarking against published spin-qubit data, we predict that our optimized semiconductor host could support long-lived and high-fidelity spin qubits. We envisage that further materials improvements in the structural quality of the quantum well, in addition to the commonly considered semiconductor/dielectric interface, may lead

systematically to quantum dots with less noise and to better qubit performance.

## 8.7. METHODS

### 8.7.1. SI/SIGE HETEROSTRUCTURE GROWTH

The $^{28}$Si/SiGe heterostructures are grown on a 100-mm n-type Si(001) substrate using an Epsilon 2000 (ASMI) reduced pressure chemical vapor deposition reactor. The reactor is equipped with a $^{28}SiH_4$ gas cylinder (1% dilution in $H_2$) for the growth of isotopically enriched $^{28}$Si. The $^{28}SiH_4$ gas was obtained by reducing $^{28}SiF_4$ with a residual $^{29}$Si concentration of 0.08%[141]. Starting from the Si substrate, the layer sequence of all heterostructures comprises a 3 µm step-graded $Si_{(1-x)}Ge_x$ layer with a final Ge concentration of $x = 0.3$ achieved in four grading steps ($x = 0.07$, 0.14, 0.21, and 0.3), followed by a 2.4 µm $Si_{0.7}Ge_{0.3}$ strain-relaxed buffer. The heterostructures differ for the active layers on top of the strain-relaxed buffer. Heterostructure A has a 9 nm tensile strained $^{28}$Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a sacrificial 1 nm epitaxial Si cap. Heterostructure B has an 9 nm tensile strained $^{28}$Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a sacrificial passivated Si cap grown at 500 °C. Heterostructure C has a 5 nm tensile strained $^{28}$Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a sacrificial passivated Si cap grown at 500 °C. A typical secondary ions mass spectrometry of our heterostructures is reported in Fig. S13 of [73] and the Ge concentration in the SiGe layers is confirmed by quantitative electron energy loss spectroscopy (EELS).

### 8.7.2. DEVICE FABRICATION

The fabrication process for Hall-bar shaped heterostructure field effect transistors (H-FETs) involves: reactive ion etching of mesa-trench to isolate the two-dimensional electron gas; P-ion implantation and activation by rapid thermal annealing at 700 °C; atomic layer deposition of a 10-nm-thick $Al_2O_3$ gate oxide; deposition of thick dielectric pads to protect gate oxide during subsequent wire bonding step; sputtering of Al gate; electron beam evaporation of Ti:Pt to create ohmic contacts to the two-dimensional electron gas via doped areas. All patterning is done by optical lithography. Double quantum dot devices are fabricated on wafer coupons from the same H-FET fabrication run and share the process steps listed above. Double-quantum dot devices feature a single layer gate metallization and further require electron beam lithography, evaporation of Al (27 nm) or Ti:Pd (3:27 nm) thin film metal gate, lift-off, and the global top-gate layer.



### 8.7.3. ELECTRICAL CHARACTERIZATION OF H-FETS

Hall-bar H-FETs measurements are performed in an attoDRY2100 variable temperature insert refrigerator at a base temperature of 1.7 K[230]. We apply a source-drain bias of 100 µV and measure the source-drain current $I_{SD}$, the longitudinal voltage $V_{xx}$, and the transverse Hall voltage $V_{xy}$ as function of the top gate voltage $V_g$ and the external perpendicular magnetic field $B$. From here we calculate the longitudinal resistivity $\rho_{xx}$ and transverse Hall resistivity $\rho_{xy}$. The Hall electron density $n$ is obtained from the linear relationship $\rho_{xy} = B/en$ at low magnetic fields. The carrier mobility $\mu$ is extracted from the relationship $\sigma_{xx} = ne\mu$, where $e$ is the electron charge. The percolation density $n_p$ is extracted by fitting the longitudinal conductivity $\sigma_{xx}$ to the relation $\sigma_{xx} \propto (n - n_p)^{1.31}$. Here $\sigma_{xx}$ is obtained via tensor inversion of $\rho_{xx}$ at $B = 0$. The box plots in Figs. 8.3**a**,**b** for heterostructure A (red) and B (blue) expand previously published data in Figs. 2f,e of

Ref. [230] by considering measurements of 4 additional H-FETs for heterostructure A (20 H-FETs in total) and of 2 additional H-FETs for heterostructure B (16 H-FETs in total).

### 8.7.4. ELECTRICAL CHARACTERIZATION OF QUANTUM DOTS

Measurements of the multi-electron quantum dots defined in the charge sensor are performed in a Leiden cryogenic dilution refrigerator with a mixing chamber base temperature $T_{\mathrm{MC}}$ = 50 mK[73]. The devices are tuned systematically with the following procedure. We sweep all gate voltages ($V_{SDRAcc}$, $V_{SDRB}$, $V_P$, $V_{SDLB}$, and $V_{SDLAcc}$) from 0 V towards more positive bias, until a source-drain current $I_{SD}$ of ≈ 1 nA is measured, indicating that a conductive channel has formed in the device. We then reduce the barrier voltages to find the pinch-off voltages for each barrier. Subsequently, we measure $I_{SD}$ as a function of $V_{SDLB}$ and $V_{SDRB}$ and from this 2D map we find a set of gate voltage parameters so that Coulomb blockade peaks are visible. We then fix the barrier voltages and sweep $V_P$ to count how many clearly defined Coulomb peaks are observed before onset of a background current. The quantum dot is tuned to show at least 9 Coulomb peaks, so that noise spectra may be fitted as in Fig. 8.2**d** with meaningful error bars. If we see less than 9 Coulomb peaks we readjust the accumulation gate voltages $V_{SDRAcc}$, and $V_{SDLAcc}$, and repeat the 2D scan of $V_{SDLB}$ against $V_{SDRB}$. In one case (device 2 of heterostructure A), we tuned device to show past 5 Coulomb peaks and still performed the fit of the charge noise spectra similar to the one shown in Fig. 8.2**d**. Further details on the extraction of the lever arms and operation gate voltages of the devices are provided in Supplementary Figs 4,5. We estimate an electron temperature of 190 mK by fitting Coulomb blockade peaks (see Supplementary Fig. 2 in Ref. [230]) measured on quantum dot devices.

For heterostructure A we apply a source drain bias of 100 μV (1 device) or 150 μV (3 devices) across the quantum dot, finite gate voltages across the operation gates of the dot, and finite gate voltages across the screening gates. We measure the current $I_{SD}$ and the current noise spectrum $S_I$ on the left side of the Coulomb peak where $|dI/dV_P|$ is largest. We use a sampling rate of 1 kHz for 1 minute using a Keithley DMM6500 multimeter. The spectra are then divided into 10 segments of equal length and we use a Fourier transform to convert from time-domain to frequency-domain for a frequency range of 167 mHz-500 Hz. We set the upper limit of the frequency spectra at 10 Hz, to avoid influences from a broad peak at around 150 Hz coming from the setup (Supplementary Fig. 3). A peak in the power spectral density at 9 Hz is removed from the analysis since it is an artifact of the pre-amplifier. To convert the current noise spectrum to a charge noise spectrum we use the formula

$$S_\epsilon = \frac{aS_I}{|d_V/d_P|^2} \tag{8.3}$$

where $a$ is the lever arm and $|dI/dV_P|$ is the slope of Coulomb peak around the center of the Coulomb peak.

For heterostructures B and C we apply a source drain bias of 150 μV across the quantum dot, finite gate voltages across the operation gates of the quantum dot, and we apply 0 V to all other gates. We measure the current $I_{SD}$ and the current noise spectrum $S_I$ on

the left side of the Coulomb peak where $|dI/dV_P|$ is largest. We use a sampling rate of 1 kHz for 10 minutes using a Keithley DMM6500 multimeter. The spectra are then divided into 15 segments of equal length and we use a Fourier transform to convert from time-domain to frequency-domain for a frequency range of 25 mHz-500 Hz. We set the upper limit of the frequency spectra at 10 Hz, to avoid influences from a broad peak at around 150 Hz coming from the setup. We use Eq. 8.3 to convert the current noise spectrum to a charge noise spectrum.

### 8.7.5. (SCANNING) TRANSMISSION ELECTRON MICROSCOPY

For structural characterization with (S)TEM, we prepared cross-sections of the quantum well heterostructures by using a Focused Ion Beam (Helios 600 dual beam microscope). HR-TEM micrographs were acquired in a TECNAI F20 microscope operated at 200 kV. Atomically resolved HAADF STEM data was acquired in a probe corrected TITAN microscope operated at 300 kV. EELS mapping was carried out in a TECNAI F20 microscope operated at 200 kV with approximately 2 eV energy resolution and 1 eV energy dispersion. Principal Component Analysis (PCA) was applied to the spectrum images to enhance S/N ratio.

## 8.8. SUPPLEMENTARY INFORMATION

### 8.8.1. MEASUREMENT OF THE THICKNESS OF THE QUANTUM WELLS

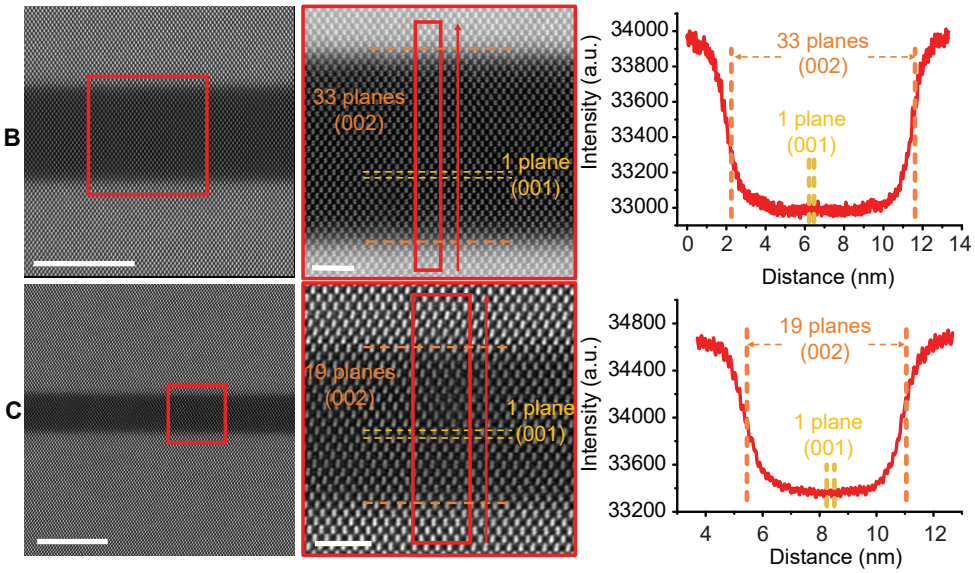


Figure 8.5: Method for computing the thickness of the quantum well based on the counting of the (002) horizontal planes, which reduces the uncertainty and bias associated to properly detecting the margins of the quantum well, for both heterostructures B and C. Scale bars of the images in the left column stand for 10 nm, while the zoom-ins in the middle column are 2 nm

To avoid possible errors associated with calibration, we measure the thickness of the Si layer in the quantum wells ($t_{qw}$) for heterostructures B and C by considering the interplanar spacing of the horizontal planes (002) of the quantum well ($d_{qw}$) and of the underlying the strain-relaxed SiGe buffer layer ($d_{buffer}$). For the $Si_{1-x}Ge_x$ buffer layer, we consider the stoichiometry $x$ as measured by means of quantitative EELS and calculate the theoretical expected cell parameter $a_{cell}$ using the following approximation of Vegard's law:

$$a_{cell} = a_{Si} + 0.2x + 0.027x^2, \tag{8.4}$$

where $a_{Si} = 5.431$ Å is the cell parameter of the diamond cubic Si crystal phase. To calculate $d_{buff}$ we use the formula for the interplanar distance of the desired plane (002) of a diamond cubic system:

$$d_{hkl} = \frac{a_{cell}}{\sqrt{h^2+k^2+l^2}} = \frac{a_{cell}}{\sqrt{0^2+0^2+2^2}} = \frac{a_{cell}}{2}. \tag{8.5}$$

Since the quantum well is strained, $d_{qw}$ is found by considering the average dilatation $\delta$ of the quantum well (002) planes with respect the (002) planes of the buffer. The dilatation $\delta$ is obtained experimentally by Geometrical Phase Analysis (GPA). The standard deviation of GPA is high for dilatation close to 0, as happens with the (220) epitaxial planes,

for which the method is not the preferred choice. Nevertheless, for the larger dilatation of the (002) planes, the relatively smaller standard deviation makes the measurement significative. As a result, $d_{qw}$ is computed by:

$$d_{qw} = d_{buff}(1+\delta). \tag{8.6}$$

Finally, the thickness of the quantum well is given by:

$$t_{qw} = n_{qw} d_{qw}, \tag{8.7}$$

where we count the number of planes forming the quantum well ($n_{qw}$) and multiply by $d_{qw}$. Therefore, the expected uncertainty of the thickness measurement lies in whether the initial and last plane of the well are being considered or not, *i.e.* the standard deviation is given by $\sigma = 2d_{qw}$.

With this in mind, for heterostructure B, where $x = 0.31$, four different measurements counting the (002) planes were performed in different regions of the quantum well, $n_{qw}$ = 33 (3 times) and 34. With an average experimental $\delta$ of -1.6±0.2 %, we obtain $d_{qw}$ = $2.704 \pm 0.007$ Å, resulting in an average thickness $t_{qw} = 9.0 \pm 0.5$ nm.

For heterostructure C, $x$ = 0.31 and two measurements counting the (002) planes were performed, $n_{qw}$ = 19 and 20. With an average experimental $\delta$ of -1.7±0.5 %, we obtain $d_{qw} = 2.701 \pm 0.014$ Å, resulting in an average thickness $t_{qw} = 5.3 \pm 0.5$ nm.

### 8.8.2. STRAIN ANALYSIS WITH RAMAN SPECTROSCOPY

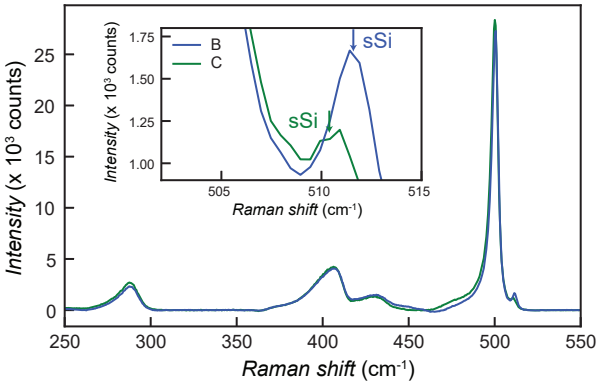


Figure 8.6: Baseline corrected Raman spectra taken with a laser wavelength $\lambda$ = 532 nm for heterostructure B and C, respectively. Spectra are band-fitted with Lorentzian-Gaussian bands, to accurately represent the values of each vibration and the shifts due to the strained structures. The inset shows the peaks due to the buried strained Si quantum well for heterostructure B and C. The blue shift of the peak for heterostructure B indicates strain relaxation compared to heterostructure C.

We calculate the strain of the Si quantum wells in heterostructures B and C by converting phonon frequency shifts into biaxial strain values [261, 262]:

$$\epsilon = \frac{\omega(\epsilon) - \omega_0}{b^{Si}}, \tag{8.8}$$

where $\omega_0 = 520$ cm$^{-1}$ is the Raman shift associated with the Si-Si vibration from the unstrained Si substrate from Ref. [263], $b^{Si} = 723 \pm 15$ cm$^{-1}$ is the strain-shift coefficient for Si reported in Ref. [264], and $\omega(\epsilon)$ is the Raman shift associated with the Si-Si vibration from the strained quantum well. For heterostructure B we measure $\omega(\epsilon) = 513.25$ cm$^{-1}$, corresponding to a tensile strain $\epsilon = (0.93 \pm 0.02)\%$. For heterostructure C we measure $\omega(\epsilon) = 511.12$ cm$^{-1}$, corresponding to a tensile strain $\epsilon = (1.22 \pm 0.02)\%$. The errors on the strain estimate arise from the 2% error reported for $b^{Si}$.

### 8.8.3. CHARGE NOISE MEASUREMENTS

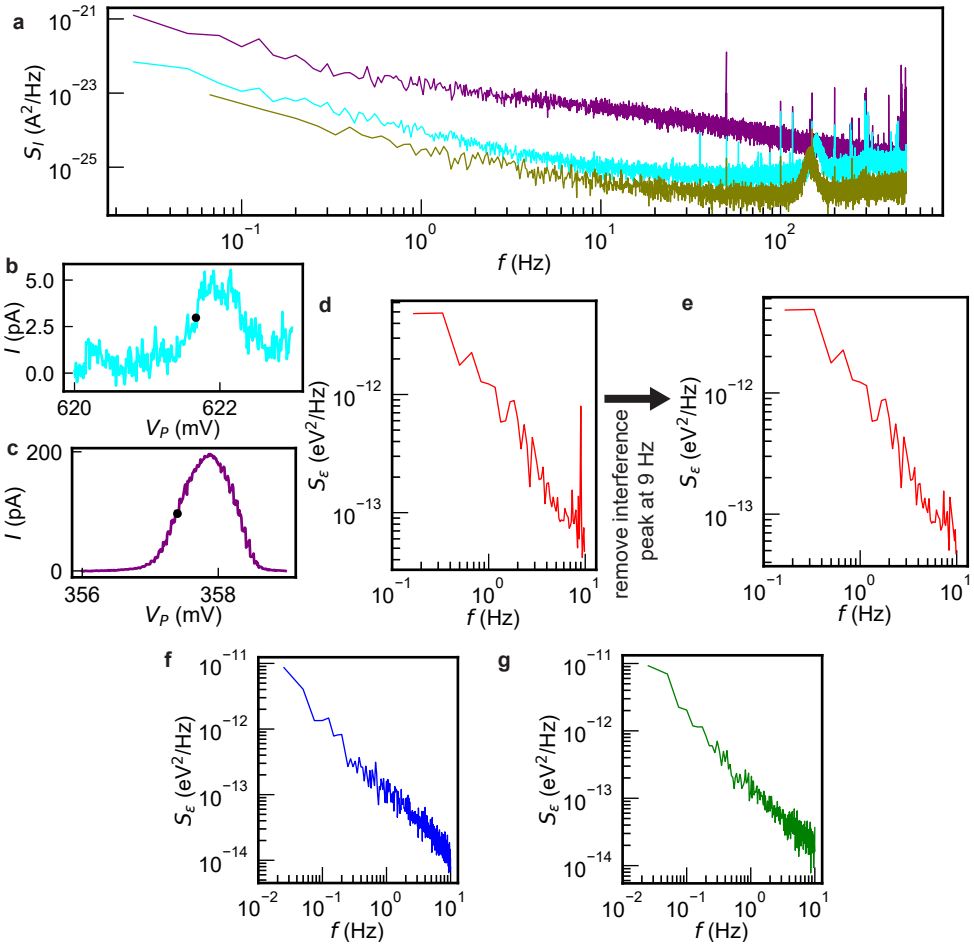


Figure 8.7: **a** Comparison of the charge noise spectrum under different measurement conditions. Lemon shows a current noise spectrum measured in Coulomb blockade on a test device from heterostructure B, indicative of the noise floor of our measurement setup. Cyan shows a current noise spectrum, measured on a device from heterostructure B on the flank of a highly-resistive Coulomb peak at a source-drain current of $\simeq$ 3 pA. Purple shows a current noise spectrum, measured on a device from heterostructure C on the flank of a less resistive Coulomb peak at a measured source-drain current of $\simeq$ 100 pA. Lemon and cyan curves show a broad interference peak at 150 Hz, as well as a flattening out of the curve at $\approx$40 Hz. **b** Coulomb peak from which the noise spectrum from heterostructure B (cyan curve in **a**) is measured. The flank of the Coulomb peak is indicated with a black dot. The Coulomb peak is highly resistive, with a source drain current at peak of $\simeq$ 5 pA, but the charge noise spectrum in **a** (cyan curve) is still distinguishable from the typical noise floor. **c** Coulomb peak from which the noise spectrum from heterostructure C (purple curve in **a**) is measured. The flank of the Coulomb peak is indicated with a black dot. **d** Charge noise measurement of Heterostructure A with an interference peak at 9 Hz arising from the measurement module. In **e** we remove the interference peak from the analysis. **f** Charge noise measurement of Heterostructure B with a different measurement module, where the interference peak is not present. **g** Charge noise measurement of Heterostructure C with the same measurement module as in **f**. The interference peak is not visible.

### 8.8.4. OPERATION GATE VOLTAGES FOR CHARGE SENSOR QUANTUM DOTS

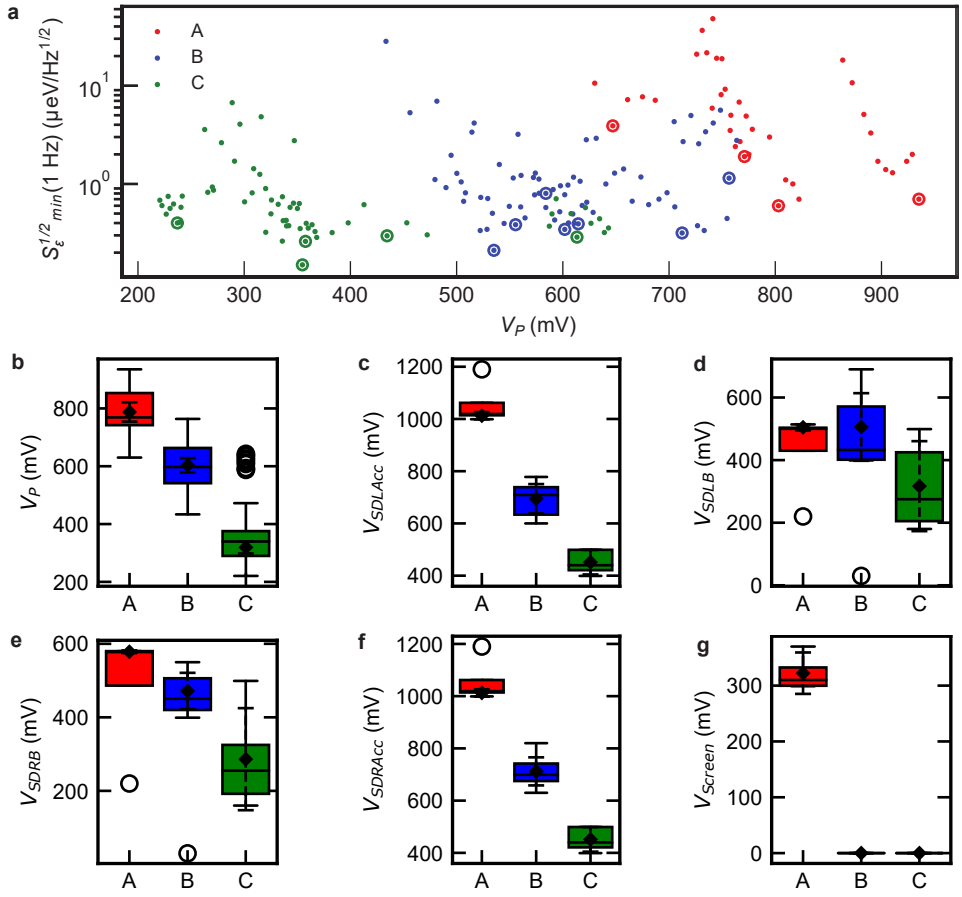


Figure 8.8: **a** Charge noise $S_\epsilon^{1/2}$ at 1 Hz as a function of the plunger gate voltage $V_P$ for all measured devices of heterostructure A (red), B (blue), C (green). The circled dots highlight the minimum $S_{\epsilon,min}^{1/2}$ at 1 Hz for each device upon varying $V_P$ within the range considered. For a given heterostructure, these $S_{\epsilon,min}^{1/2}$ values make up the distributions plotted in Fig. 2e of the main text. We recall that heterostructure A features a ≃ 9 nm thick quantum well and is terminated with an epitaxial Si cap grown by dichlorosilane at 675 °C. Heterostructure B has also a ≃ 9 nm thick quantum well but features an amorphous Si-rich layer obtained by exposing the SiGe barrier to dichlorosilane at 500 °C. Heterostructure C, having the same amorphous Si-rich termination as in heterostructure B, but a thinner quantum well of ≃ 5 nm. **b-g** Distributions of the operation gate voltages of the plunger, SDLAcc, SDLB, SDRB, SDRAcc, and screening gates, respectively (see Fig. 1**f** in the main text) for heterostructure A (red, 4 devices measured), B (blue, 8 devices measured), and C (green, 5 devices measured). With the exception of gate SDLB, all operation voltages of the charge sensor are highest in heterostructure A and lowest in heterostructure C with a difference of up to 600 mV. Note that a global screening gate is only used for the operation of heterostructure A. Quartile box plots, mode (horizontal line), means (diamonds), 99% confidence intervals of the mean (dashed whiskers), and outliers (circles) are shown.

### 8.8.5. LEVER ARM EXTRACTION

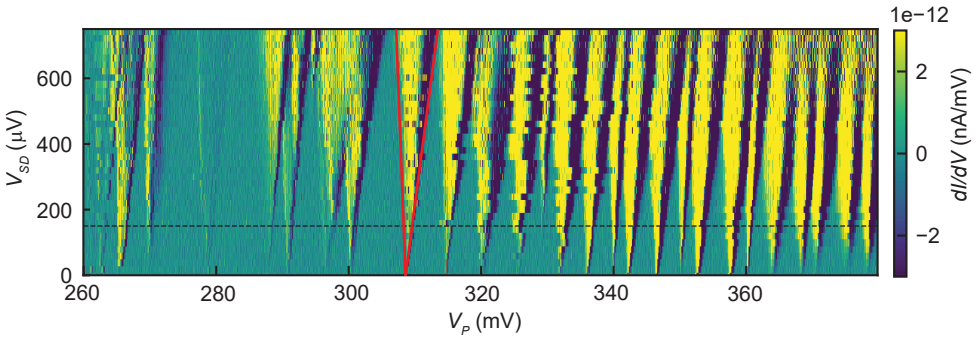


Figure 8.9: Differential conductance ($dI/dV$) showing representative Coulomb blockade diamonds as a function of the source-drain voltage ($V_{SD}$) and plunger gate voltage ($V_P$) for heterostructure C. We derive the two slopes $m_S$ and $m_D$ on both sides of each Coulomb diamond. Using the equation $a = |\frac{m_S m_D}{m_S - m_D}|$, we extract a lever arm of $a = 0.12$ eV/V for the Coulomb peak at $V_P \approx 308$ mV, where we indicate $m_S$ and $m_D$ with magenta lines. The dashed line indicates the source-drain voltage used for the charge noise measurements.

### 8.8.6. SIMULATIONS OF DEPHASING TIMES AND GATE FIDELITIES

Charge noise as measured in this paper leads to a loss of coherence for all kinds of quantum states. For qubit systems such decoherence can be described by 2 reference numbers. The qubit's relaxation time $T_1$ and it's dephasing time $T_2$. Low frequency charge noise as measured dominantly affects the dephasing time $T_2^\star$ of a qubit. Here, $T_2^\star$ references the free induction decay of a Ramsey experiment and describes the decay of a superposition state due to fluctuations in the qubit's resonance frequency. The dephasing time $T_2^\star$ depends on the characteristics of the noise as well as the susceptibility of the qubit to the fluctuations. In short, charge qubits are more susceptible to charge noise than spin qubits. For a general qubit with energies $\mathscr{E}$ the dephasing time can be expressed as

$$T_2^\star = \frac{h}{\sqrt{2}\pi \left|\frac{\partial \mathscr{E}}{\partial \mu}\right| \sqrt{2\int_{f_{\mathrm{lf}}}^{f_{\mathrm{hf}}} S_\epsilon(f)\,df}}, \tag{8.9}$$

where $S_\epsilon$ is the measured noise spectral density of the chemical potential $\mu$ and $f_{\mathrm{hf,(lf)}}$ are the high (low-) frequency cut-off frequency. Note, that this simple expression for the dephasing time only holds away from a sweet spot [265, 266], $\frac{\partial \mathscr{E}}{\partial \mu} = 0$.

#### DEPHASING OF CHARGE QUBIT

A charge qubit in general consist of two charge states with a difference in chemical potential $\epsilon = \mu_2 - \mu_1$ that are coupled via a tunnel matrix element $t_c$. Such a system can be described by the simple Hamiltonian

$$H = \frac{\epsilon}{2}\sigma_z + t_c\sigma_x, \tag{8.10}$$

where $\sigma_x$, $\sigma_y$, and $\sigma_z$ are the three Pauli matrices. Charge noise couples to the charge qubit directly via their chemical potentials. As a consequence a charge qubit is maximally susceptible to charge noise and we find $\frac{\partial \mathscr{E}}{\partial \mu} = 1$ in the regime $\epsilon \gg t_c$. We take the values for the frequency cut-offs $f_{\text{hf}} = 33GHz$ and $f_{\text{lf}} = 20Hz$ from Ref. [260] for our simulation to ease comparison.

### DEPHASING OF SPIN QUBIT

A spin qubit is ideally not affected by changes in the electrostatic environment from charge noise. However, due to intrinsic spin-orbit interaction (SOI) and artificial SOI through a micromagnet charge noise can couple to the spin degree of freedom. For a spin qubit made in SiGe using a micromagnet we find

$$\frac{\partial \mathscr{E}}{\partial \mu} = \alpha_{\text{sensor}} \frac{\partial x}{\partial V} \frac{\partial B_z}{\partial x} \mu_B g = 1.6 \times 10^{-5} \frac{\partial \mathscr{E}}{\partial \mu} = \alpha_{\text{sensor}} \frac{\partial x}{\partial V} \frac{\partial B_z}{\partial x} \mu_B g = 1.6 \times 10^{-5} \tag{8.11}$$

with the voltage displacement $\frac{\partial x}{\partial V} = 0.024nm/mV$, field gradient $\frac{\partial B_z}{\partial x} = 0.08mT/nm$, Bohr's Magneton $\mu_B = 0.0579\mu eV/mT$, g-factor $g = 2$, lever arm $\alpha_{\text{sensor}} = 0.07eV/V$, and frequency cut-offs $f_{\text{hf}} = 10kHz$ and $f_{\text{lf}} = 1.6mHz$ all taken from Ref. [111].

### GATE FIDELITY SIMULATIONS

In order to extrapolate the performance of a two-qubit CZ gate from the measured charge noise we perform numerical simulations. The details of the simulations are described in Ref. [115] using the measured charge noise as an input. We simulate the unitary evolution operator of a CZ two-qubit gate using adiabatic barrier control at the detuning charge noise sweet spot. Colored charge noise is numerically generated using the Fourier filter method [267, 268] and added to the control pulses. For the simulation we use an additional heuristic lever arm $\alpha_{\text{barrier}} = 1mV/\mu eV$ into consideration to translate the measured fluctuations in chemical potential to fluctuations in barrier voltage in the simulation. With this specification the charge noise measured in Ref. [115] would translate to $S_\epsilon^{1/2} = 0.4\mu eV/Hz^{1/2}$, a reasonable assumption. To benchmark the performance we compute the average gate infidelity a commonly used metric for the quality of gates for all measured spectral densities $S_\epsilon(f) = S_\epsilon/f^\alpha$.

# 9

# $^{28}$Si/SiGe heterostructure performance in qubit experiments

*There is plenty of room at the bottom.*

Richard Feynman

Parts of this chapter have been published in Xiao Xue*, Bishnu Patra*, Jeroen P. G. van Dijk*, Nodar Samkharadze, Sushil Subramanian, Andrea Corna, Brian Paquelet Wuetz, Charles Jeon, Farhana Sheikh, Esdras Juarez-Hernandez, Brando Perez Esparza, Huzaifa Rampurawala, Brent Carlton, Surej Ravikumar, Carlos Nieva, Sungwon Kim, Hyung-Jin Lee, Amir Sammak, Giordano Scappucci, Menno Veldhorst, Fabio Sebastiano, Masoud Babaie, Stefano Pellerano, Edoardo Charbon Lieven M. K. Vandersypen, CMOS-based cryogenic control of silicon quantum circuits, Nature **593**, 205–210 (2021) [51]

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*These authors have contributed equally

Future quantum computers capable of solving relevant problems will comprise two main building blocks — classical instrumentation to generate control signals (input) and to process readout signals (output)[269, 270, 181] and a quantum processing unit (QPU) with millions of qubits [269, 20, 271].

In current solid-state qubit implementations, such as spin-, superconducting-, or photonic-qubits an important interconnect bottleneck arises between the room temperature electronics and the quantum chip in a dilution refrigerator. Advanced lithography supports the fabrication of both control electronics and qubits in silicon using technology compatible with complementary metal oxide semiconductors (CMOS)[270]. When the electronics are designed to operate at cryogenic temperatures, they can ultimately be integrated with the qubits on the same die or package, providing a path to overcome the wiring bottleneck.

Moreover, the QPU requires a large qubit count combining high fidelity gate operation and high fidelity qubit initialization and readout. Spins in semiconductor quantum dots show long-term promise for scalable QPUs but demonstrations so far typically have used one to four qubits to optimize for either the fidelity of single- and two-qubit operations, or qubit initialization and readout.

This chapter mainly shows the results of Refs. [51] and [50], highlighting the key material improvements in Si/SiGe heterostructures that have enabled the implementation of CMOS-based cryogenic control of a silicon quantum circuit [51] and for the realization of a six-qubit quantum processor with high fidelity gate operations, initialization, and readout [50]. Both experiments together demonstrate the potential of using Si/SiGe heterostructures for a scalable quantum computing architecture.

## 9.1. CMOS-BASED CRYOGENIC CONTROL OF QUANTUM CIRCUITS IN Si/SiGe HETEROSTRUCTURES

A standard setup for semiconducting or superconducting qubits has the qubits operating in a dilution refrigerator at about 20 mK, whereas bulky microwave vector sources and arbitrary waveform generators are at room temperature (RT) and connected to the qubits via long cables and attenuators (Fig. 9.1, left). This approach has recently enabled an experimental demonstration of the advantage of quantum computing over classical computing in a random circuit sampling experiment that utilizes a superconducting quantum processor consisting of 53 qubits [18]. This system requires more than 200 coaxial control lines from RT to the quantum chip, which is operated below 20mK. This brute-force approach to reach higher qubit numbers will soon reach its limits. A promising path forward is to bring the control electronics close to the quantum chip, at cryogenic temperatures. Although important steps in this direction have been taken [273, 183, 274, 275, 276, 277, 278, 279, 280, 281], high-fidelity multi-qubit control and a universal gate set remain to be demonstrated using cryogenic controllers. A central challenge is that the power dissipation of the control electronics easily surpasses the typical cooling power of 10 μW available at 20 mK [282, 283]. Because silicon spin qubits can be operated and measured above 1 K [182, 189, 284], they are well positioned for overcoming the wiring bottleneck by on-die or on-package co-integration with classical electronics (Fig. 9.1, right) at a temperature of 1–3 K, where the cooling power is orders of magnitude

higher than at millikelvin temperatures.

A cryogenic quantum controller for practical quantum information processing must meet multiple criteria: a form factor compatible with integration in a cryogenic refrigerator; frequency multiplexing to facilitate scalability; low power consumption within the limit of refrigerator cooling power; sufficiently high output power to enable fast operations compared to the qubit coherence times; high signal-to-noise ratio (SNR) and spurious-free-dynamic-range (SFDR) for high-fidelity control; the ability to generate tailored pulse shapes and perform a universal set of quantum operations; an integrated instruction set memory for the efficient execution of complex algorithms. All these requirements can be met by commercial CMOS circuits designed to operate at a few K.

In Ref. [51], a quantum control chip is utilized operating at 3 K (cryo-controller, named Horse Ridge) and fabricated using Intel 22 nm-FinFET low-power CMOS technology [275] to coherently control two electron spin qubits in a silicon double quantum dot. In order to benchmark the limits of the controller, the qubits are kept at ~20 mK, where they are most coherent and the non-idealities of the control chip can be assessed best (Figure 9.1, middle). Extensive electrical characterization and benchmarking using the quantum processor show that the cryo-controller meets all the above criteria.

For this study the key material contribution is to provide a substrate, that may host a reliable two-qubit quantum processor such that the coherent control achieved with the cryo-controller can be benchmarked with respect to coherent control performance

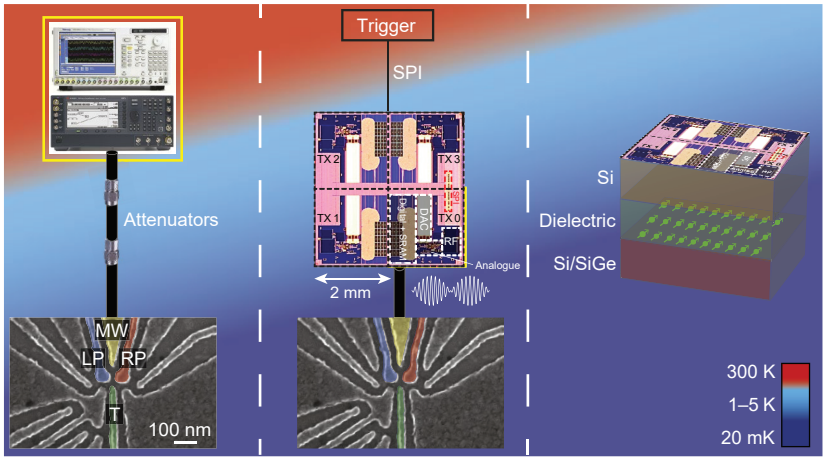



Figure 9.1: Three stages of development of the control system towards full integration. Left, RT instruments connected to qubits via coaxial lines and attenuators. Middle, cryo-controller at 1–5 K (see Extended Data Fig. 2 of Ref. [51]) directly connected to the qubits and triggered from RT using an SPI, which leaves the wiring from 1–5 K to the qubit sample unaltered, but brings a considerable reduction in the wire count from RT to 1–5 K when targeting many qubits. Right, a future perspective of fully integrated control electronics and qubits on the same package/die, eliminating dense wiring all the way down to the package/die (note that the vision is not one transmitter above every qubit, so the qubit and transmitter form factor can be different [181, 272]). Two single electron spins used as qubits are located underneath gates LP (blue) and RP (red), as shown in the SEM image. Multiplexed microwave signals are sent to gate MW (yellow) to control both qubits. Gate T (green) is used to tune the coupling between the qubits

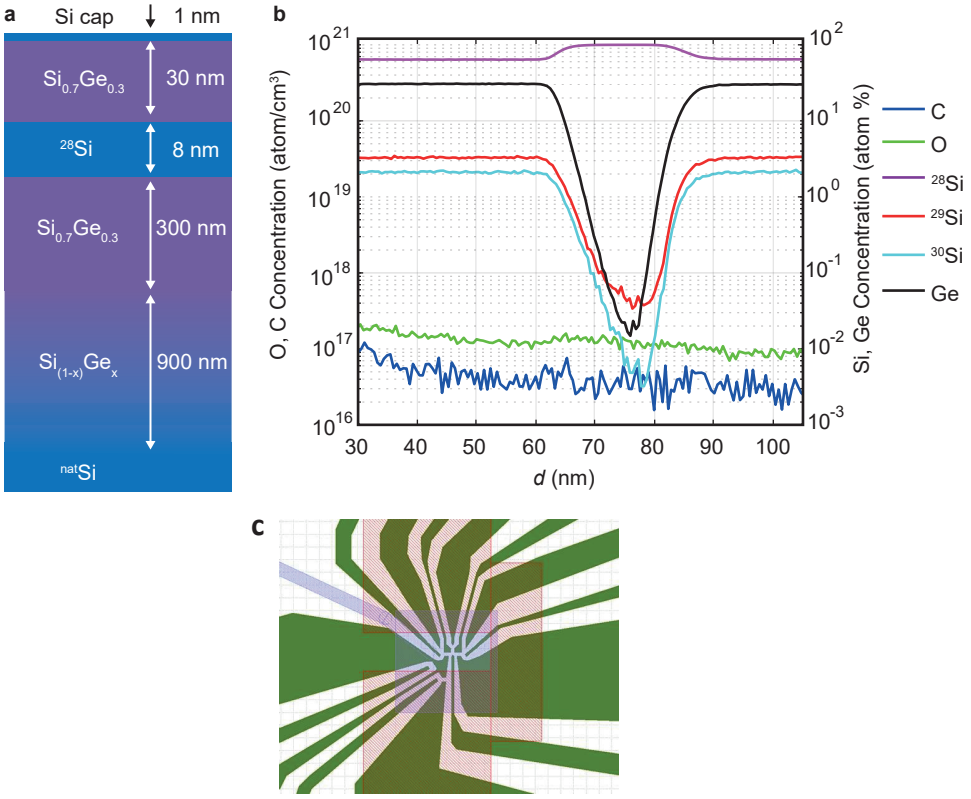



Figure 9.2: **a**, Wafer stack schematic with corresponding layer thicknesses. **b**, Depth concentration SIMS profile of $^{28}$Si (red), $^{29}$Si (blue), $^{30}$Si (purple), Ge (black), oxygen (green) and carbon (blue). The residual $^{29}$Si concentration in the quantum well is 0.08 %, considerably reducing qubit decoherence due to hyperfine interaction. Both carbon and oxygen concentrations are below their respective detection limits of $3 \times 10^{16}$ cm$^{-3}$ and $1 \times 10^{17}$ cm$^{-3}$ . **c**, Schematic showing the first and second Al gate layers in green and purple, respectively. A cobalt micro-magnet is located on top of the metallic gates (pink-shaded area).

9

against state-of-the-art room temperature electronics. Qubits that can be resonantly controlled with drive frequencies in the 2-20 GHz band are targeted, covering the typical resonance frequencies of both superconducting and spin qubits [168, 173, 285, 182, 274]. To realize these specifications we provide, for the first time within the qubit experiments in Delft, $^{28}$Si/SiGe heterostructures to suppress the decoherence through hyperfine interaction [42]. In figure 9.2**a** we see a schematic of wafer stack which comprises a Si substrate, a 900 nm linearly graded $Si_{(1-x)}Ge_x$ layer (Ge concentration x varied from 0 to 0.3), followed by a 300 nm strain-relaxed $Si_{0.7}Ge_{0.3}$ buffer layer, an 8 nm tensile strained $^{28}$Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a 1 nm sacrificial Si cap. These undoped $^{28}$Si/SiGe heterostructures support via gating the accumulation of a two-dimensional electron gas with a transport mobility of up to 1x10$^5$cm$^2$/Vs at 55 mK [225].

Figure 9.2**b** shows concentration profiles obtained by secondary ion mass spectroscopy (SIMS) of a control $^{28}$Si/SiGe heterostructure. This control $^{28}$Si/SiGe heterostructure

has an increased quantum well thickness of 20 nm, which facilitates the investigation of the chemical composition therein by reducing the impact of the knock-on SIMS artifact [286]. The concentration profiles of isotopes of Ge, $^{28}$Si, $^{29}$Si, and $^{30}$Si show a high-purity and homogeneous $^{28}$Si quantum well. The residual concentration of non-zero spin nuclei $^{29}$Si is reduced from 3.29% in the $Si_{0.7}Ge_{0.3}$ buffer and barrier to 0.08% in the quantum well, demonstrating that the $^{28}SiH_4$ precursor purity is maintained during the heterostructure deposition process. As a result, we achieve a suitable solid-state environment for the qubits where decoherence due to hyperfine interaction is minimized. Furthermore, the concentration of common background contaminants C and O is below the detection limit of around $3{\times}10^{16}$ cm$^{-3}$ and $1{\times}10^{17}$ cm$^{-3}$, respectively, reducing scattering sources in the qubit surrounding environment which can be sources of charge noise.

The quantum processor is made of a double quantum dot (DQD) electrostatically confined in the quantum well of the $^{28}$Si/SiGe heterostructure. By tuning the voltage on plunger gates LP and RP, two single electrons are locally accumulated underneath each gate, shown in blue and red in the scanning electron microscope (SEM) image in figure 9.1. By applying an external magnetic field of 380 mT, combined with the longitudinal magnetic field induced by a micro-magnet on top of the DQD (see figure 9.2**c**), the qubit states are encoded into the Zeeman split states of the two electrons, where spin-up is used as $|1\rangle$ and spin-down is used as $|0\rangle$. The resonance frequencies of Qubit 1 ($Q_1$, underneath gate LP) and Qubit 2 ($Q_2$, underneath gate RP) are 13.62 GHz and 13.51 Ghz with dephasing times $T_2^\star$ of 20.5 µs and 9.4 µs, respectively [115]. Rotations around the $\hat{x}$ and $\hat{y}$ axes are implemented by sending microwave bursts with the microwave phase controlling the rotation axis, e.g. an in-phase (quadrature) microwave burst implements a rotation about $\hat{x}$ ($\hat{y}$). The microwave bursts are applied to gate MW, which drives electric-dipole spin resonance (EDSR) enabled by the transverse magnetic field gradient from the micro-magnet [287], while the rotation around the $\hat{z}$ axis (phase control) is achieved by changing the reference phase in the cryo-controller, which adds a phase shift to all the subsequent bursts [29]. The two-qubit interaction is mediated by the exchange coupling ($J$) between the two spins [288], controlled by gate T. Its effect here is to shift the anti-parallel spin states down in energy [289]. As a result, the resonance frequency of each qubit now depends on the state of the other qubit, allowing conditional operations on each qubit via narrow-band microwave bursts [173, 285]. The corresponding four different frequencies can be individually addressed using frequency multiplexing. Both qubits are read out in single-shot mode [290].

Here we only summarize the results of Ref. [51] because the extensive electrical characterization therein is beyond the scope of this thesis. In Ref. [51] we see versatile programmability of a cryogenic quantum circuit, combined with a signal quality allowing up to 99.99 % gate fidelities, a footprint of just 4 mm$^2$, a power consumption of 384 mW, the ability to integrate multiple transmitters on one die, and operation at 3 K. All together this demonstrates the potential of the cryo-controller to address key challenges in building a large-scale quantum computer. Optimized design of cryogenic CMOS circuits - for example, the use of a narrower frequency band — can substantially reduce the power consumption (see Methods of Ref. [51]) and make it possible to work at 1K or even lower temperatures. Furthermore, FinFET quantum dots that are fully compatible with CMOS

processing [270] and increased operating temperatures (about 1K) of spin qubits show only a modest reduction in coherence times [189, 182]. These advances imply that it may be possible to fully integrate the quantum processor with the classical controller on chip or by flip-chip technology, lifting a major roadblock in scaling.

## 9.2. A SIX QUBIT QUANTUM PROCESSOR USING SI/SIGE HETEROSTRUCTURES

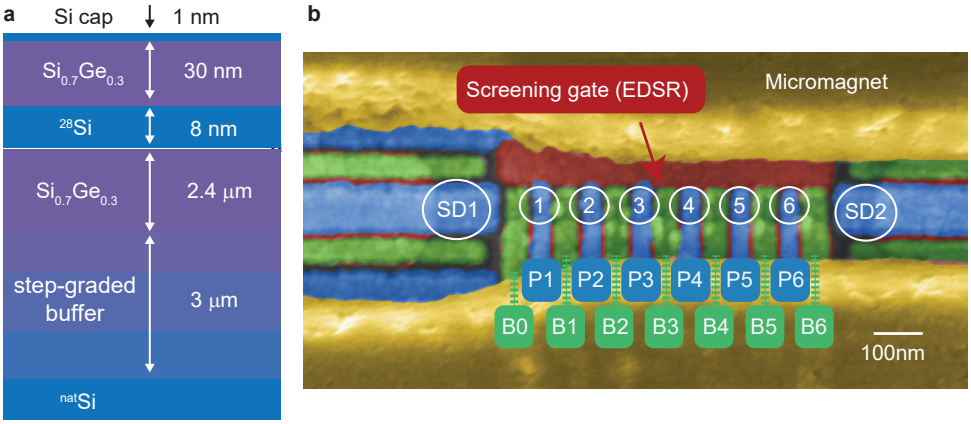
On the path to practical large-scale quantum computation, electron spin qubits in semiconductor quantum dots [207] show promise due to their inherent potential for scaling through their small size [291, 191], long-lived coherence [184] and compatibility with advanced semiconductor manufacturing techniques [208]. Nevertheless, spin qubits currently lag behind in scale when compared to superconducting, trapped ions and photonic platforms, which have demonstrated control of several dozen qubits [18, 292, 19]. By comparison, using semiconductor spin qubits, control of up to four qubits was achieved [293] and entanglement of up to three qubits was demonstrated [210, 253, 294].

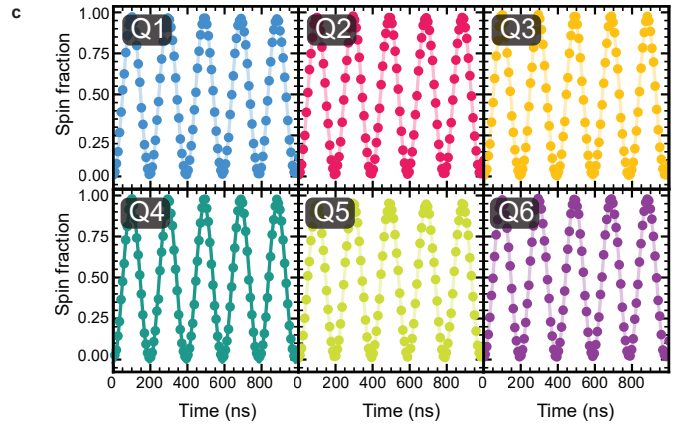
Furthermore, the experience with other qubit platforms shows that in scaling up, maintaining the quality of the control requires significant efforts, for instance to deal with the denser motional spectrum in trapped ions [295], to avert cross-talk in superconducting circuits [296] or to avoid increased losses in photonic circuits [297]. For small semiconductor spin qubit systems, state-of-the-art single-qubit gate fidelities exceed 99.9% [113, 185, 298] and two-qubit gates well above 99% fidelity have been demonstrated recently [115, 114, 231, 253]. Most quantum dot based demonstrations suffer from rather low initialization or readout fidelities, with typical visibilities of no more than 60-75%, with one recent exception [231]. Conversely, high-fidelity spin readout has been claimed based on an analysis of the readout error mechanisms, but these claims have not been validated in combination with high-fidelity qubit control [299, 300]. While high-fidelity initialization, readout, single-qubit gates and two-qubit gates have thus been demonstrated individually in small systems, almost invariably one or more of these parameters are significantly compromised while optimizing others. A major challenge and important direction for the field is therefore to achieve high fidelities for all components while at the same time enlarging the qubit count.



In Ref. [50] our isotopically enriched Si/SiGe enables the study of a system of six spin qubits in a linear quantum dot array and it is tested what performance the array can acheive using known methods such as multi-layer gate patterns for independent control of the two-qubit exchange interaction [301, 167, 225] and micromagnet gradients for electric-dipole spin resonance and selective qubit addressing [302]. Furthermore, several novel techniques for semiconductor qubits are introduced that, collectively, are critical to improve on the results and facilitate scalability, such as initialization by measurement using real-time feedback [303], qubit initialization and measurement without reservoir access, and efficient calibration routines. Initialization and readout circuits span over the full six-qubit array.

For this study the key material contribution is to provide a substrate with high valley splitting for facilitated qubit readout, as well as a uniform and low-noise environment for homogeneous qubit properties and exchange coupling. To realize these specifica-




d

| QD/Qubit | $E_{ST}$ (μeV) | $T_2^*$ (us) | $T_2^h$ (us) | Vis (%) | 1-F (%) |
|---|---|---|---|---|---|
| 1 | 199.2±47.1 | 3.0±0.2 | 14.0±3.2 | 95.5 | 0.23±0.04 |
| 2 | 229±35.5 | 2.5±0.1 | 21.1±6.7 | 95.5 | 0.13±0.02 |
| 3 | 132.6±34.1 | 3.7±0.3 | 40.1±4.5 | 98 | 0.04±0.01 |
| 4 | 84.8±31.3 | 3.7±0.3 | 37.2±3.8 | 97 | 0.12±0.02 |
| 5 | 171.3±35.4 | 5.9±0.4 | 44.7±8.2 | 93.5 | 0.09±0.02 |
| 6 | 323±23.8 | 5.1±0.4 | 26.7±4.8 | 96.5 | 0.11±0.01 |

Figure 9.3: **a** Wafer stack schematic with corresponding layer thicknesses. **b** A false-colored scanning electron microscope image of a device similar to the one used in the experiments. Each color represents a different metallization layer. Plunger (blue) and barrier (green) gates are used to define quantum dots in the channel between the screening gates (red). Two cobalt micromagnets (yellow) are placed on top of the gate stack. **c** Rabi oscillations for every qubit, taken sequentially. The spin fraction refers to the spin-up fraction for qubits 2-5 and to the spin-down fraction for qubits 1 and 6. The drive amplitudes were adjusted in order to obtain uniform Rabi frequencies of 5 MHz. **d** Table showing the valley splitting $E_{ST}$, dephasing time $T_2^*$, Hahn echo decay time, visibilites and error for each qubit.

tions we provide $^{28}$Si/SiGe heterostructure to suppress the decoherence through hyperfine interaction [42], with sharp quantum well interfaces [73] for high valley splitting [67], and a thick virtual substrate to reduce misfit and threading dislocations since these crystalline defects compromise the uniformity of the disorder landscape through the creation of recombination-generation sites for charge carriers [60, 61]. In figure 9.3**a** we see a schematic of wafer stack which comprises a Si substrate, a 3 µm step-graded $Si_{1-x}Ge_x$ layer with a final Ge concentration of x = 0.3 achieved in four grading steps (x = 0.07, 0.14, 0.21, and 0.3), followed by a 2.4 µm strain-relaxed $Si_{0.7}Ge_{0.3}$ buffer layer, an 8 nm tensile strained $^{28}$Si quantum well, a 30 nm $Si_{0.7}Ge_{0.3}$ barrier, and a 1 nm sacrificial Si cap. These undoped $^{28}$Si/SiGe heterostructures support via gating the accumulation of a two-dimensional electron gas with a transport mobility of up to $2.9x10^5 cm^2/Vs$ at 1.6 K [230].

The six-qubit array is defined electrostatically in the $^{28}$Si quantum well of a $^{28}$Si/SiGe heterostructure, between two sensing quantum dots, as seen in Figure 9.3**b**. The multilayer gate pattern allows for excellent control of the charge occupation of each quantum dot, and of the tunnel couplings between neighbouring quantum dots. These parameters are controlled independently through linear combinations of gate voltages, known as virtual gates [304]. The inter-dot pitch is chosen to be 90 nm, which for this 30 nm deep quantum well yields easy access to the regime with one electron in each dot, for short indicated as the (1,1,1,1,1,1) charge occupation.

## 9.3. PERFORMANCE OF THE QUANTUM PROCESSOR

The qubits are manipulated via electric-dipole spin resonance (EDSR) [305]. A micromagnet located above the gate-stack is designed to provide both qubit addressability and a driving field gradient (see Fig. 9.3**b** and Supplementary Data of Ref. [50]).Coherent Rabi oscillations are driven as depicted in figure 9.3**c**, where no visible damping in the first five periods is observed, indicating a clean and uniform qubit host matrix. Single-qubit gate fidelities are assessed via randomized benchmarking experiments. All average single-qubit gate fidelities are between 99.77% ± 0.04 and 99.96% ± 0.01, which demonstrates that even within this extended qubit array, high-fidelity single-qubit control is retained. The single qubit fidelity as well as the coherence times of each qubit are tabulated in figure 9.3**f**. Spin coherence is expected to be limited by charge noise coupling in by the micromagnet [306].

We measure valley splitting using magnetospectroscopy along the $N = (1,1) \rightarrow (2,0)$ transition. The signal is measured by monitoring the reflected amplitude of the rf readout signal through a nearby charge sensor as a function of plunger gate voltage $V_P$ and absolute magnetic field $|B|$. To extract the inflection point of the electron charge transition, we fit the signal of the detuning for every magnetic field to eq. (2) from Ref. [227]. To extract $B_{ST}$ we use the fitting routine discussed in chapter 6. On top of these samples there is a micromagnet lowering the magnetic field strength at the center of the sample, making the measured value a lower bound for $E_{ST}$. Low valley splittings on Si/SiGe devices have hindered progress in the past [213], but in this device all valley splittings are in the range of 100-300 µeV (see figure 9.3**d** and figure 9.4**a**-**f**).

Again, we summarize additional results of Ref. [50] because the initialization and readout schemes, as well as the 2-qubit and 3-qubit characterizations therein are be-

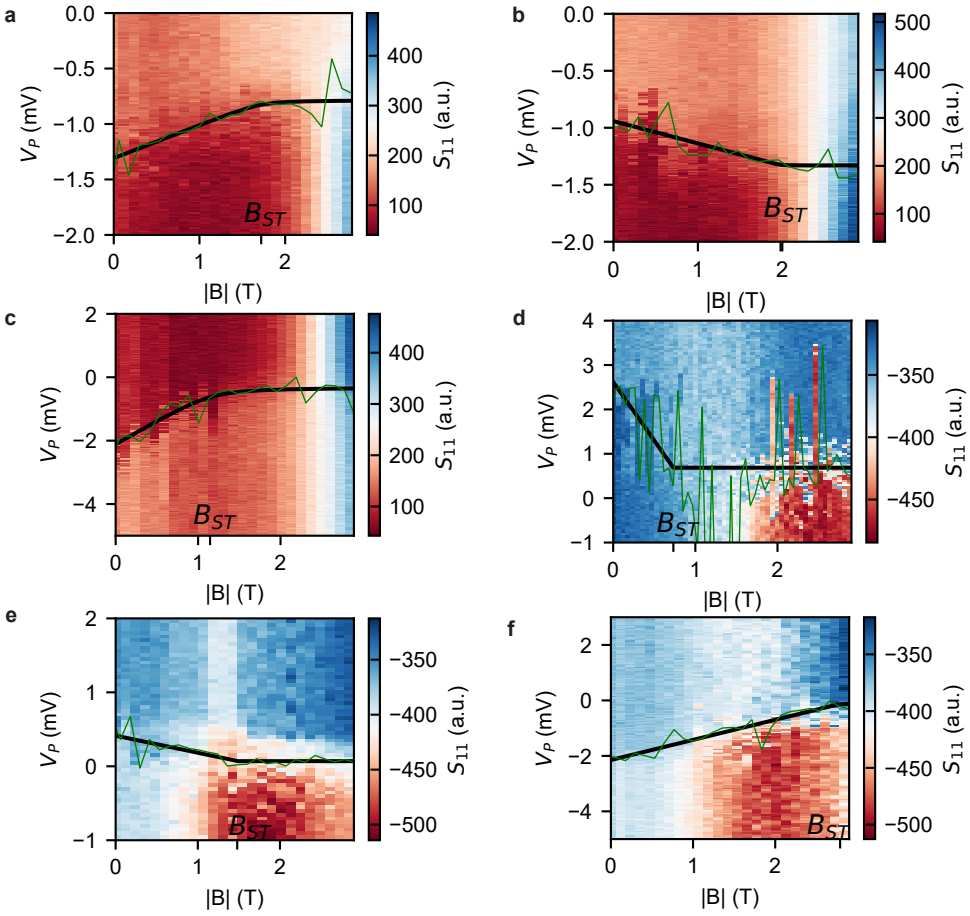



Figure 9.4: Magnetospectroscopy of each quantum dot of the six-qubit register. Along the (1,1)→(2,0) transition. We superimpose the inflection points of the charge transitions as green curves, to help the reader to follow the charge transitions. $V_P$ is the gate voltage applied to the plunger gate forming the quantum dot. For clarity, we subtract from $V_P$ in panels **a** - **f** an offset that depends on the quantum dot being measured.



yond the scope of this thesis. In Ref. [50] we see scaling to a record number of qubits for a quantum dot system, and Rabi oscillations for each qubit with visibilities of 93.5-98% are achieved (see figure 9.3**f**, implying high readout and initialization fidelities. Initialization uses a novel scheme relying on qubit measurement and real-time feedback. Readout relies on Pauli spin blockade and quantum-non-demolition measurements. This combination of initialization and readout allows the device to be operated while retaining the six electrons in the linear quantum dot array, alleviating the need for access to electron reservoirs. All single-qubit gate fidelities are around 99.9% and the high quality of the two-qubit gates can be inferred from the 89-95% fidelity Bell states prepared across the array. The development of a modular software stack, efficient calibration routines and reliable device fabrication have been essential for this experiment. Future work must

focus on understanding and mitigating heating effects leading to frequency shifts and reduced dephasing times, as this is found to be the limiting factor in executing complicated quantum circuits on many qubits. The use of simultaneous single-qubit rotations and simultaneous two-qubit CZ gates will keep pulse sequences more compact. This will require accounting for cross-talk effects, which is anticipated to be easiest for the two-qubit gates. The authors estimate that the concepts used for control, initialization and readout can be used without substantial modification in arrays that are twice as long, as well as in small two-dimensional arrays. Scaling further will require additional elements such as cross-bar addressing or on-chip quantum links [181].

## 9.4. SUPPLEMENTARY INFORMATION

### 9.4.1. DEVICE FABRICATION

**Single-layer double-quantum dot**: On top of the heterostructure, a 7 nm thick $AlO_x$ layer is deposited using atomic-layer deposition, followed by a 20 nm Al metal film, which is patterned using electron beam lithography in order to define the first gate layer, which shapes the potential landscape. Next, another 7 nm AlOx layer is deposited, followed by a 70 nm Al layer that uniformly covers the quantum dot area. Finally, a 200 nm Co film is deposited and patterned into a micro-magnet.

**Multi-layer six-qubit register**: Devices are fabricated on an undoped $^{28}$Si/SiGe heterostructure featuring an 8 nm strained $^{28}$Si quantum well, with a residual $^{29}$Si concentration of 0.08%, grown on a strain-relaxed $Si_{0.7}Ge_{0.3}$ buffer layer. The quantum well is separated from the surface by a 30 nm thick $Si_{0.7}Ge_{0.3}$ spacer and a sacrificial 1 nm Si capping layer. The gate stack consists of 3 layers of Ti:Pd metallic gates (3:17, 3:27, 3:27 nm) isolated from each other by 5 nm $Al_2O_3$ dielectrics, deposited using atomic layer deposition. A ferromagnetic Ti:Co (5:200 nm) layer on top of the gate stack creates a local magnetic field gradient for qubit addressing and manipulation. Further details of device fabrication methods can be found at [225].

# 10

# Discussion and Outlook

*What I love about science is that as you learn, you don't really get answers. You just get better questions.*

John Green

Buried quantum wells in $^{28}$Si/SiGe heterostructures are an established material platform for spin qubit research. Over the past four years we have seen high fidelity single- [112, 113] and two-qubit gates[115, 114, 231], integration into a cryogenic CMOS architecture [51], spin-photon [171, 172] and spin-spin coupling [232], and universal control of a six qubit register [50]. Many of these achievements have been achieved with Delft grown $^{28}$Si/SiGe heterostructures, also used by the Tarucha group at RIKEN [114] emphasizing the reproducible quality of the material stacks. A major contribution to these achievements have been material improvements such as reduced hyperfine interaction (chapter 9) or charge noise (chapter 8) and increased valley splitting (chapter 6 and 9), which in turn have been enabled through fast but rigorous material-device-measurement feedback cycles (chapter 4). Particularly under the aspect of fast assessment of material quality, Hall-bar-shaped H-FETs have proven to be extremely useful since we can estimate the valley splitting from quantum Hall edge states (chapter 5) and assess the impurity densities present in the system (chapter 7 and 8). Accompanied with metrology techniques such as TEM for structural characterization, SIMS, APT, and EELS for chemical analysis and Raman spectroscopy for local strain measurements, we now have an overview of different disorder types that possibly limit QPU performance.

Considering that most of the results mentioned above from Delft-grown $^{28}$Si/SiGe heterostructures are obtained using materials with a 1 nm epitaxial Si cap and an 9 nm thick quantum well we speculate, that the new generation of material stacks studied in chapter 8 with a passivated cap and 5 nm thick quantum wells, could enable devices with a higher qubit count and lower error rates (see chapter 8). QPUs that realize these requirements would put the spin qubit platform within reach of near-intermediate-scale-quantum (NISQ) devices, that are able to perform tasks which surpass the performance of today's largest supercomputers [18, 19, 307]. NISQ devices will be useful to explore many-body quantum physics [308, 16], run rudimentary quantum algorithms [18, 19, 307, 29], and could already have an impact on the business community [156].

However, to perform practical quantum algorithms we require much lower error rates (in the order of $10^{-6}$ errors [309]) and many more qubits (in the order of $10^5$-$10^6$ qubits [309]). To aim for these numbers, continued material developments are inevitable, because both qubit quality and quantity, depend on the underlying disorder in the solid-state matrix and the uniformity of the potential landscape on the relevant length scales. Hence, we need to innovate $^{28}$Si/SiGe heterostructures to keep improving on the limiting parameters.

### THE $^{28}$SI QUANTUM WELLS OF THE FUTURE

10

To increase the quality of $^{28}$Si/SiGe heterostructures for spin qubits, we have proposed several ways forward in chapter 6 and 8. In $^{28}$Si/SiGe heterostructures we reduce charge noise by reducing remote impurities and misfit dislocations and extrapolate average two-qubit error rates in the order of $2\times 10^{-3}$ therefore, to reach the desired error rates in the $10^{-6}$ regime we need further improvements in the details of $^{28}$Si/SiGe heterostructures. There are several strategies we can follow which are illustrated in figure 10.1**a** and 10.1**b**.

First, thicker barriers would increase the distance between the remote impurities and the Si quantum well, however the electrical control of the qubits is more challenging if

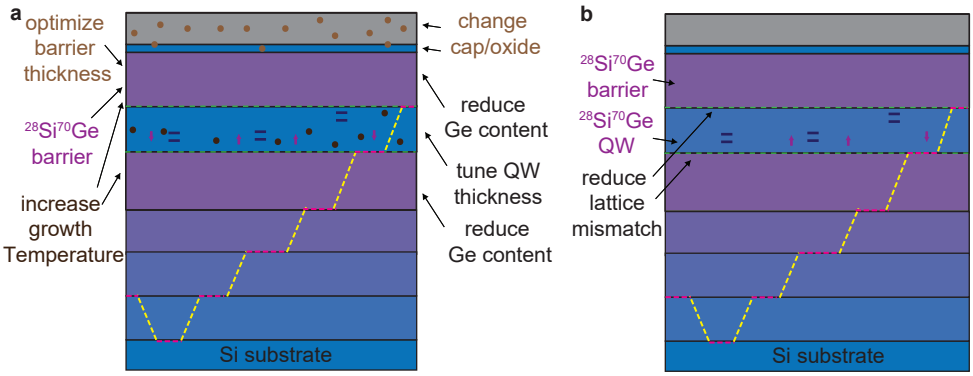



Figure 10.1: **a** Side view schematic of a Si/SiGe heterostructure with gate oxide and performance limiting noise sources: crystalline defects (pink and yellow dashed lines), diffused interfaces (green dashed line), magnetic impurities (purple arrows), background impurities (dark brown circles), ill-defined ground states (short blue parallel lines), and charged impurities (light brown circles). On the sides we see suggestions for changes in the heterostructure quality and the color coding indicates what noise source we intend to address by the respective change. Black indicates that we address both misfit and threading dislocations. **b** Side view schematic of a SiGe/SiGe heterostructure with gate oxide and performance limiting noise sources, which are adressed with this type of heterostructure: crystalline defects (pink and yellow dashed lines), diffused interfaces (green dashed line), magnetic impurities (purple arrows), and ill-defined ground states (short blue parallel lines). On the side we see comments noise source we intend to address by this type of heterostructure stack. Black indicates that we address both misfit and threading dislocations.

the quantum well is buried deeper within the heterostructure. Given the excellent baseline we are starting from, finding the optimal barrier thickness such that impurities are further away, while maintaining good control over the qubits is going to be a rewarding trade off to address in the coming years.

Second, even though our approach of passivating the cap layer to reduce remote impurities has demonstrated a significant increase in wafer-scale performance of mobility, percolation density, and charge noise, it is still important to reduce remote impurities further. Two routes are available: First, we can experiment with different gate oxides that show lower impurities densities, where for example oxides used in the microelectronic industry could provide improvements. Second, we could further experiment with the cap, however the passivation step is a self-terminating thermal process, therefore if we want to reduce impurities in the cap we would need to run an extended study on the cap growth parameters. Studies along these directions have already started in the Scappucci group at the time of writing of this thesis.

Third, although we have seen a promising reduction of misfit dislocations with 4 nm thick quantum wells, the optimal quantum well thickness should be further investigated. The reason is, that in thin quantum wells the electron wavefunction tends to penetrate deeper into the SiGe barrier and in consequence probes the magnetic momentum of the non-zero nuclear spin Si and Ge isotopes, which leads to decoherence. Hence, slightly thicker quantum wells that remain below the critical thickness (e.g. 6-7 nm) could lead to similar misfit dislocation densities while reducing the effect of hyperfine interaction. In addition, thin quantum wells have shown higher valley splitting [212].

Next, reducing the Ge content in the SiGe barriers could reduce misfit and threading dislocations densities through a smaller lattice mismatch, which could lead to further enhancement of the uniformity of the wafer. This approach has led to mobilities over $10^6$ cm$^2$/Vs in Ge/SiGe quantum wells [310]. Similar mobilities are within reach for Si/SiGe quantum wells. One problem of this approach is however that again the electron wavefunction penetrates further into the SiGe barrier, exhibiting the same challenges described in the paragraph above.

Finally, the growth temperature of the SiGe barriers is another key parameter that will need addressing in the near future. In our best performing devices the SiGe barriers around the quantum well are grown at 625 °C mainly to provide sharp quantum well interfaces. However, at this temperature, residual carbon and oxygen atoms in the growth chamber incorporate into the quantum well, which is a source of charge noise [103, 104, 105, 106]. To reduce charge noise from these background impurities we can increase the growth temperature of the barriers at the cost of more diffused quantum well interfaces. Since we also propose diffused quantum well interfaces for enhanced valley splitting in chapter 6, increasing the growth temperature is a viable route to enhance overall spin qubit performance.

Increasing the valley splitting on a wafer-scale will also need special attention. The 6-qubit quantum register from chapter 9 has extraordinarily high valley splitting in the range of 100-300 μeV, and it seems that well defined quantum well interfaces improve valley splitting. However, in chapter 6 we challenge this common picture and propose to increase the overlap of the electron wavefunction with Ge atoms by either using less defined interfaces or, more radically, to increase a small percentage of Ge into the quantum well. In either case, the valley splitting should increase. Especially the case of SiGe quantum wells is interesting because simulations show that we should be able provide heterostructures where 95 % of the qubits experience a valley splitting of ≥ 100 μeV. A beneficial side effect of SiGe quantum wells is the reduced amount of strain necessary to achieve high valley splitting, which also reduces misfit and threading dislocation densities. There are also several considerations to SiGe quantum wells. First, Ge precursors for CVD so far are not isotopically purified and hence the electron wavefunction will probe the magnetic momentum of the non-zero nuclear spin Ge isotopes, a problem that we also experience when growing thin quantum wells or reducing the Ge concentration in the barriers. Second, growing low concentrations of Ge is non-trivial and requires dedicated fine-tuning of growth parameters. Last, Ge atoms could introduce spin-orbit-coupling (SOC) of the electron which leads to spin decoherence [311]. SOC is a double-edged property, because SOC also enables all-electrical control of spin qubits, for example in Ge quantum wells [46, 312, 313] and allows for fast gate-operation times [313]. The promise of high valley splitting, lower strain, and the complicated nature of SOC make SiGe quantum wells a potential material platform for high quality QPUs, that should be further investigated.

Since decoherence through hyperfine interaction with non-zero nuclear spin Si and Ge isotopes seems to be a recurring problem with material changes in $^{28}$Si/SiGe heterostructures, it is crucial to consider growing the SiGe barriers and possible SiGe quantum wells with isotopically purified Si and Ge, which should be exclusively advantageous for spin qubit performance. Nevertheless, one has to keep in mind, that using isotopi-

cally purified Si and Ge will require usage of different gas precursors. This would lead to a change in the growth dynamics and consequently, the growth of the heterostructure stack would need to be readjusted, which would be a long-term research investment.

### Probing performance at different length scales

In terms of uniformity, we have demonstrated wafers with isotopically purified Si quantum wells, have shown statistical improvement in the spread of charge noise, and provided devices with large valley splitting, facilitating qubit readout. However, all devices shown cover areas on the nanometer length scale, which is not representative of the length scales of larger spin qubit arrays. For example, if we consider larger devices such as NISQ devices with 100-1000 spin qubits without interconnects and an average spacing of 100 nm, we would cover an area between 1 $\mu m^2$ - 10 $\mu m^2$. Similarly, a rudimentary spin qubit array of $10^6$ qubits without interconnects and an average spacing of 100 nm would cover an area between 100 µm × 100 µm. Furthermore, if we want to scale to even larger qubit counts (e.g $10^9$) and use interconnects as proposed in Ref. [181], we would cover areas of 1 $mm^2$ and beyond. Therefore, assessing the locally varying performance differences on the nanometer, intermediate (for devices that cover the length scale between 100 nm and 100 µm), and micron-scale will become more relevant when scaling to larger devices. To illustrate the relevant length scales, figure 10.2 shows a compilation of the imaginary large devices described above and a list of devices from state-of-the-art experiments in the spin qubit field, color-coded by the approximate length scales they probe. From Figure 10.2 it becomes clear that, even though the results in chapter 8 show promising uniformity and the devices in Refs [114, 231, 50, 115] indicate high material quality, the statistics gathered in this thesis run short to represent the locally varying material performance relevant for NISQ devices and larger spin qubit arrays.

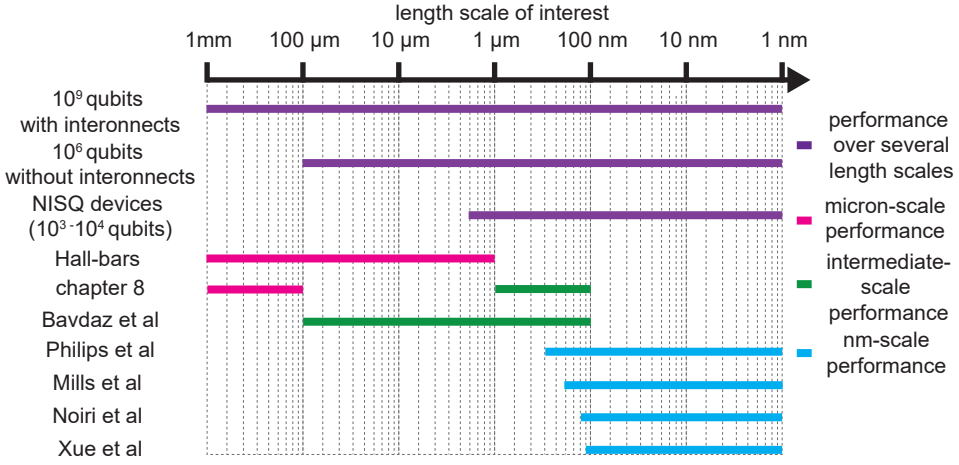



Figure 10.2: Color-coded illustration of devices probing performance at different length scales. Purple represents performance determined over several length scales (from hyperfine interaction at the nm level to micron- and millimeter-sized material variations), magenta over the micron-scale (usually probed by Hall-bar shaped HFET devices), cyan over the nm-scale (e.g. from qubit or quantum dot experiments), and green represents an intermediate length scale covering parts of the nanometer and parts of the micron length scale.

To assess performance on the micron scale we routinely use Hall-bar-shaped H-FETs throughout this thesis. However, these devices have limitations because, they average over large areas, in our case over 100 µm × 500-1000 µm and consequently lack the ability to reveal performance fluctuations on the intermediate and nanometer-scale. Even though we could reduce the size of the HFETs by two orders of magnitude to gather statistics on the intermediate scale, we would still lack the ability to assess variations on the nano-scale. Therefore, we need to find other ways to extend our probing capabilities. One option to extend statistics on the nano-scale is to expand the cryomultiplexing test bed we use for statistics on quantum dots to host an order of magnitude more quantum dots per cooldown and develop automatic test routines that facilitate and accelerate data acquisition. If we then take several quantum dots from different wafer location we could get insights on the nano-, intermediate-, and micron-scale. In addition, new cryo-multiplexers may be explored to allow for faster measurements or to enable statistical RF-measurements. Another way forward is to use sparse 2-dimensional quantum dot arrays as shown in Ref. [314]. In this publication statistics are gathered on the operation voltages of 648 single-electron transistors with varying gate sizes which are uniformly distributed over an area of 200 um x 100 um, which is representative of the intermediate length scale we are interested in probing for NISQ devices and the rudimentary $10^6$ qubit arrays described above. Exploiting such arrays to gather statistics on valley splitting, charge noise, and $t_2^\star$ should help to understand material limitations and consequently lead those key innovations that will drive progress in spin qubit research.

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# CURRICULUM VITÆ

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# LIST OF PUBLICATIONS

JOURNAL PAPERS AND PREPRINTS

9. **B. Paquelet Wuetz**, D. Degli Esposti, A. M. J. Zwerver, S. V. Amitonov, M. Botifoll, J. Arbiol, A. Sammak, L. M. K. Vandersypen, M. Russ, G. Scappucci, *Reducing charge noise in quantum dots by using thin silicon quantum wells*, preprint at https://arxiv.org/abs/2209.07242.

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7. S. G. J. Philips, M. T. Mądzik, S. V. Amitonov, S. L. de Snoo, M. Russ, N. Kalhor, C. Volk, W. I. L. Lawrie, D. Brousse, L. Tryputen, **B. Paquelet Wuetz**, A. Sammak, M. Veldhorst, G. Scappucci, L. M. K. Vandersypen, *Universal control of a six-qubit quantum processor in silicon*, Nature **609**, 919–924 (2022).

6. **B. Paquelet Wuetz***, M. P. Losert*, S. Koelling*, L. E. A. Stehouwer, A. M. J. Zwerver, S. G.J. Philips, M. T. Mądzik, X. Xue, G. Zheng, M. Lodari, S. V. Amitonov, N. Samkharadze, A. Sammak, L. M. K. Vandersypen, R. Rahman, S. N. Coppersmith, O. Moutanabbir, M. Friesen, G. Scappucci, *Atomic fluctuations lifting the energy degeneracy in Si/SiGe quantum dots*, preprint at https://arxiv.org/abs/2112.09606.

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4. **B. Paquelet Wuetz**, M. P Losert, A. Tosato, M. Lodari, P. L. Bavdaz, L. Stehouwer, P. Amin, J. S Clarke, S. N. Coppersmith, A. Sammak, M. Veldhorst, M. Friesen, G. Scappucci, *Effect of quantum Hall edge strips on valley splitting in silicon quantum wells*, Physical review letters **125** (18), 186801 (2020).

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CONFERENCE PROCEEDINGS

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