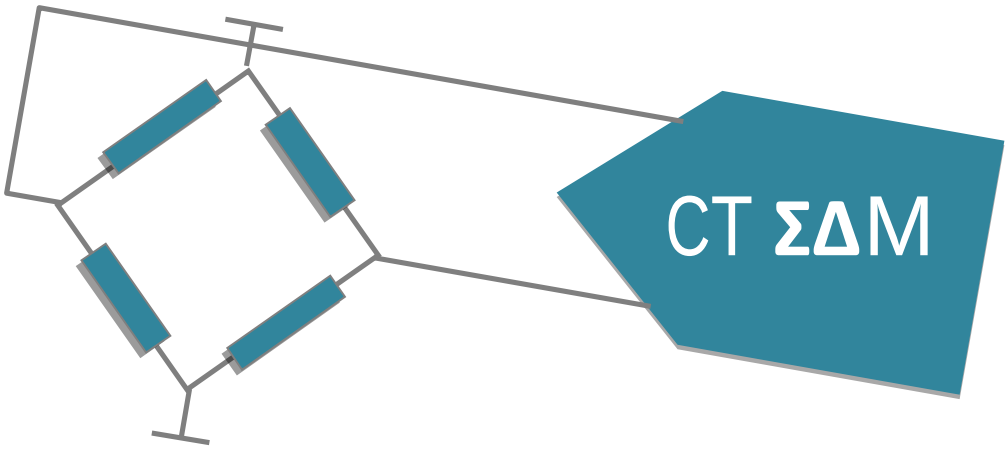
A Gm-C Continuous-Time Sigma-Delta Modulator with Improved Linearity



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To Babba, for being my hero. Peace.

And Mamma, for her love

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Abstract

Bridge sensors are widely used for accurate measurement of physical quantities such as temperature, pressure, strain or altitude. Such sensors require a low-noise, high-resolution and accurate readout system with high input impedance. In order to meet these requirements, conventional sensor readout systems use multiple stages which typically include a low-noise preamplifier, an anti-aliasing filter and a discrete-time (DT) sigma-delta modulator (ΣΔM). As a result, these systems involve several high-gain loops with total open-loop gain far exceeding the required closed-loop gain. This can lead to sub-optimal power dissipation and greater analog design complexity in design of a sensor readout system.

In recent years, Gm-C continuous-time (CT) ΣΔMs have attracted a lot of attention due to their inherent anti-alias filtering, low power dissipation, high input impedance and high resolution. However, their use in precision applications such as bridge sensor readout is limited by the nonlinearity of the input stage. In this work, a new single-bit CTΣΔM topology is proposed that employs an identical nonlinear element in the feedback path along with a low pass filter to enable nonlinearity compensation and achieve high linearity. A feedforward Gm stage further enhances the nonlinearity compensation by increasing the effective loop-gain. This approach enables more than 60 dB improvement in the nonlinearity of the input transconductor stage of the CTΣΔM.

A precision sensor readout circuit using the proposed CTΣΔM architecture is designed and implemented in 0.7 µm technology. The modulator achieves a resolution of 20 bits with a 22 nV/$\sqrt{Hz}$ noise floor and an accuracy better than 10 ppm in post-layout simulations. It consumes 240 µA current from a 5 V supply. The resolution and accuracy of the CTΣΔM designed in this work is comparable to that of state-of-the-art readout systems but with lower power dissipation and lesser analog complexity. The proposed modulators achieves 10x better linearity and accuracy compared to the state-of-the-art Gm-C based CTΣΔMs, albeit at low frequencies, with significantly less noise and power dissipation.

Thesis Committee:

Chair and Supervisor:	Dr. Kofi Makinwa
Committee Member:	Dr. Edoardo Charbon
Committee Member:	Dr. Chris Verhoeven

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1 Introduction

This chapter introduces bridge sensors, their applications and the challenges involved in design of sensor readout systems. An overview of bridge sensors is presented in Section 1.1. This is followed by a brief discussion of conventional readout systems to motivate the need for a single-stage readout system in Section 1.2. A Gm-C based continuous-time (CT) sigma-delta modulator (ΣΔM) can meet most of the requirements of sensor readout systems but suffers from the nonlinearity of its input stage. A few relevant techniques for improving the linearity of such modulators are discussed in Section 1.3 along with an overview of the proposed approach. The specifications for the precision readout system targeted in this work are explained in Section 1.4 and finally, the organization of this dissertation is presented in Section 1.5.

1.1 Bridge Sensors

Bridge sensors find widespread application in the accurate measurement of physical quantities such as temperature, pressure, strain or altitude. These sensors typically convert signals from thermal, magnetic or mechanical domains into the electrical domain which enables the use of electronic circuits for the processing of these signals. Precision sensors such as strain-gauge or temperature sensors often take the shape of a Wheatstone bridge. The impedance of one or more elements of the bridge is dependent on the quantity being measured. The bridge is said to be balanced when the impedance in both branches of the bridge are equal and the differential output voltage is zero. Any change in the quantity being measured leads to a variation in the impedance of bridge elements. This, in turn, creates an unbalance in the bridge and leads to a non-zero differential output voltage. For the full-bridge configuration shown in Figure 1.1, this differential output voltage can be expressed as:

$$Vout = \frac{\Delta}{R} Vexc \tag{1.1}$$

where, R is the nominal resistance of the bridge elements, Δ is the variation in the impedance of the bridge elements and $Vexc$ is the bridge excitation voltage.

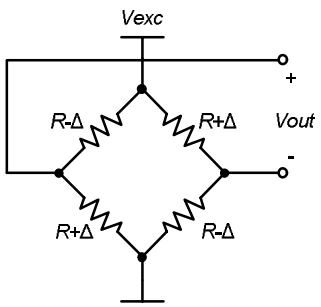


Figure 1.1 - A Wheatstone bridge sensor (full-bridge)

It can be seen from equation (1.1) that the sensitivity of a bridge sensor is dependent on the applied excitation voltage and the inherent properties of the bridge elements. Bridge sensors such as load cells or strain-gauges are very sensitive to changes in the physical quantity being measured, but their peak output signal is bound by physical elastic limits. Typically, the peak differential output signal from such sensors is limited to 2-5 mV/V. This implies that if an excitation voltage of 10 V is used, the peak differential output signal is in the range of 20-50 mV.

The analog output of the bridge needs to be converted into digital form to facilitate further processing. Applications such as a five digit weigh-scale, a μK resolution temperature sensor, or a precision altimeter require 20 bits of resolution over a full-scale range of about 50 mV. This places stringent noise and accuracy requirements on the readout system responsible for converting the analog output signal of the sensor to digital. In order to meet these requirements, conventional readout systems consist of multiple stages such as a preamplifier and an analog-to-digital converter (ADC). However, the use of multiple stages may lead to high analog complexity and inefficient power consumption. In contrast, a single-stage sensor readout system based on a low-noise ADC should lead to a simpler and more efficient solution. The motivation for building such a single-stage readout system and the challenges involved are described in more detail in the following section.

1.2 Motivation

The readout systems for precision sensors often require more than 20 bits of resolution with a peak signal of about 50 mV. This implies that the input referred noise of the readout system must be in the order of 10 nV/$\sqrt{Hz}$ for a typical 10Hz bandwidth. The high resolution requirement of such readout systems cannot be achieved by Nyquist rate ADCs. Therefore, an oversampled sigma delta modulator (ΣΔM) based ADC is needed for such applications. In order to meet the high accuracy requirement, conventional readout systems generally employ a switched-capacitor (SC) discrete-time (DT) ΣΔM for analog-to-digital conversion. As the accuracy of SC-ΣΔMs is dependent on capacitor matching, they can easily achieve accuracy in the order of a few parts-per-million (ppm). However, the input referred noise of such modulators is limited by the kT/C noise of the switched-capacitor input stage. As a result, large capacitor values are needed to meet the low noise requirements. Furthermore, the finite and dynamic input impedance of switched-capacitor input stages can cause source loading and lead to additional errors.

A typical readout chain for precision sensors consists of a preamplifier for conditioning the sensor output signal before feeding it to the ADC. A filter is also employed to reduce the errors due to the aliasing of interferers. In this way, the sensor's output signal is amplified and filtered before being fed to the ADC. The preamplifier provides a high impedance input stage for interfacing with bridge and its gain relaxes the noise specifications of the ADC. This allows the use of SC-based ΣΔM as the ADC. A general block-level diagram of a conventional sensor readout system is shown in Figure 1.2.

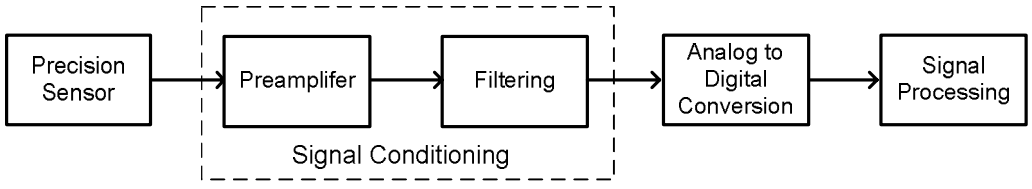


Figure 1.2 - A conventional precision sensor output readout chain

The design of such a readout system requires several high performance analog blocks for amplification, filtering and conversion. As a result, the readout chain consists of at least two high gain loops which increase its analog design complexity, power dissipation and cost. Consequently, there has been growing interest in simplifying the sensor readout chain by combining several functions in a single global feedback loop [1-4]. The ideal solution for a precision sensor readout system would be a single-step digitization scheme that incorporates both signal conditioning and analog-to-digital conversion in a single block as illustrated in Figure 1.3.

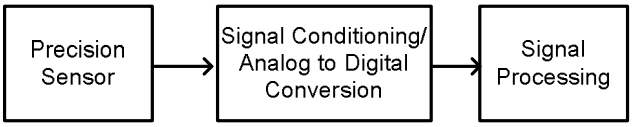


Figure 1.3 - Proposed sensor readout chain

A single-step digitization scheme may help reduce the analog complexity of the system, but places stringent requirements on the noise and input impedance of the ADC. A Gm-C based continuous time sigma-delta modulator (CTΣΔM) can fulfil the low noise and high resolution requirements of such a system. Moreover, the high-impedance transconductor input stage of such a modulator can interface with resistive sensors without loading them [3-5]. However, the nonlinearity of such modulator's input transconductor stage limits its accuracy and linearity. For instance, the nonlinearity of a simple MOS differential pair is in the order of 1% whereas precision readout systems require accuracy in the order of a few ppm. Therefore, the linearity of Gm-C CTΣΔMs must be significantly improved.

The existing circuit-level techniques for improving the accuracy and linear range of Gm-C based CTΣΔMs offer improvements in the order of 20-40 dB. However, this often comes at the cost of increased noise floor or higher power dissipation [6], [7].. The feedback-based nonlinearity compensation techniques have been shown to improve the linearity of Gm-C CTΣΔM significantly [3], [4]. But the existing topologies for nonlinearity compensation are still fairly complex, effectively shifting the problem instead of solving it.

In this work, a Gm-C based CTΣΔM architecture with improved linearity is proposed. The proposed Gm-C CTΣΔM employs global feedback to achieve high resolution and accuracy without increasing the circuit design complexity. The existing CTΣΔM topologies for improving the linearity of the system are briefly reviewed in the next section to demonstrate the need for the proposed topology.

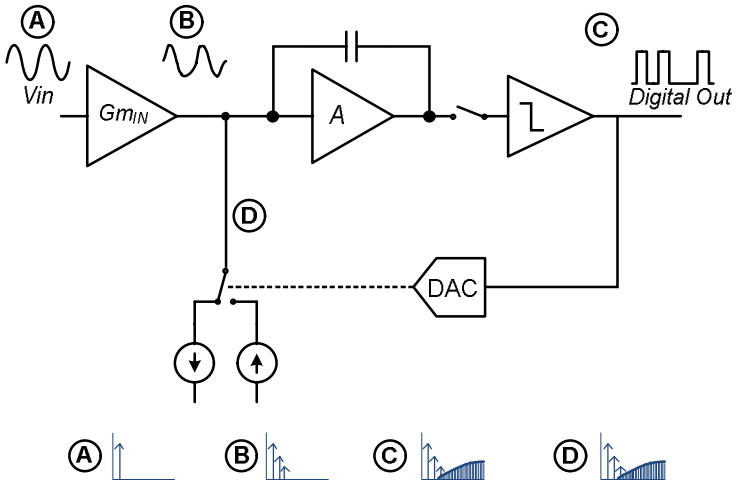


Figure 1.4 - A typical Gm-C integrator based CTΣΔM

1.3 Gm-C based Continuous-time Sigma-delta Modulator with Improved Linearity

In a typical Gm-C based CTΣΔM, the nonlinearity of the input transconductor stage directly appears at the output as illustrated in Figure 1.4. The nonlinear nature of the input stage makes CTΣΔMs unsuitable for high-precision applications. Many techniques have been proposed in past for improving the accuracy and the linear range of the input transconductor stage in a Gm-C CTΣΔM [6-9]. The commonly used techniques are based on: (a) local feedback, and (b) adaptive biasing. The linearity achievable by employing local feedback techniques such as resistive source degeneration is typically limited to 0.1% and comes at the cost of increased noise level [6]. On the other hand, techniques based on modulation of the bias current or the bias point, with input signal level, improve the input linear range, but are not suitable for sensor applications as there is little improvement in accuracy for small input signals [7], [9].

In contrast to the circuit-level techniques, the improvement in linearity offered by inserting an identical nonlinearity in the feedback path to compensate for the nonlinearity of input stage is quite significant and may be more suitable for high-precision applications [3], [4]. A CTΣΔM employing this technique with a multi-bit quantizer was proposed in [3]. In this topology, the output of multi-bit quantizer is a multi-level replica of the input signal as illustrated in Figure 1.5. Assuming that the nonlinearity of transconductor in the input path is identical to that in the feedback path, the nonlinear components in their output cancel each other. The nonlinearity of the input transconductor stage can thus, in principle, be completely compensated by the feedback transconductor. In practice, however, the improvement offered by this technique depends on the number of levels in the multi-bit quantizer and DAC being used. An accuracy of 0.02% has been demonstrated with this technique using a 5-bit quantizer and DAC [3]. Implementation of a linear DAC with 5 or more bits with linearity greater than 100 dB can be quite complicated. The performance of this approach is, therefore, limited by the complexity involved in the realizing a linear multi-bit DAC with more than 5 bits.

It may be noted that placing an identical nonlinear element in feedback offers no improvement in linearity if the quantizer and DAC are single-bit. This is because the nonlinearity of the feedback transconductor has no effect on a binary valued signal as the output would still be a two-level signal. Therefore, the signal being fed to the feedback must either be a multi-level or analog replica of the input signal.

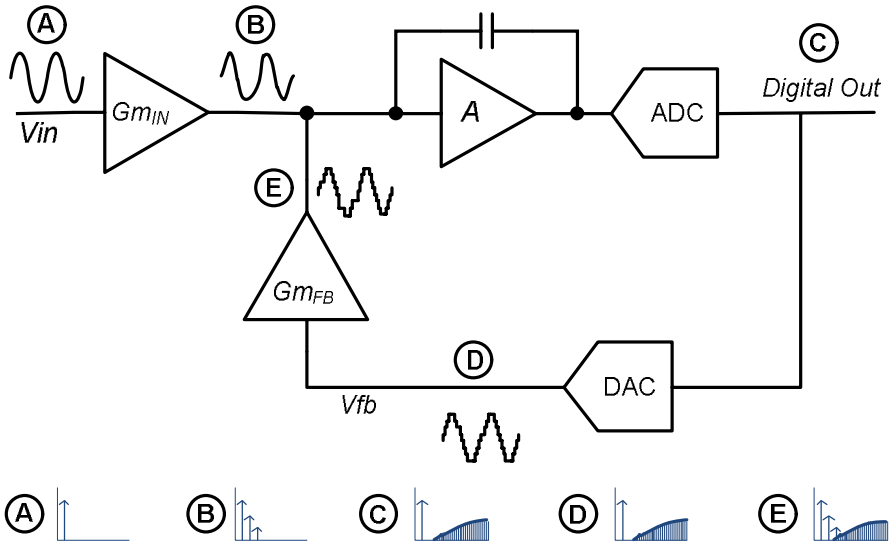


Figure 1.5 - CTΣΔM with a multi-bit ADC and DAC

In order to avoid the use of a multi-bit DAC, an alternative topology with feedback nonlinearity compensation using a single-bit quantizer along with a low pass filter (LPF) in was proposed in [4]. In this topology, the single-bit output of the ΣΔM is passed through the LPF to remove the high-frequency quantization noise. As a result, the output of the LPF mainly consists of a low-frequency analog replica of the input signal as illustrated in Figure 1.6. Thus, the nonlinearity compensation is enabled by the use of a single-bit quantizer in conjunction with a LPF. However, the LPF places an extra pole in the loop which affects its noise shaping and stability. In this approach, a high-pass path in the feedback loop compensates for the LPF's pole and restores the noise shaping of the ΣΔM. This technique has been shown to improve the distortion of the Gm-C CTΣΔM by about 35 dB [4].

There are several issues with this scheme. Firstly, in this topology, the transfer function between points A and C (Figure 1.6) is unity. As a result, the signal at the output of LPF (D) is a slightly delayed replica of the input signal due to the phase shift introduced by the LPF. This limits the linearity achieved by this approach for AC signals. Additionally, the high-pass path may require the first integrator to handle very high frequency signals. This can increase its power dissipation.

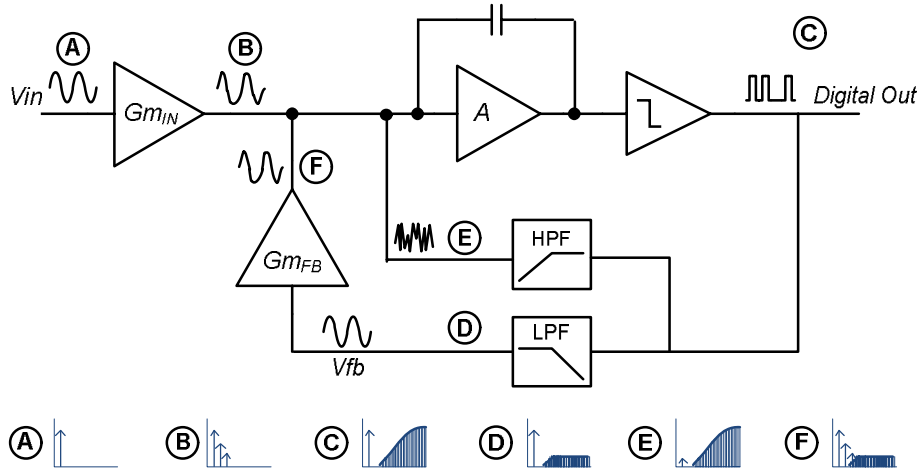


Figure 1.6 - CTΣΔM with an LPF in the feedback to convert the output bitstream to an analog signal

To summarize, the linearity achievable in existing CTΣΔM architectures employing feedback nonlinearity compensation scheme is limited either by the nonlinearity of the multi-bit DAC or the LPF's phase. In this work, a new CTΣΔM topology is proposed that uses a single-bit ΣΔM as a multi-bit ADC. A LPF in the feedback path filters the output bit-stream of this modulator to convert it into an analog replica of the input as illustrated in Figure 1.7. It may be noted that in this topology, the transfer function between points A and D (Figure 1.7) is unity. As a result, the signal at D is a perfect replica of the input signal without any additional delay. Therefore, in this approach, the LPF phase does not limit the nonlinearity compensation in this approach. Moreover, the gain of the input stage also contributes to the quantization noise shaping and therefore, the resolution required of the 1st order SDM shown in Figure 1.7 is not very high. Furthermore, the input stage only has to deal with low frequency signals, which reduces the power dissipation of the first stage.

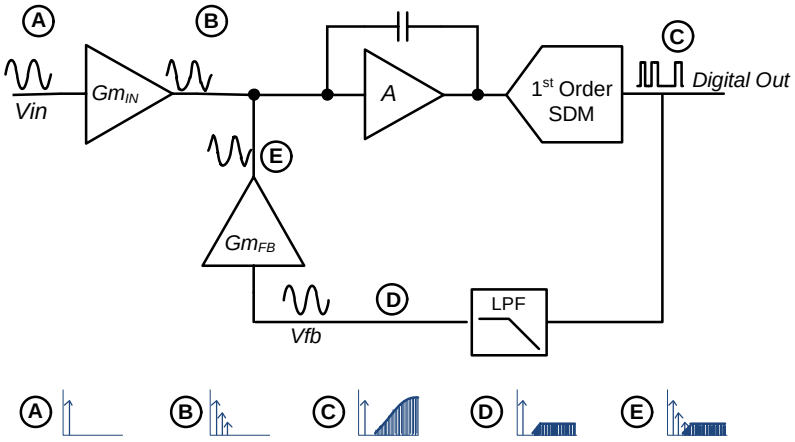


Figure 1.7 - The basic concept of the proposed CTΣΔM

There are several challenges in the design of such a CTΣΔM due to the nonlinear transconductor in the feedback path. One of the major issues is the mixing of unwanted quantization noise components with the input signal which can cause degradation in linearity and quantization noise floor. This may also introduce new challenges in the use of dynamic offset and 1/*f* cancellation techniques required for high precision. Additionally, the LPF in feedback path may cause stability issues and limit the performance of the modulator.

In this dissertation, this CTΣΔM topology is analysed in detail and several techniques are proposed to tackle the issues mentioned above and improve the performance of the system. These techniques are used to develop a generic architecture for a linear Gm-C CTΣΔM which can be employed in any application that requires an ADC with high resolution and high input impedance. Based on this generic architecture, a CTΣΔM design aimed at precision sensor readout system is implemented in 0.7 µm CMOS technology. The target specifications for this design are derived in the next section.

1.4 Requirements of a Precision Sensor Readout System

A bridge sensor readout system must detect a small differential signal carried on a large common mode voltage. As discussed earlier, precision sensor readout applications often require up to 20-bits of resolution with peak signal level as small as a few tens of millivolts. In this section, the requirements for a precision sensor readout system are discussed to derive the target specifications for this design.

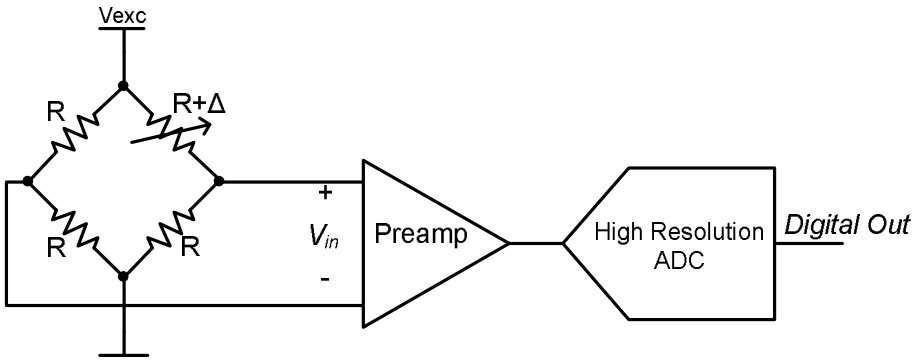


Figure 1.8 - A bridge sensor with a conventional readout system

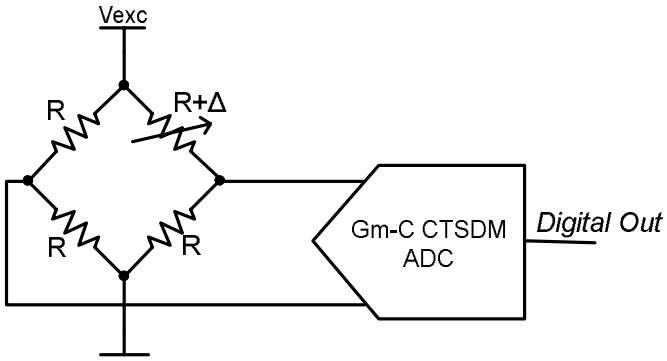


Figure 1.9 - Proposed Gm-C CTΣΔM based sensor readout system

1.4.1 Input Signal Range, Bandwidth and Resolution

In typical bridge sensor applications, the differential output of the bridge is a DC or low frequency signal with amplitude in the range of a few millivolts. In order to achieve high resolution, the thermal noise level at the sensor output can be reduced by averaging over time. However, this leads to a longer measurement time which may not be desirable in many applications. Therefore, the choice of noise bandwidth is a trade-off between resolution and measurement time. In general, a resolution of 20 bits at 5-10 Hz bandwidth for a peak input signal range of ±50mV is sufficient for a wide range of sensor applications [10].

1.4.2 Input Referred Noise

The input referred noise density of the ADC is determined by the resolution requirement. To achieve 20 bit resolution with a peak differential signal of 50 mV, the integrated input referred noise is required to be less than 50 nV. This corresponds to an input referred white noise density of 22.5 nV in a 5 Hz bandwidth assuming that the *1/f* noise power is negligible compared to the thermal noise.

1.4.3 1/*f* Noise Corner Frequency

Static low frequency errors can be removed from the system by calibration. However, dynamic cancellation techniques must be employed to remove the 1/*f* noise. By using chopping, state-of-the-art CMOS instrumentation amplifiers achieve 1/*f* noise frequency in the order of a few mHz [11]. A 1/*f* noise corner in the order of a few tens of mHz is targeted for this work.

1.4.4 Offset Error and Offset Drift

Offset error in a measurement system is caused by a mismatch between circuit elements. In modern technology, offset error can be in the order of tens of millivolts leading to a significant reduction in the dynamic range of the measurement system. Although the offset error can be factory trimmed, it may drift with time, temperature or other conditions leading to a low frequency error signal that cannot be distinguished from the signal of interest. Therefore, it is desirable to use a dynamic offset correction technique that constantly removes the offset over time; thereby minimizing the errors caused by offset and offset drift. An offset error of less than 1 µV is targeted in this work, which is comparable to state-of-the-art readout systems [12].

1.4.5 Linearity

As discussed earlier, the nonlinearity of the input stage limits the use of a Gm-C CTΣΔM in applications that require high accuracy. The CTΣΔM architecture proposed in this work can improve the overall linearity of the system significantly. In order to demonstrate the applicability of a CTΣΔM in precision readout systems, an INL of less than10 ppm is targeted which is comparable to state-of-the-art sensor readout systems [12-14].

1.4.6 Common Mode Rejection Ratio (CMRR)

A bridge transducer has a small differential voltage signal carried on a large common mode level. Therefore, it is important to have a strong rejection of common-mode variations. State-of-the-art readout systems based on current feedback instrumentation amplifiers (CFIA) achieve CMRR greater than 120 dB [11]. Since the CTΣΔM based readout system operates in current-mode, there is very little dependence of the output on input common-mode voltage level. Therefore, a CMRR value greater than 120 dB is targeted in this work.

1.4.7 Reference (Excitation) Source Rejection

The sensitivity of a bridge transducer is measured in terms of *mV* of signal per volt of excitation voltage source i.e. *mV/V*. Any variation in the excitation voltage source directly translates into a proportional change in the differential output signal of the bridge. This can cause large errors in the measurement and must be avoided to achieve high precision. Ratiometric measurement principle can be employed to reduce the effect of reference variations.

1.4.8 Power Consumption

Low power consumption is desirable in sensor readout systems mainly for two reasons: (a) use in battery operated applications and (b) to avoid self-heating of sensors that can cause cross-sensitivity issues. Therefore, the sensor readout system must consume very low power. The aim of this work is to demonstrate that the proposed architecture offers a simpler solution for sensor readout systems than the state-of-the-art [12] with lower power dissipation. Therefore, power consumption of less than 250 µA is targeted in this work.

1.4.9 Summary of Target Specifications

Table 1.1 - Target Specifications for CTΣΔM based readout system

Parameter	Target Specification
Resolution	20 bits
Bandwidth	5-10 Hz
Noise Density	22.5 nV/$\sqrt{Hz}$)
Offset	< 10 µV
Linearity	< 10 ppm
Power	<250 µA
CMRR	120 dB

1.5 Organization of the Thesis

This dissertation describes the design and implementation of a linear Gm-C CTΣΔM for bridge sensor readout applications.

The bridge sensor readout systems have been in existence for several decades. The theory and background of existing systems with a focus on conventional techniques is discussed in Chapter 2. The two most important building blocks of the conventional readout systems - preamplifier and high resolution ADC - are discussed in depth. The dynamic techniques used in high precision analog systems are also reviewed in this chapter.

Many circuit-level and system-level techniques have been proposed in the past to deal with the nonlinearity of the input stage. These techniques are reviewed in Chapter 3 with emphasis on feedback nonlinearity compensation technique. Further, the issues caused by the use of a nonlinear element and an LPF in the feedback path of a ΣΔM are discussed. This analysis is used to propose a generic architecture for high-precision Gm-C CTΣΔM.

The generic architecture proposed in Chapter 3 is used to develop the system-level design of a CTΣΔM for precision sensor readout systems in Chapter 4. This chapter also introduces the concept of the feedforward path which is crucial for improvement in the linearity of the proposed system. Furthermore, the trade-offs involved in applying dynamic techniques such as chopping and dynamic element matching are discussed in this chapter.

The circuit level implementation and layout of the proposed CTΣΔM in 0.7µm CMOS technology are presented in Chapter 5 along with the post-layout simulation results. The simulation results are used to analyse the design and compare it with the state-of-the art readout systems.

Finally, the thesis is concluded in Chapter 6 along with a summary of work to be done in future to improve this CTΣΔM design or extend it to other applications.

2 Theory and Background

Instrumentation applications typically require high resolution and accurate readout systems to precisely convert the low frequency analog output of a sensor to a digital value. This chapter covers the background of existing sensor readout systems.

A general survey of developments in precision sensor readout systems is presented in Section 2.1. Conventional readout systems consist of a low-noise instrumentation amplifier (IA) followed by an analog-to-digital converter (ADC). Several IA topologies are found in literature and some of the most commonly used topologies are reviewed in Section 2.2. The ADC that follows the IA must have sufficient resolution (up to 20 bits). Since, the resolution of most Nyquist rate data converters is limited by component mismatch; oversampling ΣΔ ADCs are generally used to achieve the required resolution without large penalty in power and area or the need for expensive trimming. The general theory of ΣΔMs with emphasis on the continuous-time sigma-delta modulators (CTΣΔM) is discussed in Section 2.3.

As discussed in Chapter 1, a sensor read-out system must have low offset, low 1/*f* noise, high linearity and high gain accuracy. The sources of these errors and dynamic techniques to mitigate these errors are reviewed in Section 2.4.

2.1 Precision Sensor Readout Systems

The output of precision sensors such as strain-gauge, thermistors or pressure sensors is analog in nature. This analog output needs to be converted into a digital signal for post-processing, recording or digitally displaying. This conversion from analog to digital is performed by a sensor readout system. The output of bridge based precision sensors is a small differential signal with peak amplitude of 20-50 mV carried on a large common-mode level. The sensor readout circuit must convert this signal to a digital code with very high resolution ($\geq$ 20 bits). Additionally, in order to avoid gain errors caused by loading of resistive sensors, the readout circuit must not draw any current from the sensor. In other words, the input impedance of the circuit must be very high.

In this section, the developments in the field of bridge sensor readout systems over the last two decades are presented.

2.1.1 Bridge-to-Frequency Converter

The earliest class of bridge readout systems were based on converting the bridge impedance to a corresponding frequency [15], [16]. Such systems embedded the resistive bridge in a relaxation oscillator with an integrator and a comparator as shown in Figure 2.1. The frequency of oscillation is determined by the bridge sensor impedance and a fixed-valued capacitor. In this way, the sensitivity of bridge sensor is converted from mV/V to Hz/V. This technique of

converting a DC signal into a corresponding AC frequency was important in the 80's and early 90's for transmitting sensor signals over long cables. However, a bridge-to-frequency system still requires the conversion of the frequency output to a digital value if further digital processing is needed. The advent of digital buses allowed reliable data transmission over long cables and led to an increased interest in digital conversion of sensor signals rather than bridge-to-frequency conversion for transmission.

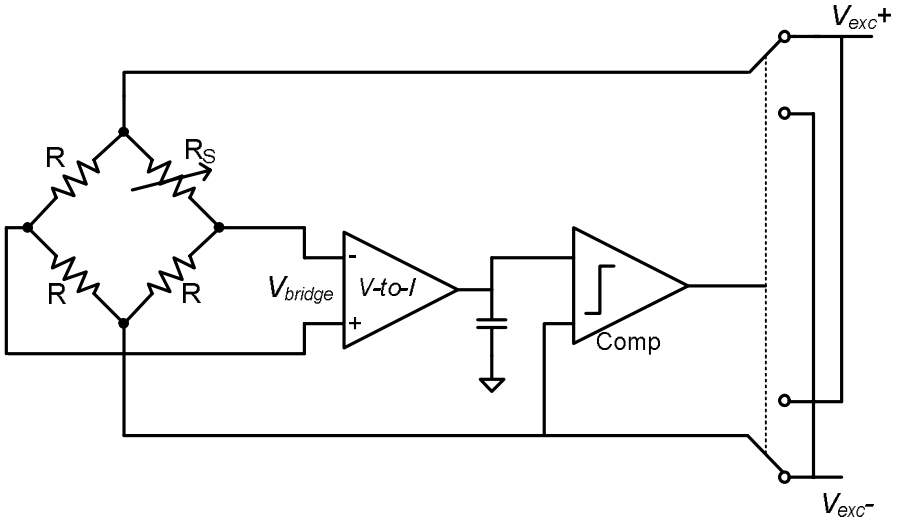


Figure 2.1 - Conceptual block diagram of a bridge-to-frequency converter [15]

2.1.2 Early Continuous-Time Sigma-Delta Modulator based Readout Systems

A system that directly digitizes sensor signals for transmission over a digital bus offers significant advantages over the bridge-to-frequency based systems. In the early 90's, several architectures for bridge sensor readouts based on continuous-time sigma-delta modulators (CTΣΔM) were proposed [17-19]. In the topology shown in Figure 2.2, the input is filtered over an RC filter and fed to a sigma-delta modulator. The first order modulator consists of a loop-filter and a multi-bit quantizer. The multi-bit feedback DAC is implemented as a pulse-width modulated (PWM) signal. The output of the loop filter is compared with the output of a ramp generator and sampled at a very high frequency. Consequently, the output of the quantizer is high for a long time if the quantizer input is large and vice-versa. This behaves like a multibit PWM-DAC working at the frequency of the ramp generator. A resolution of 20 bits has been reported with this CTΣΔM architecture [17]. However, this topology is inherently single-ended in nature as the integrator cannot be used in differential mode in order to maintain the high input-impedance. A differential version of this system requires the use of a second converter such that the two integrators track a pseudo ground over a resistor divider, in a way similar to the two-opamp instrumentation amplifier topology. This leads to higher power dissipation in the converter. Additionally, the CMRR of such a differential topology will still be limited by matching of resistors.

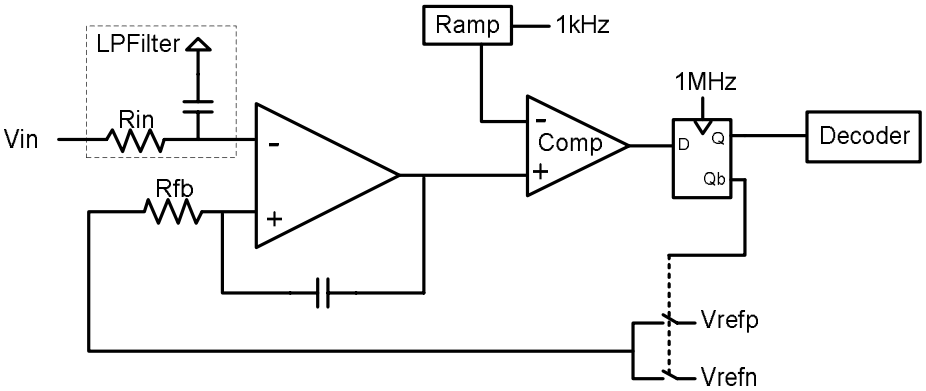


Figure 2.2 - Single-ended CTΣΔM based readout system [18]

A fully differential CTΣΔM based readout circuit was proposed in [5]. This uses transconductance amplifiers for voltage to current conversion at the input and the feedback path as shown in Figure 2.3. Furthermore, the bridge excitation voltage is used as the ΣΔM reference voltage to enable ratiometric measurement. The linearity of such a modulator is dependent on the linearity of the input and feedback V-to-I stages. Therefore, the V-to-I stages must be low-noise as well as highly linear. This results in high power consumption and limited accuracy of the modulator. The resolution reported with this architecture is limited to 13-14 bits [5]. It is possible to achieve higher resolution and accuracy if the linearity of V-to-I stage is improved at the cost of area and power.

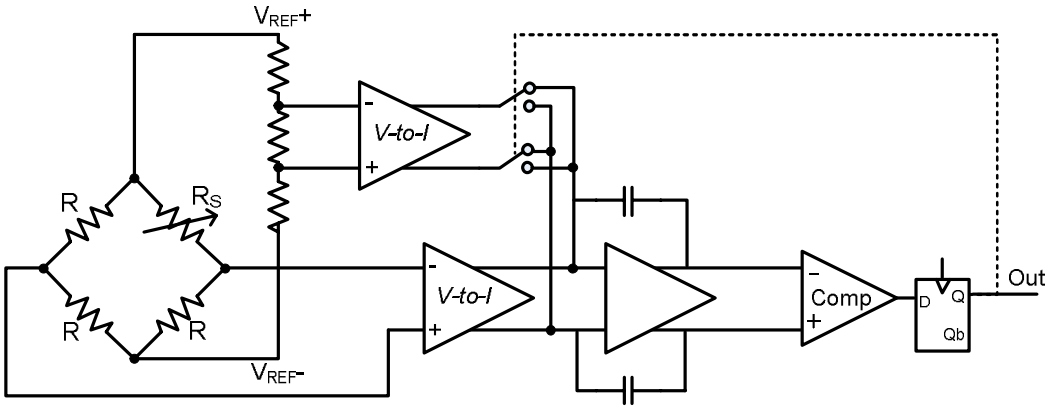


Figure 2.3 - CTΣΔM based readout system [5]

2.1.3 Discrete-Time Sigma Delta Modulator with Preamplifier

The use of a DTΣΔM offers many advantages for low bandwidth and high resolution applications such as bridge sensor readout. DTΣΔMs are capable of achieving very high accuracy as their gain depends on capacitor matching. However, there are several issues in interfacing DTΣΔM directly with a precision sensor:

(a) The input referred thermal noise of DTΣΔM with a switched-capacitor (SC) input stage is limited by the size of the sampling capacitor (*kT/C* noise). To achieve a noise floor of 20 nV with an oversampling ratio of 1000, the capacitor size needs to be in the order of 5-10 nF. Such a capacitor size is too large for on-chip implementation and affects the settling time requirements of sample-and-hold stage.

(b) The input impedance of the SC input stage of the DTΣΔM is proportional to $1/f_S C$, where f_S is the sampling frequency and C is the sampling capacitor. This implies that for high

input impedance, the sampling capacitor size needs to be small. Therefore, high input impedance and low thermal noise requirements pose contrasting requirements for the sampling capacitor size. Furthermore, the input impedance of SC integrators is dynamic in nature as the current drawn from the source is not constant over time. This may leads to dynamic source loading errors in the system.

(c) The sampling at the input node causes aliasing of interferers around the multiples of sampling frequency down to baseband creating an extra source of error. Therefore, the input signal needs to be filtered before it is sampled by the DTΣΔM.

The thermal noise, input impedance and aliasing issues make DTΣΔM unsuitable for interfacing with a precision sensor. Conventional sensor readout systems circumvent these issues by employing a low-noise pre-amplifier and signal conditioning circuit placed in front of the DTΣΔM [10]. Such a readout system is shown in Figure 2.4 along with a DAC that is often used for calibration. The differential output of the bridge may have an offset due to mismatch of bridge resistors. This offset can be large enough to saturate the preamplifier output or significantly limit the dynamic range. Therefore, the DAC is used to calibrate for the bridge offset. This is followed by the signal-conditioning circuit that usually consists of a low-noise programmable gain amplifier (PGA) and an anti-aliasing filter. The noise level of the preamplifier sets the lower limit on resolution of the readout system. The amplified signal is then fed to the DTΣΔM for digitization.

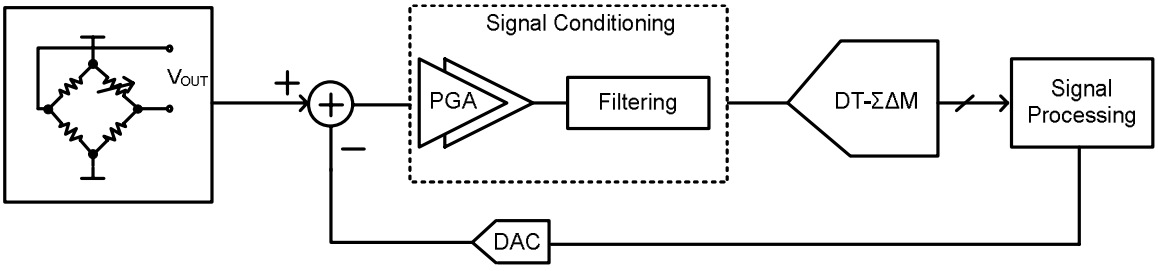


Figure 2.4 - A conventional precision sensor readout system [10]

The main disadvantage of the conventional systems is the need for two complex subsystems, a low-noise instrumentation amplifier and a high-resolution ADC, both of which require high gain amplifiers. Multiple high gain loops in the system lead to more design complexity and higher power dissipation. Furthermore, an off-chip anti-alias filter is often required to avoid errors at the input sampling stage of the DTΣΔM [13], [20]. However, even with these disadvantages, this architecture is robust and very high resolution and accuracy can be achieved. Most commercial precision sensor readout systems today are based on this architecture [12-14], [20]. To gain a better appreciation of the state-of-the-art designs using this architecture, some of the commonly used preamplifier topologies are described in the next section.

2.2 Preamplifier Topologies for Precision Sensor Readout Systems

Most conventional bridge sensor readout systems employ a low-noise instrumentation amplifier (IA) as the front-end for interfacing with the sensor. The preamplifier must exhibit low noise, low offset, high linearity, high accuracy and high CMRR. Additionally, to avoid source loading errors, the input impedance of the preamplifier must be high. The most commonly used IA topologies in literature are discussed here.

2.2.1 Two-Opamp and Three-Opamp Instrumentation Amplifiers

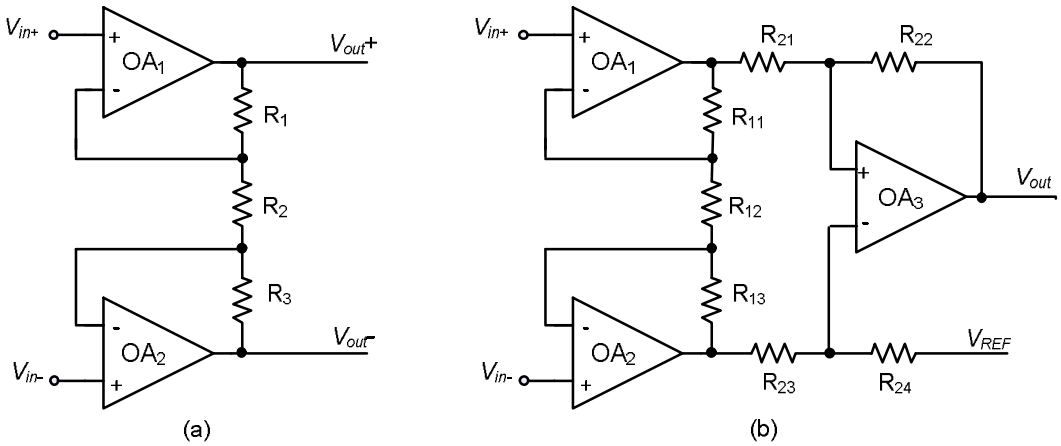


Figure 2.5 - (a) Two-opamp instrumentation amplifier (b) three-opamp instrumentation amplifier

The two-opamp IA, as shown in Figure 2.5a, is the basic instrumentation amplifier topology and is very popular in commercially available precision sensor readout systems [13], [14], [20]. The gain of this IA is set by the ratio of resistors (1+R1/R2) and therefore, high gain accuracy can be achieved by use of well-matched on-chip (or off-chip) resistors. However, the use of two low-noise high-gain operational amplifiers leads to high power dissipation in this topology. Additionally, each of the opamps must have a class AB output stage to drive the resistor divider. Furthermore, the CMRR of this architecture is limited by resistor matching (R1=R3, R2=R4). For a resistor mismatch of 0.01%, the CMRR is limited to 75dB.

The CMRR of the two-opamp topology can be improved by using the three-opamp topology, shown in Figure 2.5b. In a three-opamp instrumentation amplifier, the CMRR is improved by the gain of the first stage and therefore, does not rely solely on resistor matching. However, the higher CMRR of the three-opamp topology comes at the cost of additional power dissipation in the third amplifier. Additionally, the CMRRs of OA_1 and OA_2 need to be well matched for achieving high overall CMRR [21].

A big drawback of both of the above topologies is that moving the input common-mode (CM) level close to ground leads to saturation of the output. This prohibits the application of these IA topologies in systems that require ground-sensing or the ability to work at CM levels close to ground [22].

2.2.2 Current Feedback Instrumentation Amplifier

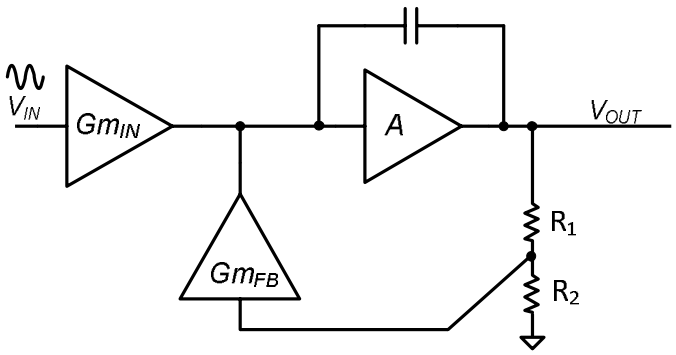


Figure 2.6 - A current feedback instrumentation amplifier

The current feedback instrumentation amplifier (CFIA) topology, as the name suggests, operates in current mode. The input and output voltages are converted into proportional currents by the input and the feedback transconductor stages and the difference current is integrated. Unlike the two-opamp or three-opamp topologies, the CM level at the input and output of this amplifier can be set independently. This enables the CFIA to potentially work at any CM level between the rails. Further, the current mode operation ensures that very high CMRR can be achieved without any need for trimming of resistors. Although the individual transconductor stages (Gm_{IN} and Gm_{FB}) used in the CFIA can be nonlinear, the overall system is linear due to the presence of the same nonlinearity in the input and feedback *Gm* stages. The gain in this amplifier is set by the ratio of resistors and *Gm* stages and is expressed as:

$$Gain = \frac{Gm_{IN}}{Gm_{FB}}\left(1+\frac{R_1}{R_2}\right) \tag{1.2}$$

As the matching of on-chip transconductors cannot be as good as resistors, this topology suffers from low gain accuracy and residual nonlinearity. However, the gain accuracy can be improved to match that of the two-opamp topology by use of the dynamic element matching technique [12]. The main disadvantage of a CFIA is the modulation of input stage transconductance with input common-mode voltage which leads to residual gain error [23].

Note that a fully differential Gm-C CTΣΔM, with V-to-I stages in both the input and the feedback paths, bears a great resemblance to the CFIA. The linearity of a Gm-C CTΣΔM is limited by the nonlinearity of the input transconductor. A single-bit Gm-C CTΣΔM does not allow compensation of this nonlinearity which limits the resolution and accuracy of CTΣΔM based readout system proposed in [5]. In a CFIA, on the other hand, the feedback signal is an analog replica of the input signal and therefore, the nonlinearity of the input *Gm* stage is compensated by the feedback *Gm* stage. This principle of feedback nonlinearity compensation has also been applied to CTΣΔMs in the past for high accuracy [3], [4] as discussed earlier in Chapter 1. These CTΣΔM topologies are discussed in more detail in Chapter 3.

2.3 Theory of Sigma Delta Modulators

Unlike Nyquist-rate ADCs, the resolution of oversampled data convertors is not limited by component mismatch as high resolution can be achieved by trading speed for resolution. The noise shaping sigma-delta modulator (ΣΔM) based ADCs can easily achieve more than 20-bits of resolution. Traditionally, only integrating or counting based data converters like dual-slope ADCs could meet the high resolution requirements, but they are not well suited for sensor readout applications due to their rather long conversion time.

In this section, the basic theory of oversampling and sigma delta modulation is discussed. The detailed analytical analysis of ΣΔMs is out of the scope of this dissertation and appropriate references are provided wherever necessary.

2.3.1 Basic Concepts

2.3.1.1 Sampling and Quantization

In any analog-to-digital conversion system, there are two types of quantization processes involved- time quantization (sampling) and amplitude quantization. Typically, a continuous-time analog signal is first converted to discrete samples by periodic sampling and then the analog value of each sample is converted into a corresponding digital code. In reality, sampling and quantization processes are not error-free due to imperfect sampling moments caused by clock jitter and amplitude quantization caused by physical component match. Generally, the performance of low-bandwidth systems is limited by amplitude quantization error, while clock jitter creates an upper bound on the resolution of high-bandwidth converters [24].

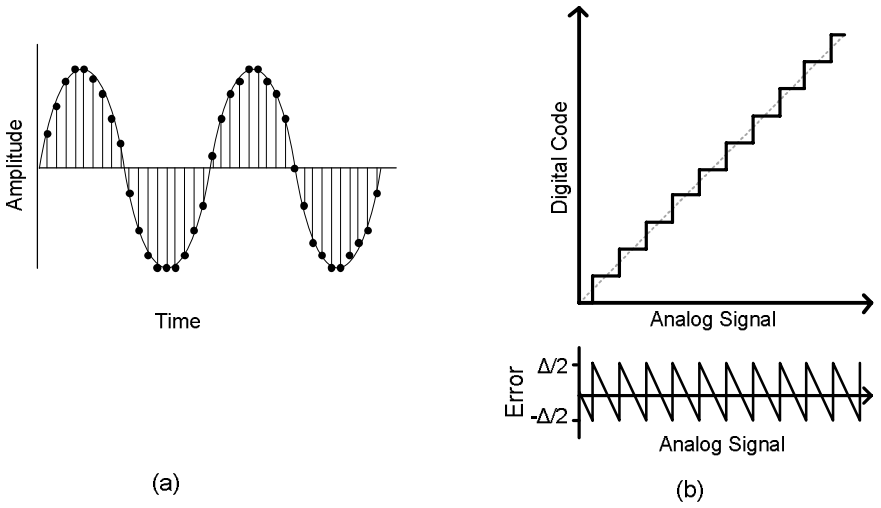


Figure 2.7 - Sampling of continuous-time signal (b) Quantization of analog signal to digital

2.3.1.2 Quantization Noise

Quantization error is the error made in conversion of an analog quantity to its corresponding digital code. For a busy (i.e. constantly changing) signal, the quantization error can be assumed to be a random error with uniform distribution and peak-to-peak amplitude equal to half of the LSB. The total energy of quantization error can be shown to be [25]:

$$Qerr_{rms}^2 = \frac{\Delta^2}{12} \tag{1.3}$$

where Δ is the LSB size.

This energy is spread over the frequency band up to half of the sampling frequency. For high number of quantization levels, the quantization error can be assumed to be white as shown in Figure 2.8. As the total energy of quantization noise is independent of the sampling frequency, the power spectral density of quantization noise floor is inversely proportional to the sampling frequency.

2.3.1.3 Oversampling

If the input signal is sampled and quantized at a frequency much higher than the Nyquist rate, quantization noise is spread over a wider band. Consequently, with higher sampling frequency, the power spectral density of quantization noise is smaller as illustrated in Figure 2.8. The high frequency components of quantization noise can be filtered out in order to achieve higher resolution. This is the fundamental principle behind oversampled data convertors.

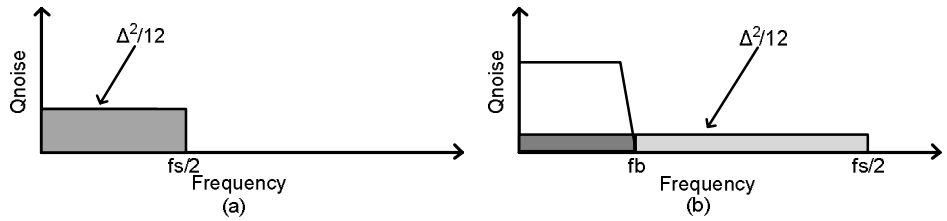


Figure 2.8 - (a) Oversampled signal in time-domain; (b) quantization noise PSD is lower with oversampling

The spectral density of quantization error is dependent on the sampling rate and can be expressed as:

$$Q_{PSD}^2 = \frac{\Delta^2}{12}\frac{2}{f_S} \tag{1.4}$$

where f_S is the sampling frequency and Δ is the LSB size.

Assuming that the quantization error outside the signal band is filtered, the signal to in-band quantization noise ratio (SQNR) can then be written as:

$$SQNR = \sqrt{3\frac{A^2}{\Delta^2}\left(\frac{f_S}{f_B}\right)} \tag{1.5}$$

where, A is the amplitude of signal, f_S is the sampling frequency and f_B is the signal bandwidth.

The equation (1.5) implies that a 3dB improvement in SQNR can be achieved by doubling the sampling frequency. The ratio of actual sampling frequency and the minimum sampling frequency mandated by Nyquist sampling theorem is called oversampling ratio (OSR) and is expressed as:

$$OSR = \frac{f_S}{2 f_B} \tag{1.6}$$

It must be stated that the assumption of the quantization noise being random and white is not always valid. However, for a busy input signal and a large number of quantization levels (greater than 5-6 bits), this assumption is generally valid, provided that there is no correlation between the input signal frequency and the sampling frequency [25] .

2.3.2 Noise Shaping

An ΣΔM uses the principle of noise-shaping to reduce the quantization noise in the signal band by shaping it to higher frequencies. The shaped high frequency quantization noise can be filtered out to achieve high SQNR. In this way, it is possible to achieve high resolution even with a single-bit quantizer in the loop.

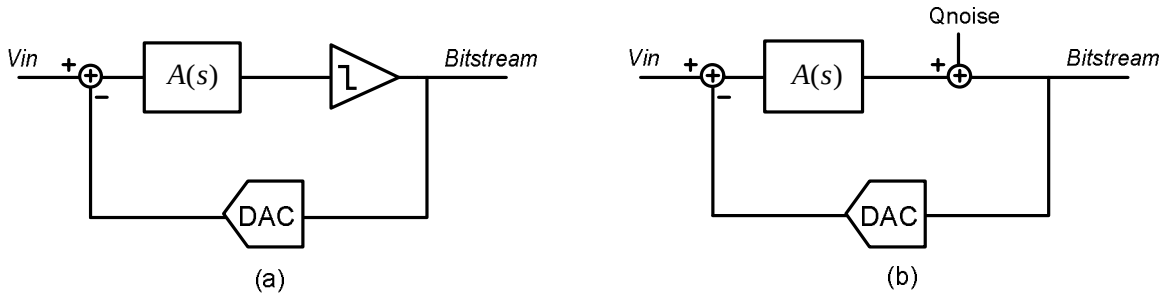


Figure 2.9 - (a) An ΣΔM with single-bit quantizer; (b) linear model of ΣΔM

Figure 2.9a shows an ΣΔM with a loop filter, *A(s)*, and a single-bit quantizer. The ΣΔM loop is nonlinear in nature due to the behaviour of the single-bit quantizer. However, a linear model of the modulator can be constructed under the assumption that the quantizer error can be modelled as additive white noise. A linear model of a first-order ΣΔM is shown in Figure 2.9b [25]. Although this model is not strictly valid as the nonlinear dynamic nature of the single-bit ΣΔM is ignored, it is useful for a first-order analysis of the behaviour of an ΣΔM. The transfer function of signal and quantization noise for this linear model is expressed as:

$$Y(s) = \frac{A(s)}{1 + A(s)} Vin + \frac{1}{1 + A(s)} Qnoise \tag{1.7}$$

It can be seen that while the signal is transferred with a gain of nearly unity, the quantization noise is suppressed by gain of the loop filter. In this way, high SQNR can be achieved by filtering the quantization noise outside the signal band. Moreover, increasing the sampling frequency of the ΣΔM leads to significant improvement in the in-band quantization noise as illustrated in Figure 2.10.

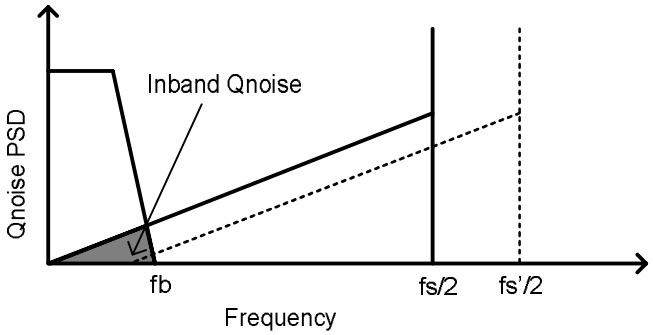


Figure 2.10 - Quantization noise energy in the signal band is reduced by noise shaping

2.3.3 First Order Sigma-Delta Modulator

A first order single-bit ΣΔM consists of an integrator as the loop filter and a single bit quantizer as shown in Figure 2.11. Assuming the linear model of quantizer, the quantization noise transfer function (NTF) and signal transfer function (STF) of the first order ΣΔM can be written as:

$$NTF = 1 + s \tag{1.8}$$

$$STF = \frac{1}{1+s} \tag{1.9}$$

Assuming an ideal integrator, the NTF expression shows that quantization noise of the ΣΔM is zero at DC and increases with a slope of 20 dB/decade. This implies that doubling the OSR leads to a 9 dB improvement in the SQNR as the quantization noise in the signal band goes down by 6dB due to first order noise shaping. This also suggests that use of a higher-order loop filter can suppress the low frequency quantization noise more efficiently. However, the additional pole in the loop can cause stability issues. The architecture of a second-order ΣΔM is discussed in the next section.

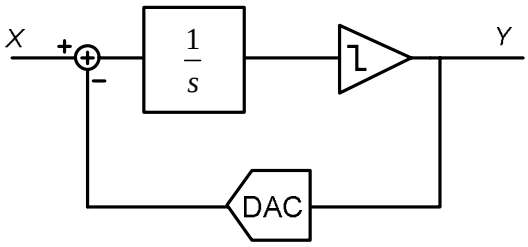


Figure 2.11 - A First order ΣΔM

2.3.4 Second Order Sigma-Delta Modulator

Increasing the number of poles in the loop-filter (or number of zeroes in the NTF) can help reduce the in-band quantization noise. Therefore, the quantization noise shaping can be further improved by use of two or more integrators in the loop-filter as shown in Figure 2.12. However, the two poles at DC in this loop make the loop unstable and a zero must be added in order to stabilize the loop. The zero can be introduced in the ΣΔM loop by employing either a feedforward path or a feedback path. Both of these approaches have certain advantages and disadvantages as discussed in the following sub-sections.

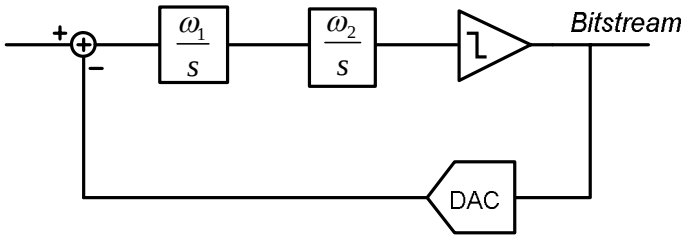


Figure 2.12 - Second order loop filter with two poles and no zeroes is unstable

2.3.4.1 Feedforward based Second Order Sigma-Delta Modulator

In a second order ΣΔM employing the feedforward topology, a zero is added by providing a path that bypasses the second integrator at high frequencies. Hence, quantization noise is suppressed by both the first and the second integrators at low frequencies, but only the first integrator at high frequencies.

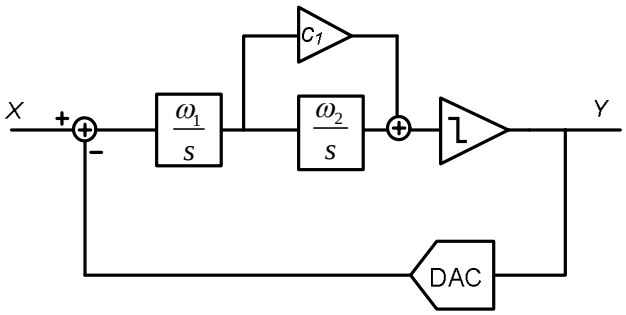


Figure 2.13 - Feedforward second-order ΣΔM

The characteristic equation for this loop can be written as:

$$Char\ eqn = 1 + \kappa \frac{\omega_1}{s}\left(c_1 + \frac{\omega_2}{s}\right) \tag{1.10}$$

The zero added by the feedforward path is at the frequency ω_2/c_1. The location of the zero can be chosen based on the desired noise shaping. Moving the zero to a lower frequency (increasing c_1) leads to a more first-order like behaviour of the system, and the system is more stable. On the other hand, moving the zero to a higher frequency (reducing c_1) leads to better noise shaping. However, if the zero is placed at very higher frequency (c_1 close to 0), it leads to instability in the modulator. The NTF and STF of this loop with linear model approximation can be expressed as:

$$NTF = \frac{s^2}{s^2 + s \cdot \omega_1 c_1 + \omega_1 \omega_2} \tag{1.11}$$

$$STF = \frac{\omega_1 (s \cdot c_1 + \omega_2)}{s^2 + s \cdot \omega_1 c_1 + \omega_1 \omega_2} \tag{1.12}$$

2.3.4.2 Feedback based Second Order Sigma-Delta Modulator

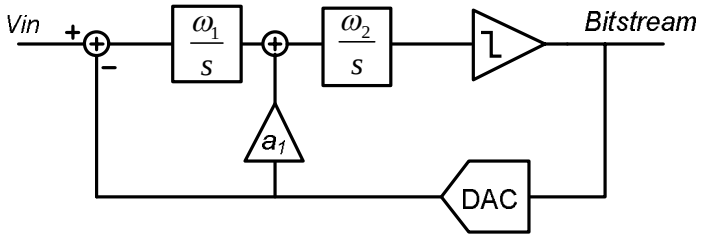


Figure 2.14 - Feedback second-order ΣΔM

In a feedback based second order ΣΔM, the high frequency components bypass the first integrator through the feedback path. The characteristic equation of this loop can be expressed as:

$$Char\ eqn = 1 + \kappa\left(a_1 + \frac{\omega_1}{s}\right)\frac{\omega_2}{s} \tag{1.13}$$

The zero in the characteristic equation is added at the frequency ω_1/a_1. As with the feedforward based ΣΔM, the location of zero determines the noise shaping and stability of the system. However, unlike the feedforward based ΣΔM, the location of zero in this topology depends on the unity gain frequency of the first integrator. The impact of this on the ΣΔM design is discussed in the next sub-section.

As in the feedforward based ΣΔM, the NTF of feedback based second order ΣΔM topology with linear model assumption can be expressed as:

$$NTF = \frac{s^2}{s^2 + s \cdot a_1\omega_2 + \omega_1\omega_2} \tag{1.14}$$

$$STF = \frac{\omega_1\omega_2}{s^2 + s \cdot a_1\omega_2 + \omega_1\omega_2} \tag{1.15}$$

2.3.4.3 Comparison of Feedforward and Feedback based Topologies

The difference between the NTF of a first-order and a second-order ΣΔM is illustrated in Figure 2.15. The NTF of both feedforward and feedback ΣΔM topologies is similar and, therefore, it is possible to achieve the same SQNR with either topology. However, there are several differences and trade-offs attached in application of the two structures, as discussed here:

1. The location of the NTF zero in a feedforward topology is set by ω2/c1 while that for feedback topology is set by ω1/a1. This implies that for the modulator to be stable, the unity gain frequency of the first integrator in a feedback topology cannot be very high while no such restriction exists for the feedforward topology. Therefore, the unity gain frequency of the first integrator in feedforward topology can be much higher than in the feedback topology. The higher first integrator gain in the feedforward structure helps to supress thermal noise of the second stage and leads to lower power consumption or better noise performance in this structure.

2. The STF of the feedback topology has a low pass response, while the additional zero in the STF of feedforward topology enables a flat response. This implies that the feedback topology is more effective in suppressing the out of band interferers while the feedforward topology is more suitable for wide-band applications.

3. The output swing of the first integrator in a feedforward topology is much smaller than that in a feedback topology. This is because the integrator in the feedback topology must cancel the large signal in the feedback path. The larger output swing may cause issues in circuit implementation.

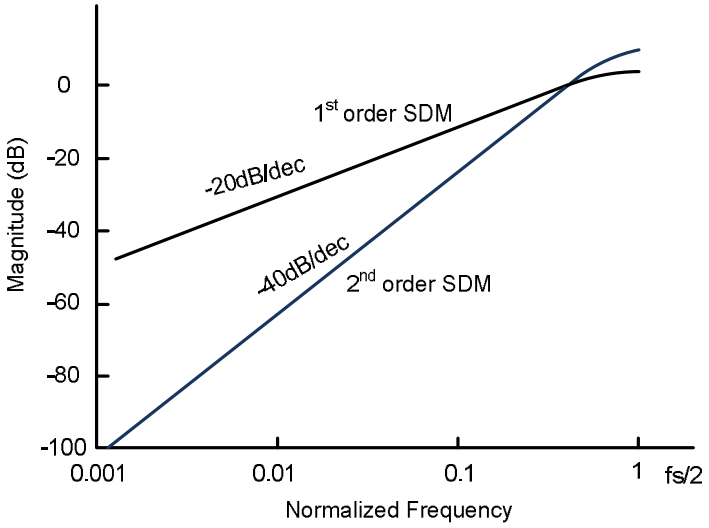


Figure 2.15 - Noise transfer function (NTF) of first and second order ΣΔM

2.3.5 Continuous-Time vs. Discrete-Time Sigma Delta Modulator

A sigma delta modulator may be implemented using either a continuous-time (CT), discrete-time (DT), or hybrid loop-filter. In general, the same noise shaping can be achieved irrespective of the loop-filter structure. The major differences between CTΣΔM and DTΣΔM are summarized in this section.

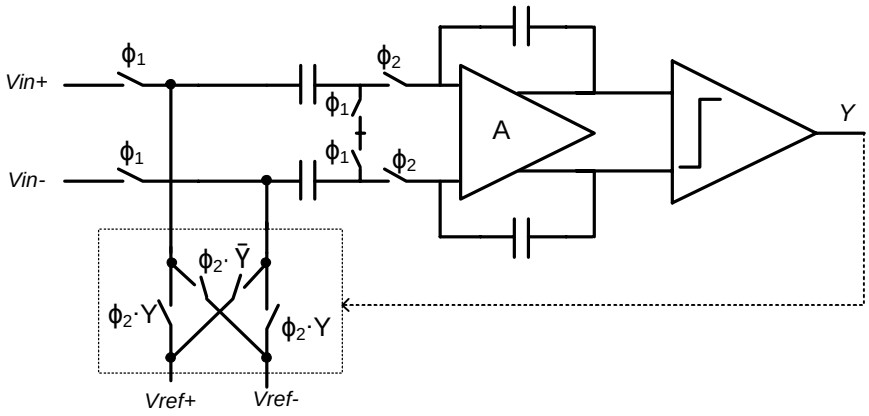


Figure 2.16 - A discrete-time implementation of a ΣΔM

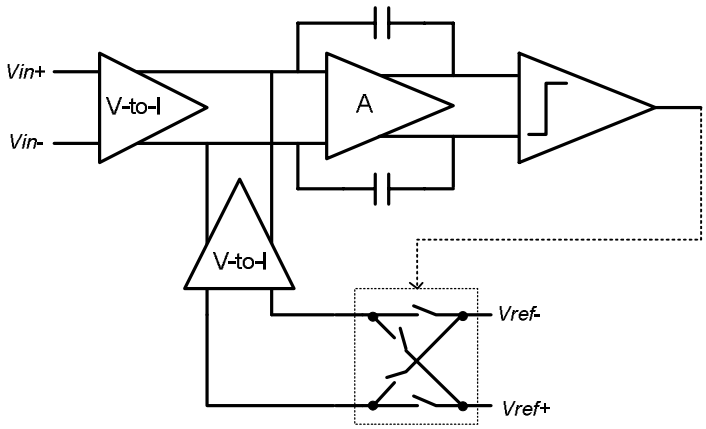


Figure 2.17 - A generic continuous-time implementation of a ΣΔM

2.3.5.1 Thermal Noise

The input referred thermal noise of a DTΣΔM is dependent on the size of the sampling capacitor and the oversampling ratio. It can be expressed as [26]:

$$V_{n,in,DTSDM}^2 \approx 2 \cdot \frac{kT}{C} \cdot \frac{1}{OSR} \tag{1.16}$$

Considering an oversampling ratio of 1000, a sampling capacitor of about 3nF is needed to achieve a noise floor of 20nV/$\sqrt{Hz}$.

On the other hand, the input referred noise of a CTΣΔM depends on the size of input stage resistor or transconductor. To achieve a noise floor of 20nV/$\sqrt{Hz}$, the input *V-to-I* stage must consist of a resistor less than 5kΩ or a transconductance greater than 0.2mS.

2.3.5.2 Gain Accuracy

The main advantage of DTΣΔMs is that the gain is set by ratio of capacitors and therefore, very high accuracy and linearity can be achieved. It is easy to achieve resolution and linearity greater than 20 bits with DTΣΔMs. On the other hand, the accuracy and linearity of CTΣΔMs is dependent on the input *V-to-I* stage. They are limited if a transconductor input stage is used while accuracy and linearity can be very high if resistors are used for *V-to-I* conversion [27], [28].

2.3.5.3 Antialiasing

In a DTΣΔM, sampling is performed at the input switched-capacitor stage. Therefore, the sampling process can cause aliasing of out-of-band interferers and noise into the signal band. This is why an off-chip low-pass filter is placed as part of the signal conditioning circuit in the conventional sensor readout chain based on a DTΣΔM.

In a CTΣΔM, the sampler is placed after the loop filter and in front of the quantizer. Therefore, the loop-filter suppresses the frequency components greater than sampling frequency before they are sampled. This lends inherent antialiasing ability to the CTΣΔM which is a significant advantage over DTΣΔMs and eliminates the need for any off-chip filters.

2.3.5.4 Input Impedance

The switched capacitor input stage of a DTΣΔM has a dynamic input-impedance set by the sampling frequency and the size of the sampling capacitor (~$1/f_S \cdot C$). A small sampling capacitor or low sampling frequency is needed to increase the input impedance of this structure. The need for high input impedance and low noise impose contrasting requirements on the capacitor size. Moreover, the dynamic nature of the input impedance requires that a buffer precede the DTΣΔM for applications requiring high precision.

The input impedance of a CTΣΔM is well-defined. An RC integrator based CTΣΔM has low input impedance while a *Gm*-C integrator based CTΣΔM has high input impedance. Therefore, a *Gm*-C integrator based CTΣΔM is perfectly suited for the precision sensor readout applications from the input impedance point of view.

2.3.5.5 Power Dissipation

The fast settling time required in DTΣΔM for high sampling frequency makes them unsuitable for very high frequency applications. Therefore, CTΣΔMs have become popular for high speed applications due to their lower power consumption. However, in terms of power dissipation, there is not much difference between the two implementations for low frequency applications.

2.4 Dynamic Precision Techniques

The typical $1/f$ noise corner in CMOS amplifiers in the target 0.7 µm technology node is in the order of 10-20 kHz while the DC offset can easily to be in the order of 10mV. These errors limit the achievable resolution in sensor readout applications and must be removed from the signal band. There are two commonly used dynamic techniques for reducing $1/f$ noise and DC offset in the signal band: (a) chopping, and (b) autozeroing. In this section, the underlying principle of these techniques will be briefly reviewed along with the pros and cons of each approach.

The mismatch between input and feedback *Gm* causes gain error in a CFIA. A common dynamic technique used for improving the matching of two elements is called dynamic element matching (DEM) and is discussed in this section.

2.4.1 Autozero Amplifier

The autozeroing technique involves sampling the offset and subtracting it from the output of the amplifier, thereby cancelling the offset, as shown in Figure 2.18. The low frequency $1/f$ noise is also cancelled in the same way as offset [29].

However, there are two main issues with autozero amplifiers:

(a) They work in two phases: the sampling phase and the gain phase. The amplifier offset is sampled in a capacitor during the sampling phase and during this time, the amplifier cannot be used. Thus, it is not possible to use the autozero amplifier in continuous-time applications. It is possible to use two autozero amplifiers in ping-pong topology where one amplifier is amplifying while the other amplifier is sampling the offset. This enables continuous-time operation, but leads to additional power and area over head.

(b) Due to the sampling process, the thermal white noise of the amplifier is folded back into the signal band. This causes an increase in the noise floor of the autozeroed amplifier. Therefore, it is not the most power efficient technique for very low-noise applications.

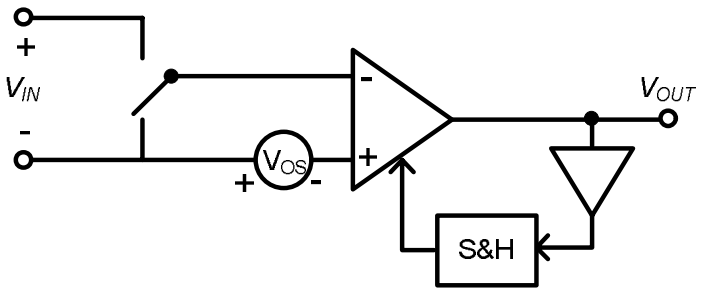


Figure 2.18 - Basic autozero amplifier

2.4.2 Chopper Amplifier

Chopping is a dynamic technique that works by modulating the offset and 1/*f* noise of the amplifier to a carrier frequency outside the band of interest. This out of band errors can then be filtered-out to achieve high resolution. The basic technique of chopping is illustrated in Figure 2.19. The switches at the input of the amplifier modulate the signal to a carrier frequency, known as the chopping frequency. The input referred offset and the 1/*f* noise of the amplifier add to the modulated input signal and are amplified. The chopping switches at the output node then demodulate the input signal back to the baseband frequency while the offset and 1/*f* are modulated to the chopping frequency and filtered-out by a low pass filter. The chopping frequency for low-bandwidth systems is usually chosen to be at least twice the 1/*f* corner frequency to prevent the tail of 1/*f* noise from appearing in the signal band.

There are several issues that must be considered in the implementation of the chopper. Firstly, the offset is amplified by the DC gain of A_1 (in Figure 2.19), while the signal is amplified by the effective gain of A_1 at the chopping frequency. Therefore, the effective DC gain of the chopper amplifier can drop if the amplifier bandwidth is smaller than chopping frequency [29]. Secondly, any mismatch in charge injection from chopper switches can create a residual offset. This residual offset is proportional to the chopping frequency but can be removed by use of nested or system level chopping techniques [12]. Thirdly, the chopper output has a ripple at chopping frequency proportional to the offset voltage, as shown in Figure 2.19E. This ripple needs to be filtered out if the chopper is followed by a sampler as the ripple can fold back into the signal band due to sampling. Furthermore, the bandwidth of chopper amplifier is limited by the chopping frequency as it cannot process any signal at higher frequency.

2.4.3 Dynamic Element Matching

Dynamic element matching is a technique in which the circuit elements that are to be matched are constantly shuffled to attain better matching ‘on average’. In a similar way to chopping, DEM creates a ripple at the frequency of shuffling the components. This technique can be used to improve the matching between the input and feedback transconductors of the CFIA in order to reduce the gain error [12].

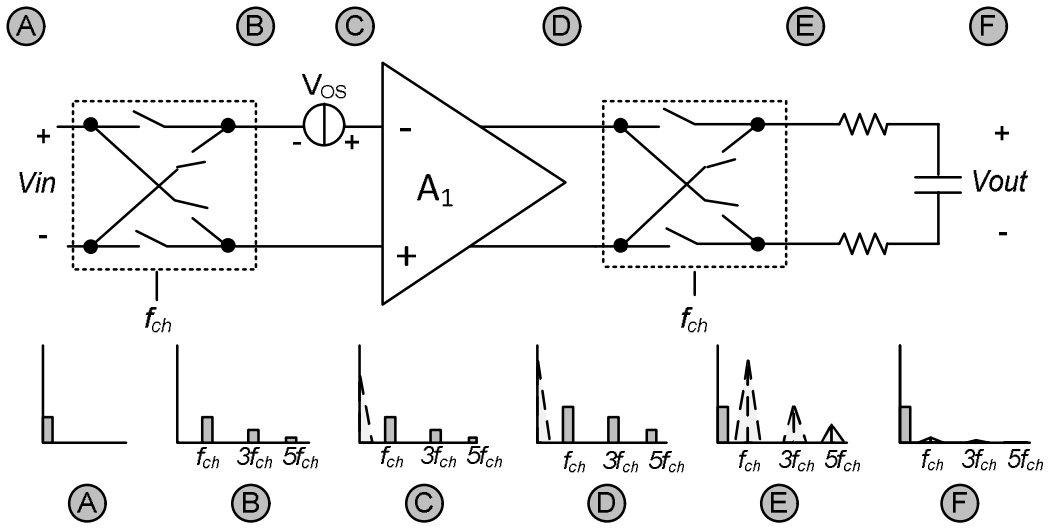


Figure 2.19 - Reducing the effect of *1/f* noise and offset by chopping

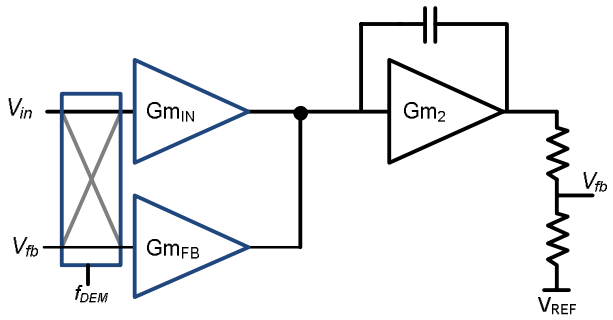


Figure 2.20 - Dynamic element matching to reduce the mismatch between input and feedback transconductors

DEM reduces the gain-error due to mismatch by modulating the error to a higher frequency, similar to chopping. Although a perfect chopper scheme can get completely rid of the additive offset error, DEM is used here to correct a multiplicative gain error term which cannot be reduced completely. To analyse the improvement in gain-error by use of DEM, let us consider that the feedback transconductor (Gm_{FB}) assumes a value different from input transconductor (Gm_{IN}) and can be expressed, without loss of generality, as:

$$Gm_{FB} = Gm_{IN}(1+\Delta) \tag{1.17}$$

where, Δ is the mismatch between two transconductors. If the input and feedback transconductors are periodically swapped, the resulting average gain of the system will be [30]:

$$Gain_{AVG} = \frac{\frac{Gm_{IN}}{Gm_{FB}} + \frac{Gm_{FB}}{Gm_{IN}}}{2} \approx 1 + \frac{\Delta^2}{2} \tag{1.18}$$

Thus, it can be seen that use of DEM can significantly reduce the gain error in a CFIA. Typically, it is possible to achieve a gain error in the order of 1% with good layout. This can then be improved to be in the order of 0.01% by use of DEM.

2.5 Summary

In this chapter, the major precision sensor measurement techniques are reviewed. Although there was a significant amount of research on the applications of CTΣΔMs for sensor readout applications in the late 80s and 90s, the nonlinearity of the available input V-to-I stages limited their use in high precision applications. The preamplifier plus DTΣΔM based architecture has now become the de-facto standard for precision sensor readout systems. The preamplifiers used in commercial systems are usually based on two-opamp and three-opamp topologies. However, it has recently been shown that a readout system based on CFIA can achieve similar performance with lower power dissipation and better CMRR.

There are several similarities between a CFIA and a Gm-C based CTΣΔM as both operate in the current mode and employ a high-impedance but nonlinear input stage. The feedback nonlinearity compensation technique enables the CFIA to achieve high linearity even with a nonlinear input stage. In the next chapter, the use of this compensation technique for improving the linearity of a Gm-C based CTΣΔM is analysed in detail.

3 Gm-C based Continuous-Time Sigma-Delta Modulator with Improved Linearity

As discussed in Chapter 2, conventional readout systems consist of a low-noise preamplifier followed by a high-resolution ADC. This chapter discusses ways to merge these two sub-systems into a single CTΣΔM. Such a single-stage readout system is easier to optimize for a given application. A CTΣΔM with a Gm-C input stage can achieve resolution similar to a system composed of a preamp and a DTΣΔM. The input Gm-stage also buffers the bridge, thereby eliminating the need for the preamp However, its nonlinearity is a significant disadvantage and the primary goal of this work is to reduce this error.

3.1 Overview of the Concept

Conventional precision sensor readout systems typically consist of an instrumentation amplifier for signal conditioning followed by a high-resolution ΣΔM. The CFIA has been shown to outperform traditional two-opamp IAs due to their ground sensing ability, lower power consumption and high CMRR [30]. Figure 3.1 shows the basic architecture of a sensor readout system that employs a CFIA based preamp followed by a ΣΔM.

The architecture shown in Figure 3.1 facilitates a structured design approach. The first stage dictates the noise and offset performance, while the second stage drives the digital output. This orthogonalization simplifies the design procedure at system level. However, this approach can lead to suboptimal performance due to overdesign of the two stages.

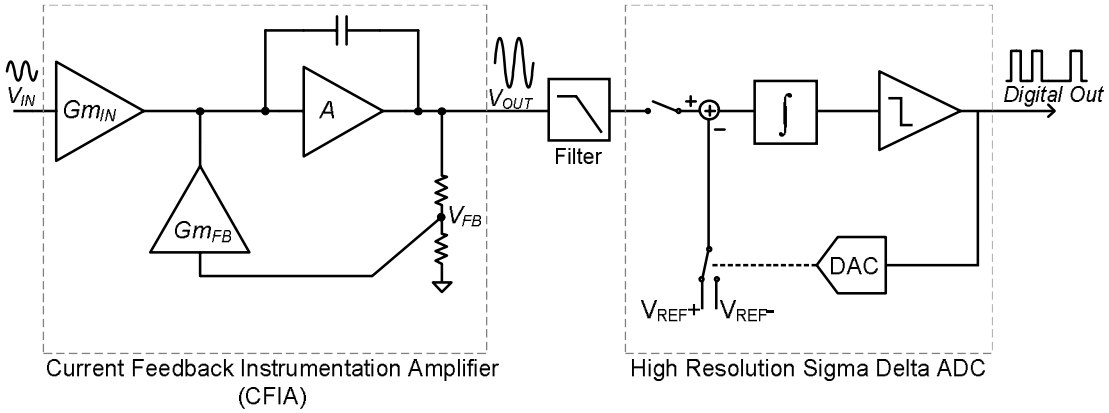


Figure 3.1 - Basic architecture of a precision sensor readout system based on a CFIA and ΣΔM

However, both the low-noise instrumentation amplifier (IA) and the high-resolution ΣΔM require high-gain stages in the loop which lead to increased analog complexity and higher power consumption. The IA also requires precision off-chip resistors either for setting the gain (in the CFIA) or for obtaining high CMRR (in the two-opamp IA). The interface between the preamplifier and the ΣΔM is also complicated by the preamplifier employing a dynamic offset cancellation technique. For instance, if the preamplifier uses chopping to reduce the offset, an off-chip low pass filter [20] or a ripple reduction loop [11] may be necessary to suppress the chopper ripple before the signal is fed to the ADC.

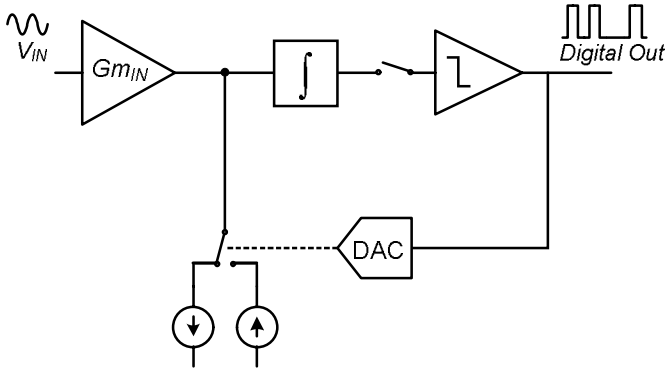


Figure 3.2 - Conceptual architecture for a single stage conversion of sensor signal.

In contrast to the traditional architecture, the use of a CTΣΔM for interfacing directly with the sensor (Figure 3.2) can simplify the design procedure. The operational transconductance amplifier (OTA) used for voltage-to-current (V-to-I) conversion can also perform the role of a preamplifier which can be useful for optimizing power dissipation. This single-step digitization system eliminates the need for any overhead circuitry required for interfacing between the IA and the ADC. Furthermore, the antialiasing capability of the CTΣΔM obviates the need for any off-chip antialiasing filter. Therefore, a CTΣΔM based readout can potentially achieve the same performance as the traditional readout systems, but with lower power consumption and fewer off-chip components.

However, the CTΣΔM architecture shown in Figure 3.2 suffers from gain error and linearity issues. The linearity of Gm-C based filters and CTΣΔM has been addressed in the past using circuit level and system level techniques. The following sections review some of the approaches used for improving the linearity of Gm-C based CTΣΔMs.

3.2 Circuit Level Techniques for Linearization of Transconductors

In this section, the non-linearity of a simple MOS differential pair is discussed. This is followed by a review of circuit level techniques for improving its linearity. These can be broadly divided into three main categories: (a) source degeneration, (b) adaptive biasing and (c) cross-coupled differential pair.

3.2.1 Background - Nonlinearity in a MOS Differential Pair

A simple MOS differential pair based transconductor consists of two common source transistors tied to a tail current source (Figure 3.3a). A small increase in the input differential voltage leads to a proportional increase in the difference between the currents flowing through the two branches. As the input differential signal is increased, the current imbalance between the two branches

increases and eventually, it approaches the saturation level set by the tail current source. This results in a nonlinear V-I transfer function as shown in Figure 3.3(b). The resulting nonlinear transconductance as a function of the differential input voltage is shown in Figure 3.3(c)

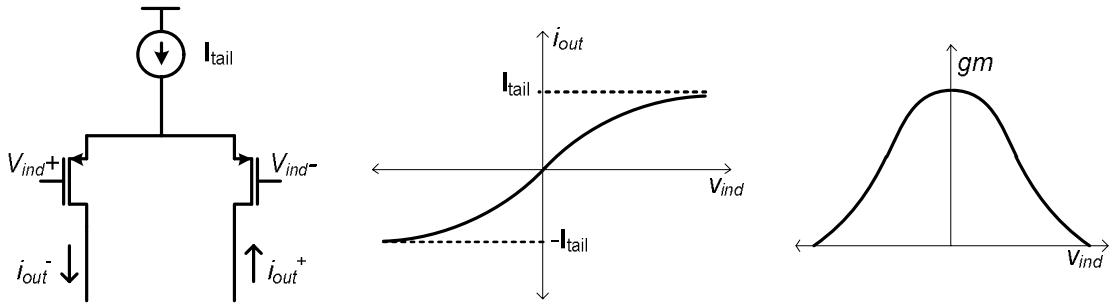


Figure 3.3 - (a) A simple MOS differential pair built using PMOS transistors; (b) voltage to current transfer function of a differential pair (c) nonlinear transconductance of the differential pair

Assuming that the two MOS transistors of the differential pair are operating in the saturation region, the quadratic dependence of current on the gate-source voltage (V_{GS}) leads to a nonlinear transfer function that can be approximated by the following expression [7]:

$$i_{out} = \frac{1}{2}\beta . v_{ind}\sqrt{\frac{4I_{tail}}{\beta} - {v_{ind}}^2} \tag{3.1}$$

where, β is a constant dependent on technology and transistor sizes, I_{tail} is the tail current of differential pair, and v_{ind} is the differential input voltage. The transistors may even be biased in the weak inversion region to achieve lower power consumption and higher noise efficiency, in which case, the transfer function of differential pair follows a hyperbolic tangent function and is expressed as [31]:

$$i_{out} \propto I_o \tanh\frac{v_{ind}}{2(V_{GS} - V_T)} \tag{3.2}$$

where, I_o is the saturation current of MOS in sub-threshold region. The Taylor expansion of this nonlinear voltage-current transfer function can be generalized, irrespective of the region of operation, as:

$$i_{out} = gm_1 v_{ind} + gm_3 {v_{ind}}^3 + gm_5 {v_{ind}}^5 + ... \tag{3.3}$$

where, gm_1, gm_3, gm_5 are the coefficients derived from the Taylor series expansion. The even harmonics are cancelled out due to the differential nature of the circuit and therefore, do not affect the overall linearity. The expression for the output current for a sinusoidal input voltage signal - $A\sin(\omega t)$ - applied to the differential pair, ignoring the higher order terms, is:

$$i_{out}(t)|_{v_{ind}=A\sin(\omega t)} = \left(gm_1 A + \frac{3}{2}gm_3 A^3\right)\sin(\omega t) + \frac{1}{4}gm_3 A^3 \sin(3\omega t) + \ ... \tag{3.4}$$

This equation highlights the third order harmonic component and the gain expansion component at the signal frequency. Therefore, the THD is a function of the coefficients of nonlinearity and input signal amplitude. The gain expansion term can lead to a nonlinear gain error at the signal

input frequency. Several circuit level techniques have been proposed in the past to tackle the nonlinearity of the simple differential pair [6-8], [32]. Three of the important techniques are reviewed in this section.

3.2.2 Source Degeneration

Source degeneration is a local feedback based technique employed to reduce the dependence of gain on the nonlinear transistors. As shown in Figure 3.4, the effective transconductance of a degenerated differential pair is dependent on a resistor, thereby resulting in a less nonlinear transfer function.

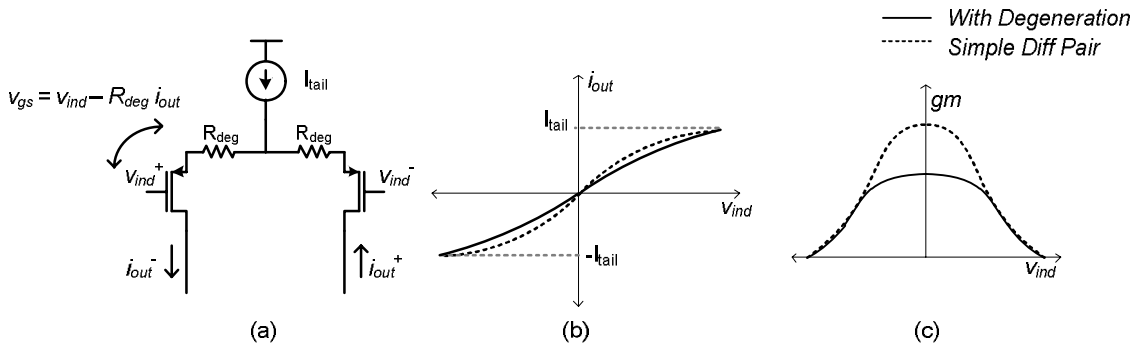


Figure 3.4 - (a) Differential pair with resistive degeneration (b) voltage-to-current transfer of the differential pair (c) Gm of the differential pair

Degeneration introduces a local negative feedback path by making the gate-source voltage of the transistor dependent on the output current. Therefore, equation (3.3) can be re-written for a degenerated differential pair as follows (ignoring higher order terms):

$$i_{out} = gm_1(v_{ind} - R_{deg} i_{out}) + gm_3(v_{ind} - R_{deg} i_{out})^3 + \ldots \tag{3.5}$$

Assuming a degeneration factor of N (=$gm_1\, R_{deg}$), the relation can be expressed as:

$$i_{out} = \frac{gm_1}{1+N} v_{ind} + \frac{gm_3}{1+N}(v_{ind} - R_{deg} i_{out})^3 \tag{3.6}$$

The local feedback mechanism reduces the effective differential signal amplitude across the nonlinear transistor by the degeneration factor, thereby reducing distortion. A more thorough analysis reveals that the THD can be reduced by the square of the degeneration factor N [7] with this mechanism. However, at the same time, the fundamental gain drops by a factor of N and the input referred noise increases by the same factor [6] too. Therefore, it requires more power dissipation for the same noise level. Furthermore, considering a nominal THD of a simple differential pair to be in the order of 1% and a degeneration factor of 10, the improvement in THD is not sufficient for precision sensor readout applications. A higher value of the degeneration factor is prohibitive due to the increase in the power dissipation.

Other local feedback based linearization techniques have been suggested in the past [6]. However, all such techniques reduce the distortion at the cost of a lower fundamental gain and increased thermal noise, which in turn leads to higher power dissipation. Therefore, they are not ideally suited to the requirements of high-precision sensor readouts. In contrast, a global feedback

mechanism can offer better trade-off for the linearity, noise and power dissipation of the readout circuit.

3.2.3 Adaptive Biasing

The input signal range in a differential pair is primarily restricted by the strong distortion caused by the limited tail current. An adaptive biasing technique modulates the tail current with the input signal (Figure 3.5) to reduce the strong nonlinearity caused by current saturation. This is done by increasing the tail current for larger differential signals to avoid slewing and reducing the tail current for smaller signals to conserve power [7]. As shown in Figure 3.5b, the tail current can be increased for large differential input signals to extend the linear range of the system. However, the distortion for small input is caused by the nonlinearity in MOS transistor, and remains unchanged.

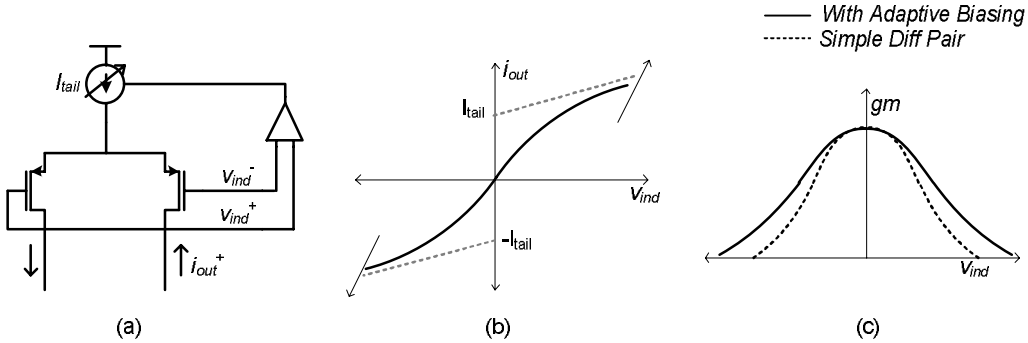


Figure 3.5 - (a) Basic concept of adaptive biasing (b) tail current is modulated depending on differential input signal (c) Gm of the differential pair

Although this technique can increase the linear range of input signal, nonlinearity in the modulation of the tail current can potentially lead to a new source of distortion in the system. . Furthermore, there is only a limited improvement (20-30dB) in the THD for small input signal levels [7]. Additionally, this requires implementation of additional circuitry that adds to the area and power dissipation of the device.

3.2.4 Cross-coupled Differential Pair

A cross-coupled pair works on the principle that two differential pairs can be used to cancel out the nonlinear part of the transfer function without significantly reducing the fundamental gain [6]. This is achieved only if the distortion coefficients of two differential pairs are matched while their fundamental gain terms are different as illustrated in Figure 3.6.

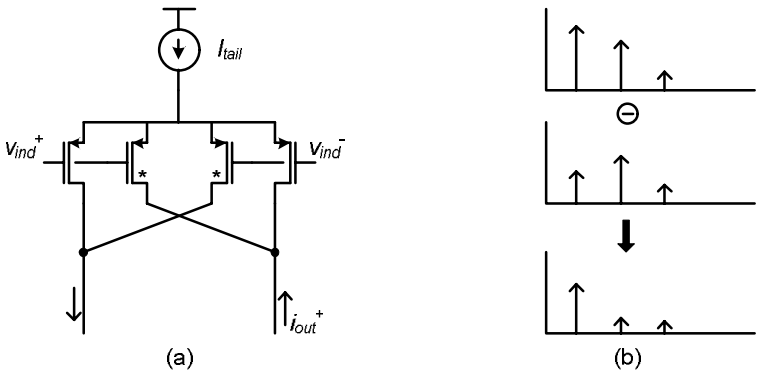


Figure 3.6 - (a) Schematic of a cross-coupled differential pair; (b) operation of cross-coupled differential pair

The general principle of operation of a cross-coupled differential pair can be understood by considering the following transfer functions of the two differential pairs:

$$i_{out} = gm_1 v_{ind} + gm_3 v_{ind}{}^3 + \ldots \qquad i^*_{out} = gm^*_1 v_{ind} + gm^*_3 v_{ind}{}^3 + \ldots$$

The transfer function of resulting cross-coupled differential pair can then be expressed as:

$$i_{out} = (gm_1 - gm^*_1) v_{ind} + (gm_3 - gm^*_3) v_{ind}{}^3 + \ldots \tag{3.7}$$

If $(gm_1 - gm^*_1)/(gm_3 - gm^*_3) > gm_1 / gm_3$, a higher THD is achieved than a simple differential pair. This principle was first applied to MOS based multipliers using the square law dependence of output current on the input differential voltage [6], [33]. However, the distortion coefficients of transistors depend on the region of transistor operation and technology. Suppressing the distortion coefficients without significantly affecting the fundamental gain term can be tricky when the transistors operate in the weak inversion region. Moreover, the additional circuitry required to implement cross-coupled stage also consumes more power and area.

3.2.5 Summary of Circuit Level Techniques for Nonlinearity Suppression

The three techniques discussed in this section and their combinations are the most commonly used ways for suppressing the nonlinearity of a transconductor. In precision sensor readout systems, the input signal is relatively small and the techniques based on adaptive biasing for extending linear range are not very useful for improving the weak distortion for these small signals. The source degeneration or local feedback based techniques result in a trade-off between noise, linearity and power dissipation. A global feedback approach can offer better trade-offs for linearizing the system. It is also interesting to note that a CFIA employs nonlinearity cancellation [23], similar to a cross-coupled differential pair, along with the global feedback to improve the overall THD. Therefore, the system level negative feedback based techniques can offer many benefits over the circuit level techniques as discussed in the next section.

3.3 Negative Feedback based Linearization

The primary motivation for Black's original work on negative feedback was to reduce nonlinearity of amplifiers based on vacuum-tubes [34]. Over the years, negative feedback has been employed for suppressing the noise, nonlinearity, and other errors in amplifiers, PLLs, ΣΔMs and many other applications. In this section, the general theory of nonlinearity suppression using negative feedback is discussed. The focus is on supressing distortion of the input Gm stage of a CTΣΔM.

3.3.1 Basic Feedback Theory for Suppression of Nonlinearity

The underlying principle in reduction of nonlinearity through feedback can be understood by considering the nonlinearity as an additive error at the output of amplifier. We assume that the error caused by the amplifier nonlinearity is additive error from a nonlinear source (Figure 3.7(b)).

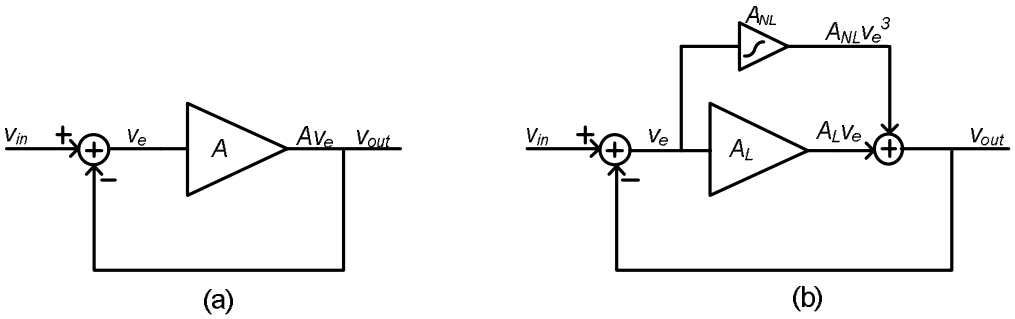


Figure 3.7 - (a) A nonlinear amplifier in negative feedback (b) the amplifier decomposed into combination a linear amplifier and a nonlinear amplifier

The amplifier shown in Figure 3.7(a) is decomposed into a linear and a nonlinear component as shown in Figure 3.7(b). For simplicity, we only consider third order distortion in the amplifier. The closed loop transfer function of the amplifier can then be expressed as:

$$v_{out} = A_L v_e + A_{NL} v_e^{\,3} \tag{3.8}$$

where, A_L is the linear gain of amplifier, A_{NL} is the coefficient of nonlinearity and v_e is the error voltage equal to $(v_{in} - v_{out})$. Substituting this to the equation(3.8), we get:

$$v_{out} = A_L \left(v_{in} - v_{out}\right) + A_{NL} \left(v_{in} - v_{out}\right)^3 \tag{3.9}$$

The equation can be re-written with the approximation that $v_{in} - v_{out} = v_e \approx v_{in}/(1 + A_L)$ as:

$$v_{out} = \frac{A_L}{1 + A_L} v_{in} + \frac{A_{NL}}{(1 + A_L)^3} \left(v_{in}\right)^3 \tag{3.10}$$

This is an important result as it shows the two mechanisms through which negative feedback leads to reduction in the nonlinearity and an increase in the input linear range of the amplifier. Firstly, the error signal applied to the amplifier in a feedback loop is much smaller than the actual input signal as $v_{in} - v_{out} = v_e \approx v_{in}/(1 + A_L)$. Secondly, the nonlinear gain coefficient (A_{NL}) is also attenuated by the loop gain. These two mechanisms together contribute to a significant reduction in the THD.

It was mentioned earlier that source degeneration also uses the principle of feedback for linearization. Although, the local feedback approach of degeneration works well for many circuits, it leads to a three-way trade-off between the noise, the linearity and the fundamental gain of the amplifier. In an ΣΔM, the gain of first stage is important for the shaping of quantization noise as well as for reducing the noise and errors from the following stages. A global feedback approach, therefore, offers far greater benefits from power efficiency standpoint as the gain of first stage is not traded-off for linearity.

3.3.2 Nonlinearity Cancellation through Negative Feedback

Consider a modified version of feedback architecture shown in Figure 3.7, where the nonlinear amplifier is outside the loop with another identical element placed in the feedback. If the two amplifiers are perfectly matched and the amplifier gain is high enough, the feedback ensures that the output signal, v_{out}, is identical to the input signal, v_{in}. Therefore, the feedback amplifier perfectly compensates the distortion generated by the input amplifier, thereby improving the overall THD.

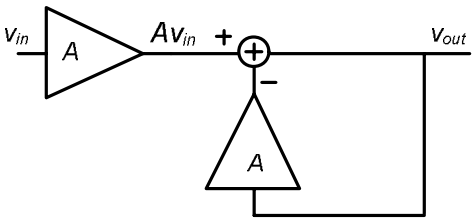


Figure 3.8 - Negative feedback for nonlinearity cancellation

A simple analysis of this loop considering only third order distortion indicates a reduction in overall distortion, as shown by the following equations:

$$v_{out} = A_L\left(v_{in} - v_{out}\right) + A_{NL}\left({v_{in}}^3 - {v_{out}}^3\right) \tag{3.11}$$

Using the relation ${v_{in}}^3 - {v_{out}}^3 = (v_{in} - v_{out})^3 + 3v_{in}v_{out}(v_{in} - v_{out})$ along with the first-order assumption $v_{in} - v_{out} \approx v_{in}/(1 + A_L)$, we get the following equation

$$v_{out} = \frac{A_L}{1 + A_L}v_{in} + \frac{A_{NL}}{(1 + A_L)^3}{v_{in}}^3 + 3\frac{A_{NL}A_L}{(1 + A_L)^2}{v_{in}}^3 \tag{3.12}$$

The second term on right hand side of the above expression represents the suppression of distortion coefficient in this architecture, and is similar to that shown in the equation (3.10) for architecture of Figure 3.7.

The resulting improvement in HD3 in this architecture is roughly $3/(1 + A_L)$, where A_L is the linear gain of the amplifier. The difference between the two negative feedback architectures is that the input signal amplitude applied to the nonlinear amplifier in this architecture is much larger than that of the architecture shown in Figure 3.7. Therefore, the linear range of this architecture is smaller than the feedback architecture of Figure 3.7. Although their linear range is smaller, current feedback instrumentation amplifiers (CFIA) employing this nonlinearity cancellation technique have been shown to achieve nonlinearity in the order of a few ppms [30].

The principle of nonlinearity cancellation (or compensation) by feedback has broad applications. For instance, it has been applied for linearizing a radio-frequency low-noise amplifier (RF-LNA) in the past [35]. However, application of this technique in a single-bit CTΣΔM is not straightforward. Due to the binary nature of the feedback bitstream, the nonlinearity in the feedback has no impact on the signal. As a result, the nonlinear element in the feedback path cannot compensate for the input stage nonlinearity. Therefore, special techniques to linearize a single-bit CTΣΔM are required and are discussed in the next section.

3.3.3 Characterizing and Modelling a Nonlinear Transconductor Stage for Simulation

In order to evaluate various techniques explored for reducing the nonlinearity of the system in this work, a practical model of nonlinear input stage was needed for simulations. To serve this purpose, the nonlinearity of a differential-pair biased in weak-inversion region with the desired noise performance was simulated in Cadence. The resulting transfer curve was fitted into a seventh order polynomial using MATLAB. The plots of original transfer curve and the fitted polynomial curve are shown in Figure 3.9.

The seventh order polynomial derived from MATLAB is given below:

$$i_{out} = v_{ind} + 21 \cdot v_{ind}^{\ 3} - 500 \cdot v_{ind}^{\ 5} + 110000 \cdot v_{ind}^{\ 7} \tag{3.13}$$

where i_{out} is the output current of the transconductor and v_{ind} is the differential input voltage. This transfer function corresponds to a THD of about 1% (-40dB) for a full-scale input of 40mV as shown in Figure 3.10

This polynomial model of the transconductor accurately represents the nonlinearity of a differential input stage and is used for all the system-level simulations in this thesis.

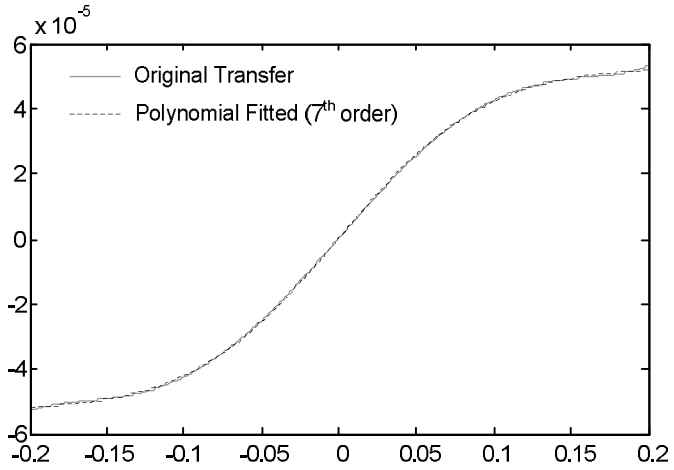


Figure 3.9 - Transfer plot of a nonlinear transconductor and corresponding polynomial fitted curve

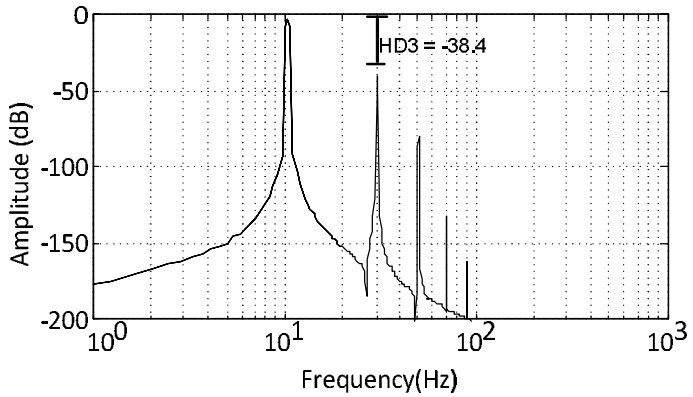


Figure 3.10 - The harmonic distortion for a sine-wave input signal with 40 mV amplitude

3.4 A CFIA with Digital Feedback as CTΣΔM

The simplistic architecture of a CTΣΔM shown in Figure 3.2, suffers from distortion due to the nonlinearity of the input transconductor. This can be reduced by using the feedback based nonlinearity cancellation theory. As discussed earlier, a CFIA uses the same technique for reducing the distortion. Therefore, the basic CFIA architecture [3], [4] can be used as a starting point to create a direct digitization system for the sensor signals. This can be done by replacing the resistor divider of a CFIA with an ADC and a DAC combination (Figure 3.11).

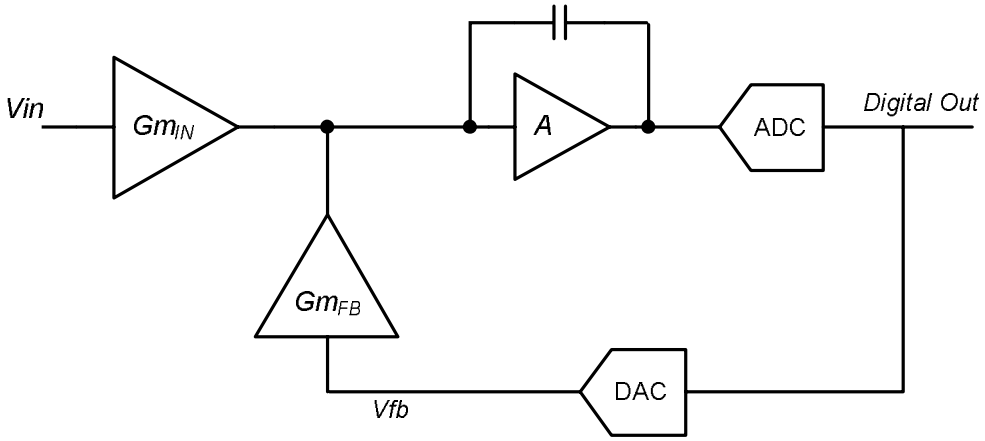


Figure 3.11 - General principle for direct digitization: A CTΣΔM created by replacing resistor divider of CFIA with an ADC-DAC combination

3.4.1 Single-bit ADC and DAC

The theory of suppression of the nonlinearity in a system through feedback does not apply to a single-bit ΣΔM. In the conventional feedback loop used in instrumentation amplifiers, the signal fed back from the output is an analog voltage or current signal. However, in a single-bit ΣΔM, the information is stored as an average of the output bitstream. In other words, the input signal value is represented in time-domain while the binary output toggles between the 1 and 0 as illustrated in Figure 3.12. The nonlinearity of the feedback transconductor (Gm_{FB}) only affects the voltage domain signals and has no impact on the time-domain average value, as illustrated in. The feedback transcondcutor only acts as a linear gain for the two-level voltage feedback signal. Therefore, the nonlinearity of the Gm_{IN} stage is not compensated by the feedback Gm_{FB} stage.

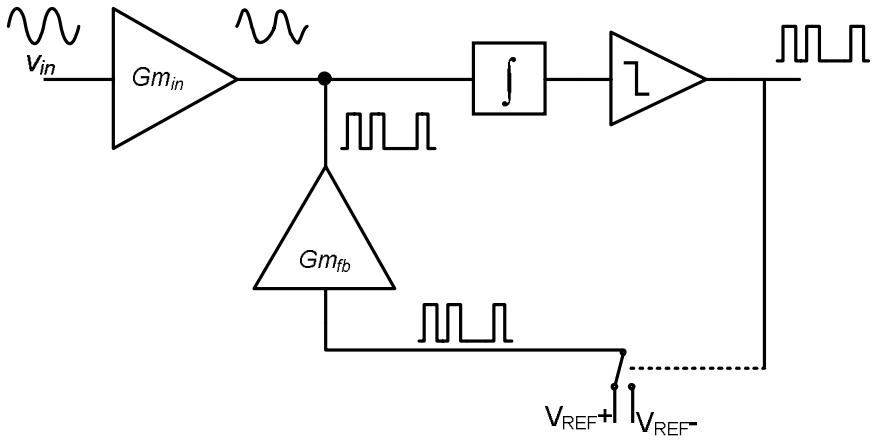


Figure 3.12 - CTΣΔM with single bit quantizer cannot enable cancellation of nonlinearities between input and feedback transconductors as it has no effect on two-level feedback signal

The advantage of a single bit ΣΔM is in the fact that the two-level feedback DAC is always linear. The transfer function of a single bit quantizer has only two points as shown in Figure 3.13. Therefore, a binary bitstream can only contain errors in the form of linear gain error or offset error. However, this implies that the nonlinearity of the input transconductor appears directly at the output.

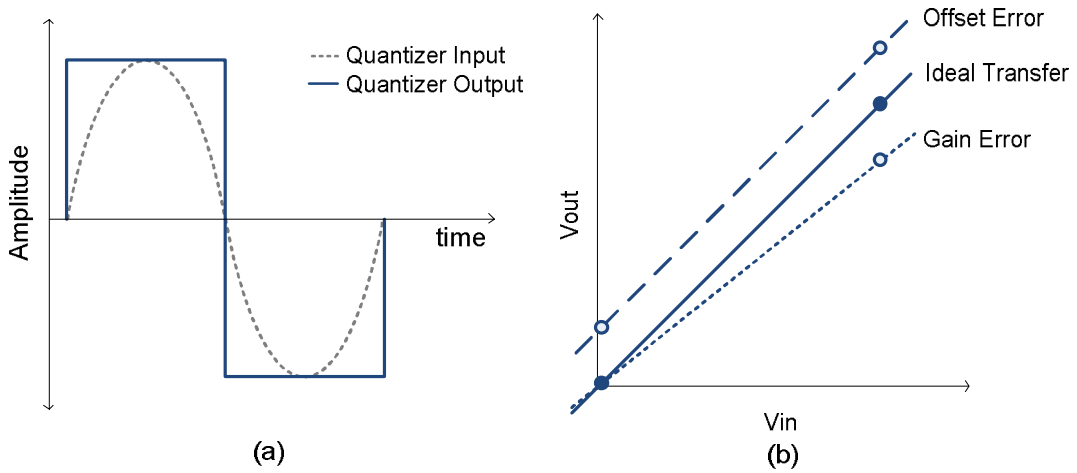


Figure 3.13 - (a) A sine wave input fed to a one-bit quantizer results in a square wave of same frequency
(b) Linear transfer function of a two-level signal

3.4.2 Multi-bit Sigma-Delta Modulator

A multi-bit ΣΔM employs a multi-bit quantizer and DAC to feedback a multi-level signal. If a multi-bit quantizer and DAC are used in place of the gain-setting resistors of CFIA, the feedback signal (Figure 3.14) is distorted by Gm_{fb} in the same way as the input signal is distorted by Gm_{in}. Therefore, assuming that Gm_{in} and Gm_{fb} are matched, the distortion of Gm_{in} is compensated through the feedback path leading to higher THD. However, the improvement in the THD depends on the number of levels of the quantizer and DAC.

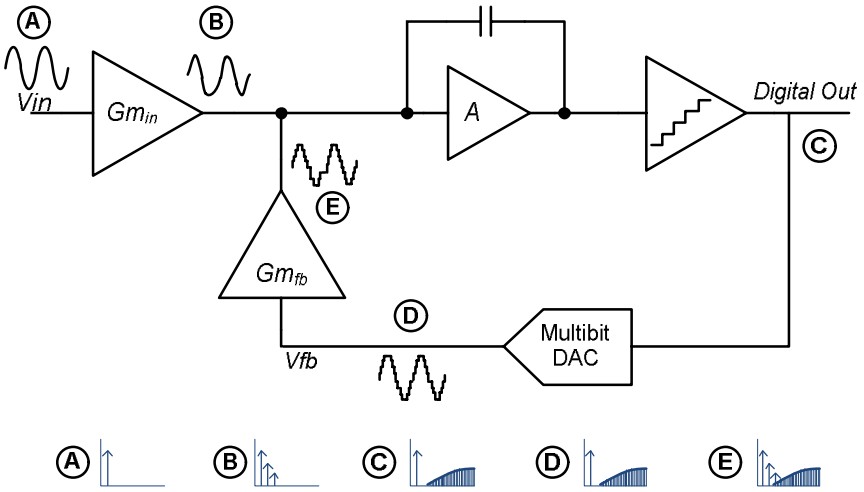


Figure 3.14 - Multi-bit CTΣΔM with nonlinearity compensation

Figure 3.14 illustrates the flow of signals in the system to show the improvement in linearity. The input signal at A is distorted by the transconductor nonlinearity and presented at B with odd harmonics of the input frequency. The feedback loop ensures that the output signal at C is a replica of the input signal. Therefore, the signal from the multi-bit DAC at D is distorted by the

feedback transconductor in the same way as the input signal, thereby compensating for the nonlinearity of the input transconductor. It may also be intuitively understood that a higher number of levels in the multi-bit DAC can enable better approximation of the ideal analog voltage. Therefore, the THD achieved using this technique is dependent on the number of bits in the multi-bit DAC. This architecture is simulated using a simple differential pair at the input biased in weak inversion with a THD of -40 dB to demonstrate this dependence. As shown in Figure 3.15, there is no improvement in THD for a single-bit DAC while the improvement saturates for multi-bit DACs with more than 5 bits. Implementation of this architecture using a 5-bit DAC with dynamic element matching has been shown to achieve a THD of -90dB [3].

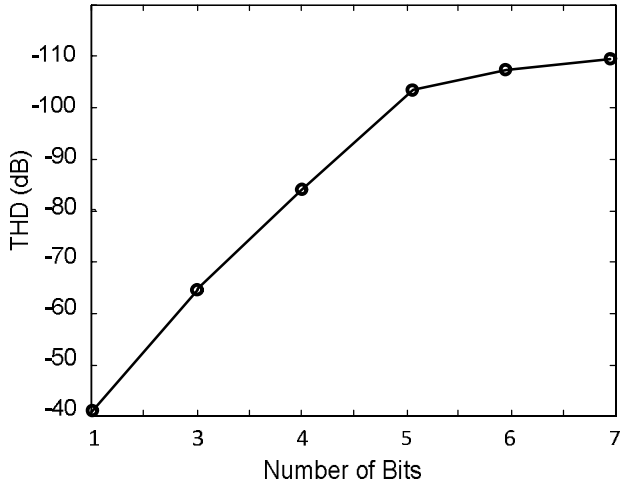


Figure 3.15 - THD vs. number of bits in a multi-bit CTΣΔM (assuming linear multi-bit DAC)

One of the major disadvantages of multi-bit ΣΔM is the nonlinearity caused by the mismatch of the DAC components. In a ΣΔM feedback loop, the quantizer nonlinearity is suppressed by the loop gain, but the DAC nonlinearity appears directly at the output node as it is in the feedback path. This limits the overall THD of the system. The distortion caused by the DAC can be reduced by using techniques like dynamic element matching (DEM). However, it is very challenging to achieve a linearity of greater than 100 dB with a 5-bit DAC

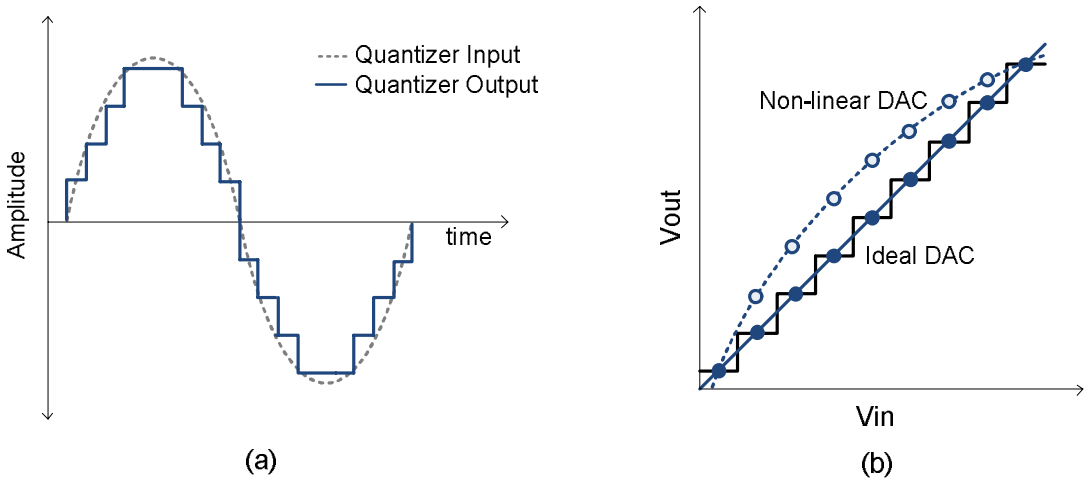


Figure 3.16 - (a) Multi-bit quantizer converts an analog signal to a multi-level signal; (b) the transfer function of a multi-bit quantizer (or DAC) which can be nonlinear

3.4.3 Frequency Domain Analysis

In the two preceding sub-sections, the impact of number of quantizer levels of the CTΣΔM on compensation of the transconductor nonlinearity was discussed. It can be seen from the time-domain view (Figure 3.16) that multiple levels of DAC enable an analog-like feedback signal that enables compensation of nonlinearity. However, the frequency domain view of this can be more revealing and helps to identify alternate solutions to the problem. In this section, the interaction of the DAC output signal with the nonlinear transconductor in feedback is presented from the frequency-domain perspective.

3.4.3.1 Overview

In an ideal single-bit or multi-bit CTΣΔM, the DAC output contains a replica of the input signal along with shaped quantization noise. In the architecture under consideration, this DAC output is fed back via a nonlinear transconductor. The nonlinearity generates intermodulation products between the input signal and quantization noise. These intermodulation products may fall into signal band, thereby limiting the achievable THD and SNR. The exact location of some of the intermodulation products between input signal and quantization noise can be shown to be on the odd-harmonics of the input signal which degrades the THD.

3.4.3.2 Intermodulation Distortion

If a two-tone signal is applied to the input of a nonlinear element, the resulting output signal will contain the harmonics of the two input signals along with its intermodulation terms. This can be seen from the effect of a third order distortion on a two-tone signal:

$$\begin{aligned}\left(A_1\sin(\omega_1 t)+A_2\sin(\omega_2 t)\right)^3 = {} & \frac{1}{4}A_1{}^3\sin(3\omega_1 t)+\frac{1}{4}A_2{}^3\sin(3\omega_2 t) && \triangleright\, 3^{rd}\ \textit{harmonic}\\ & +\frac{3}{4}A_1{}^3\sin(\omega_1 t)+\frac{3}{4}A_2{}^3\sin(\omega_2 t) && \triangleright\, \textit{Gain Expansion}\\ & +\frac{3}{4}A_1{}^2A_2\sin(2\omega_1\pm\omega_2)+\frac{3}{4}A_1A_2{}^2\sin(2\omega_2\pm\omega_1) && \triangleright\, \textit{Intermodulation}\end{aligned} \tag{3.14}$$

The output of a cubic transfer function consists of the third harmonic terms as well as the gain expansion and the intermodulation products.

3.4.3.3 Frequency Components of Quantization Noise

A conventional low-pass ΣΔM shapes the quantizer error through the action of the loop filter. This implies that low frequency quantization noise is suppressed and the frequency components close to half of the sampling frequency are amplified. The analysis of noise shaping in an ΣΔM is usually done under the assumption that the quantization noise is white. However, this assumption is not true as the quantization noise consists of tones that are strongly correlated to the input signal frequency.

To visualize this, consider a single-bit quantizer with a sine-wave input. The output of the quantizer is a square-wave with the same frequency as the input. This square-wave can be

decomposed by Fourier transform to a combination of sine waves at odd harmonics of the input frequency as shown in equation (3.15).

$$v_{sqwave}(t) = A\frac{4}{\pi}\left(\sin(\pi ft)+\frac{1}{3}\sin(3\pi ft)+\frac{1}{5}\sin(5\pi ft)+\frac{1}{7}\sin(7\pi ft)+\ldots\right) \tag{3.15}$$

where, A is the amplitude of the input signal and f is the frequency of the input square wave.

A single-bit quantizer also samples the input at a specified sampling frequency, f_S. Therefore, the high frequency components of the square wave are folded back into the band of frequencies up to half of the sampling frequency. This can be seen from the output frequency spectrum of a single-bit quantizer with a 1Hz sine wave input and a sampling frequency of 119.5Hz, as shown in Figure 3.17.

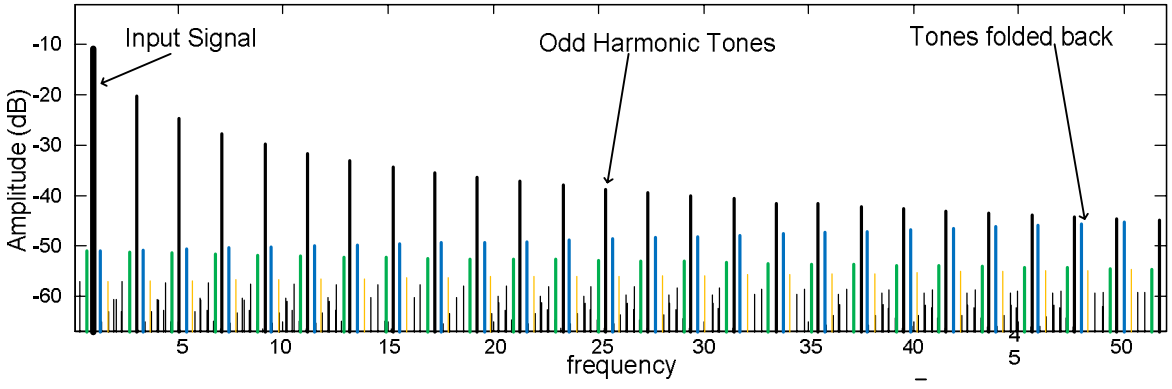


Figure 3.17 - Frequency Spectrum of output of a 1bit quantizer with sine wave input

The tones shown in Figure 3.17 can be classified as frequency components generated by three different processes, classified as follows:

a) Input signal: f_{in}
b) Odd harmonics of signal frequency such as $3f_{in}$, $5f_{in}$, $7f_{in}$:

$$(2N+1)\,f_{in,} \qquad \text{where } N \text{ is any integer} : N < f_S/(2f_{in}) \tag{3.16}$$

c) Higher frequency harmonics folded by sampling frequency:

$$(2K+1)\,f_{in} - Lf_{S,} \qquad \text{where } L,K \text{ are integers} : K > f_S/(2f_{in}) \tag{3.17}$$

It can also be shown that the output of a multi-bit quantizer also contains tones at the same frequencies as a single-bit quantizer, but the amplitudes of tones are not as strongly correlated. The frequency spectrum of a 3-bit and a 7-bit quantizer is shown in Figure 3.18.

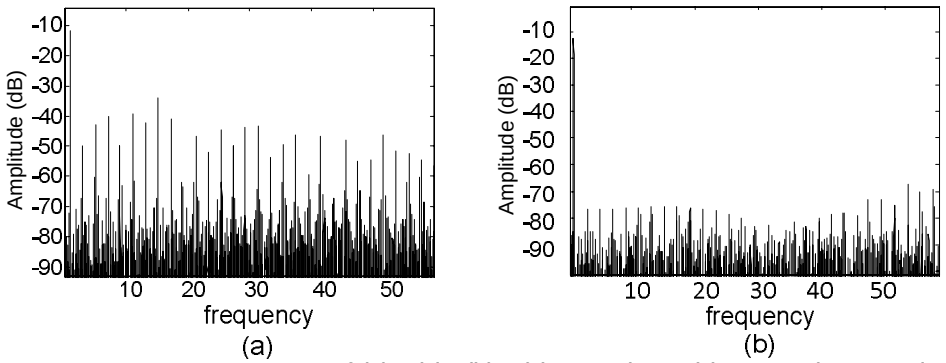


Figure 3.18 - Frequency response of (a) 3-bit; (b) 7-bit quantizer with a 1Hz sine wave input

3.4.3.4 Intermodulation of Quantization Noise

We have seen that quantization noise is indeed tonal and it is possible to identify the frequency of each of these tones. The low frequency tones produced by the quantizer are heavily suppressed by the loop gain. However, the high frequency tones in the quantization noise can mix with the input signal to produce significant intermodulation products that may fall into the signal band. These intermodulation products generated by the feedback transconductor are not suppressed by the loop gain. Therefore, they limit the overall THD of the system.

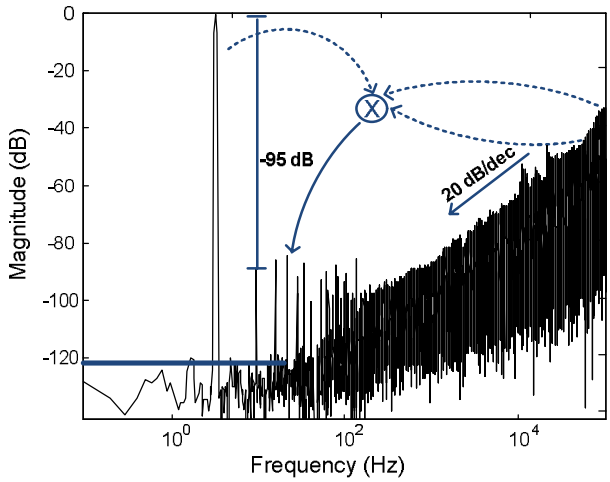


Figure 3.19 - FFT of 1st order 5-bit CTΣΔM with nonlinear transconductor at input and feedback

Figure 3.19 shows the effect of the intermodulation of quantization noise for a first order 5-bit CTΣΔM with nonlinear *Gm* stages at the input and in the feedback. The quantization noise-shaping slope of 20dB/decade is seen, as expected for a first order ΣΔM. However, the low frequency spectrum is dominated by the tones that result from intermodulation and limit the THD of the system.

It can also be shown that these low frequency intermodulation products fall on odd harmonics of the signal frequency. Recall that the output spectrum of the quantizer consists of tones at odd harmonics of input signal (equation(3.16)) and folded back harmonics (equation(3.17)). Intermodulation products of tones at these frequencies with the input frequency can be analysed to locate the frequency of resulting tones.

Consider the effect of third order distortion on the input signal along with the two odd-harmonic tones of input signal:

$$(A\sin(f_{in}) + B\sin((2N+1)f_{in}) + C\sin((2N+3)f_{in}))^3$$
$$= \underbrace{\left(\tfrac{3}{4}A^3\right)}_{\textit{Harmonic distortion term}} + \underbrace{\left(\tfrac{3}{2}AB^2 + \tfrac{3}{2}AC^2 - \tfrac{3}{2}ABC\right)}_{\textit{Intermodulation distortion terms}}\sin(f_{in}) + \underbrace{\left(-\tfrac{1}{4}A^3\right)}_{\textit{Harmonic distortion term}} + \underbrace{\tfrac{3}{2}ABC}_{\textit{Intermodulation Term at third harmonic}}\sin(3f_{in}) + \text{Other Terms} \quad (3.18)$$

where, f_{in} is input signal frequency, A is the input signal amplitude, B and C represent the amplitudes of quantization noise tones, and N is any integer.

A similar analysis can also be done for intermodulation of input frequency and two folded odd-harmonic tones:

$$(A\sin(fin) + D\sin(fs-(2K+1)fin) + E\sin(fs-(2K+3)fin))^3$$
$$= \underbrace{\left(\tfrac{3}{4}A^3 + \tfrac{3}{2}AD^2 + 3/2\,AE^2 - \tfrac{3}{2}ADE\right)\sin(fin)}_{\text{Harmonic distortion term; Intermodulation distortion terms}} + \underbrace{\left(-\tfrac{1}{4}A^3 + \tfrac{3}{2}ADE\right)\sin(3fin)}_{\text{Harmonic distortion term; Intermodulation Term at third harmonic}} + \text{Other Terms} \quad (3.19)$$

where f_{in} is input signal frequency, f_S is sampling frequency and K is an integer such that $Kf_{in} > f_S$, A is the input signal amplitude, D and E represent the amplitudes of quantization noise tones.

In each of the two cases above, the harmonic distortion terms are compensated by the input transconductor nonlinearity. However, the intermodulation terms produced by the feedback transconductor appear at the output and limit the overall linearity of the system. A more extensive calculation with more odd-harmonic tones will show intermodulation terms at other odd-harmonic frequencies as well. Intermodulation of the quantization noise tones also produces low frequency terms which contribute to a noise floor at the base band frequency, as seen in Figure 3.19.

This effect is also applicable to DC input signals and can be seen by applying cubic transfer function on the input signal with any two tones in quantization noise. The result can be expressed as:

$$(A + B\sin(\omega_{q1}t) + C\sin(\omega_{q2}t))^3$$
$$= \underbrace{A^3 + \frac{3}{2}AB^2 + \frac{3}{2}AC^2}_{\text{Harmonic distortion term; Intermodulation terms at DC}} + \underbrace{3ABC\cos(\omega_{q1}t-\omega_{q2}t) + \frac{3}{4}B^2C\sin(2\omega_{q1}t-\omega_{q2}t) + \frac{3}{4}BC^2\sin(2\omega_{q2}t-\omega_{q1}t)}_{\text{Intermodulation terms that may potentially be at low frequencies}} + \text{Other Terms} \quad (3.20)$$

where A is the DC input signal amplitude, B and C represent amplitudes of any two tones in quantization noise spectrum at frequency ω_{q1} and ω_{q2} respectively.

3.4.3.5 Verification by Simulation

The effect of intermodulation described above can be easily verified through system-level simulations. An AC signal is fed to an ΣΔM with a 5-bit quantizer and to a nonlinear element. The output bitstream of the ΣΔM is also fed to an identical nonlinear transfer function (Figure 3.20a). The difference between the two output signals is observed. Since the harmonic distortion generated by the nonlinear element would cancel out, the difference signal (*Ve*) mainly consists of intermodulation products.

In a parallel setup, a low pass filter with a cut-off frequency of $f_S/100$ is placed in between the 5-bit ΣΔM and the nonlinear element as shown in Figure 3.20b. The LPF filters out high frequency quantization noise, thereby reducing the effect of intermodulation between the signal and the quantization noise. Therefore, the intermodulation terms contained in this difference signal, *Ve'*, would be smaller.

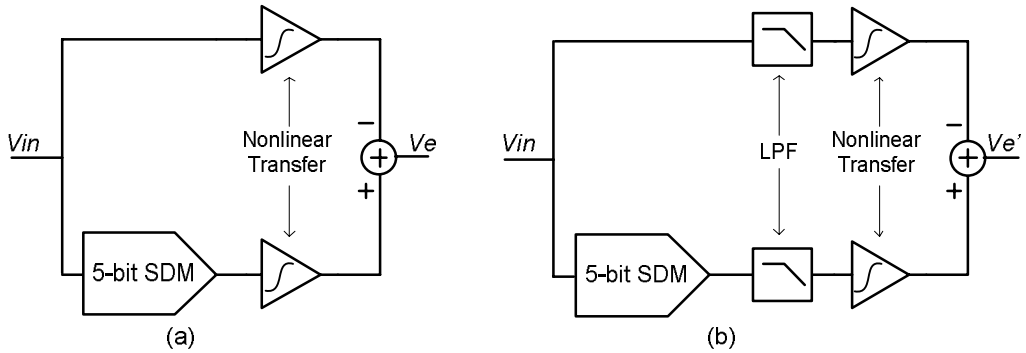


Figure 3.20 - (a) Intermodulation of quantization noise and input signal leads to error in nonlinearity cancellation; (b) quantization noise is filtered leading to better nonlinearity cancellation

The FFT plots of *Ve* and *Ve'* are shown in Figure 3.21(a) and Figure 3.21(b) respectively. As expected, the tones present at *Ve'* are significantly lower than *Ve*. The reduction in tones in *Ve'*, is a result of the filtering of the high frequency quantization noise tones before they enter the nonlinear element. This verifies the claim that the unwanted low frequency tones are created by intermodulation between the quantization noise and the input signal. With quantization noise filtered out, the noise floor is lowered by about 15dB and the third harmonic component is lowered by 30dB.

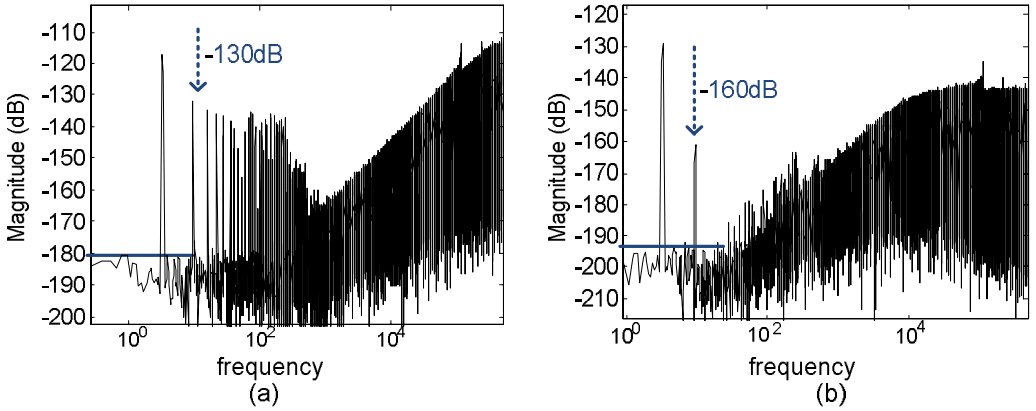


Figure 3.21 - FFT plots of outputs from two setups shown in Figure 3.20 (a) *Ve* and; (b) *Ve'*

3.4.3.6 Conclusion

The discussion in this section shows the frequency domain perspective of the effect of the input signal and the quantization noise interacting with the nonlinear transconductor in the CTΣΔM. The main conclusions that can be drawn from the foregoing analysis are summarized as follows:

1. Low frequency harmonic tones generated by the intermodulation distortion depend on the amplitude of the tones in quantization noise and not on the location of these tones.
2. Increasing the sampling frequency leads to the spreading of quantization noise in a wider band, but the amplitude of the shaped high frequency quantization noise remains unchanged. Therefore, changing the sampling frequency has little effect on the intermodulation products.
3. To improve the THD and reduce the noise floor caused by the intermodulation distortion, the amplitude of quantization noise going into the nonlinear element must be reduced.

Therefore, there are two possible solutions to this issue:

1. **Multi-bit CTΣΔM**
   A higher number of levels in a quantizer leads to weaker quantization noise tones and consequently, weaker intermodulation products. Therefore, an ΣΔM with higher number of levels in the quantizer results in lower distortion as shown in Figure 3.15.
2. **Low Pass Filter**
   An alternative to multi-bit ΣΔM is to filter the high frequency quantization noise before it goes into the nonlinear feedback *Gm* stage. An LPF placed before the *Gm* stage can help improve the THD of a single-bit CTΣΔM.

3.5 Single-bit Sigma-Delta Modulator with Filter in Feedback

As discussed in the previous section, the nonlinearity of an input *Gm* stage in a single-bit CTΣΔM cannot be compensated by the feedback *Gm* stage. A low pass filter (LPF) can convert the two-level signal from the single-bit DAC into an analog signal and reduce the high frequency quantization noise to enable the cancellation of nonlinearities in the CTΣΔM, as shown in Figure 3.22. The main idea behind the use of a filter in the feedback of a single-bit ΣΔM is that it provides a linear multi-level feedback signal in contrast to a multi-bit DAC, which can be nonlinear.

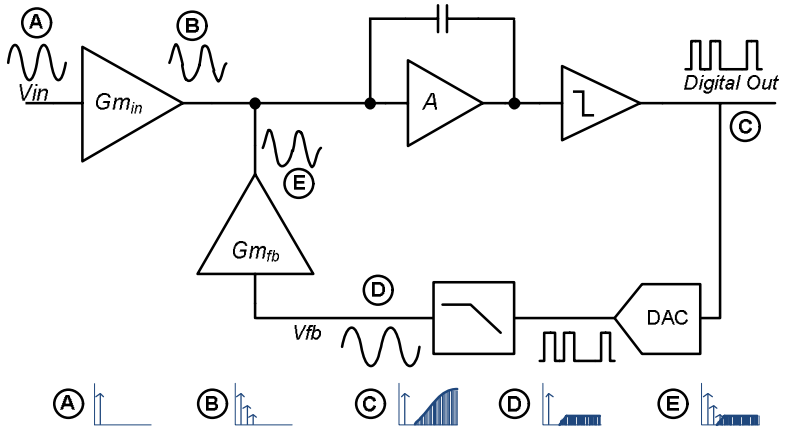


Figure 3.22 - A block diagram of CTΣΔM architecture showing a low pass reconstruction filter in feedback

The issue with using a LPF in the feedback is that it introduces a second pole in the loop that can potentially cause stability issues. In this section, the effect of the LPF on the stability and noise shaping of the ΣΔM is discussed along with the techniques to avoid these issues. Finally, the proposed technique is presented and some possible variations in the proposed architecture are explored.

3.5.1 Stability and Noise Shaping

A ΣΔM is said to be stable if the signal amplitude at all nodes is within certain bounds [25]. Due to the nonlinear dynamic nature of a ΣΔM, the loop may have stable oscillations at certain frequencies. These oscillations appear as limit cycle tones at the output of the ΣΔM. These limit cycles or stable oscillations are products of nonlinear nature of the quantizer and do not imply that the modulator is unstable. In this discussion, we analyse how the introduction of LPF in the loop

modifies the native limit cycles of the modulator and the possible issues that may occur with such addition.

Stability analysis using the linear time invariant (LTI) system theory cannot be applied directly to ΣΔM due to its nonlinear dynamic nature. The quantizer in a single-bit ΣΔM has a nonlinear gain and phase uncertainty which makes the analysis very complicated [36]. However, a linearized model of the ΣΔM gives a reasonable idea about its stability and limit cycles.

The architecture of a CTΣΔM as shown in Figure 3.22 can be modelled by assuming that the quantizer gain is κ, and a single clock cycle delay caused by DAC is included. The DAC is modelled as zero order hold with a linearly increasing phase. This linear model is presented in Figure 3.23(a) and the phase introduced by each block in the loop is specifically shown in Figure 3.23(b). The phase model is only valid for frequencies less than half the sampling frequency. However, it is sufficient for this analysis. The phase uncertainty of the quantizer is ignored in this model.

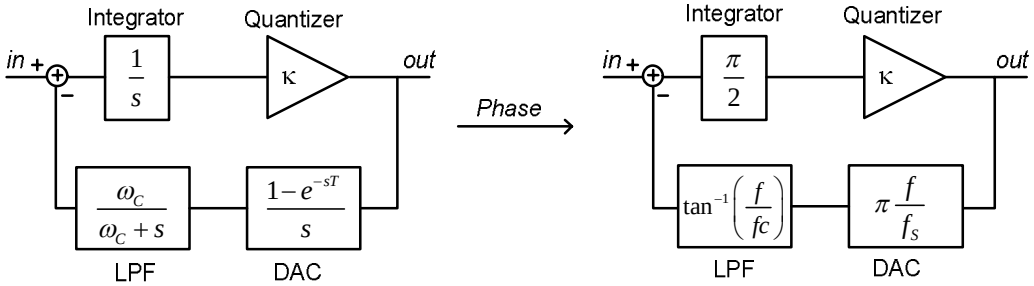


Figure 3.23 - (a) Linear model of CTΣΔM with LPF in feedback; (b) phase model of the CTΣΔM ignoring the quantizer phase uncertainty

Limit cycles are generated in an ΣΔM at frequencies where the loop gain is unity and the net phase in the loop is 2π. In a conventional first-order ΣΔM without the LPF, a limit cycle exists at $f_S/2$ as the total phase in the negative feedback loop (including the phase of DAC and integrator) equals 2π at $f_S/2$. The total phase in the loop considering the phase inversion due to negative feedback and the phase of integrator is given by:

$$LoopPhase_{SDM} = \pi + \frac{\pi}{2} + \pi \frac{f}{fs} \tag{3.21}$$

With addition of the LPF in feedback, the loop phase of the ΣΔM changes and the frequency at which the total loop phase equals 2π shifts to a lower frequency. Therefore, the limit cycle that exists at $f_S/2$ for a conventional ΣΔM must shift to a lower frequency. The location of the new limit cycle can be predicted as a function of the LPF cut-off frequency (f_{LPF}) by using the phase model shown in Figure 3.23. The total phase in the loop with LPF in feedback can be calculated to be:

$$LoopPhase_{SDM\ with\ LPF} = \pi + \frac{\pi}{2} + \pi \frac{f}{fs} + \tan^{-1} \frac{f}{f_C} \tag{3.22}$$

The zero-input limit cycle frequency can then be calculated from the following relation:

$$\tan^{-1} \frac{f_{LC}}{f_C} + \pi \frac{f_{LC}}{f_S} = \frac{\pi}{2} \tag{3.23}$$

The limit cycle of a conventional ΣΔM for zero input can be seen at $f_S/2$ in Figure 3.24(a). The introduction of an LPF in the loop introduces extra phase that shifts the zero-input limit cycle of the ΣΔM to a lower frequency as seen in Figure 3.24(b) and Figure 3.24(c). The frequency of most significant limit cycle agrees with the frequency predicted by equation (3.23).

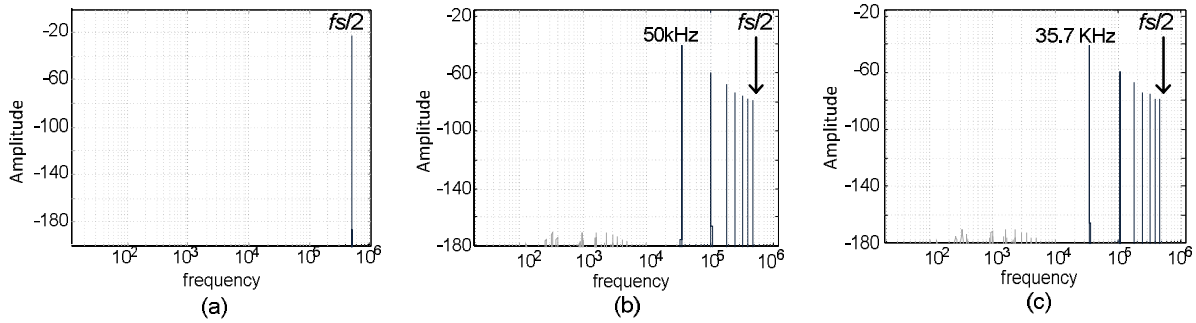


Figure 3.24 - Limit cycles for ΣΔM for zero input (Sampling Frequency of 1 MHz):
(a) no LPF (b) LPF with cut-off at 8kHz (c) LPF with cut-off at 4kHz

The total phase in the loop as a function of frequency for different values of the LPF cut-off frequency is shown in Figure 3.25. Without an LPF in the feedback, the loop phase approaches zero at $f_S/2$ frequency. However, for a ΣΔM with an LPF in the feedback path, the loop phase is zero at a lower frequency.

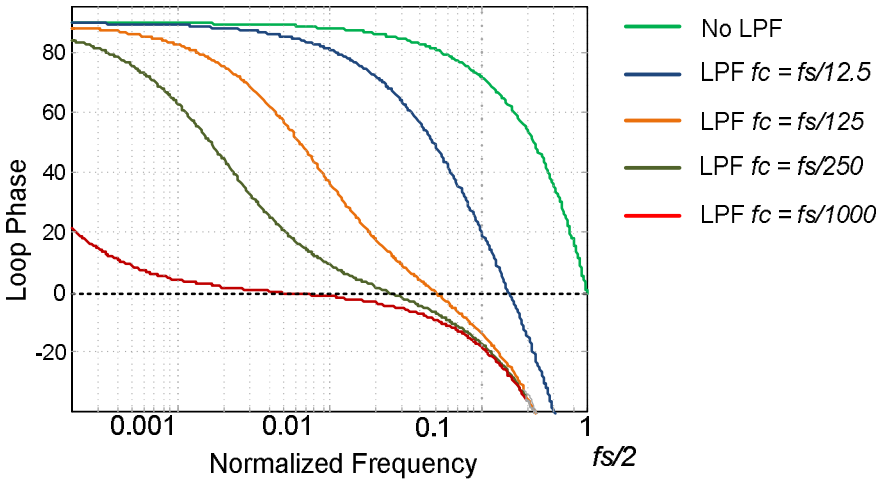


Figure 3.25 - Total loop phase for varying LPF cut-off frequency

The frequency at which loop phase becomes zero or 2π is important because of its effect on the noise shaping. The quantization noise shaping of the ΣΔM with various LPF cut-off frequencies is shown in Figure - 3.26. It can be seen that the peak frequency of the quantization noise is dependent on the cut-off frequency of the LPF.

The simulated peak frequency of quantization for different values of LPF cut-off frequency is compared with the theoretical predictions in Table 3.1. It can be seen that the location of new peak frequency of quantization noise agrees with the theoretical prediction of equation (3.23) and Figure 3.25.

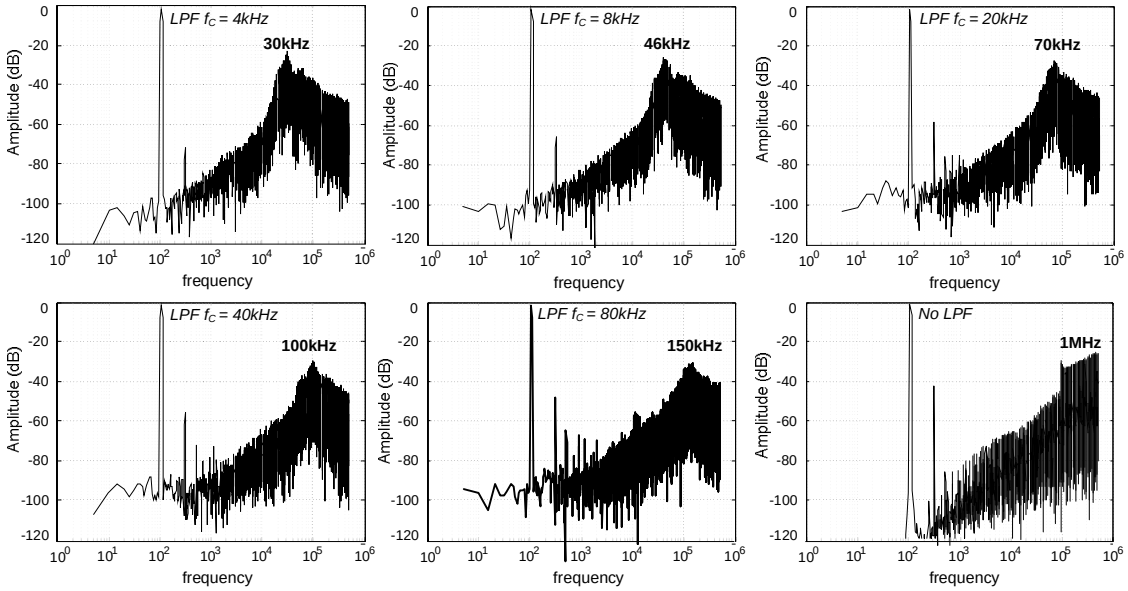


Figure - 3.26 Effect of LPF cut-off frequency on quantization noise shaping

Table 3.1 - Variation in limit cycle of ΣΔM due to the low pass filter (Sampling Frequency of 1MHz)

fc **LPF Cut-off**	***f_{LC}*** **Equation (3.23)**	***f_{peak_Qnoise}***	**LPF Suppression @Q_{noise} peak**
80 kHz	153.2 kHz	150 kHz	-6 dB
40 kHz	110 kHz	100 kHz	-8 dB
20 kHz	79 kHz	70 kHz	-10 dB
8 kHz	50.12 kHz	46 kHz	-15 dB
4 kHz	35.61 kHz	30 kHz	-17 dB

This shift in the location of the quantization noise peak leads to a problem due to reduction in the effectiveness of the LPF. As was shown in the previous section, the LPF in feedback is important for filtering the high amplitude tones of the quantization noise. However, if the quantization noise peak shifts to a lower frequency, the LPF suppression of this peak is not good enough. This leads to significant intermodulation products that limit the SNR and the THD of the system. For instance, if a first order LPF with cut-off frequency of 8kHz is chosen, the suppression of quantization noise peak at 46kHz is only about 15dB (Figure 3.27).

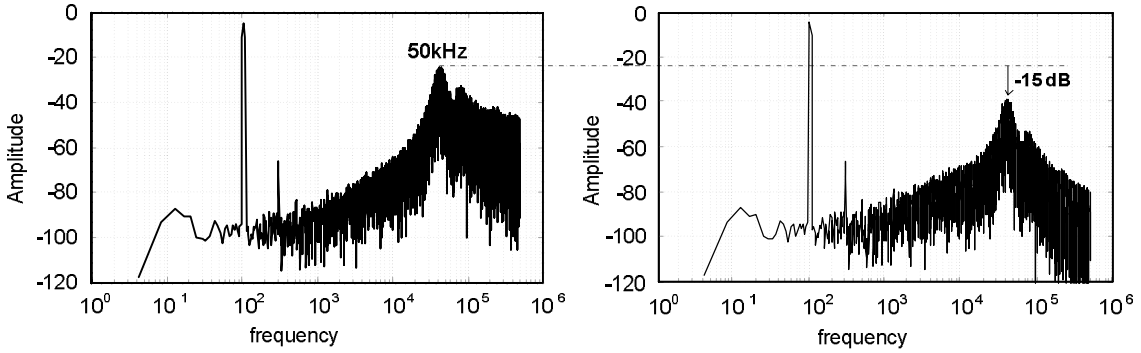


Figure 3.27 - (a) FFT of CTΣΔM output, and (b) LPF output showing suppression of quantization noise for LPF (f_C=8kHz) in feedback

The change in noise shaping due to the introduction of an LPF limits the advantage of using an LPF in the feedback path significantly. If the quantization noise shaping remains unchanged, the suppression in the amplitude of quantization noise is much better. This can lead to much smaller

intermodulation products and consequently, a higher THD. Therefore, the noise-shaping characteristic of the ΣΔM must be restored to move the peak of quantization noise closer to $f_S/2$. This can be done by introducing a zero in the loop that cancels the phase of the LPF, thereby restoring the noise shaping back to that of a conventional ΣΔM. The existing techniques to introduce this zero will be discussed in this section followed by the explanation of the proposed architecture.

3.5.2 Feedforward Unity Gain Path

The phase-shift introduced by the low pass-filter's pole can be cancelled by using a feedforward unity gain path in parallel with the LPF (Figure 3.28) [37]. This technique, however, is not the ideal solution as the high frequency quantization noise is still fed back into the nonlinear transconductor via the unity gain path. This leads to significant intermodulation products in the signal band and defeats the original purpose of employing an LPF.

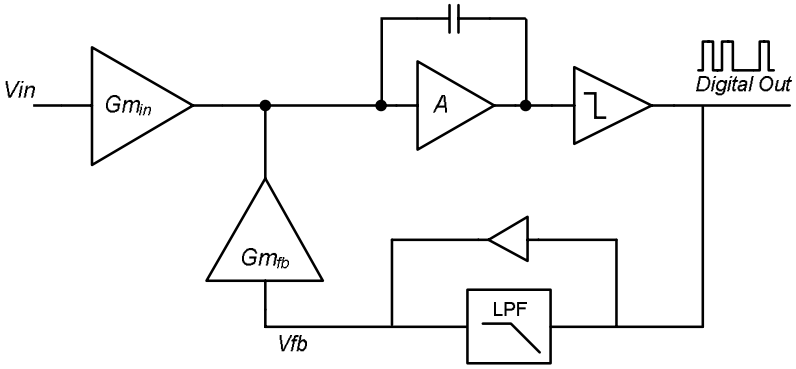


Figure 3.28 - A simple feedforward based stabilization technique

3.5.3 Using a Feedforward High Pass Path

A more sophisticated feedforward scheme for cancelling the LPF pole was proposed in [4] using separate high frequency and low frequency paths (Figure 3.29). In this architecture, the feedback *Gm* stage is placed in low frequency path, while the high-frequency signal components are fed directly to the summing node. As the high frequency path bypasses the nonlinear transconductor, no intermodulation products are generated. This leads to better compensation of the nonlinearity of the input *Gm* stage by the feedback *Gm* stage.

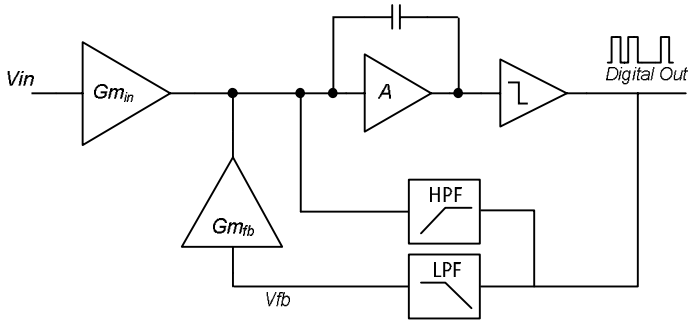


Figure 3.29 - Separate high and low frequency paths

The effect of a first-order LPF on the quantization noise of a first-order ΣΔM is shown in Figure 3.30. This simulation is done with linear input and feedback stages to highlight the effect of the first-order LPF on the quantization noise. The FFT of the ΣΔM output in Figure 3.30(a) shows the

first order noise shaping of the modulator. When this signal is passed through the LPF, it flattens the quantization noise in its stop-band as shown in the FFT of the feedback signal, *Vfb*, in Figure 3.30(b). This filtering of quantization noise leads to weaker intermodulation products between input signal and quantization noise.

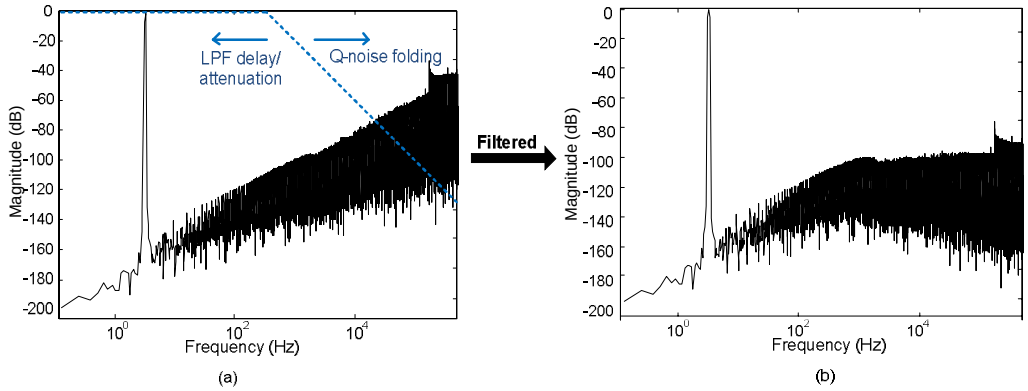


Figure 3.30 - (a) FFT plot of output of a simple first order ΣΔM with linear input and feedback stages (b) FFT plot of feedback signal with first order filtering of quantization noise as seen at *Vfb*

In a ΣΔM loop, the average value of output bitstream is identical to the input signal in amplitude and phase. The low pass filter, in the architecture shown in Figure 3.29, introduces a small phase delay and attenuation in the output signal. This implies that *Vfb* (in Figure 3.29) is a slightly delayed and attenuated version of output signal and therefore, the compensation of the nonlinearity of the input stage by the feedback *Gm* stages is not perfect, which limits the THD of the system.

The delay through the LPF can be reduced by increasing the LPF cut-off frequency; however, this comes at the cost of more quantization noise passing through the nonlinear transconductor, thereby raising the noise floor and THD due to intermodulation distortion. This trade-off, as illustrated in Figure 3.30(a), implies that the LPF cut-off frequency must be optimized to achieve the highest possible THD.

This trade-off in LPF cut-off frequency (f_{LPF}) can be mitigated by increasing the sampling frequency. As the quantization noise is spread over a wider band with a higher sampling frequency, the f_{LPF} can be increased proportionally with the sampling frequency. Increasing the f_{LPF} can help to reduce the delay and attenuation of the signal being fed back thereby improving the THD. However, increasing the sampling frequency requires that the input stage integrator handle very high frequency signals via the high pass path. Alternatively, the signal from the high frequency path could be summed at a different point which would require an additional summing node.

3.6 Proposed Architecture

The discussion so far in this chapter is summarized below:

1) A CTΣΔM with a *Gm* input stage can be used as a high-impedance, high-resolution sensor readout system
2) Compensation of the nonlinearity of the input *Gm* stage by placing a *Gm* stage with identical nonlinearity in the feedback path can result in significant improvement in the overall linearity
3) In a ΣΔM employing feedback nonlinearity compensation, intermodulation distortion products of the input signal and the quantization noise due to the feedback transconductor's nonlinearity, limit the achievable SNR and THD
4) The intermodulation products can be reduced either either by using a multi-bit quantizer and DAC in the CTΣΔM or by filtering the quantization noise before it enters the feedback transconductor
5) A CTΣΔM with single-bit DAC followed by a LPF offers several benefits over the multi-bit DAC approach in terms of design complexity, linearity, and power consumption.
6) Using a LPF in the feedback path of a conventional ΣΔM shifts in the location of the peak quantization noise as a function of f_{LPF}. This effect reduces the LPF's ability to suppress high frequency quantization noise.

In this section, a CTΣΔM architecture for direct digitization of sensor signals is proposed. It was discussed earlier that a high-resolution direct digitization of input signals can be made possible if the feedback resistor divider of the CFIA is replaced with a high-resolution ADC and DAC combination. A single-bit quantizer based ΣΔM can be used as a high-resolution ADC, if its quantization noise is filtered by a LPF. In this architecture, the integrator preceding the ΣΔM also participates in quantization noise shaping (Figure 3.31 which effectively reduces the number of high gain amplifier needed to one.

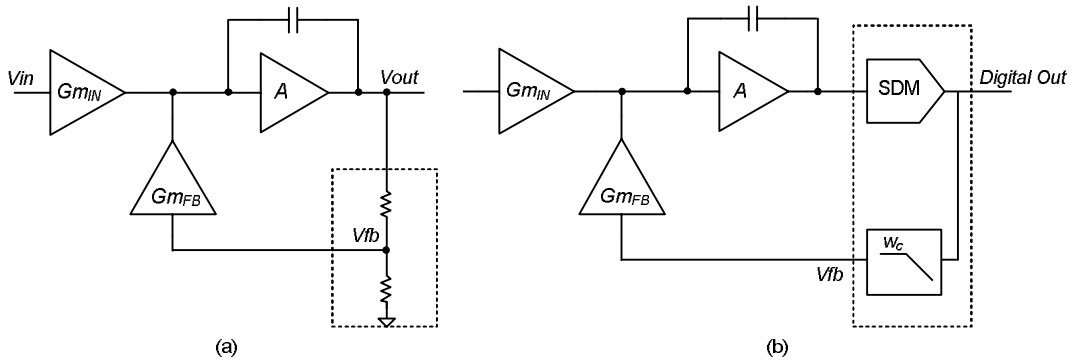


Figure 3.31 - (a) Current feedback instrumentation amplifier (b) CTΣΔM for direct digitization by replacing resistor feedback with a ΣΔM and LPF combination

3.6.1.1 Separating the Noise-Shaping and Low Pass Filtering

It was shown that the introduction of an LPF in the ΣΔM loop results in a change in the noise shaping. This happens as the LPF phase causes the loop phase to become equal to 2π at a frequency much lower than *fs*/2. In other words, the issue with the architecture of Figure 3.22 is that the quantization noise shaping as well as the filtering is done in the same loop. This issue can be resolved by separating the two processes in different loops.

In a way similar to a second order feedback based ΣΔM, a feedback path can be used to separate the LPF from the noise-shaping loop as shown in Figure 3.32. In this architecture, the shaped quantization noise is filtered by the LPF before the nonlinear feedback transconductor. The LPF phase does not influence the location of the peak of quantization noise as the high frequency quantization noise is shaped by the inner loop.

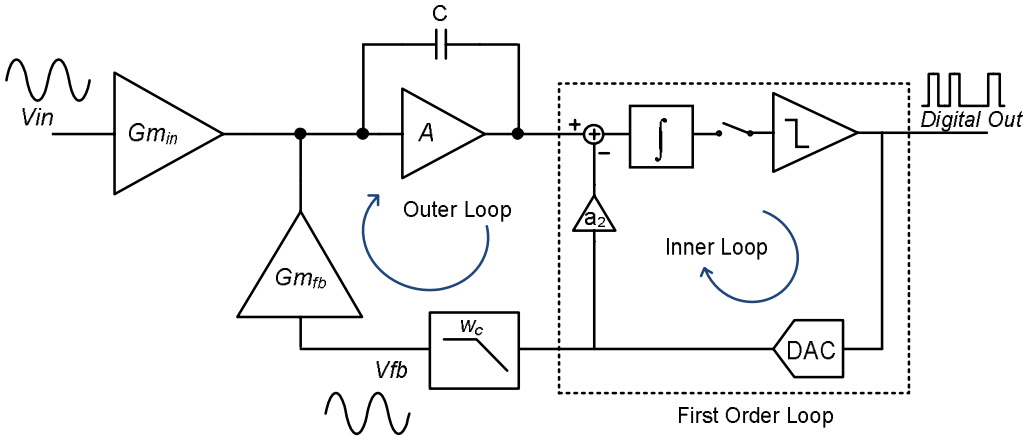


Figure 3.32 - Proposed architecture: second order feedback based ΣΔM loop with a LPF in the outer loop

3.6.1.2 THD and Stability of the System

The inner-loop in the proposed architecture is a simple ΣΔM loop. We know from the ΣΔM theory that a first order ΣΔM is perfectly stable. Moreover, the average signal transfer from input to the output of ΣΔM loop is equal to unity. The average signal transfer in the inner loop of the architecture of Figure 3.32 can be shown, on average, to equal 1/*a2*. This assumption can be used to create a linear model of this system by replacing the inner loop with a gain of *1/a2* as shown in Figure 3.33. It must be noted that this assumption is only true 'on average', and the model is not complete as it does not take into account the phase of the inner loop. However, this model facilitates a first order analysis of the linearity and the stability of the proposed system.

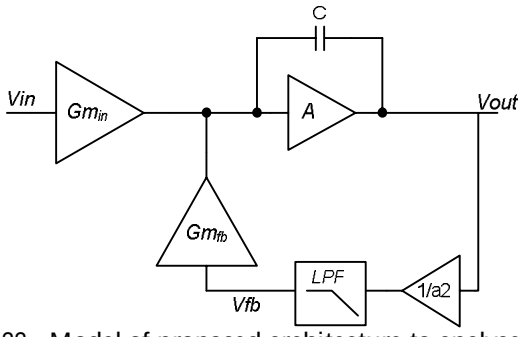


Figure 3.33 - Model of proposed architecture to analyse stability

The open-loop transfer function of the loop, shown in Figure 3.33, can be written as

$$H_{open}(s) = \frac{V_{fb}}{V_{in}} = \frac{1}{a_2}\frac{Gm_{in}}{sC}\frac{2\pi f_{LPF}}{(s+2\pi f_{LPF})} \tag{3.24}$$

where f_{LPF} is the LPF cut-off frequency, and C is the integrating capacitor.

The stability of this two-pole system depends on the relation between the unity gain bandwidth (UGBW) of the integrator and f_{LPF}. Therefore, the maximum value of the UGBW of the integrator is limited by the stability requirements. For instance, for greater than 45° phase margin in the loop with a first order LPF, it is required that $Gm/C =< 2\pi\ f_{LPF} \cdot a_2$. On the other hand, as shown in equation(3.12), the compensation of input transconductor nonlinearity by the feedback loop is dependent on the open loop gain of the integrator. Therefore, to achieve high THD, the AC gain and consequently, the UGBW of the loop must be as high as possible. Thus, the stability and the THD of the system place contrasting requirements on the unity gain frequency. This trade-off can be mitigated by use of a more complicated loop filter in the outer loop instead of a simple integrator. This is discussed in detail later in this section.

3.6.1.3 Noise Shaping and Design of Inner ΣΔM Loop

In the architecture shown in Figure 3.32, the low frequency quantization noise is second-order shaped by the two integrators in the loop. However, above f_{LPF}, quantization noise is only shaped by the inner loop. The resulting noise transfer function (NTF), as shown in Figure 3.34, has a 40dB/decade drop at low frequencies but only 20dB/decade at higher frequencies.

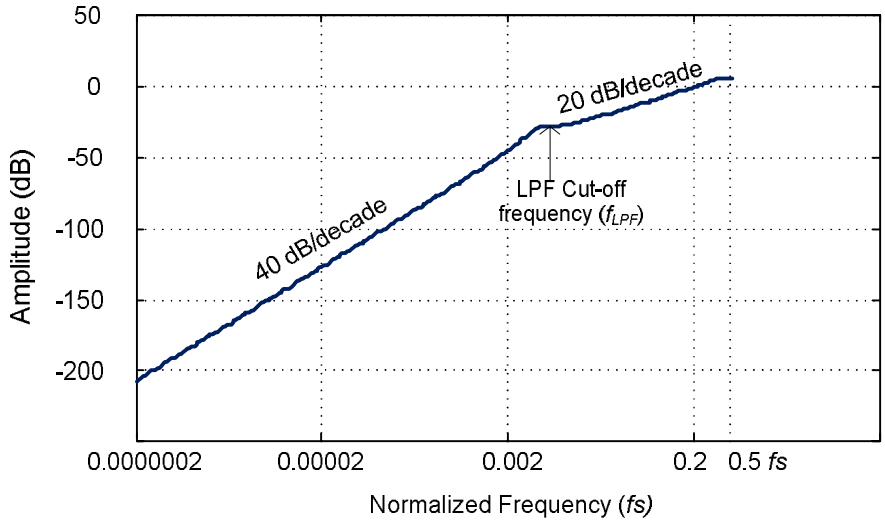


Figure 3.34 - NTF of the proposed architecture with first order ΣΔM in the inner loop

The quantization noise energy in the signal band is dependent upon f_{LPF}. The slope of the quantization noise shaping can be made steeper by use of a higher order ΣΔM in the inner loop. An inner loop built with a second-order ΣΔM is illustrated in Figure 3.35. This will result in a third order noise shaping at low frequencies and second order shaping of high frequency quantization noise. This may be desirable, if the in-band quantization noise has to be reduced or if f_{LPF} needs to be increased. However, due to steeper slope of noise shaping, a higher order LPF is needed in the feedback to filter the quantization noise. Similarly, other combinations of the order of the inner loop ΣΔM and the LPF can be explored depending on the requirements. The NTF of the CTΣΔM architecture with a second order ΣΔM in the inner loop is shown in Figure 3.36. The SNR and THD result for an example implementation with second order ΣΔM in the inner loop and is shown in Figure 3.37.

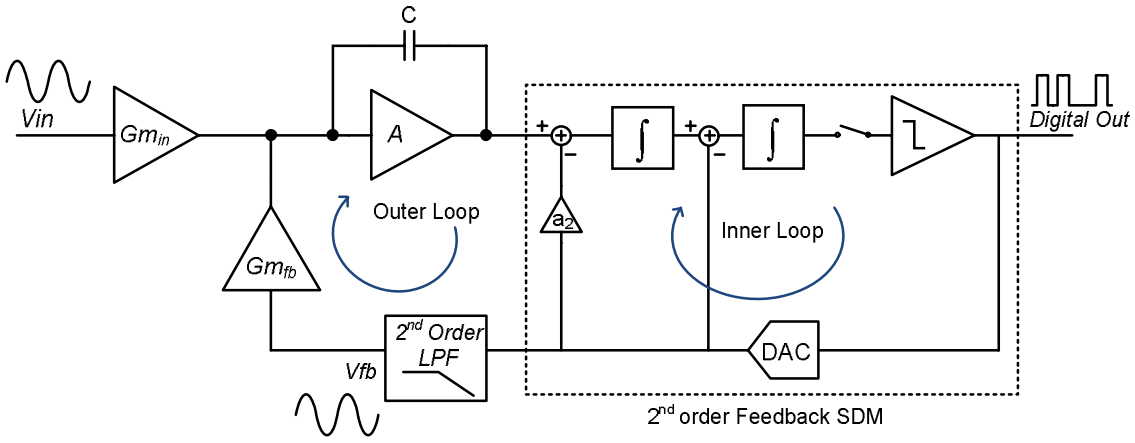


Figure 3.35 - The proposed architecture with a second-order ΣΔM in the inner loop and second-order LPF

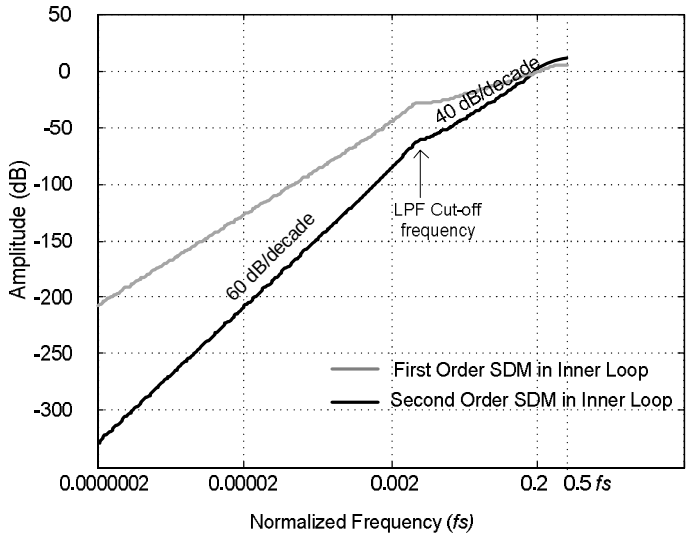


Figure 3.36 - NTF of the proposed architecture with second order ΣΔM in the inner loop

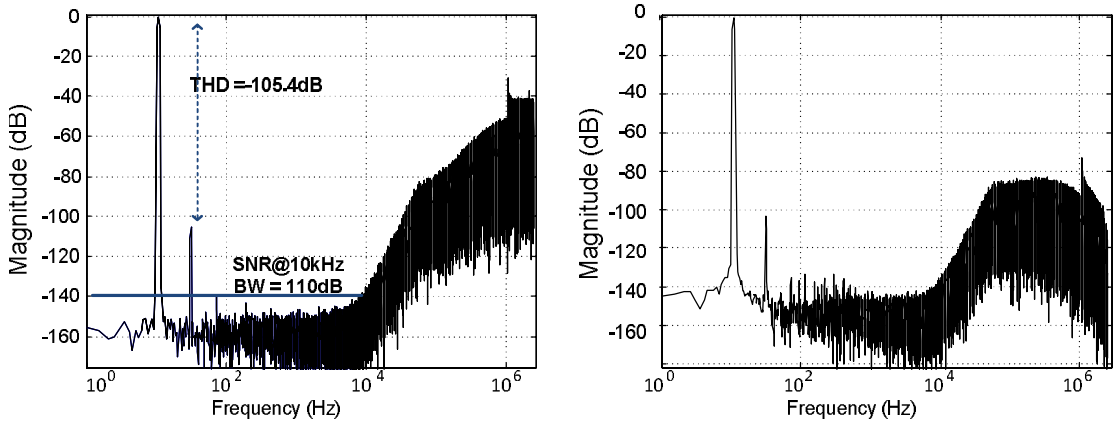


Figure 3.37 - A second order ΣΔM in the inner loop (Figure 3.35) can be used for high bandwidth applications (fs=5MHz, $\omega_{LPF}=fs/8$, $\omega_1=fs/16$, $\omega_2=fs/3$, $\omega_3=fs$)

3.6.1.4 Design of the Outer Loop

As discussed earlier, the stability requirements of the system restrict the maximum UGBW of the first integrator. As the AC loop gain and consequently, the THD of the system depends on the UGBW, the simple loop filter shown in Figure 3.32 has limited THD performance. This trade-off between stability and THD can be mitigated by a more complex design of the loop filter. For instance, a second order feedforward based loop filter can be used to increase the loop gain in the desired signal band as shown in Figure 3.38.

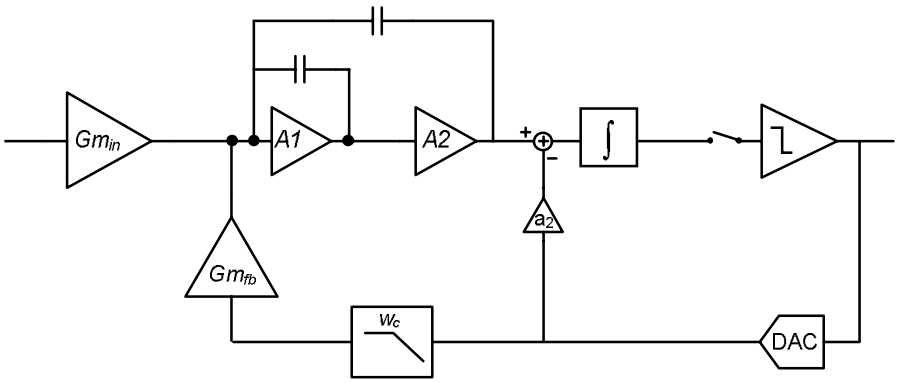


Figure 3.38 - Second order loop filter in the outer loop to achieve better THD performance

3.6.1.5 Summary of the Proposed Architecture

In this section, a CTΣΔM architecture for sensor readout systems has been proposed. It solves the issue of intermodulation of quantization noise by filtering the shaped noise through an LPF in the feedback loop. Global feedback ensures that the low frequency quantization noise is also shaped by the outer loop. The global feedback also reduces the need for more than one high-gain stages in the system.

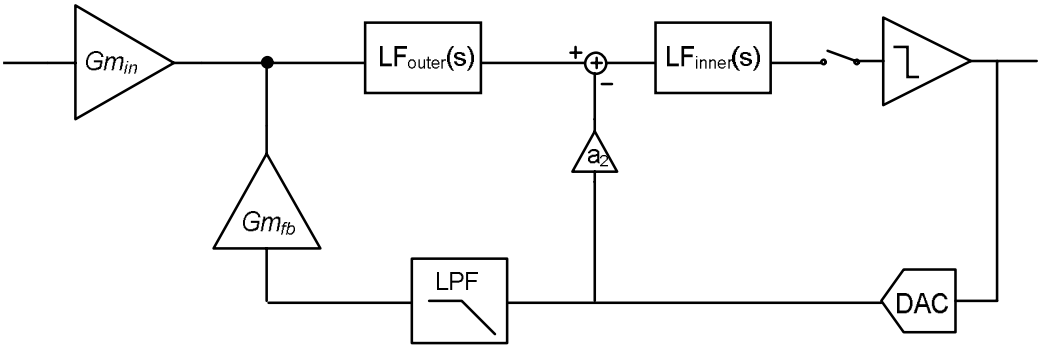


Figure 3.39 - Generic architecture of the proposed CTΣΔM

The generic architecture as shown in Figure 3.39 can be tuned to the specific needs of the target application. The target application for this work is a low frequency, high-resolution sensor readout system. Therefore, a simple integrator suffices as the loop filter of the outer loop. Further, a first order ΣΔM is used in the inner loop as high bandwidth is not desired. The detailed design of the system is presented in the next chapter.

4 System Level Design

In this chapter, the proposed CTΣΔM architecture is further analysed and the system-level design of such a modulator aimed at sensor readout application is presented. This chapter is divided into two parts. Firstly, the design of the CTΣΔM is discussed in Section 4.1, with focus on SNR, linearity and stability. Later, the application and trade-offs of using dynamic techniques such as chopping and dynamic element matching to improve offset, *1/f* noise and gain-accuracy are discussed in Section 4.2.

4.1 CTΣΔM Design for Precision Sensor Readout System

4.1.1 Overview of the System

The inner and outer loop-filters of the proposed modulator, shown in Figure 4.1, must be chosen depending upon the requirements of the application. High loop-gain is required in the outer loop to achieve low THD, while the second loop-filter design determines the noise shaping of the modulator. As the CTΣΔM in this work is designed for DC or low bandwidth applications, a first order loop filter in the outer loop is sufficient to meet the nonlinearity requirements. Moreover, as the noise bandwidth is less than 10 Hz, the noise shaping provided by a first order filter in the inner loop is sufficient for the requirements.

Figure 4.1 shows the flow of signals in the proposed CTΣΔM architecture from frequency domain perspective. A single-tone signal applied to the modulator at node A is converted by the nonlinear transconductor into a distorted current signal at node B. Assuming that the loop gain is high enough, output of the ΣΔM (at C) is a replica of the input signal along with quantization noise. This is filtered by the LPF before being fed to the feedback transconductor at E. Assuming that the input and feedback transconductors are matched and the loop gain is high enough, the distortion introduced by the nonlinear feedback transconductor at F compensate for the harmonics generated by input transconductor. This compensation of nonlinearity leads to low THD in the system.

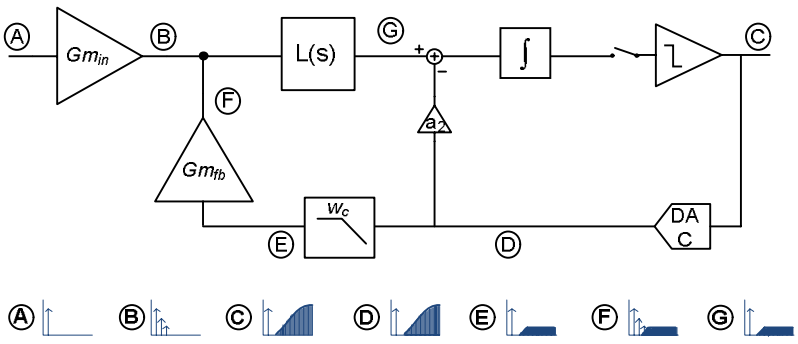


Figure 4.1 - Flow of signals in proposed architecture

The NTF of this system can be expressed as:

$$NTF(s) = \frac{s^2(s+\omega_c)}{\omega_1\omega_2\omega_c + s^2(\omega_2+\omega_c) + s^3} \tag{4.1}$$

where, ω_c is the LPF cut-off frequency in radians, ω_1 and ω_2 are unity gain frequencies of the first and the second integrators respectively.

In the pass-band of the LPF, the CTΣΔM acts like a feedback based second order modulator and therefore, quantization noise is shaped by 2nd order loop filter. Near the LPF cut-off frequency (f_{LPF}), the NTF has a set of poles and zeros, which can cause peaking. The unity gain frequency of the first integrator must be designed to be smaller than f_{LPF} for stability. However, this also leads to the first-order quantization noise shaping at frequencies higher than f_{LPF}.

In order to achieve very low THD, the compensation of nonlinearity between input and feedback transconductor needs to be perfect. In practice, this will not be the case, mainly, due to the following reasons:

a. Intermodulation distortion between the quantization noise and the input signal creates low frequency terms in the signal band. Amplitudes of the intermodulation terms depend on the amount of the quantization noise passing through the LPF, which in turn depends on f_{LPF}
b. The feedback signal at E may not be a perfect replica of input signal at A due to insufficient gain in the loop
c. The input and feedback transconductors may not be perfectly matched

In the next sections, each of these problems is considered and solved in order to achieve high resolution and linearity in the CTΣΔM.

4.1.2 SNR and Linearity

The issue of intermodulation products of the quantization noise and the input signal falling into the signal band due to the nonlinearity of the feedback transconductor was discussed in much detail in Chapter 3. To void this, the high frequency quantization noise must be suppressed by the LPF. There are two ways in which this can be achieved: (a) Reducing the f_{LPF}, (b) Increasing the order of the LPF.

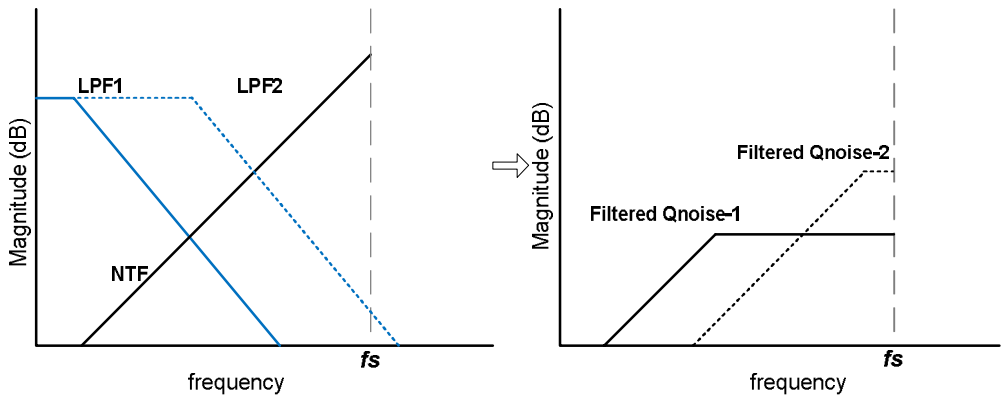


Figure 4.2 - Amplitude of filtered quantization noise depends on the LPF cut-off frequency

Low pass filtering the output of a first order ΣΔM with a first order LPF leads to a flat band of quantization noise at frequencies beyond the f_{LPF}. The amplitude of this flat band noise depends on the f_{LPF} as shown in Figure 4.2. A lower f_{LPF} value ensures that the amplitude of quantization noise passing through the filter is low. However, f_{LPF} cannot be made too low as it leads to stability issues as well as to physically large filter components.

4.1.2.1 Relation between LPF cut-off Frequency and Sampling Frequency

The large quantization noise tones near the sampling frequency are the dominant source of intermodulation products in the signal band. Increasing both the sampling frequency (f_S) and the LPF cut-off frequency proportionally ensures that the amplitude of quantization noise passing through to the nonlinear feedback transconductor remains the same (Figure 4.3). Therefore, intermodulation distortion products limiting the linearity and the signal to quantization noise ratio (SQNR) will remain the same if the ratio f_S / f_{LPF} is kept constant.

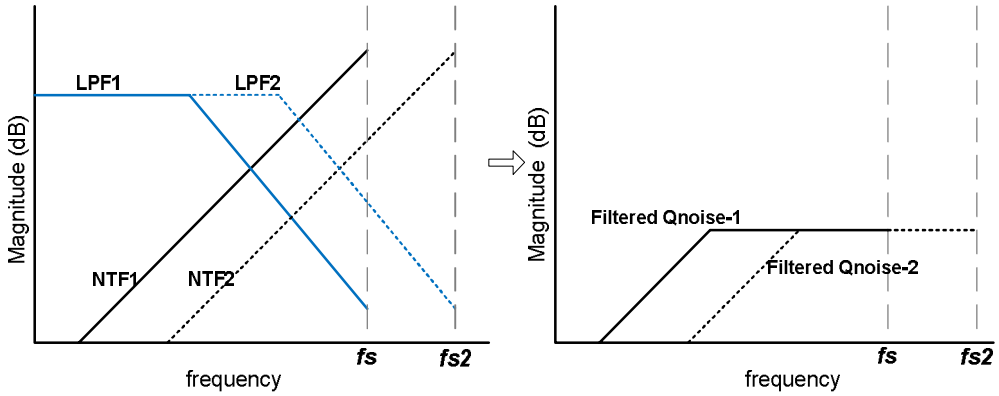


Figure 4.3 - Increasing sampling frequency and LPF cut-off frequency proportionally results in same amount of quantization noise passing through the LPF if order of the LPF is same as that of the ΣΔM

Figure 4.4 shows the simulated result of varying the f_{LPF} with constant sampling frequency and loop gain. The result shows that for very small f_S / f_{LPF} ratio, the noise floor is very high (and SQNR is low). Also, as the ratio is made larger, the noise floor drops due to better filtering of quantization noise and therefore leads to better SQNR. To achieve 20 bit resolution, the SQNR should at least be 126 dB to ensure that quantization noise does not limit the overall resolution. The simulation results shown in Figure 4.4 suggest that the f_S / f_{LPF} ratio must be greater than 90 to achieve the desired SQNR.

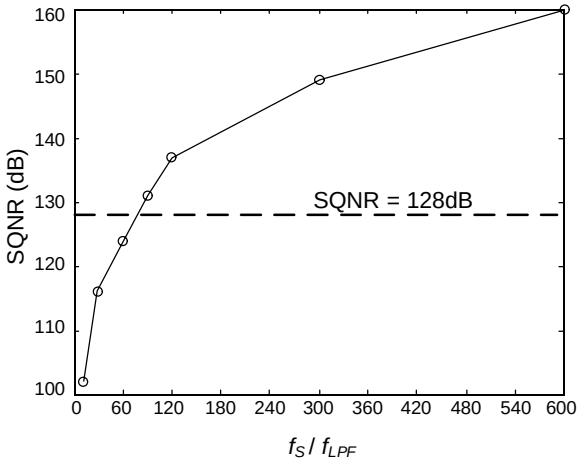


Figure 4.4 - SQNR increases with increasing the f_S / f_{LPF} ratio (fs = 1 MHz, Bandwidth = 20Hz)

It is important to note that the ratio is independent of the actual value of the sampling frequency. Therefore, there are two possible ways to achieve the desired ratio:

(a) Reducing f_{LPF} - It leads to larger component sizes for the LPF, or
(b) Increasing sampling frequency - It can potentially lead to higher power dissipation.

The component sizes for a RC low pass filter with f_S/f_{LPF} ratio of 100 with sampling frequency of 1 MHz is:

$$R_{LPF}=10k\Omega \qquad C_{LPF}=1.6nF$$

The value of resistor is taken as 10kΩ here because a large value of resistor limits the thermal noise floor of the CTΣΔM. Implementation of a 1.6nF capacitor on chip is possible but is not cost effective. Therefore, if the sampling frequency is increased, the size of the capacitor can be brought down proportionally but this will come with a penalty in terms of power dissipation. One of the strengths of the proposed architecture compared to [4] is that the input stage only sees low frequency signals as the high frequency components are filtered out. Thus, the UGB of the first integrator can be chosen to be low to ensure stability. Therefore, increasing the sampling frequency only affects the power dissipation of the quantizer which is a very small component of the total system power dissipation. Therefore, a higher sampling frequency, say 5MHz, can help to reduce the size of capacitor without significant power penalty.

4.1.2.2 DC Signal measurement accuracy

The simulation results shown in Figure 4.4 indicate that using a first order LPF is sufficient to achieve the desired SQNR. However, the aim of this work is to create a direct digitization system for sensors with near DC output signals. Therefore, it is important to consider the linearity performance of this readout architecture for DC input.

As discussed in Chapter 3, the intermodulation products of quantization noise and DC input signal can be expressed as:

$$\begin{aligned}&(a+b\sin(\omega_{q1}t)+c\sin(\omega_{q2}t))^3\\&=a^3+\frac{3}{2}ab^2+\frac{3}{2}ac^2+3abc\cos((\omega_{q1}-\omega_{q2})t)+\frac{3}{4}b^2c\sin((2\omega_{q1}-\omega_{q2})t)+\frac{3}{4}bc^2\sin((2\omega_{q2}-\omega_{q1})t)+\text{HFT}\end{aligned} \tag{4.2}$$

where, a is the input DC signal amplitude, $b\cdot\sin(\omega_{q1}t)$ and $c\cdot\sin(\omega_{q2}t)$ represent two high frequency quantization noise tones and HFT stands for high frequency terms.

The first DC term, a^3, in the above equation is a simple product of cubic nonlinearity which is perfectly compensated by the feedback loop assuming infinite DC gain. The two other DC terms, $3/2ab^2$ and $3/2ac^2$ are intermodulation products which are not compensated for by the input transconductor. These DC terms can give rise to a linear gain error at the output as they are directly proportional to the input signal, a (Figure 4.5a). However, since the quantization noise amplitudes represented by b and c are also weakly dependent on input signal amplitude, these terms can additionally create a third order nonlinear component at DC (Figure 4.5b). Some low frequency products are also shown in the equation, which contribute to the noise floor in the signal band.

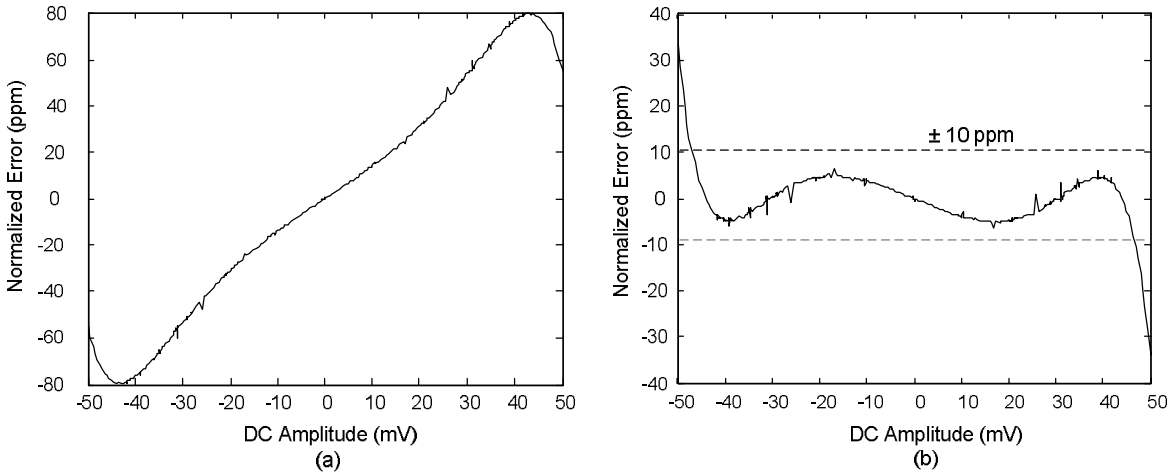


Figure 4.5 - (a) Gain error and nonlinearity in a DC signal sweep (b) Gain error corrected to highlight nonlinearities

Figure 4.5(a) shows the simulated normalized error at the output of the CTΣΔM for a DC sweep at the input. This simulation assumes perfectly matched input and feedback *Gm* stages and infinite DC gain. A systematic gain error of 80 ppm is observed due to the intermodulation of quantization noise. The gain error and third order nonlinearity are clearly visible in the plots of Figure 4.5(a) and Figure 4.5(b) respectively. The spikes seen in the error plot are caused at DC inputs that are rational fractions of reference voltage with small denominators such as:

$$\frac{1}{2}Vref, \frac{1}{3}Vref, \frac{2}{3}Vref, \frac{3}{4}Vref, \frac{3}{5}Vref, \frac{4}{5}Vref, \frac{5}{7}Vref \ldots$$

For the rational fractions of reference voltage such as these, strong limit cycles are present in the frequency spectrum as shown in Figure 4.6(b). The derivation of these limit cycles is complicated because the large amplitude tones are not fundamental to the ΣΔM but are produced only in presence of the nonlinear transconductor stages at input and feedback node. Therefore, it is sufficient to say that the limit cycles caused at the output of ΣΔM causes spikes in the INL characteristic.

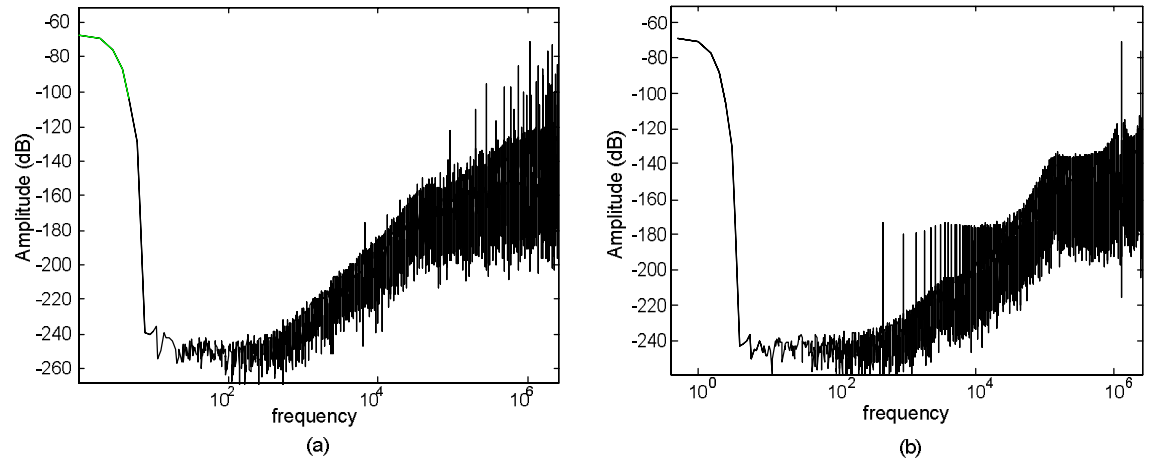


Figure 4.6 - FFT of ΣΔM output for (a) irrational DC input signal (b) DC input signal amplitude of *Vref/2*

In summary, the performance of the modulator is limited by two distinct effects:

(a) The intermodulation distortion between quantization noise and input signal. This causes gain error and third order nonlinearity as derived in equation (4.2)
(b) The low-frequency tones of quantization noise appearing for DC inputs that are rational fractions of reference voltage. The plot of normalized error shows distinguishable spikes at these input voltages.

There are two general ways to solve these problems: (a) To break the limit cycle tones using dithering and (b) Use of a higher order LPF in the feedback path for better filtering

Dithering for removal of tones

Dithering involves injecting additional noise in the system to randomize the limit cycles of ΣΔM. This results in weaker limit cycle tones at the output of ΣΔM and as a result the spikes in the spectrum disappear (Figure 4.8). In this experiment, a small white-noise dither signal is applied to the second integrator in the ΣΔM loop to analyse the effect on tones and linearity of the system. The FFT of output shows that the use of dithering completely removes the low frequency tones in the spectrum for input signal amplitude of Vref/2 (Figure 4.7). Figure 4.8 shows that the spikes in the INL seen in Figure 4.5 are significantly reduced. However, the gain error and third order nonlinearity remains same as the case without dithering. This is because gain error and nonlinearity are only created due to the intermodulation effect which is dominated by high frequency quantization noise tones. Although dithering reduces the low-frequency tones in quantization noise, the amplitude of quantization noise at high-frequencies remains unchanged. As a result, no improvement in gain error and third-order nonlinearity is seen with dithering.

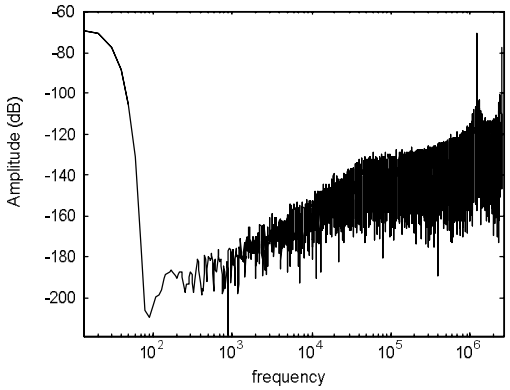


Figure 4.7 - No visible tones at DC signal of Vref/2 with dither applied

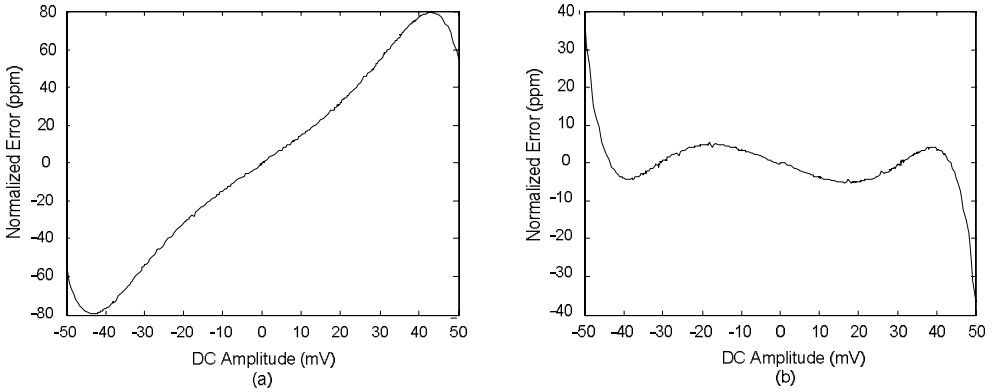


Figure 4.8 - DC input sweep with dithering and a first order LPF in feedback showing (a) Gain error and nonlinearity in a DC signal sweep (b) Gain error corrected to highlight nonlinearities

Second Order Low Pass Filter

A relatively simple solution to solve the problems of low frequency limit cycle tones and third order nonlinearity is to reduce the quantization noise going into the nonlinear feedback transconductor even further. This can be done either by reducing the cut-off frequency of the LPF or by using a second order LPF. With a second order LPF, the frequency spectrum does not show the low frequency limit cycles as shown in Figure 4.9. This also reduces the systematic gain error and third order nonlinearity from the transfer curve as shown in Figure 4.10. The spikes in the INL code are now quite small and can be neglected. The disadvantage of this approach is the additional pole introduced in the loop causes extra phase-shift and affect the loop stability.

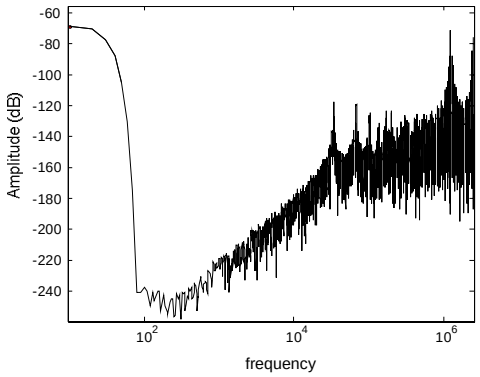


Figure 4.9 - FFT of output with Vref/2 input signal using second order LPF in feedback shows no low frequency tones

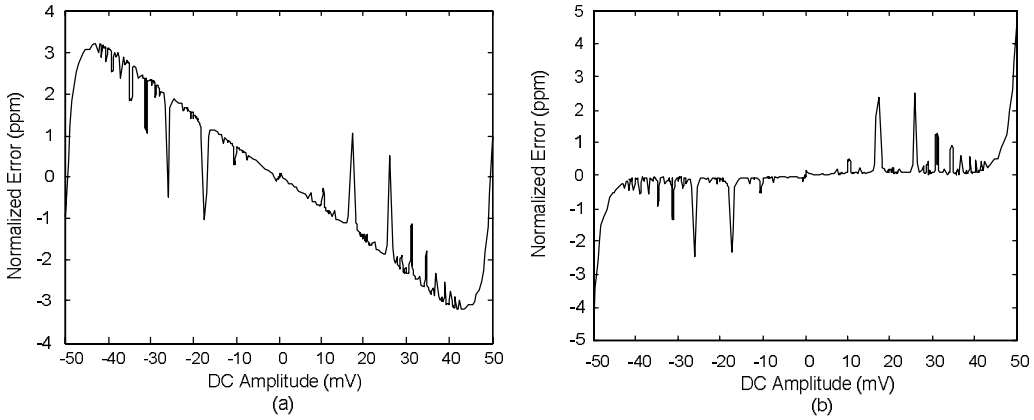


Figure 4.10 - DC input sweep with a second order LPF in feedback showing (a) Gain error and nonlinearity in a DC signal sweep (b) Gain error corrected to highlight nonlinearities

4.1.2.3 AC Signal accuracy (Harmonic Distortion)

The total harmonic distortion (THD) for an AC signal, in the proposed architecture, is limited by three factors: (a) Gain in the outer loop, (b) Intermodulation of quantization noise and (c) Mismatch between the input and the feedback transconductors. In this section, we assume perfectly matched transconductors and only the first two factors are discussed.

As an integrator is used as the loop filter, the gain in the loop drops linearly with frequency. Nonlinearity cancellation in the loop is proportional to the loop gain and, therefore, the THD of the system drops with increasing frequency (Figure 4.11). However, at very low frequencies, the THD may be worse than what is predicted by feedback theory due to intermodulation of quantization noise. This implies that for very low frequencies, THD is limited by quantization noise folding; while at higher frequencies, it is limited by the gain of the integrator. As the target

application for this work is the processing of low frequency sensor signals, the focus is on achieving very high THD at low frequencies which requires reduction in the intermodulation terms. As a second order LPF filters the quantization noise better, the intermodulation products are much smaller leading to very high THD at low frequencies as shown in Figure 4.11.

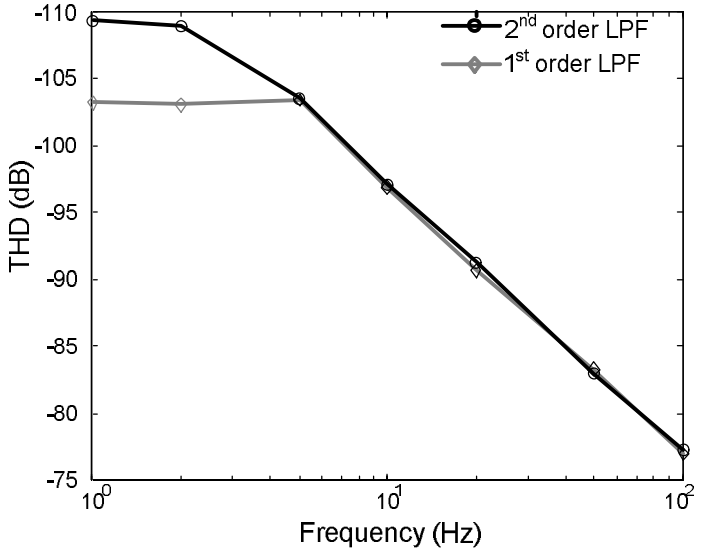


Figure 4.11 - THD vs. frequency plot for 1st order and 2nd order LPF (f_S=5 MHz, f_{LPF}=50 kHz)

4.1.2.4 Summary

The result for different filter configurations is summarized in Table 4.1. The choice of the filter is made on the basis of achievable nonlinearity and component sizes. In a real implementation, the upper bound on THD and INL may be due to mismatch between input and feedback transconductors. The state-of-art INL performance for a CFIA based readout system is ~5ppm [12]. Therefore, it is of interest to see if the proposed architecture for direct digitization can match this performance. Therefore, the filter configuration is chosen to limit the systematic nonlinearity to half of the state-of-art INL. It can also be observed that achieving the same INL or THD performance with a first order LPF requires much larger component sizes for R and C. Therefore, the use of a second order LPF is also advantageous from the component-size point of view.

Table 4.1 - Gain error and nonlinearity errors for different filter configurations (for 5 MHz sampling frequency and maximum signal amplitude of 40mV)

Filter Type	**Filter Order**	**Pole Freq f_{LPF} (kHz)**	**f_S /f_{LPF}**	**Gain Error**	**INL**	**THD (3 Hz)**
Passive RC	First	40 kHz	125	80ppm	8 ppm	-103 dB
Passive RC	First	8 kHz	625	4 ppm	1 ppm	-108.6 dB
Passive RC	First	4 kHz	1250	1 ppm	1 ppm	-109 dB
Passive RC	Second	40kHz / 40kHz	125	3 ppm	2.5 ppm	-109 dB
Passive RC	Second	20kHz / 20kHz	250	< 1 ppm	2 ppm	-109 dB

4.1.3 Stability

Stability analysis of a sigma delta modulator is often performed using a root locus method with variable gain 'κ' of the single bit quantizer. However, it is possible to get a more intuitive understanding of stability in the proposed CTΣΔM by modelled it as a LTI system. This can be done by creating a LTI black box model of the inner ΣΔM loop to simplify the analysis of system stability (Figure 4.12).

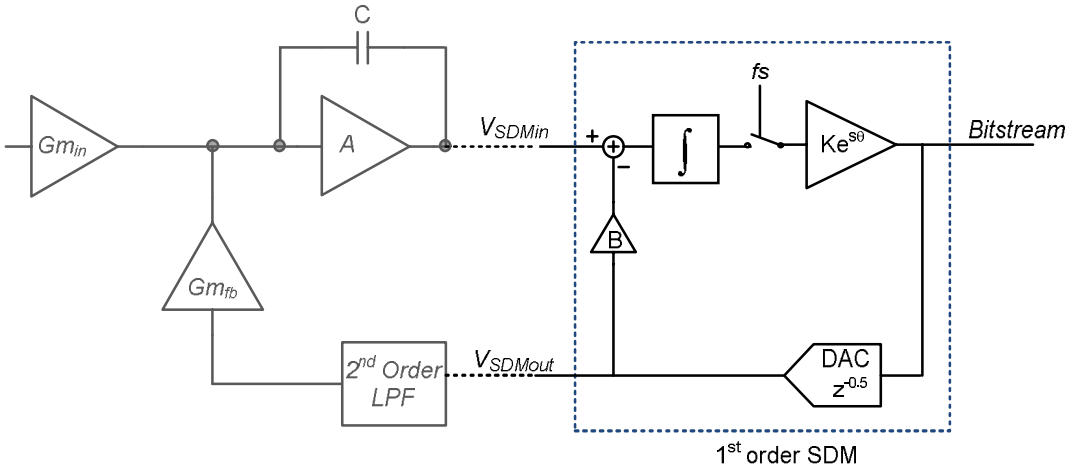


Figure 4.12 - System architecture highlighting the second loop composed of a 1st order ΣΔM

4.1.3.1 LTI Black box Model of 1st Order Sigma Delta Modulator

The closed loop transfer function for the inner loop of the CTΣΔM consisting of 1st order ΣΔM can be written as:

$$F_{closed}(s) = \frac{V_{SDMout}}{V_{SDMin}} = \frac{\frac{\kappa}{s}}{1 + B \cdot \frac{\kappa}{s} DAC(s)} \tag{4.3}$$

where, *k* is the quantizer gain, and *DAC(s)* represents the transfer function of a zero order hold block.

The feedback theory for LTI systems suggests that if the loop-gain is high enough, the net closed-loop gain and phase of the loop is determined by the feedback. This theory cannot be directly applied here due to the nonlinear quantizer gain. However, to avoid analytical analysis of this nonlinear system, the gain and phase response of the ΣΔM can be modelled as a black box. This can be done by extracting the gain and phase response of the ΣΔM over the frequency range of interest from simulations of the ΣΔM loop. A simulation of the setup is shown in Figure 4.13(a) and the simulation is done using the SIMULINK tool. Note that the closed-loop phase response is analysed at the output of DAC, which is the node that feeds the bitstream to the LPF in the outer loop as shown in Figure 4.12.

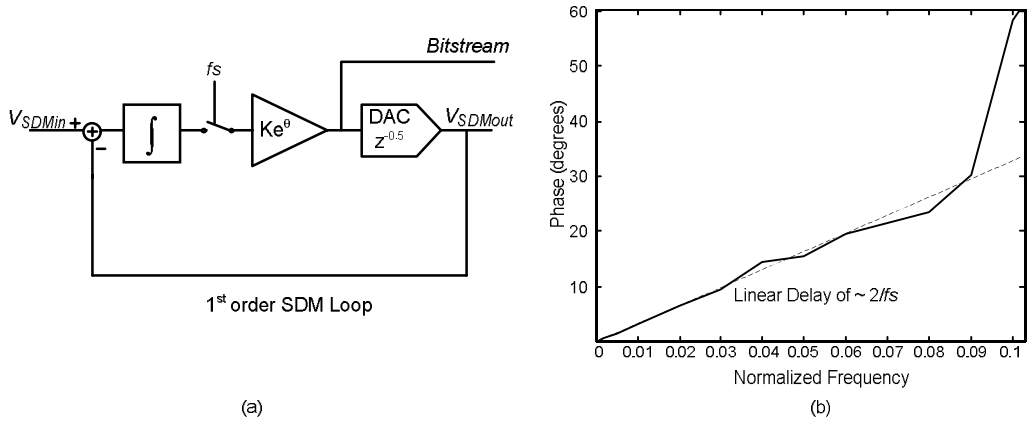


Figure 4.13 - (a) First order sigma delta modulator block (b) Phase vs. frequency response from input to output of the ΣΔM block

The CTΣΔM loop shown in Figure 4.12 tends to be unstable around the LPF pole. As the LPF pole frequency in this design is chosen to be about 100 times smaller than the sampling frequency, the frequency range of interest for this stability analysis is limited to about 0.1*fs*. It will be shown that this is indeed sufficient for the design of a stable system.

The gain response across the frequency of interest is nearly unity, but the phase response is more interesting. The phase response shows that for small input frequencies (< $0.1f_S$), the ΣΔM block introduces nearly a constant delay of 2 sampling clock cycles. This result can be used to model the ΣΔM as a delay element with a gain of unity and the model is valid for frequencies up to $0.1f_S$. Therefore, the ΣΔM block can be modelled as a simple delay:

$$SDM_{InnerLoop}(s) = e^{-s(2T_S)} \tag{4.4}$$

where $SDM_{InnerLoop}(s)$ represents the frequency response of first order ΣΔM and T_S is the sampling time.

4.1.3.2 Application of LTI Black box Model for CTΣΔM Stability Analysis

The stability analysis for the system shown in Figure 4.12 can be done by using the black box model of inner-loop ΣΔM. Figure 4.14 shows this linearized model of CTΣΔM with the inner loop ΣΔM represented as a phase delay of 2 clock cycles. A gain of *1/B* in feedback is added to model the coefficient *B* as it appears in the system shown in Figure 4.12. By using this model, the stability analysis of the loop simplifies to that of a linear third order loop with three poles and a linear phase delay of the ΣΔM.

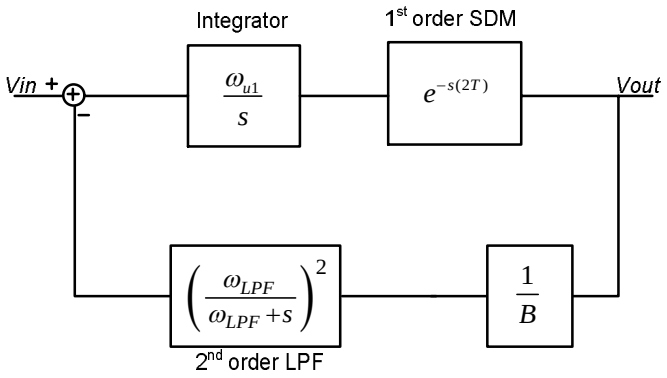


Figure 4.14 - Linear Time Invariant model of proposed ΣΔM for stability analysis

The second order LPF pole locations are decided by the SQNR and linearity requirements as discussed in Section 4.1.2. Two poles located at ω_{LPF}, contribute 90 degree phase at this frequency. Along with the integrator pole, it implies that the total phase of the loop at ω_{LPF} is greater than 180 degrees. Therefore, unity gain bandwidth of the loop must be lower than the ω_{LPF} for the linearized system to be unconditionally stable. However, a low unity gain frequency results in lower loop gain and affects the THD for AC signals. Therefore, the value for integrator unity gain frequency (ω_u) must be chosen to be as high as possible without the system being unstable.

$$H_{closed}(s) = \frac{\frac{\omega_u}{s}}{1 + B\frac{\omega_u}{s}\left(1 + \frac{\omega_{LPF}}{s}\right)^2} \tag{4.5}$$

Figure 4.15 shows the bode-plots of the system described by equation (4.5), excluding the ΣΔM block, for different values of ω_u. The feedback coefficient, *B*, is assumed to be unity for this analysis. A smaller unity gain frequency of integrator will make the system more stable but result in lower AC loop gain and therefore lead to worse THD performance. A higher unity gain frequency will lead to a smaller phase margin.

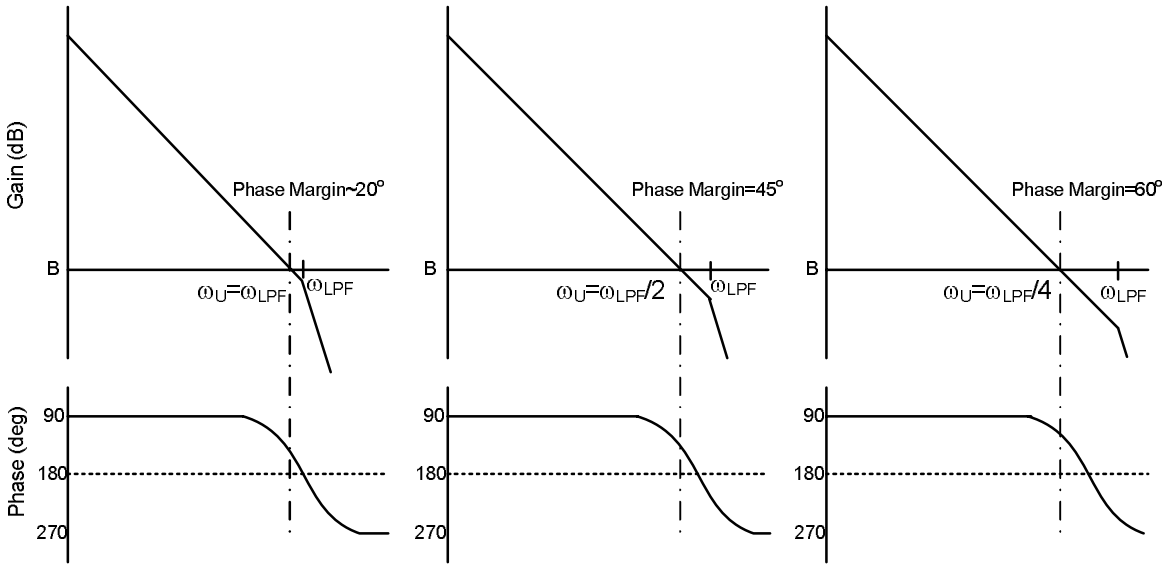


Figure 4.15 - Bode plots showing the phase margin excluding the phase of ΣΔM for different values of integrator unity gain frequency

If ω_u is placed at half of the LPF cut-off frequency, then the phase margin of the loop is 45 degrees, excluding the phase of the inner-loop ΣΔM. If we also include the phase of the ΣΔM block (~3 degrees at *f*s/200 as f_{LPF} is chosen to be *f*s/100), the net phase margin of system is about 42 degrees. This phase margin is sufficient for stability considering that effect of parasitics on the pole location will not be large owing to the large capacitor sizes for integrator and LPF (order of 100 pF).

4.1.4 Feedback Gain Coefficient

The foregoing discussion was primarily focused on the linearity and stability of the system; but another important consideration that has not yet been discussed in detail is the dimensioning of the components. In a *Gm*-C integrator, the unity gain bandwidth can be expressed as:

$$\omega_u = \frac{Gm}{C} \tag{4.6}$$

where, *Gm* is the transconductance of the transconductor and C is the integrating capacitor.

The cut-off frequency of LPF was chosen to be $\omega_{LPF} \sim f_S/20$ for quantization noise and linearity and ω_u of the first integrator is chosen as $\omega LPF/2$ for stability. This implies that for sampling frequency of 5MHz, ω_{LPF} should be 250krads/s and ω_{u1} must be about 125krads/s. This implies that for a nominal transconductance value of 0.5mS, the integrating capacitor size of 4nF is needed, which is too large for cost efficient on chip implementation. The integrating capacitor size can be reduced by introducing a feedback coefficient and increasing the unity gain frequency of integrator proportionally (as shown in Figure 4.16). This does not change the loop stability, while resulting in a lower integrating capacitor size

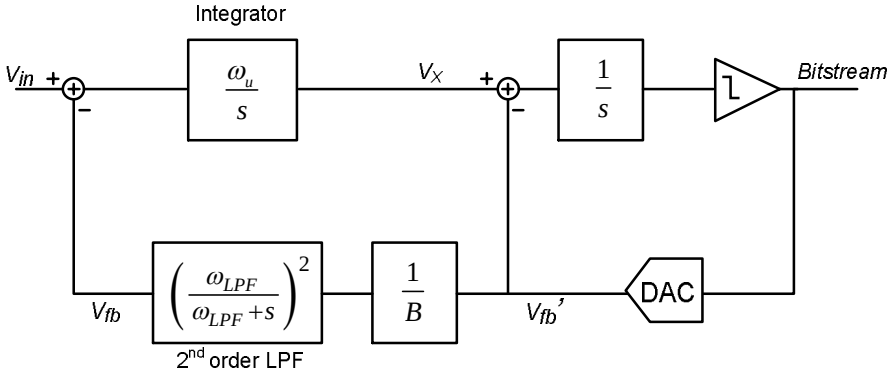


Figure 4.16 - Introducing the feedback gain coefficient in the loop

A simple feedback gain coefficient of 1/*B* in the loop can increase the unity gain frequency required for stability by *B* times and thereby, reduce size of integrating capacitor by the same ratio. A gain factor *B* of 10 is selected in this design to allow sufficiently small capacitor sizes for on-chip implementation.

4.1.5 Feedforward Path

The feedback factor helps in reducing the size of integrating capacitors, but it also leads to an increase in the output swing of first integrator by the gain factor. For a feedback coefficient of 10, this implies that the output swing is about 10 times the input signal amplitude. This increase in output swing can lead to issues in circuit level implementation. However, this can easily be avoided by employing a feedforward path. More importantly, the feedforward path also improves the linearity of the system by improving the effective closed loop gain.

4.1.5.1 Reducing Integrator Swing

In the system shown in Figure 4.16, signal V_{fb}' consists of V_{in} amplified by B and quantization noise. Assuming high gain in the second integrator, the node at V_X should also have the same

signal amplitude as V_{fb}' at low frequencies. Therefore, the amplitude of signal at node V_X can be written as:

$$V_X \simeq V_{fb}' = BV_{in} + V_Q \tag{4.7}$$

where, V_X is the output of first integrator, V_{in} is the input signal and V_Q represents quantization noise.

This implies that considering an input signal of 50 mV and a feedback factor of 10, the output of first integrator has amplitude greater than 500 mV. This large swing can cause issues in circuit level implementation of integrator and choppers and therefore needs to be reduced.

The swing at the output of first integrator can be reduced by use of a feedforward path from the input node [3]. The modified architecture including the feedforward path is shown in Figure 4.17. As the second integrator forces the difference of low frequency signals at summation node to be zero, we can write:

$$V_X' + V_{ff} \simeq V_{fb}' \tag{4.8}$$

Substituting V_{fb}' from equation (4.7), we get:

$$V_X' + V_{ff} = BV_{in} + V_Q \tag{4.9}$$

As V_{ff} is the amplitude of feedforward signal, therefore $V_{ff} = BV_{in}$. The equation can be rewritten as:

$$V_X' = V_Q \tag{4.10}$$

This implies that the output of first integrator has no signal content but only consists of quantization noise. A mismatch in the feedback and feedforward gain factors can lead to some amount of signal content coming into the integrator output. However, assuming a worst-case mismatch of 10%, the maximum signal amplitude at the output of first integrator would be in the order of 50mV which can be tolerated.

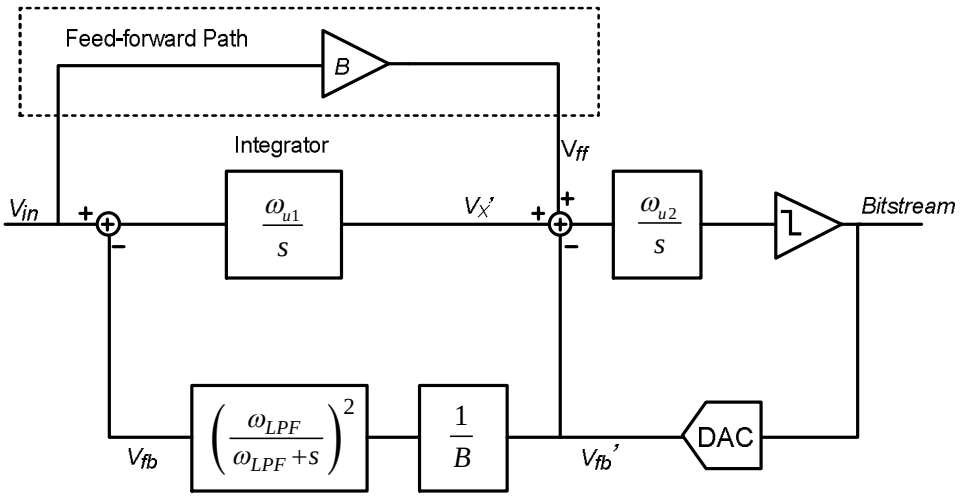


Figure 4.17 - System architecture with the feedforward path included

4.1.5.2 Improvement in Linearity with Feedforward Path

Introduction of the feedforward path has a significant impact the linearity of the system. The compensation of nonlinearity depends on the effective loop gain in the system. This is because the loop gain determines the error between signals entering the input and feedback transconductors. The feedforward path reduces this error by increasing the effective loop gain. To appreciate this, let us consider a simple close-loop amplifier structure with a feedforward path as shown in Figure 4.18.

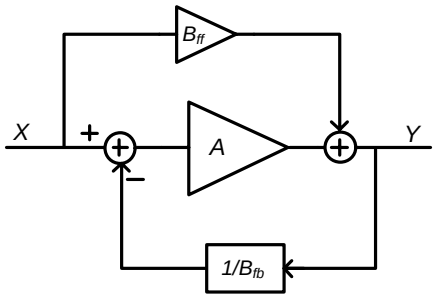


Figure 4.18 - Amplifier with input feedforward

The closed loop transfer of the loop without the feedforward path (B_{ff}=0) is expressed as:

$$Y_{no\_feedforward} = X \cdot B_{fb} \frac{A}{(A + B_{fb})} \tag{4.11}$$

where, A is the loop gain of the system and B_{fb} is the feedback gain factor.

With the feedforward path applied as shown in Figure 4.18, the relationship between input and output can be written as:

$$Y_{with\_feedforward} = A \cdot \left(X - \frac{1}{B_{fb}} Y \right) + B_{ff} \cdot X \tag{4.12}$$

which yields following relation for closed-loop transfer:

$$Y_{with\_feedforward} = X \cdot B_{fb} \frac{(A + B_{ff})}{(A + B_{fb})} \tag{4.13}$$

where, B_{ff} is the feedforward coefficient.

If B_{ff} and B_{fb} are assumed to be perfectly matched, the closed-loop gain of the amplifier has no error as shown in equation (4.13). In other words, the transfer from input to output is perfect. Therefore, the output signal is a better replica of the input signal which can lead to significant improvement in nonlinearity compensation of the CTΣΔM. It may also be noted that any nonlinearity in the feedforward path is attenuated by the open-loop gain of the amplifier and, therefore, is not significant.

However, in reality there is bound to be a mismatch between the feedback and the feedforward coefficient which places a lower bound on the error. Considering an absolute mismatch value of Δ_{ff} between B_{ff} and B_{fb}, we get the following closed loop transfer:

$$Y_{with\_feedforward} = X \cdot B \frac{A + (B + \Delta_{ff})}{A + B} \tag{4.14}$$

From this relation, it can be shown that the effective loop gain of the closed loop amplifier with feedforward path is:

$$A' \approx \frac{A}{\Delta_{ff}} \tag{4.15}$$

where Δ_{ff} is the absolute mismatch between feedback and feedforward coefficients, and A is the original gain of the amplifier.

If there is no mismatch, the effective loop gain is infinity and the effective THD is drastically improved as shown in Figure 4.19(a.2) and Figure 4.19(b.2). But, even with an absolute mismatch of 0.1 (10% for a feedback factor of 1) between the two coefficients, the effective loop gain improves by 10 times. The improvement in THD with feedforward path is illustrated in Figure 4.19. It can be seen that with 10% mismatch in the coefficients, the improvement in THD is about 20dB which can be predicted from the ten times increase in the effective loop gain.

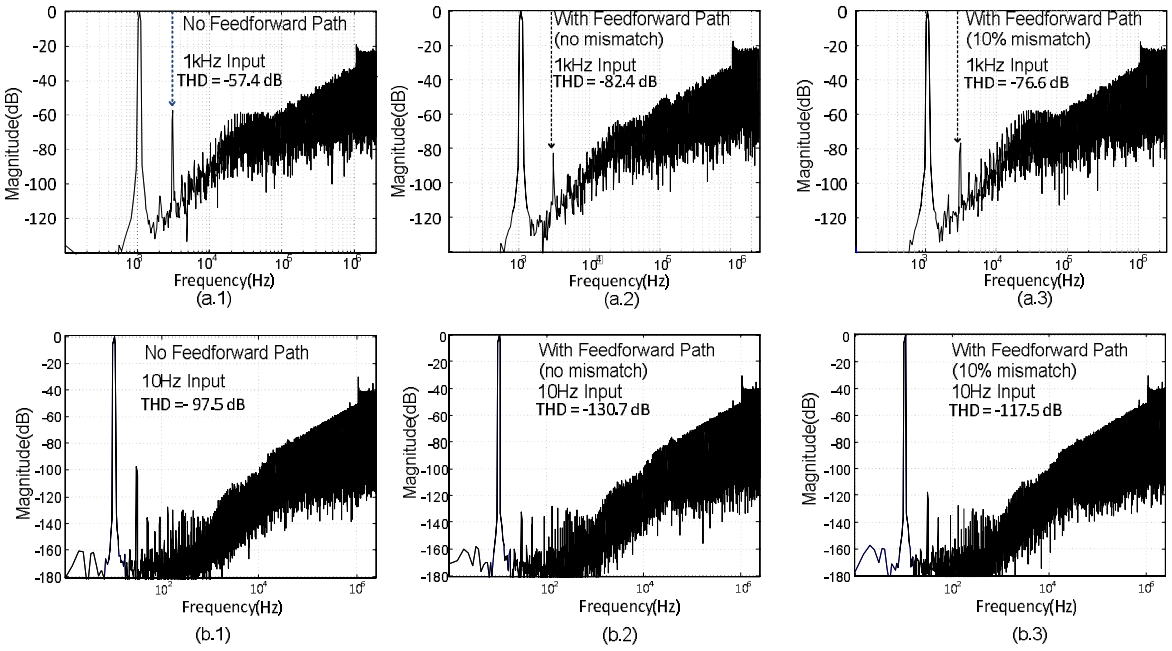


Figure 4.19 - Improvement in linearity with feedforward path for (a) 1 kHz input, (b) 10 Hz input

It must be noted that the feedforward path does not affect the actual loop gain of the system, and therefore the noise and other parameters remain nearly unchanged. Moreover, the improvement in THD depends on the absolute value of error and not the percentage mismatch. This implies that if the feedback gain factor of 10 is used, a 1% error can cause an error of 0.1 in absolute value of the coefficient. Therefore, the feedforward path is more effective in improving the nonlinearity if the feedback gain factor is smaller.

4.1.6 Effect of Non-ideal behaviour

The system analysis of the sigma delta modulator so far only involved only ideal blocks. In this section, the effect of non-ideal behaviour of the major blocks is analysed to derive the specifications for circuit level implementation.

4.1.6.1 First Integrator Gain

The DC gain of first integrator is critical for cancellation of nonlinearities between input and feedback transconductor. Gain of the first stage is also crucial for suppressing noise, nonlinearity and offset errors of succeeding stages.

The INL performance with varying DC gain of first integrator is shown in Figure 4.20, with and without the feedback path. It can be seen that with feedforward path, INL better than 5ppm can be achieved by using the feedforward path with 80dB DC gain as compared to the 100dB gain required without feedforward path.

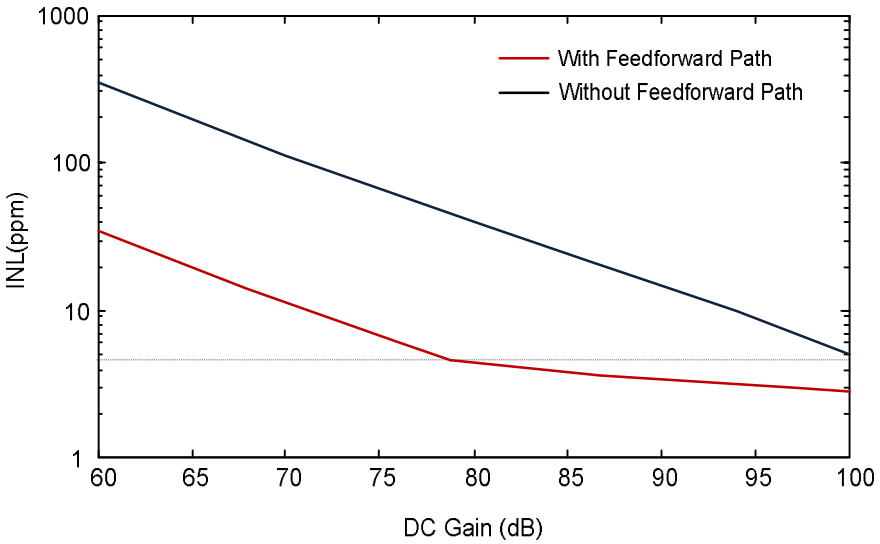


Figure 4.20 - Variation in INL with DC Gain

4.1.6.2 Mismatch in Input and Feedback Transconductors

A mismatch between the input and feedback *Gm* stages can limit the performance of the readout system in two ways: (a) gain error and (b) distortion due to imperfect cancellation of nonlinearity. The gain of this CTΣΔM is defined by:

$$Gain = B\frac{Gm_1}{Gm_{1fb}} \tag{4.16}$$

where, Gm_1 and Gm_{1fb} represent the input and feedback transconductors respectively. This mismatch may drift over time due to PVT variations creating a low frequency gain error drift component in signal band which cannot be distinguished from actual signal. A mismatch between the two transconductors also leads to unequal distortion components that are not completely compensated, thereby limiting the linearity of the system.

There are several ways to improve the matching between the two transconductors like trimming, calibration of gain error, and dynamic element matching (DEM). Use of single temperature trim does not solve the gain error drift issue and continuous calibration of gain error requires the use of a dedicated loop [30]. Dynamic element matching (DEM) is a simpler and low cost technique that reduces the average mismatch between the transconductors and can be used in conjunction with one of these techniques or independently. In this work, dynamic element matching of the input and feedback transconductors is used to average out gain and distortion coefficients. The trade-offs involved in using DEM in this architecture are discussed in Section 4.2.

4.1.6.3 Mismatch between Feedforward and Feedback Coefficients

A mismatch between the feedforward and feedback coefficients has two effects: (a) increased signal swing at the output of first integrator and (b) drop in the achievable linearity performance. Although the increase in signal swing due to mismatch is not very large. For instance, a mismatch of 10% causes the first integrator output swing to be about 40-50mV, which is tolerable. However, the drop in the linearity can significantly limit the system performance. The variation in INL with mismatch is shown in Figure 4.21. It can be seen that INL remains within 10ppm for up to 20% mismatch between feedforward and feedback coefficients (with 80dB DC gain).

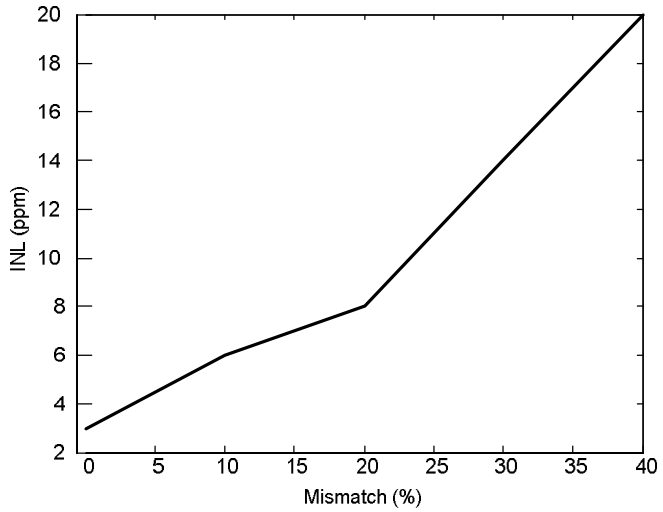


Figure 4.21 - Change in INL with mismatch between feedforward and feedback coefficients (80dB DC Gain)

4.1.6.4 Clock Jitter

Clock jitter causes the amount of reference charge being integrated to vary over different cycles and therefore manifests itself as noise at the output. Signal to noise ratio for a continuous time sigma delta ADC with a single bit quantizer can be expressed as [39]:

$$SNR_{jitter} = 10\log\left(\frac{1}{4}\frac{OSR}{\sigma_j^{\,2} f_s^{\,2}}\right) \tag{4.17}$$

The OSR in this design is very high, which helps reduce the errors due to cock jitter. If we consider a clock jitter of 100ppm on the 5MHz sampling clock, the resulting SNR_{jitter} value is equal to 128dB in a 10Hz signal band. Further, it has also been shown in past that using a filter in feedback of a ΣΔM effectively creates a multibit feedback and helps in reducing clock jitter [39-

41]. A LPF in the feedback path reduces the effect of clock jitter by decreasing the amount of charge variation due to jitter as illustrated in Figure 4.22. Therefore, clock jitter is not a critical source of error in this design.

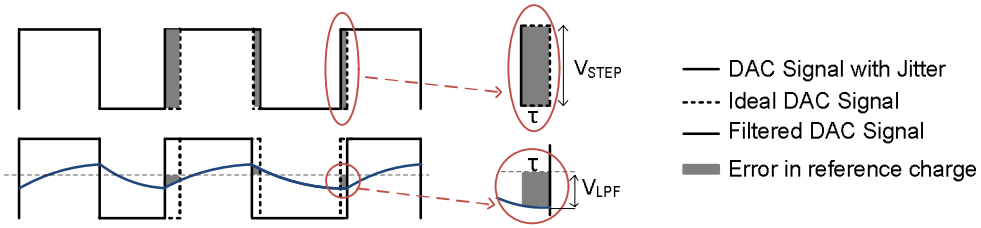


Figure 4.22 - Error in reference charge due to clock jitter bin the feedback

4.1.6.5 Asymmetric Rise and Fall of DAC Output

Finite rise and fall time of the DAC output results in nonlinearity due to inter symbol interference (ISI) in a single-bit CTΣΔM. In this design, the errors due to rise-time of DAC signal are attenuated due to LPF action. Furthermore, a return-to-zero (RZ) DAC is employed to minimize ISI errors.

4.1.6.6 Signal Dependent Comparator Delay

A quantizer usually incorporates a positive feedback loop to amplify the input signal sufficiently to give a binary output. Resolving a small input signal needs to be amplified more number of times through the positive feedback loop, thereby causing larger delay through the comparator as compared to large input signal. Therefore, the delay of a quantizer is inversely proportional to the input signal value. This input signal dependence of the quantizer delay can cause nonlinearity in the transfer function of the modulator.

To solve this issue, a synchronizer is used to ensure that the DAC output only changes at the clock edge. A simple D flip-flop (DFF) can be used as synchronizer to remove the data dependent delay as shown in Figure 4.23. In this illustration, the DFF is designed to work on the opposite edge of the clock with respect to the comparator.

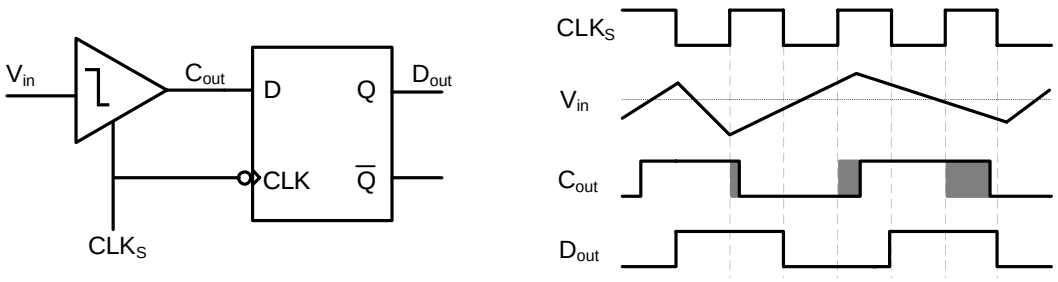


Figure 4.23 - D flip-flop used as synchronizer to remove data dependent delay

4.2 Proposed CTΣΔM with Dynamic Techniques for Precision

In a conventional sensor readout system, a high resolution ADC is preceded by a precision instrumentation amplifier which relaxes the offset, noise and linearity specifications of the ADC. However, if we wish to achieve similar performance without the instrumentation amplifier, the ADC must be designed for very low offset, 1/f noise and high linearity. The use of dynamic

techniques enables to not only reduce these errors, but also the low frequency errors caused due to offset or gain error drift.

The various known dynamic techniques used in precision systems were discussed Chapter 2. In this section, the application of these techniques in the proposed sigma delta modulator is discussed along with the trade-offs. The details of implementation of these techniques at circuit level are discussed later in Chapter 5.

4.2.1 1/*f* noise-corner and Chopping Frequency

The proposed architecture includes two gain stages in the loop both of which may need to be chopped, to achieve very low offset and 1/f noise corner. The implementation of chopper from system level is shown in Figure 4.24. The offset and noise of second integrator is reduced by the loop gain of the first stage and therefore, if the gain of first stage is high enough, the second stage of chopper may not be necessary.

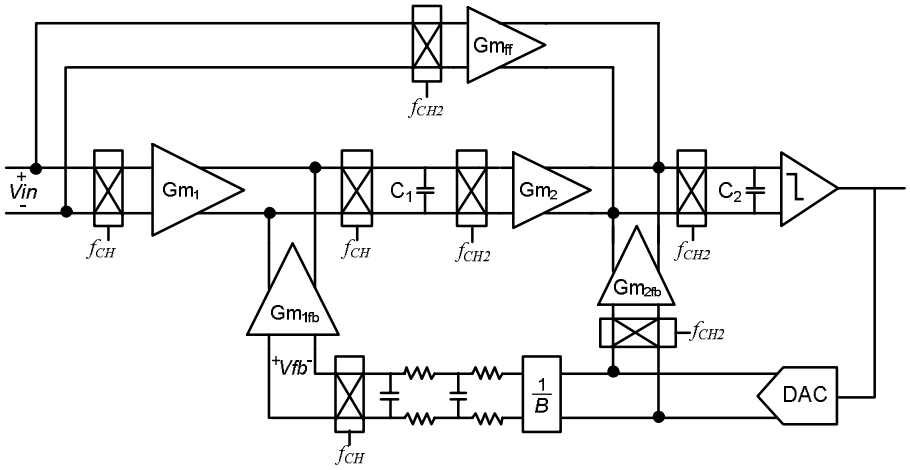


Figure 4.24 - Proposed CTΣΔM with choppers

4.2.1.1 Chopping of First Stage

The chopping of the first stage is critical to achieving low offset and 1/*f* noise as the noise of succeeding stages is suppressed by gain of the first stage. The chopping frequency must be higher than the 1/*f* noise corner frequency so that the resulting 1/*f* noise corner is at a very low frequency (sub-Hz). The choppers placed in both the input and feedback transconductor paths modulate the signal to chopping frequency. The output chopper modulates the offset and 1/f noise while demodulating the input signal back to low frequencies. The modulation of offset results in a ripple at the amplifier output with amplitude proportional to the DC offset and inversely proportional to the chopping frequency[11]:

$$V_{out,ripple} = \frac{V_{OS} \cdot \omega_{u1}}{2 f_{ch1}} \tag{4.18}$$

where, V_{OS} is the offset voltage, ω_{u1} is the unity gain frequency of the first integrator (~100krad/s) and f_{ch1} is the chopping frequency. This implies that for an offset voltage of 3mV and chopping frequency of 10 kHz, the chopper ripple amplitude is15mV.

The implementation of chopping in this CTΣΔM topology is complicated by the interaction between the chopper ripple, quantization noise and the nonlinear transconductor in the feedback path. The chopper ripple mixes with quantization noise to create intermodulation products due to the nonlinearity of the feedback transconductor. These intermodulation products result in an increase in the low frequency noise floor and poorer compensation of transconductor nonlinearity.

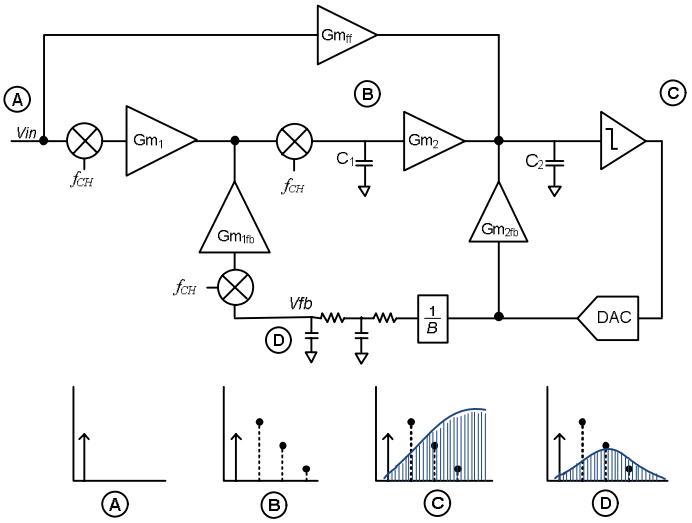


Figure 4.25 - Chopper ripple and filtered quantization noise

The mixing of quantization noise and chopper ripple takes place at the feedback transconductor and therefore, the preceding LPF filters out the high frequency quantization noise which helps reduce the intermodulation products (Figure 4.25). The filtered quantization noise rises with a slope of 40dB per decade in the pass band of the LPF and falls at 20dB/decade at frequencies higher than the cut-off frequency of the LPF as shown in Figure 4.26. The chopping frequency must be chosen such that the quantization noise at that frequency is not high. This implies that the chopping frequency must be chosen to be either much smaller or much higher than the LPF cut-off frequency (~40kHz). A lower limit on chopping frequency is set by the *1/f* noise corner of the amplifier. Moreover, a low chopping frequency will result in larger amplitude of the chopper ripple and consequently more intermodulation products. On the other hand, a higher chopping frequency will result in smaller amplitude of chopper ripple, but if the chopping frequency is increased much above the amplifier bandwidth, it would result in a drop in amplifier's effective DC gain [29]. This will lead to imperfect mismatch cancellation of the input and feedback transconductors, increasing the nonlinearity and gain error.

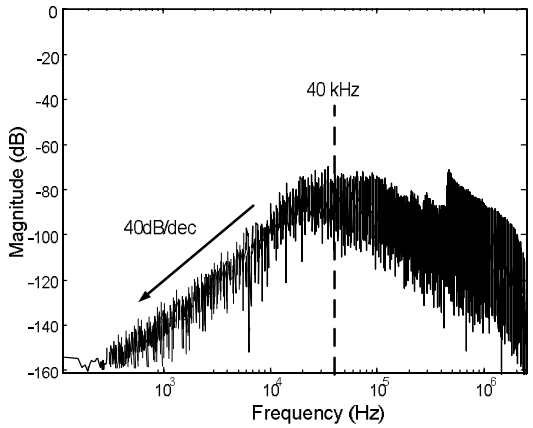


Figure 4.26 - Output of the filter in feedback showing the filtered quantization noise

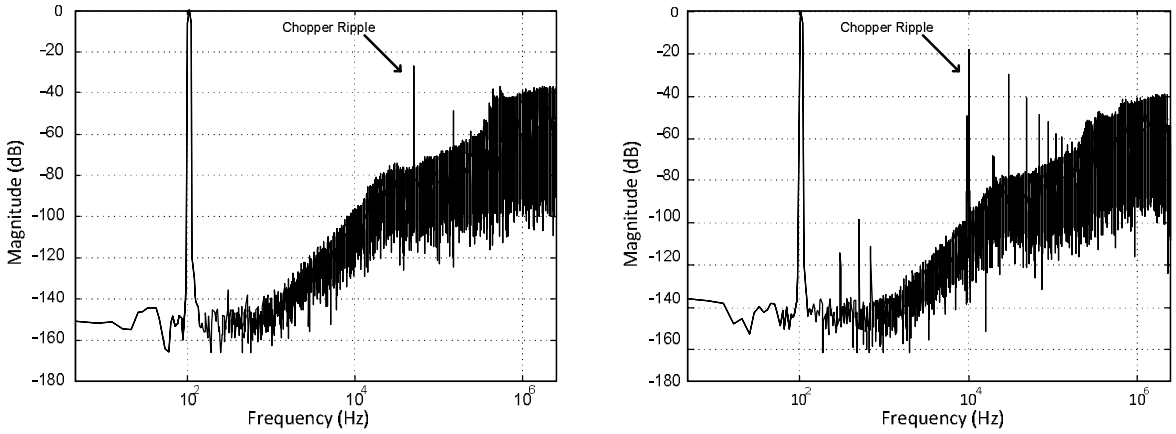


Figure 4.27 - FFT of the output of CTΣΔM with two chopper frequencies: (a) 100 kHz and (b) 10 kHz

The effect of mixing of chopper ripple with quantization noise is shown in Figure 4.27. If a chopping frequency higher than the LPF cut-off frequency is chosen, the chopper ripple amplitude is smaller and the in-band spurious tones and noise floor are also much lower. Similar effect can also be seen in DC simulations results. The effect on DC performance due to mixing of quantization noise and chopper ripple depends only on the chopper ripple frequency and the amplitude of quantization noise at that frequency. Therefore, a higher chopping frequency results in lower chopper ripple amplitude and smaller error at DC.

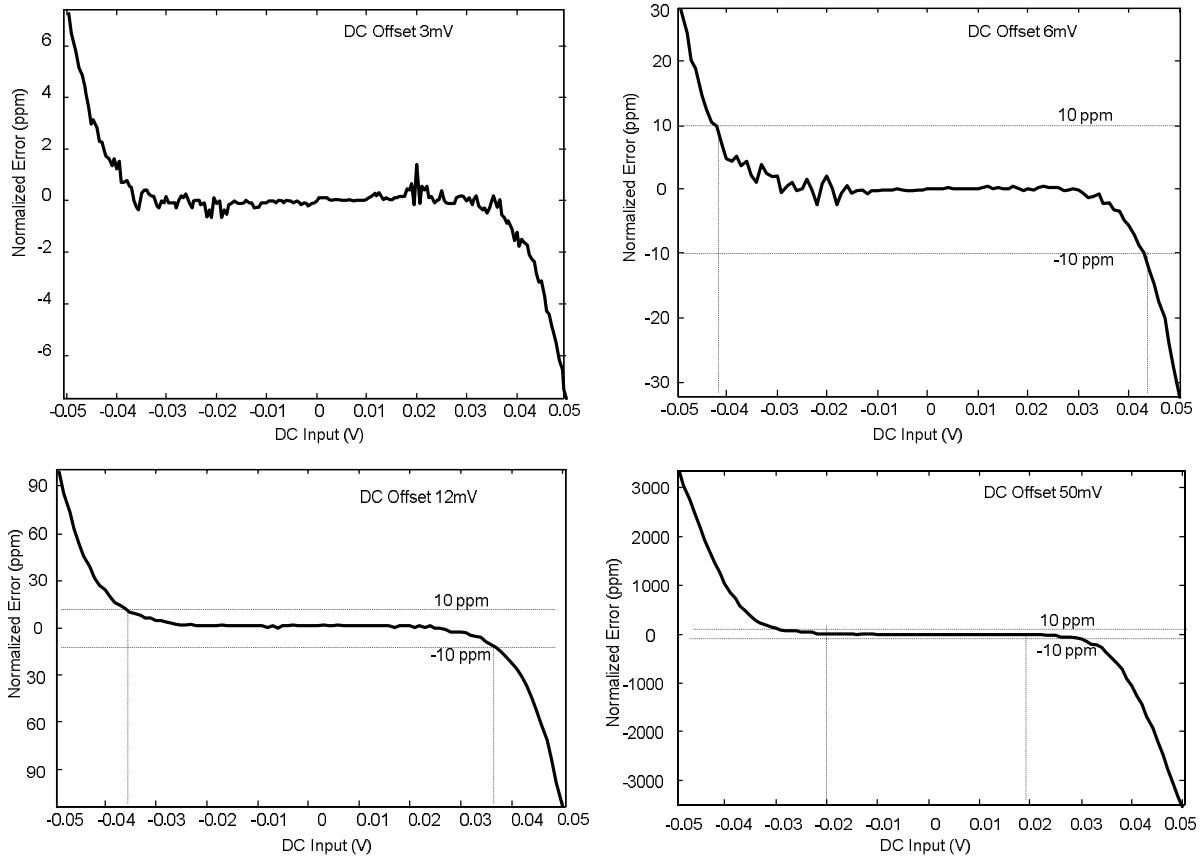


Figure 4.28 - Decreasing linear range with increasing offset due to mixing of chopper ripple with quantization noise

4.2.1.2 Chopping of Second stage and Feedforward Path

The offset and *1/f* noise of second stage are less critical, than first stage, as they are scaled down by gain of the first integrator. Nevertheless, to achieve very low offset and *1/f* noise corner, it may be necessary to apply chopping in second stage as well. The ripple caused by the second stage chopper also appears at the output and causes the same mixing effect as the first stage chopper. However, as the leakage of offset or *1/f* noise of second stage is reduced by the first stage, the chopping frequency for second stage can be chosen to be higher so that the chopper ripple amplitude is smaller.

4.2.1.3 System Level Chopping

The residual offset caused by charge-injection mismatch in chopper switches is directly proportional to the chopping frequency [11]. This residual error can be reduced by another level of low frequency chopper. System level chopping technique can be used to modulate the residual offset by chopping the entire signal chain as shown in Figure 4.29. Typically, system level chopping is done at a frequency comparable to the measurement speed. For instance using exactly two cycles of system level chopping in one measurement cycle ensures that the residual offset is completely cancelled.

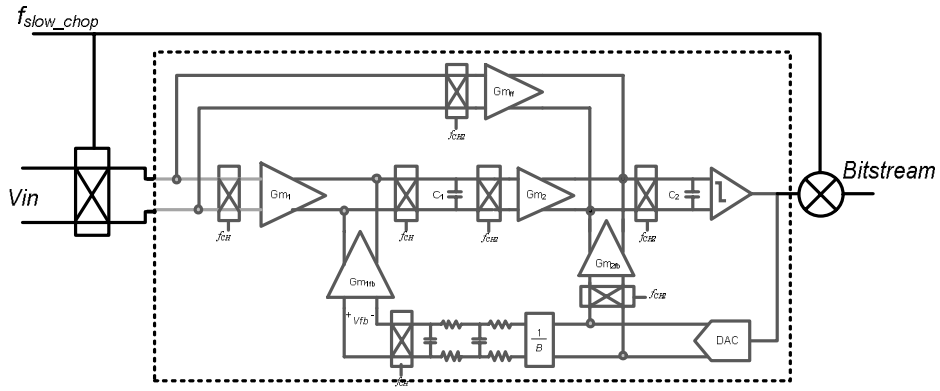


Figure 4.29 - System Level Chopping

4.2.2 Gain Error and Nonlinearity - Dynamic Element Matching (DEM)

A mismatch between input and feedback transconductors can lead to two types of errors in the proposed architecture: (a) gain error, and (b) worse nonlinearity compensation. This mismatch can be reduced by use of dynamic element matching (DEM) technique as discussed in Chapter 2.

DEM involves periodically shuffling the position of mismatched elements in order to achieve better matching 'on-average'. This technique can also be used to reduce the mismatch between the two transconductors by periodically swapping them between input and feedback positions. This results in an average value of gain which is much less impacted by the mismatch that can be expressed as:

$$Gain_{AVG} \approx 1 + \frac{\Delta^2}{2} \tag{4.19}$$

where Δ is the mismatch between Gm_1 and Gm_{1fb}. It can be seen from this relation that the gain error caused by a nominal mismatch of 1% can be reduced to about 0.005%.

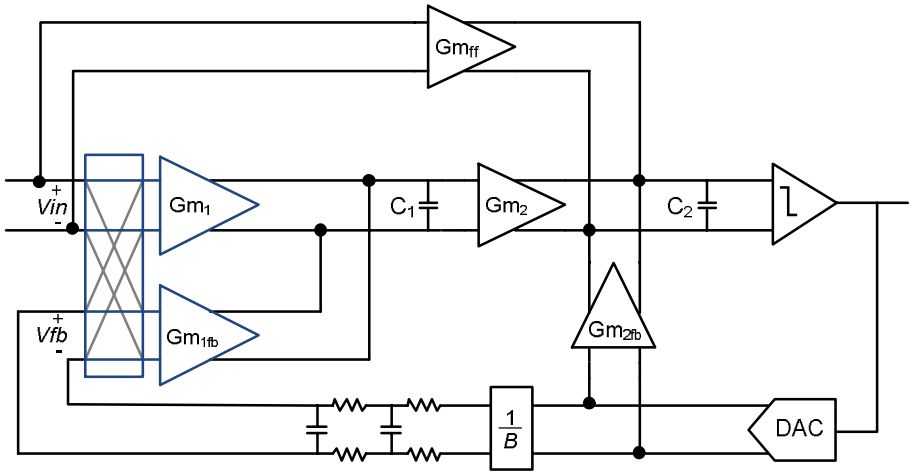


Figure 4.30 - Use of dynamic element matching for the input and feedback Gm stages

However, like chopping, DEM involves periodic shuffling of mismatched *Gm* stages. Therefore, the gain of the loop in each cycles of DEM is different. This causes a ripple at the output of the ΣΔM dependent on the mismatch between the *Gm* stages and the DEM frequency. The DEM ripple may cause intermodulation products with quantization noise resulting in a low frequency noise floor. The effect of DEM on low frequency noise floor is dependent on two factors as also shown in Table 4.2 - SQNR as a function of DEM frequency for different mismatch values from system level simulations. Higher DEM frequency results in better SQNR as the amplitude of filtered quantization-noise is smaller at a higher frequency and consequently, the intermodulation products are weaker. The system-level simulation results suggest that a DEM frequency higher than 50 kHz is required to achieve SQNR greater than 123 dB, if the mismatch between input and feedback paths is 1%.

Table 4.2 - SQNR as a function of DEM frequency for different mismatch values

f_{DEM}	**Δ=10%**	**Δ=1%**
	SQNR(20Hz)	SQNR(20Hz)
20 kHz	113 dB	119 dB
50 kHz	115 dB	123 dB
100 kHz	121 dB	133 dB
200 kHz	125 dB	135 dB

4.2.3 Ratiometric Measurement

A bridge sensor outputs a differential voltage proportional to the change in impedance of a bridge element. The sensitivity of a bridge sensor is measured in terms of *mV/V* with respect to the excitation voltage. Any variation in the excitation voltage is directly referred to the differential output of the bridge sensor. Therefore, bridge measurements are usually very sensitive to variations in the excitation signal. Ratiometric measurement technique (Figure 4.31) is a popular way for measurement of bridge sensors. The basic principle behind ratiometric measurement is that the variations in the absolute value of signals can be removed by measurement of a ratio.

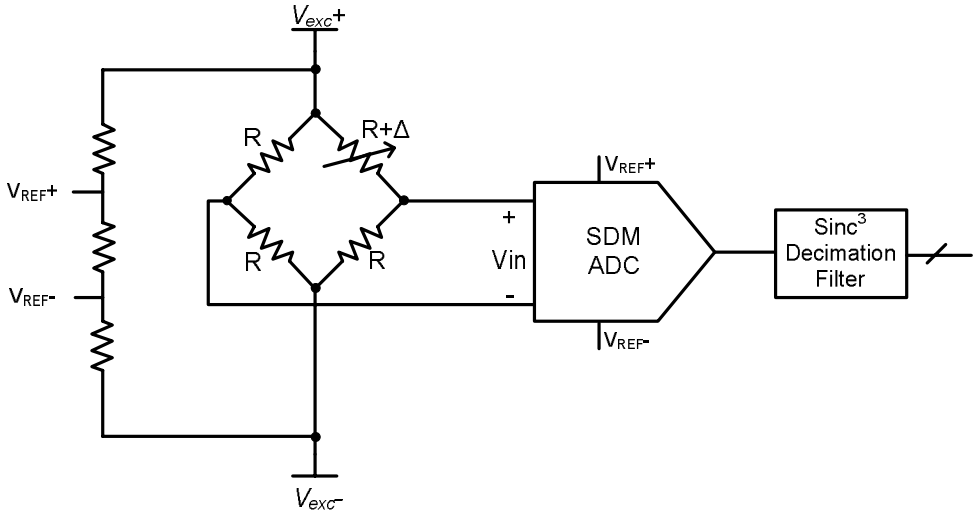


Figure 4.31 - Interfacing a bridge transducer to the proposed CTΣΔM ADC

In a ratiometric measurement system, the output of bridge transducer is measured as a ratio of differential signal and the DC excitation voltage. This can be done by using the same reference source for the bridge and the ADC. With this approach, any variation in absolute value of the bridge excitation voltage does not affect the measurement system accuracy. Figure 4.31 shows the interfacing between a bridge transducer and the proposed CTΣΔM. The reference voltage of a bridge transducer is typically a value between 1.2V and 10V. Since, the SQNR of the ΣΔM is measured as a function of its reference voltage; a large reference voltage can lead to loss of resolution. Therefore, a linear attenuation circuit is required to generate reference voltage for ΣΔM from the large bridge excitation voltage.

4.2.4 Input and Feedback Common Mode Levels

In a typical CFIA, the common mode level of the feedback transconductor is fixed and independent of the input common mode level. Although this is useful for improving CMRR, CFIA suffers from gain error and linearity issues because a difference in common mode levels effects matching of the two *Gm* stages is a source of gain error

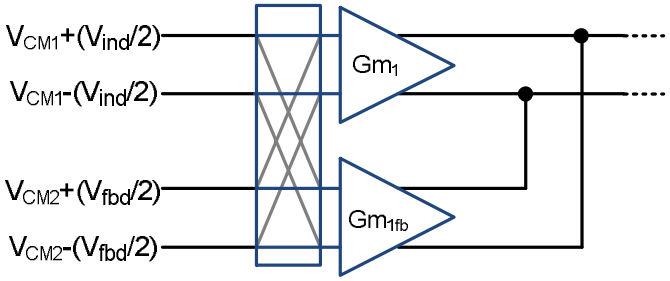


Figure 4.32 - Input and Feedback transconductors with different common mode voltages in a CFIA

Gain error caused by difference in common mode level can be modelled by including the variation in transconductance due to different common-mode levels as Δ_{CM} , therefore:

$$Gm_{1fb} = Gm_1(1+\Delta+\Delta_{CM}) \tag{4.20}$$

where Δ represents random mismatch between $Gm_1$and Gm_{fb}, and Δ_{CM} represents the mismatch between the two *Gm* stages due to different input common mode (CM) levels. When the two *Gm* stages are swapped using DEM, the resulting transfer can be expressed as [30]:

$$Gain_{avg,DEM} = \frac{\frac{Gm_1}{Gm_{1fb}}+\frac{Gm_{1fb}}{Gm_1}}{2} \simeq 1+\Delta_{CM}+\frac{\Delta^2}{2}+\frac{\Delta\cdot\Delta_{CM}}{2} \tag{4.21}$$

Although the inherent random mismatch between the two *Gm* stages is reduced by DEM, the mismatch caused by different CM levels remains the same.

The proposed architecture for direct digitization of sensor signals is also based on current feedback principle and inherits all the benefits of a CFIA. Moreover, the CM level of the feedback transconductor is not fixed and can easily be changed by changing the CM level of the reference.

For instance, in a bridge transducer system, the CM level of the bridge output is dictated by the excitation voltage. Since the reference of ΣΔM is derived from the same excitation source (as shown in Figure 4.32), it is possible to match the CM level of input and feedback transconductors. Therefore, unlike a CFIA, the same gain accuracy can be achieved irrespective of the input CM level. This is very advantageous for the gain error and linearity performance of the measurement system and greatly simplifies the system.

4.3 System Design Summary

The design choices described so far in this chapter summarized in this section.

4.3.1 High Level System Design

The overall system level architecture of proposed system is illustrated in Figure 4.33. The architecture shown in this figure is essentially a differential version of the architecture presented in Figure 4.17. The input stage features a Gm-C integrator with differentially connected capacitors which helps lower the capacitance value by a factor of 2.

The second integrator is also built with Gm-C integrators as it simplifies the design procedure. It is possible to build the second stage using an R-C integrator or a discrete time integrator. However, using RC integrator in second stage leads to drop in the DC gain of the first integrator while use of switched capacitor based integrator in second loop is as the integrating capacitor of the first stage must be isolated with a buffer before the second stage. Using a Gm-C integrator in second stage allows an easy implementation of the feedforward path, with a gain of *B*, by use of a scaled version of Gm_2.

Voltage DAC and RC low pass filter are used in the feedback to keep the implementation simple.

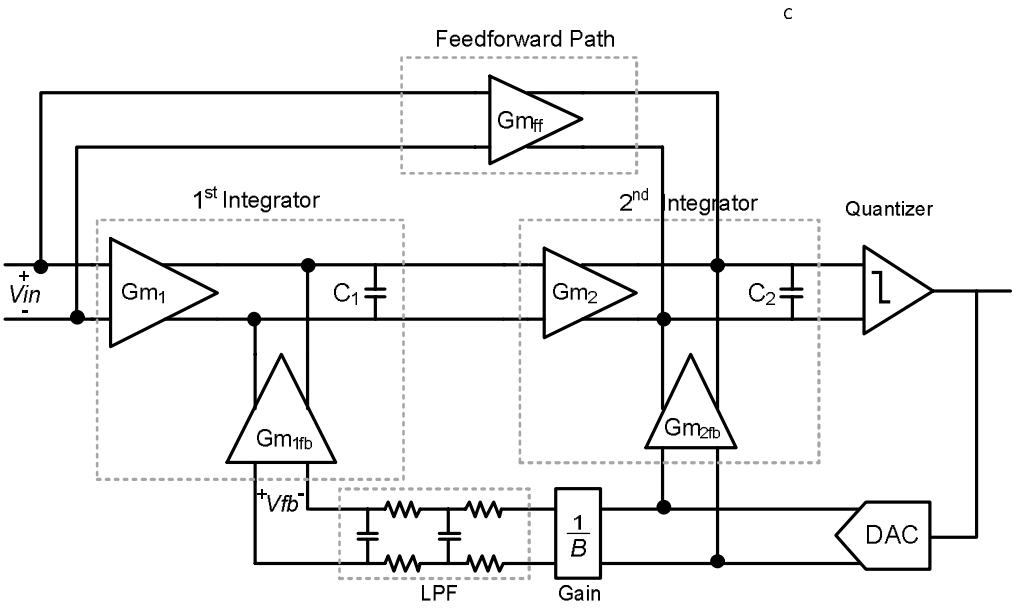


Figure 4.33 - Proposed Continuous Time Sigma Delta Modulator

4.3.2 Sampling Frequency

The various reasons contributing to the choice of the sampling frequency have been discussed earlier and are summarized here:

1. High sampling frequency allows LPF cut-off frequency and first integrator unity gain frequency to be high, thereby significantly reducing the component dimensions.
2. High unity gain frequency of first integrator also implies more gain in the outer loop which helps in THD performance for AC signals

For these reasons, the sampling frequency should be chosen to be as high as the technology can allow. In this design, the sampling frequency is chosen to be 5MHz to have small enough capacitor sizes. For a 10 Hz bandwidth, a 5MHz sampling frequency implies an OSR of 250,000. Note that such a high oversampling ratio is not required to achieve the desired SQNR performance but to limit the component dimensions. Although a higher sampling frequency could have been chosen, but this value allows the capacitors to be implemented on chip without bringing in any complication in circuit design.

4.3.3 Design of Coefficients

The design coefficients of a ΣΔM are important for loop transfer function as well as the signal swing at the output of integrators. In the architecture under consideration, the feedback LPF cut-off frequency is set by the SQNR and linearity requirements and is chosen to be:

$$\omega_{LPF} = \frac{2\pi f_S}{125} \tag{4.22}$$

For a phase margin greater than 40 degrees, the unity gain of the first integrator must be set to:

$$\omega_{u1} = \frac{\omega_{LPF}}{2} = \frac{2\pi f_S}{250} \tag{4.23}$$

The feedback coefficient of B (=10) is used to reduce the size of integrating capacitor and therefore, the unity gain bandwidth of first integrator with the feedback coefficient is:

$$\omega_{u1} = B\frac{\omega_{LPF}}{2} = B\frac{2\pi f_S}{250} \tag{4.24}$$

The second integrator unity gain bandwidth, ω_{u2}, does not affect the noise shaping or stability as it is followed by a single bit quantizer and the scaling of the integrator does not change the decision of the comparator. Therefore, ω_{u2} is only important to determine the signal swing at the input of comparator. In order to have a signal swing in the order of 10mV at the input of comparator, the following value condition must be satisfied:

$$\omega_{u2} > \frac{2\pi f_S}{50} \tag{4.25}$$

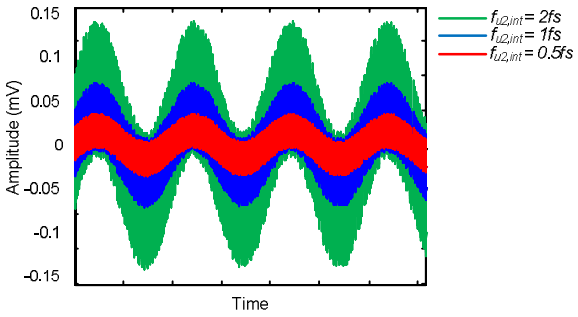


Figure 4.34 - Signal Swing at the output of second integrator

4.3.4 Loop Transfer Function

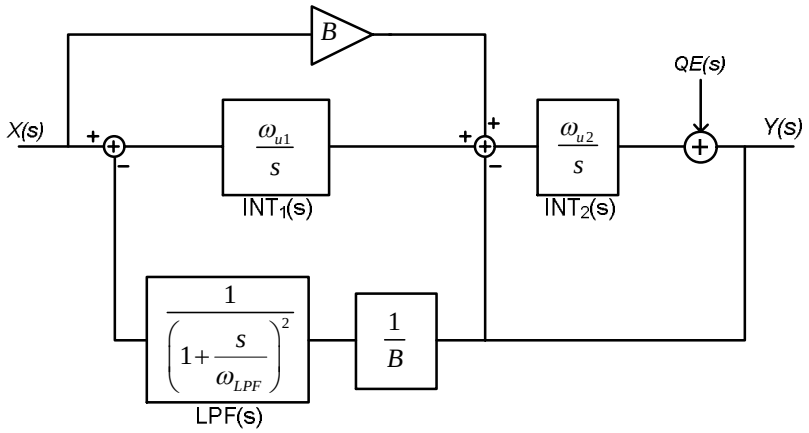


Figure 4.35 - Linear model of the proposed architecture

The loop transfer function of the proposed architecture can be derived from the linearized model of the CTΣΔM shown in Figure 4.35.

The signal transfer function of this loop can be written as:

$$STF(s) = \frac{INT_1(s)INT_2(s) + B\ INT_2(s)}{1 + LPF(s)INT_1(s)INT_2(s)/B + INT_2(s)} \tag{4.26}$$

where, $INT_1(s)$, $INT_2(s)$, $LPF(s)$ and B are as shown in Figure 4.35.

At frequencies lower than the LPF cut-off frequency, this can be approximated to:

$$STF(s)_{LOW\_FREQ} = B \tag{4.27}$$

With increasing frequency, the poles of feedback LPF and integrator create a resonator which leads to peaking at frequency near the LPF cut-off frequency. At higher frequencies, the STF has a low pass response as shown in Figure 4.36. The gain of 20 dB at low frequencies corresponds to the *B* set to a value of 10. The peaking in the STF can be reduced by improving the phase margin of the system. The chosen values of first integrator unity gain bandwidth, ω_{u1}, and LPF cut-off frequency, ω_{LPF}, give rise to ~5dB peaking in the STF. This peaking is acceptable as it is outside the signal band of the ADC and the sigma delta modulator is stable.

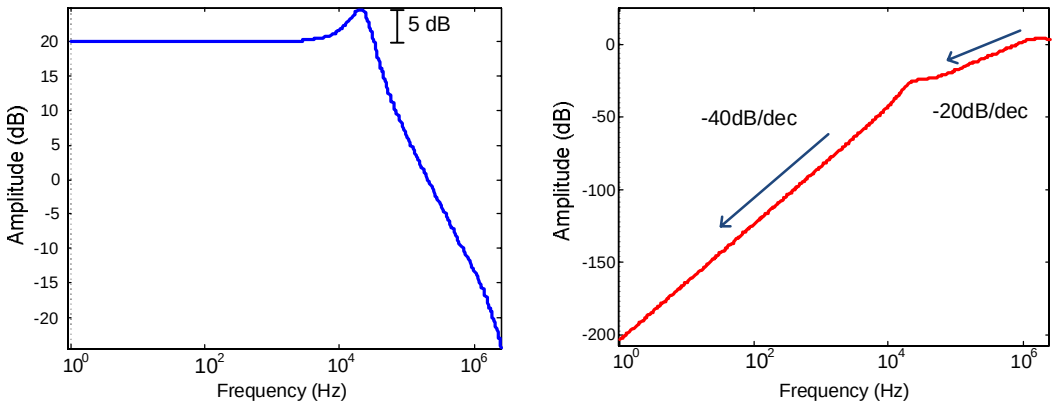


Figure 4.36 - (a) Signal Transfer Function (b) Noise Transfer Function

The noise transfer function is of greater interest because it shows how the quantization noise is shaped in the system. The NTF for the proposed architecture can be written as:

$$NTF(s) = \frac{1}{1 + LPF(s)INT_1(s)INT_2(s)/B + INT_2(s)} \tag{4.28}$$

$$NTF(s) = \frac{1}{1 + \frac{1}{B}\left(\frac{1}{1+\frac{s}{\omega_{LPF}}}\right)^2 \frac{\omega_{u1}\omega_{u2}}{s^2} + \frac{\omega_{u2}}{s}} \tag{4.29}$$

This suggests second order noise shaping at low frequencies. For $s < j\omega_{u1}/B$ the NTF can be expressed as:

$$NTF(s)|_{s<j\omega_{u1}/B} = \frac{s^2}{\omega_{u1}\omega_{u2}/B} \tag{4.30}$$

For higher frequencies, however, the NTF only shows a first order noise shaping:

$$NTF(s)|_{s>j\omega_{u1}/B} = \frac{s}{\omega_{u2}}$$

The noise transfer function, shown in Figure 4.36, has a -40 dB/decade slope at low frequencies, but only -20 dB/decade slope for frequencies above the unity gain frequency of the integrator.

4.3.5 Input Signal Range - Overload

In a conventional second order sigma delta modulator with single bit quantizer, the input range without overload is limited to roughly 0.7 times the reference voltage [25]. A signal with amplitude greater than this can cause overload condition leading to instability in a typical single-bit second-order modulator. However, the inner 1st order ΣΔM loop and LPF in this architecture together behave like a multibit quantizer and DAC and, therefore, the overload condition does not set in for signal amplitudes below the reference voltage. Therefore, the effective dynamic range of this topology is about 3 dB higher than that of a conventional feedback based second order ΣΔM.

It must be stated that the dominant overload condition in a Gm-C CT ΣΔM is caused by the saturation (or clipping) of input transconductor stage. However, the reference voltage is usually chosen to be smaller than the transconductor saturation voltage to avoid strong distortion due to saturation. Therefore, the maximum signal amplitude depends on the reference voltage which is chosen to be in the range of 50-60 mV in this design. The clipping voltage for the input stage is around 100 mV as shown in Figure 3.9

4.3.6 Requirements for Matching of Coefficients

Three key matching requirements that must be met to achieve the desired performance in this system:

(a) Offset

Offset is caused by mismatch of the transistors forming the differential pair. The system level simulations for chopping show that to achieve an INL less than 10 ppm for an input signal range of 40-50mV, the offset (before chopping) must less than 6 mV (Figure 4.28)

(b) Input/Feedback transconductor matching (Gain error)

According to the system level simulation results shown in Table 4.2, the gain error must be around 1% to enable the DEM frequency to be in the order of 20-50 kHz. Therefore, the sizing and layout of input and feedback transconductors must be performed to minimize the gain error.

(c) Feedforward Coefficient

As discussed earlier, the limitation in DC gain of the amplifier can be overcome by employing the feedforward path. However, the improvement in linearity with feedforward path is limited by the matching of feedforward and feedback coefficients. As per the simulation results shown in Figure 4.21, absolute error in the feedforward coefficient value must be less than 0.2 to achieve an INL of 10 ppm with 80 dB DC gain. For a feedforward coefficient of 10, this corresponds to a matching better than 2%.

4.3.7 Summary

The choice of various design parameters is summarized in Table 4.3.

Table 4.3 - Design Parameter Summary

Parameter	Relation	Value
Sampling Frequency	Fs	5 Mhz
LPF Cut-off Frequency	$\omega_{LPF} = 2\pi fs/125$	2π 40 kHz
Feedback Gain Factor	B	10
Unity Gain Frequency –1st Integrator	$\omega_{u1} = \omega_{LPF}/2$	2π 200 kHz
Unity Gain Frequency – 2nd Integrator	$\omega_{u2} > 2\pi fs/50$	2π 100 kHz
Feedforward Gain	$Gm_{ff} = B\ Gm_2$	10
Offset (before chopping)		< 6 mV
Gain Error (before DEM)		< 1%
Matching of Feedforward Coefficient		< 2%

5 Implementation and Results

In chapter 4, system level simulations were used to derive the specifications for the various circuit blocks of the proposed CTΣΔM-based bridge readout system. In this chapter, the circuit level implementation and layout of the design will be discussed in detail. The design was implemented in a 0.7 µm CMOS technology and the Cadence simulation results are presented here.

5.1 Overview

In this section, the architecture of the proposed CTΣΔM is reviewed from the circuit design point of view. Further, the major sources of error, the noise budget, and the matching requirements of the circuits are discussed.

5.1.1 Architecture Overview

The CTΣΔM architecture designed in this work is illustrated in Figure 5.1.Gm-C integrators are used in both the stages and a current buffer (CB) is used to sum the current from the input and the feedback Gm stages. The use of Gm-C integrators for all the stages leads to a simpler design and allows for better matching of the loop filter's coefficients. Furthermore, the use of a Gm stage in the feedforward path preserves the high input impedance of the readout system.

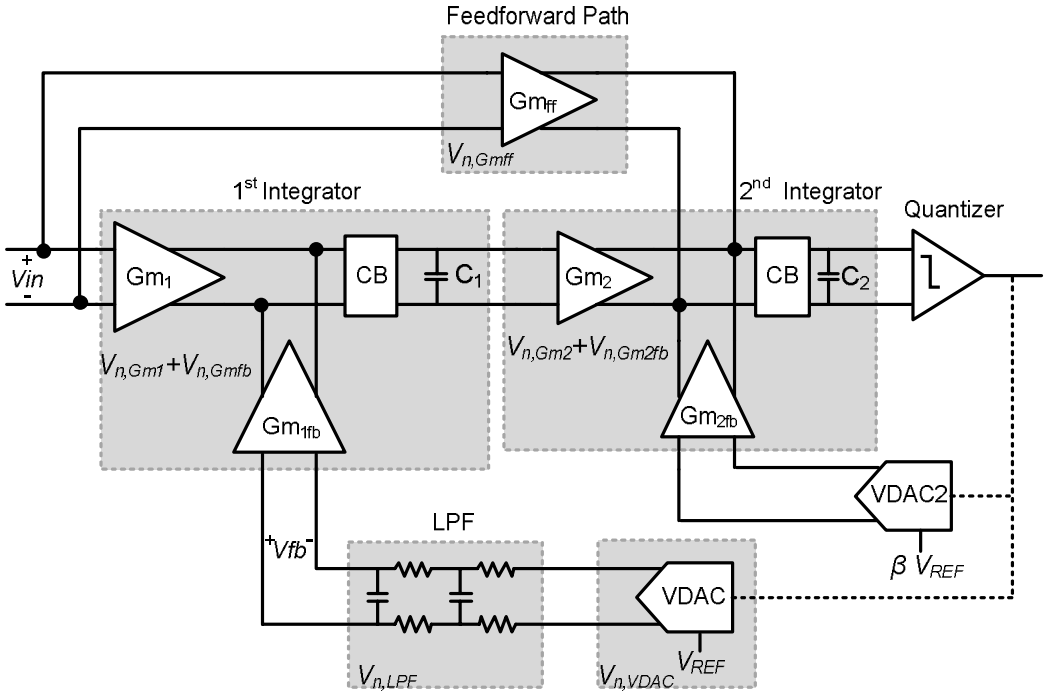


Figure 5.1 - System level architecture of the CTΣΔM

To limit the size of the on-chip capacitors, the sampling frequency is chosen to be 5 MHz. The quantized output is fed to the feedback transconductors through voltage DACs (VDAC and VDAC2). The reference voltage of the VDAC, which drives the first-stage, is chosen to be 60mV to allow a peak input signal level of 50mV with no overload. The feedback factor β can be implemented either by scaling the voltage reference of VDAC2 or by scaling the feedback transconductor Gm_{2fb}. In this implementation, the reference voltage of the VDAC2 is scaled as it is easier to create a more accurate and more tunable feedback factor using this approach. The output of the VDAC is fed to a simple second-order RC filter that filters out high frequency quantization noise. It should be noted that the noise of the RC filter adds directly to the input referred noise of the CTΣΔM. This is discussed in more detail in the following sub-section.

The specifications for each block derived from the system level simulations of Chapter 4 are summarized in Table 5.1.

Table 5.1 - Specification for circuit level implementation

Parameter	Specification
First Integrator	
DC Gain	>80dB
Unity Gain BW	200 kHz
Second Integrator	
DC Gain/ UGBW	Not critical
Input referred noise floor	22 nV/$\sqrt{Hz}$
1/f noise corner	As low as possible
Sampling Frequency	5 MHz
LPF Pole Frequency	40 kHz
V_{REF}	60 mV
Feedback Coefficient (β)	1/10
Feedforward Gain	1/β (=10)

5.1.2 Noise Budget

Assuming that the quantization noise floor is sufficiently low, achieving 20-bit resolution with 50 mV peak signal amplitude requires an input-referred thermal noise of less than 50 nV_{rms}. For a 5 Hz noise bandwidth, this corresponds to a thermal noise floor of less than 22 nV /$\sqrt{Hz}$, assuming that the 1/*f* noise corner is low enough.

The total input referred noise for the system can be expressed as:

$$V_{n,input} = V_{n,Gm1} + V_{n,Gmfb} + V_{n,LPF} + \frac{V_{n,Gm2} + V_{n,Gm2\,fb}}{G_{DC,1^{st}\,stage}} + \frac{Gm_{ff}}{Gm_2}\frac{V_{n,Gmff}}{G_{DC,1^{st}\,stage}} \tag{5.1}$$

where, $V_{n,input}$ is the input referred noise of the system, $G_{DC,1st\ stage}$ is the DC gain of the first stage, and $V_{n,Gm1}$, $V_{n,Gm1fb}$, $V_{n,Gm2}$, $V_{n,Gm2fb}$, $V_{n,Gmff}$, $V_{n,LPF}$ represent the input-referred noise of the different system blocks (refer to Figure 5.1).

Since the thermal noise of the second stage and the feedforward stage is reduced by the gain of the first stage, the system;s thermal noise will be dominated by the first stage and the feedback RC filter.

The input-referred noise of a Gm stage is inversely proportional to its transconductance value, which in turn is proportional to its tail current. Therefore, the input referred noise is inversely proportional to the power dissipation.

$$V_{n,Gm1} \approx \sqrt{\frac{4kT}{Gm_1}} \propto \sqrt{\frac{4kT}{I_{D1}}} \tag{5.2}$$

where, Gm_1 is transconductance of the input stage and I_{D1} is the tail-current source of the input differential pair.

On the other hand, the noise density at the output of an RC low pass filter is proportional to the square root of its total resistance within the signal band. Therefore, the value of the resistance used in the filter must be minimized to achieve a low noise floor. However, the filter's target cut-off frequency is around 40 kHz and therefore, the required RC product is relatively large. If a small resistor value is used to achieve low thermal noise, the size of the capacitor increases proportionally which in turn leads to larger area. This leads to a trade-off between noise and area as shown by following equation:

$$V_{n,LPF} = \sqrt{4kTR} = \sqrt{\frac{4kT\omega_{LPF}}{C_{avg} \cdot A_{cap}}} \tag{5.3}$$

where, ω_{LPF} is the cut-off frequency of the LPF in rads/sec, C_{avg} is the average capacitance per unit area and Acap is the area of the capacitor.

Equations (5.2) and (5.3) clearly show a trade-off between area and power dissipation as both the first Gm stage and the RC-filter contribute to the total input referred noise. As a compromise, the noise budget of the system is distributed equally between the input Gm-stage and the RC-filter:

$$V_{n,Gm1} + V_{n,Gm1fb} \approx V_{n,LPF} \approx 15.5nV/\sqrt{Hz} \tag{5.4}$$

This leads to a LPF with a total capacitance of ~400pF which can (just) be implemented on-chip.

5.2 Circuit Design

In this section, the detailed circuit design of the various blocks of the CTΣΔM is described.

5.2.1 First Stage Integrator

The key design requirements for the first integrator are low noise, low offset and high gain. High gain of this stage relaxes the noise and offset requirements of the following stages. It also facilitates the compensation of the input stage's nonlinearity by that of the feedback path. The low offset and low 1/*f* noise corner requirements are achieved to some extent by using large transistors in the input pair. However, this is not enough to achieve the offset and 1/*f* noise requirements and therefore, chopping is used to modulate the remaining offset and 1/*f* noise of the integrator to a frequency outside the band of interest.

In this section, the chosen integrator topology is first described, followed by the transistor level design of its operational transconductor amplifier (OTA). The simulated noise performance is

then shown along with the chopping strategy. Finally, the effect of chopping on the DC gain and the transfer function of the integrator are discussed.

5.2.1.1 Choice of Topology

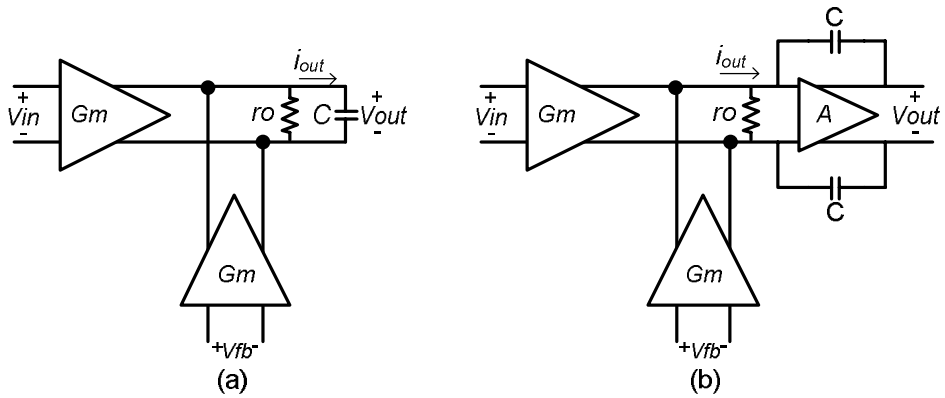


Figure 5.2 - (a) Gm-C with passive differentially connected capacitor (b) Gm-C with active-C structure

As shown in Figure 5.2, there are two possible ways of implementing a Gm-C integrator. The DC gain of the integrator with passive current summation over differentially connected capacitor (Figure 5.2a) is limited by the gain of the OTA. However, it requires only one capacitor, which is half the size of the ones used in the Figure 5.2b. topology and results in four times less capacitor area. Although the additional gain stage of the Figure 5.2b can provide higher DC gain, it comes at the expense of more power dissipation.

In the chosen 0.7µm CMOS technology, it is possible to achieve a DC gain greater than 100dB with a gain-boosted single-stage OTA. Therefore, the topology shown in Figure 5.2a is chosen to save area and power dissipation.

5.2.1.2 Design of OTA

To speed up the design process, the OTA used in this work is a slightly modified version of a previous design [12], provided by Rong Wu. This OTA was also used in the design of an state-of-the-art CFIA based sensor readout system [20]. A further advantage of re-using this OTA is that it facilitates a good comparison between the proposed and previous approaches. The circuit of the OTA is briefly discussed here to highlight the key features relevant to the design of the proposed system.

The OTA is based on a gain-boosted folded-cascode architecture. The input differential pairs are biased in weak-inversion to achieve high power efficiency. The input pairs (M1-M2, M7-M8) are cascoded by LVT transistors (M3-M4, M9-M10), whose gates are also connected to the input. These LVT transistors make the drain-to-source voltage (V_{DS}) of the input transistors independent of the input common-mode voltage, thereby resulting in better CMRR. The tail current sources are also cascoded for high CMRR. To reduce excess noise from the current sources of the cascode branches, transistors M_{13}, M_{14}, M_{19}, and M_{20} are resistively degenerated. The gain-boosting amplifiers are implemented as scaled-down versions of this fully differential folded-cascode topology.

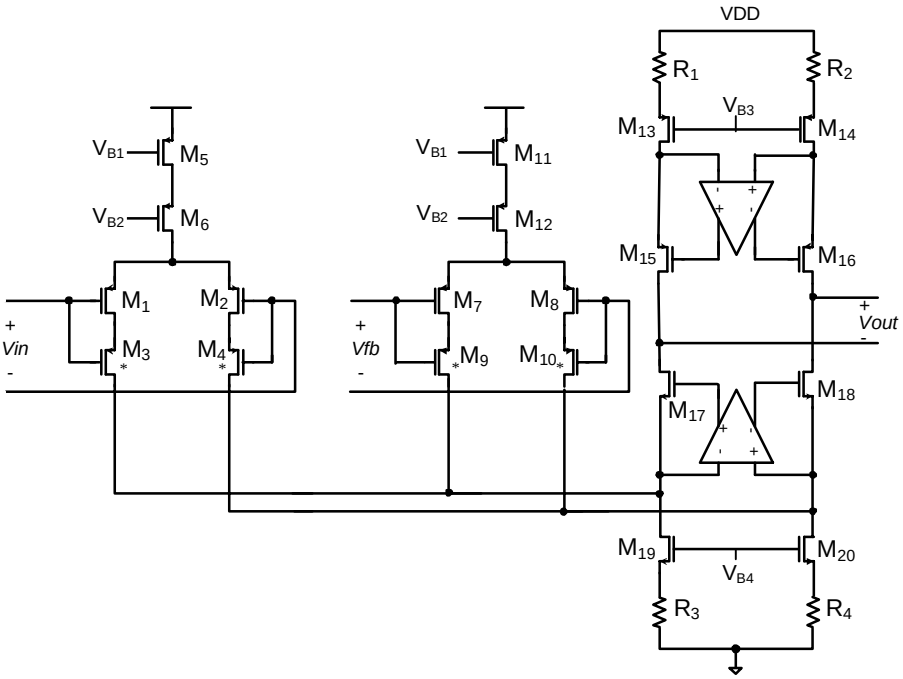


Figure 5.3 - Gain boosted folded cascode OTA for first stage integrator (Courtesy: Rong Wu[4])

The transconductance of the input differential pairs is 0.55 mS .The open-loop gain and phase of this OTA without any output load is shown in Figure 5.4. The dominant pole is set by the capacitance at the output node. The total capacitance at this node is approximately

$$C_{out} = C_{gdM15} + C_{gdM16} + C_{gdM17} + C_{gdM18} \sim= 0.055 \text{ pF}$$

Simulations show that the extrapolated unity gain frequency, i.e. ignoring the second pole, is at 1.47 GHz.

$$UGBW_{single\_pole} = \frac{Gm_1}{C_{out}} = 1.47GHz \tag{5.5}$$

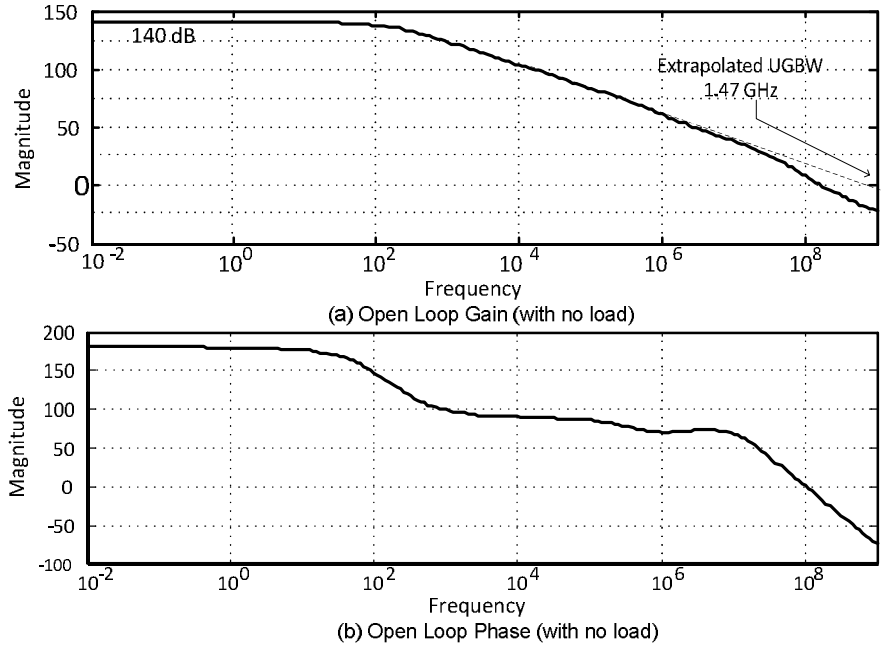


Figure 5.4 - Open loop gain and phase with no external load

5.2.1.3 Noise

The major contributors to the input-referred noise of the OTA are:

(a) The input pairs (M1-M2, M7-M8)
(b) The current sources (M19-M20, M13-M14)

The total input-referred thermal noise spectral density can be expressed as

$$V_{n,input} = V_{n,in,M1-M2} + V_{n,in,M3-M4} + \frac{1}{gm_{1,2}}\left(\frac{gm_{19,20}}{1+gm_{19,20}R_{3,4}}V_{n,in,M19-M20} + \frac{gm_{13,14}}{1+gm_{13,14}R_{3,4}}V_{n,in,M13-M14}\right) \quad (5.6)$$

The optimum noise performance can be achieved by choosing a high value of *gm* for the input pair and a low value of *gm* for the current sources. For high power efficiency, the input pairs are biased in weak inversion region where the gm/I_D ratio is highest. Additionally, input pairs (M_1-M_2 and M_3-M_4) are sized to have large area for low offset and 1/*f* noise corner frequency. As the current flowing into the NMOS current source transistors (M_{19} and M_{20}) is highest, the value of $gm_{19,20}$ is much higher than $gm_{13,14}$. Therefore, assuming that transistors M_1-M_4 are large enough, the leading contributors to 1/*f* noise are transistors M_{19} and M_{20}. To mitigate this, the noise of these transistors is reduced by resistive degeneration. Similarly, the PMOS current source transistors (M_{13} and M_{14}) are also degenerated to reduce their noise.

The thermal noise floor in this design is about 12.5 nV/$\sqrt{Hz}$ and its 1/*f* noise corner frequency is at 17 kHz as shown in Figure 5.5. The chopping frequency must then be greater than 30 kHz to have noise floor lower than 15.5 nV/$\sqrt{Hz}$ as desired.

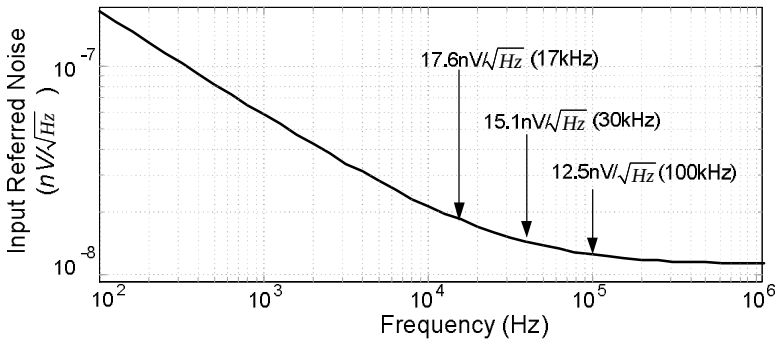


Figure 5.5 - Input referred noise of the OTA used in the first stage

5.2.1.4 Chopping Strategy

The offset and 1/*f* noise of the amplifier are modulated out of the signal band by chopping. To achieve a low 1/*f* noise corner frequency, the entire OTA circuit is placed between the choppers as shown in Figure 5.6.

The noise level after chopping is simulated using the periodic steady state (PSS) simulation tool of Cadence. The resulting noise spectra with two different chopping frequencies (30 kHz and 50 kHz) are shown in Figure 5.7. The two noise spectra show peaks at odd harmonics of chopping frequency, which will give rise to chopper ripple.

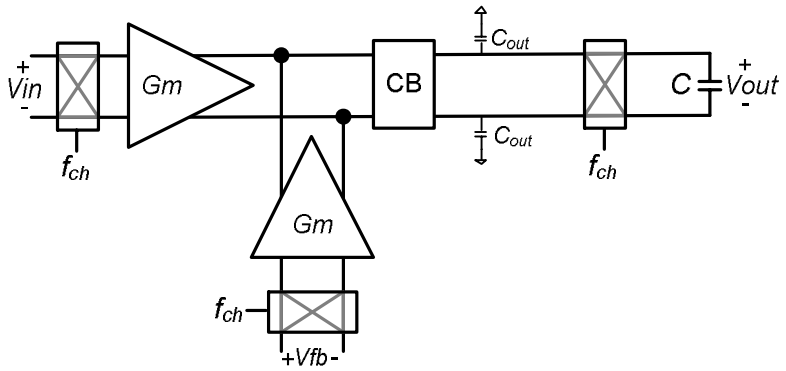


Figure 5.6 - Chopping strategy for the first stage

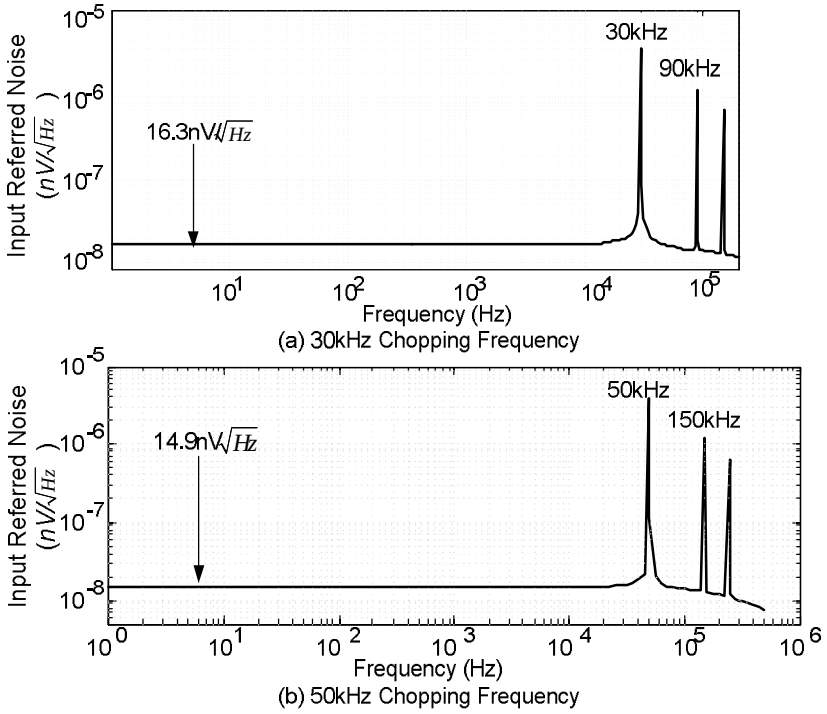


Figure 5.7 - Noise floor after chopping for two different chopping frequencies

5.2.1.5 Impact of chopping on DC gain

The effective DC gain of a chopped amplifier can drop due to the limited bandwidth of the amplifier. If the chopping frequency is greater than the bandwidth of the amplifier, its effective DC gain can be estimated by following equation:

$$DC\ Gain_{chopped} \approx \frac{UGBW_{single\_pole}}{f_{chop}} \tag{5.7}$$

where, $UGBW_{single\_pole}$ is the extrapolated unity gain frequency of an amplifier without any load, and f_{chop} is the chopping frequency.

Therefore, the DC gain of a chopped amplifier is effectively determined by its unity gain frequency and the chopping frequency. For a chopping frequency of 50 kHz, the resulting DC gain is about 89dB, which is higher than the target value in Table 5.1.

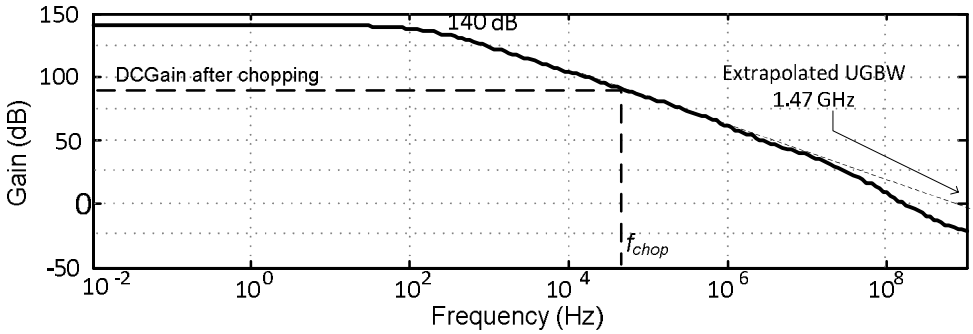


Figure 5.8 - Effect of chopping on the DC gain of the amplifier (no external load)

5.2.1.6 Integrator Transfer Function

The desired UGBW of the first integrator (ω_{u1})is 200 kHz. Therefore, given the *Gm* of the OTA, the size of integrating capacitor can be estimated from:

$$\omega_{u1} = \frac{Gm_1}{C_{int1}} \tag{5.8}$$

As the OTA's differential transconductance is about 0.55mS, the size of the capacitor is about 400pF for the desired ω_{u1}. However, differentially connecting the integrating capacitor means that the capacitor's size can be halved (Figure 5.2b). This implies that an integrating capacitor of 200pF is sufficient. The resulting transfer function of the integrator is shown in Figure 5.9.

It may be noted that the drop in the DC gain of the amplifier after chopping is only dependent on the parasitic capacitance at the output node of the amplifier, before the output chopper switches. It is unaffected by the load capacitor placed after the chopper switches.

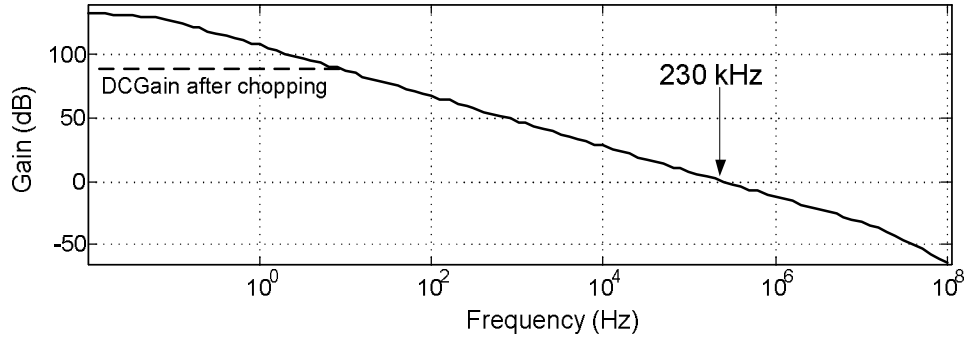


Figure 5.9 - Integrator transfer function (C_{int1} = 200pF)

5.2.1.7 Nonlinearity

As the input differential pair is biased in weak inversion, its nonlinearity is significant. The simulation results for the Gm's nonlinearity are shown in Figure 5.10. The distortion coefficients extracted from this curve are shown in this equation:

$$i_{out} = v_{ind} + 21 \cdot v_{ind}^{\ 3} - 500 \cdot v_{ind}^{\ 5} + 110000 \cdot v_{ind}^{\ 7} \tag{5.9}$$

The harmonic distortion for an AC simulation is shown in Figure 5.11 to be around -38.5 dB.

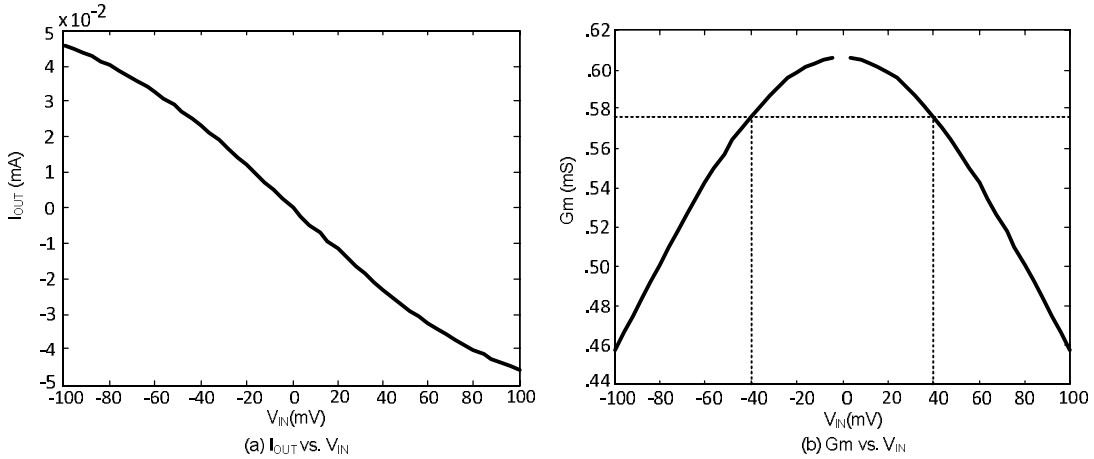


Figure 5.10 - DC sweep simulation result of the differential pair showing the nonlinear Gm

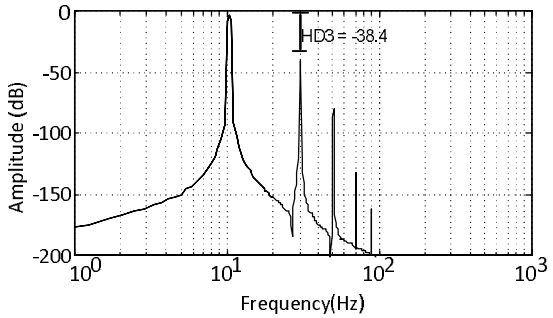


Figure 5.11 - Harmonic distortion for a 40mV sine wave

5.2.1.8 Common-Mode Feedback

An active continuous-time common-mode feedback (CMFB) circuit (Figure 5.12a) is used in the OTA. The dominant pole of the CMFB circuit is at the output node of the amplifier. It was discussed earlier that connecting the load capacitor differentially across the output leads to a smaller capacitor size. However, in this configuration, there is no common-mode load and therefore, the stability of the CMFB circuit suffers. Therefore, in order to better control the stability of the CMFB circuit, the integrating capacitor is divided into differential and common-mode capacitors as shown in Figure 5.12b. The simulated phase-margin of the CMFB circuit is shown in Figure 5.13.

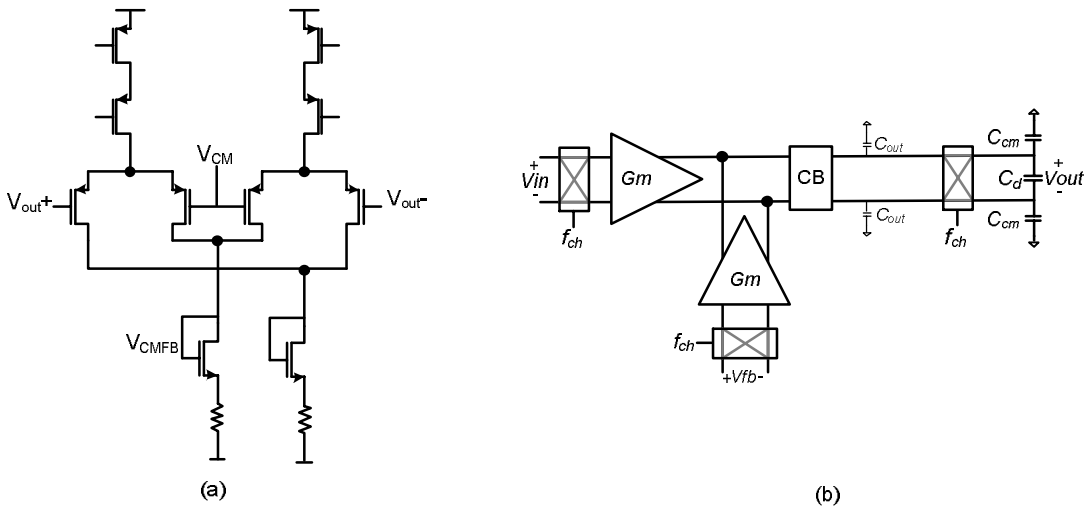


Figure 5.12 - (a) CMFB Circuit (b) Configuration of C_{load}

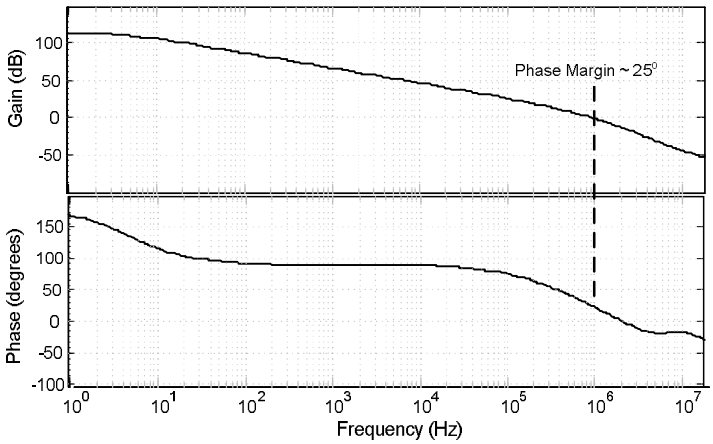


Figure 5.13 - Phase Margin of the Common Mode Feedback Circuit

5.2.2 Second Integrator and Feedforward Path

The key requirement for the second integrator and the feedforward path is the matching of their coefficients. The noise and offset of the second stage are suppressed by the gain of the first stage. However, in order to achieve a very low 1/*f* noise corner, it may be required to chop both first and second stages as in [11]. In this section, the implementation of the second integrator stage and the feedforward path is described.

5.2.2.1 Choice of Topology

There are several possible circuit topologies that can be used for the second integrator: (a) RC integrator, (b) passive R-C filter, (c) discrete-time switched capacitor (SC) integrator, and (d) Gm-C integrator. In this section, their pros and cons will be discussed.

One of the issues with employing an RC integrator (Figure 5.14a) or a passive RC filter in the second stage is that the resistor will effectively be in parallel with the output of the first integrator and will, therefore, limit its DC gain. Ensuring a first stage DC gain of 80dB implies that the resistors in the second stage integrator must be larger than 20MΩ. The input-referred noise of such large resistors will degrade the noise performance of the system. Furthermore, as the feedforward path must be implemented using a high impedance *Gm*-stage and if the second integrator employs an RC stage, the feedforward and the feedback coefficient will not be well matched. Similar issues are encountered if a discrete-time SC integrator is used in the second stage.

It is clear from the above discussion that a *Gm*-C based topology is most suitable for the second stage integrator (Figure 5.14b). The transconductance Gm_2 of the second integrator will not load the first stage (or load the first stage) and therefore has no effect on its DC gain. Additionally, a *Gm-C* based integrator allows better matching between the second stage and its feed-forward path. The feedforward gain is implemented by sizing the Gm_{ff} to be β times the value of Gm_2.

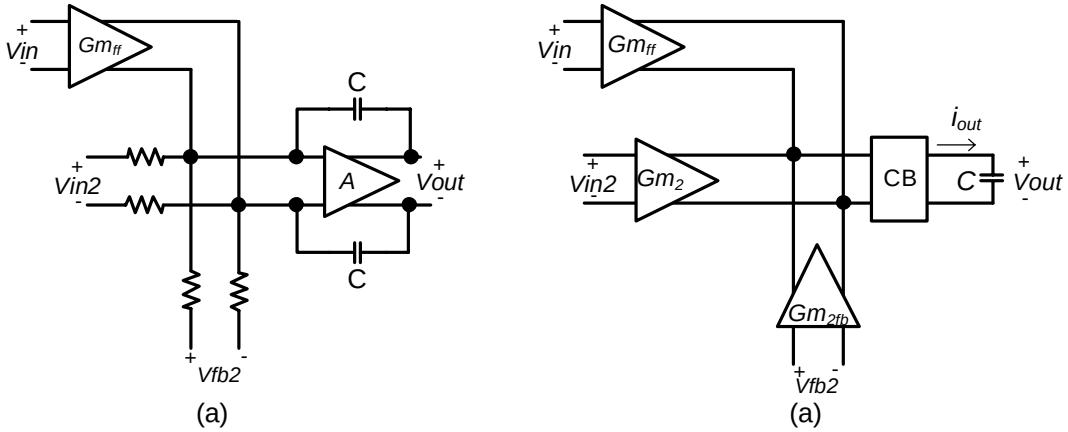


Figure 5.14 - (a) RC integrator with Gm feedforward path (b) Gm-C based integrator

5.2.2.2 Design of OTA

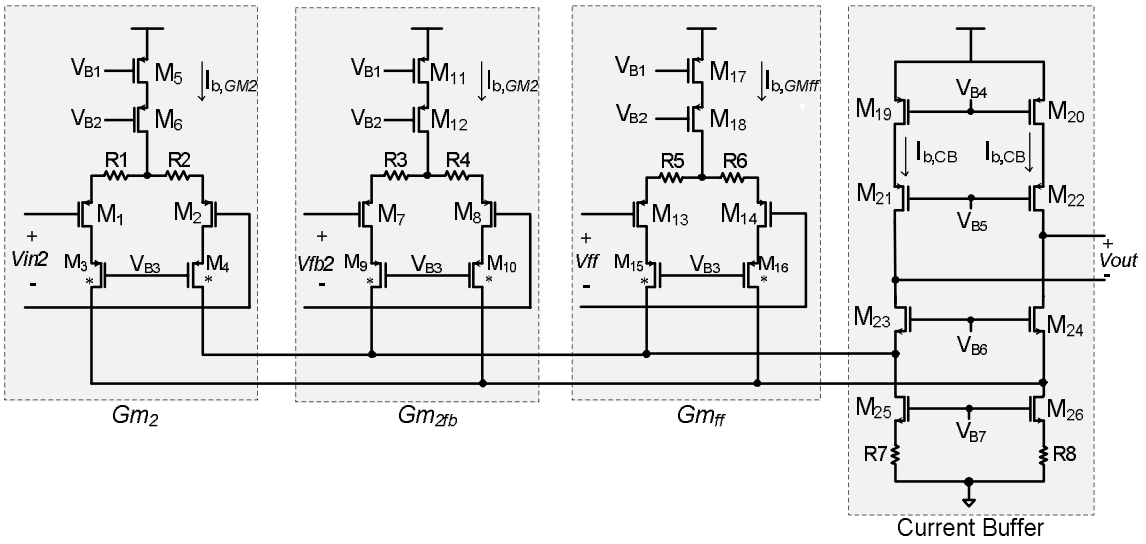


Figure 5.15 - Schematic of the second-stage OTA

Table 5.2 - Design parameters of the second-stage OTA

Parameter	Value
M_1, M_2, M_4, M_8, M_{13}, M_{14}	10u/1u
R_1, R_2, R_3, R_4	360kΩ
R_5, R_6	25kΩ
$I_{b,GM2}$	2.7 uA
$I_{b,GMff}$	9 uA
$I_{b,CB}$	6 uA

The second-stage OTA is implemented using a folded-cascode topology. Its summing node can then be used to perform the feedforward and feedback summation in the current domain. The gain of the feedforward path is set by the ratio of Gm_2 and Gm_{ff}. The differential pairs are resistively degenerated to ensure that their transconductances match better, since resistor matching is better than transistor matching.

The feedback to the second integrator comes from a single-bit voltage-DAC (VDAC2) as shown in Figure 5.1. The reference voltage of VDAC2 is $\beta \cdot V_{REF}$. As V_{REF} is chosen to be around 50mV,

the bitstream driven swing at the input to the feedback differential pair is about ±500mV. This can lead to large spikes in the current being fed to the current summation nodes. In turn, these current spikes can cause voltage spikes at the input nodes of Gm_2 and Gm_{ff} via the gate-source capacitances of their input pairs. To reduce the impact of such voltage spikes, cascode transistors are placed in series with the various differential pairs.

To further mitigate problems due to large switching voltages at the input of the Gm_{2fb} differential pair, the DAC of the second stage is implemented in the current domain rather than in the voltage domain. As shown in Figure 5.16, this is done by switching the output current of Gm_{2fb} instead of input voltage. This is equivalent to using a current DAC (IDAC), but the matching of Gm_2 and Gm_{2fb} is better assured with this topology. In order to minimize the power dissipation in this stage, the differential pairs are designed to have the smallest possible transconductance limited by the size of degeneration resistors. A value of 2µS is chosen, which requires that the value of the degeneration resistors be around 500kΩ.

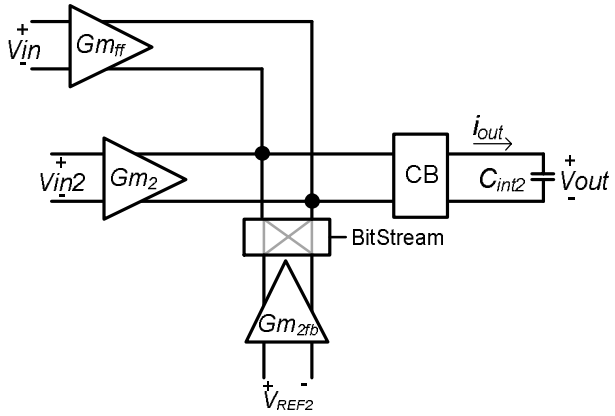


Figure 5.16 - Implementation of DAC for second stage

5.2.2.3 Noise

The noise of the second stage is suppressed by the loop gain of the first stage. In order to not limit the overall input referred noise, the noise floor of this stage is required to be lower than (assuming 80 dB gain in first stage:

$$V_{n,in,2^{nd}\,stage} < \frac{V_{n,in}}{10^4} \simeq 220uV/\sqrt{Hz} \tag{5.10}$$

Although this noise floor is easily achievable, the 1/*f* noise corner of the second stage can limit the 1/*f* noise corner of the system if the second stage is not chopped. In the 0.7 µm technology, the flicker-noise of an NMOS transistor is around 10 times larger than a PMOS transistor with the same area. Therefore, the NMOS current source transistors of the folded cascode OTA (M25 and M26) are the dominant sources of 1/*f* noise. Therefore, these transistors are resistively degenerated to limit their 1/*f* noise. The corresponding input referred 1/*f* noise corner of this stage is shown in Figure 5.17. The noise spectrum is suppressed by the first stage gain of around 80 dB, and therefore, the overall 1/*f* noise corner of the system is likely to be below 0.1 Hz. A lower 1/*f* noise corner can be achieved either by chopping the second stage or by the use of system-level chopping.

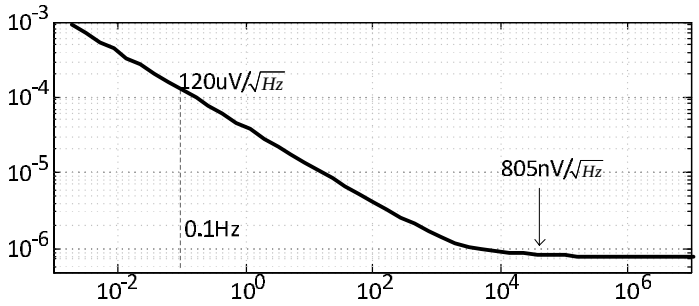


Figure 5.17 - Noise spectrum of second stage OTA

5.2.2.4 Integrator Transfer Function

C_{int2} is chosen to be 2pF which results in a unity gain frequency of 200kHz. The resulting transfer function of the second integrator is shown in Figure 5.18.

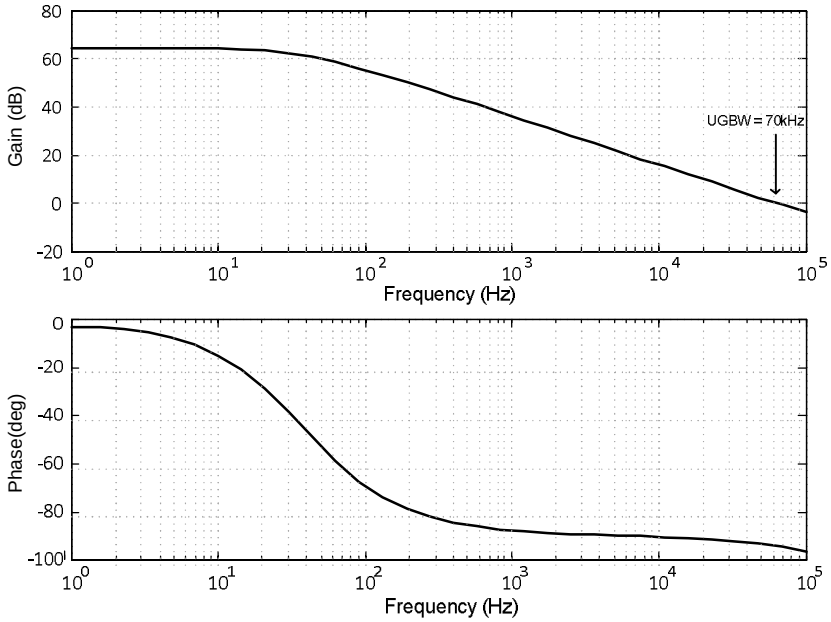


Figure 5.18 - Gain and Phase response of second stage integrator

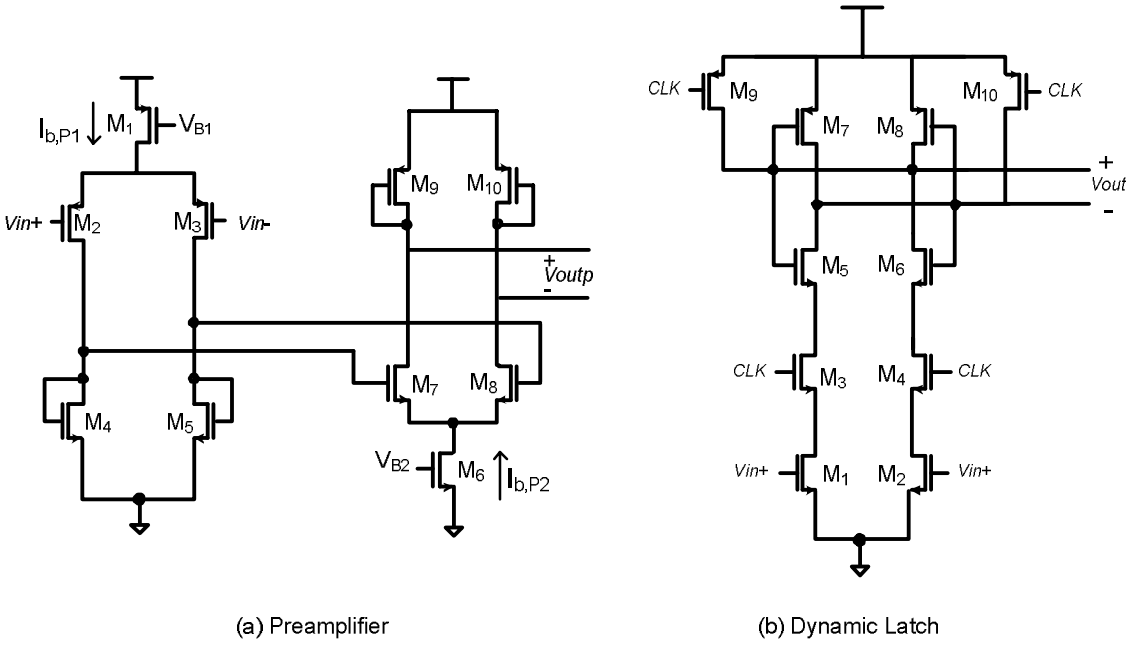
5.2.3 Quantizer

5.2.3.1 Design of Quantizer

The quantizer noise and error in a sigma-delta modulator is suppressed by the loop gain of preceding stages. Therefore, the main design requirement for the quantizer is a high sampling speed with low power consumption. A dynamic latch based comparator is commonly used in ΣΔMs, usually preceded by a preamplifier to suppress kick-back noise. In this design, a two-stage preamplifier is used before the latch, while a dynamic latch based comparator is used to achieve the 5 MHz sampling speed requirement. Each of the two stages of the preamplifier is based on a simple differential pair with diode load (Figure 5.19a). The majority of power consumed in the quantizer is spent in the preamplifier as the latch does not dissipate static current.

The dynamic latch, shown in Figure 5.19b, works in two phases: (a) precharge, and (b) decision. During the precharge phase, the clock signal is low and the output nodes are charged to high state.

On the rising edge of the clock, the precharge phase ends and both the outputs momentarily settle to the mid-rail position. Thereafter, depending on the polarity and amplitude of input voltage, one of the output nodes is discharged while the other goes high. The time taken in decision is inversely proportional to the amplitude of the signal. The preamplifier provides high gain and helps speed-up the decision of the latch.



(a) Preamplifier (b) Dynamic Latch

Figure 5.19 - (a) Preamplifier circuit to suppress the kick-back noise of the dynamic comparator (b) Dynamic latch based comparator

5.2.3.2 Processing of Quantizer Output

The dynamic latch of the comparator turns both the outputs to high state during the precharge phase. However, the precharge operation must not be visible to the feedback DAC. Therefore, the dynamic latch is followed by a NAND-SR latch that holds the previous value when both the inputs are high (Figure 5.20).

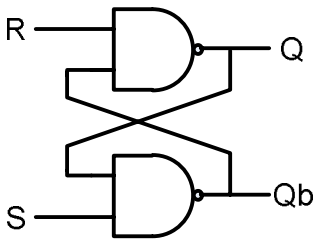


Figure 5.20 - NAND-SR latch holds the output during precharge phase of the comparator

Table 5.3 - SR latch truth-table

S	R	Q
0	1	0
1	0	1
1	1	HOLD
0	0	--

It was discussed in chapter 4 that the data-dependent delay of the comparator can cause nonlinearity in the output. Furthermore, both the Q and Qb outputs of the SR latch are not perfectly synchronized as there is a gate-delay between the two. A gate-delay of 100ps can cause a timing mismatch of ~200 ppm for a 5 MHz clock. Therefore, both polarities of the output must be synchronized perfectly. This can be easily done by the use of two D-flipflops which

synchronize the two outputs with a common clock. In this configuration, delay between the two output polarities is only caused by component mismatch and is of the order of ~1ps.

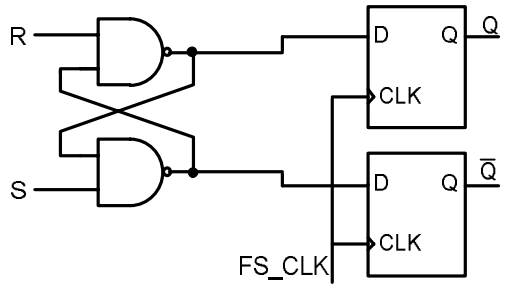


Figure 5.21 - Synchronization of the feedback pulses

5.2.4 Voltage DAC and Low Pass Filter

5.2.4.1 Voltage DAC

The output of voltage DAC is fed to an RC low pass filter. The accuracy of the ΣΔM is only as good as the accuracy of the feedback DAC. As the reference voltage needed for the modulator is very small (50 mV), it is not possible to generate it accurately. Therefore, an off-chip voltage reference of 5V or 3V is used and this voltage is attenuated to get the desired reference voltage. It is possible to combine a passive attenuation circuit with the RC low pass filter to create a compact and accurate voltage feedback circuit (Figure 5.22).

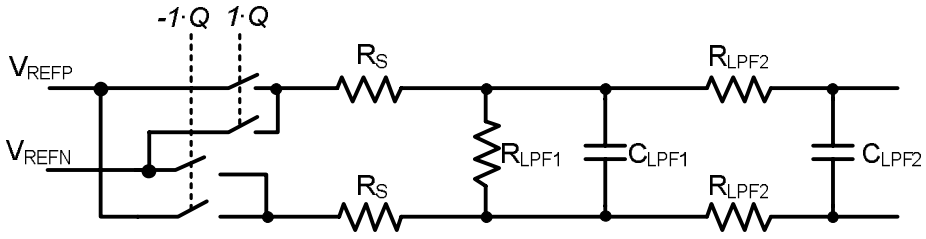


Figure 5.22 - Voltage DAC and LPF

Any mismatch in charge-injection of the switches can decrease the input impedance of the reference source. The switch sizes are chosen to be small to minimize charge-injection and decrease the dynamic input impedance. The input impedance for reference source is therefore decided by the LPF resistors R_S and R_{LPF1}.

5.2.4.2 Low Pass Filter

In the circuit shown in Figure 5.22, a reference voltage of 5V is used and attenuated to 50mV by the ratio of resistors R_S and R_{LPF1}. To achieve this, the resistor ratio required is given by:

$$\frac{R_{LPF}}{2R_S + R_{LPF}} = \frac{1}{100} \tag{5.11}$$

The value of R_S must be chosen to be approximately 50 times R_{LPF}. The noise contributed by the resistor R_S is negligible as it is also attenuated by the resistor divider. The poles of the two LPF stages are set by the time constants - $R_{LPF1}C_{LPF1}$ and $R_{LPF2}C_{LPF2}$. The resistor value is chosen on the basis of the noise specifications and the capacitor area. The total output referred noise of the

LPF is expressed in the following equation, assuming a negligible noise contribution from the reference source:

$$V_{n,LPF} = \sqrt{4kT(R_{LPF1} + 2R_{LPF2})} \tag{5.12}$$

For the allocated noise floor of 15.5nV/$\sqrt{Hz}$, the required size of R_{LPF1}+ 2·R_{LPF2} is ~15kΩ. Considering the desired pole frequency of ~40kHz, this resistor size leads to an on-chip capacitor area of around 1.2nF, which turns out to be more than one and half times the area of the rest of the circuit. Therefore, in this design, noise is traded-off for a smaller capacitor size. The chosen resistor values are:

$$R_{LPF1} = 10k\Omega \text{ and } R_{LPF2} = 5\ k\Omega$$

The corresponding size of LPF capacitors is 400pF each. This leads to an LPF noise floor of 18nV/$\sqrt{Hz}$ and an overall noise floor of 23.6nV/$\sqrt{Hz}$. Additionally, an option is provided to place external resistors and capacitors parallel to the on-chip components for test purposes. The off-chip components can be used to tune the performance of the design.

5.2.4.3 Return-to-Zero

As discussed in Chapter 4, the finite and asymmetric rise/fall time of the DAC can result in nonlinear inter-symbol-interference (ISI). To tackle this issue, return-to-zero (RZ) signalling is used. In this design, the return-to-zero is implemented by shorting the two terminals of DAC with a dedicated switch as shown in Figure 5.23.

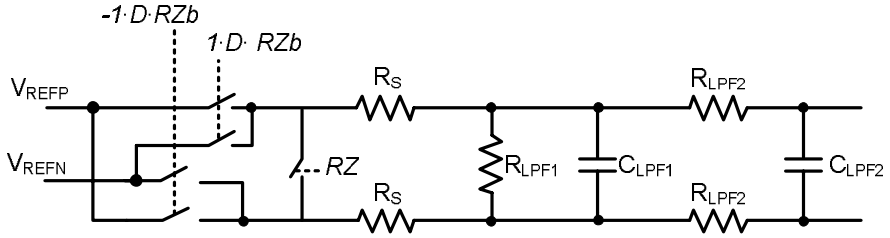


Figure 5.23 - Return-to-zero DAC

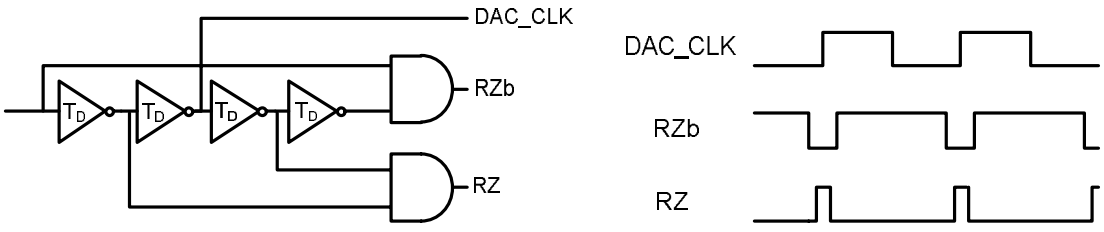


Figure 5.24 - Return-to-zero logic

The timing of return-to-zero is shown in Figure 5.23. When RZ switch turns on, the other DAC switches must be in off state so that the positive and negative reference terminals are not shorted. When RZ switch turns on, the nodes V_R+ and V_R- are shorted and their potential settles to the common-mode level of the reference.

5.3 Layout

The circuit was implemented in 0.7 µm CMOS technology. The layout of the circuit is shown in Figure 5.25. The cross-coupled layout technique was used for circuit blocks where good matching was desired such as the input and feedback transconductors, and the degeneration resistors of second stage and feedforward transconductor stages. The first OTA stage is critical for performance of the chip and therefore is placed as far away from the digital logic as possible. Decoupling capacitors are distributed over the chip filter supply noise. Further, to avoid any coupling between digital and analog parts of the chip, the analog areas are isolated from the digital logic by use of guard rings. Separate supply and ground lines are used for digital and analog supply. The digital and analog supply and ground lines are connected outside the chip on the board.

The total area of the chip including IO pads is 9.6 mm^2. The active area is around 3 mm^2. About a third of the chip area is occupied by the capacitors employed by the low pass filter. A part of these capacitors can be placed off-chip to reduce the chip area.

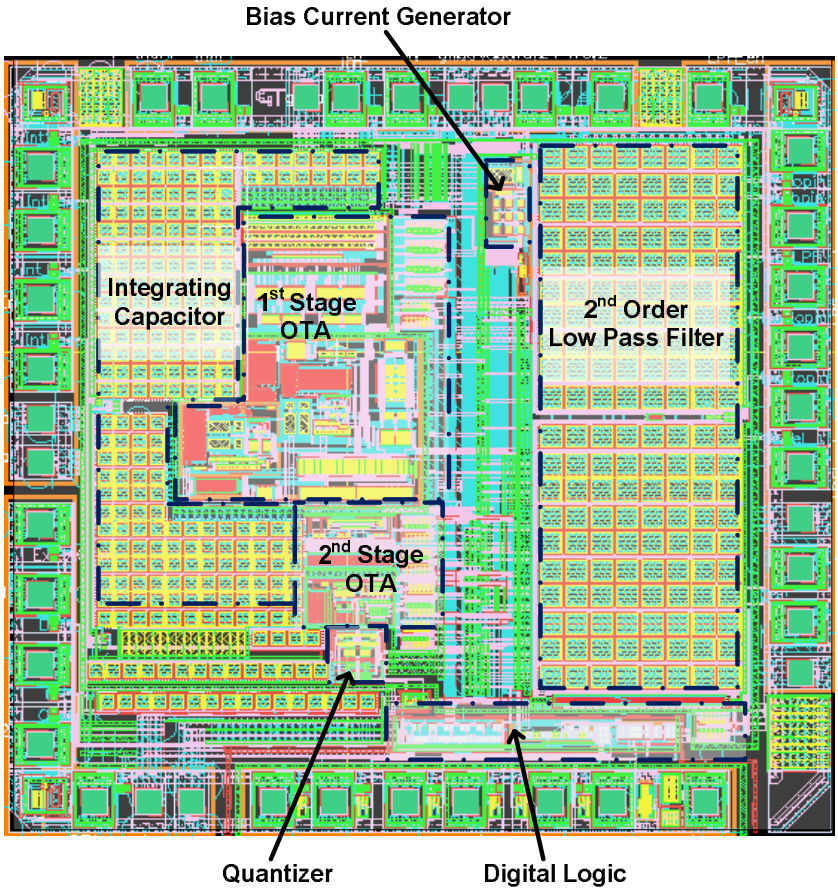


Figure 5.25 - Chip layout showing various blocks

Although a test chip was taped out in On-Semiconductor's 0.7 µm CMOS technology, an error in the mask generation meant that the chip was not fully functional. After discovering their error, the foundry agreed to process the design again, but unfortunately this is still on-going at the time of writing this thesis. However, the results from system-level, circuit-level and post-layout simulations of the CTΣΔM are presented in this thesis to demonstrate the expected performance of the test chip.

5.4 Results

In this section, the simulation results of the CTΣΔM are presented. The simulations are done using Cadence Spectre and the parasitic extraction from layout is done with Calibre PEX. The native Monte Carlo tool of Cadence was used for mismatch simulations. Cadence PSS, Pnoise and PXF tools are used for AC simulations.

As mentioned earlier, the OTA used in the input stage is a slightly modified version of an existing design for which the chip measurement results have been published [20]. Therefore, the simulation results from Monte Carlo and PSS tools were verified against the IC measurement results. The Monte Carlo results for offset and gain error were found to be in close agreement with the measurement results. The measured 1/*f* noise corner of the OTA is lower than that predicted by Cadence, but the results from simulation are assumed to be correct for this design.

5.4.1 Amplifier Post-Layout Simulations

5.4.1.1 Gain

The main impact of layout parasitics is on the frequency response of the OTA. The extrapolated UGBW of the OTA in post-layout simulations is ~500 MHz which implies a parasitic capacitance of 0.1pF at the output node. With this UGBW, an effective DC Gain of 80dB can be achieved with the target 50 kHz chopping frequency determined from system level simulations.

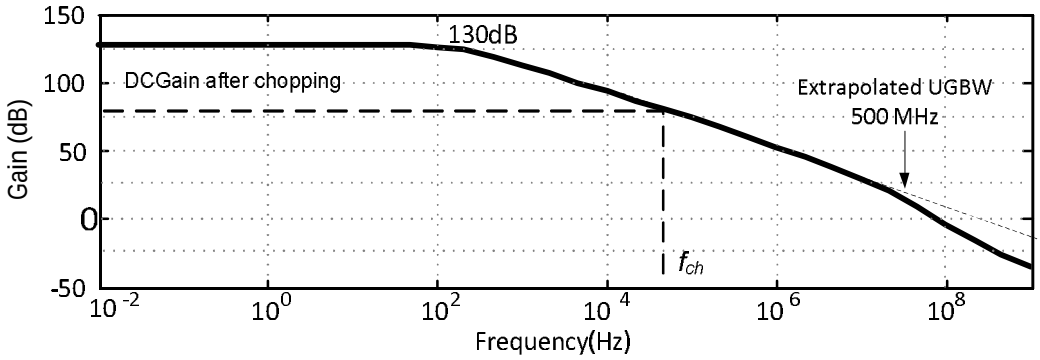


Figure 5.26 - Frequency response of Gain of the OTA with no load (Post-layout)

The frequency response of the integrator with a load of 200 pF capacitor is shown in Figure 5.27. The resulting UGBW of the integrator is at 200 kHz as desired from the system level specifications.

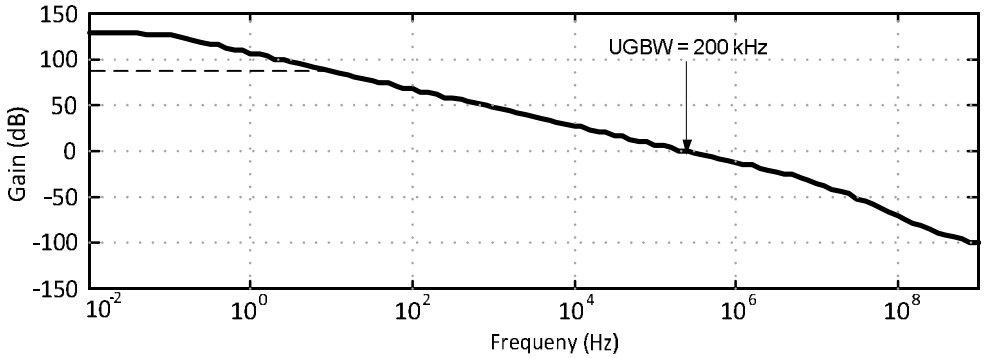


Figure 5.27 - Frequency response of Gain of the OTA with 200pF load (Post-layout)

5.4.1.2 Offset and Noise

The noise and offset simulations of the system are performed assuming a linear amplifier model as shown in Figure 5.28. This model is not applicable to the large signal feedback of the CTΣΔM. However, this assumption does hold good for the input stage, as the feedback LPF filters the single-bit quantizer output and the signal appearing at the feedback *Gm* stage is a replica of its input stage.

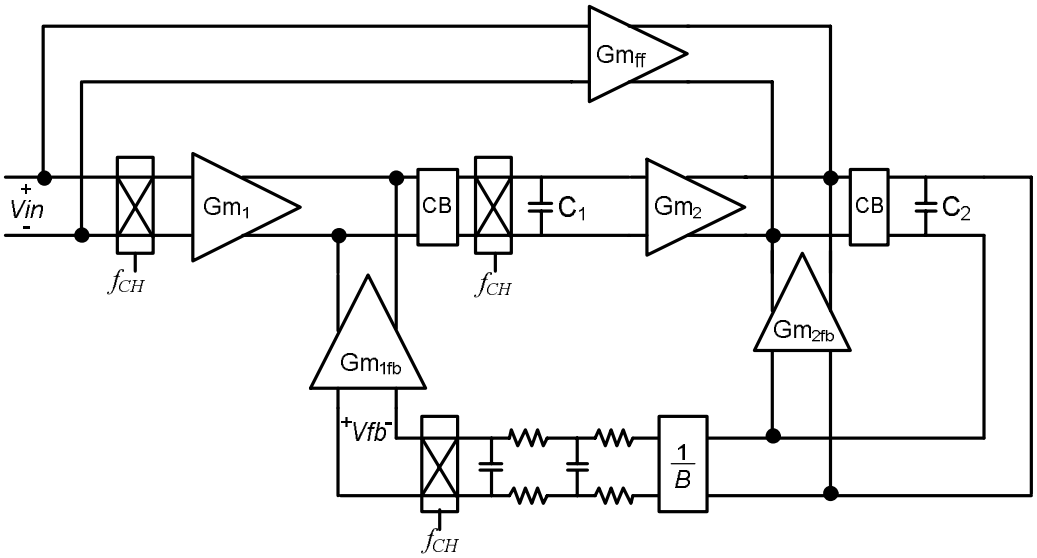


Figure 5.28 - Linear model of the CTΣΔM for noise and offset simulations

The layout of the OTA was performed to minimize sources of systematic offset and gain-error. Therefore, extra attention was paid to the matching of the input differential pairs and the tail current sources. A common-centroid (ABBA) technique was used for the layout of these transistors. The simulated post-layout systematic offset of the circuit is ~3µV, which is much smaller than the simulated random mismatch (Figure 5.29).

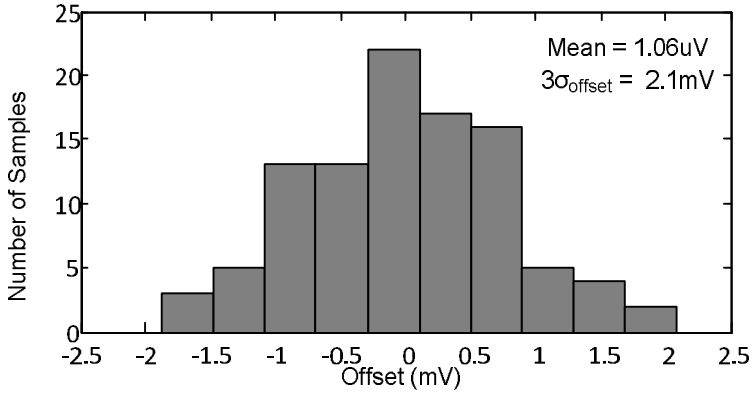


Figure 5.29 - Monte Carlo simulation for offset of first stage

Mismatch in layout parasitics can also cause an increase in the chopped noise floor. In this design, the noise floor after chopping at 30 kHz or 50 kHz frequency does not change significantly. The post-layout PSS noise simulation results are shown in Figure 5.30

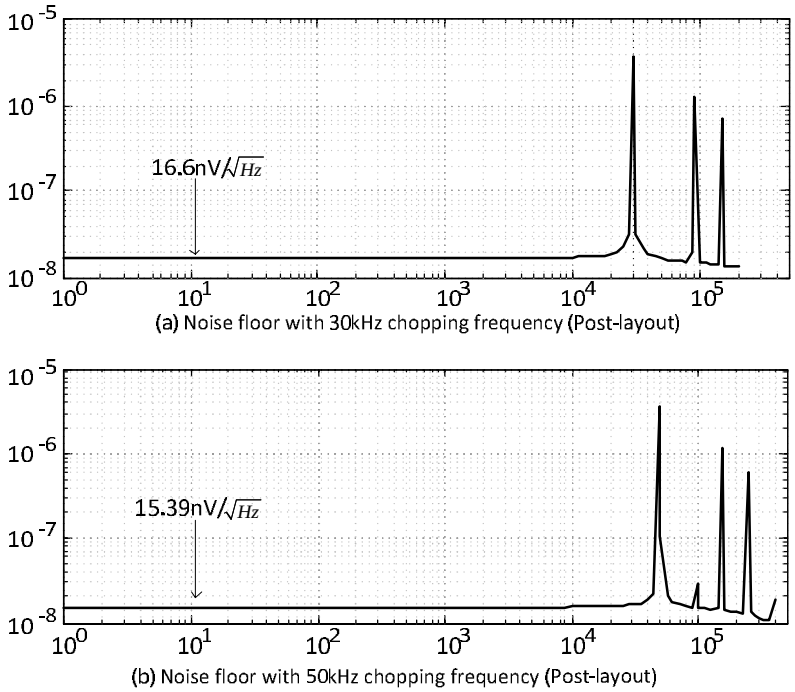


Figure 5.30 - Noise floor after chopping (post-layout)

5.4.1.3 Gain Error

The main disadvantage of a CTΣΔM with a Gm-C input stage is the low gain accuracy since the matching between the *Gm* stages is not expected to be as good as that of resistors or capacitors. Monte Carlo simulation of the input stage showed an expected gain error of 0.63% (Figure 5.31). As explained in Chapter 4, this gain error can be improved by the use of DEM. The amplitude of the DEM ripple will be dependent on the value of gain error. Like the chopper ripple, however, it can be completely removed by the SDM's decimation filter.

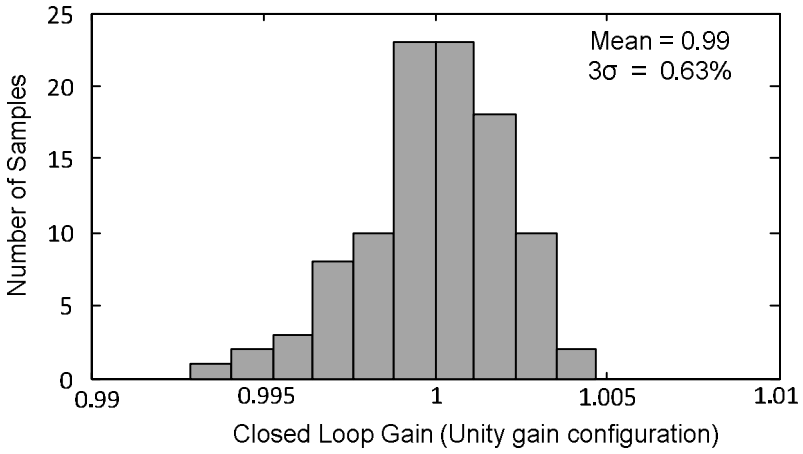


Figure 5.31 - Gain error of the input stage

5.4.1.4 Common Mode Rejection Ratio

The Monte Carlo simulations for CMRR show a mean of 165dB. The worst case CMRR value within 3σ is around 145dB. This is the CMRR of only the input stage and may degrade slightly when placed in a CTΣΔM. However, as the CMRR of the proposed modulator is mainly dependent on the input stage, these results show that the targeted CMRR of 120dB should be easily achieved.

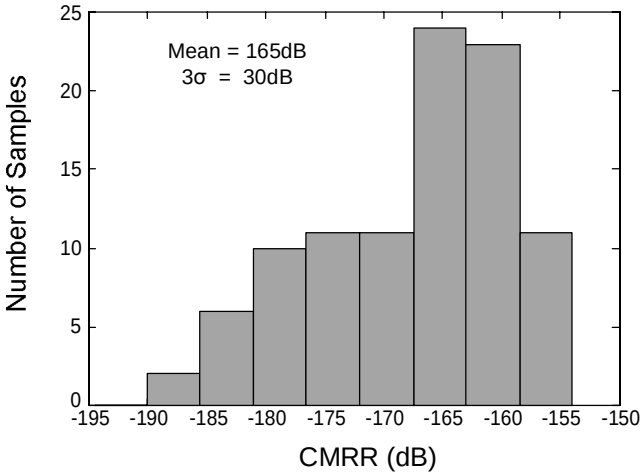


Figure 5.32 - Monte Carlo simulation results for CMRR

5.4.1.5 Feedforward-coefficient Matching

Recall from Chapter 4 that the improvement in linearity of the CTΣΔM depends on the matching of the absolute value of feedforward coefficient with the feedback coefficient. This is because the effective loop-gain for nonlinearity compensation improves by a factor of 1/Δ, where Δ is the absolute error in value of the feedforward coefficient.

The differential pairs used in second stage are resistively degenerated to improve the matching of the feedforward coefficient with the feedback coefficient. Results for Monte Carlo simulations suggest a 3σ matching of 0.15%. Further, considering the systematic error in absolute value of 0.06, the worst-case error in the coefficient would be less than 0.1. This is better than the required 0.2 absolute matching of feedforward coefficient as specified in Chapter 4 to achieve an INL better than 10 ppm.

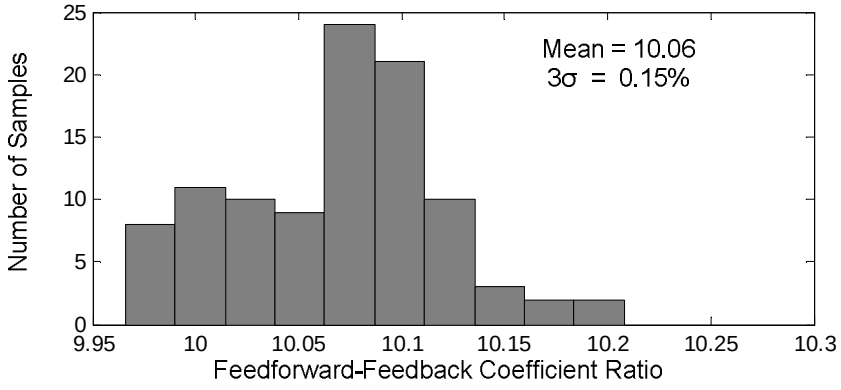


Figure 5.33 - Montecarlo simulation for matching of feedforward coefficient

5.4.2 CTΣΔM Simulation Results

As the frequency band of interest is small while the sampling frequency is relatively high, transient simulations of the CTΣΔM take very long to simulate. To speed up the process, the modulator is divided into two parts: (a) a forward path that includes the loop filters, quantizer and an ideal feedback DAC, and (b) a feedback path that includes the DAC circuit and the LPF. Each of these blocks must work within the specifications. Integrating the two parts does not lead to any additional error due to the overlapping components – the quantizer and the LPF.

5.4.2.1 Forward Path Simulation Results

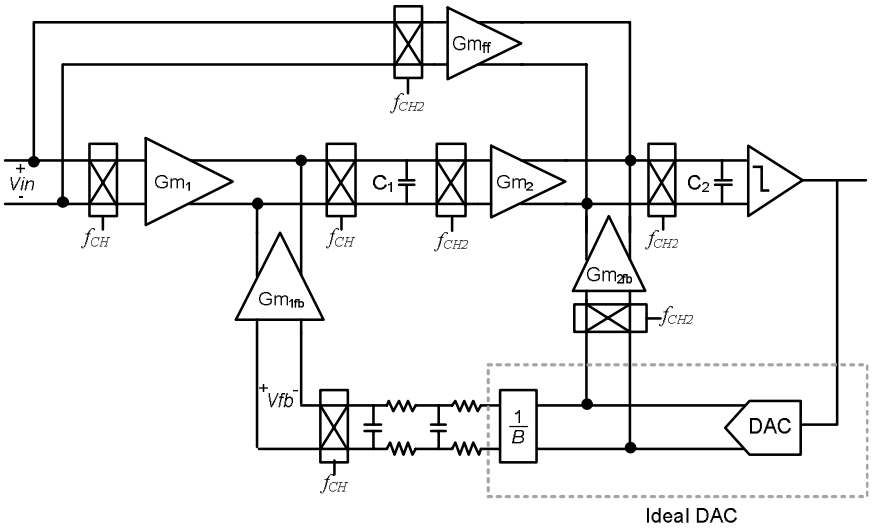


Figure 5.34 - Setup for forward path simulations is done with ideal feedback DAC

Feedforward Path

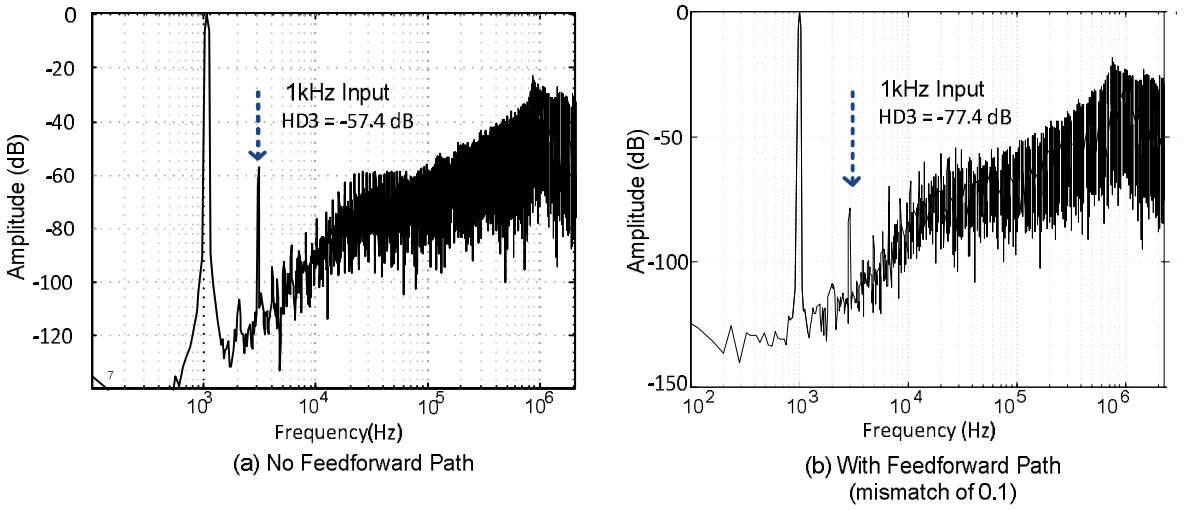


Figure 5.35 - FFT of the CTΣΔM output for a 1 kHz sinusoidal input signal (no-offset)

Recall from the discussion in Chapter 4 that the THD of the system without the feedforward path depends on the AC loop gain of the first stage. The THD improves by around 20 dB, with addition of the feedforward path (with a mismatch of 0.1). The simulation result for an AC input signal is shown in Figure 5.35. The open-loop HD3 of the input transconductor alone is 38 dB for

a 40 mV 1 kHz input signal as shown in Figure 5.11. With nonlinearity compensation and feedforward path, the HD3 is improved by around 40 dB at 1 kHz. The improvement in HD3 is greater for a lower frequency signal as the AC loop gain of the integrator is higher.

Impact of Chopping

The intermodulation of chopper ripple with quantization noise can cause the noise floor to rise and can degrade the THD of the system. Therefore, the choice of chopping frequency must be made carefully. The degradation caused by ripple depends on its amplitude and frequency. The amplitude of chopper ripple is proportional to the offset value and inversely proportional to the chopping frequency.

To see the effect of chopper ripple frequency on the THD, the circuit is simulated with a 3mV offset and at 20 kHz and 50 kHz chopping frequencies. As discussed in Chapter 4, if the chopping frequency is close to the LPF's cut-off frequency, intermodulation between the chopper ripple and the quantization noise results in a higher quantization noise floor. It also leads to a higher third harmonic as can be seen in the simulation results (Figure 5.36). The residual offset is smaller than 100nV in this simulation. However, the main cause of residual offset is the mismatch between chopper switches, which is not simulated here. The circuit simulation results in Cadence are in agreement with the MATLAB simulation results as shown in Figure 5.36b.

The simulation is done with a 200 Hz input signal frequency as a lower frequency would take too much simulation time. A lower input signal frequency would result in a better THD performance.

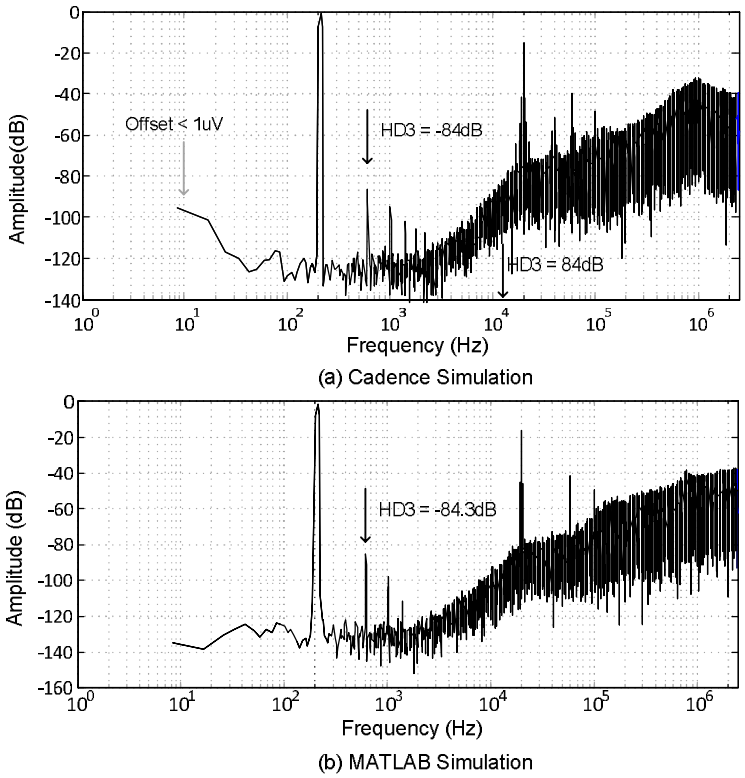


Figure 5.36 - Cadence and MATLAB simulation results for a 40mV, 200Hz input signal with an offset of 3mV and chopping frequency of 20 kHz

A lower noise floor can be achieved by choosing the chopping frequency to be higher than the LPF's cut-off frequency. Using a chopping frequency at 50 kHz (greater than 40 kHz LPF pole frequency) results in an improved HD3 of 96 dB as shown in Figure 5.37.

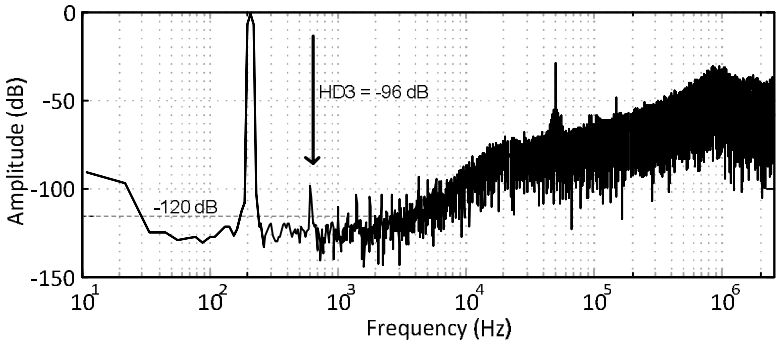


Figure 5.37 - Cadence simulation result for 40mV, 200Hz input signal with an offset of 3mV and chopping frequency of 50 kHz

It may be noted that the noise shaping characteristic of the Cadence simulations is slightly different from that of the MATLAB simulations in that the quantization noise peaks at around 1 MHz. This is caused by the half-cycle delay in the synchronizer employed to eliminate the data-dependent delay of the comparator. This change in noise shaping affects the noise floor and THD as it reduces the effectiveness of the feedback LPF. However, these effects can be reduced by decreasing the synchronizer's delay from half a clock cycle to some smaller value. This flexibility is implemented on the chip.

DC Sweep Simulation

The simulation for DC inputs shows a normalized error of less than 10ppm for an input range of 45mV. This result is in good agreement with the system level simulations.

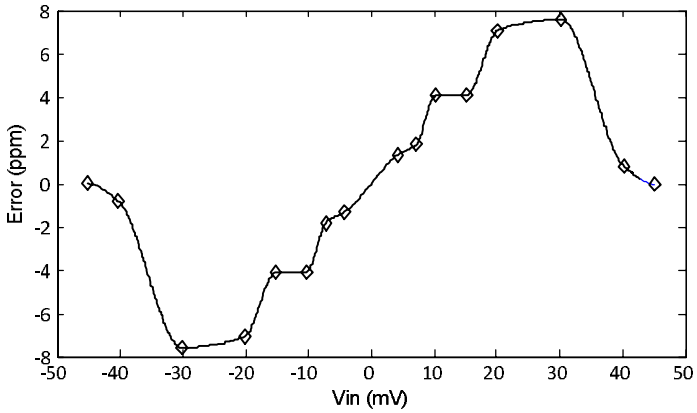


Figure 5.38 - Normalized error for DC inputs

5.4.2.2 Feedback Path Simulations

The feedback path simulations are critical as any errors in the feedback path are directly referred to the input. The feedback path is simulated with 10% mismatch in switch size to model the worst case mismatch. The resulting error curves show that the NRZ-DAC has about 2-3 times higher INL than the RZ-DAC (Figure 5.39). However, errors in both of these DACs are much smaller than the forward path error. This implies that the errors in forward path dominate the overall error in the system. The error curve for RZ-DAC shows less than 1ppm INL.

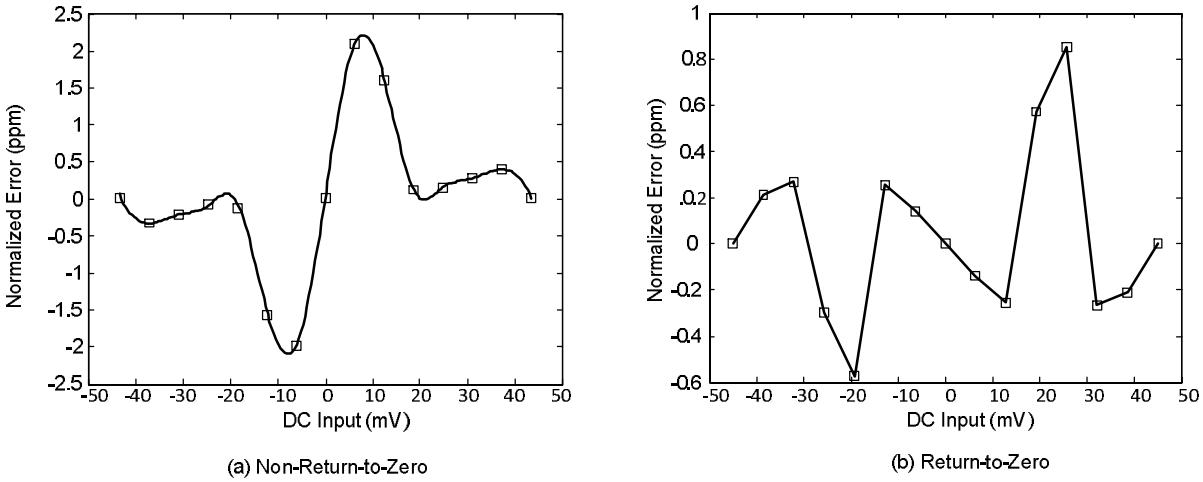


Figure 5.39 - Normalized error in the feedback path

5.4.3 Power Dissipation

The total supply power dissipation of the system is 220 µA over a 5 V supply. The power dissipation of each block is summarized in the Table 5.4

Table 5.4 - Power Dissipation

Circuit Block	Power Dissipation
First Integrator	190.5 µA
Second Integrator	24 µA
Feedforward Path	14 µA
Quantizer (Static)	7 µA
Bias Circuit	5 µA
Total	**240 µA**

5.4.4 Summary and Discussion of Results

5.4.4.1 Comparison with State-of-the-Art

The key results of this work are summarized and compared with state-of-the-art results published using other precision sensor readout system architectures.

Table 5.5 - Comparison of Results

	This work	**Wu** [12]	**ADS 1282** [20]	**Sarhangnejad** [4]	**Zwan** [3]
Architecture	Gm-C CTΣΔM	CFIA/ DTΣΔM	2 Opamp IA/ DTΣΔM (Gain = 8)	Gm-C CTΣΔM	Gm-C CTΣΔM (Multibit)
FSR	± 45 mV	± 40 mV	± 500 mV	± 50 mV	± 1.2 V
BW	10 Hz	10 Hz	10 Hz	100 Hz	500 kHz
Noise Floor	22 nV/sqHz	16 nV/sqHz	6 nV/sqHz	200 nV/sqHz	-
SNR	118 dB	126 dB	127 dB	79 dB	54 dB
INL	< ± 10 ppm	< ± 5ppm	± 0.5ppm	-	200 ppm
THD (@10Hz)	-110 dB	-	-122 dB	-87 dB	-70 dB
Offset	< 1 µV	< 200 nV	+/- 1 µV	32 µV	340 µV
CMRR	> 120 dB	120 dB	110 dB	> 120 dB	> 80 dB
Power	240 µA (5V)	270 µA (5V)	3.8 mA (5V)	400 µA (5V)	2.54 mA (5V)
Technology	0.7 µm CMOS	0.7 µm CMOS	-	0.7 µm CMOS	-
Area	9.5 mm^2 (3 mm^2 active)	11.5 mm^2 (6 mm^2 active)	--	3.3 mm^2	15 mm^2

5.4.4.2 Discussion of Results

As actual measurement results of the test chip are not available, the comparison drawn in Table 5.5 is only indicative. However, the results of circuit-level simulations are in complete agreement with the results of system-level simulations and, more importantly, are also in line with measurements on a similar CFIA, which gives a high level of confidence in the validity of these simulations.

The most important consideration for this work was the THD and INL performance of the CTΣΔM. The improvement obtained in the linearity performance is significantly aided by the feedforward path as seen in both system and circuit level simulations. The ± 8 ppm linearity achieved in the circuit-level simulations corresponds well with the expectation from system-level simulations with a 1% mismatch in the feedforward coefficient. Furthermore, the feedforward

coefficient has a random mismatch of less than 0.15% (3σ) which is too small to significantly impact the THD and INL. Furthermore, any systematic mismatch in this coefficient can be tuned to improve the linearity. Therefore, it is reasonable to expect an INL of $< \pm 10$ ppm in chip measurements. This INL is comparable to other CFIA based readout systems and CTΣΔMs and is an order of magnitude improvement over the state-of-the-art accuracy of CTΣΔMs. However, it is still an order of magnitude higher than the performance of state-of-the-art readout systems based on a two-opamp IA.

The noise floor achieved in this work depends on the noise of the input Gm stage and the feedback LPF resistor. The noise floor can be reduced by increasing the size of LPF capacitors at the cost of more area or external components. In this chip, an option is provided to use off-chip capacitors and resistors to reduce the LPF noise in order to explore the lower limit on achievable noise floor.

The offset that can be achieved with this technique is not limited by any system-level concerns. Therefore, an offset comparable to CFIA based readout systems can potentially be achieved with the proposed architecture.

As the proposed architecture borrows heavily from a CFIA, similar CMRR and power dissipation numbers can be achieved. The post-layout and Monte Carlo simulation results suggest that very high CMRR can indeed be achieved with the proposed architecture. The Monte Carlo results gain credibility from the fact that the simulation results for offset and gain-error match the measurement results from previous CFIAs with a similar design.

The main strength of the proposed CTΣΔM architecture is its lower power consumption, high CMRR and fewer analog blocks compared to commercially available sensor readout systems. Moreover, its power dissipation is slightly lower than that of CFIA based readout systems.

6 Conclusion

6.1 Summary

In this thesis, the theory and implementation of a CTΣΔM-based sensor readout system has been presented. The use of CTΣΔM improves upon conventional sensor readout systems by combining an instrumentation amplifier and an ADC in a single loop. This allows for a more efficient design procedure and lower power dissipation than the state-of-the-art readout systems.

The main contribution of this work is developing the theory and architecture for precision CTΣΔM with high input impedance. This is achieved by the use of feedback nonlinearity compensation and a generic architecture for linear Gm-C CTΣΔM based readout systems. The nonlinearity compensation is enabled by the use of a low pass filter in the feedback path which creates a trade-off between stability and THD of the system for AC signals. This trade-off is mitigated by employing a feedforward path that aids the nonlinearity compensation by increasing the modulator's effective loop gain and thus making the system suitable both for DC and AC signals.

The CTΣΔM-based readout system was implemented in 0.7 µm technology. Unfortunately, a mask error at the foundry meant that its performance could not be measured. However, the functionality and merits of the proposed architecture have been demonstrated through extensive circuit and system level analysis and simulations. These show that the CTΣΔM achieves state-of-the-art resolution and accuracy with lower power dissipation and reduced analog complexity. The residual offset, CMRR and gain-error are also comparable to the state-of-the art.

A drawback of the proposed system is a more complicated trade-off between the choice of chopping frequency and the resulting quantization noise floor and linearity. However, the noise floor and accuracy of the modulator can be preserved by choosing the chopping frequency in conjunction with the cut-off frequency of the filter in the modulator's feedback path.

The proposed CTΣΔM topology offers significant advantages over existing high accuracy CTΣΔM topologies and is a simpler and more efficient solution for the precision sensor readout systems.

6.2 Future Work

1. The number of circuit simulations that could be done was limited by the long simulation runtimes. Therefore, measurement of a correctly fabricated chip is needed to confirm the effectiveness of this concept.

2. The interaction of chopper ripple and quantization noise can limit the overall performance of this system. Although a suitable choice of the chopping frequency allows the desired performance to be achieved, a more robust mechanism may be sought in the future. In order to achieve this, the input stage can be auto-zeroed before chopping or a chopper ripple reduction loop may be used depending on the application requirements.

3. The active area of the design is less than 30% of the total chip area, which is currently dominated by the capacitors of the LPF. The use of an FIR filter in place of an RC-filter should result in a more compact design. However, this will present new challenges for circuit noise, quantization noise and implementation.

4. The generic architecture proposed in Chapter 3 of this dissertation can be employed in various applications that require a high impedance input stage. The design of this circuit was aimed at low-bandwidth precision sensor readout systems. However, this concept can be used in different applications by altering the design of the outer or inner loop-filters of the generic architecture. In general, the proposed technique can be used to integrate the preamplifier and ΣΔM functions in applications requiring lower noise or higher accuracy over wider bandwidth.

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