STUDIES IN WAVE DIGITAL FILTER THEORY AND DESIGN

REINDER NOUTA

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Nicole.
Oan Heit en Mem.

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CHAPTER 1

SUMMARY.

With the rapid technological advances in digital devices, circuits and systems, signal processing by digital techniques has become increasingly attractive [1-10]. One of the possibilities of digital signal processing is digital filtering. A digital filter is a discrete-time system consisting of additions, multiplications and delay elements which operates on an input sequence of numbers to produce an output sequence of numbers according to some numerical algorithm.

A digital filter can be used in several forms. We mention four of them.

1. A digital filter can operate on an analog signal through sampling and conversion, according to the scheme shown in figure 1.1.

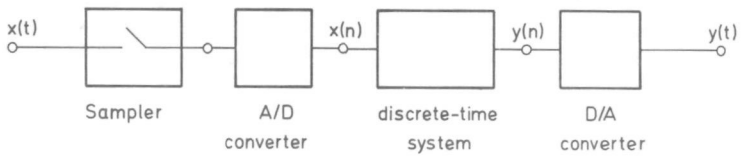


Fig. 1.1. A digital filter operating in an "analog environment"

The signals x(t) and y(t) in figure 1.1 are analog signals and x(n) and y(n) are the corresponding sequences of numbers.

2. A digital filter can operate on signals which are already in digital form and remain in that form too.
3. A digital filter can be used to simulate an analog, continuous-time system on a digital computer.
4. A digital filter can be the implementation of an algorithm, programmed on a general purpose computer and operating on real numbers.

Digital filtering is used (or will be used in the near future) in various areas of application. We mention some.

1. In telecommunications. Especially in digital transmission, FDM to TDM conversion or vica versa [11-13], detection of tones, echo canceling.
2. Speech processing and processing of audio signals in general. For instance, we have the problems of speech analysis and synthesis for bandwidth reduction [14,15] and music synthesis.
3. The processing of multi dimensional data, for instance pictures [16].
4. Radar and sonar signal processing.
5. Signal processing in geophysics.

For more details about these applications we refer to Oppenheim [17].

Digital filtering offers several advantages:

1. Flexibility. The filter characteristics may be changed easily simply by reading in some new parameters. A simple digital filter, implemented using hardware and operating sufficiently fast, can be used to realize a number of filters in a time-shared way.
2. Reliability. A number of problems such as element tolerances, sizes of components etc. that arise in analog systems can be avoided. Instead, we have the possibility of constructing identical systems in an easy way and a whole system may be completely integrated on one LSI chip.
3. Accuracy. The accuracy of a digital filter can be much better than its analog counterpart. Its limitations will mostly arise where it is connected to an analog "outside world".
4. Typical possibilities in discrete-time systems only. There are possible

applications for digital filters which have no analog counterpart. We mention two of them. Digital filters can be designed to have exact linear phase. We can design stable multidimensional digital filters.

The above mentioned advantages and possibilities, the modern LSI technology and the availability of extensive computational facilities are the reasons why the field of digital filtering and digital signal processing in general is developing quite rapidly. The digital filtering principles have already been applied for quite some time in sampled data control systems [18] and the design methods developed there are still used, and have been adapted to deal with modern technological possibilities and applications.
In addition to these conventional methods, modern methods have also been developed. One of these methods is called wave digital filtering [19] and is discussed in the rest of the chapters. We mention various problems related to the development of digital filter methods.

1. In the linear theory various problems such as different structures and related coefficient accuracy, noise performance and dynamic range are studied.
2. In the nonlinear theory of digital filtering we encounter problems of stability of discrete-time systems, overflow occurrence etc. Structures which are equivalent as far as the linear theory is concerned may have quite different nonlinear properties.
3. Implementation problems. The study of this aspect may range from the design of very fast digital hardware to the development of computer programs.

The wave digital filters form a class which have been introduced as digital simulations of resistivily terminated lossless LC filter networks [20-26] and the so-called unit element filters from microwave filter technology [27-30]. This has been done in order to maintain the excellent properties of these analog filters in their digital counterparts. The most important ones of these nice properties are given below.

1. Analog lossless filters, especially ladder structures, have a low sensitivity to element variations in the filter passbands. Stopband poles can easily be adjusted. These properties can be maintained in the corresponding wave digital filter [31,32].
   The first mentioned property results in a low accuracy of multiplier coefficients. This leads to the possibility of designing really selective digital filters without excessive coefficient accuracy. It also leads to nice noise and dynamic range properties [33,34].
2. The inherent stability and, moreover, the energy handling property, of the resistivily terminated lossless analog filters give rise to a rather unique nonlinear stability property of the wave digital filter. This contrasts with the conventional digital filters [35,36].

Following disadvantages of wave digital filters are to be mentioned.

1. The flow diagram corresponding to a wave digital structure of degree n is in general more complicated than the structure of a conventional digital filter with the same degree n and identical transfer function in the sense that more arithmetical operations are needed.
2. Wave digital filter structures are less modular than conventional structures.

Example: The transfer function H(z) realizing the amplitude characteristic shown in figure 1.2 (first half of a period) is

$$H(z) = \frac{z^3 + 3z^2 + 3z + 1}{345.1z^3 - 819.3z^2 + 665.8z - 183.6} = \frac{Y(z)}{U(z)} . \qquad (1.1)$$

(The variables and symbols used in this example are defined in chapter 2).

A conventional flow diagram corresponding to (1.1) is shown in figure 1.3. There the coefficients of (1.1) are directly present as multiplier coefficients. In contrast a wave digital flow diagram corresponding to (1.1) is shown in figure 1.4.

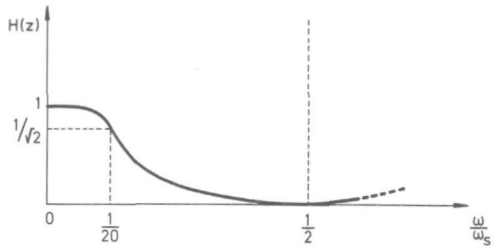


Fig. 1.2. The amplitude characteristic of transfer function (1.1).

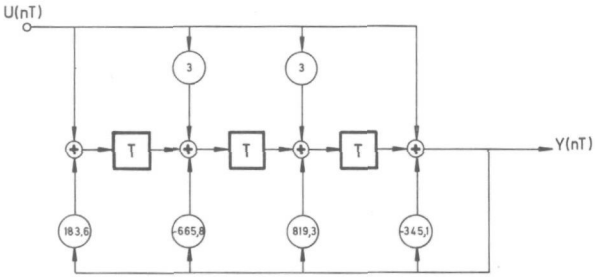


Fig. 1.3. A conventional flow diagram corresponding to transfer function (1.1).

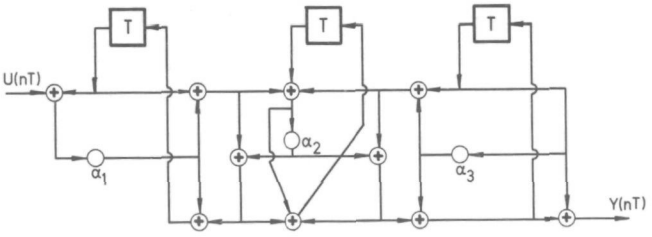


Fig. 1.4. A wave digital filter flow diagram corresponding to transfer function (1.1).

The parameters of the wave digital filter are:

$\alpha_1 = \alpha_3 = 0.1367$, $\alpha_2 = 0{,}0212$ (rounded to 4 decimals). Two aspects concerning the figures 1.3 and 1.4 are mentioned here:

1. Complexity. Figure 1.3 consists of 6 multipliers, 7 adders (with 2 inputs) and 3 delays T. Figure 1.4 has 3 multipliers, 12 adders (with 2 inputs) and 3 delays.
2. Sensitivity. A change in the fourth decimal of a coefficient in figure 1.3 (819.3 → 819.4) has an effect in the second decimal of $H(z)\big|_{z=1}$. For figure 1.4 we have for a change of α_1 from 0.1367 into 0.1368 a change of $H(z)\big|_{z=1}$ within the tolerances of rounding to four decimals.

We conclude the summary by giving a summary of the contents of the chapters 2 - 8.

Chapter 2.

In this chapter the wave digital filter is introduced starting from classical LC filters, conventional digital filters and microwave filters (the unit element). The chapter serves as an introduction to the subject and is not claimed to be either original or complete. The essential features of wave digital filters (linear theory as well as nonlinear aspects) are described shortly. The practical case of ladder wave digital filters is studied. This is a class of wave digital networks which results from applying a translation procedure to the classical LC doubly terminated analog filters. In the chapters 3 and 4 novel material is given which removes the ladder restriction.

Chapter 3.

In classical LC synthesis theory the Jauman structure is well-known. It is a grounded two-port equivalent of the symmetrical two-port lattice. The Jauman structure opens the possibility of realizing transfer functions which are unrealizable in the ladder form and uses the canonical number of elements. By "canonical" we mean here that the number of lossless elements equals the order of the transfer function. The only restriction for the Jauman structure is its symmetry which means that in terms of the impedance matrix description we have to satisfy $Z_{11} = Z_{22}$. A disadvantage of the Jauman structure is that it does not have the sensitivity properties which result in a ladder network. In this chapter we translate the Jauman structure into wave digital form and show that the wave digital network is canonical in terms of the number of multipliers.

Chapter 4.

In network synthesis theory a well-known method of synthesizing a scattering transfer matrix using the lossless elements gyrator, transformer, inductance, capacitance and unit element, is by factoring this matrix into lower order parts. This way, a general transfer function (within realizability constraints) can be synthesized using sections of zeroth, first and second

order. Because these sections do not have the ladder form, the translation method into wave digital form fails in general due to the occurrence of delay-free loops. In this chapter a way is given to avoid this and be able to synthesize a general transfer function (up to the introduction of extra delay) in wave digital form. If reciprocity is to be maintained, also a fourth order section is needed. Due to the non-ladder form of the sections it has not been possible to find wave digital sections which are lossless, only passivity is guaranteed. The meaning of losslessness and passivity in this context is discussed in chapter 2.

Chapter 5.

In this chapter possible implementation of wave digital filter networks using flexible hardware is discussed. For a number of filters (including the true ladder networks) a method is given to construct flow diagrams which use the minimal (or close to minimal) number of memory locations for intermediate variables. It is also shown, especially for the wave digital true ladder networks, that a numbering of internal variables of the corresponding flow diagrams exists such that only the information of two memory locations is needed in each instruction cycle, which defines one arithmetical operation. This is particularly useful for implementation with the so-called two-adress structure.

Chapter 6.

In this chapter an experimental hardware structure is described which has been constructed to study the wave digital filter behaviour in an analog environment. The various flow diagrams are easily programmable and multiplier coefficients are very easily adjustable to test the sensitivity performance. The whole structure operates fast enough to perform experiments in and above the audio range.

Chapter 7.

The possibility of multiprocessor implementation is explored in this chapter. Although only examples of wave digital filters are given, the proposed method is applicable to a much broader class of signal processing

algorithms. When these algorithms are divided into parts to be computed by separate processors, the danger of dead-lock is present. In a dead-lock situation processors are waiting for inputs from other processors which are waiting for the same reason. The result is that the whole calculation process stops and cannot be continued. A theorem concerning the presence of dead-lock is given. The material given in this chapter is meant to be introductory. The whole multiprocessor implementation problem of signal processing algorithms combines the study of a suitable computer architecture, the programming of these structures and efficient forms of algorithms to be computed.

Chapter 8.

In this chapter a dutch version of this summary is given.

CHAPTER 2

INTRODUCTION.

In this chapter we bring together enough material for the reader to understand the essentials of wave digital filter theory and study the following chapters.
For that purpose we give in section 2.1 a review of some elementary concepts from linear sampled-data theory. In section 2.2 the so-called unit element from microwave filter theory is introduced. This unit element plays quite a role in the wave digital filter theory which will follow. In the rest of the sections of this chapter the fundamentals of wave digital filters are given.

2.1. The Z-transform and the bilinear transform[1-8].

In sampled-data theory, the Z-transform is a well-known tool in handling the difference equation between in- and output of a linear discrete-time system. Just as the Laplace transform in linear continuous-time systems, the use of the Z-transform leads to the definition of a transfer function H(z) which is the ratio of two polynomials in the complex variable z.

Let
$$H(z) \triangleq \sum_{k=o}^{\infty} h(kT)z^{-k} \qquad (k = \text{integer}). \qquad (2.1)$$

where h(kT) is the impulse response of the system at instants of

time kT. By introducing the transformation $z = e^{pT}$ (2.2)
in (2.1) we obtain the Laplace transform of a pulsed wave with pulse amplitudes given by h(kT).
Relation (2.2) which defines a map of the p-plane onto the z-plane, is shown in figure 2.1 where we have

$$\omega_s \triangleq \frac{2\pi}{T} \quad (\omega_s \text{ is the sample radial frequency}) \tag{2.3}$$

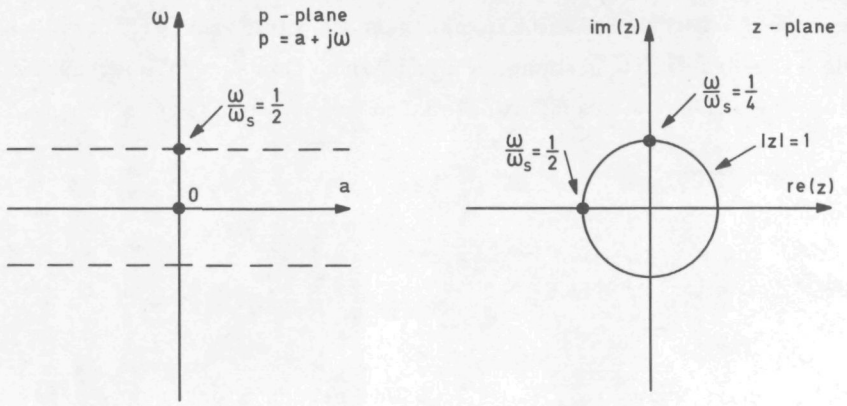


Fig. 2.1. The p-plane and z-plane related by $z = e^{pT}$.

Without further proof we state a few well-known properties of the transforms used:
The open left-half of the p-plane is mapped periodically onto the inner part of the unit circle in the z.-plane.
The imaginary axis of the p-plane is consequently mapped periodically on the unit circle in the z-plane.

A rational transfer function H(z) of a stable system has poles in the inner part of the unit circle. Because of the periodicity along the jω-axis in the p-plane, frequency specifications for linear discrete-time systems lead to transfer functions which are trancedental functions in p and become rational in z if (2.2) is used.

In order to simplify approximation methods for obtaining transfer functions from specifications, the bilinear transform is introduced.

Let

$$w \triangleq \frac{z-1}{z+1} = \frac{1-z^{-1}}{1+z^{-1}} = \frac{1-e^{-pT}}{1+e^{-pT}} = \tanh\left(p\,\frac{T}{2}\right) \triangleq u + jv. \tag{2.4}$$

By this transformation the left part of a periodicity strip in the p-plane which is mapped within the unit circle in the z-plane is now mapped onto the left half of the w-plane. In the next section we will introduce w-plane elements (unit element, w-plane inductance, w-plane capacitance) by using the Richards transformation from microwave filter theory.

For $p = j\omega$ we have

$$u=0 \text{ and } v = \tan\left(\frac{\omega T}{2}\right) = \tan\left(\frac{\omega}{\omega_s}\,\pi\right). \tag{2.5}$$

This relation is shown in figure 2.2. One period along the ω-axis for which we have

$$\left|\frac{\omega}{\omega_s}\right| \leq \frac{1}{2} \tag{2.6}$$

is now mapped onto the entire v-axis in the w-plane.

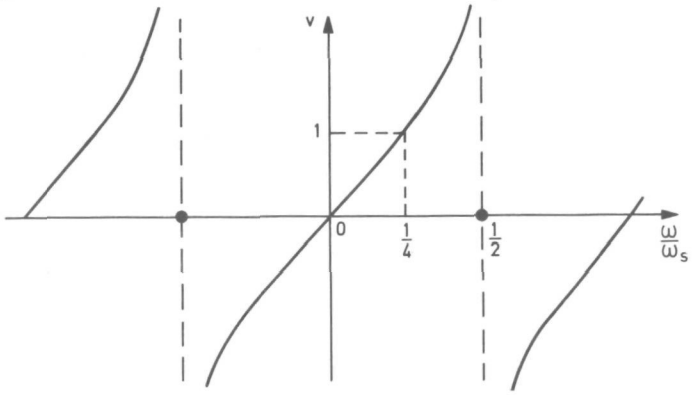


Fig. 2.2. Part of the function $v = \tan(\frac{\omega}{\omega_s}\pi)$.

Methods which have been developed in the continuous case for the design of transfer functions from filter specifications along the entire w-axis can be used here.

We obtain w-plane transfer functions which transform into z-plane functions using (2.4). This way, we eliminate the problem of finding a transfer function using periodic functions for the approximation of specifications along the ω-axis. Two aspects need mentioning here.

The first one is the non-linearity of relation (2.5) as shown in figure 2.2. The second one is that a transfer function H(w) with linear phase (or constant group-delay) does not lead to a transfer function H(z) with the same property, indeed

$$\tan \phi^{(w)} = \frac{v}{u} \longrightarrow \phi^{(w)} = \arctan\left(\frac{v}{u}\right)$$

$$\tau_g = -\frac{d\phi}{d\omega} = -\frac{\partial \phi^{(w)}}{\partial v} \cdot \frac{\partial v}{\partial \omega} = \tau_g^{(w)} \cdot \frac{\partial v}{\partial \omega} = \tau_g^{(w)} \frac{\frac{T}{2}}{\cos^2\left(\frac{\omega T}{2}\right)} \qquad (2.7)$$

(τ_g = group-delay).

For further information about the above mentioned method of obtaining digital filter transfer functions we refer to the literature [5].

2.2 The unit element. [27-30]

In this section we give a short introduction to the synthesis of microwave filters. Instead of lumped elements in the low frequency case we have here as a basic element a lossless transmission line of length ℓ and characteristic impedance R as shown in figure 2.3.

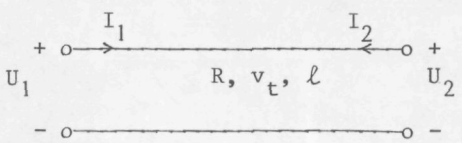


Fig. 2.3. A lossless transmission line of length ℓ and characteristic impedance R (unit element).

The chain matrix K of such a line is defined and given by

$$\begin{vmatrix} U_1 \\ I_1 \end{vmatrix} = K \begin{vmatrix} U_2 \\ -I_2 \end{vmatrix}, \quad K = \begin{bmatrix} \cos\left(\frac{2\pi\ell}{\lambda}\right) & jR\sin\left(\frac{2\pi\ell}{\lambda}\right) \\ j\cdot\frac{1}{R}\sin\left(\frac{2\pi\ell}{\lambda}\right) & \cos\left(\frac{2\pi\ell}{\lambda}\right) \end{bmatrix} \tag{2.8}$$

in which $$\lambda = \frac{v_t}{f}, \tag{2.9}$$

where v_t equals the propagation speed and λ is the wave length in the line. In the case when more than one line element is used in the synthesis, we shall require that these elements have the same ℓ. They may have different characteristic impedances R. The choice made for ℓ can then be expressed as

$$\ell = \frac{\lambda_r}{4}, \tag{2.10}$$

where λ_r equals the wave length corresponding to some specific frequency f_r.

In the case a microwave lowpass filter is constructed a possible choice for f_r is the cut-off frequency. In the case of a bandpass filter f_r is chosen to be the centre frequency.

Using (2.9) and (2.10) we obtain

$$K = \frac{1}{\sqrt{1+\tan^2\left(\frac{\pi}{2}\cdot\frac{f}{f_r}\right)}} \begin{bmatrix} 1 & j.R\tan\left(\frac{\pi}{2}\cdot\frac{f}{f_r}\right) \\ j\cdot\frac{1}{R}\tan\left(\frac{\pi}{2}\cdot\frac{f}{f_r}\right) & 1 \end{bmatrix} \tag{2.11}$$

The connection between the microwave theory and the wave digital theory is made by choosing:

$$w = \tanh\left(\frac{p}{4f_r}\right) \tag{2.12}$$

This is known as the Richards transform.

With $p = a + j\omega$ and $w = u + jv$ (a and u real parts, ω and v imaginary parts) we obtain for a=0

$$v = \tan\left(\frac{\pi}{2} \cdot \frac{f}{f_r}\right). \tag{2.13}$$

Expression (2.13) introduced in (2.11) with $v = \frac{w}{j}$

leads to

$$K = \frac{1}{\sqrt{1-w^2}} \begin{bmatrix} 1 & wR \\ \frac{w}{R} & 1 \end{bmatrix} \tag{2.14}$$

The w-plane element described by (2.14) is called a unit element. Except for an, easy to deal with, factor $(\sqrt{1-w^2})^{-1}$ the chain matrix K is rational in w and can be used in w-plane synthesis. The impedances Z_1 and Z_2 at port 1 of the transmission line with port 2 short-circuited or left open, are

$$Z_1 = Rw \quad , \quad Z_2 = \frac{R}{w} \tag{2.15}$$

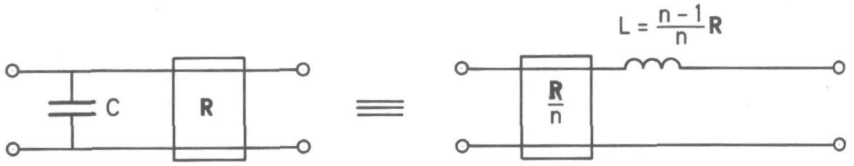
Z_1 is called a w-plane inductance and Z_2 is called a w-plane capacitance. We can now apply classical methods of synthesizing continuous lossless filters and obtain networks containing w-plane elements. We can also use table books [21-24] for the design of w-plane LC ladder filters. Synthesis of w-plane filter networks is even more flexible than in the continuous filter case because of the presence of an additional w-plane element, the unit element. For convenience, the Z-, Y- and S-matrix (reference resistances 1Ω) of this element are given in section 2.7.

In microwave theory, this flexibility is restricted due to physical difficulties arising in building series-parallel connections of transmission lines (open- or short circuited at port 2). These difficulties can be circumvented by making use of the all-pass property of a unit element with characteristic impedance R=1Ω. A number of these unit elements, which only introduce additional group-delay, is then cascaded with the ladder network and "shifted into" the ladder networks

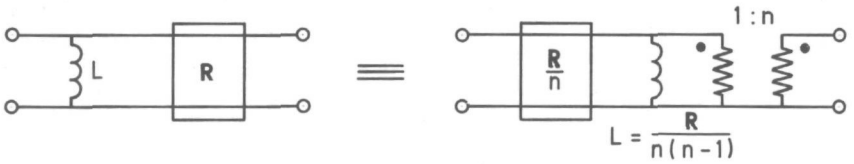
such that for instance only either parallel- or series connections of w-plane inductances os capacitances or resonant circuits remain between unit elements.

This "shifting into" the w-plane ladder network is performed by applying some w-plane identities (so-called Kuroda identities) of which the most important ones are given below.

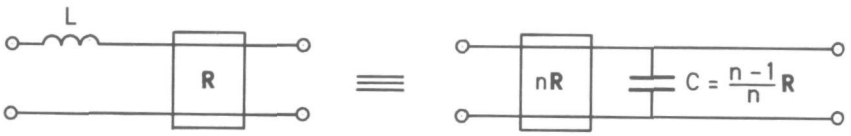
Some w-plane identities.



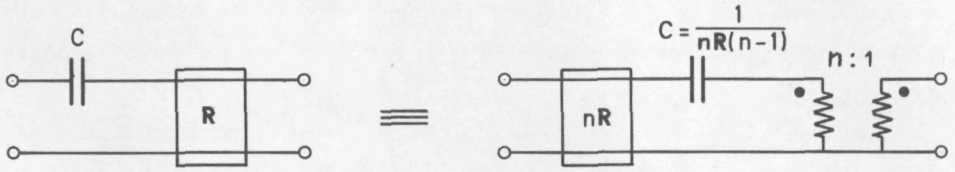
$n = 1 + RC$



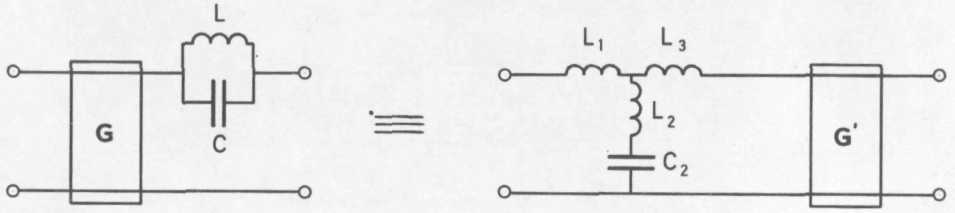
$n = 1 + \frac{R}{L}$



$n = 1 + \frac{L}{R}$

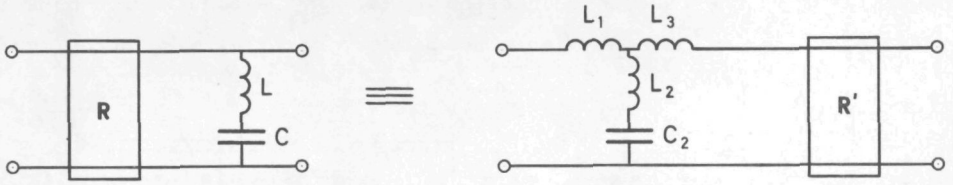


$$n = 1 + \frac{1}{RC}$$



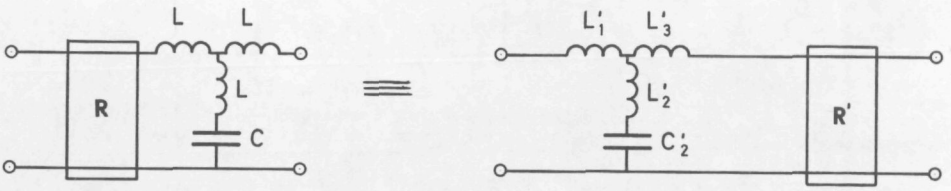
with $G' = \dfrac{G}{1 + LC + LG}$, $L_3 = \dfrac{LC}{G'(1 + LC)}$, $L_1 = -\dfrac{LC}{G} < 0$,

$L_2 = \dfrac{C}{GG'}$, $C_2 = LGG'$.



$$R' = \frac{(1 + LC)R}{1 + LC + RC}, \quad L_3 = -R' < 0, \quad L_1 = R,$$

$$L_2 = \frac{RR'}{R - R'}, \quad C_2 = \frac{LC}{RR'}(R - R').$$



$$L_1L_2 + L_1L_3 + L_2L_3 = 0,$$

$$R' = \frac{R(L_1 + L_2) + L_2'RC_2 + L_1^2}{(L_1 + L_2)\{1 + C_2(R + L_1 + L_2)\}}, \quad C_2' = C_2 + \frac{1}{R} - \frac{1}{R'},$$

$$L_1' = \frac{L_2C_2R(R + L_1)}{L_2C_2R - L_1}, \quad L_2' = \frac{L_2C_2}{C_2'}, \quad L_3' = \frac{-L_1'L_2'}{L_1' + L_2'}.$$

Some equivalences between w-plane resonant circuits and cascaded unit elements are also very important for the rest of this chapter and are given below.

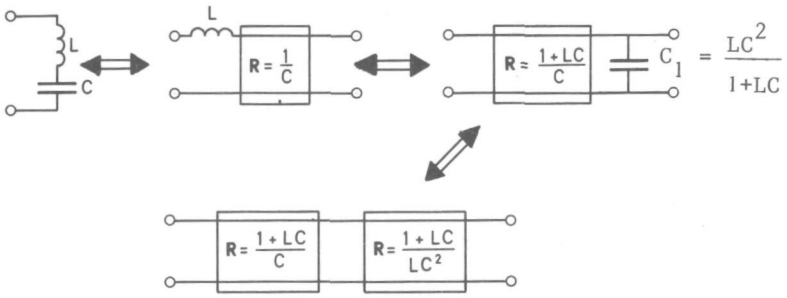


Fig. 2.4a. Equivalence between a w-plane series resonant circuit and a cascade connection of two unit elements.

It shows that a series resonant circuit of w-plane elements is equivalent to the cascade connection of two unit elements with port 2 left open. A similar equivalence holds for a parallel resonant circuit.

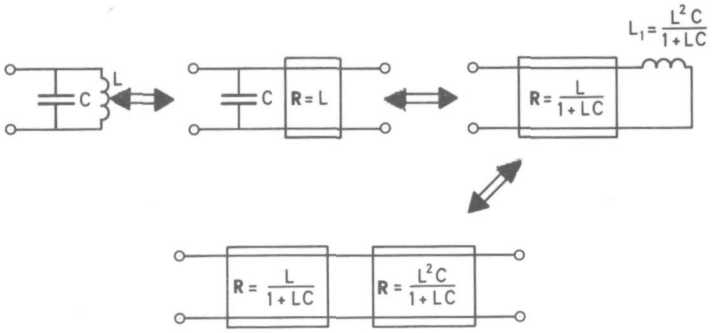


Fig. 2.4b. Equivalence between a w-plane parallel resonant circuit and a cascade connection of two unit elements.

2.3. Why wave digital filters?

In section 2.1 we have indicated a method for finding transfer functions of digital filters. Once such a transfer function has been found, several realizing structures can be given.

If we have the transfer function H(z) given as

$$H(z) = \frac{\sum_{m=0}^{N} b_m z^{-(N-m)}}{\sum_{n=0}^{N} c_n z^{-N(-n)}} = \frac{Y(z)}{U(z)} \qquad \text{or:} \tag{2.15}$$

$$Y(z) = b_N U(z) + \sum_{\alpha=0}^{N-1} \{b_\alpha U(z) - c_\alpha Y(z)\} z^{-(N-\alpha)} \qquad (c_N = 1),$$

then a realization as given in figure 2.5 follows directly.

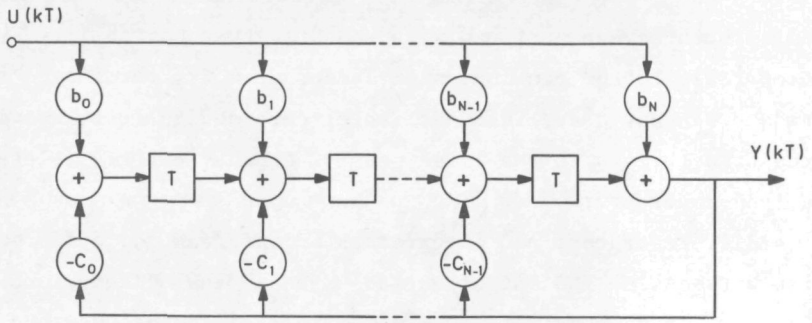


Fig. 2.5. Flow diagram corresponding to (2.15).

We observe that the coefficients present in H(z) appear directly as multiplier coefficients in figure 2.5. See also the example in chapter 1. There is no problem of finding a realization. There is, however, an accuracy problem. In the case of selective filter transfer functions, the poles are clustered close to the unit circle in the z-plane. Figure 2.6 gives an example of a 10th order bandpass digital filter having its centre frequency at $\frac{\omega}{\omega_s} = \frac{1}{4}$.

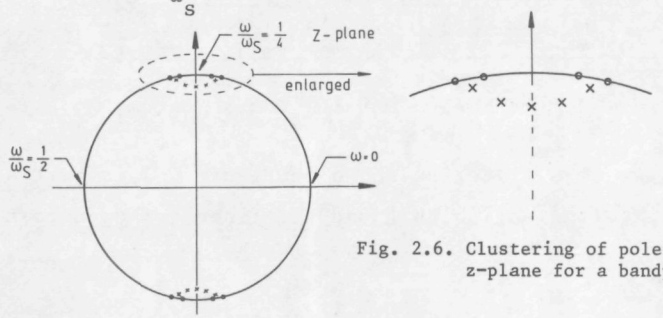


Fig. 2.6. Clustering of poles and zeros in the z-plane for a bandpass function.

The effect of such a clustering is already shown partially in the filter example of chapter 1. The denominator polynomial of H(z) has coefficients which need to be known very accurately. Insufficient accuracy of these may even cause one or more poles of H(z) to shift out of the unit circle in the z-plane and cause instability. We conclude that a structure like figure 2.5 is a very sensitive one. This situation can be improved by splitting up the transfer function into second order sections, but the sensitivity problem remains. There are also considerations with respect to propagation of round-off errors for which the cascade filter is disadvantegeous - see Oppenheim [17]. The question arises whether digital structures can be found with sensitivity and stability properties comparable to the continuous LC ladder networks terminated in resistances. In any case, in RC-active circuit design it is known that the structures with the least sensitive behaviour are related to the LC ladder structure [48]. In the continuous case one could think of using differentiators and integrators and program the differential equation between in- and output variables on an analog computer instead of using an LC ladder network terminated in resistances but then the same sensitivity problem arises. On the contrary, continuous LC ladder filters of very high order can be constructed satisfactorily using element values of about 1% accuracy.
At this point we can summarize two essential properties of these filters which clarify their insensitive behaviour.

1. A typical lowpass ladder filter is shown in figure 2.7.

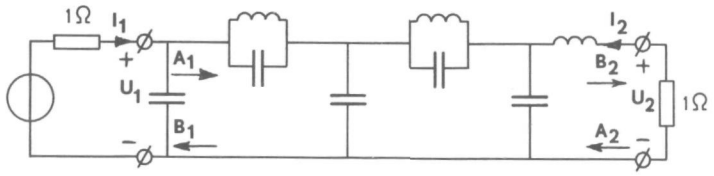


Fig. 2.7. Typical lowpass lossless LC ladder filter (sixth order).

The power transfer of a filter as shown in figure 2.7 is best described by the power scattering variables A and B defined for each port as follows:

$$\left.\begin{aligned} A_i &= \frac{1}{2\sqrt{R_i}}\,(U_i + R_i I_i) \\ B_i &= \frac{1}{2\sqrt{R_i}}\,(U_i - R_i I_i) \end{aligned}\right\} \qquad i = 1,2 \tag{2.17}$$

The resistances R_i in (2.17) are called the reference resistances of each port and are normalised to be 1Ω. The relations between A_i and B_i of the lossless two-port network may be put in matrix form, and the power scattering matrix $S(j\omega)$ is then defined as

$$B = S \cdot A \tag{2.18}$$

In terms of (2.17) and (2.18) we have that $\left|S_{21}(j\omega_i)\right|^2$ defines that part of the maximal available power at the input source which is transferred to the output load for the frequency $f_i = \omega_i/2\pi$. It follows directly that for all ω

$$0 \leq \left|S_{21}\right|^2 \leq 1 \tag{2.19}$$

For passband frequencies f_i where the output is matched to the input we have that

$$\left|S_{21}(j\omega_i)\right|^2 = 1, \tag{2.20}$$

indicating that at frequencies adjacent to f_i $|S_{21}|^2$ can only become smaller.

If we now define a first order sensitivity coefficient S_c to be

$$S_c = \frac{\partial \left|S_{21}\right|^2}{\partial(\text{every element value})} \tag{2.21}$$

then we conclude that for frequencies where (2.20) holds, we obtain

$$S_c = 0. \tag{2.22}$$

Apparently we may have frequencies f_i in the passband of a filter where the sensitivity to element variations is zero. This indicates, roughly,

that the passband characteristic is insensitive. A typical amplitude characteristic, obtainable with the network of figure 2.7, is shown in figure 2.8.

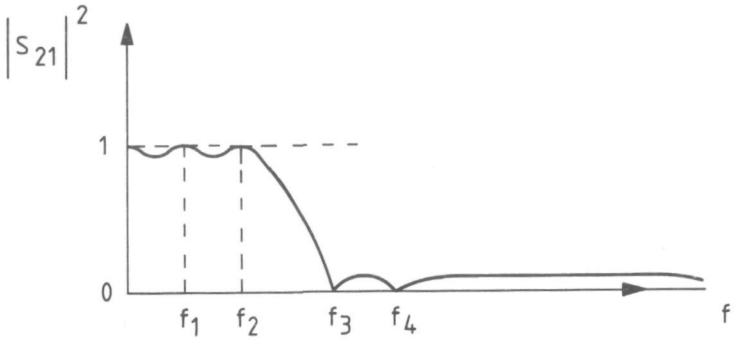


Fig. 2.8. A power transfer characteristic obtainable with the network of figure 2.7.

For three frequencies (0, f_1, f_2) we have optimal power transfer, for three other frequencies (f_3, f_4, ∞) we have zero power transfer. We may conclude that the passband sensitivity is low, due to these frequencies with optimal power transfer and that the stopband is relatively insensitive due to the fact that two frequencies (f_3 and f_4) can be adjusted by trimming the resonant circuits.

2. A rather trivial property of the network of figure 2.7 is that it consists of lossless elements (inductances and capacitances) and resistances. Accordingly, inaccuracies in element values can never lead to instabilities.

We conclude the discussion about the continuous LC ladder network with the observation that apparently the best way known to-day to solve a linear differential equation with selective properties is to split it into zero- and first order equations in such a way that a lossless network is realized in a structure as close to a ladder network as possible.

It has been the idea of Fettweis [19] to introduce the properties of the continuous lossless ladder structure into the theory of digital filters. The procedure to be followed consists of the three steps indicated below.

1. Find a transfer function H(w) from specifications along the imaginary axis in the w-plane as described in section 2.1 using well-known methods from continuous LC filter theory or microwave filter theory.

2. Synthesize this transfer function in the w-plane as described in section 2.2, having the transformer, gyrator inductance, capacitance and unit element available as lossless elements.

3. Transform the scattering matrix description of the network into a computable digital structure using the w-transform and synthesis techniques to be discussed in the following sections and chapters.

Step 3 needs some further explanation.
Instead of using the power scattering matrix formulism it is easier to introduce the voltage scattering parameters A and B to be defined for each port k as:

$$\left.\begin{aligned} A_k &= U_k + R_k I_k \\ B_k &= U_k - R_k I_k \end{aligned}\right\} \qquad (2.23)$$

In (2.23), R_k is the reference resistance, which is a positive constant and in general different for each port k. The use of wave parameters is motivated by following considerations:

1. The properties we want to introduce from continuous LC filters into digital filters rely heavily on the power transfer which is described by wave parameters.

2. The use of the voltage-scattering parameters in addition to the bilinear transform leads to digital structures which are computable. It

turns out (as shown in the next section) that in this way the inductance, capacitance and unit element lead to simple delay elements in the digital case. The Kirchhof relations of the w-plane network produce computable relations at least for the ladder case.
The resulting digital structures are called wave digital structures.

2.4. The translation procedure of elements and interconnections and its properties.[19,31-38]

In this section we consider each element, the interconnections and discuss various properties.

2.4.1. The inductance.

We have the relation $U = w\,L\,I$ (figure 2.9). (2.24)

Applying the bilinear transform leads to

$$U = \frac{z - 1}{z + 1} L.I. \tag{2.25}$$

We now introduce the voltage scattering parameters A and B from (2.23) with $R = L$, (2.26)

which leads to $B = -\frac{1}{z} A.$ (2.27)

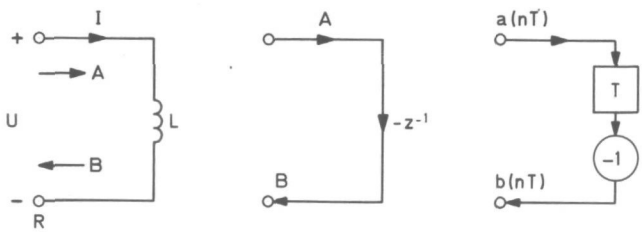


Fig 2.9. The w - plane inductance.

In (2.27) the inductance value L has disappeared, but this value is present in the defining relations of A and B through (2.26). This value will appear again when ports with different values of R in their definitions of A and B have to be connected. This will be discussed later on. We conclude that translation of the inductance leads in this case to the difference equation

$$b(nT) = -a(nT - T). \tag{2.28}$$

2.4.2. The capacitance.

We have (figure 2.10) $U = \frac{1}{wC} I.$ (2.29)

Applying the bilinear transform and choosing the normalizing resistance R in the defining equations of A and B to be

$$R = \frac{1}{C}, \tag{2.30}$$

we obtain $B = \frac{1}{z} A$ (2.31)

which is shown in figure (2.10).

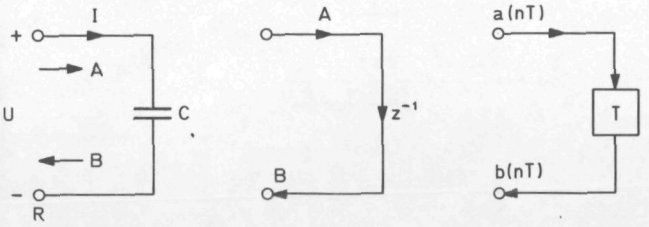


Fig. 2.10. The w - plane capacitance.

2.4.3. The unit element (figure 2.11).

The impedance matrix can be obtained from (2.14). Applying the bilinear transform leads to

$$\left.\begin{aligned} U_1 &= \frac{R(z+1)}{z-1} I_1 + \frac{2R\sqrt{z}}{z-1} I_2 \\ U_2 &= \frac{2R\sqrt{z}}{z-1} I_1 + \frac{R(z+1)}{z-1} I_2 \end{aligned}\right\} \qquad (2.32)$$

This transforms into

$$\left.\begin{aligned} B_1 &= z^{\frac{1}{2}} A_2 \\ B_2 &= z^{\frac{1}{2}} A_1 \end{aligned}\right\} \qquad (2.33)$$

when both normalizing port resistances are chosen equal to R, the impedance value of the unit element.

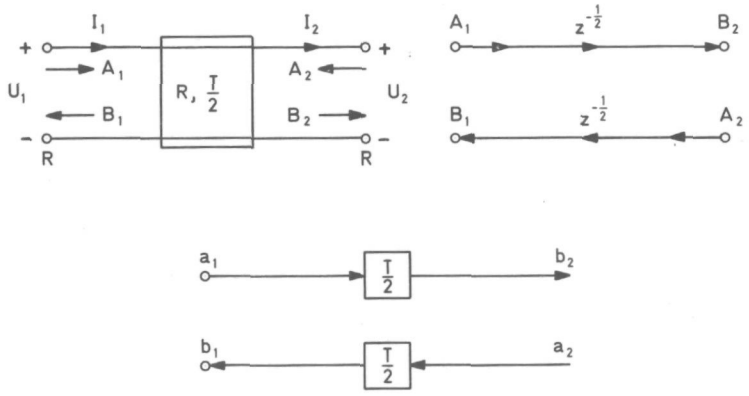


Fig. 2.11. The unit element.

In figure 2.11 we observe that delays $^{T}/_{2}$ occur in translations of structures containing unit elements. Later on, we will show that these delays $^{T}/_{2}$ can be removed and only delays T are left.
By describing the translation of an open- or short-circuited port, the equivalence of a unit element with one port open or short-circuited and a w-plane capacitance or inductance is shown directly.

From figures 2.9, 2.10 and 2.11 we conclude that the frequency dependent elements from the continuous case all lead to very simple digital networks containing delay elements.

2.4.4. Translation of an open or short-circuited port.

The translations follow directly from the defining equations of A and B (with general port resistances) and are given in figures 2.12 and 2.13 respectively.

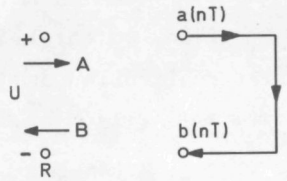


Fig. 2.12. Open port.

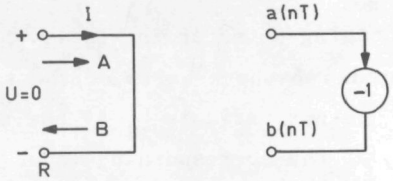


Fig. 2.13. Short-circuited port.

The equivalence between the translation of (i) a capacitance and a unit-element with open port 2 and (ii) of an inductance and an unit-element short-circuited at port 2 is now obvious from the figures 2.10, 2.11, 2.12 and 2.9, 2.11, 2.13.

2.4.5. The transformer (figure 2.14)

We start with the equations

$$\left.\begin{aligned} I_1 &= -nI_2 \ , \\ U_2 &= nU_1 \ . \end{aligned}\right\} \tag{2.34}$$

For the voltage-scattering matrix $\mathbb{S}$ defined by

$$B = \mathbb{S}.A \tag{2.35}$$

we obtain

$$\mathbf{S} = \frac{1}{g_1 + n^2 g_2} \begin{bmatrix} g_1 - n^2 g_2 & 2ng_2 \\ 2ng_1 & -(g_1 - n^2 g_2) \end{bmatrix}. \qquad (2.36)$$

In (2.36), g_1 and g_2 are the normalizing port conductances.
If we now put

$$g_1 = n^2 g_2 \qquad (2.37)$$

then

$$\mathbf{S}_{11} = \mathbf{S}_{22} = 0. \qquad (2.38)$$

So, by choosing R_2 according to (2.35) with R_1 given, we obtain a situation whereby both ports of the transformer realization are reflection-free. The output variable b_1 of the transformer realization is then independent of the corresponding input variable a_1.
The same holds for b_2 and a_2. If a port of some wave digital structure has this property, it will be called "matched".

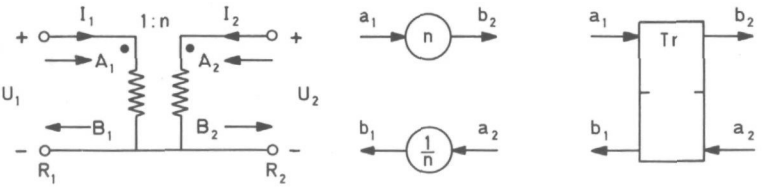


Fig. 2.14. The transformer.

When (2.37) is introduced in (2.36) we obtain the realization which is given in figure 2.14 indicating that both ports are matched. The symbol we use later on for the matched transformer realization is given in figure 2.14.
In general a matched port is pictured as port 1 in figure 2.15.
Is is useful to stress the fact that matching is a port condition (and not a signal property) defined in the corresponding $\mathbf{S}$ matrix.

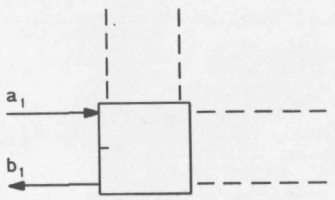


Fig. 2.15. Adapter with port 1 matched.

2.4.6. The gyrator (figure 2.16).

A gyrator is defined by

$$\left.\begin{aligned} U_1 &= -RI_2 \\ U_2 &= RI_1 \end{aligned}\right\} \qquad (2.39)$$

which leads to the voltage-scattering matrix $\mathfrak{S}$ given by

$$\mathfrak{S} = \frac{1}{R^2 g_1 g_2 + 1} \begin{bmatrix} R^2 g_1 g_2 - 1 & -2Rg_2 \\ 2Rg_1 & R^2 g_1 g_2 - 1 \end{bmatrix} . \qquad (2.40)$$

If we put $$R^2 g_1 g_2 = 1 \ , \qquad (2.41)$$

then $\mathfrak{s}_{11} = \mathfrak{s}_{22} = 0$,

which leads directly to the realization of figure 2.16.

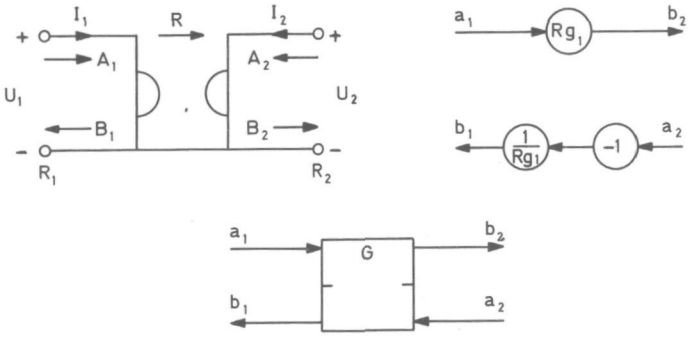


Fig. 2.16. The gyrator.

2.4.7. Voltage source with internal resistance (figure 2.17).

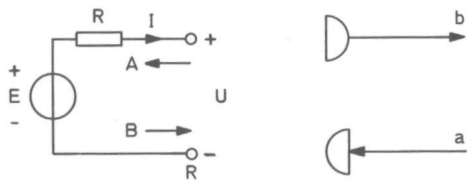


Fig. 2.17. Voltage source with internal resistance R.

We have $E = U + RI$, (2.42)

or: $B = E$, (2.43)

if the normalization is chosen to be R.

Hence, a wave source and sink * represent, in the normalization R, the voltage source with internal resistance R.

* From here on we will use only simple arrows for the source and sink.

2.4.8. Resistive load (figure 2.18).

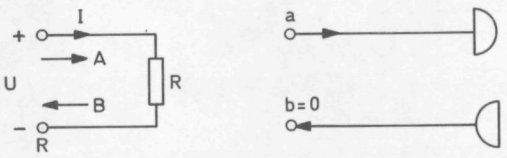


Fig. 2.18. Resistive load R.

The equation

$$U + RI = 0 \tag{2.44}$$

leads to $B = 0$, in the normalization R. (2.45)

Case 2.48 is a special case of case 2.4.7.

2.4.9. Series- or parallel connection of n-ports and their equivalences.

So far, we have only discussed the translation of the most interesting one-port or two-port elements, from the w to the z-domain. However, to obtain translations of complete filter structures these translations of elements have to be interconnected. For that purpose we will now study the translation of general series- and parallel connections of n-ports.

The parallel connection (figure 2.19).

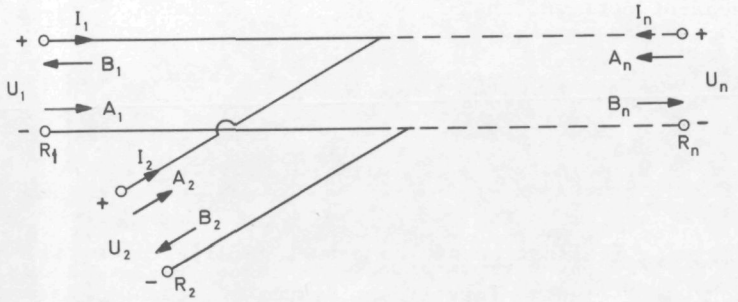


Fig. 2.19. Parallel connection of n ports.

From figure 2.19 we observe that the parallel connection is defined by:

$$U_1 = U_2 = \ldots\ldots\ldots = U_n \qquad (2.46)$$

and $$I_1 + I_2 + \ldots\ldots + I_n = 0.$$

These relations combined with the defining equations of A and B lead to

$$B_\nu = (\alpha_1 A_1 + \alpha_2 A_2 + \ldots\ldots + \alpha_n A_n) - A_\nu \quad , \qquad (2.47.a.)$$

$$\alpha_\nu = \frac{2G_\nu}{G_1 + G_2 + \ldots\ldots + G_n} \quad , \qquad (2.47.b.)$$

$$G_\nu = \frac{1}{R_\nu} \quad , \quad \alpha_1 + \alpha_2 + \ldots\ldots + \alpha_n = 2 \qquad (2.47.c.)$$

$$\nu = 1, 2, \ldots\ldots n. \qquad (2.47.d.)$$

In (2.47) we have n multiplier coefficients α_ν present which depend only on the normalizing port resistances R_ν. It follows directly that in this case

$$0 < \alpha_\nu < 2. \qquad (2.48)$$

However, it also follows that the multiplier coefficients are not mutually independent which means that the coefficient of one port can be eliminated. This port shall be called a dependent port. Choosing n as dependent port we find

$$B_n = A_n - \sum_{\nu=1}^{n-1} \alpha_\nu (A_n - A_\nu)$$

$$B_\nu = B_n + (A_n - A_\nu) \quad , \quad \nu = 1, 2, \ldots\ldots n-1. \qquad (2.49)$$

There remains a realization of the n-port parallel connection using n-1 multiplier coefficients. This linear system of equations expressing B_ν in terms of A_ν as a building block is called an adapter. It "adapts" the various elements to each other. Their different port resistances are to be introduced in (2.47) or (2.49).

The term "matched port" has been introduced when we discussed the transformer and gyrator translations but also a n-port parallel adapter can be made to have a matched port. This, however, entails a condition on the port resistances. Suppose e.g. that port n is matched. From (2.47) we obtain then

$$\left.\begin{aligned} &\alpha_n = 1\ ,\ G_n = G_1 + G_2 + \ldots\ldots + G_{n-1}\ , \\ &\alpha_1 + \alpha_2 + \ldots\ldots\ \alpha_{n-1} = 1,\ \alpha_\nu = \frac{G_\nu}{G_n}\ . \end{aligned}\right\} \qquad (2.50)$$

Because the sum of the multiplier coefficients equals 1, we may choose again a dependent port (except port n) and eliminate one of the multiplier coefficients.

As will be shown later on, adapters with a matched port play an important role in obtaining digital realization which are actually numerically computable. In other words, adapters with a matched port are very helpful in avoiding delay-free loops in the digital realizations.

In figure 2.20 we show the symbol for the n-port parallel adapter for two cases, with or without a matched port.

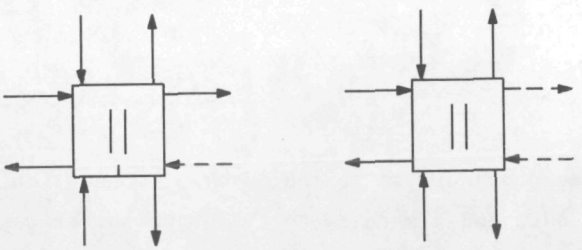


Fig. 2.20. N-port parallel adapter with and without a matched port.

The series connection (figure 2.21).

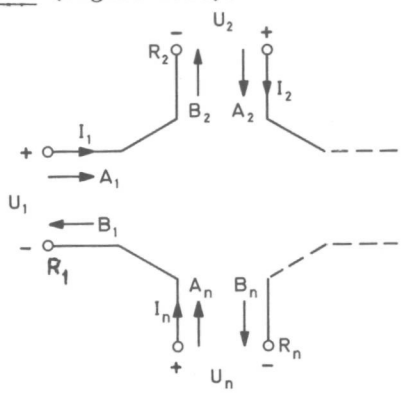


Fig. 2.21. Series connection of n ports.

With reference to figure 2.21, the series connection is defined by

$$\left.\begin{aligned} U_1 + U_2 + \ldots\ldots + U_n &= 0 \\ I_1 = I_2 = \ldots\ldots &= I_n . \end{aligned}\right\} \qquad (2.51)$$

Introducing the voltage scattering parameters, this leeds to

$$B_\nu = A_\nu - \alpha_\nu (A_1 + A_2 + \ldots. + A_n) , \qquad (2.52.a.)$$

$$\alpha_\nu = \frac{2R_\nu}{R_1 + R_2 + \ldots\ldots R_\nu} , \qquad (2.52.b.)$$

$$\alpha_1 + \alpha_2 + \ldots\ldots + \alpha_n = 2, \ \nu = 1, 2, \ldots\ldots n. \qquad (2.52.c.)$$

Following the same procedure as in the parallel connection case we may have a dependent port and a matched port. In the latter case we have (port n is matched)

$$\left.\begin{aligned} &\alpha_n = 1 \ , \ R_n = R_1 + R_2 + \ldots\ldots R_{n-1} \\ &\alpha_1 + \alpha_2 + \ldots\ldots + \alpha_{n-1} = 1 \ , \ \alpha_\nu = \frac{R_\nu}{R_n} \end{aligned}\right\} \qquad (2.53)$$

Again we may choose a dependent port (not port n) and eliminate one of the multiplier coefficients which leaves a structure with n - 2

coefficients, all having the property

$$0 < \alpha_\nu < 1. \tag{2.54}$$

This, of course, holds also for the parallel adapter with a matched port. The general symbol for the series adapter is shown in figure 2.22, again for the two cases.

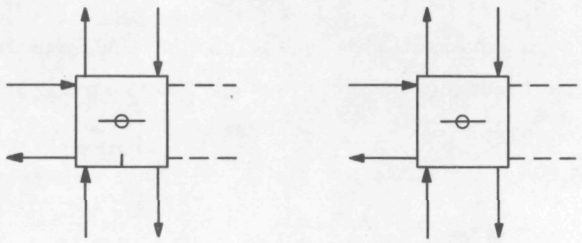


Fig. 2.22. N-port series adapter with and without a matched port.

Equivalences between parallel and series adapters. [52]

Writing

$$A'_\nu = \alpha_\nu A_\nu \ , \ B'_\nu = \alpha_\nu B_\nu \ ,$$

which changes equation (2.47.a.) into

$$B'_\nu = \alpha_\nu (A'_1 + A'_2 + \ldots\ldots + A'_n) - A'_\nu \ . \tag{2.55}$$

Except for a sign reversal, this equivalence is represented pictorially in figure 2.23.

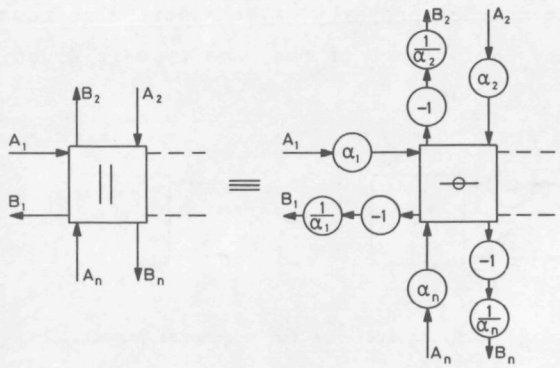


Fig. 2.23. Equivalence obtaining a series adapter from a parallel adapter.

Similarly, we may write

$$A'_\nu = \frac{A_\nu}{\alpha_\nu} \ , \quad B'_\nu = \frac{B_\nu}{\alpha_\nu} \ , \tag{2.56}$$

which changes (2.52.a.) into

$$B'_\nu = A'_\nu - (\alpha_1 A'_1 + \alpha_2 A'_2 + \ldots\ldots + \alpha_n A'_n) \ . \tag{2.57}$$

Except for a sign reversal this equation has the same form as a part of (2.47) which leads to the equivalence shown in figure 2.24.

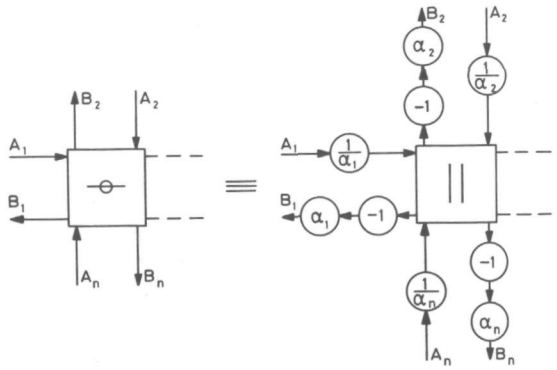


Fig. 2.24. Equivalence obtaining a parallel adapter from a series adapter.

It should be mentioned at this point that the multiplier coefficients remain the same in the equivalences of the figures 2.23 and 2.24. It follows directly that the matched property of some port also remains.
Another elementary equivalence of the same type is given in figure 2.25.

Fig. 2.25. Equivalence for a general N-port.

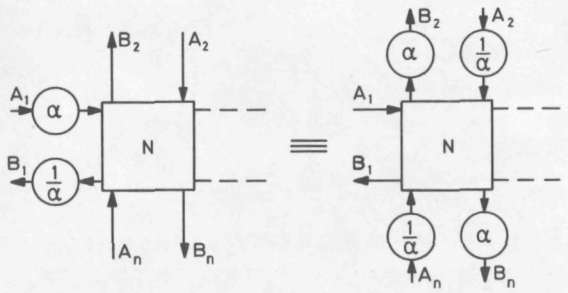


Fig. 2.26. Equivalence for a general N-port.

2.4.10. Two-port and three-port adapters.

The two-port adapter.

To connect two ports with different port resistances, we need a two-port adapter. The two-port adapter can be seen as the simplest parallel adapter (see fig. 2.19) or as the simplest series adapter (see fig. 2.21). Thus, series and parallel adapters are reduced to the same scheme except for the sign convention of voltages and currents.
Taking the parallel adapter convention we obtain from (2.49) with port 2 as dependent port the following relation between A's and B's:

$$\mathcal{S} = \begin{bmatrix} -(1 - \alpha_1) & 2 - \alpha_1 \\ \alpha_1 & 1 - \alpha_1 \end{bmatrix} = \begin{bmatrix} -\alpha & 1 + \alpha \\ 1 - \alpha & \alpha \end{bmatrix}, \qquad (2.58)$$

with $$\alpha_1 = \frac{2G_1}{G_1 + G_2}, \quad \alpha \triangleq 1 - \alpha_1 = \frac{R_1 - R_2}{R_1 + R_2} \qquad (2.59)$$

Regarding A_1 and A_2 as input variables then the two realizations corresponding to (2.58) are given in figure 2.27.

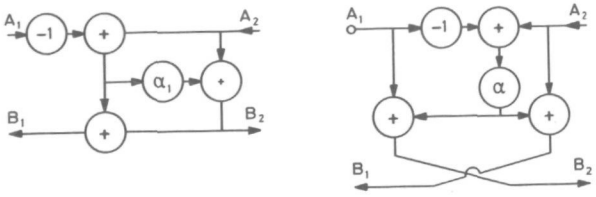


Fig. 2.27. Two flow diagrams for the two-port adapter.

The three-port parallel adapter.

For n = 3 the system of equations from (2.49) becomes

$$\mathfrak{S} = \begin{bmatrix} \alpha_1 - 1 & \alpha_2 & 2 - \alpha_1 - \alpha_2 \\ \alpha_1 & \alpha_2 - 1 & 2 - \alpha_1 - \alpha_2 \\ \alpha_1 & \alpha_2 & 1 - \alpha_1 - \alpha_2 \end{bmatrix} . \qquad (2.60)$$

A flow diagram corresponding to (2.60) is shown in figure 2.28.

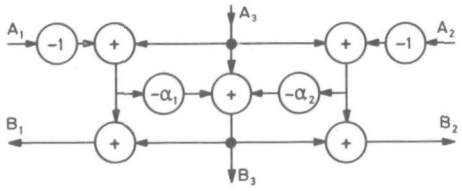


Fig. 2.28. Flow diagram for a three-port parallel adapter.

For a three-port parallel adapter with port 3 matched and port 2 as dependent port we obtain from (2.50),

$$\mathcal{S} = \begin{bmatrix} \alpha_1 - 1 & -\alpha_1 + 1 & 1 \\ \alpha_1 & -\alpha_1 & 1 \\ \alpha_1 & -\alpha_1 + 1 & 0 \end{bmatrix} . \qquad (2.61)$$

$\mathcal{S}_{33} = 0$. indicates that port 3 is matched. A flow diagram corresponding to (2.61) is shown in figure 2.29.

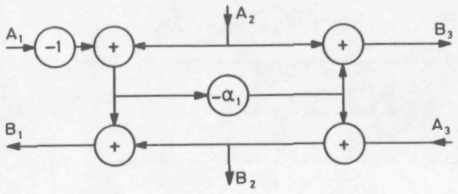


Fig. 2.29. Flow diagram for a three-port parallel adapter with port 3 matched.

The three-port series adapter.

For n = 3 and port 3 as dependent port the system of equations (2.52) can be written as

$$\mathcal{S} = \begin{bmatrix} 1 - \alpha_1 & -\alpha_1 & -\alpha_1 \\ -\alpha_2 & 1 - \alpha_2 & -\alpha_2 \\ \alpha_1+\alpha_2 - 2 & \alpha_1+\alpha_2 - 2 & \alpha_1+\alpha_2 - 1 \end{bmatrix} . \qquad (2.62)$$

A corresponding flow diagram is shown in figure 2.30.

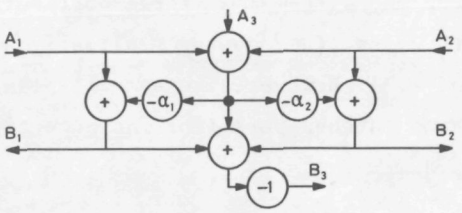


Fig. 2.30. Flow diagram for a three-port series adapter.

For a three-port series adapter with port 3 matched and port 2 as dependent port we obtain using (2.53)

$$\mathbf{S} = \begin{bmatrix} 1 - \alpha_1 & -\alpha_1 & -\alpha_1 \\ \alpha_1 & 1 - \alpha_1 & \alpha_1 \\ -1 & -1 & 0 \end{bmatrix} \tag{2.63}$$

A corresponding flow diagram is shown in figure 2.31.

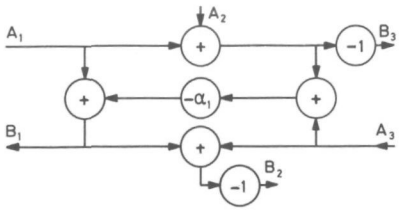


Fig. 2.31. Flow diagram for a three-port series adapter with port 3 matched.

The combination of a three-port adapter and the transformer realization.

As we have seen in section 2.4.5. (figure 2.11) the matched realization of a transformer requires two multiplier coefficients, n and 1/n. For reasons that will become clear later, it is useful to have realizations involving transformers in which only coefficients of value n or 1/n (but not both) are occurring. This is possible if transformer and adapter realizations are combined. We show this in figure 2.32 and 2.33 for the combination of a transformer realization with (i) a three-port parallel adapter and with (ii) a three-port series adapter having a matched port in both cases. The adapter realizations used are given in the figures 2.29 and 2.31. However, the same is possible with adapter realizations having no matched port (for instance figure 2.28 and 2.30).

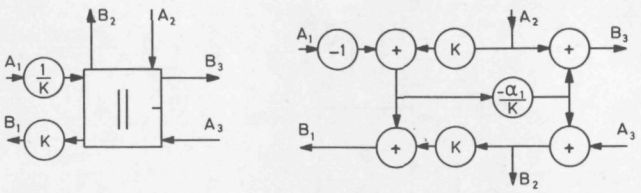


Fig. 2.32. Combination of a three-port parallel adapter (with port 3 matched) and a transformer flow diagram.

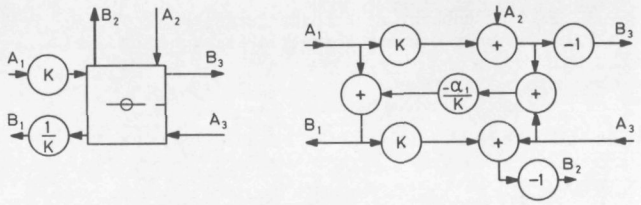


Fig. 2.33. Combination of a three-port series adapter (with port 3 matched) and a transformer flow diagram.

So far, we have given adapter realizations with or without a matched port without explaining why. In section 2.4.14 we will give two examples showing possibilities to avoid delay-free loops. In these examples we use the adapters introduced.

2.4.11. An equivalence concerning adapters and T/2 delay elements.

In section 2.4.3. we have introduced the wave digital translation of the unit element consisting of two T/2 delay elements.
We give two equivalences now, which are helpful to avoid these T/2 delay elements in the wave digital filter structures to be discussed in section 2.4.14.
In figure 2.34 we have a general n-port adapter and to each port the translation of a unit element is connected.

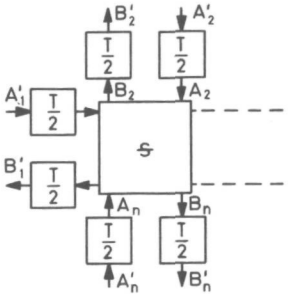


Fig. 2.34. A general n-port adapter with a unit element connected at each port.

The general n-port adapter is described by the matrix relation

$$\underline{B} = \mathfrak{S}.\underline{A}$$

or in terms of $\underline{A}'$ and $\underline{B}'$ (with reference to figure 2.34):

$$z^{\frac{1}{2}}\underline{B}' = \mathfrak{S}(z^{-\frac{1}{2}}\underline{A}'). \tag{2.64}$$

(2.64) can be rewritten in two ways:

First: $\underline{B}' = \mathfrak{S}.(z^{-1}\underline{A}')$, which leads to figure 2.35.
Second: $\underline{B}' = z^{-1}(\mathfrak{S}.\underline{A}')$, which leads to figure 2.36.

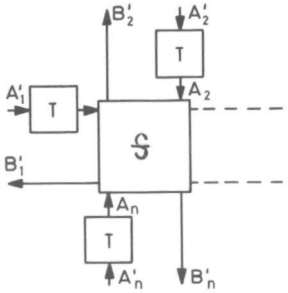


Fig. 2.35. Network which is equivalent to the figures 2.34 and 2.36.

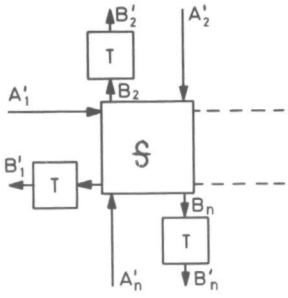


Fig. 2.36. Network which is equivalent to the figures 2.34 and 2.35.

In both cases only delay elements of delay T are left.

2.4.12. The circulator and bridged gyrator.

The 3-port circulator consisting of a gyrator with three ports is shown in figure 2.37 and its wave flow diagram is shown in figure 2.38 with appropriate normalization as indicated in figure 2.37.

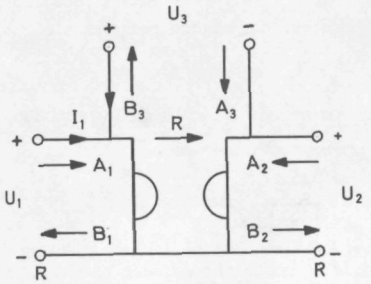


Fig. 2.37. A three-port circulator.

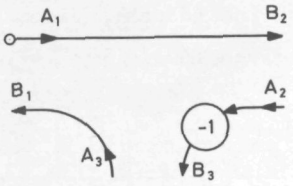


Fig. 2.38.
Flow diagram corresponding to figure 2.37.

The wave digital translation of figure 2.39 is now directly found to be as shown in figure 2.40.

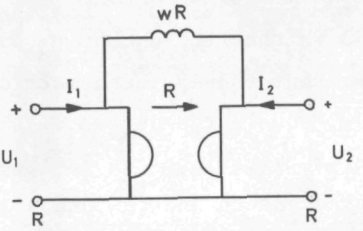


Fig. 2.39.
A circulator bridged by an inductance.

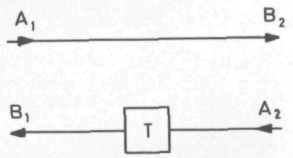


Fig. 2.40.
Flow diagram corresponding to figure 2.39.

2.4.13. Translation of lossless impedances.

In this section we indicate how to translate a lossless impedance in wave digital form.

Each lossless impedance can be synthesized in the Foster-, Cauer- or mixed form. These different circuits lead to different wave digital structures and different multipliers coefficients.

As an example we show in figure 2.41 a general impedance network in the first Cauer form.

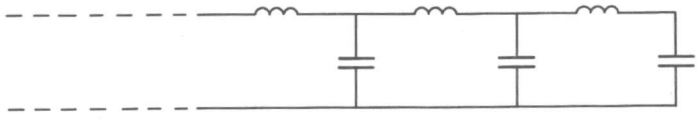


Fig. 2.41. Example of a general lossless impedance network.

By means of the adapters discussed in section 2.4.10 a possible translation is given in figure 2.42.

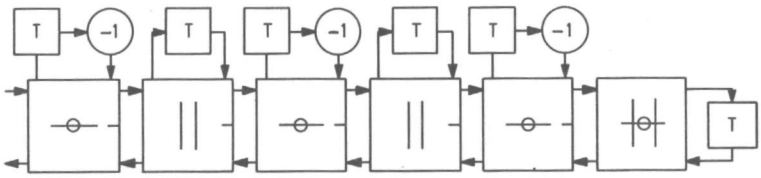


Fig. 2.42. Possible wave digital translation of the network of figure 2.41.

An easy consequence of realization 2.42 is that the number of delay elements and multiplier coefficients present equals the number of elements in figure 2.41 and accordingly, equals the degree of the impedance. We conclude that wave digital impedance realizations can be obtained canonically in both the number of delay elements and the number of multiplier coefficients needed. It can be verified that for other realizations than the first Cauer form the same conclusion holds.
We finally give some translation using unit elements of the parallel resonant circuit as shown in figure 2.3.
First figure 2.43 is obtained after applying the equivalence between the figures 2.34 and 2.36.

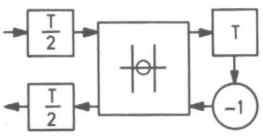


Fig. 2.43. A possible translation of a parallel resonant LC circuit.

Next using figure 2.23a for the two-port adapter we arrive at figure 2.44.

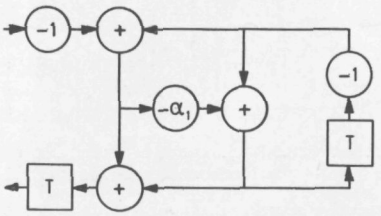


Fig. 2.44. Flow diagram which is equivalent to that of figure 2.43.

2.4.14. An example of a filter.

In this section we will give a simple numerical example of how to obtain a wave digital structure from a given continuous network. The example is given in figure 2.45 and the numerical values are from Saal's tables (C0450 c, θ = 42) [23].

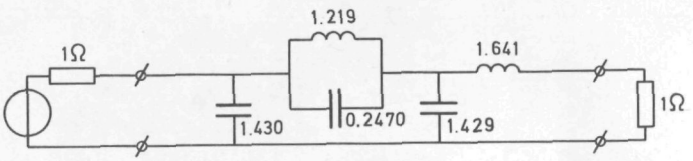


Fig. 2.45. Example of a fourth order elliptic function lowpass filter.

We give two possibilities. In the first one we use additional unit-elements to avoid delay-free loops and in the second one we use the concept of matched ports for the same purpose.

First case.

In this case we add three unit elements of impedance value 1 to the lossless network, one of these at the input port and two at the output port. After having shifted these unit elements into the network by using Kuroda identities (see section 2.2) we arrive at figure 2.46.

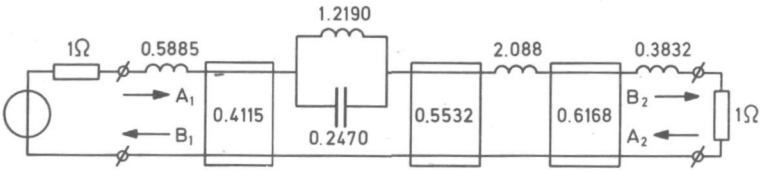


Fig. 2.46. Network which results from figure 2.45 when three unit elements are shifted into the structure.

If we use the adapters of the figures 2.27 and 2.30 and after applying the equivalences from section 2.4.11 we find figure 2.48 (A delay of T/2 at the output B_2 has been neglected). It is readily observed that this flow diagram is numerically realizable.

Second case.

In this case we use the concept of matched ports and obtain figure 2.47. Figure 2.49 shows the flow diagram which is again computable.

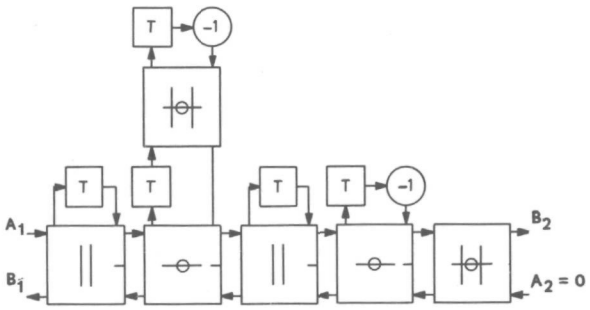


Fig. 2.47. Wave digital translation of the filter of figure 2.45 when the concept of matched ports is used.

The structure of figure 2.46 has not been used in an optimal way. The additional unit elements could have been used more optimally if these had contributed also to the selectivity of the filter. But then the unit elements should have been introduced already in the approximation stage.

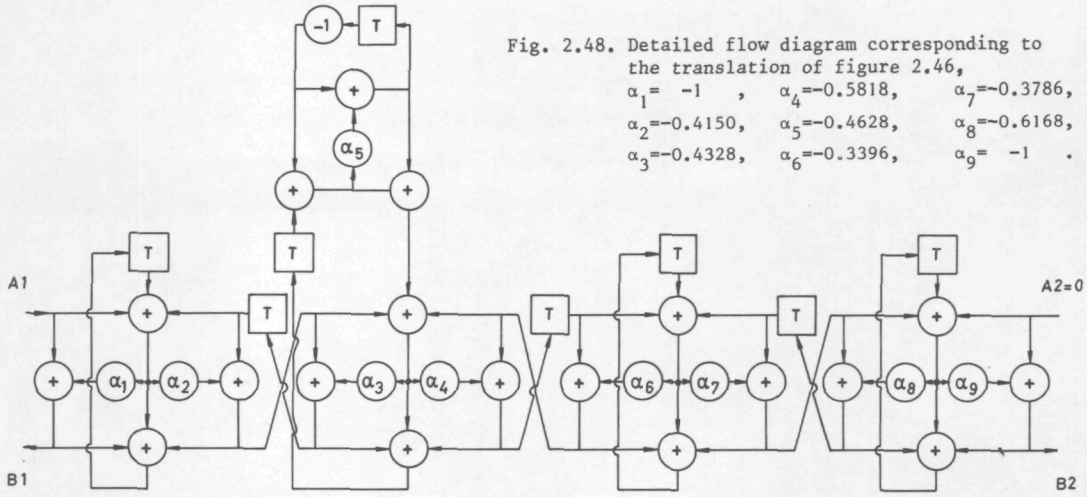


Fig. 2.48. Detailed flow diagram corresponding to the translation of figure 2.46,
α_1= -1 , α_4=-0.5818, α_7=-0.3786,
α_2=-0.4150, α_5=-0.4628, α_8=-0.6168,
α_3=-0.4328, α_6=-0.3396, α_9= -1 .

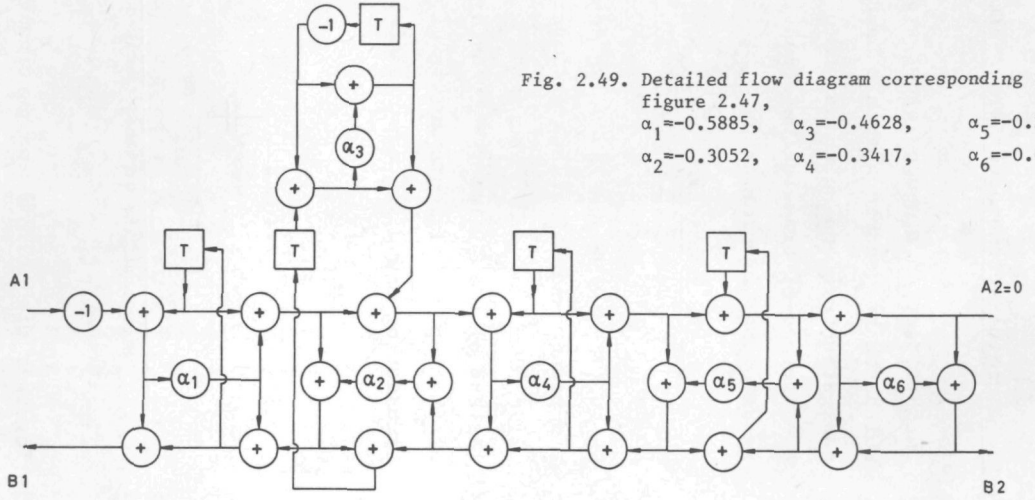


Fig. 2.49. Detailed flow diagram corresponding to figure 2.47,
α_1=-0.5885, α_3=-0.4628, α_5=-0.2192,
α_2=-0.3052, α_4=-0.3417, α_6=-0.6448.

Also in the second case figure 2.49 is not minimal in the sense that the number of delay elements needed could have been reduced by one using the fact that in figure 2.45 a loop of capacitances is present. [53,54]

2.4.15. A useful second-order transformation.

In this section a second order transformation will be briefly described which can be used to obtain a bandpass filter from a wave digital lowpass structure and which has some advantages compared to the normally used method of translating a continuous bandpass filter structure. We have the transformation

$$w \rightarrow \frac{z^2 - \beta z + 1}{z^2 - 1}, \quad \{\beta = 2\cos(\omega_c T),\ -2 \leq \beta \leq 2\} \tag{2.65}$$

which transforms a w-plane lowpass transfer function directly into a z-plane bandpass transfer function.

Instead of the bilinear transform we now use (2.65) in the translation of the w-plane elements and it will be sufficient to illustrate this by translating a w-plane capacitance.

We have $U = \frac{I}{wC}$.

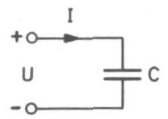


Fig. 2.50. The w-plane capacitance.

Together with (2.65) and putting $C' = 1/R$ we obtain

$$\frac{U}{I} = \frac{z^2 - 1}{z^2 - \beta z + 1} . R . \tag{2.66}$$

Introducing the voltage scattering parameters A and B in the

usual way, we find

$$\frac{B}{A} = \frac{U - RI}{U + RI} = \frac{\frac{U}{I} - R}{\frac{U}{I} + R} = \frac{\beta z - 2}{2z^2 - \beta z} = \frac{-2z^{-2} + \beta z^{-1}}{-\beta z^{-1} + 2} . \qquad (2.67)$$

(2.67) then may be rewritten as

$$B = z^{-1}\{\tfrac{1}{2}\beta(B + A) - z^{-1}A\} , \qquad (2.68)$$

and a realization is shown in figure 2.51

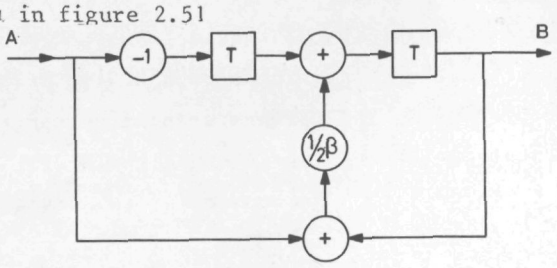


Fig. 2.51. Flow diagram corresponding to (2.69).

In an exactly similar way the w-plane inductance can be handled. In that case figure 2.51 can be used with the input A changed into -A. The translation of frequency-independent elements and connections is not affected by the transformation (2.66).

We may conclude that in any wave digital lowpass filter structure in which the delay elements have only value T (and not T/2), one may replace each of these by the diagram of figure 2.51. This will change the lowpass structure into a bandpass structure. The lowpass multiplier coefficients do not change and are now responsible for bandwidth and selectivity, while only one independent coefficient $\frac{1}{2}\beta$ (appearing as many times as delay elements of delay T in the lowpass filter) is responsible for the center frequency of the bandpass. In this case it will be extra advantageous to have the number of delays T in the lowpass filter minimized to the canonical number (the order of the continuous network) because the number of multiplications and delay elements in the bandpass is directly influenced.

2.5. Sensitivity, losslessness and stability.

2.5.1. Sensitivity.

In section 2.3. the sensitivity and lossless properties of the continuous lossless ladder structure have been introduced as important reasons for the development of the wave digital filters. In this section we will discuss some properties of wave digital filters which are the consequence of insensitivity, losslessness and stability of the translated continuous structures. In section 2.4 we translated these continuous structures using the voltage scattering matrix description. However, the lossless filters itself are described by the power scattering parameters. The relation between these two descriptions needs some attention.

The power scattering parameters are defined by

$$A'_k = \frac{U_k + I_k R_k}{2\sqrt{R_k}}, \qquad B'_k = \frac{U_k - I_k R_k}{2\sqrt{R_k}} \tag{2.69}$$

and the power scattering matrix is given by

$$B' = S' A' \tag{2.70}$$

Comparing this with the voltage scattering parameters where we have (2.23) and

$$B = S \cdot A \tag{2.71}$$

we obtain the relation between S'_{21} and S_{21}.

$$S'_{21} = \left.\frac{B'_2}{A'_1}\right|_{A'_2=0} = \frac{U_2 - I_2 R_2}{\sqrt{R_2}} \cdot \frac{\sqrt{R_1}}{U_1 + I_1 R_1} = \frac{R_1}{R_2} \frac{U_2 - I_2 R_2}{U_1 + I_1 R_1} = \sqrt{\frac{R_1}{R_2}} \cdot S_{21}.$$

So, only if $R_1 = R_2$ does the wave digital network actually realize S'_{21} otherwise $\sqrt{\frac{R_2}{R_1}} \cdot S'_{21}$ is realized. If we now use the definition of

attenuation (in db) as

$$A'_t(j\omega) = -\ 20\ \log|S'_{21}(j\omega)| = -20\ \log\sqrt{\frac{R_1}{R_2}} - 20\ \log\ |S_{21}(j\omega)| = -K + A_t$$

or $\quad A_t = A'_t + K$, where $K = 20\ \log\sqrt{\dfrac{R_1}{R_2}}$ $\qquad (2.72)$

The wave digital translation realizes the same attenuation as the continuous network only if $R_1 = R_2$ (K may be positive or negative).

Now for the continuous network we have

$$\left.\frac{\partial\ A'_t}{\partial\ (\text{some element value})}\right|_{\omega_i} = 0$$

in reflection zero's ω_i located in the passband. Because the multiplier coefficients in the wave digital translations are continuous functions of the element values in the corresponding network we may conclude that

$$\left.\frac{\partial\ (A'_t)}{\partial\ (\text{some multiplier coefficient})}\right|_{\omega_i} = 0. \qquad (2.73)$$

But we have

$$\frac{\partial A_t}{\partial \alpha_k} = \frac{\partial A'_t}{\partial \alpha_k} + \frac{\partial K}{\partial \alpha_k}\ . \qquad (2.74)$$

For that reason it is of importance to discuss $\dfrac{\partial K}{\partial \alpha_k}$.

The effect of variations on the ideal values of multiplier coefficients is of direct importance for instance for the complexity in hardware realizations of digital filters because the multiplier is a complex part of that hardware. When $\dfrac{\partial K}{\partial \alpha_k}$ can be kept small of even zero, then we may conclude that wave digital filters need an accuracy of multiplier coefficients which is comparable to the accuracy of element values needed in lossless, continuous ladder filters. Before indicating ways of making both K and $\dfrac{\partial K}{\partial \alpha}$ from relations (2.72) and (2.74) equal to zero, we observe that in the adapter realizations discussed in sections 2.4.9 and 2.4.10

the number of independent multiplier coefficients is such that if these coefficients are rounded or truncated their deviations from the original values can be translated back into deviations of the element values in the original network. This remains possible in an uncritically wide range. The consequence of this is that the translation of a lossless ladder structure (see the examples in section 2.4.14 for instance) can still be translated back to that same lossless ladder structure (with other element values and terminating resistance, in general) when the multiplier coefficients deviate from their original value. Here we have also the main reason for the use of the voltage scattering parameters as variables instead of the power variables. In the latter case more multiplier coefficients than the degree of freedom would have been needed which leads to the situation that the wave digital filter would only be equivalent to the lossless network (and have comparable properties) if the multiplier coefficients were known with infinite accuracy.

The two examples from section 2.4.14 have both $K \neq 0$ and $\frac{\partial K}{\partial \alpha_i} \neq 0$ because, if we keep the source resistance at 1Ω to fix the impedance level, then the rounding or truncating of the multiplier coefficients causes the element values to change and the load resistance to deviate from 1Ω. We will now indicate two ways of obtaining both $K = 0$ and $\frac{\partial K}{\partial \alpha_i} = 0$.

a. Instead of realizing the transfer function S_{21} (and thus b_2 as output) we may also realize a specified S_{11} (and thus use b_1 as an output). In the latter case the in- and output port of the lossless network are the same and consequently in (2.73) we have $R_2 = R_1$ which means $K = 0$.
   Also, as rounding or truncation of multiplier coefficients does not effect this situation, we have $\frac{\partial K}{\partial \alpha_i} = 0$ [33].

b. In restricting oneself to symmetrical or piece-wise symmetrical networks one has that rounding or truncating multiplier coefficients can be translated back into changes of the lossless elements only.
The load resistances are effected in an identical way which makes $K = 0$ and $\frac{\partial K}{\partial \alpha_i} = 0$. An example of such a network is given in fig. 2.52.

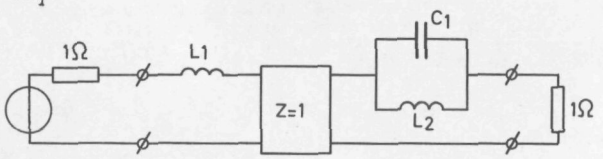


Fig. 2.52. Example of a piece-wise symmetrical network (the use of two three-port adapters with two ports of equal port resistance).

The symbolic translation is shown in figure 2.53.

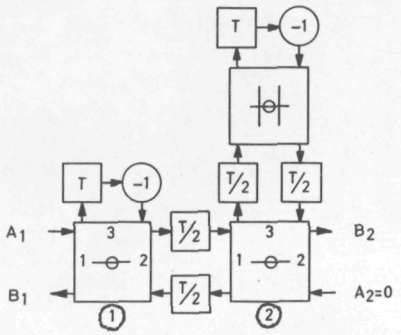


Fig. 2.53. The translation of figure 2.52.

The adapters (1) and (2) in figure 2.53 both have two ports with equal port resistances, which means that in equations (2.52) we have

$$R_1 = R_2 = 1, \quad \alpha_1 = \alpha_2 = \alpha = \frac{2}{2 + R_3} . \tag{2.75}$$

It follows that in figure 2.53 only one multiplication remains per adapter and that rounding α causes only R_3 to change and not R_1 and R_2. This results again in $K = 0$ and $\frac{\partial K}{\partial \alpha_i} = 0$.

A general symmetrical structure having this property will be discussed in chapter 3.

2.5.2. Losslessness.

For a constant passive n-port network the passivity results in

$$\mathbf{U}^T\mathbf{I} \geq 0. \tag{2.76}$$

In which $\mathbf{U}$ and $\mathbf{I}$ are vectors of port voltages and currents.
In terms of voltage scattering parameters we can rewrite (2.76) as

$$(\mathbf{A}^T + \mathbf{B}^T)\mathbf{G}(\mathbf{A} - \mathbf{B}) \geq 0$$

or $$\mathbf{A}^T\mathbf{G}\mathbf{A} - \mathbf{B}^T\mathbf{G}\mathbf{B} \geq 0. \tag{2.77}$$

G is the diagonal matrix of port conductances $g_i (i = 0,1...n)$.
We remark here that (2.76) and (2.77) only express the fact that the n-port network only absorbs energy. For example, for port 1 of the n-port network it follows that

$$(a_1^2 - b_1^2)g_1 \geq 0. \tag{2.78}$$

Introducing the voltage scattering matrix $\mathbf{S}$ in (2.77) it follows that

$$\mathbf{A}^T(\mathbf{G} - \mathbf{S}^T\mathbf{G}\mathbf{S})\mathbf{A} \geq 0 \text{ , for all vectors } \mathbf{A}. \tag{2.79}$$

In the lossless case, we have equality sign for all $\mathbf{A}$ in (2.79) and conclude that

$$\mathbf{G} - \mathbf{S}^T\mathbf{G}\mathbf{S} = \mathbf{0}. \tag{2.80}$$

In the previous section we saw that variations in coefficient values due to rounding or truncation could be translated back into changes of element values in the original continuous filter network including the load resistance. This means in terms of $\mathbf{G}$ and $\mathbf{S}$ satisfying (2.80) that if $\mathbf{S}$ changes into $\mathbf{S}'$ due to coefficient variations, a corresponding $\mathbf{G}'$ can be found such that now $\mathbf{G}'$ and $\mathbf{S}'$ satisfy (2.80).

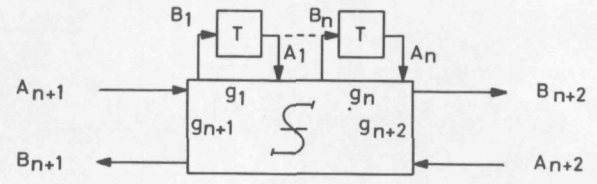


Fig. 2.54. Wave digital translation of an (n+2)-port frequency independent network loaded with n capacitances.

For the general time invariant case any realizations can be brought into the form of figure 2.54 where $\mathfrak{S}$ is a constant voltage scattering matrix defined by:

$$\begin{vmatrix} B_1 \\ \vdots \\ B_n \\ B_{n+1} \\ B_{n+2} \end{vmatrix} = \begin{bmatrix} & & \\ & \mathfrak{S} & \\ & & \end{bmatrix} \cdot \begin{vmatrix} A_1 \\ \vdots \\ A_n \\ A_{n+1} \\ A_{n+2} \end{vmatrix}, \qquad (2.81)$$

If we replace $[B_1 \ldots B_n]^T$, $[A_1 \ldots A_n]^T$, $[B_{n+1}, B_{n+2}]^T$, $[A_{n+1}, A_{n+2}]^T$ by $X^T_{(k+1)}$, $X^T_{(k)}$, $Y^T_{(k)}$, $U^T_{(k)}$ in (2.82) then we obtain for (2.77) in the lossless case:

$$[X^T_{(k+1)}\ Y^T_{(k)}] \begin{bmatrix} G_1 & 0 \\ 0 & G_2 \end{bmatrix} \begin{vmatrix} X_{(k+1)} \\ Y_{(k)} \end{vmatrix} = [X^T_{(k)}\ U^T_{(k)}] \begin{bmatrix} G_1 & 0 \\ 0 & G_2 \end{bmatrix} \begin{vmatrix} X_{(k)} \\ U_{(k)} \end{vmatrix} \qquad (2.82)$$

where $G_1 = \begin{bmatrix} g_1 & & 0 \\ & \ddots & \\ 0 & & g_n \end{bmatrix}$ and $G_2 = \begin{bmatrix} g_{n+1} & 0 \\ 0 & g_{n+2} \end{bmatrix}$ (2.83)

Equation (2.82) leads to

$$X^T_{(k+1)}G_1X_{(k+1)} + Y^T_{(k)}G_2Y_{(k)} = X^T_{(k)}G_1X_{(k)} + U^T_{(k)}G_2U_{(k)} \cdot \qquad (2.84)$$

Each part of (2.84) is a positive quadratic form because the elements of G_1 and G_2 are positive.
We can rewrite (2.84) as

$$X^T_{(k+1)}G_1X_{(k+1)} - X^T_{(k)}G_1X_{(k)} = U^T_{(k)}G_2U_{(k)} - Y^T_{(k)}G_2Y_{(k)} \cdot \qquad (2.85)$$

Equation (2.85) can be interpreted as an energy balance of a general wave digital network. The difference in stored energy in the network between two sampling instants k and k + 1 equals the difference in energy between input and output at instant k. It expresses the losslessness of the network.

2.5.3. Stability in the zero input case.

We discuss shortly the stability for the zero input linear case. The expressions are needed in the discussion of the nonlinear case in section 2.6. Using figure 2.54 and equations (2.77) and (2.78) for the lossless case we write

$$(a_1^2g_1 + \ldots + a_n^2g_n) - (b_1^2g_1 + \ldots + b_n^2g_n) = b^2_{n+1}g_{n+1} + b^2_{n+2}g_{n+2} \cdot \qquad (2.86)$$

In terms of the notations of (2.85) we obtain

$$(g_1X^2_{1(k)} + \ldots + g_nX^2_{(k)}) - (g_1X^2_{1(k+1)} + \ldots + g_nX^2_{n(k+1)} =$$

$$= g_{n+1}y^2_{n+1(k)} + g_{n+2}y^2_{n+2(k)} \cdot \qquad (2.87)$$

We may conclude that the stored energy will decrease and go to zero when k increases. From (2.87) we observe directly that, in the case of the translation of a lossless network without input and output port the stored energy in the wave digital network remains constant.

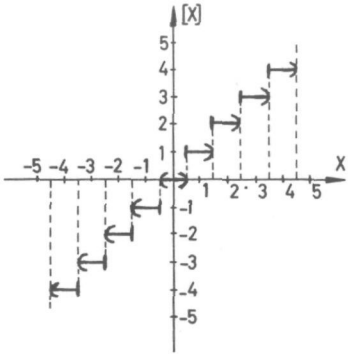
2.6. Nonlinear aspects.

So far in this chapter we have discussed the linear theory of discrete systems and in particular wave digital filters. We will now pay some attention to nonlinear effects in structures which have been developed by linear theory in the form of a computer algorithm or in hardware.
In most implementations variables are represented with a finite number of bits.
The consequence of this is that with a fixed number of decimals or bits, there will be a biggest number (absolute value) and a smallest number (unequal to zero) which can be represented. This restriction e.g. causes nonlinear effects.
Especially in hardware situations where increasing the number of bits for representation of variables means a more complex and in most cases more expensive hardware, it is useful to study the effects of a finite number space for variables.
We will restrict ourselves to calculations in fixed point format, because addition and multiplication are easier to implement than in floating point format.
If we forget, for a moment, the presence of a biggest number (in absolute value), then addition is always performed without error. Only multiplication with a real number (in wave digital filters mostly between -2 and +2) will cause errors because of the necessity of rounding or truncation after the multiplication. The multiplication $y = \alpha.x$ will lead to the result

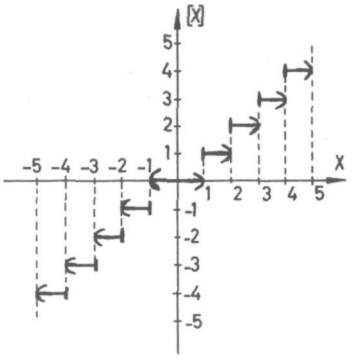
$$y' = [\alpha.x] \ , \qquad (2.88)$$

in which x is an integer, α is a multiplication coefficient, y' is an integer and the brackets denote a rounding or truncation operation. We will mention here three possible definitions of the operation [ ]:

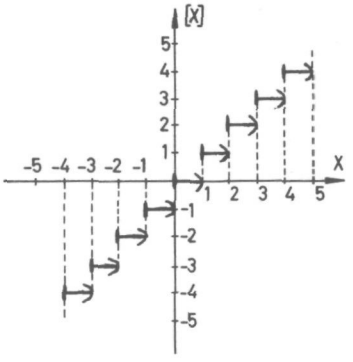
1. rounding (see figure 2.55a).
2. magnitude truncation (figure 2.55b).
3. value truncation (figure 2.55c).



a. Rounding.



b. Magnitude truncation.



c. Value truncation.

Fig. 2.55. Three types of rounding or truncation.

As an example of what such a nonlinearity might cause, a simple series resonant circuit (figure 2.56) is translated into figure 2.57.
$LC = 1$, $\beta = \frac{1}{1+L}$, the nonlinearity is takes as magnitude truncation.

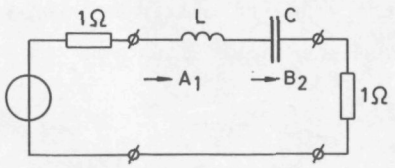


Fig. 2.56. A simple series resonant circuit.

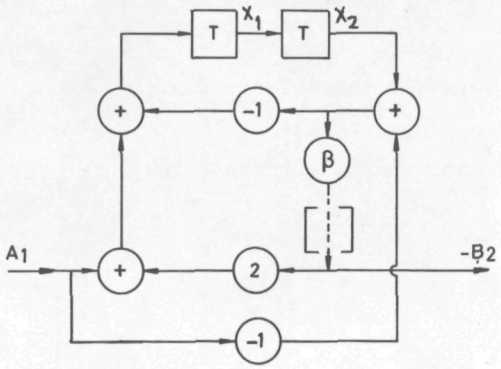


Fig. 2.57. A wave digital translation of figure 2.56

Suppose we calculate the impulse response for $A_1(0) = 16$,

$A_1(kT) = 0 \qquad (k \neq 0)$,

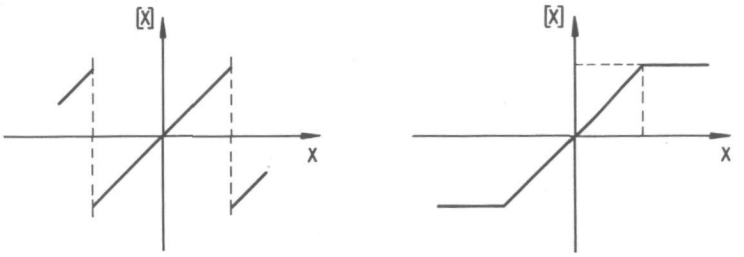
$x_1(0) = x_2(0) = 0, \beta = 1/32$.

The result is given below.

k	0	1	2	3	4	5	6	7	8	9	10	11	→ k
$A_1(kT)$	16	0	0	0	0	0	0	0	0	0	0	0	. . . . .
$x_1(kT)$	0	32	0	-30	0	30	0	-30	0	30	0	-30	. . . . .
$x_2(kT)$	0	0	32	0	-30	0	30	0	-30	0	30	0	. . . . .
$-B_2(kT)$	0	0	1	0	0	0	0	0	0	0	0	0	. . . . .

We observe that the output goes to zero but the state vector does not instead an oscillation is observed. Note that the oscillation in fig. 2.56 is unobservable at the output.
In general, the nonlinearity due to multiplication rounding or truncation will cause deviations from the ideal situation for both the output and state vector.

So far we have discussed the effect of multiplication rounding or truncation which is the only nonlinearity occurring if we suppose that there is no restriction on the largest representable number. If this restriction is violated then the effect of overflow has to be taken into account. This nonlinearity depends again on the arithmetic being used,
we mention here two possible characteristics.
1. The two's-complement characteristic (figure 2.58a).
2. The saturation characteristic (figure 2.58b).



a. Two's complement characteristic. b. Saturation characteristic.

Fig. 2.58. Two possibilities for overflow characteristics.

It will be clear that overflow has a strong nonlinear character.
If a discrete time system is in a overflow state and remains so when the input signal is removed, then the proper operation of the system is destroyed.
First, an easy but important property of this nonlinear behaviour is now given.

Proposition 2.1.

Fluctuations in a discrete-time system without input signal and in which a finite number of bits (or decimals) is available for representation of the variables, have a periodic character.

Proof.

Due to the finite number of bits available for each variable, the whole system can only have a finite number of different states. The transition from state X_k to X_{k+1} is completely defined by the arithmetic used. Suppose that the system reaches the state X_{k+n} after n cycles such that

$$X_{k+n} = X_k.$$

We may conclude directly that

$$X_{k+n+1} = X_{k+1},$$

hence the periodicity is proved. Note that the proof remains valid even when the number space is sufficiently large such that overflow will not occur.

Theorem 2.1.

A sufficient condition for the absence of oscillations in zero-input wave digital filter networks is that

$$\sum_i g_i b_i'^2 \leq \sum_i g_i b_i^2 , \quad i=1,2.....n+2 \tag{2.89}$$

holds for the structure of fig. 2.54. b_i is the ideal output value of port i and b_i' is the output value of port i if errors due to overflow and/or multiplication rounding or truncation are included. The equal sign in (2.89) is sufficient in the case the output values at port n+1 and/or n+2 are unequal to zero.

Proof.

The proof follows directly using the material of section 2.5.3. (2.89) guarantees that the stored energy will decrease and finally reach zero in

finite time because the variables have finite precision.

Proposition 2.2.

Condition (2.89) may be reduced to

$$\left|b_i'\right| \leq \left|b_i\right| . \tag{2.90}$$

Proof.

Condition (2.89) is also satisfied if

$$g_i b_i'^2 \leq g_i b_i^2 \tag{2.91}$$

or:

$$\left|b_i'\right| \leq \left|b_i\right|. \tag{2.92}$$

In the case of overflow oscillation a simple method can be devised so that (2.90) is satisfied. First, care has to be taken that overflow only occurs at the adapter outputs.

Now, both characteristics given in figure 2.58 satisfy automatically (2.90). In the hardware case the two's complement characteristic is the simpler one because front chopping of the two's complement representation of each adapter output variable guarantees (2.90).

The method to be shown for the case of oscillations due to multiplication rounding or truncation (also called limit-cycle oscillations) is slightly more complex. The general method is given by Fettweis [35] but we restrict ourselves here to the two-port and three-port adapters given in this chapter.

Suppose in the fixed point arithmetic case we do not round or truncate following a multiplication but perform all the calculations needed in the flow diagram exactly, then magnitude truncation of all the adapter outputs is sufficient to satisfy (2.90). In hardware however, this is not practical mostly. For this case, the value truncation on a multiplication is the most convenient way to reduce the number of bits. Now for each output of the two-port and three-port adapters given in this chapter, we can state that at most one such error is propagated to each output.

Let the ideal ouput value be b_i. To satisfy (2.90) with the smallest possible error we have to obtain b_i' with b_i' is the magnitude truncated value of b_i. The ouput value which is obtained at the output when value truncation on the multiplication is performed is denoted by b_i''.
Two cases are to be distinguished.

First case.

The error propagates to the output without change of sign.

If

$$b_i'' \geq 0 \longrightarrow b_i' = b_i''. \tag{2.93}$$

Condition (2.90) is satisfied if the output is kept as b_i'', due to the fact that in this case value truncation has the same effect as magnitude truncation.

If

$$b_i'' < 0 \longrightarrow b_i' = b_i'' + \text{"1"}. \tag{2.94}$$

To satisfy (2.90) the output must be modified to $b_i' = b_i'' + \text{"1"}$. By "1" is meant a least significant bit in the representation.

Second case.

The error propagates to the output with change of sign.
We have the following:

$$\left.\begin{aligned} b_i'' > 0 &\longrightarrow b_i' = b_i'' - \text{"1"} \\ b_i'' \leq 0 &\longrightarrow b_i' = b_i''. \end{aligned}\right\} \tag{2.95}$$

If these rules are satisfied then also the existence of limit-cycle oscillations is prevented.
This possibility of suppressing zero-input oscillations is quite a unique property of wave digital filters which indicates an extra advantage of these structures.
For a discussion on a method to implement (2.90) in the floating point arithmetic case we refer to [49].

2.7. Important matrices for lossless two-port networks.

In chapter 4 we will use the Tellegen polynomials A,B,C,D, H and K [56] to prove several two-port equivalences. For that reason we give the Z -, Y -, K - and S-matrices of a lossless two-port network in terms of the Tellegen polynomials.

$$Z = \frac{1}{C}\begin{bmatrix} A & H-K \\ H+K & B \end{bmatrix}, \quad Y = \frac{1}{D}\begin{bmatrix} B & -(H-K) \\ -(H+K) & A \end{bmatrix},$$

$$K = \frac{1}{H+K}\begin{bmatrix} A & D \\ C & B \end{bmatrix}, S = \frac{1}{A+B+C+D}\begin{bmatrix} (D-C)+(A-B) & 2(H-K) \\ 2(H+K) & (D-C)-(A-B) \end{bmatrix} \tag{2.96}$$

The Tellegen polynomials have the following properties:

1. A,B,C,D, H and K are polynomials with real coefficients.
2. A,B and H are even (odd) polynomials and C,D and K are odd (even) polynomials.
3. $AB-H^2 = CD - K^2$.

For convenience we also give the Z -, Y -, and S-matrix description of the unit element.

$$Z = \frac{R}{w}\begin{bmatrix} 1 & \sqrt{1-w^2} \\ \sqrt{1-w^2} & 1 \end{bmatrix}, \quad Y = \frac{1}{Rw}\begin{bmatrix} 1 & -\sqrt{1-w^2} \\ -\sqrt{1-w^2} & 1 \end{bmatrix}, \quad S = \frac{1}{1+\frac{(R^2+1)}{2R}w}\begin{bmatrix} \frac{R^2-1}{2R}w & \sqrt{1-w^2} \\ \sqrt{1-w^2} & \frac{R^2-1}{2R}w \end{bmatrix} \tag{2.97}$$

2.8. Conclusions.

In the previous sections of this chapter material has been brought together which can serve as an introduction to wave digital filter theory. Additional information can be found in [53,54,57,58].

The sensitivity and stability properties of wave digital filters which are the main advantages of these filters have been discussed. The structure of these filters is more complex than the direct realizations of the corresponding transfer functions. Obviously, this is the price to be paid for the excellent properties.

In the next chapters 3 and 4, the ladder restriction on the filter structure is removed in the sense that more general transfer functions are also synthesized in wave digital form.

CHAPTER 3

THE JAUMAN STRUCTURE.

3.1. Introduction.

In chapter 2 the wave digital concept has been introduced. It consists mainly of a translation procedure of resistively terminated lossless LC filters into wave digital form. The procedure is such that a wave digital filter flow diagram results in a number of multipliers which equals the degrees of freedom in the original LC filter. Rounding or truncating the multiplier coefficients is necessary in a practical situation but these deviations from the ideal values can always be translated back into deviations of the elements of the LC filter from their ideal values. Equation (2.80) can be satisfied for the ladder structures discussed sofar (except possibly for the gyrator and transformer). The lossless ladder network is however restrictive in terms of the transfer functions which can be realized. The resistively terminated, reciprocal, lossless LC ladder filter consisting of w-plane elements, can only realize transfer functions with transmission zero's on the imaginary axis in the w-plane. Only in the case the reflection function S_{11} is used instead of the transmission function S_{21}, transfer functions with zero's away from the imaginary axis in the w-plane can be realized.

Of course, lossless LC networks in the non-ladder form can be translated into wave digital form by obtaining a general (n+2)-port adapter from a network consisting of n elements. This general adapter, however, will have a flow diagram not having the property mentioned above when coefficients are rounded or truncated. The number of coefficients will be far more than the degrees of freedom in the original LC network so that a lot of nice

properties are lost. For that reason it is useful to study the possibility of translating other LC filter structures into wave digital form which enable the realization of more general transfer functions than the ladder network. The Jauman structure is such a filter network. The contents of this chapter is based on the author's publication given as reference 37, where the Jauman structure is translated into wave digital form. At the same time, reference 38 announched results on the same subject.
The Jauman structure is a well-known grounded lossless two-port equivalent of the symmetric lattice which can be used as a canonical realization of symmetric, grounded, lossless, reciprocal two-port networks. If Z_{11} and Z_{22} are two-port impedance matrix parameters then by symmetry is meant here:

$$Z_{11} = Z_{22}. \tag{3.1}$$

With this structure complex transmission zeros can be realized, which is not the case with the ladder type structures in which series and shunt arms consist of lossless impedances. It will be shown in this chapter that a transfer function of degree n requires exactly n delay elements and n multipliers in its wave digital flow diagram if the tranfer function can be realized in the Jauman structure. The equivalence of the symmetric lattice and the Jauman structure is given in figure 3.1.

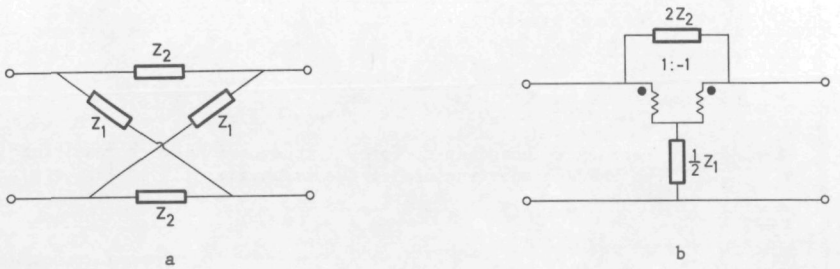


Fig. 3.1. Equivalence between the symmetric lattice (a) and the Jauman structure (b).

For figure 3.1 we have:

$$\left.\begin{aligned} Z_1 &= Z_{11} + Z_{12} = \frac{A + H}{C}\,, \\ Z_2 &= Z_{11} - Z_{12} = \frac{A - H}{C}\,. \end{aligned}\right\} \qquad (3.2)$$

In (3.2) Z_1 and Z_2 are lossless impedances and A, H and C are Tellegen polynomials.

The translation of the Jauman structure is worked out in detail in the following sections.

3.2. Calculation of the unnormalized voltage scattering matrix of the Jauman adapter.

We shall regard the second part of figure 3.1 as a constant reciprocal four-port network of which two ports are terminated in a lossless impedance. This four-port network is shown in figure 3.2.

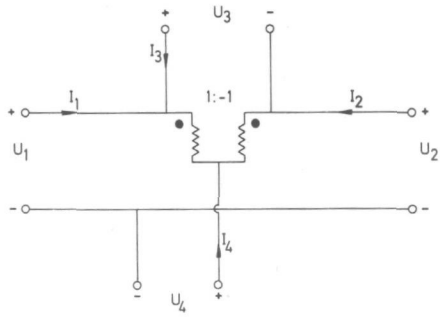


Fig. 3.2. Frequency-independent reciprocal four-port network resulting from the Jauman structure if the impedances $\frac{1}{2}Z_1$ and $2Z_2$ are left away.

The wave digital tranlation of the network of figure 3.2 will be called the Jauman adapter. Applying the usual definitions of the voltage scattering parameters and the following system of equations from figure 3.2

$$\left.\begin{aligned} U_1 - U_2 - U_3 &= 0 \\ U_1 + U_2 - 2U_4 &= 0 \\ I_1 - I_2 + 2I_3 &= 0 \\ I_1 + I_2 + I_4 &= 0 \end{aligned}\right\} \qquad (3.3)$$

we obtain

$$\begin{bmatrix} 1 & -1 & -1 & 0 \\ 1 & 1 & 0 & -2 \\ g_1 & -g_2 & 2g_3 & 0 \\ g_1 & g_2 & 0 & g_4 \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ A_3 \\ A_4 \end{bmatrix} = \begin{bmatrix} -1 & 1 & 1 & 0 \\ -1 & -1 & 0 & 2 \\ g_1 & -g_2 & 2g_3 & 0 \\ g_1 & g_2 & 0 & g_4 \end{bmatrix} \begin{bmatrix} B_1 \\ B_2 \\ B_3 \\ B_4 \end{bmatrix}. \qquad (3.4)$$

This finally leads to the voltage scattering matrix $\underline{S}$ given in (3.6) with

$$N = 4g_1g_2 + 4g_1g_3 + 4g_2g_3 + 4g_2g_3 + 4g_3g_4 + g_1g_4 + g_2g_4. \qquad (3.5)$$

$$\underline{S} = \frac{1}{N} \begin{bmatrix} 4g_1g_2+4g_1g_3-4g_2g_3 & 8g_2g_3-2g_2g_4 & 4g_3g_4+8g_2g_3 & 8g_3g_4+4g_2g_4 \\ -4g_3g_4+g_1g_4-g_2g_3 & & & \\ 8g_1g_3-2g_1g_4 & -4g_3g_4-4g_1g_3+4g_1g_2 & -4g_3g_4-8g_1g_3 & 8g_3g_4+4g_1g_4 \\ & +4g_2g_3-g_1g_4+g_2g_4 & & \\ 8g_1g_2+4g_1g_4 & -8g_1g_2-4g_2g_4 & -4g_1g_2+4g_1g_3+4g_2g_3 & 4g_2g_4-4g_1g_4 \\ & & +4g_3g_4-g_1g_4-g_2g_4 & \\ 8g_1g_3+4g_1g_2 & 8g_2g_3+4g_1g_2 & 4g_2g_3-4g_1g_3 & -4g_1g_2-4g_1g_3-4g_2g_3 \\ & & & +4g_3g_4+g_1g_4+g_2g_4 \end{bmatrix} \qquad (3.6)$$

3.3. Some flow diagrams for the Jauman adapter.

The voltage scattering matrix (3.6) looks quite complicated. The number of degrees of freedom in figure 3.2 is 3 which means that a flow diagram for (3.6) has to be found using 3 independent multipliers in order to satisfy equation (2.82) when the coefficients are rounded or truncated. We may of course reduce the number of multipliers by imposing conditions on the port conductances of figure 3.2 and leading to a simplification of (3.6).
We will discuss three different possibilities. In each case we will start by imposing a different number of conditions on the port conductances. We have not been able to find flow diagrams for (3.6) however, without introducing the symmetry of the structure. This leads to a limited applicability of the wave digital Jauman structure in a larger network.

Theorem 3.1.

A flow diagram corresponding to (3.6) can be found by imposing the following three conditions

$$g_1 = g_2 \ , \qquad \$_{33} = \$_{44} = 0, \tag{3.7}$$

leading to a flow diagram without multipliers having coefficients dependent of the port conductances. Equation (2.80) remains satisfied if g_1 deviates from its original value.

Proof:

The conditions (3.7) imply that no free parameter is left over. From the expression of $\$_{33}$ in (3.6) together with (3.7) we obtain

$$8g_1g_3+4g_3g_4 = 4g_1^2+2g_1g_4 \ . \quad (N \neq 0) \tag{3.8}$$

The same for $\$_{44}$ from (3.6):

$$4g_3g_4+2g_1g_4 = 8g_1g_3+4g_1^2 \ . \quad (N \neq 0) \tag{3.9}$$

Subtracting (3.9) from (3.8) results in

$$4g_3 = g_4. \quad (g_1 \neq 0) \tag{3.10}$$

Equation (3.8) together with (3.10) gives

$$g_1^2 = 4g_3^2, \qquad g_1 = 2g_3 \ . \tag{3.11}$$

(for $g_1 = -2g_3$ we have N = 0).

Finally, (3.6) reduces to (3.12).

$$\mathbf{S}_1 = \begin{bmatrix} 0 & 0 & \frac{1}{2} & 1 \\ 0 & 0 & -\frac{1}{2} & 1 \\ 1 & -1 & 0 & 0 \\ \frac{1}{2} & \frac{1}{2} & 0 & 0 \end{bmatrix} \cdot (g_1=g_2,\ 4g_3=g_4,\ g_1=2g_3) \tag{3.12}$$

A flow diagram corresponding to (3.12) is shown in figure 3.3.

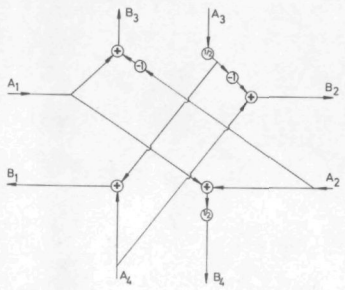


Fig. 3.3. A flow diagram corresponding to (3.12). (A Jauman adapter)

The flow diagram does not contain multipliers with coefficients dependent on port conductances. If g_1 changes into g_1', then g_3' and g_4' follow from (3.7), (3.10) and (3.11) in such a way that equation (2.80) remains satisfied, but now with the accented port conductances. End of proof.

We will now show that the structure resulting from the method of realizing wave digital lattice filters published by Fettweis, Levin and Sedlmeyer [38] is equivalent to the realization of the Jauman adapter given above. For that purpose we introduce the reflectances S_1 and S_2 to be defined as

$$A_3 = S_1 B_3 \qquad \text{and} \qquad A_4 = S_2 B_4 . \tag{3.13}$$

The combination of (3.12) and (3.13) directly results in

$$\left.\begin{aligned} 2B_1 &= S_1(A_1 - A_2) + S_2(A_1 + A_2) \\ 2B_2 &= -S_1(A_1 - A_2) + S_2(A_1 + A_2) \end{aligned}\right\}. \tag{3.14}$$

The expressions (3.14) are the same as the expressions (6) in their paper.

Theorem 3.2.

A flow diagram corresponding to (3.6) can be found by imposing the following two conditions

$$\mathfrak{S}_{11} = \mathfrak{S}_{22} = 0. \tag{3.15}$$

Leading to a flow diagram with one multiplier coefficient. Equation (2.80) remains satisfied if g_1 deviates from its original value. Using this flow diagram leads however in general to incomputable filter structures.

Proof:

The conditions (3.15) lead to the following two expressions:

$$\left.\begin{aligned} 4g_1g_2+4g_1g_3+g_1g_4 &= 4g_2g_3+2g_3g_4+g_2g_4 \\ 4g_1g_2+4g_2g_3+g_2g_4 &= 4g_3g_4+4g_1g_3+g_1g_4 \end{aligned}\right\} \tag{3.16}$$

By subtraction we obtain from (3.16)

$$g_1(4g_3 + g_4) = g_2(4g_3 + g_4), \tag{3.17}$$

which leads to

$$g_1 = g_2. \tag{3.18}$$

(we restrict ourselves to positive conductances)

Equation (3.18) together with (3.16) results in

$$g_1^2 = g_3g_4 . \tag{3.19}$$

Finally, we obtain (3.20).

$$\mathfrak{S}_2 = \begin{bmatrix} 0 & B-C & A+B & 2(A+C) \\ B-C & 0 & -(A+B) & 2(A+C) \\ 2(A+C) & -2(A+C) & B-C & 0 \\ A+B & A+B & 0 & -(B-C) \end{bmatrix}, \tag{3.20}$$

where $$N = 8g_1^2 + 8g_1g_3 + 2g_1g_4, \tag{3.21}$$

and $$A = \frac{4g_1^2}{N}\ ,\ B = \frac{8g_1g_3}{N}\ ,\ C = \frac{2g_1g_4}{N}\ ,\ 2A + B + C = 1. \tag{3.22}$$

If one of the parameters A, B or C is eliminated in turn using (3.22), we obtain 3 possible systems given below.

$$\left.\begin{aligned} B_1 &= (B - C)(A_2 + \tfrac{1}{2}A_3 - A_4) + \tfrac{1}{2}A_3 + A_4 \\ B_2 &= (B - C)(A_1 - \tfrac{1}{2}A_3 - A_4) - \tfrac{1}{2}A_3 + A_4 \\ B_3 &= (B - C)(-A_1 + A_2 + A_3) + A_1 - A_2 \\ B_4 &= (B - C)(\tfrac{1}{2}A_1 + \tfrac{1}{2}A_2 - A_4) + \tfrac{1}{2}A_1 + \tfrac{1}{2}A_2 \end{aligned}\right\} \text{(A eliminated)} \tag{3.23a}$$

$$\left.\begin{aligned} B_1 &= (A + C)(-2A_2 - A_3 + 2A_4) + A_2 + A_3 \\ B_2 &= (A + C)(-2A_1 + A_3 + 2A_4) + A_1 - A_3 \\ B_3 &= 2(A + C)(A_1 - A_2 - A_3) + A_3 \\ B_4 &= (A + C)(-A_1 - A_2 + 2A_4) + A_1 + A_2 - A_4 \end{aligned}\right\} \text{(B eliminated)} \tag{3.23b}$$

$$\left.\begin{aligned} B_1 &= (A + B)(2A_2 + A_3 - 2A_4) - A_2 + 2A_4 \\ B_2 &= (A + B)(2A_1 - A_3 - 2A_4) - A_1 + 2A_4 \\ B_3 &= 2(A + B)(-A_1 + A_2 + A_3) + 2A_1 - 2A_2 - A_3 \\ B_4 &= (A + B)(A_1 + A_2 - 2A_4) + A_4 \end{aligned}\right\} \text{(C eliminated)} \tag{3.23c}$$

Each of the systems (3.23) requires only one distinct multiplier coefficient (B - C, A + C or A +B), although a flow diagram of each of the systems cannot be drawn using only one multiplier. If we eliminate g_4 then the multiplier coefficients can readily be calculated as

$$B - C = 1 - \frac{2g_1}{g_1 + 2g_3},\quad A + C = \frac{g_1}{g_1 + 2g_3},\quad A + B = \frac{2g_3}{g_1 + 2g_3}\ . \tag{3.24}$$

If g_1 changes into g_1', then g_2', g_3' and g_4' follow from (3.18), (3.24) leaving (2.80) satisfied with accented port conductances. Expression (3.19) however leads to difficulties when one of the systems (3.23) is used as a Jauman adapter to realize a wave digital filter. Because the ports 3 and 4 are not matched, it means that g_3 and g_4 are to be fixed by the impedances

$2Z_2$ and $\frac{1}{2}Z_1$. Then also g_1 and g_2 are fixed by (3.19) and (3.18), which means that for instance two-port adapters have to be used to adapt g_1 and g_2 to the values of other elements or adapter port conductances in the general case. This leads to the occurrance of delay-free loops which makes the structure incomputable. End of proof.

Theorem 3.3.

A flow diagram corresponding to (3.6) can be found by imposing the following conditions:

$$g_1 = g_2 = 1. \tag{3.25}$$

It leads to the presence of two different multiplier coefficients. Equation (2.80) remains satisfied.

Proof.

The conditions (3.25) lead to a simplification of (3.5) into

$$N_1 = 4g_3g_4 + 8g_3 + 2g_4 + 4. \tag{3.26}$$

If we now put

$$C_1 = \frac{4g_3g_4}{N_1}\,,\quad D_1 = \frac{8g_3}{N_1}\,,\quad E_1 = \frac{2g_4}{N_1} \text{ and } F_1 = \frac{4}{N_1}\,, \tag{3.27}$$

$$(C_1 + D_1 + E_1 + F_1 = 1)$$

then (3.6) simplifies into (3.28).

$$\mathfrak{S}_3 = \begin{bmatrix} -C_1+F_1 & D_1-E_1 & C_1+D_1 & 2(C_1+E_1) \\ D_1-E_1 & -C_1+F_1 & -(C_1+D_1) & 2(C_1+E_1) \\ 2(E_1+F_1) & -2(E_1+F_1) & C_1+D_1-E_1-F_1 & 0 \\ D_1+F_1 & D_1+F_1 & 0 & C_1-D_1+E_1-F_1 \end{bmatrix}. \tag{3.28}$$

Using (3.28) we can eliminate one of the parameters C_1, D_1, E_1 or F_1 and obtain 4 different systems given below.

$$
\left.\begin{aligned}
B_1 &= (E_1+F_1)(A_1-A_2-A_3) + (D_1+F_1)(A_1+A_2-2A_4) - A_1 + A_3 + 2A_4 \\
B_2 &= (E_1+F_1)(-A_1+A_2+A_3) + (D_1+F_1)(A_1+A_2-2A_4) - A_2 - A_3 + 2A_4 \\
B_3 &= 2(E_1+F_1)(A_1-A_2-A_3) + A_3 \\
B_4 &= (D_1+F_1)(A_1+A_2-2A_4) + A_4
\end{aligned}\right\} \quad (3.29a)
$$

(C_1 eliminated)

$$
\left.\begin{aligned}
B_1 &= (C_1+E_1)(-A_1-A_2+2A_4) + (E_1+F_1)(A_1-A_2-A_3) + A_2 + A_3 \\
B_2 &= (C_1+E_1)(-A_1-A_2+2A_4) + (E_1+F_1)(-A_1+A_2+A_3) + A_1 - A_3 \\
B_3 &= 2(E_1+F_1)(A_1-A_2-A_3) + A_3 \\
B_4 &= (C_1+E_1)(-A_1-A_2+2A_4) + A_1 + A_2 - A_4
\end{aligned}\right\} \quad (3.29b)
$$

(D_1 eliminated)

$$
\left.\begin{aligned}
B_1 &= (C_1+D_1)(-A_1+A_2+A_3) + (D_1+F_1)(A_1+A_2-2A_4) - A_2 + 2A_4 \\
B_2 &= (C_1+D_1)(A_1-A_2-A_3) + (D_1+F_1)(A_1+A_2-2A_4) - A_1 + 2A_4 \\
B_3 &= 2(C_1+D_1)(-A_1+A_2+A_3) + 2A_1 - 2A_2 - A_3 \\
B_4 &= (D_1+F_1)(A_1+A_2-2A_4) + A_4
\end{aligned}\right\} \quad (3.29c)
$$

(E_1 eliminated)

$$
\left.\begin{aligned}
B_1 &= (C_1+D_1)(-A_1+A_2+A_3) + (C_1+E_1)(-A_1-A_2+2A_4) + A_1 \\
B_2 &= (C_1+D_1)(A_1-A_2-A_3) + (C_1+E_1)(-A_1-A_2+2A_4) + A_2 \\
B_3 &= 2(C_1+D_1)(-A_1+A_2+A_3) + 2A_1 - 2A_2 - A_3 \\
B_4 &= (C_1+E_1)(-A_1-A_2+2A_4) + A_1 + A_2 - A_4
\end{aligned}\right\} \quad (3.29d)
$$

(F_1 eliminated)

We observe that each possibility requires 2 multiplier coefficients. We have

$$
\left.\begin{aligned}
C_1+D_1 &= \frac{2g_3}{2g_3+1} & D_1+F_1 &= \frac{2}{g_4+2} \\
C_1+E_1 &= \frac{g_4}{g_4+2} & E_1+F_1 &= \frac{1}{2g_3+1}\,.
\end{aligned}\right\} \quad (3.30)
$$

The result of rounding or truncating two of these coefficients can be translated back into deviations of g_3 and g_4 from their ideal values. Equation (2.80) remains satisfied using these new values. End of proof.

A number of flow diagrams have been obtained above for the Jauman adapter. It gives some flexibility in the choice of flow diagram and multiplier coefficients to be used.

3.4. Some properties of the Jauman structure.

In this section we give some specific properties of the Jauman structure, which make it a rather interesting alternative to the ladder structure. Also the applicability of the Jauman network in a larger filter structure is discussed briefly.
We start with the following theorem.

Theorem 3.4:

If the degree of the transfer function to be implemented using the Jauman structure equals n, then a flow diagram using n delay elements and n multiplier coefficients can always be given. (The structure is canonic in terms of delay elements and multiplier coefficients).

Proof:

It is a property of the Jauman network of figure 3.1 that the sum of the degrees of the impedances $Z_1(n_1)$ and $Z_2(n_2)$ equals n. Now, in section 2.4.13 it has been shown that a lossless impedance of order n_1 (n_2) can be realized using n_1 (n_2) unit elements which transform into n_1 (n_2) delay elements ($n_1+n_2=n$). In the wave digital translation of these impedances $(n_1-1)+(n_2-1)$ two-port adapters (using the same amount of multipliers) are needed. In the case the Jauman adapter from theorem 3.1 is used, two two-port adapters are needed in addition to connect the impedance translations. A total of $(n_1-1)+(n_2-1)+2=n$ multipliers results. A similar situation arises in the case of the Jauman adapters from theorem 3.3. End of proof.

Due to the inherent symmetry of the Jauman structure a property results which has already been discussed in section 2.5.1 concerning sensitivity. Because for the Jauman adapters found always the condition $g_1 = g_2$ holds, we have in terms of section 2.5.1 that $K = 0$ and $\delta K/\delta\alpha_k = 0$ no matter what output (B_1 or B_2) is chosen.

A third nice property of the wave digital Jauman structure can be mentioned. The flow diagram is relatively simple (it uses less additions/subtractions in general) compared with true ladder realizations of the same transfer function. A disadvantage of the wave digital Jauman structures as discussed above is the limited applicability as symmetric part of a larger filter structure. We mention two possibilities by showing two examples.

Example 1: The continuous network is shown in figure 3.4 and its wave digital translation in figure 3.5. The Jauman adapter as developed in theorem 3.1 is used here. The entire network is symmetric and could have been realized in the Jauman structure as a whole.

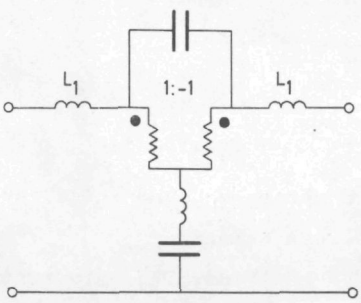


Fig. 3.4. The Jauman structure as a part of a larger symmetrical network.

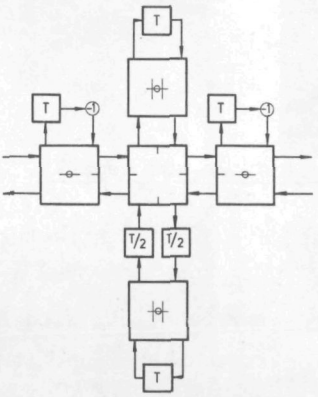


Fig. 3.5. A wave digital translation of figure 3.4.

Example 2: We have the figures 3.6 and 3.7. Here the Jauman network is connected to the rest of the circuit by means of two unit elements of equal impedance. However, the presence of these two unit elements makes the optimal synthesis procedure for such a network more difficult.

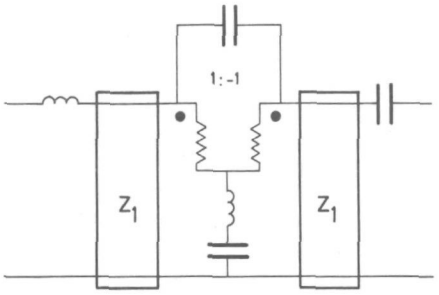


Fig. 3.6. The Jauman structure as part of a larger network using two unit elements.

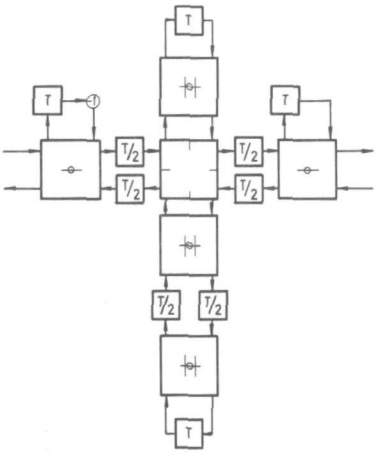


Fig. 3.7. A wave digital translation of figure 3.6.

3.5. Conclusions and remarks.

1. The wave digital structure, given in this chapter, is canonic in terms of the number of delay elements and multipliers needed.
2. Transfer functions with complex zeros can be realized. The only restriction is that the function is realizable as a scattering transfer (or reflection) function of the symmetrical and reciprocal Jauman network consisting of w-plane elements.
3. The wave digital structure given here, is less complex in terms of the number of arithmetical operations needed, compared with a wave digital ladder network of the same order. Increasing the order of the Jauman network by 2, leads to two extra two-port adapters. The same for a true ladder wave digital filter network leads to two extra three-port adapters and one two-port adapter.
4. Only the adjustability of transmission zeros is lost. The sensitivity

property in the passband is the same as in a ladder network, in the stop-band the sensitivity is worse.

5. Wave digital Jauman networks with very simple multiplier coefficients and useful filter characteristics have been obtained [37,38]. An example of such a filter has been constructed using TTL integrated circuits. Details are given in reference 37.

CHAPTER 4

WAVE DIGITAL CASCADE SYNTHESIS

The wave digital networks discussed sofar in the chapters 2 and 3 have certain restrictions on the transfer function which can be realized.
In chapter 2 we have been mainly concerned with the translation of ladder type networks consisting of w-plane elements into wave digital form. The ladder structure, however, is only capable of realizing transmission zeros on the imaginary axis of the w-plane. In the case n unit elements are present in the ladder structure we have n factors $(1-w^2)^{\frac{1}{2}}$ present in the numerator of the transfer function. Transmission zeros anywhere in the w-plane can be realized using the Jauman structure discussed in chapter 3 but in this case we have the restriction that the w-plane network has to be reciprocal and symmetrical ($Z_{11}=Z_{22}$).
It is the purpose of this chapter to indicate methods of realizing general transfer functions. The structures searched for, should have the following properties:

1. Canonical in terms of delay elements T.
2. Minimal in the number of independent multiplier coefficients.
3. Computability.
4. Losslessness.

The method which is given in this chapter uses the approach developed in the chapters 2 and 3. This approach is to translate analog, lossless networks into wave digital structures by using adapters and delay elements as given in chapter 2.
The material given here has already been published in references 40 and 41.

The method is only partially succesful as far as the properties mentioned above are concerned. The structures found are computable, but only passivity instead of losslessness is guaranteed. These properties are obtained by introducing extra unit elements in the translated analog networks. After publication of the method a number of authors have attacked the same problem (or parts of it) using the same approach in order to try avoiding the need of extra unit elements and/or a smaller number of multipliers [59-61].

Recently, a second approach has been published [62,63]. In this case the transfer function to be synthesized is also the S_{21} of a scattering matrix. But now the corresponding scattering transfer matrix is directly factorized into first and second order parts in the z-domain. The method leads to canonical, computable and passive digital structures.

In this chapter, however, the first approach is taken.

In the theory of lossless two-port networks, a synthesis method by means of cascade factorization of the scattering transfer matrix is well-known [64]. In the rest of this chapter we will assume knowledge of this method. Each transfer function which is realizable as a transfer function of a doubly terminated lossless two-port network can be realized using cascaded sections of the zeroth, first, second and fourth order. Fettweis [64] gives the corresponding networks. In this chapter we will give wave digital translations of those networks (or of closely related networks). It turns out in [64] that an infinite number of solutions of the synthesis problem exists, we will concentrate specifically on those sections for which

$$S_{21}(w)\Big|_{w=0} = 1 \qquad (4.1)$$

holds.

4.1 Zero order sections.

In this case we have the gyrator and the transformer. For both sections wave digital realizations have already been given in chapter 2.

4.2 First order sections.

4.2.1 First order reciprocal sections.

The first order reciprocal sections consisting of a simple series (or parallel) inductance or capacitance can be realized using methods already available in chapter 2.

4.2.2 First order non-reciprocal sections.

Referring to (4.1) it is sufficient to consider the section shown in figure 4.1. All other first order non-reciprocal sections can be reduced to zero order sections in cascade with figure 4.1.

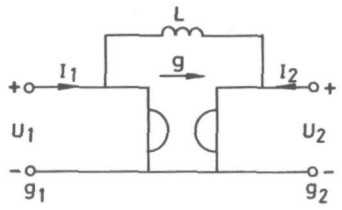


Fig. 4.1. First order non-reciprocal section.

The Tellegen polynomials corresponding to the section of figure 4.1 are:

$$\left.\begin{aligned} &A = B = H = 1, \\ &C = wLg^2,\ D = wL,\ K = wLg. \end{aligned}\right\} \qquad (4.2)$$

We give first two direct translations of figure 4.1.

(1):A direct translation of figure 4.1 into wave digital form using the adapters introduced sofar is given in figure 4.2. However it turns out that this network is numerically unrealizable because of the presence of delay-free loops.

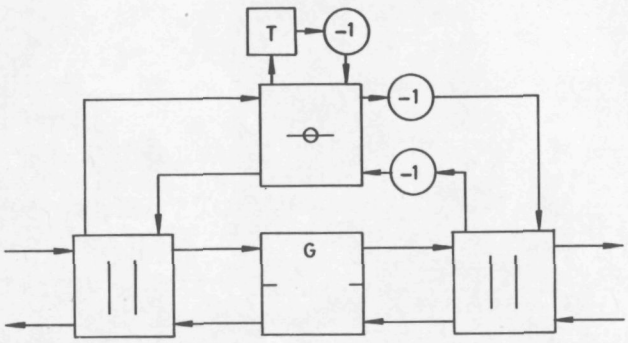


Fig. 4.2. Direct wave digital translation of the network of figure 4.1.

(2):Another attempt can be made to translate figure 4.1 into a computable wave digital form. For that purpose we will use figures 2.39 and 2.40 from chapter 2. We copy figure 4.1 as shown in figure 4.3. If we have the condition in figure 4.1

$$Lg < 1, \tag{4.3}$$

then we may define

$$L_1 g = 1 \quad \text{with } L_1 < L \text{ (fig. 4.3)} \tag{4.4}$$

Using figure 2.40 we obtain figure 4.4 as the wave digital translation of figure 4.3. However, we have to conclude that this structure is numerically unrealizable too.

A possible solution to the problem illustrated above turns out to be the introduction of extra delay in the network by means of a unit element. We will now show that the network of figure 4.6 can be made equivalent to the one of figure 4.5 and that it is realizable numerically. We now show the equivalence by expressing the elements of figure 4.6 in terms of the elements of figure 4.5.

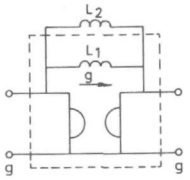


Fig. 4.3. The inductance from the section of fig. 4.1 has been split such that (4.4) holds for L_1.

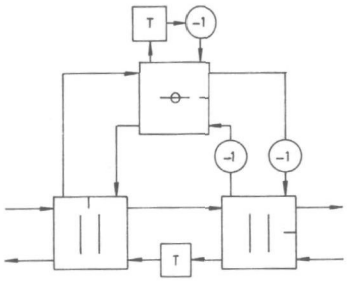


Fig. 4.4. Wave digital translation of the network of figure 4.3.

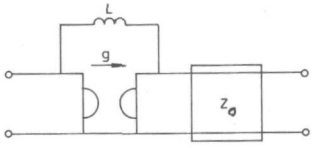


Fig. 4.5. The section of fig. 4.1 cascaded with a unit element.

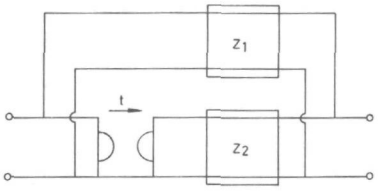


Fig. 4.6. Network which is equivalent to that of fig. 4.5.

Theorem 4.1.

The structure of fig. 4.6 is equivalent to fig. 4.5 if

$$z_1 = z_0 + L,\quad z_2 = \frac{z_0(z_0 + L)}{L} \quad \text{and} \quad t = \frac{gL}{z_0+L}$$

Proof:

A simple calculation shows that the chain matrix K of fig. 4.5 is given by:

$$K = \frac{1}{1 + wLg}\begin{bmatrix} 1 & wL \\ wLg^2 & 1 \end{bmatrix} \cdot \frac{1}{\sqrt{1 - w^2}}\begin{bmatrix} 1 & wz_0 \\ \frac{w}{z_0} & 1 \end{bmatrix} =$$

$$= \frac{1}{(1 + wLg)\sqrt{1-w^2}}\begin{bmatrix} 1 + \frac{L}{z_0}w^2 & (z_0+L)w \\ (Lg^2 + \frac{1}{z_0})w & (z_0+Lg^2)w^2+1 \end{bmatrix} = \frac{1}{H' + K'}\begin{bmatrix} A' & D' \\ C' & B' \end{bmatrix}$$

(4.5)

On an admittance basis the polynomial system of (4.5) can be partitioned as follows:

$$\left.\begin{aligned}
\frac{A'}{D'} &= \frac{1 + w^2\frac{L}{z_0}}{(z_0 + L)w} = \frac{1}{(z_0 + L)w} + \frac{\frac{L}{z_0}w}{z_0 + L} = \frac{A_1}{D_1} + \frac{A_2}{D_2} \\
\frac{B'}{D'} &= \frac{1+z_0Lg^2w^2}{(z_0 + L)w} = \frac{1}{(z_0 + L)w} + \frac{z_0Lg^2w}{z_0 + L} = \frac{B_1}{D_1} + \frac{B_2}{D_2} \\
\frac{H\pm K}{D'} &= \frac{(1\pm wLg)\sqrt{1 - w^2}}{(z_0 + L)w} = \frac{\sqrt{1 - w^2}}{(z_0 + L)w} \pm \frac{Lg\sqrt{1 - w^2}}{z_0 + L} = \frac{H_1}{D_1} \pm \frac{K_2}{D_2}
\end{aligned}\right\} \qquad (4.6)$$

The chain matrix K_1 of the first part of (4.6) is given as

$$K_1 = \frac{1}{\sqrt{1 - w^2}} \begin{bmatrix} 1 & (z_0 + L)w \\ \frac{w}{z_0 + L} & 1 \end{bmatrix} . \qquad (4.7)$$

Clearly, (4.7) is the chain matrix of a unit element z_1 with

$$z_1 = z_0 + L. \qquad (4.8)$$

The chain matrix K_2 of the second part of (4.6) can be found to be

$$K_2 = \frac{1}{\sqrt{1 - w^2}} \begin{bmatrix} \frac{w}{gz_0} & \frac{z_0 + L}{Lg} \\ \frac{Lg}{z_0 + L} & z_0gw \end{bmatrix} = \qquad .$$

$$= \begin{bmatrix} 0 & \frac{z_0 + L}{gL} \\ \frac{gL}{z_0 + L} & 0 \end{bmatrix} \cdot \frac{1}{\sqrt{1 - w^2}} \begin{bmatrix} 1 & \frac{wz_0(z_0+L)}{L} \\ \frac{wL}{z_0(z_0 + L)} & 1 \end{bmatrix} \qquad (4.9)$$

which indicates the cascading of a gyrator with a gyration conductance t and a unit element z_2 with

$$t = \frac{gL}{z_0 + L} \quad \text{and} \quad z_2 = \frac{z_0(z_0 + L)}{L} \ . \tag{4.10}$$

We conclude that z_1 and z_2 are positive and that t has the same sign as g.

End of proof.

The wave digital translation of fig. 4.6 is shown in fig. 4.7. It requires 5 multipliers. Using fig. 2.32 the gyrator multipliers can be combined with the parallel adapter. This results in 4 essentially different multiplier coefficients.

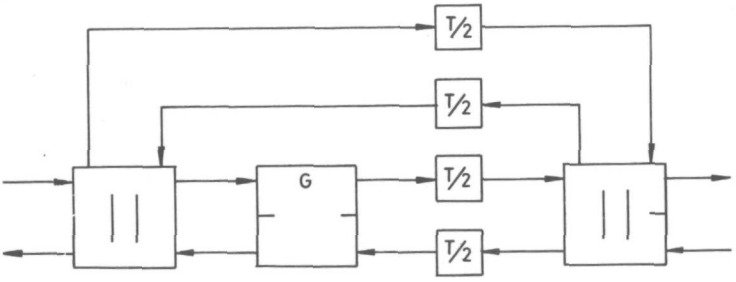


Fig. 4.7. Wave digital translation of the network of fig. 4.6.

We remind here that the transfer function of figure 4.6 is of the following general form:

$$S_{21} = \frac{(a_1 w + 1)\sqrt{1 - w^2}}{b_1 w^2 + b_2 w + 1} \ , \tag{4.11}$$

which shows that 3 different coefficients are present.
Later on in this chapter we will discuss further properties of figure 4.7. In any case, no delay-free loops are present so that the structure is numerically realizable.

4.3. Second order sections.

4.3.1. Second order reciprocal sections.

The second order reciprocal sections consisting of simple series (or parallel) resonant circuits are realized using elementary methods. There remains the section shown in figure 4.8. All other second order reciprocal sections can be reduced to figure 4.8 in cascade with zero order sections.

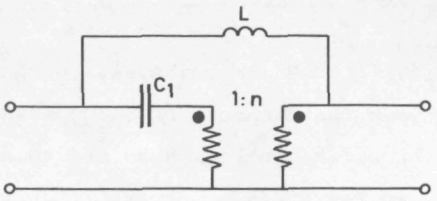


Fig. 4.8. Second order reciprocal section.

The corresponding Tellegen polynomials are given as

$$\left.\begin{aligned} A &= LC_1w^2 + n_1^2 & C &= C_1(n_1 - 1)^2w \\ B &= n_1^2LC_1w^2 + n_1^2 & D &= n_1^2Lw \\ H &= n_1LC_1w^2 + n_1^2 & K &= 0. \end{aligned}\right\} \qquad (4.12)$$

In order to find a numerically realizable structure we cascade a unit element with figure 4.8 as shown in figure 4.9 and prove the equivalence with figure 4.10 by expressing the elements of figure 4.10 in terms of those of figure 4.9.

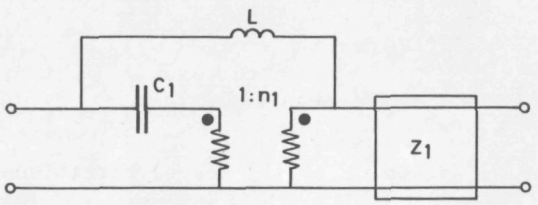


Fig. 4.9. The section of fig. 4.8 cascaded with a unit element.

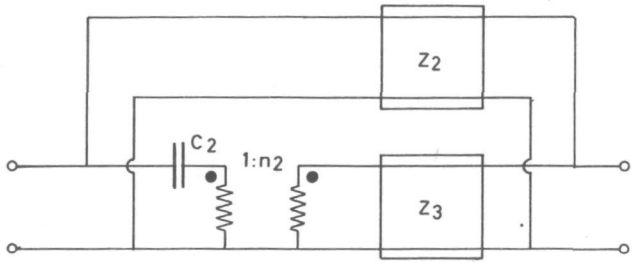


Fig. 4.10. Network which is equivalent to that of fig. 4.9.

Theorem 4.2.

The network of fig. 4.9 is equivalent to that of fig. 4.10 if relations between the elements of both networks hold. Positive values of C_1, L and z_1 in fig. 4.9 lead to positive values of C_2, z_2 and z_3 in fig. 4.10.

Proof.

The chain matrix description of fig. 4.9 is calculated as follows:

$$K_1 = \frac{1}{n_1 LC_1 w^2 + n_1^2} \begin{bmatrix} LC_1 w^2 + n_1^2 & n_1^2 Lw \\ C_1 (n_1 - 1)^2 w & n_1^2 LC_1 w^2 + n_1^2 \end{bmatrix} \cdot \frac{1}{\sqrt{1 - w^2}} \begin{bmatrix} 1 & wz_1 \\ \frac{w}{z_1} & 1 \end{bmatrix} =$$

$$= \frac{1}{(n_1 LC_1 w^2 + n_1^2)\sqrt{1 - w^2}} \left[\begin{array}{c|c} w^2 (LC_1 + \frac{n_1^2 L}{z_1}) & LC_1 z_1 w^3 + w(n_1^2 z_1 + n_1^2 L) \\ \hline \frac{n_1^2 LC_1}{z_1} w^3 + w\{C_1 (n_1 - 1)^2 + \frac{n_1^2}{z_1}\} & w^2 \{C_1 z_1 (n_1 - 1)^2 + n_1^2 LC_1\} + n_1^2 \end{array}\right] \tag{4.13}$$

The polynomial system of (4.13) can be partitioned as given in (4.14).

$$\left.\begin{aligned}
\frac{A_1}{D_1} &= \frac{w^2\left(LC_1 + \frac{n_1^2 L}{z_1}\right) + n_1^2}{LC_1 z_1 w^3 + w(n_1^2 z_1 + n_1^2 L)} = \frac{1}{(z_1 + L)w} + \frac{a_1 w}{d_1 w^2 + 1} \\
\frac{B_1}{D_1} &= \frac{w^2\, C_1 z_1 (n_1 - 1)^2 + n_1^2 LC_1 + n_1}{LC_1 z_1 w^3 + w(n_1^2 z_1 + n_1^2 L)} = \frac{1}{(z_1 + L)w} + \frac{b_1 w}{d_1 w^2 + 1} \\
\frac{H_1}{D_1} &= \frac{(n_1 LC_1 w^2 + n_1^2)\sqrt{1 - w^2}}{LC_1 z_1 w^3 + w(n_1^2 z_1 + n_1^2 L)} = \frac{\sqrt{1 - w^2}}{(z_1 + L)w} + \frac{h_1 w\sqrt{1 - w^2}}{d_1 w^2 + 1}
\end{aligned}\right\} \quad (4.14)$$

In (4.14) we have

$$\left.\begin{aligned}
a_1 &= \frac{L^2 C_1 z_1 + n_1^2 L(z_1 + L)}{n_1^2 z_1 (z_1 + L)^2}, \qquad h_1 = \frac{LC_1\{z_1(\frac{n_1 - 1}{n_1}) + L\}}{n_1 (z_1 + L)^2} \\
b_1 &= \frac{C_1[\{\frac{z_1(n_1 - 1)}{n_1}\} + L]^2}{(z_1 + L)^2}, \qquad d_1 = \frac{LC_1 z_1}{n_1^2 (z_1 + L)}
\end{aligned}\right\} \quad (4.15)$$

The first part of the partitioning in (4.14) describes a unit element with a characteristic impedance

$$z_2 = z_1 + L. \quad (4.16)$$

For the second part of the partitioning in (4.14) we have the chain matrix

$$K_2 = \frac{1}{h_1\sqrt{1 - w^2}} \begin{bmatrix} a_1 & d_1 w + \frac{1}{w} \\ c_x w & b_1 \end{bmatrix}, \quad (4.17)$$

$$\text{with } c_x = \frac{LC_1\{z_1(\frac{n_1 - 1}{n_1}) + L\}^2}{z_1 (z_1 + L)^3}. \quad (4.18)$$

It can easily be shown that K_2 can be partitioned into three parts as follows:

$$K_2 = \frac{1}{\sqrt{1-w^2}} \begin{bmatrix} 1 & \frac{1}{b_1 w} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{h_1}{b_1} & 0 \\ 0 & \frac{b_1}{h_1} \end{bmatrix} \begin{bmatrix} 1 & w\frac{b_1}{c_x} \\ w\frac{c_x}{b_1} & 1 \end{bmatrix} . \qquad (4.19)$$

We have the cascade connection of a series capacitance $C_2 = b_1$, a transformer with $n_2 = \frac{b_1}{h_1}$ and a unit element with $z_3 = \frac{b_1}{c_x}$ as a realization of the partition of K_2.

The equivalence of the figures 4.9 and 4.10 has now been proved. For the element values we have

$$\left.\begin{aligned} z_2 &= z_1 + L, & n_2 &= \frac{z_1(n-1)}{n_1 L} + 1 \\ C_2 &= \frac{C_1\left[\left\{\frac{z_1(n_1-1)}{n_1}\right\} + L\right]^2}{(z_1+L)^2}, & z_3 &= \frac{z_1(z_1+L)}{L}. \end{aligned}\right\} \qquad (4.20)$$

We observe that the element values are positive, exept for n_2, which may become negative.

End of proof.

The wave digital translation of figure 4.10 is shown in figure 4.11.

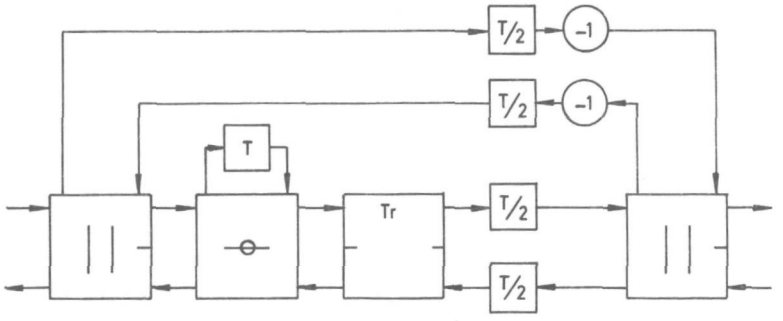


Fig. 4.11. Wave digital translation of the network of fig. 4.10.

The structure of figure 4.11 requires 5 different multiplier coefficients (it is supposed that the transformer multipliers are combined with an adapter). It does not contain delay-free loops so that it is numerically realizable.

At this point the work which has been published on the translations of the so-called C-sections [59-61] equivalent to figure 4.8 for $n < 0$, needs to be mentioned. Scanlan and Fagan [60] give figure 4.12 as a realization of a C-section with a transmission zero greater than unity. Its wave digital translation is shown in figure 4.13, where the four delays of T/2 have been transformed into two of delay T. But this figure has an analog, continuous equivalent of figure 4.14.

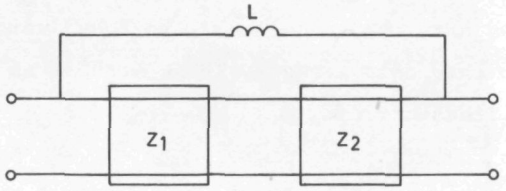


Fig. 4.12. C-section with a transmission zero greater than unity given by Scanlan and Fagan.

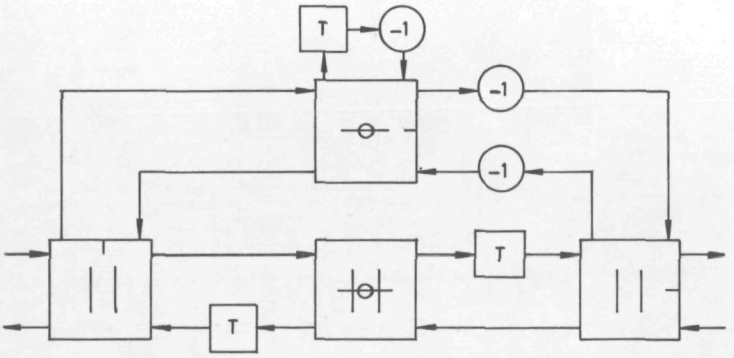


Fig. 4.13. Wave digital translation of the network of fig. 4.12.

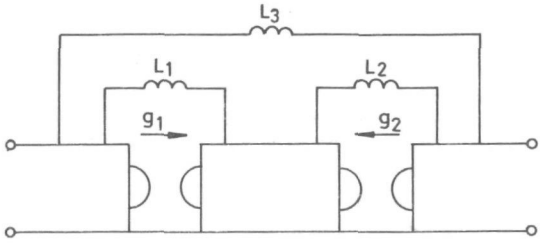


Fig. 4.14. Network which is equivalent to fig. 4.12.

In figure 4.14 we have $g_1 L_1 = g_2 L_2 = 1.$ (4.21)

Because the inductances in figure 4.14 form a loop, we can eliminate one of the delay elements of figure 4.13 making this structure canonic in the number of delay elements needed. For a further discussion on these matters we refer to Meerkötter [54].

Finally, we mention here the so-called Ikeno loop, which realizes a C - section cascaded with a unit element. These structures have been sufficiently described in the literature [65,66].

4.3.2. Second order non-reciprocal section.

We consider the section shown in figure 4.15 and cascade it with a unit element as shown in figure 4.16.

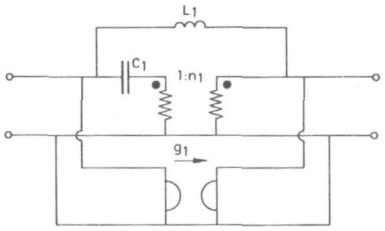


Fig. 4.15. Second order non-reciprocal section.

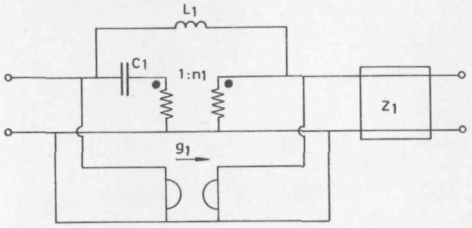


Fig. 4.16. The section of fig. 4.15 cascaded with a unit element.

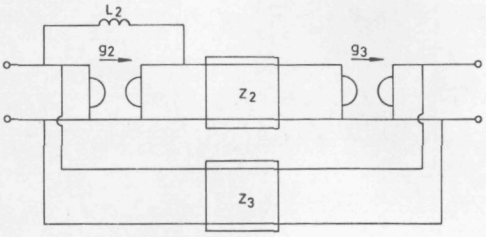


Fig. 4.17. Network which is equivalent to that of fig. 4.16.

Theorem 4.3.

The network of fig. 4.17 is equivalent to that of fig. 4.16 if relations between the elements of the two networks are satisfied. Positive values of C_1, L_1 and z_1 in fig. 4.16 lead to positive values of L_2, z_2 and z_3 in fig. 4.17.

Proof:

The Tellegen polynomials of fig. 4.15 are:

$$\left.\begin{aligned} A &= L_1C_1w^2 + n_1^2 \quad , & C &= C_1(n_1 - 1)^2 + g_1^2L_1n_1^2w \quad , \\ B &= n_1^2L_1C_1w^2 + n_1^2 \quad , & D &= n_1^2L_1w \quad , \\ H &= n_1L_1C_1w^2 + n_1^2 \quad , & K &= g_1L_1n_1^2w. \end{aligned}\right\} \qquad (4.22)$$

Cascading a unit element z_1 leads to the chain matrix K_1 of figure 4.16:

$$K_1 = \frac{1}{(n_1L_1C_1w^2+g_1L_1n_1^2w+n_1^2)\sqrt{1-w^2}} \left[\begin{array}{c|c} L_1C_1w^2+n_1^2 & n_1^2L_1w \\ \hline \{C_1(n_1-1)^2+g_1L_1n_1^2\}w & n_1^2L_1C_1w^2+n_1^2 \end{array}\right] \left[\begin{array}{cc} 1 & wz_1 \\ \frac{w}{z_1} & 1 \end{array}\right] =$$

$$= \frac{1}{(n_1^2L_1C_1w^2+g_1L_1n_1^2w+n_1^2)\sqrt{1-w^2}} \times$$

$$\times \begin{bmatrix} w^2\{L_1C_1 + \frac{n_1^2L_1}{z_1}\} + n_1^2 & | & w^3\{L_1C_1z_1\}+w\{n_1^2z_1+n_1^2L_1\} \\ & | & \\ w^3\{\frac{n_1^2L_1C_1}{z_1}\}+w\{C_1(n_1-1)^2+g_1^2L_1n_1^2+\frac{n_1^2}{z_1}\} & | & w^2\{z_1C_1(n_1-1)^2+g_1^2L_1n_1^2z_1+n_1^2L_1C_1+n_1^2\} \end{bmatrix} . \tag{4.23}$$

The polynomial system of (4.23) can be partitioned into the following form:

$$\left.\begin{aligned} \frac{A_1}{D_1} &= \frac{w^2\{L_1C_1 + \frac{n_1^2L_1}{z_1}\}+ n_1^2}{w^3\{L_1C_1z_1\} + 2n_1^2(L_1 + z_1)} = \frac{1}{(z_1 + L_1)w} + \frac{a_1w}{d_1w^2 + 1} \\ \frac{B_1}{D_1} &= \frac{w^2\{z_1C_1(n_1 - 1)^2 + g_1^2L_1n_1^2z_1 + n_1^2L_1C_1\} + n_1^2}{w^3\{L_1C_1z_1\} + wn_1^2(z_1 + L_1)} = \frac{1}{(z_1 + L_1)w} + \frac{b_1w}{d_1w^2 + 1} \\ \frac{H_1 \pm K_1}{D_1} &= \frac{(n_1L_1C_1w^2 \pm g_1L_1n_1^2w + n_1^2)\sqrt{1 - w^2}}{w^3\{L_1C_1z_1\} + wn_1^2(z_1 + L_1} = \frac{\sqrt{1 - w^2}}{(z_1 + L_1)w} + \frac{(h_1w \pm h_2)\sqrt{1 - w^2}}{d_1w^2 + 1} \end{aligned}\right\} \tag{4.24}$$

The constants a, b, h_i, h_2 and d_1 are given by

$$a_1 = \frac{L_1^2C_1z_1 + n_1^2L_1(z_1 + L_1)}{n_1^2z_1(z_1 + L_1)} , \quad b_1 = \frac{C_1\{\frac{z_1(n_1 - 1)}{n_1} + L_1\}^2 + g_1^2L_1z_1(z_1 + L_1)}{(z_1 + L_1)^2} \tag{4.25}$$

$$h_1 = \frac{L_1C_1\{z_1(\frac{n_1 - 1}{n_1}) + L\}}{n_1(z_1+ L_1)^2} , \qquad h_2 = \frac{g_1L_1}{z_1 + L_1} , \qquad d_1 = \frac{L_1C_1z_1}{n_1^2(z_1 + L_1)} . \tag{4.26}$$

The first part of the partitioning in (4.24) is again a unit element with

$$z_2 = z_1 + L_1. \tag{4.27}$$

For the second part of the partitioning of (4.24) we can find a C-polyno-

mial given as

$$C = \frac{h_1^2}{d_1} w^2 + h_2^2 = c_1 w^2 + c_2. \tag{4.28}$$

The chain matrix K_2 of the second part of the partitioning of (4.24) can now be written and decomposed as follows:

$$K_2 = \frac{1}{(h_1 w + h_2)\sqrt{1-w^2}} \begin{bmatrix} a_1 w & d_1 w^2 + 1 \\ c_1 w^2 + c_2 & b_1 w \end{bmatrix} =$$

$$= \frac{1}{\left(w + \frac{h_2}{h_1}\right)\sqrt{1-w^2}} \begin{bmatrix} \frac{h_2}{h_1} & \frac{h_1(c_1+c_2)}{c_1 b_1 h_2} w \\ \frac{c_1 b_1 h_2}{h_1(c_1+c_2)} w & \frac{h_2}{h_1} \end{bmatrix} \begin{bmatrix} 1 & \frac{c_1+c_2}{b_1 h_2^2} w \\ \frac{b_1 h_2^2}{c_1+c_2} w & 1 \end{bmatrix} \begin{bmatrix} 0 & \frac{1}{h_2} \\ h_2 & 0 \end{bmatrix}. \tag{4.29}$$

From (4.29) we obtain the rest of the element values of figure 4.17:

$$\left.\begin{aligned} g_3 = \frac{1}{h_2} = \frac{z_1 + L_1}{g_1 L_1}, \quad z_2 = \frac{c_1 + c_2}{b_1 h_2^2} = \frac{1}{z_1 L_1 g_1^2 (z_1 + L_1)}, \\ L_2 = \frac{h_1^2 (c_1 + c_2)}{c_1 b_1 h_2^2} = \frac{c_1}{g_1^2 n_1^2 (z_1 + L_1)^2}, \quad g_2 = \frac{c_1^2 \{z_1 (\frac{n_1 - 1}{n_1}) + L_1\}}{g_1^2 n_1^3 (z_1 + L_1)^3}. \end{aligned}\right\} \tag{4.30}$$

We conclude that only g_2 and g_3 may become negative, the rest of the element values in figure 4.17 is always positive.

End of proof.

To obtain a numerically realizable wave digital translation of fig. 4.17 we use the equivalence of the figures 4.5 and 4.6. The structure of fig. 4.18 finally results.

If we combine again the multipliers of the gyrator realizations with adapters we need 7 different multiplier coefficients in figure 4.18.

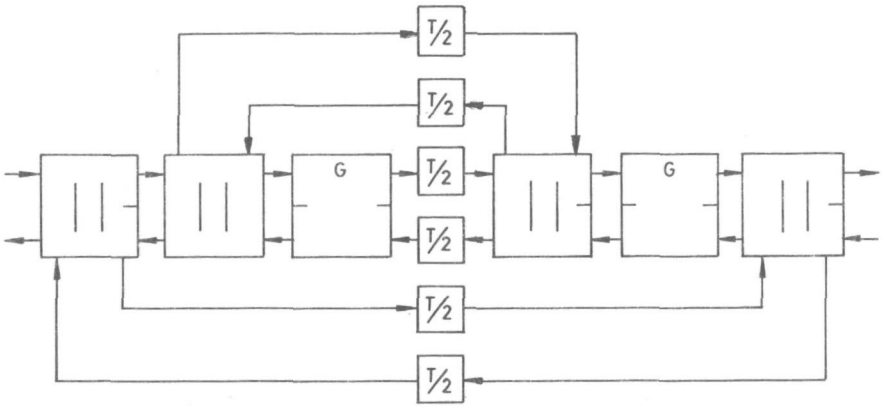


Fig. 4.18. Wave digital translation of the network of fig. 4.17.

Now that the numerically realizable wave digital structure of figure 4.18 has been found, a general transfer function can be synthesized, although for each first or second order section which is needed, a unit element may be needed in addition. However, we may want to synthesize the transfer function of a reciprocal lossless network containing complex transmission zero's. If we want to maintain reciprocity, it means that also a translation of a fourth order reciprocal section is needed. This is studied in the next section.

4.4. Fourth order reciprocal section.

We start from figure 4.19, which is a fourth order reciprocal section transparent at zero frequency cascaded with a unit element.
We will find an equivalent network of the one given in figure 4.19 and show how to calculate the element values of that equivalent network. This equivalent structure is given in figure 4.20.

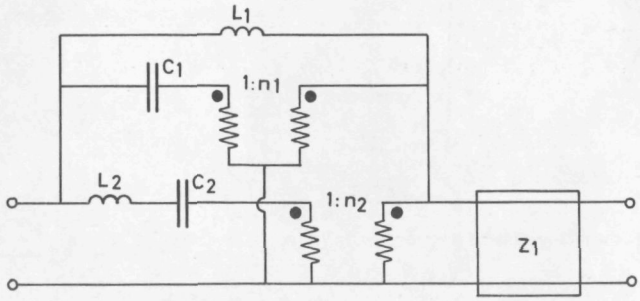


Fig. 4.19. Fourth order reciprocal section cascaded with a unit element.

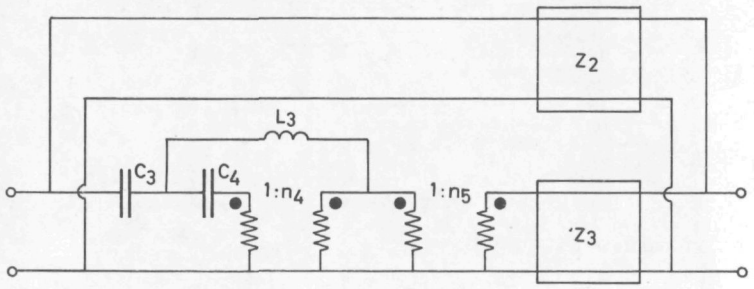


Fig. 4.20. Network which is equivalent to that of fig. 4.19.

Theorem 4.4.

The network of fig. 4.20 is equivalent to that of fig. 4.19 if relations between the elements of both networks are satisfied. Positive values of the elements in fig. 4.19 (except n_1 and n_2) lead to positive values in fig. 4.20 (except n_4 and n_5).

Proof:

The section itself (figure 4.19 without unit element) is described by the following Tellegen polynomials:

$$\left.\begin{aligned} A_1 &= a_1w^4 + a_2w^2 + a_3, \\ B_1 &= b_1w^4 + b_2w^2 + a_3, \\ H_1 &= h_1w^4 + h_2w^2 + a_3, \\ D_1 &= d_1w^3 + d_2w, \\ C_1 &= c_1w^3 + c_2w. \end{aligned}\right\} \tag{4.31}$$

In terms of element values:

$$\left.\begin{aligned} &a_1 = n_2^2L_1C_1L_2C_2 \quad , a_2 = n_1^2n_2^2L_2C_2 + n_2^2L_1C_1 + n_1^2L_1C_2, \; a_3 = n_1^2n_2^2, \\ &b_1 = n_1^2n_2^2L_1C_1L_2C_2 \; , b_2 = n_1^2n_2^2L_2C_2 + n_1^2n_2^2L_1C_1 + n_1^2n_2^2L_1C_2, \\ &h_1 = n_1n_2^2L_1C_1L_2C_2 \; , h_2 = n_1^2n_2^2L_2C_2 + n_1n_2^2L_1C_1 + n_1^2n_2L_1C_2, \\ &d_1 = n_1n_2L_1L_2C_2 \quad , d_2 = n_1n_2L_1, \\ &c_1 = n_2^2C_1L_2C_2(1 - n_1)^2 + L_1C_1C_2(n_1 - n_2)^2, \; C_2 = n_1^2C_2(1-n_2)^2 + n_2^2C_1(1-n_1)^2. \end{aligned}\right\} \tag{4.32}$$

Cascading this section with a unit element of impedance z_1 leads to the system of polynomials given below.

$$\left.\begin{aligned} &A_2 = A_1 + w\frac{D_1}{z_1} = a_4w^4 + a_5w^2 + a_6, \; C_2 = C_1 + \frac{wB_1}{z_1}, \\ &B_2 = wz_1C_1 + B_1 = b_3w^4 + b_4w^2 + a_6, \; D_2 = wz_1A_1 + D_1 = d_3w^5 + d_4w^3 + d_5w \\ &H_2 = H_1\sqrt{1 - w^2}. \end{aligned}\right\} \tag{4.33}$$

In terms of element values:

$$a_4 = n_2^2L_1C_1L_2C_2 + \frac{n_1^2n_2^2L_1L_2C_2}{z_1}, \; a_5 = n_1^2n_2^2L_2C_2 + n_2^2L_1C_1 + n_1^2L_1C_2 + \frac{n_1^2n_2^2L_1}{z_1},$$

$$a_6 = n_1^2n_2^2,$$

$$b_3 = z_1n_2^2C_1L_2C_2(1 - n_1)^2 + z_1L_1C_1C_2(n_1 - n_2)^2 + n_1^2n_2^2L_1C_1L_2C_2,$$

$$b_4 = z_1n_1^2C_2(1 - n_2)^2 + z_1n_2^2C_1(1 - n_1)^2 + n_1^2n_2^2L_2C_2 + n_1^2n_2^2L_1C_1 + \tag{4.34}$$

$$+ n_1^2n_2^2L_1C_2,$$

$$d_3 = z_1 n_2^2 L_1 C_1 L_2 C_2, \quad d_5 = n_1^2 n_2^2 (z_1 + L_1),$$

$$d_4 = z_1 n_1^2 n_2^2 L_2 C_2 + z_1 n_2^2 L_1 C_1 + z_1 n_1^2 L_1 C_2 + n_1^2 n_2^2 L_1 L_2 C_2.$$

The system of polynomials can be partitioned as follows:

$$\left.\begin{aligned} \frac{A_2}{D_2} &= \frac{a_4 w^4 + a_5 w^2 + a_6}{d_3 w^5 + d_4 w^3 + d_5 w} = \frac{a_6}{d_5 w} + \frac{a_7 w^3 + a_8 w}{d_6 w^4 + d_7 w^2 + 1} \\ \frac{B_2}{D_2} &= \frac{b_3 w^4 + b_4 w^2 + a_6}{d_3 w^5 + d_4 w^3 + d_5 w} = \frac{a_6}{d_5 w} + \frac{b_5 w^3 + b_6 w}{d_6 w^4 + d_7 w^2 + 1} \\ \frac{H_2}{D_2} &= \frac{(h_1 w^4 + h_2 w^2 + a_3)\sqrt{1 - w^2}}{d_3 w^5 + d_4 w^3 + d_5 w} = \frac{a_6\sqrt{1 - w^2}}{d_5 w} + \frac{(h_3 w^3 + h_4 w)\sqrt{1 - w^2}}{d_6 w^4 + d_7 w^2 + 1}. \end{aligned}\right\} \quad (4.35)$$

It follows directly that the first part of the partitioning given in (4.35) is the admittance description of a unit element of impedance value z_2 with

$$z_2 = \frac{d_5}{a_6} = \frac{n_1^2 n_2^2 (z_1 + L_1)}{n_1^2 n_2^2} = z_1 + L_1. \quad (4.36)$$

It can be proved easily that splitting off a unit element of impedance value z_2 does not destroy realizability of the remaining system so that we we may conclude at once that

$$a_6, a_7, b_7, b_8 > 0. \quad (4.37)$$

We have

$$\left.\begin{aligned} &d_6 = \frac{d_3}{d_5}, \quad d_7 = \frac{d_4}{d_5}, \\ &a_7 = \frac{a_4 - a_6 d_6}{d_5}, \; a_8 = \frac{a_5 - a_6 d_7}{d_5}, \; b_5 = \frac{b_3 - a_6 d_6}{d_5}, \\ &b_6 = \frac{b_4 - a_6 d_7}{d_5}, \; h_3 = \frac{h_1 - a_6 d_6}{d_5}, \; h_4 = \frac{h_2 - a_6 d_7}{d_5}. \end{aligned}\right\} \quad (4.38)$$

For a later step in the synthesis procedure it will be convenient to have an explicit expression for the transmission zero of the polynomial H_2. We have

$$\frac{h_4}{h_3} = \frac{h_2 - a_6 d_7}{h_1 - a_6 d_6} = \frac{1}{L_2 C_2} + \frac{n_1^2\{n_2(z_1 + L_1) - z_1\}}{n_2^2 L_2 C_1\{n_1(z_1 + L_1) - z_1\}} \,. \tag{4.39}$$

The second part of the partitioning in (4.35) which has to be synthesized further, is of the fourth order with a polynomial

$$\text{with} \qquad \left.\begin{aligned} C_3 &= c_3 w^4 + c_4 w^2 \,, \\ c_3 &= \frac{h_3^2}{d_6} \,, \quad c_4 = (a_8 b_6) - h_4^2 . \end{aligned}\right\} \tag{4.40}$$

As a term $(1 - w^2)^{\frac{1}{2}}$ is present in the new H-polynomial, we can split off a unit element, which will be done on the right. The chain matrix formulation of this process is as follows:

$$K = \frac{1}{H_3}\begin{bmatrix} A_3 & D_3 \\ C_3 & B_3 \end{bmatrix} = \frac{1}{H_4}\begin{bmatrix} A_4 & D_4 \\ C_4 & B_4 \end{bmatrix} \cdot \frac{1}{\sqrt{1 - w^2}}\begin{bmatrix} 1 & wz_3 \\ \frac{w}{z_3} & 1 \end{bmatrix} . \tag{4.41}$$

In (4.41) the polynomials A_3, B_3, H_3 and D_3 are obtained from the second part of the partitioning in (4.34). It can readily be shown that the polynomials A_4, B_4, C_4, D_4 and H_4 can only have the polynomial form given below:

$$K = \frac{1}{(h_3 w^3 + h_4 w)\sqrt{1 - w^2}} \begin{bmatrix} a_7 w^3 + a_8 w & d_6 w^4 + d_7 w^2 + 1 \\ c_3 w^4 + c_4 w^2 & b_5 w^3 + b_6 w \end{bmatrix} =$$

$$= \frac{1}{(h_3 w^3 + h_4 w)} \begin{bmatrix} a_8 w^3 + a_9 w & d_8 w^2 + d_9 \\ c_5 w^2 & b_7 w^3 + b_8 w \end{bmatrix} \cdot \frac{1}{\sqrt{1 - w^2}} \begin{bmatrix} 1 & w z_3 \\ \frac{w}{z_3} & 1 \end{bmatrix} . \quad (4.42)$$

The theory of cascade factorization now guarantees that the coefficients of the polynomials A_4, B_4, C_4 and D_4 and z_3 will be positive and are given by

$$\left.\begin{aligned} z_3 &= \frac{B_4 + D_4}{A_4 + C_4}\bigg|_{w=1} = \frac{b_5 + b_6 + d_6 + d_7 + 1}{a_7 + a_8 + c_3 + c_4}, \\ b_8 &= b_6, \quad b_7 = c_3 z_3, \quad c_5 = c_4 - \frac{b_8}{z_3}, \\ d_9 &= 1, \quad a_8 = \frac{d_6}{z_3}, \quad a_9 = a_8 - \frac{d_9}{z_3}, \quad d_8 = d_7 - (a_9 z_3). \end{aligned}\right\} \quad (4.43)$$

There remains a third order network described by the polynomials H_4, A_4, B_4, C_4 and D_4. Because of the fact that polynomial H_4 has a factor w there are two possibilities for first order sections to be split off: a series capacitance or a shunt inductance, which may be split off at the left or at the right. If we restrict ourselves to splitting off at the left, then the two possibilities, in terms of its chain matrix description, are given below:

$$\frac{1}{h_3 w^3 + h_4 w} \begin{bmatrix} a_8 w^3 + a_9 w & d_8 w^2 + d_9 \\ c_5 w^2 & b_7 w^3 + b_8 w \end{bmatrix} =$$

$$1^e: = \frac{1}{wC_3} \begin{bmatrix} wC_3 & 1 \\ 0 & wC_3 \end{bmatrix} \cdot \frac{1}{h_5 w^2 + h_6} \begin{bmatrix} a_{10} w^2 + a_{11} & d_{10} w \\ c_6 w & b_9 w^2 + b_{10} \end{bmatrix},$$

$$2^e: = \frac{1}{wL}\begin{bmatrix} wL & 0 \\ 1 & wL \end{bmatrix} \cdot \frac{1}{h_5 w^2 + h_6}\begin{bmatrix} a_{10}w^2+a_{11} & d_{10}w \\ c_6 w & b_9 w^2+b_{10} \end{bmatrix} . \qquad (4.44)$$

In the second case, from matrix multiplication it is observed that the result does not fit the third order polynomial system. We conclude that only splitting off a series capacitance C_3 remains.
We obtain:

$$\left.\begin{aligned} C_3 &= \frac{b_8}{d_9}\ , \quad b_{10} = d_9\ , \quad a_{10} = \frac{a_8}{C_3}\ , \\ b_9 &= \frac{b_7}{C_3}\ , \quad c_6 = \frac{c_5}{C_3}\ , \quad a_{11} = \frac{a_9 - c_6}{c_3}\ , \\ d_{10} &= \frac{d_8 - b_9}{C_3}\ , \quad h_5 = \frac{h_3}{C_3}\ , \quad h_6 = \frac{h_4}{C_3}\ . \end{aligned}\right\} \qquad (4.45)$$

A second order system of polynomials is left over. In order to arrive at the structure of figure 4.8 we have to split off a transformer. In terms of the chain matrix description:

$$K = \frac{1}{h_5 w^2 + h_6}\begin{bmatrix} a_{10}w^2 + a_{11} & d_{10}w \\ c_6 w & b_9 w^2 + b_{10} \end{bmatrix} =$$

$$= \frac{1}{h_5 w^2 + h_6}\begin{bmatrix} a_{12}w^2 + a_{13} & d_{11}w \\ c_7 w & b_{11}w^2 + b_{12} \end{bmatrix} \cdot \begin{bmatrix} \frac{1}{n_5} & 0 \\ 0 & n_5 \end{bmatrix} . \qquad (4.46)$$

The second order section we want to obtain, is transparent for zero frequency which means:

$$\frac{2h_6}{a_{13} + b_{12}} = 1. \qquad (4.47)$$

The constants n_5, a_{12}, d_{11}, c_7, b_{11} and b_{12} can now be calculated :

$$\left.\begin{aligned} &n_5 = \frac{h_6}{a_{11}}\,, \quad a_{13} = b_{12} = h_6\,, \quad a_{12} = a_{10}n_5\,, \\ &b_{11} = \frac{b_9}{n_5}\,, \quad d_{11} = \frac{d_{10}}{n_5}\,, \quad c_7 = c_6 n_5. \end{aligned}\right\} \tag{4.48}$$

The theory of cascade factorization guarantees that a_{12}, a_{13}, d_{11}, c_7, b_{11} and b_{12} all have the same sign.
The element values of L_3 and C_4 and the ratio n_4 now follow directly:

$$L_3 = \frac{d_{11}}{a_{13}}\,, \qquad C_4 = \frac{b_{11}}{d_{11}}\,, \qquad n_4 = \frac{b_{11}}{h_5}\,. \tag{4.49}$$

As d_{11}, a_{13}, b_{11} and d_{11} have the same sign, we may conclude that L_3 and C_4 will be positive.
We have now proved the equivalence of the figures 4.19 and 4.20 and given a way how to calculate the element values of figure 4.20.

End of proof.

Figure 4.20 is not the only structure which could have been found. Especially the sequence of factorizations which has been done on the second part of the partitioning of (4.35) is in fact quite arbitrarily. It is now clear how one arrives at a numerically realizable wave digital translation of fig. 4.20. We first change it into fig. 4.21.

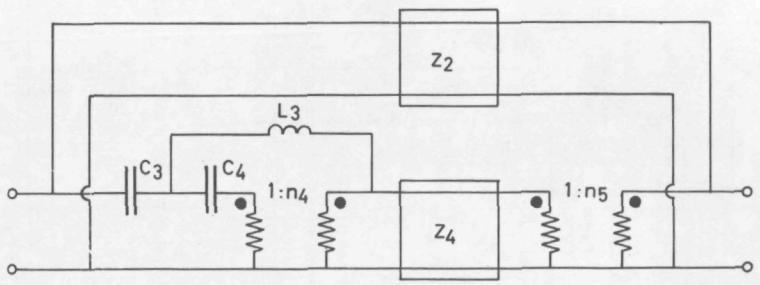


Fig. 4.21. Another network which is equivalent to fig. 4.19.

With $z_4 = \frac{z_3}{n_5^2}$. (4.50)

We now use the equivalence of the figures 4.9 and 4.10 and obtain figure 4.22.

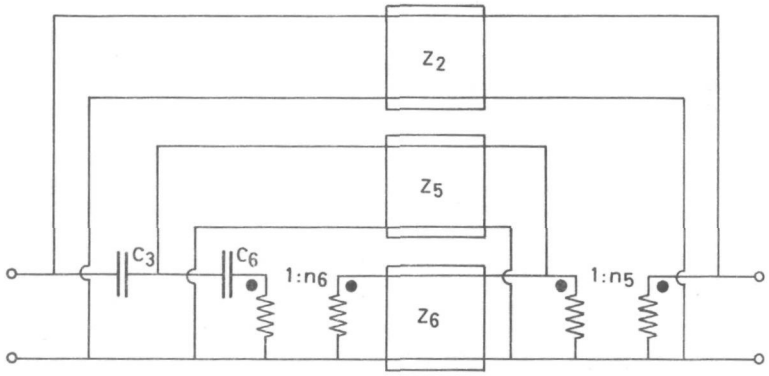


Fig. 4.22. Network which results from fig. 4.21 when the equivalence of fig. 4.9 and 4.10 is used.

The wave digital translation of figure 4.22 is given in figure 4.23 and it is readily observed that it is numerically realizable. If we combine the multipliers of the transformer realizations with adapters, we need essentially 9 different multiplier coefficients in figure 4.23.

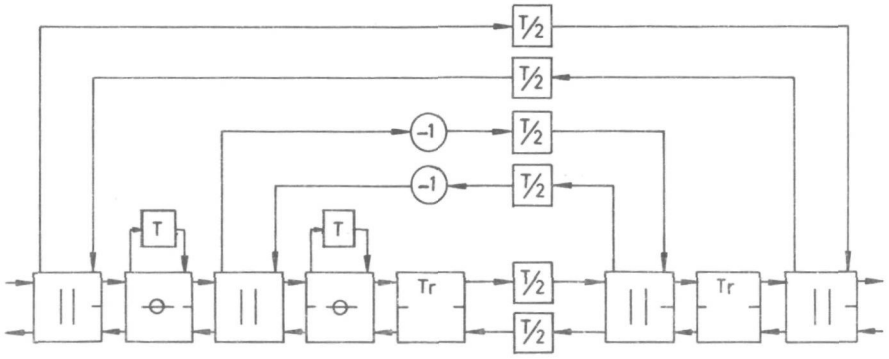


Fig. 4.23. Wave digital translation of the network of fig. 4.22.

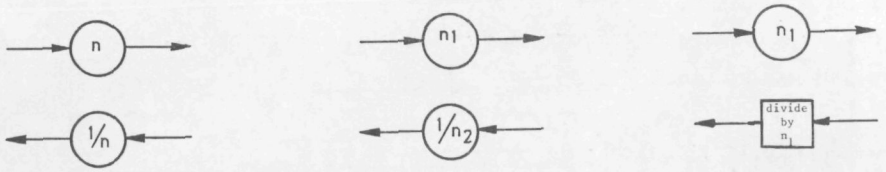
4.5. On the passivity properties of the structures introduced in the previous sections.

The wave digital structures introduced in the chapters 2 and 3 all have the property that the structure remains equivalent to the original network when multiplier coefficients are varied independently. Only the elements (in the Jauman structure the terminating resistance is excluded) in the corresponding network obtain a different value. It means that Kirchhof relations and transformer and gyrator relations remain satisfied. These properties are no longer true in general for the structures introduced in this chapter. We will show this by specific examples.

The transformer.

The flow diagram for the ideal case is shown again in figure 4.24a (we have $n^2 g_2 = g_1$). Due to rounding or truncation we may arrive at figure 4.24b (with $n_2 = n_1 + \delta$). It is now not possible any more to translate back to an analog transformer. This remains possible if we introduce a divider as shown in figure 4.24c. From the passivity condition as stated in expression (2.80) it follows for figure 4.24b (with $n_1^2 g_2' = g_1$) that following condition must be satisfied:

$$\begin{bmatrix} 0 & n_1 \\ \frac{1}{n_1+\delta} & 0 \end{bmatrix} \cdot \begin{bmatrix} g_1 & 0 \\ 0 & g_2' \end{bmatrix} \cdot \begin{bmatrix} 0 & \frac{1}{n_1+\delta} \\ n_1 & 0 \end{bmatrix} = \begin{bmatrix} g_1 & 0 \\ 0 & (\frac{n_1}{n_1+\delta})^2 g_2' \end{bmatrix} \leq \begin{bmatrix} g_1 & 0 \\ 0 & g_2' \end{bmatrix} . \qquad (4.50)$$



a. Ideal case with two multipliers.

b. Case where two coefficients have been rounded independently.

c. Case with rounding of n and one divider.

Fig. 4.24. Three different situations for the transformer flow diagram.

Equation (4.50) is valid only if $\left|\frac{n_1}{n_1+\delta}\right| \leq 1.$ (4.51)

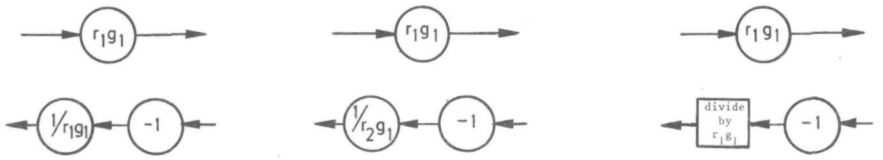
We have now proved the following theorem:

Theorem 4.5.

In the case multiplier coefficients have finite accuracy the transformer realization of figure 4.24b will be passive iff (4.51) holds.

The gyrator.

We have the situation of figure 4.25.



a. Ideal case with two multipliers. b. Case where two coefficients have been rounded independently. c. Case with rounding of rg_1 and one divider.

Fig. 4.25. Three different situations for the gyrator flow diagram.

If rounding or truncation has been applied, rg_1 has changed into r_1g_1 and $\frac{1}{rg_1}$ has changed into $\frac{1}{r_2g_1}$ (r, r_1 and r_2 are gyration resistances, g_1 and g_2 are port conductances with $r^2g_1g_2 = 1$ in the ideal case). Only in the case of figure 4.25c it remains possible to translate back to a lossless gyrator. In the case of figure 4.25b the passivity condition can again be applied which leads to

$$\begin{bmatrix} 0 & r_1g_1 \\ \frac{-1}{(r_1+\gamma)g_1} & 0 \end{bmatrix}\begin{bmatrix} g_1 & 0 \\ 0 & g_2' \end{bmatrix}\begin{bmatrix} 0 & \frac{-1}{(r_1+\gamma)g_1} \\ r_1g_1 & 0 \end{bmatrix} = \begin{bmatrix} g_1 & 0 \\ 0 & \frac{r_1^2g_2'}{(r_1+\gamma)^2} \end{bmatrix} \leq \begin{bmatrix} g_1 & 0 \\ 0 & g_2' \end{bmatrix} \tag{4.52}$$

Relation (4.52) is valid only if

$$\left| \frac{r_1}{r_1 + \gamma} \right| \leq 1 \quad \text{(we have used } r_2 = r_1 + \gamma \text{ and } r_1^2 g_1 g_2' = 1\text{).} \qquad (4.53)$$

It means that we have proved the following theorem.

Theorem 4.6.

In the case the multiplier coefficients have finite accuracy the gyrator realization shown in figure 4.25b is passive iff (4.53) holds.

The transformer parallel adapter combination.

In the figures 4.11 and 4.23 we had a matched transformer combined with a three port parallel adapter (we suppose the unit element to be shifted to the left "through" the transformer). This is shown in figure 4.26.

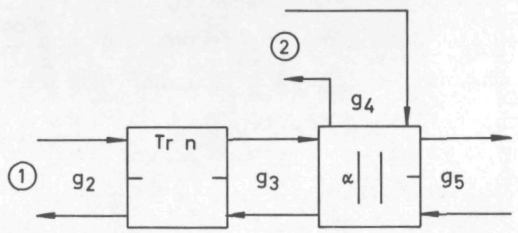


Fig. 4.26. Combination of a transformer and a three-port parallel adapter.

We must assume that the port conductances g_2 and g_4 have changed into g_2' and g_4' due to the influence of rounding or truncation of multiplier coefficients in the rest of the structure connected to ports (1) and (2). The rounding or truncation of n into n_1 and of $1/n_1$ into $1/(n_1+\delta_1)$ and of α into α' has yet to be taken care of. We show that this is possible in a passive way.For the transformer alone we have proved it already. The condition is

$$\left| \frac{n_1}{n_1 + \delta_1} \right| \leq 1 \text{ with } n_1^2 g_3' = g_2' \text{ in this case.}$$

But also the deviation of α into α' has an effect on g_3'. The coefficient α is a function of g_4 and g_3 which means in our case that a deviation in α causes a deviation of g_3' into $g_3'' = g_3' + \delta_2$.
Now the passivity condition leads to

$$\begin{bmatrix} 0 & n_1 \\ \frac{1}{n_1+\delta_1} & 0 \end{bmatrix} \begin{bmatrix} g_2' & 0 \\ 0 & g_3'+\delta_2 \end{bmatrix} \begin{bmatrix} 0 & \frac{1}{n_1+\delta_1} \\ n_1 & 0 \end{bmatrix} = \begin{bmatrix} g_2'+n_1^2\delta_2 & 0 \\ 0 & \frac{n_1^2}{(n_1+\delta_1)^2} g_3' \end{bmatrix} \leq \begin{bmatrix} g_2' & 0 \\ 0 & g_3'+\delta_2 \end{bmatrix} \tag{4.54}$$

We conclude from (4.54) that the conditions for passivity are

$$\delta_2 \leq 0 \quad \text{and} \quad \frac{n_1^2}{(n_1+\delta_1)^2} g_3' \leq g_3' + \delta_2. \tag{4.55}$$

We observe that $\delta_1 = 0$ leads to $\delta_2 = 0$, which means losslessness. It means also that the realization of figure 4.24c combined with a three port parallel adapter in the way of figure 4.26 cannot be made passive.
We have now proved the following theorem.

Theorem 4.7.

> In the case multiplier coefficients have finite accuracy then the structure of figure 4.26 is passive iff figure 4.24b is used for the transformer and (4.55) holds.

The gyrator parallel adapter combination.

This occurs in the figures 4.7 and 4.18, repeated in figure 4.27.
We suppose that, due to variations of coefficients in the rest of the structure, g_2 and g_4 have changed into g_2' and g_4'. Due to the necessity of rounding or truncating the coefficient rg_2 into $r_1 g_2'$ we obtain the change of g_3 into $g_3' = g_3 + \gamma_1$ with $r_1^2 g_2' g_3' = 1$. Now the rounding or truncation of α into α' leads to an effect on g_3' changing into $g_3'' = g_3' + \gamma_2$. We have now from the passivity condition:

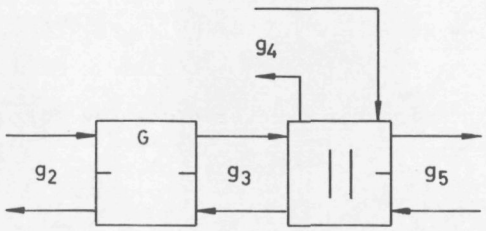


Fig. 4.27. Combination of a gyrator and a three-port parallel adapter.

$$\begin{bmatrix} 0 & r_1 g_2' \\ \dfrac{-1}{(r_1+\gamma_1)g_2'} & 0 \end{bmatrix} \begin{bmatrix} g_2' & 0 \\ 0 & g_3'+\gamma_2 \end{bmatrix} \begin{bmatrix} 0 & \dfrac{-1}{(r_1+\gamma_1)g_2'} \\ r_1 g_2' & 0 \end{bmatrix} = \begin{bmatrix} g_2'+r_1^2 g_2'^2 \gamma_2 & 0 \\ 0 & \dfrac{r_1^2}{(r_1+\gamma_1)^2} g_3' \end{bmatrix}$$

$$\leq \begin{bmatrix} g_2' & 0 \\ 0 & g_3'+\gamma_2 \end{bmatrix} \tag{4.56}$$

From (4.56) it follows that

$$\gamma_2 \leq 0 \quad \text{and} \quad \frac{r_1^2}{(r_1+\gamma_1)^2} g_3' \leq g_3' + \gamma_2. \tag{4.57}$$

This proves the following theorem.

Theorem 4.8.

In the case multiplier coefficients have finite accuracy the structure of figure 4.27 is passive iff figure 4.25b is used for the gyrator and (4.57) holds.

4.6. Conclusions and remarks.

1. The results obtained in this chapter prove the following theorem.

   Theorem 4.9.

   > A passive cascade synthesis of wave digital networks having transfer functions with transmission zeros anywhere in the z-plane is possible if the introduction of some extra delay is allowed.

2. It has been shown that only passivity and computablity is guaranteed in the structures found and the interesting question whether actually wave digital lossless structures for these sections can be found, remains.

3. Due to the bridged nature of the networks found, and the number of coefficients which is not minimal, the sensitivity behaviour of the wave digital networks obtained, will deviate from the optimal lossless ladder networks.

4. The complexity of the networks found, gives some insight in the price to be paid if a general transfer function is to be realized in wave digital form and the method of translation of analog lossless networks is used.

5. If we start with a transfer function and the number of sections to be used which need a unit element is n_1 then a factor $(1-w^2)^{n_1/2}$ has to be present in the numerator of the transfer function. These unit elements can also contribute to the selectivity if they are already introduced in the approximation stage of the problem at hand.

6. We may also start with a lossless network which is already in factorized form. In this case we introduce unit elements by cascading them with either end of the network. The characteristic impedance of these unit elements has to be 1. This means that only group-delay is added (in this case the unit element acts as an all-pass network).

CHAPTER 5

ON THE EFFICIENT IMPLEMENTATION OF WAVE DIGITAL FILTER ALGORITHMS USING PROGRAMMABLE HARDWARE

5.1 Introduction.

The material presented in this chapter is based on the author's publications given as references 42, 44 and 45. It deals with properties of wave digital filter algorithms which are of importance if these algorithms are to be implemented using flexible hardware. For that purpose a structure consisting of the following four parts is worth to be studied.

1. Arithmetical memory.

In this memory the internal variables in a flow diagram which need to be used again are stored temporarily. To optimize the dimensions of this memory it is necessary to know the number of internal variables in the filter algorithm which need to be stored simultaneously and also the number of bits needed for the representation of these variables. The first item mentioned is one to be studied in this chapter.

2. Coefficient memory.

In this memory the multiplication coefficients are stored. Due to the insensitivity property of wave digital filters the coefficients need not be known very accurately. The dimensions of this memory are not studied in this chapter.

3. Program memory.

If we suppose that each instruction word in this memory defines one operation

to be performed such as an input/output operation, an addition/subtraction or a multiplication, then the number of bits needed for each word in this memory is worth to be investigated. This aspect is also studied in this chapter.

4. Arithmetic unit.

Here the actual arithmetical operations take place. The actual hardware here may range from a very simple and slow full adder in series arithmetic to very complicated and fast operating parallel adders and multipliers in various structures. In the next section of this chapter we will discuss two of these structures in more detail.

In the rest of this chapter we will be mainly concerned with the study of the true ladder wave digital filter network, and its properties concerning the dimensions of the memories mentioned above, this being the most important wave digital filter network. However, we will also briefly study some other networks. A number of theorems will be proved concerning various properties of the true ladder wave digital filter algorithm. Some are mentioned below.

Property 1.

It will be shown that various wave digital filter algorithms do not need the subtraction operation. Stated otherwise: the inverter is not needed in these flow diagrams. It may be necessary in this case to neglect inverters and multipliers occurring at in- and outputs of these flow diagrams. This is not important however, these operations at in- or outputs have no basic influence on the filter operation.

Property 2.

If the number of delay elements in some filter flow diagram is n' and we suppose that the input is also to be stored simultaneously to these n' variables, then the minimal number N_{min} of arithmetical memory locations needed is

$$N_{min} = n' + 1 \qquad (5.1)$$

It will be shown that flow diagrams can be given such that (5.1) is obtained or approximated very closely.

Property 3.

It will be shown that, for instance in the true ladder wave digital filter flow diagrams, the additions or subtractions can always be programmed in such a way that only two memory locations a and b are involved as in

$$a \pm b \rightarrow b \qquad (5.2)$$

Property 4.

To satisfy (5.2) it means that each instruction word in the program memory has to carry information about two arithmetical memory adresses and an operation to be performed. The number of bits needed to code this information is very likely to increase when the complexity of the flow diagram and the number of memory locations needed, increases. However, it will be shown that flow diagrams and methods exist which enable the number of bits needed in each instruction word to be constant (not dependent on an increasing order of the filter) and small.

5.2 Two important programmable arithmetical structures.

5.2.1 The Random Access Memory - Arithmetic Logic Unit combination.

This combination opens the possibility of performing a logic or arithmetic operation like (5.2) on one or two variables in one clock cycle. Two available integrated circuits having this property need to be mentioned in this context:

a. The 4-bit expandable bipolar microcontroller 6701 of Monolithic Memory Inc., and
b. the 4-bit microprocessor slice Am 2901 of Advanced Micro Devices Inc.

In these circuits 16 arithmetical memory locations are available. A typical example of an operation which can be performed in one clock cycle is: add the contents of locations a and b, shift the result one bit to

the right and store it in location b. It means that information about two locations a and b and a combination of two operations needs to be available in parallel in one instruction word.

5.2.2 The Random Access Memory - Accumulator combination.

A typical operation is in this case for instance:
add or subtract the content of location a to the content of the accumulator. The information of only one memory location is needed in one instruction word but the number of instructions needed to perform an addition for instance, is now larger. The filter flow diagram need not satisfy relation (5.2) but a numbering of variables in flow diagrams such that (5.2) is satisfied is of importance for both instruction word length and number of arithmetical memory locations needed.

5.3 Some important wave digital filter structures and properties of the corresponding flow diagrams.

In this section it will often be necessary to indicate the presence of inverters in the flow diagrams corresponding to adapters as given in chapter 2. Fortunately, in the adapters obtained there inverters only occur at inputs of adapters in most cases. This will be indicated as shown in figure 5.1 where the adapter realization has an inverter at input A_1 and one at output B_n.

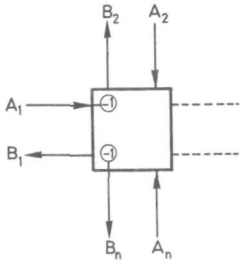


Fig. 5.1. Symbolic notation for the case an adapter has inverters at input A_1 and output B_n.

5.3.1 True ladder structures with all attenuation poles at infinite frequency in the w-plane.

For this type of wave digital filter network we prove the following theorem.

Theorem 5.1: For a true ladder wave digital filter network having all attenuation poles at infinite frequency in the w-plane, a flow diagram can be given having the following properties simultaneously:

1. Inverters are not needed in the flow diagram, inverters possibly occurring at inputs or outputs are neglected.
2. A numbering of variables can be given such that the maximum number of variables N to be stored simultaneously equals

$$N = n' + 2 \tag{5.3}$$

where n' equals the number of delay elements present in the flow diagram.

3. The additions can be arranged in such a way that the requirements for a two-adress structure are satisfied as

$$a + b \rightarrow b \tag{5.4}$$

4. The number of bits needed to code the information for two arithmetic memory locations in each instruction word in the program memory is 2 (independent of the order of the filter).

Proof: A possible translation of figure 5.2 (degree n is odd) into wave digital form using various equivalences given in chapter 2 is shown in the figures 5.3 and 5.4.

Fig. 5.2. Ladder network with all attenuation poles at infinite frequency in the w-plane.

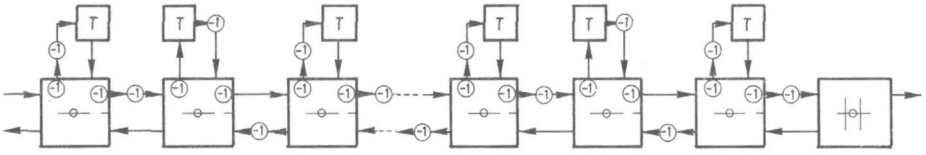


Fig. 5.3. A possible wave digital translation corresponding to fig. 5.2 where only series adapters are used in cascade.

Multipliers and inverters at inputs and outputs of the figures 5.3 and 5.4 have been neglected. It is easily seen that all the inverters from figure 5.3 cancel out or can be shifted out of the network such that figure 5.4 satisfies property 1. The internal variables in figure 5.4 have been numbered in such a way that the number of n' + 2 is maximally used, which proves property 2 and by inspection of figure 5.4 also property 3 turns out to be satisfied. This follows also from table 5.1 where all the operations (excluding input- and output operations) have been listed together with a list of memory locations involved in each operation. The final list in table 5.1 shows the list of differences between successive memory locations needed. There are only 4 sets of differences present (1,1; 1, -1; -1,0 and 2,0) which means that the coding of this information in each instruction word needs only 2 bits, independent of the order n of the filter. This proves property 4. The above is only valid for the degree n odd, but exactly the same result can be obtained for n even in the same way. This proves theorem 5.1.

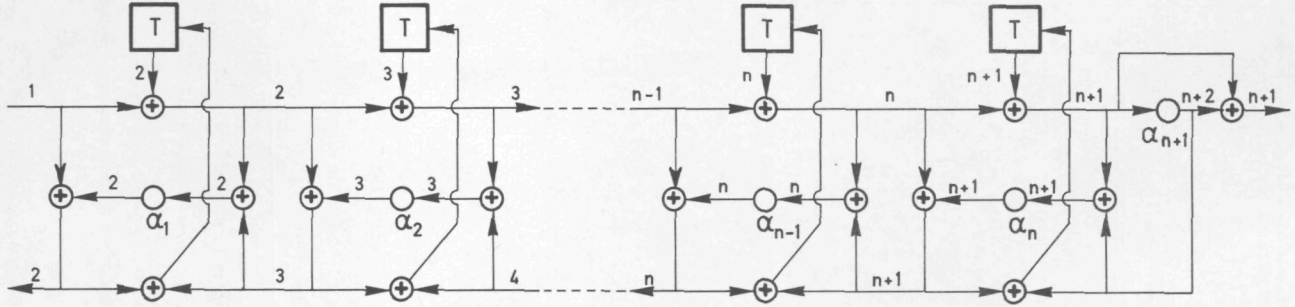


Fig. 5.4. Detailed flow diagram corresponding to fig. 5.3.

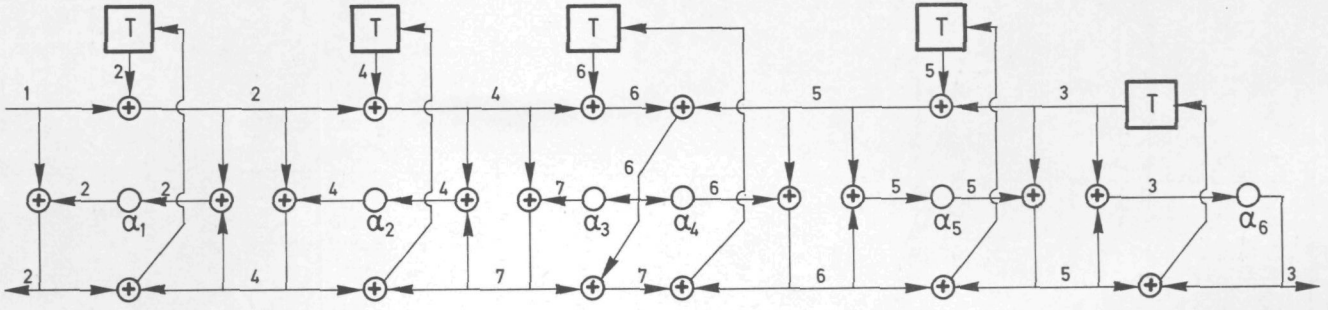


Fig. 5.6. Detailed flow diagram corresponding to fig. 5.5.

operations	memory locations involved	difference between successive locations needed
$1 + 2 \rightarrow 2$	1, 2	
$2 + 3 \rightarrow 3$	2, 3	1, 1
⋮	⋮	⋮
$n-1 + n \rightarrow n$	n-1 , n	1, 1
$n + n+1 \rightarrow n+1$	n , n+1	1, 1
$n+1 \cdot \alpha_{n+1} \rightarrow n+2$	n+1 , n+2	1, 1
$n+2 + n+1 \rightarrow n+1$	n+2 , n+1	1, -1
$n+1 \cdot \alpha_{n} \rightarrow n+1$	n+1 , n+1	-1, 0
$n + n+1 \rightarrow n+1$	n , n+1	-1, 0
$n+1 + n \rightarrow n$	n+1 , n	1, -1
$n \cdot \alpha_{n-1} \rightarrow n$	n , n	-1, 0
$n-1 + n \rightarrow n$	n-1 , n	-1, 0
⋮	⋮	⋮
$4 + 3 \rightarrow 3$	4, 3	1, -1
$3 \cdot \alpha_{2} \rightarrow 3$	3, 3	-1, 0
$2 + 3 \rightarrow 3$	2, 3	-1, 0
$3 + 2 \rightarrow 2$	3, 2	1, -1
$2 \cdot \alpha_{1} \rightarrow 2$	2, 2	-1, 0
$1 + 2 \rightarrow 2$	1, 2	-1, 0
$3 + 2 \rightarrow 2$	3, 2	2, 0
$4 + 3 \rightarrow 3$	4, 3	1, 1
⋮	⋮	⋮
$n+1 + n \rightarrow n$	n+1 , n	1, 1
$n+2 + n+1 \rightarrow n+1$	n+2 , n+1	1, 1

Table 5.1. The sequence of operations corresponding to fig. 5.4.

Another structure of the same type of ladder network but having a different way of assigning matched ports to the adapters is illustrated by a fifth order network. The block diagram is shown in figure 5.5 using only series adapters. The detailed flow diagram with the numbering of variables is shown in figure 5.6.

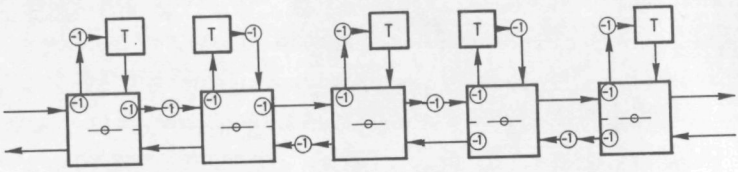


Fig. 5.5. Possible wave digital translation of fig. 5.2 for the case the filter order is 5 and with a distribution of matched ports which differs from fig. 5.3.

In table 5.2 the complete sequence of operation is given for figure 5.6.

$1 + 2 \rightarrow 2$	$4 + 2 \rightarrow 2$
$2 + 4 \rightarrow 4$	$7 + 4 \rightarrow 4$
$3 + 5 \rightarrow 5$	$6 + 7 \rightarrow 7$
$4 + 6 \rightarrow 6$	$6 \cdot \alpha_4 \rightarrow 6$
$5 + 6 \rightarrow 6$	$5 + 6 \rightarrow 6$
$6 \cdot \alpha_3 \rightarrow 7$	$6 + 5 \rightarrow 5$
$4 + 7 \rightarrow 7$	$5 \cdot \alpha_5 \rightarrow 5$
$7 + 4 \rightarrow 4$	$3 + 5 \rightarrow 5$
$4 \cdot \alpha_2 \rightarrow 4$	$5 + 3 \rightarrow 3$
$2 + 4 \rightarrow 4$	$3 \cdot \alpha_6 \rightarrow 3$
$4 + 2 \rightarrow 2$	$5 + 3 \rightarrow 3$
$2 \cdot \alpha_1 \rightarrow 2$	$6 + 5 \rightarrow 5$
$1 + 2 \rightarrow 2$	$7 + 6 \rightarrow 6$

Table 5.2. The sequence of operations corresponding to fig. 5.6.

We may conclude again that relation (5.2) is satisfied in this case, even with the plus sign in (5.2). The number of memory locations needed is 7 which can readily be generalized to n' + 2 in the general case. However, in this type of structure the number of sets of differences is greater due to the more complex way the filter algorithm is evaluated. It can be found that this number is less than 16 which means 4 bits for its coding. To conclude this section we give a third realization now, using only three-port parallel adapters as given in section 2.4 and for n odd starting from the dual of figure 5.2. The block diagram is given in figure 5.7 and the detailed flow diagram in figure 5.8. The sequence of operations is then shown in table 5.3.

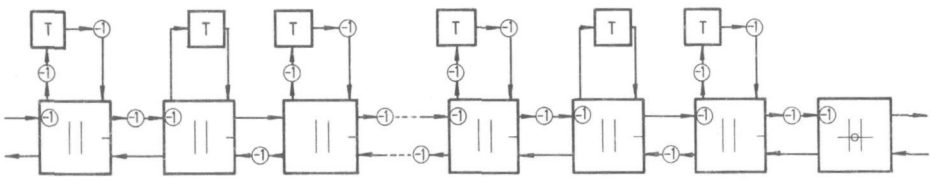


Fig. 5.7. Possible wave digital translation of fig. 5.2 where only parallel adapters are used in cascade.

operations	memory locations involved	difference between successive memory locations
$2 + 1 \rightarrow 1$	2, 1	2, 1
$1.\alpha_1 \rightarrow 3$	1, 3	-1, 2
$3 + 2 \rightarrow 2$	3, 2	2, -1
$4 + 2 \rightarrow 2$	4, 2	1, 0
$2.\alpha_2 \rightarrow 5$	2, 5	-2, 3
$5 + 4 \rightarrow 4$	5, 4	3, -1
⋮	⋮	⋮
$2n + 2n-2 \rightarrow 2n-2$	2n, 2n-2	1, 0
$2n-2 .\alpha_n \rightarrow 2n+1$	2n-2, 2n+1	-2, 3
$2n+1 + 2n \rightarrow 2n$	2n+1, 2n	3, -1
$2n . \alpha_{n+1} \rightarrow 2n+2$	2n, 2n+2	-1, 2
$2n+2 + 2n \rightarrow 2n$	2n+2, 2n	2, -2
$2n+1 + 2n \rightarrow 2n$	2n+1, 2n	-1, 0
$2n + 2n-2 \rightarrow 2n-2$	2n, 2n-2	-1, -2
⋮	⋮	⋮
$5 + 4 \rightarrow 4$	5, 4	-1, 0
$4 + 2 \rightarrow 2$	4, 2	-1, -2
$3 + 2 \rightarrow 2$	3, 2	-1, 0
$2 + 1 \rightarrow 1$	2, 1	-1, -1

Table 5.3. The sequence of operations corresponding to fig. 5.8.

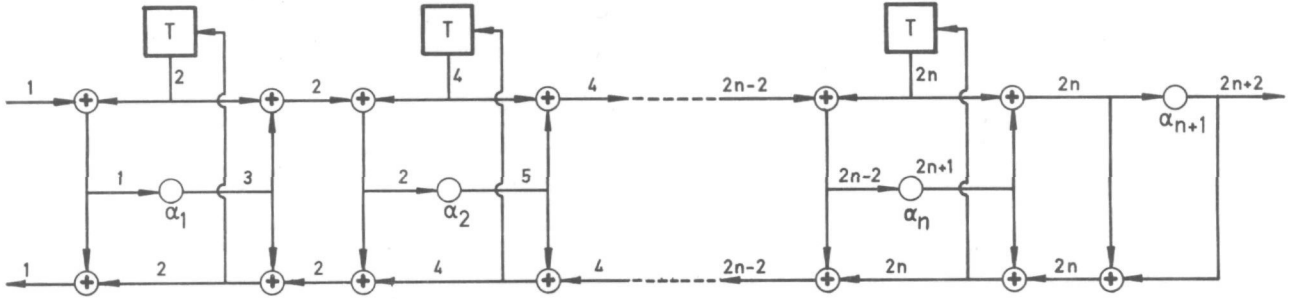


Fig. 5.8. Detailed flow diagram corresponding to fig. 5.7.

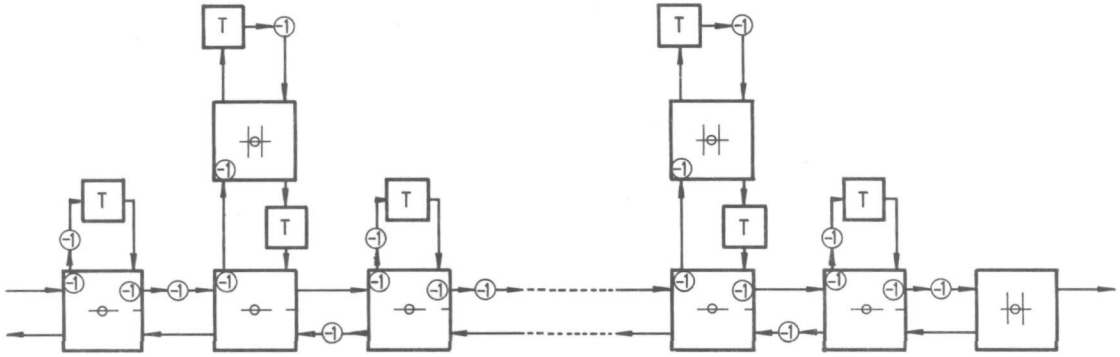


Fig. 5.10. Symbolic wave digital translation of fig. 5.9.

The number of memory locations needed in this case is 2n + 2 or 2n' + 2 instead of n' + 2 in the case of three-port series adapters. Also the set of differences is larger than in the case of table 5.1. It is 10 and therefore to be coded using 4 bits.
But relation (5.2) is again satisfied, even with the plus sign.

In case we use three-port series- and parallel adapters as they naturally occur in translating figure 5.1, relation (5.2) cannot be satisfied and the number of memory locations needed for n odd is again 2n'+2 as can be verified in the same manner as shown before.

5.3.2 True ladders with attenuation poles at finite frequencies (w-plane).

In this section we will restrict ourselves to ladder networks with at most a second order inpedance in series and/or shunt arms. We first discuss the structure shown in figure 5.9 (degree n is odd and $n \geq 3$).

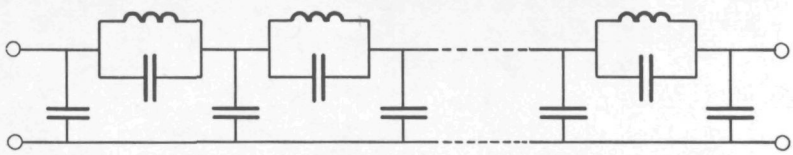


Fig. 5.9. Ladder network with attenuation poles at finite frequencies in the w-plane.

We use the knowledge gained in the previous section and restrict ourselves to using series adapters, for the resonant circuits we will use the two-port adapter given in figure 2.27a, for a reason which will become clear later. After some use of adapter equivalences we arrive at the figures 5.10 and 5.11. We state the following theorem concerning the flow diagram of figure 5.11:

Theorem 5.2. For the ladder network shown in figure 5.9 and the order $n \geq 3$, wave digital translations can be obtained having respectively following properties:

Property 1.

The numbering of internal variables can be such that relation (5.2) holds.

Property 2.

$$N = n' + 3 \tag{5.5}$$

is a sufficient number of arithmetical memory locations for all the internal variables to be stored simultaneously. In (5.5) n' is the number of delay elements present in the flow diagram of figure 5.11.

Property 3.

$$N = 2n + 1 \tag{5.6}$$

is sufficient to guarantee the possibility of coding the information necessary for two memory locations in each instruction word in the program memory with a number of bits independent of the filter order n.

Property 4.

Only the properties 1 and 2, and the properties 1 and 3 can hold simultaneously.

Proof:

The numbering of variables in figure 5.11 already proves property 1. The number of variables used in figure 5.11 is 2n + 1 as in property 3. However, this number can be reduced. It may be observed from the flow diagram that the variables with the numbers 5, 9, ... 2n-1 in the two-port adapters are not used simultaneously and accordingly could have been replaced by only one location. If this is done then the number reduces to n' + 3 which is given in property 2. However, in this case the difference in successive memory locations needed in the computation of the flow diagram will increase with n (or n') which means that the number of bits in the instruction words needed for these locations will also depend upon n in the general case. The property 4 follows directly

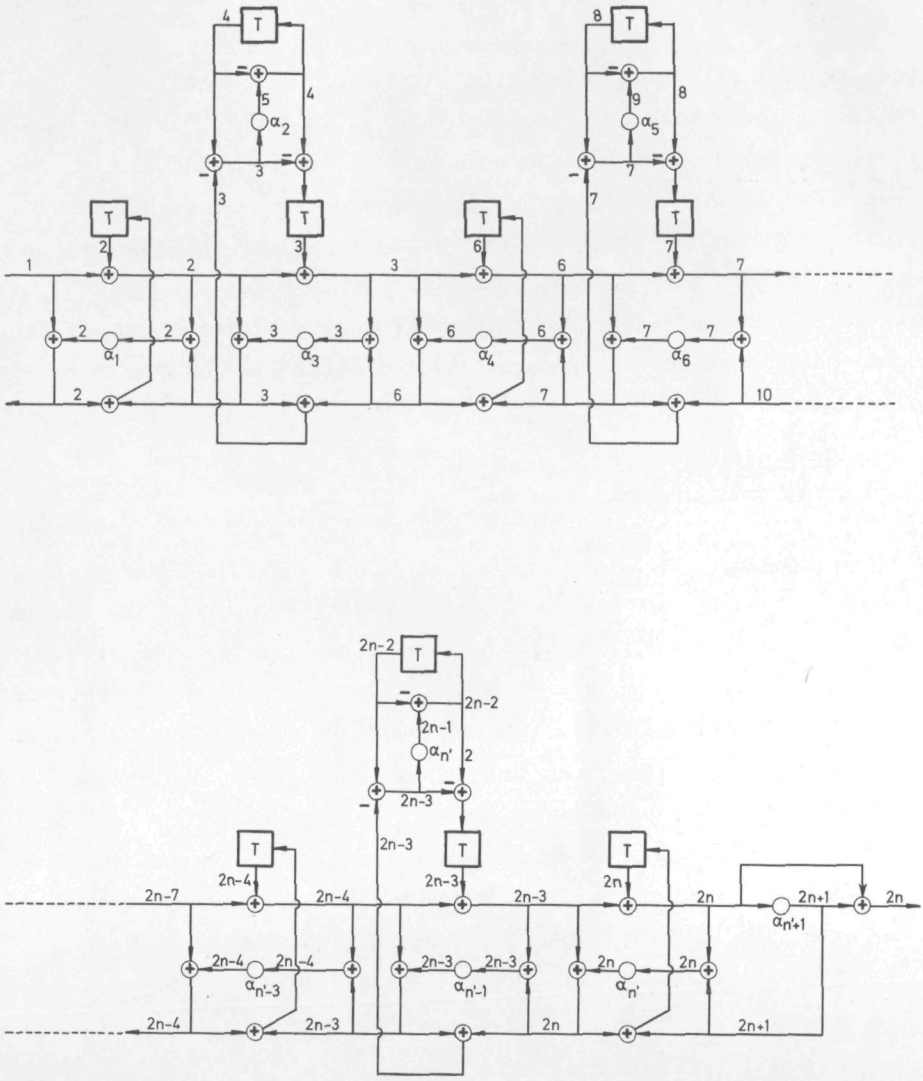


Fig. 5.11. Detailed flow diagram corresponding to fig. 5.10.

which completes the proof of the theorem.

A more general situation arises if, instead of only parallel resonant circuits in the series arms of the ladder as in figure 5.9, we now allow a first or second order impedance in each series or shunt arm of the ladder. However, in this case it can be proved in a straightforward way using methods already shown in the proofs of the theorems 5.1 and 5.2 that also in this more general case theorem 5.2 holds. It is essential to use only cascaded three-port series adapters and for the second order impedances the cascade of two unit elements has to be applied.

5.3.3 True ladder filters with scaling.

In the previous sections we have only discussed unscaled realizations. However, if scaling multipliers have to be introduced then the number of memory locations needed will increase. If we restrict ourselves to three-port series adapters of the structure used here and scaling multipliers are being shifted into the adapters (see figure 2.33) then it is easily verified that one extra memory location is needed in the adapter. If resonant circuits are present and therefore two-port adapters are used then this extra memory location can be the same one as for instance in figure 5.11 location 5. This is possible because they are not used simultaneously. We conclude that the number $n' + 3$ is sufficient for the ladder structures discussed sofar.

5.3.4 The general true ladder structure.

In the previous sections we did not discuss the canonic realization [53,54] of ladder filters. Due to the resulting bridged structure in that case it will not be possible to satisfy relation (5.2) and also the use of adapter equivalences to obtain only a cascade of three-port series adapters is less interesting because the resulting multipliers can no longer be shifted out of the network. The result is then also

the need of more memory locations than n' + 3.

We conclude the study of the flow diagrams of true ladder wave digital filter networks by the proof of the following theorem.

Theorem 5.3: For a general doubly terminated lossless ladder network a wave digital translation can be found having a flow diagram with the following properties:

Property 1.

The numbering of internal variables can be done in such a way that (5.2) is satisfied.

Property 2.

A number N of arithmetical memory locations such that

$$N = n' + 2 + x \ , \tag{5.7}$$

is sufficient for all the intermediate results to be stored simultaneously.

In (5.7) n' equals the number of lossless elements in the lossless network. In addition

x = 1 if scaling is applied,

x = 1 if resonant circuits are present,

x = 0 otherwise.

Property 3.

In the case the number of memory locations available is greater than the number given by (5.7), the value of x can be increased in order to simplify the coding of instructions especially for high order filters.

Proof:

If the order of the impedances in series- and shunt arms of the lossless ladder network is at most 2, then properties 1, 2 and 3 have been proved in sufficient detail in the theorems 5.1 and 5.2. It remains to be demonstrated for higher order impedances. This will be done by the example of figure 5.12, resulting in the figures 5.13 and 5.14.

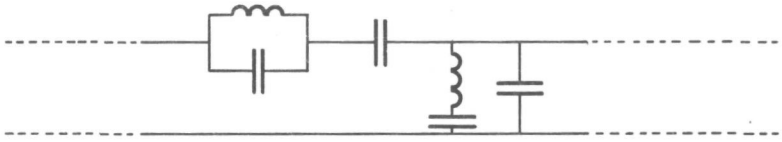


Fig. 5.12. Part of a ladder network in which the order of the ladder arm impedances is greater than 2.

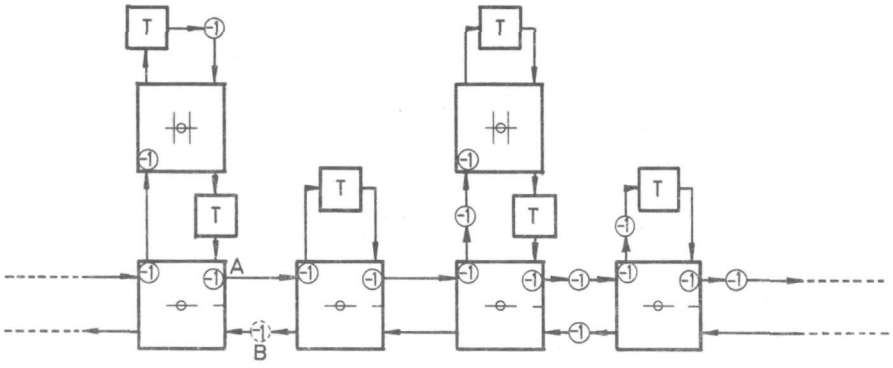


Fig. 5.13. Symbolic wave digital translation of fig. 5.12.

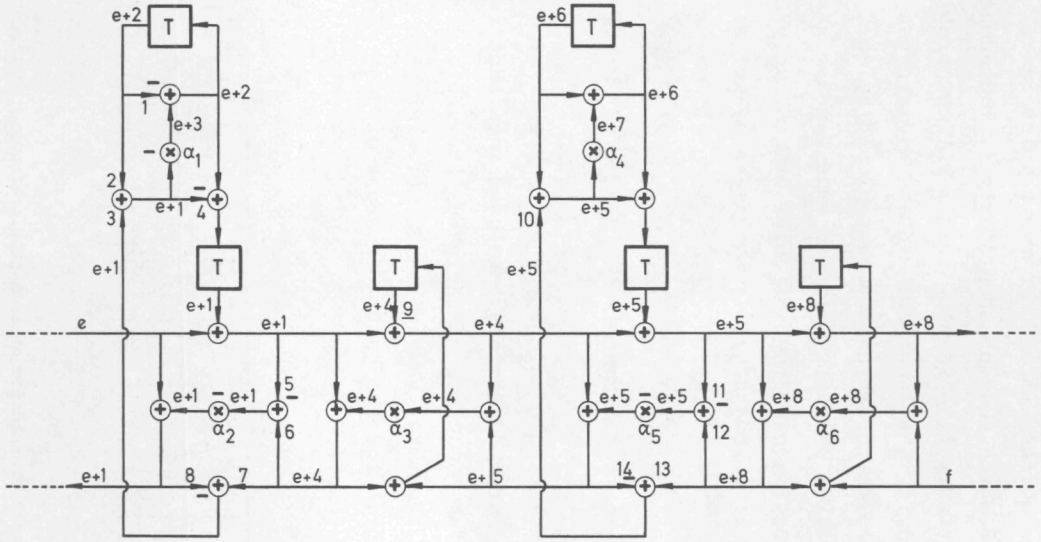


Fig. 5.14. Detailed flow diagram corresponding to fig. 5.13.

The only basic difference of figure 5.12 compared to previously discussed structures is that in this case at least two three-port series adapters are in cascade without (or both) being the result of an equivalence transformation from a three-port parallel adapter. To be able to satisfy (5.2) two inverters are shifted into the network which cancels inverter A and leaves inverter B which guarantees property 1. The numbering of internal variables in figure 5.14 is not minimal but comparable to the method used in figure 5.11. The locations e+3 and e+7 are not used simultaneously and could therefore have been replaced by one, leading to the numbering satisfying property 2 in the same way as in figure 5.11. For higher order impedances no basic difficulty arises, only the first and second Foster form of impedance realizations is essential. End of proof.

5.3.5 A cascade connection of unit elements.

In figure 5.15 the translation of a cascade of four unit elements is shown. One type of two-port adapter has been used such that inverters could be shifted out. The numbering of variables is such that relation (5.4) is satisfied and the total number is minimal. This can easily be generalized to be n + 1 for the general cascade of unit elements.

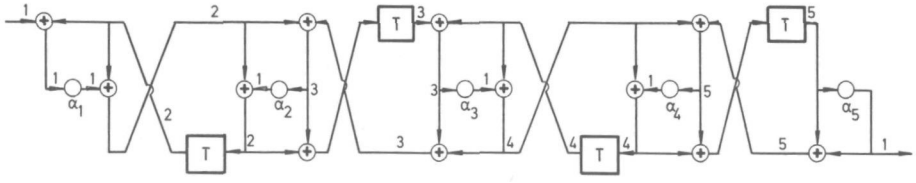


Fig. 5.15. Wave digital translation of a cascade of four unit elements.

The sequence of operations corresponding to figure 5.17 is given below.

input → 1	4 + 3 → 3	1 + 5 → 5
2 + 1 → 1	2 + 3 → 3	4 + 5 → 5
$1.\alpha_1$ → 1	$3.\alpha_2$ → 1	$5.\alpha_4$ → 1
1 + 2 → 2	1 + 2 → 2	1 + 4 → 4
4 + 3 → 3	2 + 3 → 3	4 + 5 → 5
$3.\alpha_3$ → 1	$5.\alpha_5$ → 1	
1 + 4 → 4	1 → output	

Without a further proof we state the following theorem concerning this structure.

Theorem 5.4.

A flow diagram, corresponding to a cascade connection of unit elements, can be given such that the following properties hold:

Property 1.

Relation (5.4) is satisfied.

Property 2.

The number of arithmetic memory locations is equal to n+1 and accordingly minimal (n is the order of the network).

It is clear from the above example that also in the case of lossless impedance realizations and thus for the Jaumann structure too, the number of memory locations needed, is proportional to n'. In this case n' is the number of delay elements T and also the order of the structure.

5.3.6 A cascade structure using only unit elements with characteristic impedance 1.

An example is shown in figure 5.16 where the order n=7.

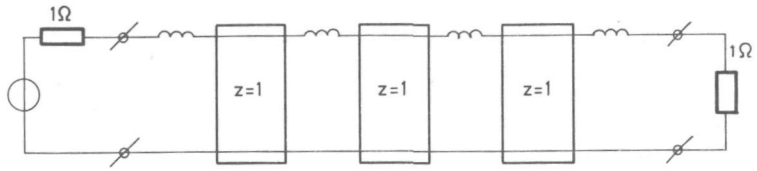


Fig. 5.16. A cascade structure for which the wave digital translation will contain only three-port series adapters with two ports of equal port impedances.

The schematic translation is shown in figure 5.17 and the flow diagram in figure 5.18. Due to the fact that unit elements of characteristic value z = 1 are used, the three-port series adapters only need one multiplier each.

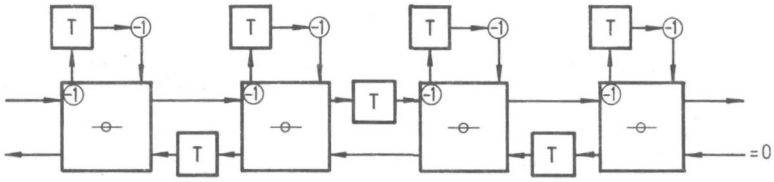


Fig. 5.17. Wave digital translation of of fig. 5.16.

We observe from figure 5.18 that relation (5.2) is satisfied, even with the plus sign and that the number of memory locations is 9, which can readily be generalized to n + 2.

5.3.7 A 5th order canonic lowpass filter network.

For details about the way of arriving at a canonic structure we refer to [53]. The relevant figures are 5.19, 5.20 and 5.21.

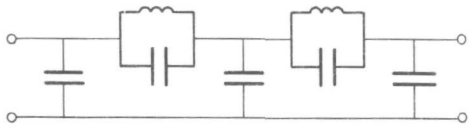


Fig. 5.19. A 5^{th} order lowpass filter network.

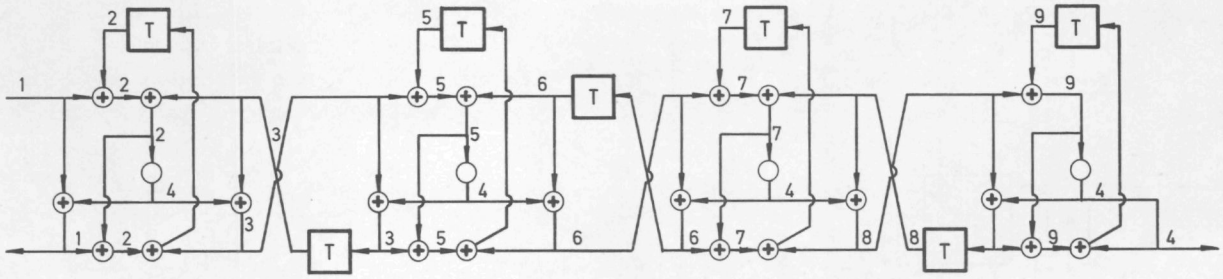


Fig. 5.18. Detailed flow diagram corresponding to fig. 5.17.

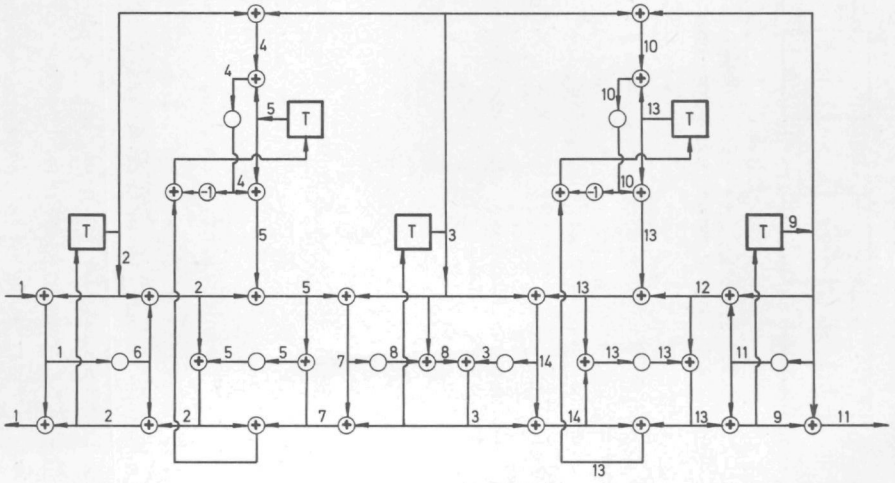


Fig. 5.21. Detailed flow diagram corresponding to fig. 5.20.

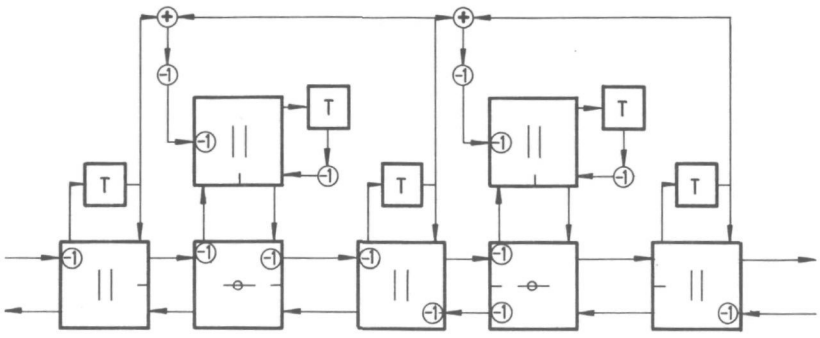


Fig. 5.20. Symbolic wave digital translation of fig. 5.19 using the canonic number of delay elements.

This example has been added to the contents of this chapter to indicate some consequences of (5.2) not being satisfied and the number of memory locations needed compared to other structures discussed.

5.4 Conclusions.

In this chapter we have discussed some algorithmic properties of the most important wave digital filter structures. We believe that these properties are relevant mostly for possible hardware applications in terms of microcontroller or microprocessor realizations especially those with the two-adress structure.
For the true ladder structure it is proved that the calculations can always be done in the form of (5.2), which enables one addition or subtraction to be performed in one clock cycle and shortens the instruction word length. We have also indicated that the number of memory locations needed in some structures increases with n' (n' equals the number of lossless analog elements) and not with 2n'. The minimal number of n' + 1 as been reached for the unit element filter and approached very closely for the general true ladder case. For this type of filter the optimal numbering of variables is such that the contents of the program memory needed can also easily be generated.

CHAPTER 6

A FLEXIBLE EXPERIMENTAL HARDWARE STRUCTURE FOR WAVE DIGITAL FILTERS

6.1 Introduction.

Already very early during the research in wave digital filter theory reported in these chapters, it was felt to be very helpful if a programmable hardware wave digital filter were available. It was decided to construct such a circuit to be able to study wave digital filter operation in an analog environment. This provides for signal handling flexibility, fast execution of experiments and real life testing of the proposed algorithms. Also, one can easily introduce experiments on the accuracy (number of bits) to be used.

6.2 Description of the structure.

Below we give a list of the major features and components of the structure.

1. Some major features and properties.

   a. Only bipolar TTL integrated circuits have been used (except for the program memory).
   b. The internal wordlength is 20 bits.
   c. Two's complement fixed point arithmetic is used.
   d. Input-output circuitry:
      A-D converter (12 bits), conversion time 25 μsec),
      D-A converter (12 bits). Also a 20 bit digital input and output is available. This output is shown using 20 LED's.

2. The arithmetical memory.

This memory consists of 64 words, 20 bits each.
The 16 x 4 bit random access memory TTL circuit SN7489 is used. As 3-state versions were not available at the time the construction was started, this memory has a separate input (8 to 1 line 20 bits multiplexer) and output (20 bits busline).

3. Arithmetical unit.

The following circuits have been used for the arithmetical operations.

a. A 20 bits parallel full adder.
b. A 20 bits two's complement inverter.
c. A 20 x 20 bits series-parallel multiplier ($\simeq$ 2 µsec.).
d. A circuit which is able to perform the operations necessary to suppress limit-cycle oscillations (see section 2.6).

It turned out that a very fast multiplier was not necessary, when the multiplier is busy it was nearly always possible to perform some other operation.

4. The program memory.

This memory consists of 1024 words of 11 bits each.
The 2102, a MOS, 1024 x 1 bit random access memory, access time $\simeq$ 0.7 µsec., has been used. As no loops will occur in the programs, a simple synchronous 10 bits binary counter can be used to adress the instruction words. We used a 0-1 Mhz clock frequency, which means that each 1 µsec. an 11 bits instruction word is available to be decoded into two main parts:

a. The operation to be performed (coded in 5 bits)
b. The arithmetical memory location which is involved (coded in 6 bits, $64 = 2^6$).

The list of 15 instructions and the corresponding code of 5 bits is given below:

1)	1 1 0 0 0	multiplier output to arithm. memory input
2)	1 1 0 0 1	output A-D converter to " " "
3)	1 1 0 1 0	inverter output to arithm. memory input
4)	1 1 1 0 0	full adder output " " " "
5)	1 1 1 1 0	"passifier" circuit output to arithm. memory input
6)	1 1 1 1 1	a coefficient (1 out of 16) " " " " (from 16x12 switches)
7)	1 0 0 0 0	from arith. memory to multiplier input A
8)	1 0 0 0 1	" " " " D-A converter
9)	1 0 0 1 0	" " " " inverter input
10)	1 0 0 1 1	" " " " full adder input A
11)	1 0 1 0 0	" " " " full adder input B
12)	1 0 1 1 0	" " " " "passifier" circuit input
13)	1 0 1 1 1	" " " " multiplier input B
14)	0 1 1 1 1	reset of program counter
15)	0 0 0 0 0	start A-D converter.

Obviously, the coding of instructions has not been done in an optimal way (15 instructions could have been coded using 4 bits), but in order to simplify the decoding an extra bits was used.

The program memory is loaded by a self-developed card reader which reads "1" s and "0" s from 80-column IBM cards. Each column of such a card can carry an 11 bits instruction + 1 bit clock signal, which means that a filter program uses quite few cards as a permanent storage.

5. The coefficient memory.

This memory consists of switches, 16 coefficients of 12 bits each can be adjusted, read in or changed manually during filter operation

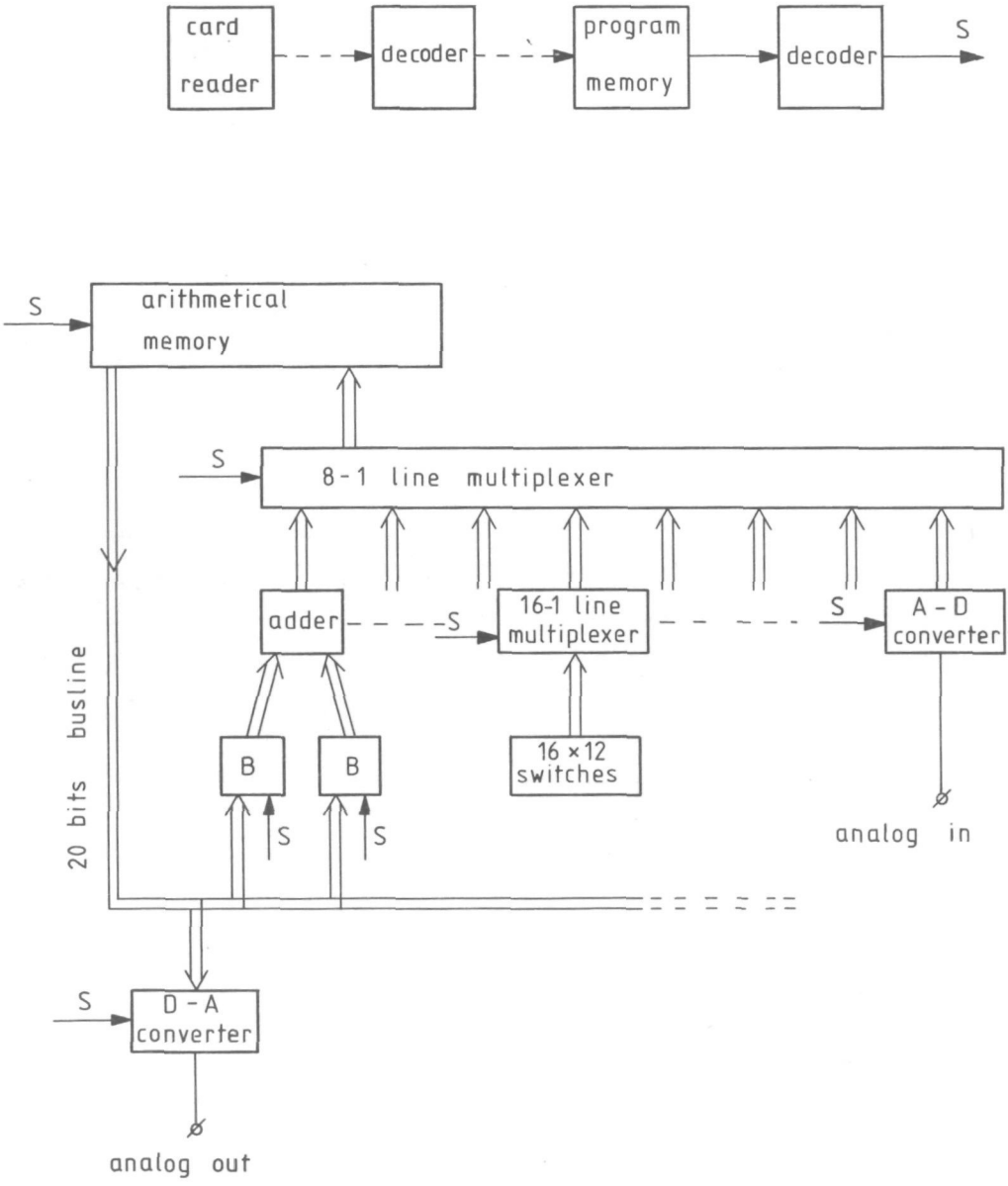


Fig. 6.1. Block diagram of the experimental programmable wave digital filter hardware (only a part of the arithmetical circuits is shown).

making coefficient sensitivity observation quite easy. The decimal value of each coefficient can range between +2 and -2, being the range of most coefficients used in wave digital filters.

Having explained the various components of the structures briefly, the block diagram in figure 6.1 shows the global picture. The various arithmetical circuits are connected between the busline and one input of a 8 to 1 line multiplexer input through buffer circuits. In the next section a fully programmed example is given.

6.3 A program example.

A number of wave digital filters have been programmed. We mention here for instance a 10th order bandpass filter and a 16th order elliptic function lowpass filter. For details we refer to [70,71]. We conclude this section by showing the details of one simple example, namely the wave digital network discussed in section 2.6, shown in figure 2.56 and reproduced here for convienence.

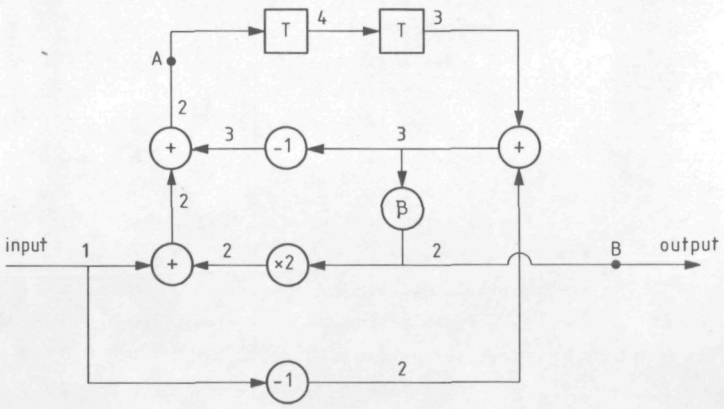


Fig. 6.2. Possible flow diagram corresponding to a simple w-plane damped series resonant circuit.

At the points A and B the passifying operation as discussed in section 2.6 has been applied to prevent the occurrence of zero-input limit cycles or overflow-oscillations.

instruction number from list of instructions	operation to be performed + arithm. mem. location involved	binary code in program memory
2	A-D converter output → 1	1 1 0 0 1 0 0 0 0 0 1
15	start A-D converter	0 0 0 0 0 0 0 0 0 0 0
9	1 → inverter input	1 0 0 1 0 0 0 0 0 0 1
3	inverter output → 2	1 1 0 1 0 0 0 0 0 1 0
6	read in coeff. B	1 1 1 1 1 0 1 0 0 0 1
10	3 → adder input A	1 0 1 0 0 0 0 0 0 1 1
11	2 → adder input B	1 0 0 1 1 0 0 0 0 1 0
4	adder output → 3	1 1 1 0 0 0 0 0 0 1 1
7	3 → multiplier input	1 0 0 0 0 0 0 0 0 1 1
13	coeff. B → multiplier input	1 0 1 1 1 0 1 0 0 0 1
9	3 → inverter input	1 0 0 1 0 0 0 0 0 1 1
3	inverter output → 3	1 1 0 1 0 0 0 0 0 1 1
1	multiplier output → 2	1 1 0 0 0 0 0 0 0 1 0
12	2 → input pass.operator	1 0 1 1 0 0 0 0 0 1 0
5	output pass.op. → 5	1 1 1 1 0 0 0 0 1 0 1
8	5 → D/A converter input	1 0 0 0 1 0 0 0 1 0 1
10	2 → adder input A	1 0 1 0 0 0 0 0 0 1 0
11	2 → adder input B	1 0 0 1 1 0 0 0 0 1 0
4	adder output → 2	1 1 1 0 0 0 0 0 0 1 0
10	2 → adder input A	1 0 1 0 0 0 0 0 0 1 0
11	1 → adder input B	1 0 0 1 1 0 0 0 0 0 1
4	adder output → 2	1 1 1 0 0 0 0 0 0 1 0
10	2 → adder input A	1 0 1 0 0 0 0 0 0 1 0
11	3 → adder input B	1 0 0 1 1 0 0 0 0 1 1
4	adder output → 2	1 1 1 0 0 0 0 0 0 1 0
9	4 → inverter input	1 0 0 1 0 0 0 0 1 0 0
3	inverter output → 4	1 1 0 1 0 0 0 0 1 0 0
9	4 → inverter input	1 0 0 1 0 0 0 0 1 0 0
3	inverter output → 3	1 1 0 1 0 0 0 0 0 1 1
12	2 → input pass.operator	1 0 1 1 0 0 0 0 0 1 0
5	output pass.operator → 4	1 1 1 1 0 0 0 0 1 0 0
14	reset program counter	0 1 1 1 1 0 0 0 0 0 0

Example of a filter program.

The total number of instructions to be executed each sampling period equals 32 which leads to a sampling frequency of 31.2 kHz if the program counter clock frequency equals 1 MHz. This example gives an idea of the actual speed of the system. One addition for instance takes 3 μsec, one multiplication takes 5 μsec but during the busy period of 2 μsec another two-cycle operation can be performed.

6.4 Conclusions and remarks.

A flexible, and easily programmable, experimental hardware wave digital filter has been briefly described. Using it, a lot of insight has been gained in various properties of wave digital filters such as suppression of parasitic oscillations, necessity of scaling, internal resonance effects and sensitivity to multiplier coefficient accuracy variations.

CHAPTER 7

ON THE MULTIPROCESSOR IMPLEMENTATION OF DIGITAL SIGNAL PROCESSING ALGORITHMS IN GENERAL AND WAVE DIGITAL FILTERS IN PARTICULAR

7.1. Introduction.

The material presented in this chapter is based on the contents of the references 46 and 47. In this chapter we explore a number of design problems for the concurrent implementation of digital signal processing algorithms in general and wave digital filter flow diagrams in particular. Today, most of the published work on implementation of digital signal processing algorithms is concerned with the design of very fast operating special purpose hardware. For instance, for the Fast Fourier Transform very fast hardware exists [8]. In this chapter however we will explore some possibilities of a more flexible implementation. For instance, it may be very advantageous to have programmable hardware which can serve several purposes simply by changing the contents of some memories, and use it in combination with a minicomputer. In the rest of this section the problem of parallel processing is addressed. In section 7.2 we discuss a method to treat concurrency problems. In section 7.3 we introduce the concept of Petri nets [72,73] which is used for modeling purposes. In section 7.4 we give finally some detailed examples of wave digital filter flow diagrams implemented using parallel operating processing units.

Parallel processing.

We mention three major applications of parallel processing:

1. The parallel processing of jobs on a general purpose computer. The proper handling of these jobs involves the design of operating systems through the theory of concurrent processes [74 - 77].
2. Parallel operating computers, each handling specific parts of jobs [78].
3. Parallel operating processing units such as microcomputers, controllers, hardware multipliers, FFT processors etc., implemented to process algorithms such as digital filters in one or more dimensions, fourier transforms or convolutions, processing various signals in real time [17].

The first two mentioned applications have in common that the nature of the jobs to be handled, is unknown to the designer of the system. The third application has the feature that each algorithm is known in detail. We will restrict ourselves to this last mentioned application. A statement which is relevant for this application has been given by Stone [79] and is written below:

> "One of the most important, yet least understood, aspects of parallel processing is the effect of interconnections of registers and processing units on computational speed"

Stated otherwise, we have the following problem:

Problem.

> Given a flow diagram in terms of additions/subtractions, multiplications and delay elements, what is the "best" (in some sense to be defined) way to implement this flow diagram in a flexible manner using a number of parallel operating processing units.

To be more specific, we give three examples of flow diagrams next.

Example 1: A wave digital filter structure.

Various flow diagrams of filters for given specifications can be found. The problem is then to find a flow diagram which can most effectively be split into parts to be implemented using processing units operating synchronously or asynchronously. Modularity might be obtainable this way. In this respect, the true ladder wave digital filter structure will be shown (in section 7.4) to be worse compared to the Jauman structure.

Example 2: An FFT algorithm [8,80,81].

An FFT algorithm for a certain number of points may be realized in a number of different flow diagrams. Figure 7.1 shows such an algorithm schematically having n_1 input and n_2 output points. This algorithm can be split into parts in various different ways, for instance by drawing horizontal and/or vertical lines in the corresponding flow diagram. Each possibility leads to entirely different parts having quite different properties. The result may not even be computable.

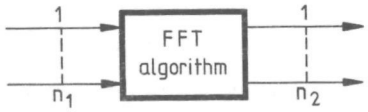


Fig. 7.1. An FFT algorithm having n_1 inputs and n_2 outputs.

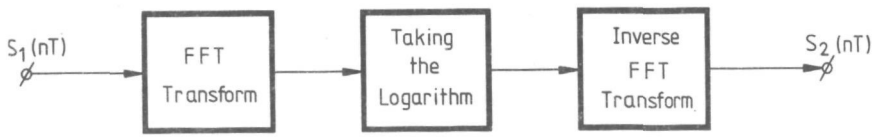


Fig. 7.2. Part of a homomorphic speech analysis system.

Example 3: The homomorphic speech analysis system [17].

Part of this system is shown in figure 7.2 where $s_1(nT)$ and $s_2(nT)$ are both time signals. A lot of computations is needed here. For real time operation, fast and parallel operating programmable hardware might be designed.

In this chapter we will only study example 1 in some detail and formulate only some aspects concerning the more general problems of the examples 2 and 3. With the above examples in mind we can be more precise about the main problem stated before. Some more detailed problems are:

1. How is the flow diagram to be split into parts? What is the number of parts and what is their relationship. In this respect the concepts of pipelining [82] and precedence graphs [83] need be mentioned.
2. Has the splitting into parts been done in such a way that dead-locks are avoided [84,85]? Such a splitting into parts is only then computable. Finding out whether a particular splitting into parts is computable or not and when there are a lot of possibilities, calls for an efficient way of testing in a computer aided interactive way.
3. Will the parallel system operate synchronously or asynchronously? This means, shall the designer decide on fixed speeds of processors and calculations or not? In this respect the definitions of Kung [86] are of importance. He distinguishes between:
   a. Synchronic operation. Here we have fixed speeds of processors and operations.
   b. Synchronized operation. Here we do not assume any speed relation. We do assume however, that variables need to be exchanged between the various units. At the time of an exchange between units, one of the two may have to wait for the other.
   c. Asynchronic operation. In this case, processors operate on, globally available data in an independent way.
4. How shall the interconnection of the several units be implemented [79]?
5. What is the amount of memory needed and where should it be located (concentrated in one memory or distributed amongst the various processing units)? This choice will lead to quite different situations.
6. What is the speed of the system which can be obtained?
7. What is the computational efficiency of the various units used?
8. What is the sensitivity to the system speed of some speed variation on one or more processing units or types of operations to be performed?

The first major problem which arises is that of computability. This problem isaddressed in the next section.

7.2. Processes, causality relations, causality graphs and computability.

Definition of a process.

> Each connected part in which a flow diagram has been divided, is called a process.

The number of processes may be different from the number of processing units on which the processes are to be implemented. For each process we have to define a sequence in which the calculations take place. This ordering can be expressed in terms of a causality relation.

Definition of a causality relation.

> A causality relation for a process defines a sequence in which inputs are needed in the computational scheme and outputs become available.

Each process will now be modeled by a causality relation. This model is however not unique in general.

Example:

> The process of figure 7.3 can be modeled using the causality relation shown in figure 7.4. The vertical line in figure 7.4 represents the sequence of computations in the process. Only the variables which are needed by or from other processes are indicated by arrows. The input and output variables are ordered along the vertical line according to their need or availability in the computational sequence. Each process can be modeled this way and after that the various causality relations are connected by connecting the arrows having the same variable number. The structure which results is called a causality graph.

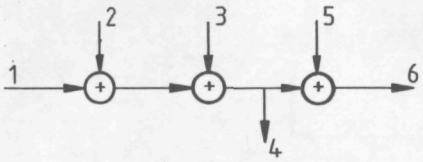


Fig. 7.3. Example of a simple process.

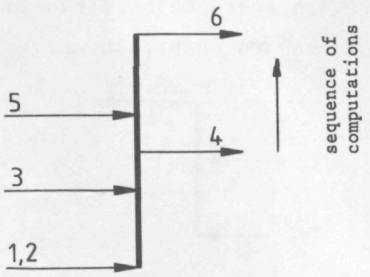


Fig. 7.4. Causality relation corresponding to fig. 7.3.

Definition of a causality graph.

> The causality graph is the graph which results when all the causality relations corresponding to the various processes are connected by connecting all the arrows having identical variable numbers.

In the general case where we have n_1 processes to be implemented using n_2 processing units ($n_1 \geq n_2$) in a synchronized way we may need some kind of a control processor to assure that exchange of variables between units is performed in a correct way. In the case of a synchronic implementation we can find out in the design stage in which sequence and at what clock cycle instant specific variables can be exchanged.

The dead-lock problem.

The problem which now arises in the causality graph is that of computability. First we may want to distinguish between two cases A and B if more than one causality relation is to be implemented on one processing unit.

Case A: We predetermine the sequence in which the relations are to be calculated by the processor.

Case B: We do not predetermine this sequence but we let it be determined by the sequence in which variables needed, become available.

This choice influences the occurrence of dead-locks. An example is shown in figure 7.5 where we have two causality relations X and Y to be implemented on one processor, showing also the variables 1 until 5.

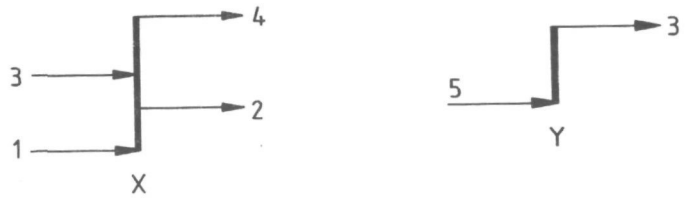


Fig. 7.5. The causality relations X and Y.

Suppose the variables 1 and 5 are known and suppose we have case A which can mean first X then Y in this example. We have dead-lock because variable 3 will never be computed because we cannot finish relation X. In case B, the processor not having available variable 3 will skip to relation Y, calculate 3, return to X and calculate 4. No dead-lock in case B. For case A, let us combine the relations to be implemented in one processor according to their computational scheme. We can now introduce the following definition.

Definition of a proper directed circuit.

A proper directed circuit in a causality graph is a directed loop in the graph which is closed in the following way:

a. The direction of arrows must be followed.
b. Inside the causality relations (or the combined causality relations in case A) the computation sequence must be followed.

An example is given in figure 7.6 where the relations from figure 7.5 are combined.
The following theorem concerning the presence of these loops can now be proved.

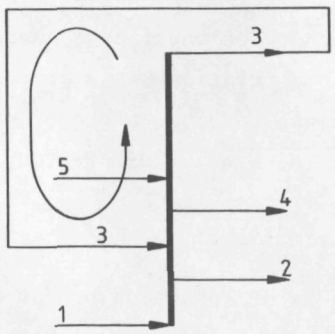


Fig. 7.6. Combination of the X and Y.

Theorem 7.1.

A necessary and sufficient condition for dead-lock is the occurrence of at least one proper directed circuit in the causality graph.

Proof:

First we combine the causality relations for which we want case A to hold, into one relation such that we are left with, say n, causality relations for which case B holds. Together they form the causality graph to be implemented using an unspecified number of processing elements.

Proof of the necessary condition:

Suppose n_1 out of the n relations are left unfinished (dead-lock). One of these relations, say R_1, waits for an input from (there are two cases):

1. Relation R_1 itself, a result which would have become available at a later stage if R_1 could have been proceded on. This means there is a proper directed circuit in R_1 itself. End of proof.
2. Another relation, say R_2, which cannot be finished either. For R_2 we have the same two possibilities:
   Either R_2 is unfinished because of lack of a result which would have been available at a later stage in R_2 itself or because of lack of

a result from another relation, say R_3, etc.
This has to terminate because of the finite number n_1 of relations which are unfinished. Either some relation has a proper directed circuit by itself, or some relation has to close a proper directed circuit involving a number of n_2 relations ($n_2 \leq n_1$). End of proof.

Proof of the sufficient condition.

In this case there is at least one proper directed circuit within the causality graph which means that there is a part of this graph which cannot be calculated. This means that some number of relations are unfinished and this means that some number of processing elements are waiting for inputs never to come: dead-lock. End of proof.

In figure 7.7 a causality graph is shown consisting of 4 causality relations. One proper directed circuit is present involving two of the relations (R_1 and R_2). Three relations (R_1, R_2 and R_3) cannot be finished (inputs 1 and 5 are assumed to be known initially).

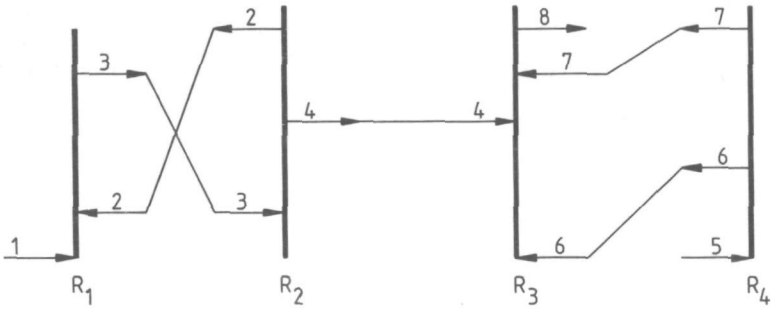


Fig. 7.7. Causality graph having one proper directed circuit.

7.3. Petri nets.

Petri nets and related models are being used to model various systems. For an interesting introduction and references to the existing literature we refer to [72,73]. A Petri net is used to model the interconnection of modules. For example arithmetic units, parts of programs or whole processors. Each module is represented by a "transition", the symbol is a bar. Each transition will have inputs and outputs for which the symbol is a circle. These circles are called "places". These places are connected to the transitions by directed arcs. To be able to indicate the flow in the Petri net the places are marked by a nonnegative number of "tokens". In our case the presence of a token will indicate that a variable has been calculated and/or is available. A transition is said to be enabled or firable if each of its input places contains at least one token. Firing a transition consists of removing from each input place one token and adding one token to each output place. This is explained in figure 7.8 where the situation before and after firing the transition is shown.

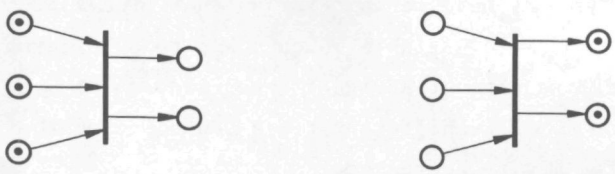


Fig. 7.8. Distribution of tokens before and after firing the transition.

In our case we want to model the partitioning of a given flow diagram consisting of adders/subtractors, multipliers and delay elements. In the previous section these various parts have been called processes and the computability of the interconnection of the processes has been studied. In this section we will study the timing of the various processes and its interconnections. For timing purposes, for instance in the case of an addition, the type of operation to be performed is not of importance but only the number of inputs which have to be present at the same time and the computation time for the operation to be performed. For that reason it is

of use to construct a Petri net model for the flow diagram to be computed. Each arithmetical operation in the flow diagram will be represented by a transition. The sequence in which the computations take place can be indicated by the presence of tokens. In the case of a digital filter flow diagram the initial marking will show tokens at the state variables.
As we want to do the whole sequence of computations in a number of separate processing elements, we have to divide the complete Petri net model into parts corresponding to the processes from the previous section. Each process consists of course of a number of trasitions in general, which we will combine into one "modified" transition. Because we also study the timing we will also include in the modified transition the various time slots needed. Different arithmetical or input/output operations may take different times or clock cycles. To mention some:

1. One addition or subtraction of two variables.
2. A multiplication by a constant.
3. Taking a variable to an output port of a processor.
4. Exchange of a variable between two processors.
5. One processor may have to wait for another processor to finish the computation of some variable which needs to be exchanged.
6. In a processing element having the two-address structure an addition or subtraction may take different times dependent whether it involves two or three memory addresses.

A simple example.

Suppose we have the process shown in figure 7.9. For simplicity we will assume the following three times needed (these assumptions will be valid also in the rest of this chapter).

1. Addition/subtraction : 1 time slot.
2. Multiplication : 10 time slots.
3. Input/output of a variable : 1 time slot.

The modified Petri net model of figure 7.9 is given in figure 7.10. So far, we have assumed that inputs b and d were available at the time they were needed. This may not be the case in general. If input b is available at time slot 4 the model of figure 7.10 changes into that of figure 7.11.

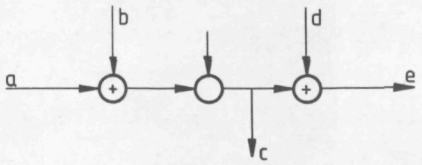


Fig. 7.9. A simple sequence of computations.

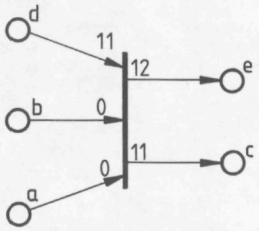


Fig. 7.10. Modified transition corresponding to fig. 7.9 and showing the relevant time instants.

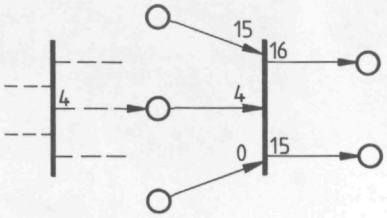


Fig. 7.11. Situation in fig. 7.10 when an input is only available later.

In the next section we will give two, more complete, examples of wave digital filters.

7.4. Two examples of wave digital filters.

The general procedure is as follows:

1. The flow diagram is split into parts. Each part is computable.
2. The number of processors is fixed. The same number of modified Petri net transitions is constructed. Because the examples are simple, a test for dead-lock occurrance is not necessary, this can be done by inspection.

First example: A fifth order Cauer-type lowpass true ladder filter.

The adapter network is shown in figure 7.12 and the corresponding flow diagram in figure 7.13. The flow diagram is split into 6 parts, given in the figures 7.14, 7.16, 7.18, 7.20 and 7.22 (twice). The corresponding modified Petri net transitions are given in the figures 7.15, 7.17, 7.19, 7.21 and 7.23 (twice).

We discuss in some detail the two-, three- and four processor case now but first we observe from figure 7.13 that the whole flow diagram takes 106 time slots (one processor case).

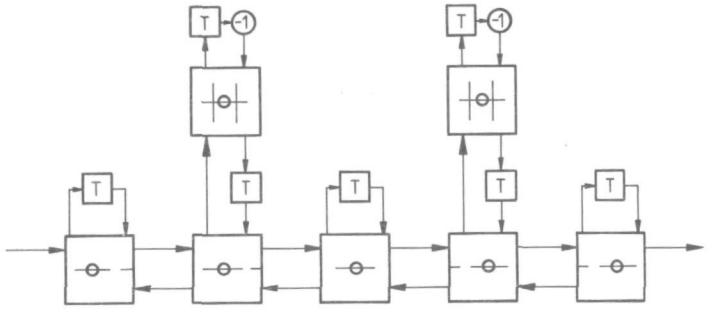


Fig. 7.12. Fifth order wave digital lowpass filter network.

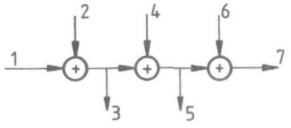


Fig. 7.14. Part of fig. 7.13.

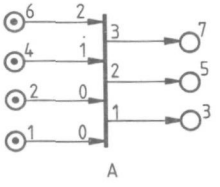


Fig. 7.15. Modified transition corresponding to fig. 7.14.

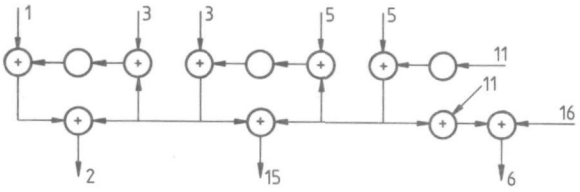


Fig. 7.16. Second part of fig. 7.13.

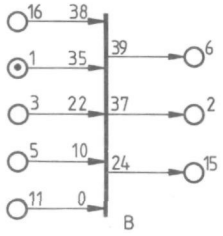


Fig. 7.17. Modified transition corresponding to fig. 7.16.

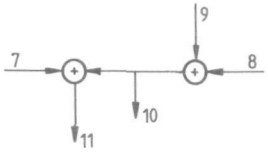


Fig. 7.18. Third part of fig. 7.13.

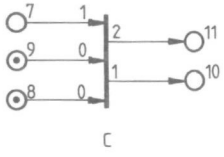


Fig. 7.19. Modified transition corresponding to fig. 7.18.

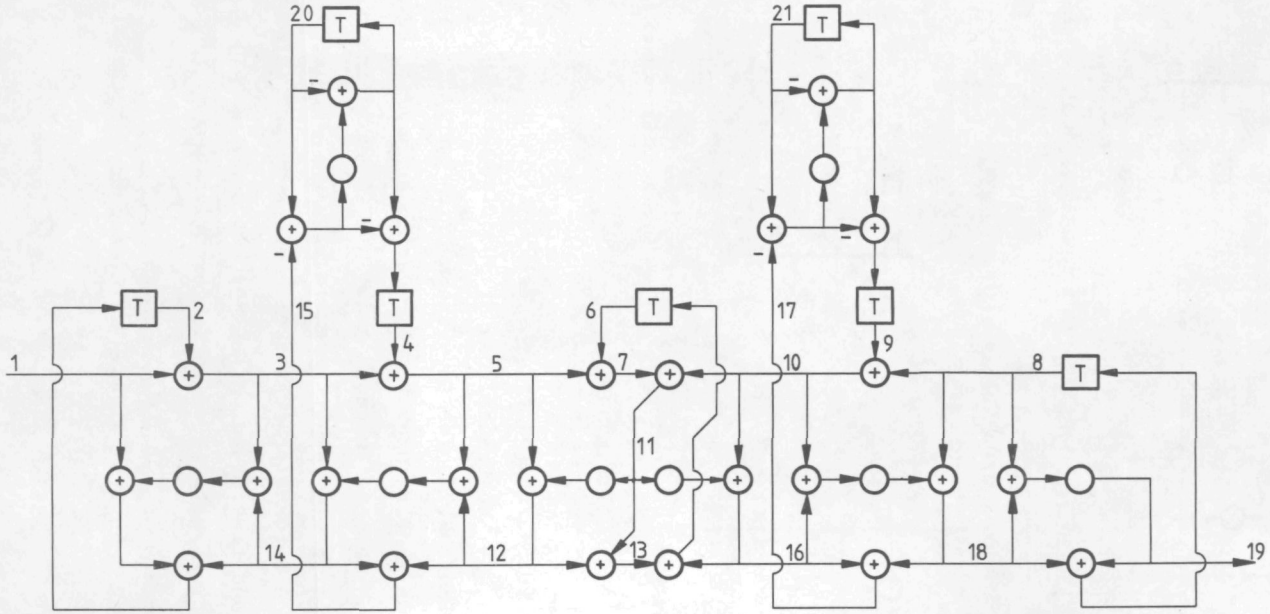


Fig. 7.13. Flow diagram corresponding to fig. 5.12.

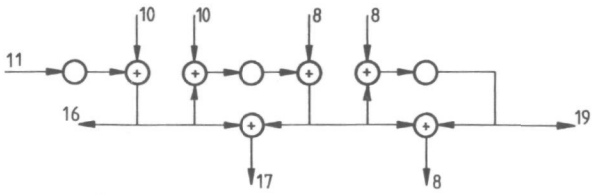


Fig. 7.20. Fourth part of fig. 7.13.

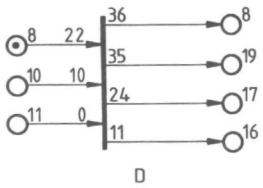


Fig. 7.21. Modified transition corresponding to fig. 7.20.

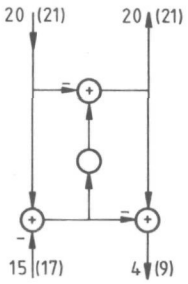


Fig. 7.22. Fifth (sixth) part of fig. 7.13.

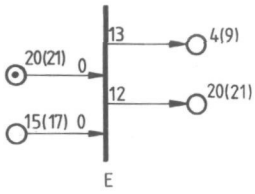


Fig. 7.23. Modified transition corresponding to fig. 7.22.

Two processor case.

We combine the transitions of the figures 7.15, 7.17 and 7.23 into the one given in figure 7.24 and the transitions of the figures 7.19, 7.21 and 7.23 are combined into figure 7.25. The two figures 7.24 and 7.25 correspond to the two processors we want to use. Because variables have to be exchanged, these two transitions have to be connected. This is shown in figure 7.26. Finally, a useful timing diagram is given in figure 7.27. In this figure, a distinction is made between processor time slots during which computations are actually done, and time slots during which the processors are waiting or exchanging variables. Only those variables which are exchanged, are shown in this figure.

The entire scheme takes 60 time slots. The efficiency of the both processors can be calculated as:

processor 1: $55/60 \times 100\ \% = 91.6\ \%$ (approx.).

processor 2: $51/60 \times 100\ \% = 85\ \%$ (approx.).

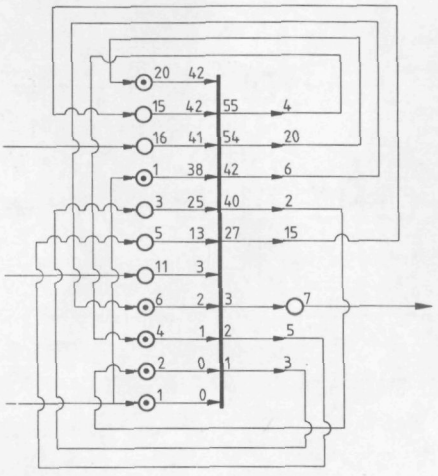


Fig. 7.24. Combination of the transitions of fig. 7.15, 7.17 and 7.23.

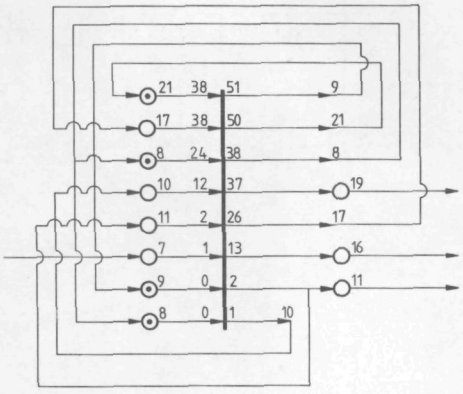


Fig. 7.25. Combination of the transitions of fig. 7.19, 7.21 and 7.23.

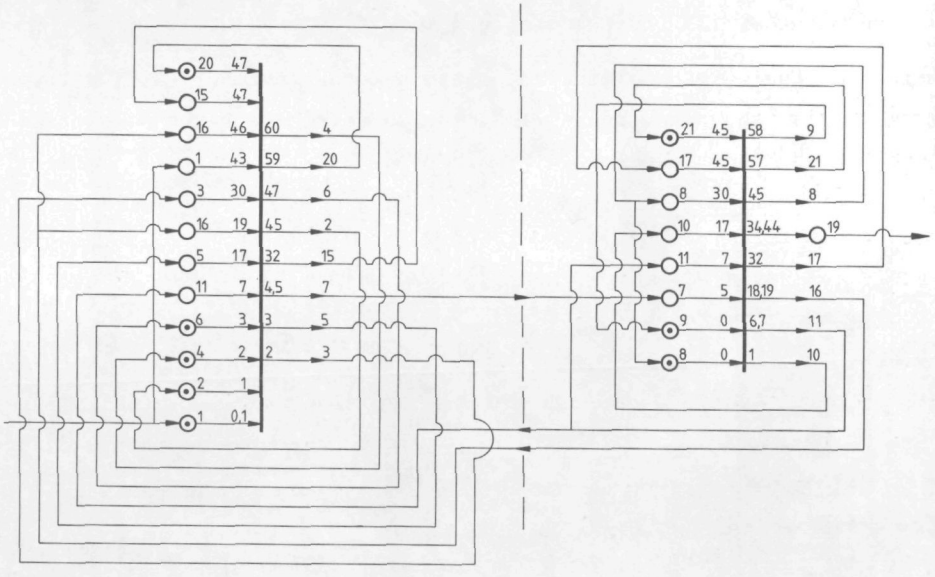


Fig. 7.26. A two processor implementation of fig. 7.13.

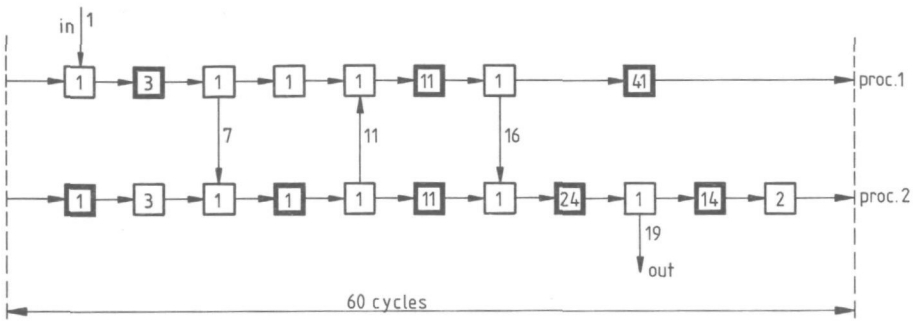


Fig. 7.27. Timing diagram corresponding to fig. 7.26.

Three processor case.

We make the following three combinations of transitions.

1. The figures 7.15 and 7.17 combine into figure 7.28.
2. The figures 7.19 and 7.21 combine into figure 7.29.
3. The figures 7.23 (twice) combines into figure 7.30.

Combining these three modified transitions leads to figure 7.31 with its timing diagram shown in figure 7.32. The whole scheme takes 61 slots (60 in the two processor case).

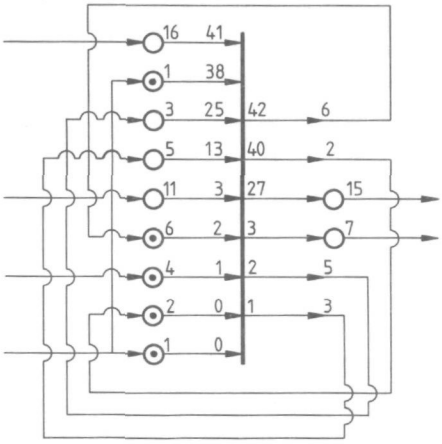


Fig. 7.28. Combination of the transitions of fig. 7.15 and 7.17.

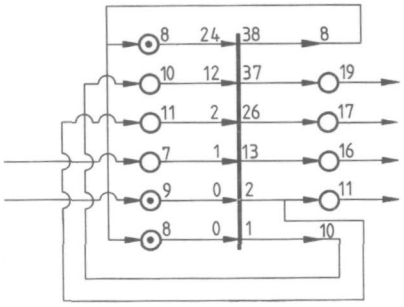


Fig. 7.29. Combination of the transitions of fig. 7.19 and 7.21.

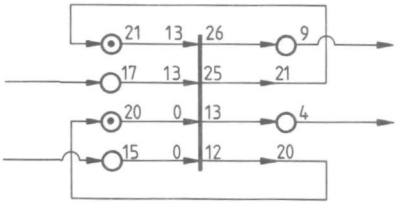


Fig. 7.30. Two transitions from fig. 7.23 combined.

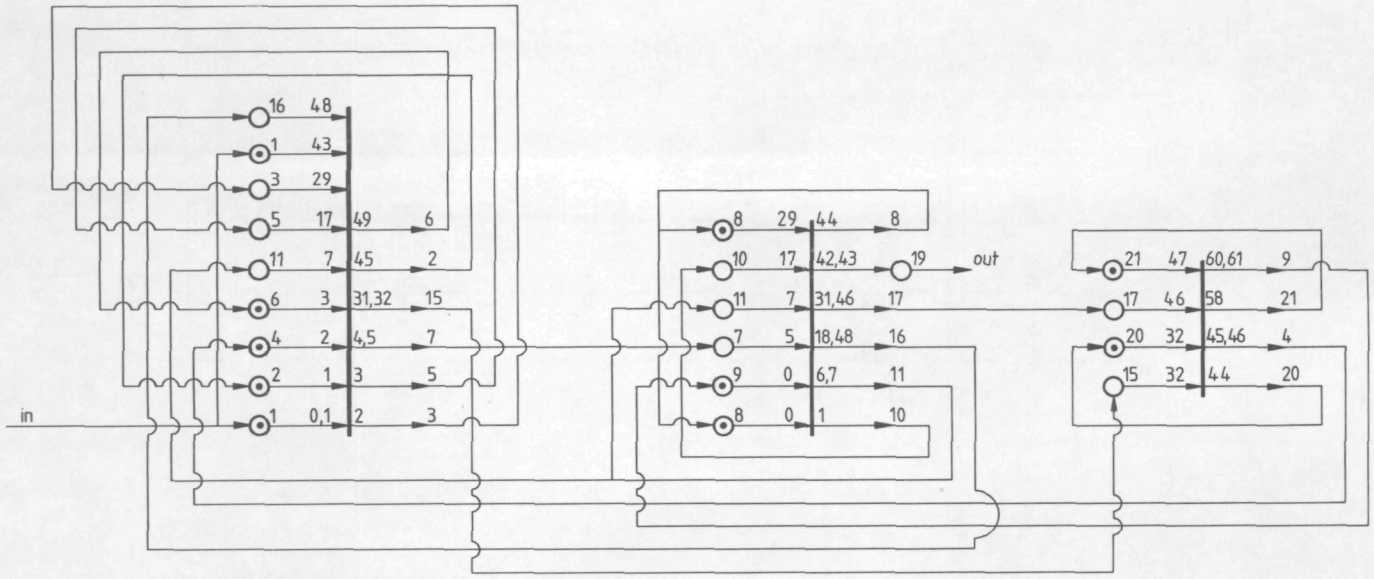


Fig. 7.31. A three processor implementation for fig. 7.13.

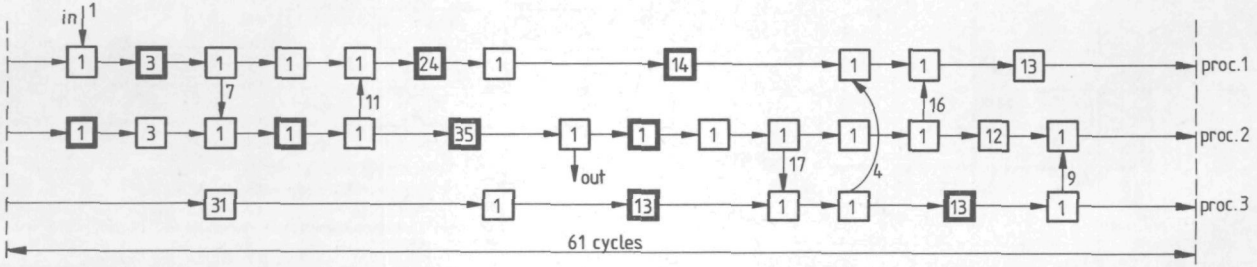


Fig. 7.32. Timing diagram corresponding to fig. 7.31.

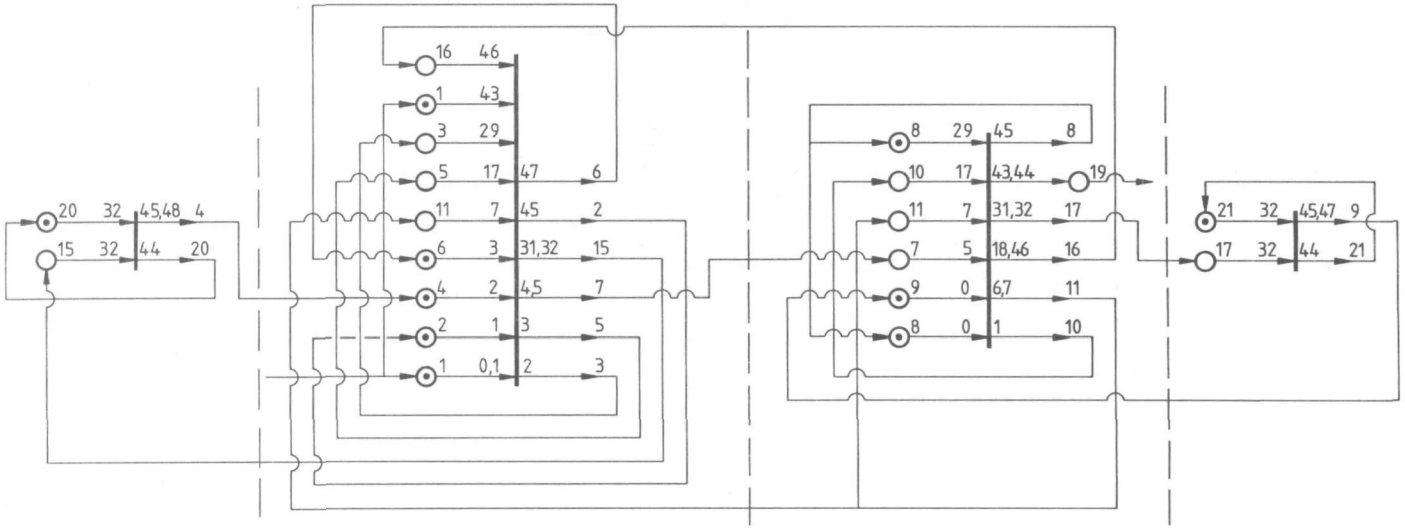


Fig. 7.33. A four processor implementation of fig. 7.13.

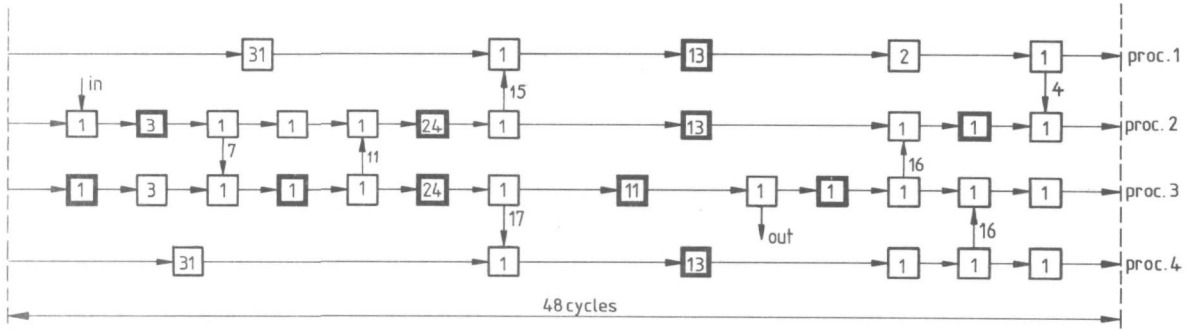


Fig. 7.34. Timing diagram corresponding to fig. 7.33.

Four processor case.

The only difference here with the three processor case is that now the both transitions from figure 7.23 are implemented in separate processors. This leads to figure 7.33 with the timing diagram shown in figure 7.34. In this case 48 time slots are needed.

Second example: A fifth order lowpass Jauman filter structure.

The chosen network is given in the figures 7.35 and 7.36. The same type of processing modules with the same calculation times as in the first example are assumed.

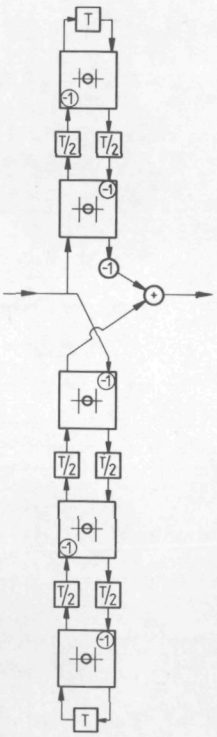


Fig. 7.35. A fifth order Jauman structure.

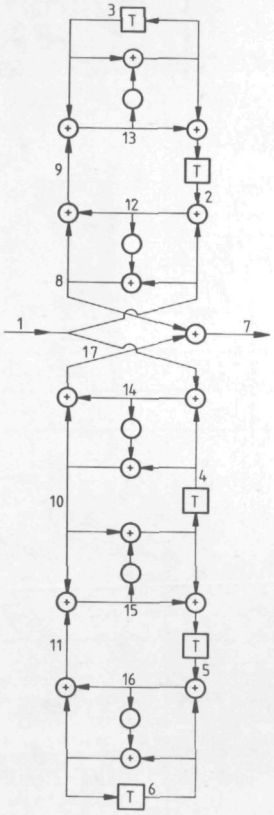


Fig. 7.36. Possible flow diagram corresponding to fig. 7.35.

The three processor case.

For this example we will only give a three processor implementation. The three transitions corresponding to the three parts in which the flow diagram of figure 7.36 has been divided, are given in figure 7.37. The three processor implementation is shown in figure 7.38 with the timing diagram in figure 7. 39. The entire calculation scheme takes 29 time slots in this case. This means quite a reduction compared with the three processor implementation of the first example.

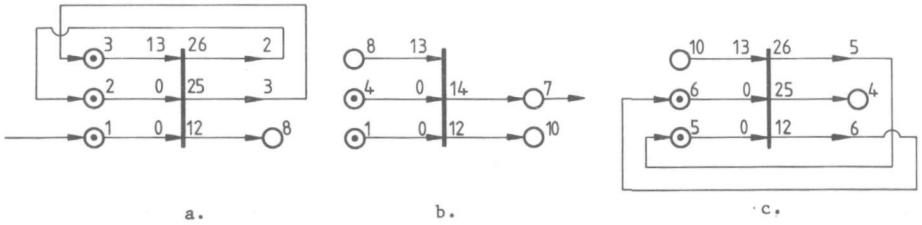


Fig. 7.37. Three transitions corresponding to three parts of fig. 7.36.

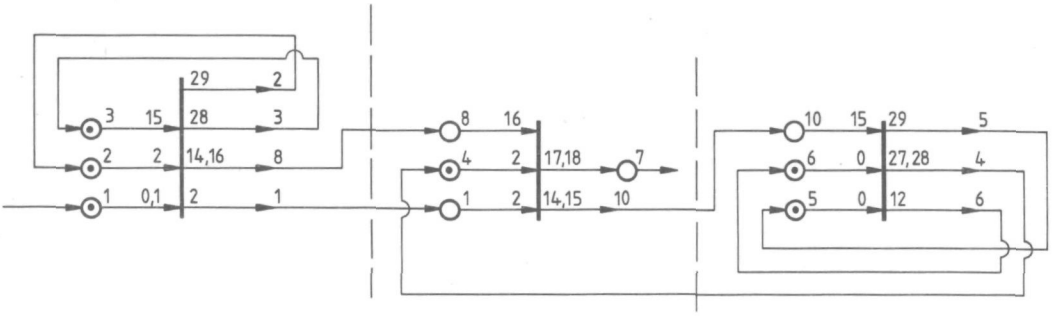


Fig. 7.38. A three processor implementation of fig. 7.36.

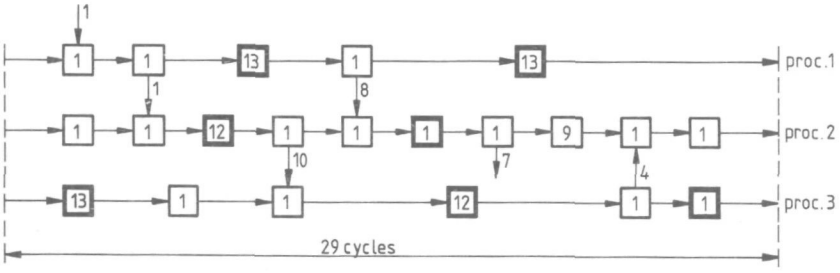


Fig. 7.39. Timing diagram corresponding to fig. 7.38.

Two remarks can be given regarding this implementation.

1. It can easily be shown that in this second example the multiplication time slots could have been increased until 18 reaching then the same total number of time slots needed as in the three processor implementation of the first example.
2. If the filter order is increased by 2, leading to two extra adapters, and we also add one processor, we can keep the total number of time slots needed nearly constant. Of course, this assumes the same multiplier coefficient accuracy. This indicates some kind of modularity for this Jauman structure.

7.5. Conclusions.

1. Only a very limited part of the whole problem of multiprocessor implementation of signal processing algorithms has been explored. However, the proposed methods are believed to be very powerfull. If the flow diagrams to be implemented, for instance a Discrete Fourier Transform algorithm, become more complex, the whole method should be programmed and used in an interactive way.
2. In the case a dead-lock is found, the question of what should be changed in the partitioning in order to avoid this dead-lock is important and needs more investigation.
3. In the examples we have supposed that all the modules were identical and able of performing all the operations needed. The method however, can equally well be used if this is not the case and for instance separate multipliers are used.
4. Both examples have been designed for synchronic operation. Of course, the assumptions of time slot needed for each operation will have a great influence on the final result and in general there will be more types of operations needed in the case a single-chip or single-board computer is used as building block in a multiprocessor implementation.
5. The first example shows clearly that a true ladder wave digital filter network is not split very efficiently in more than two parts. The introduction of extra unit elements could lead to improvement in this situation. The second example shows that the Jauman network has quite

different properties in this respect. However, the Jauman structure is more sensitive, especially in the stopband. If attenuation poles are needed to be well defined in terms of frequency and of good quality in terms of db's suppression, it may be necessary to choose other implementations for the impedances in the Jauman network than those chosen in the example which may be less efficiently operated in parallel in the multiprocessor case.

6. The problem of modeling calculation processes and processor structures is studied by various authors at this moment. References 87 and 88 give examples in this respect.

CHAPTER 8

SAMENVATTING

Met de snelle technologische vooruitgang in digitale komponenten, schakelingen en systemen, is ook de signaalbewerking door middel van digitale technieken steeds zinvoller geworden [1-10]. Een van de mogelijkheden van digitale signaalbewerking is digitale filtering. Een digitaal filter is een diskrete-tijd systeem wat bestaat uit optellers, vermenigvuldigers en geheugenelementen. Dit systeem werkt op een reeks getallen als ingangssignaal en verwerkt dit tot een uitgangsreeks van getallen met behulp van een rekenalgoritme. Een digitaal filter kan in verschillende vormen worden gebruikt. We noemen enkele.

1. Een digitaal filter kan analoge signalen verwerken door middel van bemonstering en omzetting in digitale vorm. Het blokschema van figuur 8.1 ontstaat dan.

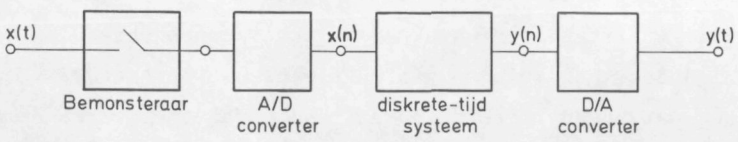


Fig. 8.1. Een digitaal filter werkend in een "analoge omgeving".

De signalen x(t) en y(t) in figuur 8.1 zijn analoge signalen en x(n) en y(n) zijn de hiermee overeenkomende reeksen getallen.

2. Een digitaal filter kan signalen verwerken die al in digitale vorm zijn en dit ook blijven.
3. Een digitaal filter kan gebruikt worden ter simulatie van een analoog, continue systeem op een digitale computer.
4. Een digitaal filter kan eenvoudig als een algoritme gebruikt worden, geprogrammeerd op een computer en werkend op getallen.

Digitale filtering wordt (of zal in de naaste toekomst worden) gebruikt in verschillende toepassingsgebieden. Hieronder volgen enkele.

1. In de telecommunicatie. Speciaal in de digitale transmissie, omzetting van FDM naar TDM (of omgekeerd) [11-13], toondetectie, echo onderdrukking.
2. Verwerking van spraaksignalen, of meer algemeen, het verwerken van signalen in het audio gebied. Hier zijn bijvoorbeeld de problemen van spraak analyse en synthese voor het beperken van de benodigde bandbreedte [14,15], en de synthese van muziek.
3. Het verwerken van meerdimensionale data zoals bijvoorbeeld televisie beelden [16].
4. Het verwerken van radar en sonar signalen.
5. Het verwerken van signalen afkomstig van aardbevingen of bodem exploratie.

Voor meer details over deze toepassingen verwijzen we naar Oppenheim [17].

Digitale filtering heeft een aantal voordelen:

1. Flexibiliteit. Filter karakteristieken kunnen eenvoudig worden gewijzigd door het inlezen van enkele nieuwe parameters. Een digitaal filter wat geconstrueerd is met behulp van snel werkende komponenten, kan meerdere filters tegelijk verwezenlijken.
2. Betrouwbaarheid. Een aantal problemen zoals toleranties, afmetingen, enz., zoals die bij analoge systemen kunnen optreden, kunnen hier vermeden worden. In de plaats daarvan kunnen op eenvoudige wijze identieke systemen geconstrueerd worden en hele systemen op een LSI chip integreren.

3. Nauwkeurigheid. De nauwkeurigheid van een digitaal filter kan veel beter zijn dan van een corresponderend analoog filter. Beperkingen ontstaan veelal bij de overgang naar de "analoge omgeving".
4. Enkele mogelijkheden die uniek zijn voor diskrete-tijd systemen. Bij digitaal filteren ontstaan mogelijkheden die analoog niet te realiseren zijn. We kunnen bijvoorbeeld digitale filters ontwerpen met exact lineair fase verloop. Ook kunnen stabiele meerdimensionale filters worden ontworpen.

De bovengenoemde voordelen en mogelijkheden, de moderne LSI technologie en het beschikbaar zijn van uitgebreide rekenfaciliteiten zijn de reden voor de snelle ontwikkeling van het vakgebied der digitale filtering en signaalbewerking. De principes van digitale filtering worden reeds lang toegepast in bemonsterde regelsystemen [18] en de ontwerp methodes die in dit gebied zijn ontwikkeld, worden nog steeds gebruikt. Om aan te sluiten bij moderne mogelijkheden en toepassingen worden ze echter verder ontwikkeld. Een van deze moderne ontwikkelingen is het digitale golffilter [19] en dit type filter is behandeld in de vooraf gaande hoofdstukken. De studie van de digitale filtermethoden omvat verschillende onderwerpen:

1. De lineaire theorie wordt ontwikkeld ten behoeve van nieuw te vinden realizaties en methoden voor het ontwerp. Ruis en dynamisch bereik zijn enkele concrete onderwerpen hieruit.
2. De nietlineaire theorie omvat de studie van stabiliteit in diskrete-tijd systemen, overflow en mogelijke parasitaire oscillaties. Strukturen die equivalent zijn wat de lineaire theorie betreft, kunnen zeer verschillende nietlineaire eigenschappen bezitten.
3. De implementatie. De studie van dit aspect omvat het ontwerp van computer programma's zowel als de ontwikkeling van snelle filterschakelingen werkend "in real time".

De digitale golffilters vormen een klasse van digitale filters en zijn geintroduceerd als digitale simulaties van, met weerstanden afgesloten, verliesvrije LC filters [20-26] en de microgolffilters bestaande uit eenheidselementen [27-30]. Dit vanwege de mogelijkheid de uitstekende eigenschappen van deze filters te behouden in de digitale situatie. De belangrijkste

eigenschappen, hier bedoeld, volgen nu.

1. De bovengenoemde analoge, verliesvrije filters, speciaal de ladderstrukturen, hebben in de doorlaatband een lage gevoeligheid voor variaties van elementen. Bovendien kunnen dempingspolen in de sperband gemakkelijk worden afgeregeld (in het geval van een laddernetwerk). Deze eigenschappen kunnen worden behouden in de bijbehorende digitale golffilters [31,32], de eerstgenoemde eigenschap heeft tot gevolg dat slechts een geringe nauwkeurigheid van vermenigvuldigingscoefficienten nodig is. Dit maakt het mogelijk zeer selectieve digitale filters te ontwerpen met slechts geringe nauwkeurigheid van coefficienten. Eeveneens geeft het aanleiding tot prettige ruis- en dynamisch bereik eigenschappen [35,36].
2. De inherente stabiliteit en, nog belangrijker, het op vermogensoverdracht gebaseerd zijn van deze met weerstanden afgesloten verliesvrije filters, leveren in het corresponderende golffilter unieke stabiliteitseigenschappen. Dit in tegenstelling tot de situatie bij conventionele digitale filters [35,36].

Ook kunnen enkele nadelen van digitale golffilters worden genoemd.

1. Het stroomschema van een digitaal golffilter van graad n is ingewikkelder dan het corresponderende conventionele digitale filter van graad n en met dezelfde overdrachtsfunctie. Er zijn meer rekenbewerkingen nodig.
2. Digitale golffilters zijn minder modulair van opbouw dan de conventionele strukturen.

Voorbeeld: De overdrachtsfunktie H(z) die de amplitudekarakteristiek oplevert, zoals die in figuur 1.2 te zien is (slechts de eerste halve periode) is:

$$H(z) = \frac{z^3 + 3z^2 + 3z + 1}{345.1z^3 - 819.3z^2 + 665.8z - 183.6} = \frac{Y(z)}{U(z)} \qquad (8.1)$$

(De hier gebruikte variabelen en symbolen zijn gedefinieerd in hoofdstuk 2).

Een conventioneel schema voor (8.1) is gegeven in figuur 8.3. De coefficienten in (8.1) zijn eveneens coefficienten in figuur 8.3. Het schema van een corresponderend golffilter is te zien in figuur 8.4. Hierin hebben we $\alpha_1=\alpha_3=0.1367$, $\alpha_2=0.0212$ (afgerond op 4 decimalen)

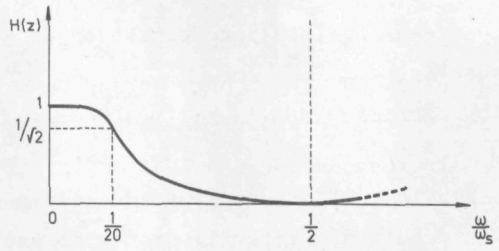


Fig. 8.2. De amplitude karakteristiek van overdrachtsfunktie (8.1).

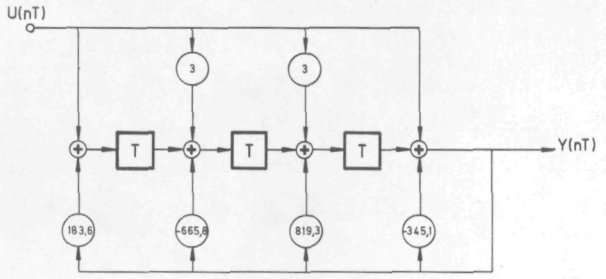


Fig. 8.3. Een conventioneel schema voor overdrachtsfunktie (8.1).

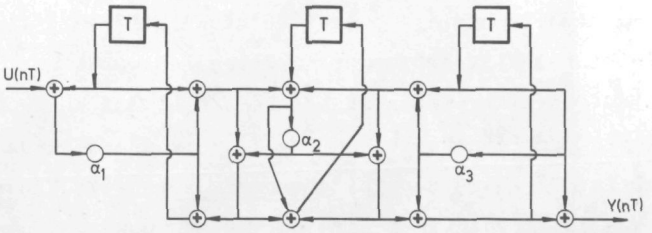


Fig. 8.4. Het schema van een digitaal golffilter voor overdrachtsfunktie (8.1).

Het verschil in complexiteit is duidelijk. Een indruk van het verschil in gevoeligheid voor beide netwerken wordt nu gegeven. Een afwijking in de vierde decimaal van een coefficient in figuur 1.3 (819.3 → 819.4) heeft een effect in de tweede decimaal van $H(z)\big|_{z=1}$. Voor figuur 8.4 heeft een afwijking van α_1 van 0.1367 naar 0.1368 een verandering in $H(z)\big|_{z=1}$ tot gevolg die binnen de afronding valt.

Tenslotte geven we nog een samenvatting van de inhoud van de hoofdstukken 1 tot en met 7.

Hoofdstuk 1.
Dit hoofdstuk omvat een engelstalige versie van de samenvatting die in hoofdstuk 8 gegeven is.

Hoofdstuk 2.
Hier wordt het digitale golffilter geintroduceerd vanuit de klassieke LC filters, de conventionele digitale filters en de eenheidselementenfilters. Dit is gedaan om het lezen van de volgende hoofdstukken te vereenvoudigen. Er is echter geen poging gedaan tot volledigheid, zowel voor hoofdstuk 2 als de corresponderende literatuurlijst. De belangrijkste kenmerken van de golffilters (lineair zowel als nietlineair) zijn kort behandeld, hoofdzakelijk voor de ladderstruktuur. Dit is een klasse golffilters die verkregen wordt door middel van een vertaalprocedure uit de klassieke LC ladderfilters. In de hoofstukken 3 en 4 wordt deze beperking grotendeels opgeheven.

Hoofdstuk 3.
Uit de LC synthese theorie is de Jauman struktuur bekend. Het is een geaarde tweepoort equivalent aan de symmetrische kruistakschakeling. De Jauman struktuur maakt het mogelijk overdrachtsfunkties te realiseren die in de ladder vorm niet realiseerbaar zijn. Bovendien wordt het "kanonieke" aantal elementen gebruikt. Kanoniek betekent hier dat het aantal elementen (alleen de frekwentie-afhankelijke) gelijk is aan de graad van de overdrachtsfunktie. De enige beperking van de Jauman struktuur is de symmetrie. In termen van de impedantie matrix parameters houdt dit laatste in dat $Z_{11} = Z_{22}$ geldt. Een nadeel van de Jauman struktuur is dat de karakteristieke eigenschappen van de ladderstruktuur natuurlijk afwezig zijn. In dit hoofdstuk wordt de Jauman struktuur in digitale vorm vertaald en aangetoond dat het digitale netwerk kanoniek is in het aantal vermenigvuldigers.

Hoofdstuk 4.

Een bekende methode uit de LC synthese theorie maakt gebruik van een splitsing van de overdrachtsmatrix (gebaseerd op verstrooingsparameters) in stukken van lagere orde. Op deze manier kan een algemene overdrachtsfunktie (binnen de beperkingen van realiseerbaarheid) gesynthetiseerd worden met behulp van stukken van de nulde, eerste en tweede orde. Omdat deze stukken niet de ladderstruktuur bezitten, faalt in het algemeen hier de vertaalprocedure in digitale vorm. Deoorzaak hiervan is het optreden van vertragingsloze rekenlussen. In dit hoofdstuk wordt aangetoond dat de methodiek wel lukt als extra vertraging in de vorm van eenheidselementen aan de klemmen van het tweepoort netwerk wordt toegevoegd. Het is niet mogelijk gebleken, verliesvrije golffilters te vinden, slechts passiviteit is gegarandeerd. De betekenis van verliesvrijheid en passiviteit in dit verband is gegeven in hoofdstuk 2.

Hoofdstuk 5.

De inhoud van dit hoofdstuk is gericht op mogelijke implementatie van golffilters gebruik makend van flexibele hardware. Voor een aantal verschillende filterstrukturen (de ladderstructuren inbegrepen) worden rekenschema's gegeven die zodanig zijn dat een minimaal aantal (of dichtbij dit minimale aantal) geheugenplaatsen nodig zijn voor het tijdelijk opslaan van tussenresultaten. Ook worden zodanige nummeringen van interne variabelen gegeven dat in elke programma instruktie, die één rekenkundige bewerking definieert, slechts de informatie van twee geheugenplaatsen (en dus twee variabelen) nodig is. Dit laatste is efficient bijvoorbeeld in het geval van implementaties met de twee-adres struktuur.

Hoofdstuk 6.

In dit hoofdstuk wordt experimentele hardware beschreven die gebouwd is om de werking van digitale golffilters te kunnen bestuderen in een analoge omgeving. De verschillende rekenschema's zijn gemakkelijk programmeerbaar en vermenigvuldigingscoefficienten zijn zeer eenvoudig in te stellen, wat het bepalen van gevoeligheid voor coefficientenvariaties vergemakkelijkt.

Het geheel werkt zodanig snel dat een sinus-oscillator gebruikt kan worden als bron van het ingangssignaal en een oscillograaf of een spectrum analyser voor de bestudering van het uitgangssignaal.

Hoofdstuk 7.

De mogelijkheden van multiprocessor implementatie worden in dit hoofdstuk bekeken. Hoewel alleen voorbeelden van golffilters worden gegeven, is de gebruikte methodiek toepasbaar voor meer algemene algoritmen uit de digitale signaalbewerking. Als deze algoritmen in stukken worden verdeeld om door aparte processoren te worden verwerkt, bestaat de mogelijkheid van "dead-lock". Het resultaat van dead-lock is dat het gehele rekenproces stopt en niet verder wordt afgemaakt omdat processoren wachten op rekenresultaten van andere processoren die om dezelfde reden staan te wachten. Er wordt een theorema over het optreden van dead-lock gegeven. De stof die in dit hoofdstuk wordt gegeven is slechts bedoeld ter inleiding. Het totale probleem van de multiprocessor implementatie van rekenalgoritmen uit de digitale signaalbewerking is een combinatie van het vinden van de juiste processor struktuur, de programmering van die struktuur en het zoeken naar de meest efficiente algoritmen.

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LEVENSBERICHT.

De schrijver van dit proefschrift werd op 8 oktober 1941 te Tzummarum (Friesland) geboren. In 1958 behaalde hij het MULO B diploma aan de Christelijke school voor MULO te Sint Annaparochie en ging daarna naar de H.T.S. te Leeuwarden waar in 1962 het diploma van de studierichting Elektrotechniek verkregen werd. Tenslotte werd op 2 februari 1968 het diploma van Elektrotechnisch ingenieur behaald aan de Technische Hogeschool te Delft.

Sinds 1 augustus 1966 is hij werkzaam aan de Technische Hogeschool te Delft bij de vakgroep Netwerktheorie, eerst als technisch ambtenaar en sinds 2 februari 1968 als wetenschappelijk medewerker.

Daar verrichtte hij wetenschappelijk onderzoek, eerst in de passieve netwerksynthese en later in de filtertheorie. Het onderzoek dat geleid heeft tot het samenstellen van dit proefschrift werd gestart in 1972. Zijn belangstelling gaat nu vooral uit naar de implementatie met behulp van programmeerbare hardware van geschikte algoritmen uit de digitale signaalbewerking en de modeleringsproblemen die hierbij een rol spelen.

S T E L L I N G E N

Het bewijs van de mogelijkheid (of onmogelijkheid) stabiele, kanonieke, verliesvrije, digitale golffilters te ontwerpen met willekeurige overdrachtsfunktie, zou een waardevolle bijdrage zijn aan de theorie van de digitale golffilters.

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Het verband tussen de theorie van de automorphe funkties en de approximatietheorie van filterkarakteristieken verdient meer aandacht van netwerktheoretici.

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Om een systematische synthese van digitale processornetwerken voor digitale signaalbewerking mogelijk te maken is het noodzakelijk dat hiervoor basiselementen worden gedefinieerd.

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Het onderzoek naar de invloed van verschillende processorstrukturen op de verwerking van een digitale datastroom is een onontgonnen gebied.

- - - - - - - - - - -

Het totale probleem van de multiprocessor implementatie van rekenalgoritmen uit de digitale signaalbewerking is een combinatie van het vinden van de meest efficiënte algoritmen, de juiste processorstruktuur en de programmering van die struktuur.

- - - - - - - - - - -

Volgens sommigen dient het vakgebied der Elektrotechniek zich te ontwikkelen binnen de grenzen van de huidige vakgroepsindeling in onze afdeling. Het opkomen van digitale signaalbewerking als een belangrijk vakgebied is echter een bewijs van de noodzaak bestaande strukturen te doorbreken.

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Het verdient overweging op stations in Nederland vertrektijden en aankomsttijden van treinen in dezelfde mate te vermelden.

- - - - - - - - - - -

De bezorgdheid van chauffeurs van vrachtauto's voor andere weggebruikers lijkt soms omgekeerd evenredig aan het tonnage van hun voertuig.

- - - - - - - - - - -

De stelling:

"Een bewijsvoering is in veel gevallen niet meer dan een gebrek aan verbeeldingskracht."

is onvoldoende bewezen.

- - - - - - - - - - -

De betiteling van het Christendom als "een beweging", zoals dit werd gedaan in een recente televisie uitzending, plaatst dit Christendom bewust of onbewust naast afscheidings- en vrijheidsbewegingen en is af te keuren.

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