DELFT UNIVERSITY OF TECHNOLOGY

Precision Current Mirror

by

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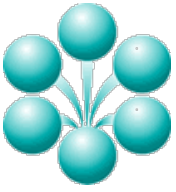
ELECTRONIC AND INSTRUMENTATION



July 2010

Declaration of Authorship

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Abstract

Faculty of Electrical Engineering, Mathematics and Computer Science
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This thesis is about an innovative technique of designing a precision current mirror which enables us to achieve a very high DC accuracy with ripple free output signal, without using an external low pass filter to suppress the unwanted ripple. The word 'precision' here means that the current mirror has an accurately defined input-to-output relationship in terms of gain, linearity and offset. The idea behind this design is basically a combination of trimming followed by Dynamic element matching (DEM). Test chips are fabricated to test the functionality and performance of the new concept. The DC accuracy obtained from the mirror is 0.18% and AC ripple is suppressed by 50X compared to state-of-the-art. The chip area (without padring) is 0.84mm^2. The supply voltage ranges from 11V to 40V. This design was done using a high performance analog process (50HPA07HV) from Texas Instruments (TI). This is a high voltage BiCMOS process (40V compatible) having minimum gate length of 0.6um analog devices compatible with 0.3um gate length digital....

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Dedicated to my mother...

Chapter 1

Introduction

1.1 Motivation

A current mirror shown in the figure 1.1 is a common block used in most analog circuits. As the name indicates, a 'Current Mirror' is a circuit which is used for copying the current. M1 is a diode connected, which acts as input device and M2 acts as output device. The aspect ratio of M1 and M2 are kept same to make 1:1 mirror. Same gate-source voltage across M1 and M2 ensures equal current flow through both the devices (neglecting non-idealities). IIn is the input current that needs to be copied and IOut is the output current from the mirror. 'R' is the load resistance.
The word 'precision' with reference to current mirrors means that the mirror should have an accurate input-to-output relationship in terms of gain error, non-linearity and offset. Some important specifications should always be considered during the design of the current mirror which can rate it as a 'good' or 'bad' mirror. These specifications are as follows:

1) Error - The difference between input and output currents is usually expressed, in terms of gain, offset and non-linearity.

2) Small signal output resistance - This determines the fluctuations in the current level with respect to the voltage applied at the output of the mirror. Ideally, a current mirror should have infinite output impedance, which means that the current mirror should produce the same current regardless of the output voltage variations.

3) Compliance voltage limit - This indicates how much voltage headroom the current mirror requires to work properly. The lower the compliance voltage, the better is the

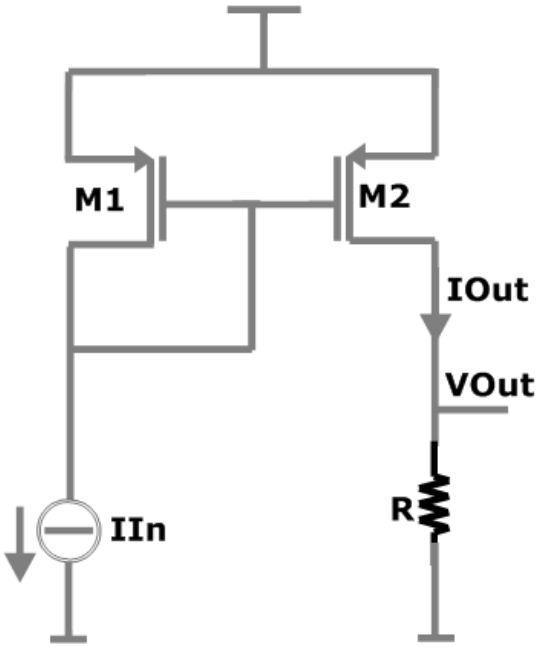


FIGURE 1.1: Simple current mirror

mirror.

Current mirrors are used as biasing blocks for opamps, generating an analog output in current steering DAC, industrial current drivers and in many other applications. Current mirror errors (due to mismatch) deteriorate the performance of precision analog circuits. A few industrial products that rely heavily on the precision of a current mirror for their use in other applications are discussed next.

The XTR111 [4] is a precision voltage-to-current converter from Texas Instruments. The typical DC accuracy of XTR111 is 0.015%, over a wide output current range from 0-25mA. This is, to date, the most accurate voltage-to-current converter reported. Moreover, the quiescent current reported for this product is quite low at 550μA. However, the main disadvantage of this product is the AC ripple at the output, which restricts its use in many applications where a precision current source is needed. The only way to suppress the AC ripple is to use an external filter. The compliance voltage of this product extends from ground to 2V (maximum) below the positive supply.

The XTR300 [5], another product from Texas Instruments, is a complete output driver for industrial and process control applications. The maximum DC accuracy of the output current that can be obtained from this product is 0.12% over a small current range from 0.24mA-2.4mA. It uses a high-precision opamp, an instrumentation amplifier and

an accurate resistor to achieve this DC accuracy. But the compliance voltage is slightly lower, ranging from ground to 3V below.

The AD5412 [1] is a 12 bit current steering DAC designed to meet the requirements of industrial process control applications from Analog Devices. The maximum DC accuracy of the output current reported for this product is ±0.13% for a wide output current range from 0-20mA and the compliance voltage extends from ground to 2.5V below the positive supply.

The MAX15500 [3] is an industrial current/voltage output conditioners from Maxim. It has a wide output current range from 0-24mA, with a maximum DC accuracy of ±0.5% at the full scale current output. The quiescent current reported for this product is 7mA, higher than that of other products. Table 1.1 lists some state-of-the-art specifications of precision voltage-to-current converters.

TABLE 1.1: Current state-of-art for precision voltage-to-current converters

Parameters	XTR111 [4]	XTR300 [5]	AD5412 [1]	MAX15500 [3]
Output current range (mA)	0-25	0.24-2.4	0-24	0-24
Max DC accuracy at FS output current (%)	0.1	0.12	±0.13	±0.5
Output Ripple at FS output current (%)	0.8	-	-	-
Compliance voltage from positive supply (V)	2	3	2.5	-
Supply range (V)	7-44	5-20	10.8-40	15-32.5
Temperature range	-40°C-85°C	-40°C-85°C	-40°C-85°C	-40°C-85°C
Large signal rise time (μs)	10@500Ω	-	40@350Ω	600@750Ω
Quiescent current (mA)	0.55	2.3	4	7

Until now, using thin film resistors and a low-offset amplifier [7] is the most common method of realizing a current mirror with high DC precision, see figure 1.2. A low-offset amplifier (A) ensures equal drain-source voltage across M1 and M2, which is very important for the getting a high DC accuracy. This has three main disadvantages which are as follows:

1) It requires a costly IC technology with precision matched resistors (R1 and R2).

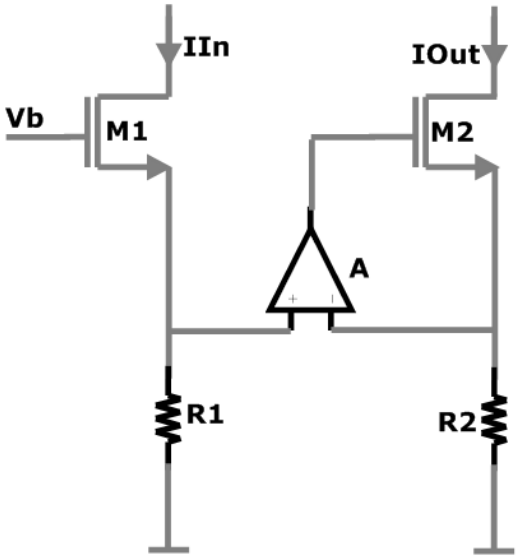


FIGURE 1.2: Current mirror using precision resistor and amplifier

2) It requires a low-offset amplifier, which means more chip area, hence more production cost.

3) The amplifier (A) adds significant noise to the current mirror's output.

4) A resistor-based current mirror requires more voltage headroom, which reduces the output voltage swing.

The other way of getting high DC accuracy is to use DEM [25]. DEM is a technique, which involves interchanging the unit elements (used to construct the circuit) periodically, so that the relative mismatches among them are averaged out over one time period. Chopping is a special case of DEM when it is applied on 2 devices only. For instance a 1:1 current mirror can be chopped for getting a good DC accuracy [10], which has its own limitations. The main disadvantage is a chopping ripple which is not desirable in many applications, for example, when a current mirror is used as a current reference.

This thesis is about the design of a high precision current mirror in modern CMOS technology that eliminates the drawbacks mentioned above while achieving state-of-the-art DC precision over a wide range of an output current.

1.2 Accuracy of Current Mirror

The accuracy of a current mirror is governed by the matching of the devices which are used for its construction. The higher the matching, the better the accuracy of the output current produced. It is very important to investigate the merits and demerits of both MOS and Bipolar current mirror before proceeding further.

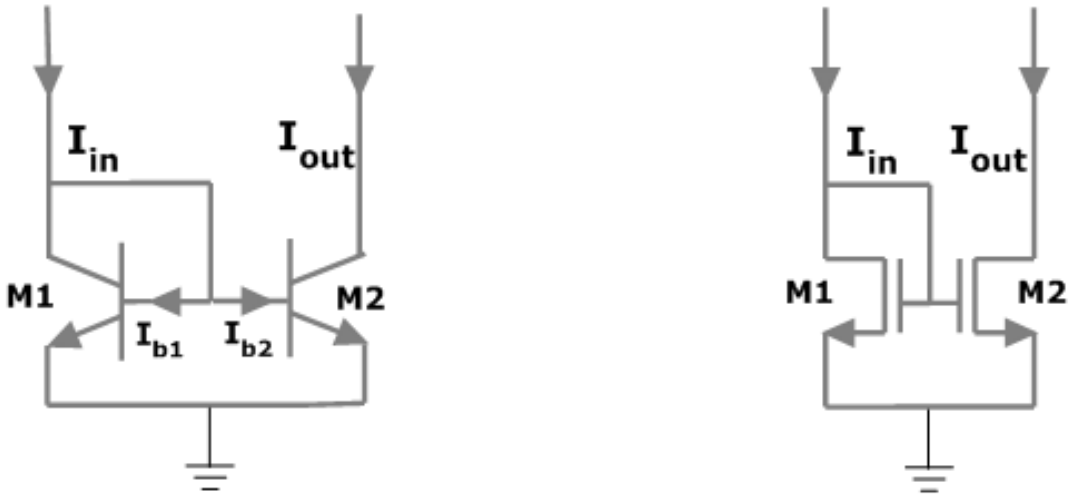


FIGURE 1.3: a) BJT current mirror b) MOSFET current mirror

Figure 1.3 shows the basic implementation of current mirror using a) BJTs and b) MOSFETS. Due to the finite base current of a BJT, the input current will not be equal to the output current in the BJT configuration, even in the case of perfectly matched devices. Since the gate current of a MOSFET is negligible, the MOSFET configuration does not have this drawback. This means a better DC accuracy can be gained using MOSFET current mirror instead of BJT mirror shown in figure 1.3.

The current transfer function for a BJT mirror (neglecting the early effect and mismatch between the mirror pair) is:

$$I_{out} = \frac{I_{in}}{1 + 2/\beta_F} \tag{1.1}$$

where β_F is the current gain of the transistor. Factor β_F in the denominator is nothing but the gain error which can vary significantly over process/corners. To remove the dependency of the output current on β_F, the current gain of the device should be much higher than 10^5.

Current transfer function for a MOSFET mirror (assuming perfect matching between the mirror pair and neglecting channel length modulation) is:

$$I_{out} = I_{in} \tag{1.2}$$

Compared to MOSFETs, BJTs have superior performance when it comes to matching and $1/f$ noise [16]. Therefore, if input referred noise or offset is one of the critical parameter for an application then it is always advisable to use BJT. Opamps in which MOSFET input pairs are used, usually show 10 to 100 times worse performance compared to BJT when low frequency noise and offset is calculated. However, MOSFET have their own advantages over BJT like processing cost, very low leakage current (current flowing into the gate of MOS device is negligible).

However, the perfect matching of transistors only exists in the world of fantasy. Real world transistors have mismatch which limits the performance of high precision circuits. The major errors due to mismatch between the devices are the gain error, offset and non-linearity. It is instructive to investigate various sources of mismatch and its effect on the performance of a current mirror.

1.3 Mismatch Sources

Mismatch sources in transistors can be divided into two categories a) Deterministic and b) Random. Mismatch due to threshold voltage (V_T) and transconductance coefficient (β) comes under random mismatch while mismatch due to drain-source voltage variations comes under deterministic mismatch. This can be eliminated by careful design.

1.3.1 V_T mismatch

V_T is known as the threshold voltage of a MOS transistor. Neglecting the body effect, the threshold voltage for PMOS transistor can be defined as [18]:

$$V_{TP} = (-|Q_{SD}(max)| - Q_{SS})(\frac{t_{ox}}{\epsilon_{ox}}) + \phi_{ms} - 2\phi_{fn} \tag{1.3}$$

where, $|Q_{SD}(max)|$ is the maximum space charge density per unit area in inversion layer. Q_{SS} is the trapped charge density per unit area. ϕ_{ms} is the metal-semiconductor work function and ϕ_{fn} is the potential difference between intrinsic fermi level and fermi level in an n-type substrate. The maximum space charge density per unit area in inversion

layer can be expressed as [18]:

$$|Q_{SD}(max)| = \sqrt{4\epsilon_s e N_d V_T ln\frac{N_d}{n_i}} \tag{1.4}$$

where N_d is the doping concentration of the substrate, n_i is the intrinsic electron concentration that depends on temperature and ϵ_s and e are constants. Substituting (1.4) in (1.3) we get,

$$V_{TP} = (-\sqrt{4\epsilon_s e N_d V_T ln\frac{N_d}{n_i}} - Q_{SS})(\frac{t_{ox}}{\epsilon_{ox}}) + \phi_{ms} - 2\phi_{fn} \tag{1.5}$$

From the equation (1.5) it can be seen that the V_T of a transistor depends on doping (N_d) concentration. Since N_d is non-uniform over the die, we cannot predict the exact value of threshold voltage. It can also be seen that threshold voltage also depends on intrinsic electron concentration (n_i), which is temperature dependent. V_T is inversely proportional to the rise in the temperature [24].

It can concluded that the threshold voltage of MOS transistors have a strong dependency on technology and temperature.

If the relative distance between the matched transistors on the chip is neglected, the variation in the threshold voltage (V_T) of the MOS transistor is modeled by [15]

$$\sigma_{V_T} = \frac{A_{VT}}{\sqrt{WL}} \tag{1.6}$$

where A_{VT} is a process dependent parameter and σ is the standard deviation. For example, if A_{VT} is equal to 10mVμm and W*L is equal to 100μm^2 then σ_{V_T} is equal to 1mV.

If the body effect is included then the threshold voltage of PMOS transistor is defined as [18]:

$$V_T = V_{TP} + \frac{\sqrt{2q\epsilon_s N_d}}{C_{ox}}(\sqrt{|2\phi_{fn} + V_{BS}|} - \sqrt{|2\phi_{fn}|}) \tag{1.7}$$

where, V_{BS} is the bulk to source potential. If bulk and source are shorted together (which is generally the case in most of the design) then

$$V_T = V_{TP} \tag{1.8}$$

However, two transistors on same die cannot match perfectly because of several reasons. One of them is a temperature drift on-chip, which cause some mismatch between the

devices. To minimize the effect of mismatch on circuit performance, it is very important to layout the analog circuit carefully.

1.3.2 Beta mismatch

β is the transconductance coefficient which is defined as:

$$\beta = \mu C_{ox}(\frac{W}{L}) \tag{1.9}$$

where μ is the carrier mobility, C_{ox} is the oxide capacitance and $\frac{W}{L}$ is the aspect ratio. Any mismatch in these parameters will change the transconductance coefficient. For example, 1% mismatch in μ and 1% mismatch in C_{ox} can be converted to 2% mismatch in $\frac{W}{L}$.

μ can be expressed as [18]:

$$\mu = \frac{e\tau}{m} \tag{1.10}$$

where m is the effective mass of the charge carriers, τ is the mean time of collision between the particles and e is the electronic charge constant.

There are generally two types of scattering in semiconductors: a) Lattice and b) Ionized impurity. Both are temperature dependent and show positive and negative temperature coefficients respectively [18]. The ionized impurity scattering depends on impurity concentration, which makes the charge mobility impurity concentration dependent. The doping concentration is not uniform over a die and can vary by 30% or even more. Therefore two devices on the same die have different charge mobility (μ), which can give rise to mismatch between them.

C_{ox} is the oxide capacitance and can be expressed as follows [18]:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{1.11}$$

where, ϵ_{ox} is the dielectric constant of the oxide and t_{ox} is the oxide thickness. Any variation in the oxide thickness will change the capacitance per unit area [13, 14]. The IC technology used for the design has typical gate oxide thickness of 138Å. Due to process variations, the minimum and maximum values are 132Å and 144Å respectively, indicating 4.35% variation in the thickness of gate oxide. Mismatch in the thickness can be minimized by placing the devices closer and making a common centroid layout [13, 14]. In addition, oxide thickness also causes a variation in V_T which is a second order effect and will not be discussed.

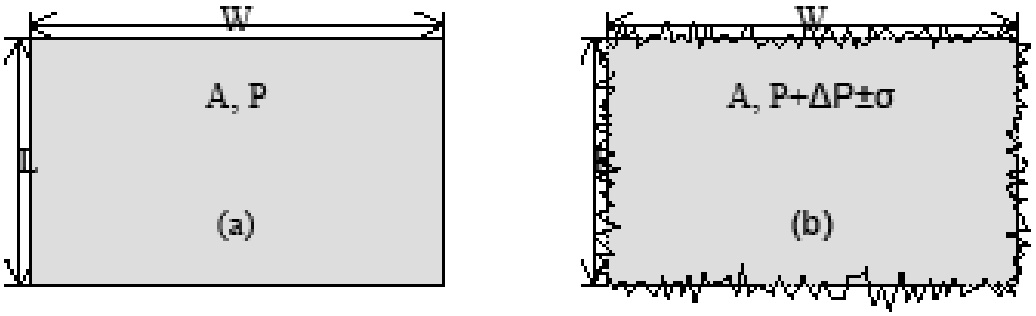


FIGURE 1.4: a) Without LER b) With LER

Intra-die random fluctuations inherent to fabrication process introduces Gate Line Edge Roughness (LER) [17] while defining the gate dimension of the devices. Figure 1.4 shows the effect on the edges without LER and with LER. The roughness in the gate edges adds mismatch, which cannot be eliminated. LER also introduces mismatch in threshold voltage (V_T) and gate oxide capacitance (C_{ox}) [20, 27].

1.3.3 V_{ds} mismatch

Drain-source voltage mismatch can cause error in the mirror output, independent of all other parameters. Therefore it is very important to take care that the drain-source voltage of the matched pair is kept equal. The effect of V_{ds} mismatch is visible generally due to finite output impedance. An ideal current amplifier has zero input and infinite output impedance. In reality neither of them is possible.

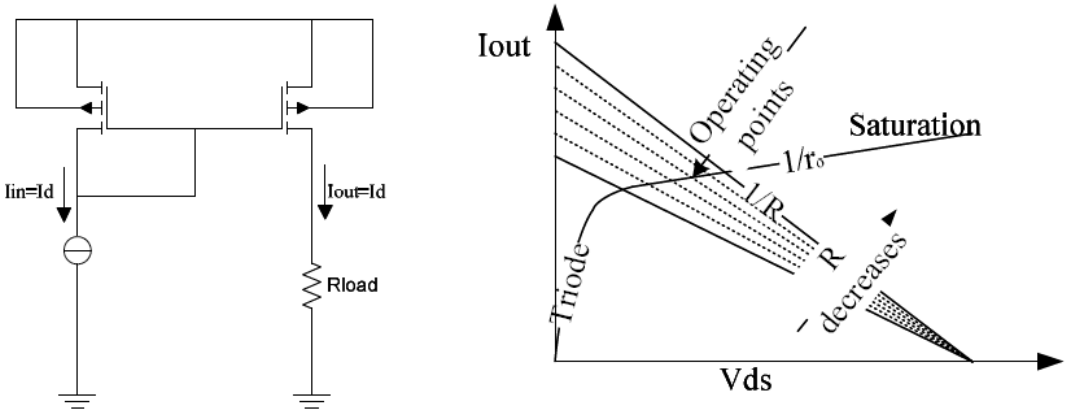


FIGURE 1.5: a) PMOS current mirror with load b) Output characteristic

Figure 1.5 shows a current mirror with load resistance and its output characteristics. The current mirror is working in saturation region where it behaves like a current source with finite output impedance. It can be seen from figure 1.5(b), as the load resistance changes, the operating point shifts, which in turn changes the output current because the current mirror has finite output impedance. The change in the output current is due to channel length modulation in the MOS devices, which can be avoided by cascoding and gain boosting [6, 19].

1.3.4 Effect of mismatch sources in current mirror

The errors in the current mirror output are due to three different mismatch sources as described above. Among them, the error due to V_T and β mismatch is different from that of V_{DS} mismatch. The former ones are introduced by technology. They are random errors while the latter is the deterministic error.

Let us consider 1:1 current mirror as shown in figure 1.3(b). The aspect ratio of M1 and M2 is same. The maximum absolute error in the output current from the mirror due to V_T, β and V_{DS} mismatch is given in [24]. In strong inversion region:

$$\frac{\Delta I_{out}}{I_{out}} = \sqrt{\left(\frac{\sigma_\beta}{\beta}\right)^2 + \frac{4\sigma_{V_T}^2}{(V_{GS}-V_T)^2}} + \left|\frac{\lambda}{1+\lambda V_{DS}}\Delta V_{DS}\right| \tag{1.12}$$

In the weak inversion:

$$\frac{\Delta I_{out}}{I_{out}} = \sqrt{\left(\frac{\sigma_\beta}{\beta}\right)^2 + \left(\frac{\sigma_{V_T}}{nU_T}\right)^2} + \left|\frac{exp\left(\frac{-V_{DS}}{U_T}\right)}{1-exp\left(\frac{-V_{DS}}{U_T}\right)}\frac{\Delta V_{DS}}{U_T}\right| \tag{1.13}$$

In both strong and weak inversion σ_β and σ_{V_T} can be expressed as [11, 15]

$$\frac{\sigma_\beta^2}{\beta^2} = \frac{A_\beta^2}{WL} \tag{1.14}$$

$$\sigma_{V_T}^2 = \frac{A_{V_T}^2}{WL} \tag{1.15}$$

Above two are very simple mismatch model of a MOSFET in strong and weak inversion region. This simplified analysis is accurate enough for our design. For more accurate modeling of the MOSFET readers can refer to [11, 15] for more details. Though the expression of a sigma variation is same in both strong and weak inversion but their values are different. In weak inversion, the coefficients, A_β and A_{V_T}, are larger than those in strong inversion. For same size transistors, a better matching can be obtained in strong inversion compared to weak inversion region.

Error due to mismatch in V_{DS} can be minimized by careful design, hence it will not be considered in the following example. Suppose if the matching coefficients of the PMOS transistor having aspect ratio ($600\mu m/2\mu m$) are: $A_\beta = 2\%\mu m$ and $A_{V_T} = 10mV\mu m$ then $\frac{\sigma_\beta}{\beta} = 0.058\%$ and $\sigma_{V_T} = 0.29mV$.

If the transistor works in strong inversion and overdrive voltage is 200mV then:

$$\frac{\Delta I_{out}}{I_{out}} = \sqrt{\left(\frac{\sigma_\beta}{\beta}\right)^2 + \frac{4\sigma_{V_T}^2}{(V_{GS} - V_T)^2}} = 0.3\% \tag{1.16}$$

If the transistor works in weak inversion and $nU_T = 50mV$ then:

$$\frac{\Delta I_{out}}{I_{out}} = \sqrt{\left(\frac{\sigma_\beta}{\beta}\right)^2 + \left(\frac{\sigma_{V_T}}{nU_T}\right)^2} = 0.58\% \tag{1.17}$$

From the above analysis it can be concluded that error in weak inversion is greater than the error in strong inversion. Hence current mirror transistors should be biased in strong inversion for getting a good DC performance.

1.4 Target application - XTR111

The XTR111 is a precision voltage-to-current converter, designed for standard 0mA-20mA or 4mA-20mA analog signals, which can source up to 36mA [4]. Figure 1.6 shows the system level diagram of XTR111. The ratio between the input voltage and the output current is set by the external resistor R_{SET}. An external PMOS transistor (Q_1) is a high power device, which ensures high output impedance and low compliance voltage for the mirror (maximum 2V below the VSP). The adjustable 3V to 15V sub-regulator output provides the supply voltage for additional circuitry. Transistor (Q_2) acts as a clamp for the external current limit. I-Mirror is a 1:10 dynamic element matched (DEM) current mirror, which ensures high DC accuracy (maximum 0.1% DC error with respect to full scale current level of 25mA) at the cost of significant ripple at the output (0.8% with respect to full current level of 25mA). The DEM'ing frequency for this product is 100kHz. Figure 1.7 shows the DEM'ing ripple which is taken from the datasheet [4]. It is the actual measurement on silicon. The XTR111 is used in many applications, for example, as a universal voltage controlled current source, a current or a voltage output for 3 wire sensor system, PLC output programmable driver, current mode sensor extraction, etc.

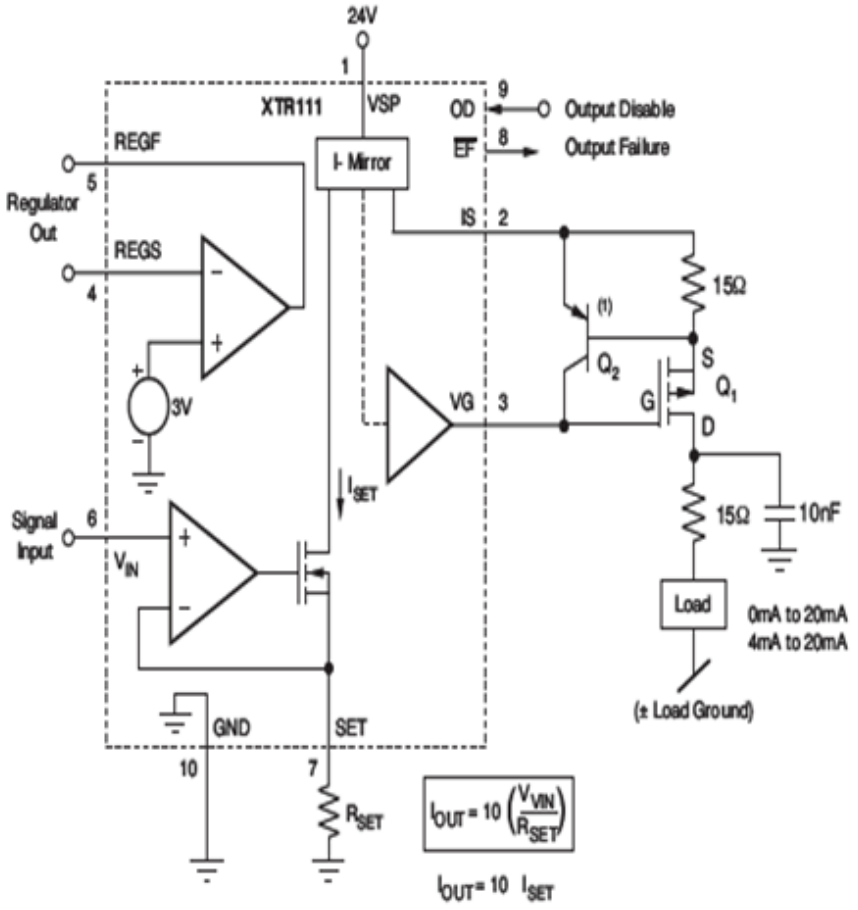


FIGURE 1.6: Precision Voltage-to-Current converter - XTR111

The speed at which DEM is done and the output ripple is a concern for this product. Another problem with this product is that there is no in-built circuit protection on chip which can limit the output current when no load is connected. For this an external transistor clamp Q_2 is required. My target is to design a new circuit, which can overcome the problem of output ripple without sacrificing the DC accuracy. Also an on-chip solution will be designed for output current limit.

1.5 Goals

The specifications for this project were decided by keeping state-of-the-art in mind. The aim is to make a new version of XTR111, which can replace the existing one. The specifications that are aimed for this project are as follows:

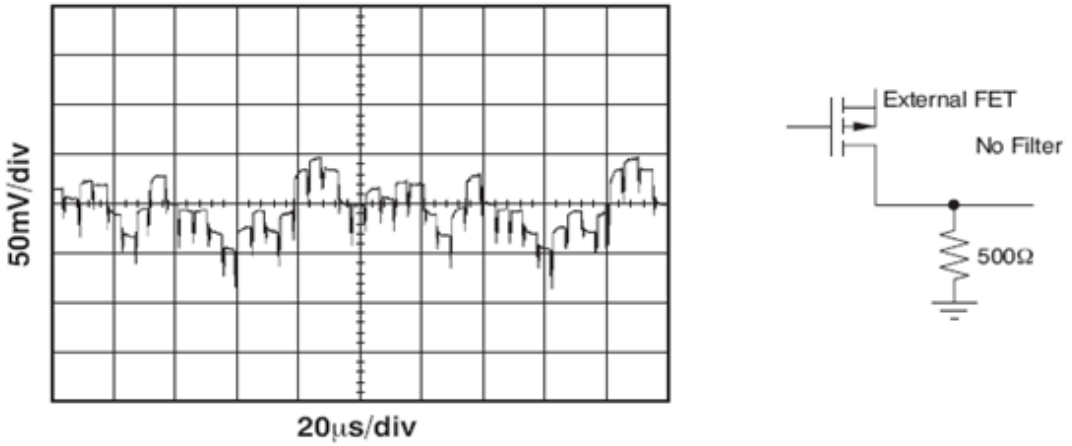


FIGURE 1.7: DEM'ing ripple from XTR111

1) Wide input current range from 10μA to 2.5mA
2) Output current range from 100μA to 25mA (Gain 10X)
3) DEM'ing frequency (speed) = 250kHz
4) DC accuracy < 0.1%full scale current level of 25mA
5) Maximum output ripple < 4uA for full scale current level of 25mA
6) Compliance voltage to positive rail < 2V
7) Wide supply range = 11V to 40V
8) On-chip protection for external current limits
9) Single supply voltage

1.6 Organization of thesis

This thesis will focus on the design of a high-precision current mirror with high DC and AC accuracy. Current mirrors, mismatch sources and its effect on the mirror's performance are investigated in this chapter.

Chapter 2 will outline a brief introduction about the work, which was done in past to make an accurate current mirror. In the starting of the chapter, non-idealities of switches will be discussed followed by three well-known techniques for making an accurate mirror a) Dynamic element matching (DEM), b) Sampling and c) Trimming. Finally, the way to reduce the DEM ripple in voltage domain will be discussed.

Chapter 3 will present a new technique of designing a high precision current mirror.

Later the system-level design will be discussed followed by circuit implementation and layout details.

Chapter 4 will present the detailed simulation results. Later the measurement results will be presented and finally the chip photo will be shown.

Chapter 5 will conclude the thesis by telling about the goals which are achieved. To improve the design further, some future possibilities will be given.

Chapter 2

Literature Review

2.1 Introduction

In this chapter, some of the previous work done in the past will be presented. In section 2.2, an analysis on switches is presented owing to their frequent use in analog circuits. The section will outline important aspects about switches describing various tradeoffs. In section 2.3 and 2.4 sampling and modulations techniques will be discussed, which will be used in the design of a high-precision current mirror. In section 2.5 trimming technique is discussed. Finally, a way to reduce the DEM ripple will be described.

2.2 Switches

The techniques for making high precision current mirrors, presented later in the chapter, incorporate switches that make use of CMOS transistors. Therefore, it is very important to investigate the various properties of CMOS switches.

An ideal switch has a zero ON resistance, infinite OFF resistance and zero delay from input to output. In reality, a CMOS switch has a finite resistance when the switch is OFF (open) and non-zero resistance when the switch is ON (closed). These non-ideal effects should be taken care by proper selection and design. The OFF resistance of the minimum size CMOS switches can vary from 500MΩ to few GΩ, while the ON resistance can be as high as 10kΩ. The finite ON resistance of the switch, cause a voltage drop across it when the current is passed. ON resistance of the switch plays an important role in analog design, one of the design parameters, which should be designed carefully.

There will be some delay in the signal path, which should be taken into consideration. It will take some time for the switch to perform its action when the gate voltage is applied because there will be some delay in the formation of the inversion layer under the gate (responsible for conduction). However, the main problem for the dynamic analog circuit is charge injection from these MOS switches and noise contribution due to finite ON resistance. These things are discussed next.

2.2.1 Charge Injection and feedthrough from MOSFETS used as Switch

Charge injection from MOS switches is a critical problem in analog design. In most switched circuits, charge injection is the limiting factor. Figure 2.1 shows the charge injection model of a basic MOS switch [26]. When the gate potential is greater than

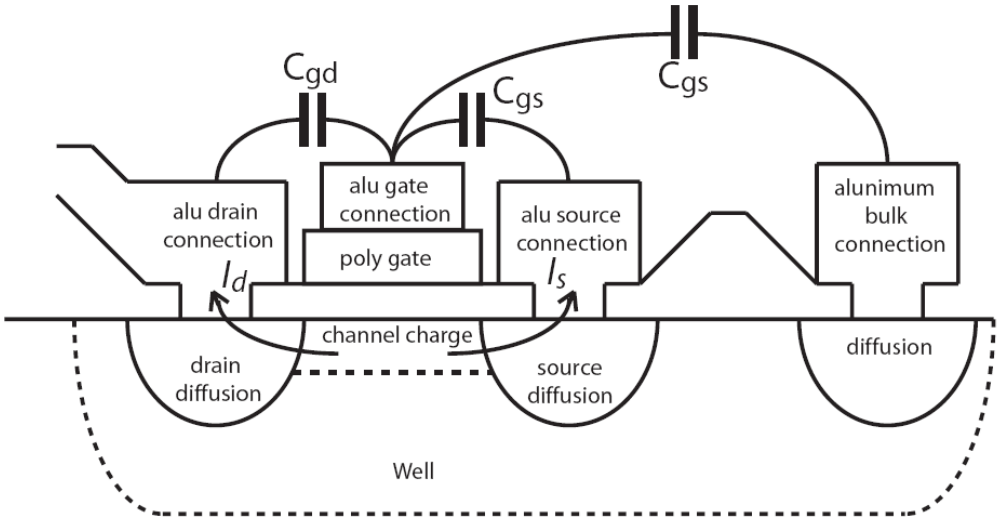


FIGURE 2.1: Charge injection model

the threshold voltage of the transistor, an inversion layer is formed underneath the gate, which is responsible for the conduction. This inversion layer extends from source to drain. The charge contained in this layer is expressed as [19]:

$$Q_{ch} = WLC_{ox}(V_{GS} - V_T) \tag{2.1}$$

where, L denotes the effective channel length, W is the width and C_{ox} is the oxide capacitance. V_{GS} is the gate voltage applied to the transistor with respect to source and V_T denotes the threshold voltage.

When the switch turns OFF, or in other words, when the gate potential is too low to create an inversion layer, the channel charge Q_{ch} splits between drain and source terminals according to the ratio of their relative impedance. This phenomenon is known as 'Charge Injection'. For a minimum size switch in 0.7μm process, having W=1μm, L=0.7μm, V_T=0.7V, V_{GS}=5.5V and C_{ox}=2fF/μm^2 the channel charge equals Q_{ch}=6.72fC [26]. This charge can cause a voltage step of 6.72mV over a 1pF capacitor. Such an excess voltage across the sampling capacitor on top of the signal voltage is a major problem in sample and hold circuits. This can limit the accuracy of the circuit.

Referring to figure 2.1, C_{gd} is the gate to drain capacitance, C_{gs} is the gate to source capacitance and C_{gb} is the gate to bulk capacitance. These parasitic capacitances are another source of error when a MOSFET is used as a switch. When the switch turns ON and OFF, it not only changes the state of gate but it also changes the state of the drain, source and bulk of the transistor. Among these, the disturbance caused in bulk is negligible [19]. For a small change in gate-source voltage of a transistor δV_{GS}, charge injection due to gate-source capacitance can be expressed as:

$$Q_{GS-inj} = \delta V_{GS} C_{gs} \tag{2.2}$$

From the above equation it can be concluded that the charge injection due to gate-source capacitance has a linear dependency on the change in gate-source voltage. This means that the changes in the gate-source voltage will have an effect on residual offset. DC accuracy is limited by this residual offset. Charge injection is also a problem for getting good PSRR and CMRR [19]. Standard ways to reduce the charge injection will be described in the following paragraph.

The most common method to reduce charge injection is to add a dummy switch or use a complementary switch instead of one switch. Figure 2.2 shows charge injection cancellation by adding a) dummy switch and b) PMOS and NMOS transistors in parallel [19, 26]. It can be seen from figure 2.2(a) that MOSFET M_1 is the main switch and MOSFET M_2 acts as a dummy switch with half (W/L) as compared to M_1. Both of the switches are governed by complementary clock signals as shown in the figure 2.2. The idea behind this technique is that, when M_1 switches OFF, half of the charge will go towards V_{in} and other half will go towards C_H and V_{out}. MOSFET M_2, which is half the size of M_1, is driven by an opposite clock signal and will restrict the amount of charge going inside the capacitor C_H. Ideally, there will be no charge injection on C_H. However, in reality this is not true because it is difficult to get a perfect matching of the switches in layout. The assumption of equal splitting of charge between drain and source is also not true because it will depend of the source and drain impedance.

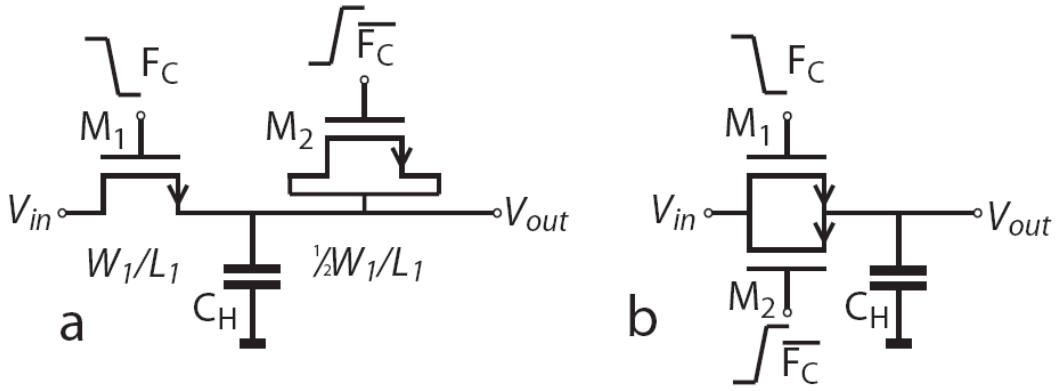


FIGURE 2.2: Charge injection cancellation by adding a) Dummy switch b) PMOS and NMOS in parallel

Another technique is to place a PMOS and NMOS transistor in parallel. These are then driven by opposite clock signals as shown in figure 2.2(b). The idea behind this technique is that, when M_1 closes, transistor M_2 also closes at the same time. The charge injection from PMOS switch will consist of holes while that of NMOS will consist of electrons, which will compensate each other. The charge balance equation for both the switches can be written as follows:

$$WLC_{ox}(V_{F_C} - V_{in} - V_{T,n}) = WLC_{ox}(V_{in} - 0 + V_{T,p}) \tag{2.3}$$

From the above equation the optimum value of V_{in} can be calculated, which is

$$V_{in,opt} = \frac{(V_{F_C} - V_{T,n} - V_{T,p})}{2} \tag{2.4}$$

In practice this is not possible because it is very difficult to match the layout of both transistors. Moreover, the threshold voltage of the NMOS and PMOS depends on the mobility coefficients, which cannot be controlled as they depend on technology and temperature [19].

Another way to reduce charge injection is to make use of a differential circuit configuration. Figure 2.3 shows the circuit diagram where switches are connected in a differential configuration [19, 26]. From figure 2.3 it can be seen that if q_{inj1} is equal to q_{inj2}, there will be no differential charge left on capacitor C_H. But there will be some left over differential charge, when a differential input voltage is applied because of the

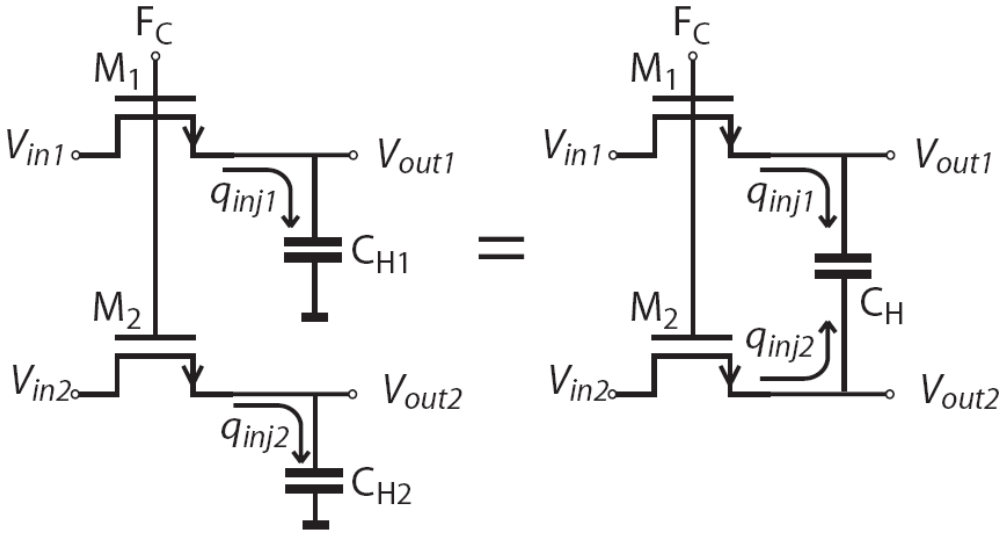


FIGURE 2.3: Differential configuration

different V_{GS} of M_1 and M_2.

$$\delta q_{inj,V_{in}} = q_{inj1} - q_{inj2} = WLC_{ox}(V_{in2} - V_{in1}) \tag{2.5}$$

Moreover, the mismatch between M_1 and M_2 will also contribute to the charge injection. This is often the dominant source of error. From the whole analysis it can be concluded that, the charge injection can be minimized by careful layout and design, but it cannot be eliminated completely.

2.2.2 Noise

Generally, a MOSFET used as a switch will contribute two types of noise: thermal noise and sampling noise. Thermal noise is generated because of finite ON resistance of the switch. When the switch is used to build sample and hold circuits, it contributes to sampling noise, which is stored on the sampling capacitor.

The ON resistance of the switch is given by [19]:

$$R_{ON} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)} \tag{2.6}$$

and the thermal noise contributed by resistance of value RΩ at temperature T is [19]:

$$V_{noise,R} = \sqrt{4kTR} \tag{2.7}$$

where, k is the Boltzmann constant, R is the value of resistance in ohms, T is the temperature in Kelvin and $V_{noise,R}$ is the thermal noise voltage.
The rms voltage generated by the switch in a sample and hold circuit is given by [19]

$$V_{samplingNoise} = \sqrt{\frac{kT}{C}} \tag{2.8}$$

where, k is the Boltzmann constant, T is the temperature in Kelvin, C is the value of sampling capacitor in Farad and $V_{samplingNoise}$ is the rms noise voltage. Sampling noise voltage limits the performance of many high precision circuits. This can be reduced by increasing the value of sampling capacitor C, which in turn loads the subsequent stage and reduce the speed of the system. There is always a tradeoff between speed and accuracy of the system when using sampled signals in analog circuit design.

2.3 Sampling Technique: The Current Copier

It is possible to design high precision circuits by using sampling techniques. The most commonly used sampling technique is called auto-zeroing [10]. Sampling can also be used to design a current mirror having a good DC accuracy. One such circuit is a current copier [25], whose working principle will be described in the next sub-section. The circuit use sample and hold [8, 23, 25] scheme, which was invented two decades back.

2.3.1 Working Principle

Figure 2.4 shows the basic implementation of current copier circuit. Transistor M is the main device, C is the sampling capacitor, S_1 and S_2 are sampling switches and I_{in} is the input current, which is supposed to be copied. R is the load resistance. In the practical circuits, switches S_1 and S_2 will be implemented using MOSFET operating in deep triode region. The current copier circuit works in two phases. In the 1^{st} phase, switch S_1 is ON and switch S_2 is OFF. In this phase, transistor M is diode connected to the input current source I_{in}. The gate-source voltage V_{GS} is stored on the capacitor C corresponding the input current I_{in}. In the 2^{nd} phase, switch S_1 is OFF and switch S_2 is ON. The gate-source voltage stored on the capacitor in previous step will produce the output current. This current will be equal to the input current (as in the first phase), if the channel length modulation (of M), sampling noise ($\frac{kT}{C}$) and charge injection from the switches are neglected. The voltage stored on the capacitor with transistor M acts as a current source.

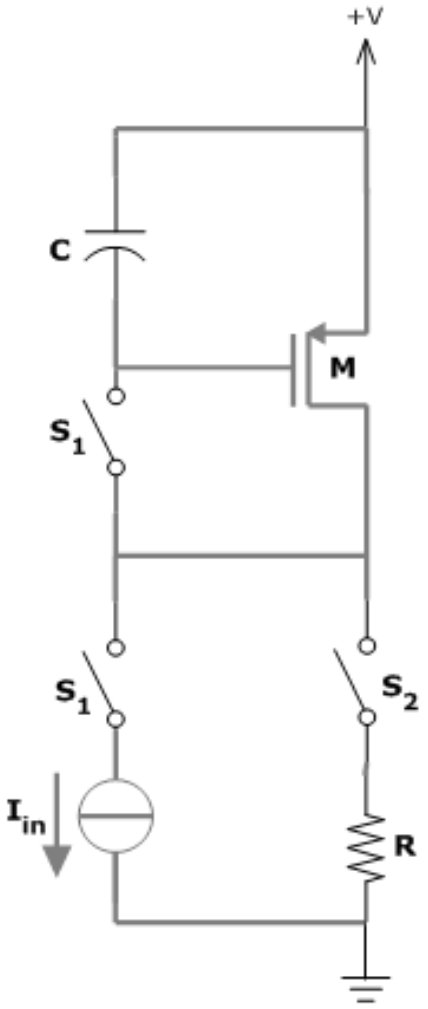


FIGURE 2.4: Current Copier Circuit

In time domain, the input and output current relationship is governed as follows:

$$I_{out}(n) = I_{in}(n - \frac{1}{2}) \tag{2.9}$$

The above equation tells that there will be a delay of half clock cycle between the output and the input signal; hence this circuit cannot be used continuously in time domain.

2.3.2 Advantages and Limitations

This technique can achieve high DC accuracy ($\pm 0.1\%$) but has limitations, which makes it difficult to use in high-precision analog circuit design. These are as follows:

1) The architecture with single current copier cannot work continuously in time domain. To make it work continuously, at least 2 current copiers are required. When first current copier will be in the sampling phase, second will be used to produce an output current and vice versa.

2) There is always a tradeoff between speed, accuracy and chip area.

3) This architecture is not suitable for making a current mirror with large gain. A mirror with gain of 10 requires 11 devices with 11 sampling capacitors. If the sampling capacitors are too big (for reducing $\frac{kT}{C}$ noise) then this architecture will not be feasible as it will consume large chip area. Moreover, the circuit will take more time to settle because 10 devices need to be settled before it can amplify the input signal correctly.

4) Since switches are used in this architecture, the charge injection and clock feedthrough are always a problem. Due to the charge injection from switch, the voltage stored on the sampling capacitor will be disturbed; hence the output current will be an inaccurate copy of the input current. The best ways to reduce the effects of charge injection are described in section 2.2.1.

5) Sampling action adds additional KT/C noise. This noise is sampled on the capacitor with the signal and charge injection error from MOS switch. To reduce the sampling noise, size of capacitor should be increased, which is again a tradeoff between area consumption and accuracy.

It can be concluded that, the voltage stored on the sampling capacitor will consists of 3 parts a) Charge due to the signal current, b) Charge injection error voltage from MOS switch and c) $\sqrt{KT/C}$ noise voltage. To get a high DC accuracy the size of sampling capacitor should be really big to suppress $\frac{kT}{C}$ noise. For example, input current range means a certain small range in V_{GS} which needs to be sampled very accurately. If V_{GS} range is 200mV and minimum DC error is 0.1% of full scale value, then error voltage should be equal to 0.1% of 200mV, which is equal to 200μV. Thus a sampling capacitor of at least 103.5fF is needed to achieve this noise specification (provided charge injection from the switch is neglected). In reality charge injection from the sampling switch is the dominant. To bring down the noise to 200μV, the size of the sampling capacitor should be increased, which further increases the chip area.

2.4 Modulation Technique: Dynamic Element Matching

Dynamic element matching is another technique to make a high accuracy current mirror. This technique was invented two decades ago [9]. It is a very powerful way to achieve very high DC accuracy. DEM technique can be extended to N number of devices. If the DEM operation is carried out only on 2 devices then it is known as chopping [10]. Chopping is used in many industrial opamps to reduce the input referred offset. To simply the whole analysis, DEM operation (or chopping for this particular case) on only 2 devices will be discussed next.

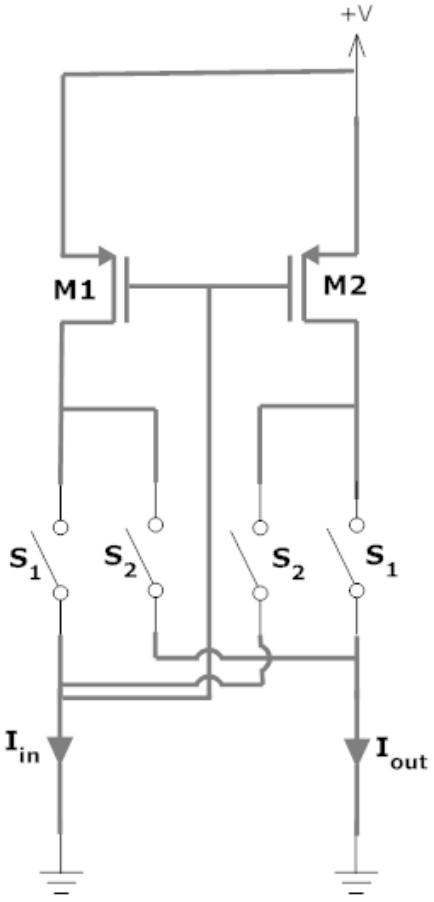


FIGURE 2.5: Dynamic Element Matching

2.4.1 Working Principle

The figure 2.5 shows the basic implementation of this technique (assuming DEM is carried out on only 2 devices M_1 and M_2). It consists of 6 MOS devices. M_1, M_2 are the main device and S_1, S_2 are the MOS switches. The circuit works in two phases. In

phase1, switches S_1 are ON and switches S_2 are OFF. This means device M_1 acts as input and device M_2 as output. In phase2, switches S_1 are OFF and switches S_2 are ON. In this phase, device M_1 acts as output and device M_2 as input.

In the phase1, the current input to device M_1 is I_{in}. In reality, there is a mismatch between these two devices. The mismatch value will be governed by equation (1.14). Due to the mismatch between these two devices, the output current will be different than input current. If the mismatch current is denoted by δI then the output current flowing from the device M_2 will be equal to

$$I_{out} = I_{in} + \delta I \tag{2.10}$$

In the phase2, the input current I_{in} is now flowing through the device M_2. Due to mismatch between M_1 and M_2 the output current will be different from the input. Since the mismatch between the two devices is the same as in phase1, the output current is given by

$$I_{out} = I_{in} - \delta I \tag{2.11}$$

From the equations (2.10) and (2.11), it can be concluded that the current error due to mismatch can be removed by simply adding the two equations. Adding both the equations together we get,

$$I_{out} = I_{in} \tag{2.12}$$

Dynamic element matching is a modulation technique which modulates the mismatch and gives rise to a high frequency ripple at its modulating frequency. The magnitude of a high frequency ripple is directly proportional to the relative mismatch between the mirror devices. The mismatch among the mirror devices can be reduced either by trimming or using degeneration resistors [19]. Figure 2.6 clearly shows the modulation effect by giving rise to a small AC signal at the top of DC, which is undesirable in many high precision applications. In phase 1, when the switch S_1 is ON the current output is $I_{out} = I_{in} + \delta$ I while in phase 2, when the switch S_2 is ON the current output is $I_{out} = I_{in}$ - δ I.

Quantitatively, the DC output current will be given by

$$I_{DC,out} = \frac{1}{T}\int_0^T I_{out}(t)dt \tag{2.13}$$

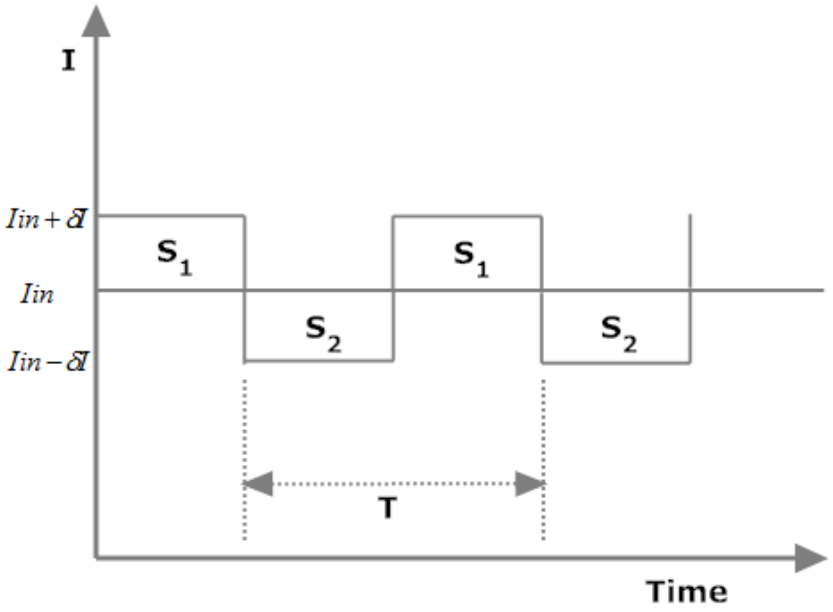


FIGURE 2.6: DEM (or chopping) ripple in AC mode

$$I_{DC,out} = \frac{1}{T}\left(\int_{0}^{T/2} (I_{in} - \delta I)dt \int_{T/2}^{T} (I_{in} + \delta I)dt\right) \tag{2.14}$$

$$I_{DC,out} = I_{in} \tag{2.15}$$

Equation (2.15) clearly shows that AC ripple is averaged out over one time period and high DC accuracy is achieved. The amplitude of the high frequency components in frequency domain is given by [24]

$$a_k = \frac{\delta I}{k\pi}[1 - (-1)^k] \tag{2.16}$$

where, a_k is the amplitude of the ripple at k^{th} frequency.

Depending on the value of k we can calculate the amplitude of the ripple. If the k is even then,

$$a_k = 0 \tag{2.17}$$

and if k is odd then,

$$a_k = \frac{\delta I}{k\pi} \tag{2.18}$$

Equations (2.17) and (2.18) clearly shows that, even harmonics are cancelled and only odd harmonics are left over. Figure 2.7 shows the frequency spectrum of the DEM current mirror assuming there is a mismatch of 1% with respect to DC output current

of 25mA (δ I = 250μA).

This technique can be extended for current mirrors having a gain larger than 1. For

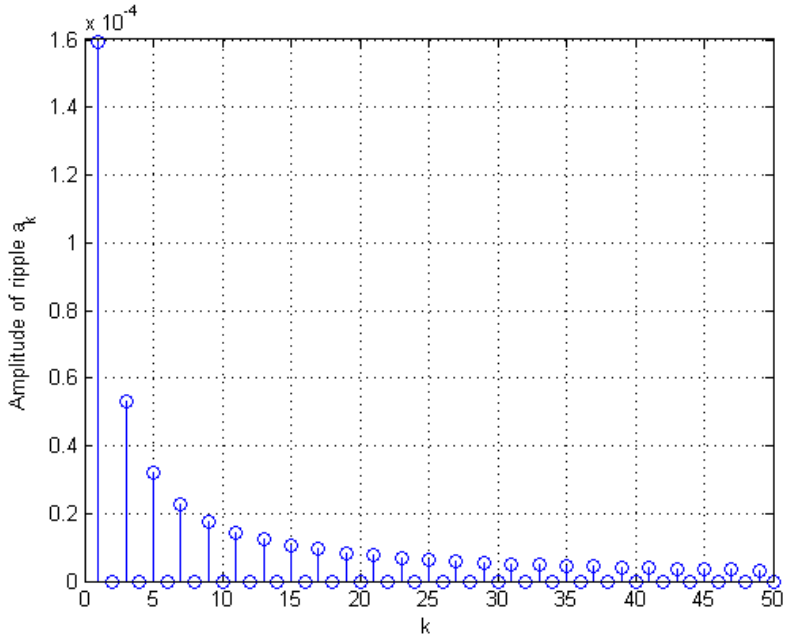


FIGURE 2.7: Frequency Spectrum of Dem'ed current mirror

such a circuit output ripple will not be a simple square wave. The output will be a much complex signal (see figure 1.7) but the conclusion will be the same. To separate AC ripple from the DC signal, a low pass filter should be applied at the output. After knowing the distribution of this ripple in frequency domain, an efficient filter can be designed [22] to separate AC from DC.

2.4.2 Advantages and Limitation

This technique has several advantages which are as follows:

1) A very high DC accuracy can be obtained.

2) Based on the selection of DEM frequency, the $1/f$ noise can be eliminated.

The major disadvantage of this technique is large ripple at the DEM frequency. The magnitude of this ripple can either by reduced by degenerating the mirror devices or trimming it before doing DEM. Alternatively, DEM ripple can also be suppressed by an off-chip low pass filter. This will be discussed in the section 2.6. However, there is a

need to develop new techniques, which can get rid of the ripple without the use of an external low pass filter.

2.5 Trimming Technique

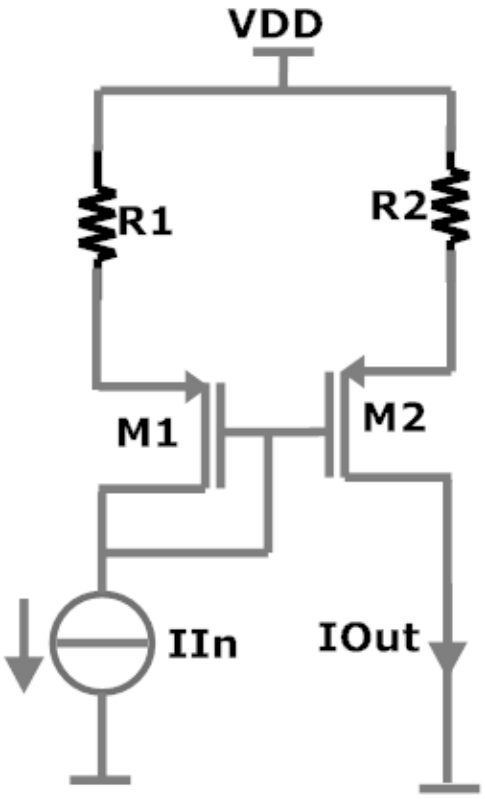


FIGURE 2.8: Precision current mirror by using laser trimming

Trimming is another technique that allows designing a high precision current mirror. Trimming can be referred as one-time adjustment, which is done after the chip has been fabricated to remove the relative mismatch between mirror devices. It does not use DEM or automatic calibration technique (on-chip) to achieve the desired accuracy.

2.5.1 Working Principle

The circuit shown in the figure 2.8 is a 1:1 high precision current mirror that uses laser trimming [2]. 'IIn' is the input current that needs to be copied and 'IOut' is the output current. R1 and R2 are degeneration resistances used for improving the matching between M1 and M2 [19]. A systematic mismatch is deliberately added in the circuit by choosing a higher value of R1 compared to R2. Once the chip is fabricated the value

of R2 is increased by laser trim. The value of R2 is increased up to that extent, till the source-gate voltage of M1 becomes equal to source-gate voltage of M2. The mismatch between the source-drain voltages are taken care by using gain-boosting and cascoding [6, 19]. This ensures equal current flow through both M1 and M2.

2.5.2 Advantages and Limitation

A high DC accuracy is obtained by this technique but it has some limitations, which are as follows:

1) More cost in production due to use of laser trimming.

2) Trimming is not valid over changing input current levels and temperature drifts.

3) More compliance voltage is needed because of additional voltage drop over degeneration resistances.

2.6 Ripple Reduction Technique

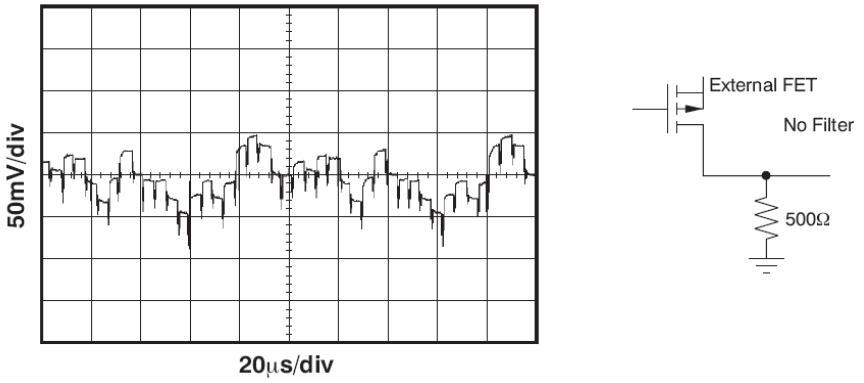


FIGURE 2.9: DEM ripple without filter

A standard technique to suppress the DEM ripple is to use an external low pass filter. Figure 2.9 shows the DEM ripple at the output of the XTR111 [4] when no filter is used. This ripple is at a full scale output current level of 25mA (worst case). After filtering the output signal (with a low pass filter) the peak-to-peak value of DEM ripple is decreased by nearly one order of magnitude (see figure 2.10). The use of filter is not preferred because it is off-chip and bulky component. Therefore, it is desired to develop

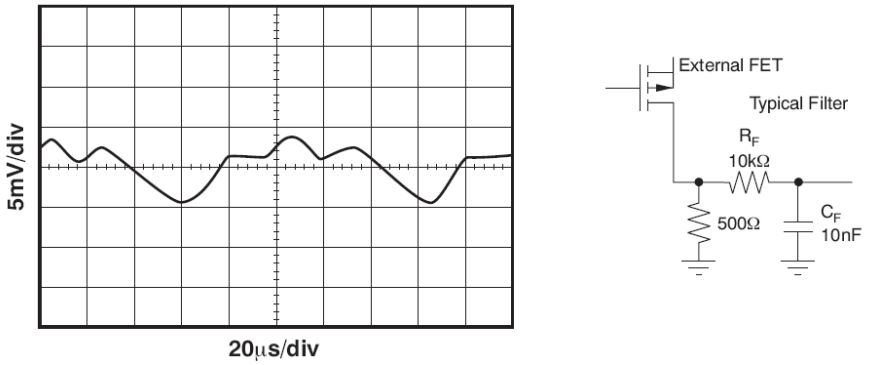


FIGURE 2.10: DEM ripple after adding filter

a new technique, which can get rid of the unwanted DEM ripple without the use of an external filter.

2.7 Conclusion

This chapter describes the importance and limitation of the CMOS switches used in the design of analog circuits. Further, three useful techniques (a) sampling, (b) modulation and (c) trimming were discussed with their advantages and disadvantages. After this, a standard way to suppress the DEM ripple is described, which makes use of large capacitor off-chip. The use of external capacitor is not desired because it is bulky and off-chip. The following chapter will present a new on-chip technique, which can get rid of unwanted DEM ripple without the use of off-chip components.

Chapter 3

Proposed Circuit Concept

3.1 Introduction

This chapter will present a new technique for designing a precision current mirror. It will further give a brief overview of the complete system-level design, followed by a detailed discussion of the critical blocks with their simulation results. Finally, the chip layout will be shown.

3.2 New Trimming Technique

The new technique is about trimming the mismatch errors before doing Dynamic Element Matching (DEM). It uses the sample and hold technique with DEM. This technique is almost similar to the technique reported in [21]. In this paper, the author used auto-zeroing with chopping. DEM gives a good DC accuracy but at the expense of AC ripple in the output. There are a couple of ways to reduce this ripple. A common practice is to place an off-chip low pass filter to suppress this ripple. This ripple can be both in the current and the voltage domain. Chopping is a special case of DEM when it is used on a pair of device, for example, chopping an input pair of an opamp. To the author's knowledge, there is no existing technique (except [24]) that can reduce the DEM ripple in the current domain without the use of an external low pass filter. The new technique is different from the existing ones. To make the analysis simple DEM will be performed on only 2 devices.

In the existing technique, filtering is followed by DEM (or chopping as DEM is performed only on 2 devices) as shown in the figure 3.1. From the figure 3.1, it is clear how the DEM (or chopping) ripple is reduced. Initially, there is some positive and negative

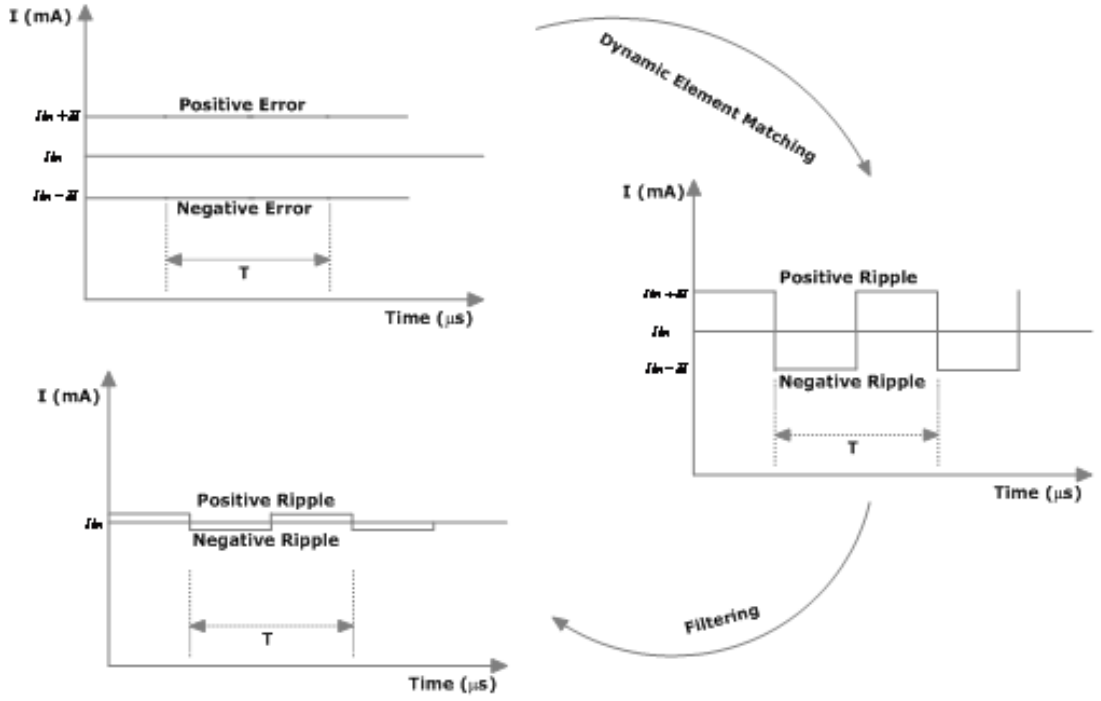


FIGURE 3.1: Existing Sequence

error with respect to the reference current level I_{in}, which needs to be copied by the mirror (refer figure 2.5). The positive and negative error is because of the mismatch between the 2 devices. After the DEM operation (described in section 2.4), there will be a ripple at the output. Finally, this ripple will be suppressed by an off-chip low pass filter.

The method of filtering the DEM ripple can also be applied on-chip. The on-chip solution is restricted only to the voltage domain, especially for the chopping ripple. Moreover, an on-chip solution will increase the chip area (use of big capacitor in the low pass filter) and thus the cost. The idea of suppressing the chopping ripple is not feasible in the current domain because it requires a high quality inductor on-chip, which is difficult to make. In the proposed technique, this problem will be tackled and an efficient on-chip solution will be developed without significantly increasing the chip area.

In the proposed circuit, DEM is followed by calibration as shown in the figure 3.2. DEM ripple can be minimized by calibrating the devices first and then doing DEM as shown in the figure 3.2. This sequence can also be applied for N number of devices. For simplicity DEM on only 2 devices are considered. Amplitude of the DEM ripple is directly proportional to the mismatch among the devices, which are undergoing the DEM operation. If the mismatch among the devices is calibrated out before the DEM operation is performed, the amplitude of the DEM ripple will be less. This is shown in

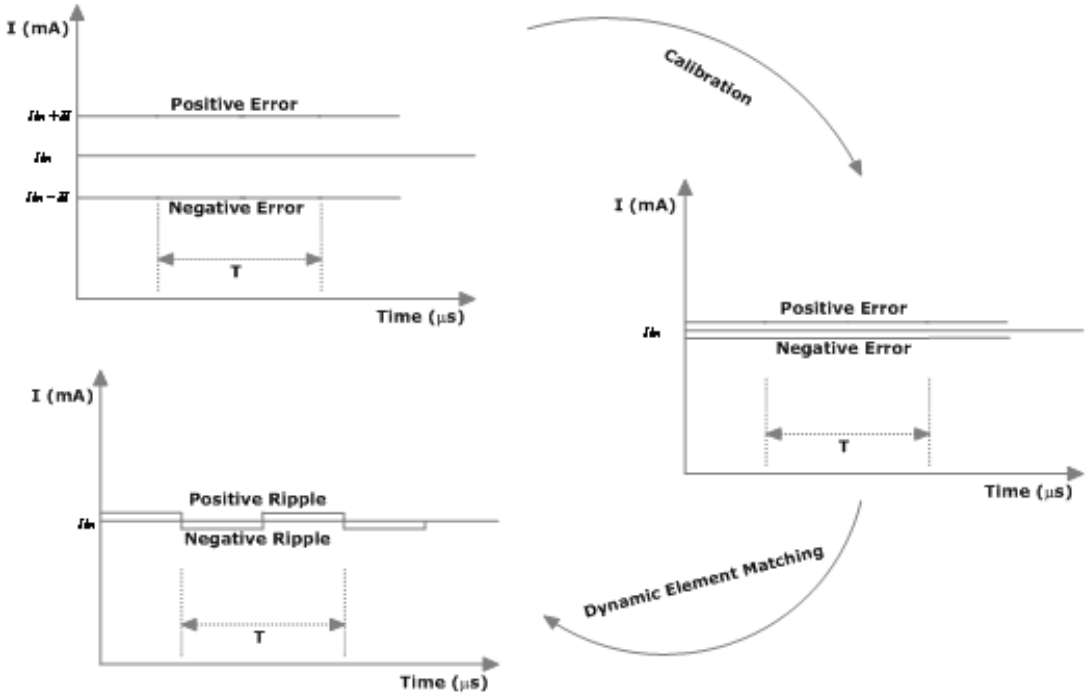


FIGURE 3.2: Proposed Sequence

figure 3.2. In the first step, the mismatch between the devices is reduced by calibration, which decreases the initial error. Finally, the DEM operation is performed, resulting in a smaller ripple.

Hence, the same performance (figure 3.1) can be obtained by designing an on-chip calibration circuit that can calibrate the mismatch prior to the DEM operation (figure 3.2). In [24] the author used the same idea to suppress the DEM ripple in the current domain. He proposed a 2-point calibration technique [24] to reduce the mismatch among the mirror devices before doing DEM. He showed that the error due to the threshold voltage (V_T) variation is dominant at lower current level (couple of μA), while at higher current level (couple of mA) error due to threshold voltage (V_T) variation and beta (β) variation is nearly the same. Based on this result, a 2-point calibration technique was proposed to eliminate the relative mismatch among the mirror devices. In this technique, a sequence of V_T - β - V_T calibration is performed at lower, higher and lower current respectively. Although this technique should achieve good accuracy over a wide current range, it is rather complex and requires a significant amount of extra circuitry.

In this work, a 1-point calibration can be done to remove the relative mismatch among the mirror devices. The 1-point calibration will be performed at the same input current level that needs to be copied. If the mirror devices are calibrated for a specific input

current, then at that current level, the relative mismatch among the mirror devices will be equal to zero. The working principle of a current mirror with a new on-chip 1-point calibration technique will be described next.

3.2.1 Working Principle

The working principle of the new current mirror is very simple. For calibrating the current mirror devices, a separate circuit block will be added to the main current mirror. The main function of the calibration circuit is to eliminate the relative mismatch between the devices.

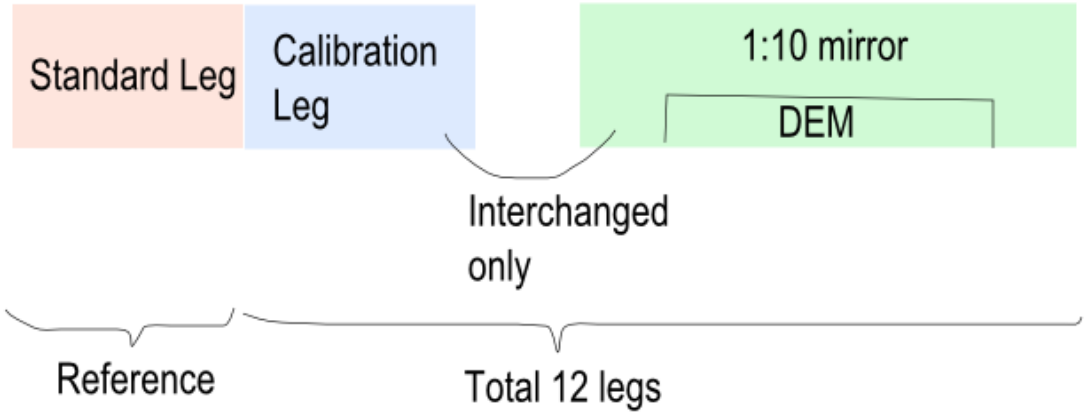


FIGURE 3.3: Calibration scheme

11 devices are needed to make a current mirror with a gain of 10. One of them will be connected to the input and the remaining 10 will be connected to the output of the mirror. In order to reduce the ripple all of them need to be calibrated. This will be done by taking one of the 11 devices out of the main current mirror, calibrating it in a separate calibration circuit, and putting it back into the main mirror. This process will continue for all the 11 devices. Because of the necessity to remove a current leg out of the main mirror for calibration, we need 12 identical current devices. The calibration of the current device involves comparing that leg to a standard device, which is the other addition compared to a normal DEM mirror. Each device will be referred as 'leg' in further discussion. An overview of the complete idea is given in the figure 3.3. The red rectangle is the standard leg and the blue rectangle is the leg which needs to be calibrated. The green rectangle is the 1:10 DEM current mirror. In total there are 12 equal legs and a standard leg. Digital logic will select 2 legs among 12. One of them will be the leg that needs to be calibrated and the other will be connected to the input of the DEM current mirror. The remaining devices will be connected to the output of

TABLE 3.1: Calibration order of 12 legs

L_{std}	L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	L_{10}	L_{11}	L_{12}
1^{st} Step	i/p	cal	o/p	o/p	o/p	o/p	o/p	o/p	o/p	o/p	o/p	o/p
2^{nd} Step	o/p	i/p	cal	o/p	o/p	o/p	o/p	o/p	o/p	o/p	o/p	o/p
...	...	...	...	...	...	...	...	...	...	...	...	...
12^{th} Step	cal	o/p	o/p	o/p	o/p	o/p	o/p	o/p	o/p	o/p	o/p	i/p

the DEM current mirror. This implies that 12 devices will be interchanged periodically between calibration, input or output leg. All the legs in the calibration phase will be calibrated with respect to the same standard leg (red). All the devices are calibrated at the end of a 12 clock period. If these calibrated devices are used to make a DEM current mirror, it is expected to get a high DC accuracy without significant DEM ripple.

Table 3.1 shows the calibration order of the 12 legs. In the first pass, L_1 is the input leg, L_2 is the calibration leg and L_3-L_{12} are the output legs. In the second pass, L_2 (the leg which was calibrated in the first pass) will serve as input, L_3 is the calibration leg and rest are the output legs. This cycle will continue until all the 12 legs are calibrated with respect to the standard leg (L_{std}). Mismatch between the output legs and the input leg will be more when an uncalibrated leg is used as an input compared to a calibrated leg. This is because when the calibrated input leg is compared to the output legs (which consist of zero or more calibrated legs) offers lower error current. In the subsequent cycle, due to increase in the number of calibrated legs at the output, reduces error current linearly to a lower value. After one complete cycle (12 clock periods), the relative mismatch among the legs is eliminated and all the legs will start behaving in the same way. This technique can be used for 1:N current mirror, which will require N+3 devices in total.

Figure 3.4 shows the conceptual circuit that is used to calibrate the mirror devices. It consists of the standard leg and the (interchangeable) calibration leg. In the circuit, both current legs are fed with a current IIn1 and IIn2, which are an inaccurate copies of the main input current IIn (figure 3.5). This leads to a voltage V_{GS} across transistor M_s in the standard leg. The same voltage is forced onto the gate of transistor M_c in the calibration leg via switch S_g. Due to mismatch between the standard leg and the calibration leg, forcing a V_{GS} on transistor M_c that is derived from transistor M_s, leads to the calibration leg outputting a slightly different current than IIn2. This error current flows through switch S_s and then charges or discharges a capacitor C. The voltage across this capacitance is converted into a current through transistor M_3. This current is then fed back to the source of transistor M_c, and it effectively cancels out the initial

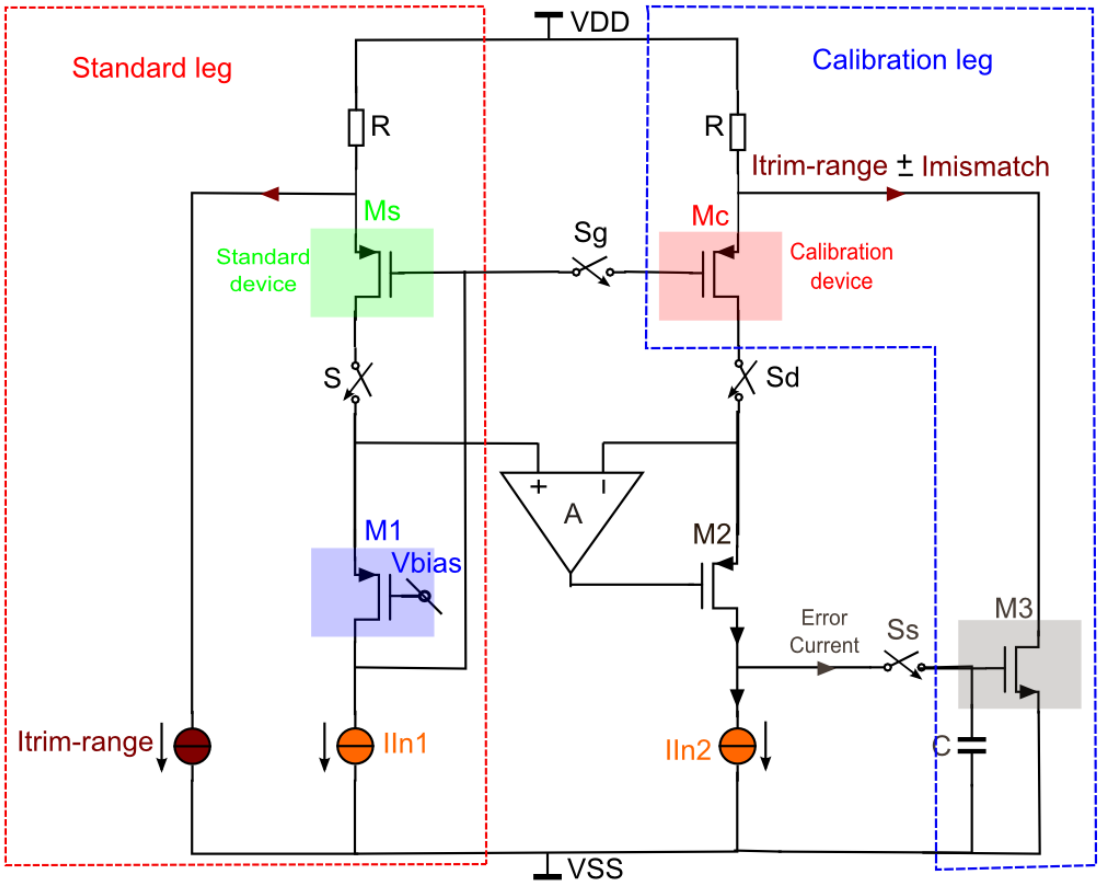


FIGURE 3.4: Calibration circuit

mismatch of the calibration leg. Once the voltage on capacitor C has settled to a final value, switch S_s can be opened, and the calibrated leg can now be used inside the main DEM mirror (figure 3.5). Therefore, as indicated in figure 3.4, each moveable current leg has its own capacitor C and V-I converter M_3. The above described calibration procedure is constantly repeated on all 12 moveable current legs, since temperature changes, discharging of capacitor C or changes to the main input current can cause the calibration to become invalid. Current Itrim-range is needed since the calibration current flowing through transistor M_3 can only take current away from the calibration leg, not add it. Quantitative analysis is done below to make this clear.

Suppose that the threshold voltage of the standard device is less than the threshold voltage of the calibration device (assuming same β for both the devices),

$$V_{T,M_s} < V_{T,M_c} \tag{3.1}$$

then to ensure a same current flow through both the devices, V_{SG} of both the devices should have a relationship as follows:

$$V_{SG,M_s} < V_{SG,M_c} \tag{3.2}$$

To ensure the above condition (equation (3.2)), the trimming current (Itrim-range ± Imismatch) has to flow into the degenerative resistor R, which means the source potential of M_c should be greater than VDD. This is impossible because transistor M_3 can only sink a current. Therefore, a constant current Itrim-range is pulled out from the source of M_s, making sure that the calibration of the M_c is possible when its threshold voltage is greater than the threshold voltage of the standard device. If the equation (3.1) holds true, then the feedback current will be smaller than the Itrim-range which is given by the equation below:

$$Ifeedback = Itrim - range - Imismatch \tag{3.3}$$

otherwise, the feedback current will be greater than the Itrim-range which is:

$$Ifeedback = Itrim - range + Imismatch \tag{3.4}$$

Imismatch is the current which consists of 4 parts:

1) The difference in the current mismatch between M_s and M_c because of V_T and β variations.

2) The current mismatch between IIn1 and IIn2 current.

3) The input-referred offset of amplifier A.

4) The mismatch between two degenerative resistances R.

An amplifier 'A' with transistor M_2 is a regulated cascode, used for regulating the V_{DS} of M_c. M_1 is a cascode transistor of a standard device (M_s). Vbias is a gate bias of M_1, which sets its source voltage, thus the drain voltage of M_c by the help of the regulated cascode structure.

Once the calibration circuit is settled, the calibration leg is disconnected from it and is used in the main DEM mirror shown in figure 3.5. M_{c1-11} with $M_{3,1-11}$ and capacitor C_{1-11} are the legs which are already calibrated (after 11 clock periods). Among them,

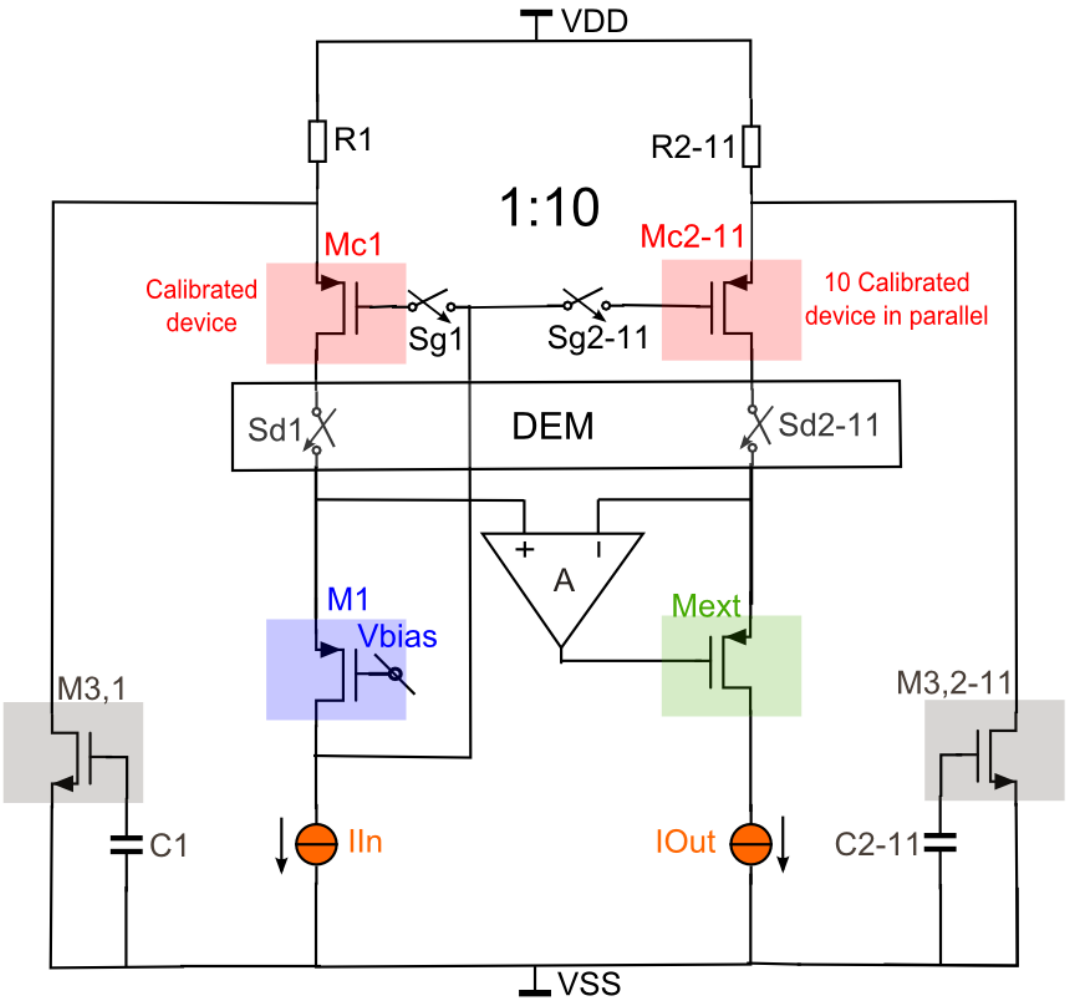


FIGURE 3.5: Main DEM mirror

one will be connected to the input and remaining will be connected to the output. IIn is the input current that needs to be copied. To prevent excessive heating of the chip at the full scale output current of 25mA, an external cascode power device (M_{ext}) will be interfaced with the chip.

If the devices (M_c) are calibrated at a different source-drain voltage compared to the source-drain voltage across the devices when it is used in the main mirror (input or output), there will be a DC error in the output current. Hence, Vbias ensures the same drain-source voltage over the calibrated devices (when it is connected to the main mirror), as in the calibration circuit (figure 3.4). Rectangle represents the DEM operation on 1:10 current mirror.

3.2.2 Advantages and Limitations of the calibration circuit

There are several advantages of the circuit which is used for calibrating the devices. These are as follows:

1) A very simple circuit is used for calibrating the devices.

2) Instead of sampling the signal directly, an error signal is sampled.

3) The variations in the standard leg (process/corners) are not important because all the devices will be calibrated with respect to same standard leg. Same applies to IIn1 and IIn2 (refer figure 3.4).

4) There is no need of a high performance amplifier 'A' (figure 3.4) to regulate the drain-source voltage of the device that needs to be calibrated. An input-referred offset of the amplifier will be the common mode error for all the devices which are getting calibrated.

Since the calibration is not ideal, there are several limitations of this scheme which are as follows:

1) The charge injection and feedthrough from the sampling switch S_s (figure 3.4) will corrupt the final error voltage stored on the sampling capacitor C.

2) The charge leakage from the sampling capacitor C with time (as charge needs to be hold for 11 clock cycles) and temperature will affect the circuit performance.

3) Since IIn1 and IIn2 are inaccurate copies of IIn some residual ripple at the output of the DEM mirror will remain.

4) An extra current (Itrim-range) is needed to calibrate the devices (refer figure 3.4), thus increasing the quiescent current of the circuit.

5) The circuit needs at least 12 clock periods to fully settle.

3.3 Design Considerations

Some design considerations should be taken into account before the actual circuit implementation. The calibration circuit shown in the figure 3.4 is the heart of the complete circuit. Based on the target specifications (refer to section 1.5), some simple hand calculations should be done to estimate the value of different components used in the circuit.

3.3.1 Design values for the calibration circuit

The following hand calculations are made for the circuit shown in the figure 3.4. The compliance voltage of the current mirror extends from ground to 2V (maximum) below the positive supply. Based on this specification, the value of the degeneration resistor 'R' should be chosen. The maximum current that can flow through the degeneration resistor 'R' is 2.5mA (full scale input current). The value of the resistor 'R' should neither be too big nor too small. If the resistor value is large, the voltage drop across it will exceed the compliance voltage specs at 2.5mA of input current. If the resistor value is very small, trimming current (Itrim-range) that needs to be pulled out from the source of M_s will be large. This will increase the total power consumption. Taking all these factors into account the value of the degeneration resistance 'R' is chosen to be 200Ω. The voltage drop over the degeneration resistance 'R' is 500mV for a full scale input current of 2.5mA. Remaining 1.5V will be used by the mirror devices (M_{c2-11}) and external cascode transistor M_{ext} (refer to figure 3.5).

A systematic mismatch (Itrim-range) is added in the standard leg to allow calibration in both the directions. This is already described in the working principle. Itrim-range is a common-mode current for all 12 identical devices (1 calibration leg + 11 mirror legs). Imismatch is an error current at the top of Itrim-range, which includes error due to four main sources:

1) The threshold voltage mismatch between M_s and M_c (translates to a current mismatch via resistance 'R').

2) The beta mismatch between M_s and M_c.

3) The current mismatch between IIn1 and IIn2.

4) An input-referred offset of the amplifier 'A' (translates to a current mismatch via

output impedance of M_c).

If the total contribution of current mismatch values mentioned in 1, 2, 3 and 4 is large, Itrim-range should be designed to have a larger value compared to the total current mismatch. This is necessary for proper working of the calibration circuit (as the current pulled out from the source of Mc should never go below zero). The value of Itrim-range should not be very large because it will increase the total power consumption. Therefore, a large device size should be used to bring down the mismatch. Thus, there is a tradeoff between power consumption and chip area. Based on the above discussion, either Itrim-range should be fixed or the total mismatch for the three cases (1, 2 and 3) should be defined. The value of Itrim-range is set at 20μA. Based on the value of Itrim-range, other design parameters should be calculated such that the total current mismatch (3 sigma) for the three cases (1, 2, and 3) should not exceed 20μA.

The aspect ratio (W/L) of M_s and M_c is set at (600/2.1), which contributes to a threshold voltage mismatch of 0.16mV (one sigma) according to the equation (1.6). Thus, a current mismatch will be 0.8μA (0.16mV/200Ω).

Based on the value of A_β (from the design manual) and aspect ratio (600/2.1), the absolute error in the current between M_s and M_c is 0.014% (1 sigma). This error is calculated by using equation (1.14). For a maximum input current of 2.5mA, the current error due to beta mismatch between the devices is 0.35μA (0.00014*2.5mA).

The current mismatch between IIn1 and IIn2 is set at 1.3μA (one sigma), which is calculated by using the equation (1.6).

A standard folded cascode [19] topology is chosen for amplifier 'A'. At 10μA of input current, the drain voltage of M_s is nearly equal to VDD. To sense the drain voltage of M_s, NMOS input pair is chosen for amplifier 'A'. The maximum input-referred offset of amplifier 'A' is designed to be 3.5mV (1 sigma). At a full scale current of 2.5mA, the output impedance looking inside the drain of M_c is 10kΩ. This offset translates into an error current of 0.35μA (3.5mV/10kΩ).

Thus, total current mismatch (for cases 1, 2, 3 and 4) is equal to $\sqrt{0.8^2 + 0.35^2 + 1.3^2 + 0.35^2}$ = 1.6μA (one sigma). Even for a current mismatch of 6 sigma, the chosen value of Itrim-range is good enough for the calibration circuit to work properly.

To reduce the charge injection, the switch Sg is chosen to be the minimum size. Excess

charge from this switch will change the gate voltage, which is not desired.

3.3.2 Design values for the main DEM mirror

The following hand calculations are made for the circuit shown in the figure 3.5. The value of each resistance (R1-11) is 200Ω. The aspect ratio (W/L) of all the devices (M_{c1-11}) is (600/2.1). This (W/L) is chosen by searching for a large device that is as much in strong inversion as possible, without having a prohibitively large saturation voltage at maximum current (over temperature and corners).

Some hand calculations should be made for the amplifier (A) that is used for driving the gate of the external cascode (M_{ext}) transistor. 'A' is chosen to be a standard folded cascode amplifier with NMOS input pair. Folded cascode topology with NMOS input pair is chosen so that the amplifier can sense a voltage up to positive supply. As per the target specifications, the maximum tolerable error in the output current is 0.1% of 25mA (full scale output current). This translates into an error current of 25μA. The error in the output current arises because of the mismatch between the current mirror legs and offset of the amplifier (A). Since the mirror legs are DEM'ed periodically, the mismatch among them are averaged out over one time period. The dominant source of the error that remains is the offset of the amplifier (A). This offset changes the drain voltage of the mirror legs, thus creating an error in the output current.

The total output conductance of the mirror devices (M_{c2-11}) is 1.15mS. This translates to a maximum error voltage of 21.74mV (25μA/1.15mS), which can be tolerated at the drain of the mirror devices. If amplifier 'A' is designed for an offset of 21.74mV, the error in the output current will be worse as compared to 0.1% (full scale 25mA). This is because of other non-ideal effects on-chip. Taking all these things into consideration, the amplifier (A) will be designed for a maximum input-referred offset of 4.5mV (3 sigma) under all conditions.

Finite gain and voltage mismatch between the input pair (of the amplifier 'A') and current mirror devices (used for biasing the amplifier 'A') are the major contributors of offset. Thus, the total offset can be divided into parts (a) 4mV and (b) 0.5mV that will be contributed by voltage mismatch and finite gain of the amplifier (A) respectively. The sizing of the input pair and current mirror devices (used in the amplifier) are done according to the equation (1.14).

The maximum output voltage from the amplifier 'A' is restricted to 12V below the positive supply (after taking the V_T value of various M_{ext} into account). Open loop gain specification for the amplifier can be calculated from the output voltage and offset requirement (0.5mV). The open loop gain (G) that is required for the amplifier is 24000 (12V/0.5mV). This translates into a gain of 87.6dB. To be on a safer side, the amplifier will be designed for an open loop gain (G) of 100dB.

The amplifier 'A' with M_{ext} forms a 2 stage opamp. Thus, a compensation capacitor of 5pF is added at the output of 'A' for making it stable at the lowest output current of 100μA, that flows through M_{ext} (worst case). From the spice model file of M_{ext}, it was noted that C_{GD} and C_{GS} of this device is equal to 19.5pF and 80pF respectively. The slewing behavior of the whole mirror is dependent on the slew rate of the amplifier 'A'. For a step input of 1V at V_{IN} (figure 1.6), the maximum time which amplifier can take to settle is 10μs (from specifications). This implies that the slew rate of the amplifier should be greater than 0.1V/μs. The slew rate of 'A' depend on tail current and load capacitance, which it needs to drive when a step input is given. The total load capacitance at the output of 'A' is equal to 80pF + 19.5pF + 5pF = 104.5pF. For simple hand calculations, let us assume that the total load capacitance at the output of 'A' is 100pF. Therefore, the tail current that is needed for the amplifier 'A' should be equal to 10μA (100pF*0.1V/μs). NMOS input pair is biased in weak inversion and their g_m is calculated by using $g_m = I_D/nU_T$. The g_m required for the input pair is 100μS (assuming n=2, U_T=25mV and I_D=5μA). Hence, the unity gain bandwidth of the amplifier (A) with M_{ext} should be equal to 650kHz (100μS/2*pi*(19.5pF + 5pF)). The speed of the amplifier 'A' decreases by a factor of 3.9X (19.5pF/5pF), when it is interfaced with M_{ext}. The reduction in the speed is due to the parasitic gate-drain capacitance of M_{ext}. Hence, the amplifier (A) should be designed for a GBW (gain bandwidth product) of at least 2.54MHz (650kHz*3.9) when it is not loaded with M_{ext}.

3.4 System-Level Design

Before going into the actual circuit implementation details, it is very important to understand the complete system and the voltage domain partitioning (VP). The IC process that is used for this design is a 40V process from Texas Instruments (TI). This process provides the flexibility to the designer, to use either a high voltage device (5V gate-source and 40V drain-source; 40V gate-source and drain-source tolerable) or a low voltage device (5V drain-source and 5V gate-source tolerable). From the process manual (from TI), it was noted that the mismatch coefficient of a high voltage device is much worse compared to a low voltage device. Moreover, high voltage device needs a larger chip

area, and have poor g_m and large parasitic capacitance. Therefore, the high voltage devices should be used only when it is needed.

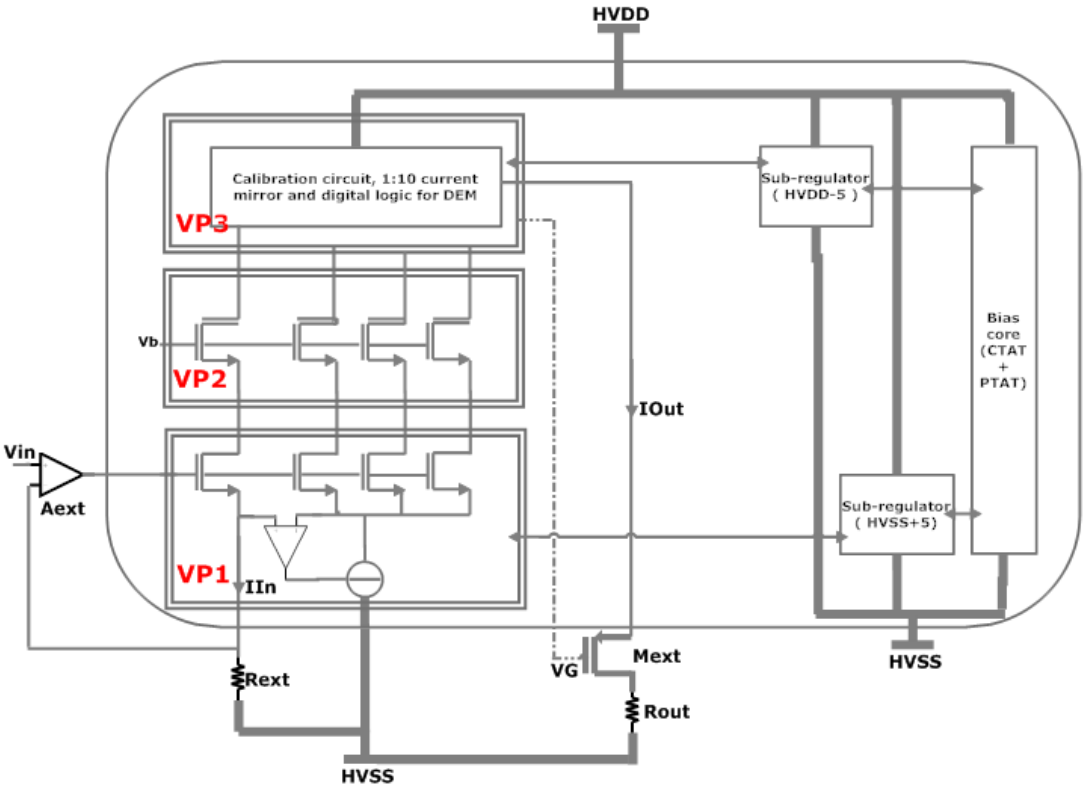


FIGURE 3.6: System Level Diagram

The system level diagram is shown in figure 3.6. Amplifier (Aext) and resistor (Rext) are off-chip components. The ratio of Vin (input voltage to the Aext) over resistor Rext sets an input current that needs to be copied by the mirror. The end goal of the product is to integrate the external amplifier (Aext) as well, but that because of limited time, it was kept off-chip as it is not essential to prove the new mirror concept. The output current (IOut) is 10 times the input current (IIn). Since the output current from the mirror is 25mA for a full scale input current of 2.5mA, hence a power device (Mext) is interfaced with the chip to prevent it from overheating. The gate drive (VG) for the power device is generated inside the chip. Rout is the load resistance. On the right side of the figure 3.6, there is a CTAT + PTAT biasing core (giving a bias current independent of temperature variations). There are two sub-regulators, which act as supply for other circuit blocks. The one at the bottom gives 5 volts up from the negative rail (HVSS), while the top one gives 5 volts down from the positive rail (HVDD). On the left side of the figure 3.6, the block at the bottom is responsible for generating an input,

adaptive bias and trimming currents (IIn1 and IIn2) that needs to be fed to the calibration circuit (figure 3.9). The block at the top contains the calibration circuit, 1:10 DEM current mirror and a digital circuit for generating the control signals. The control signals (coming from the digital circuit) will decide which leg among the 12 legs will be the calibration, input or output legs. The block between the top and the bottom block contains drain extended transistors (5V gate-source and 40V drain-source), which are used for translating the input signal from a low-side to a high-side. Finally, the bold line represents the external power supply and a line with double sided arrow depicts the interaction of various blocks with each other.

3.4.1 Voltage Domain Partitioning

The output current from the mirror can only be sourced; therefore the whole mirror can be in a high-side isolation well except for the input current block that needs to be at a low-side to interface with a low-voltage opamp. An external input opamp Aext is added, which generates an input current by dropping Vin over Rext. On the left side of the figure 3.6, both the top and the bottom block needs matching. This makes the use of a low voltage transistor an obvious design choice. Hence, the complete system can be divided into 3 voltage partitions (VP). VP-1, VP-2 and VP-3 as shown in the figure 3.6. VP-1, VP-2 and VP-3 are working from HVSS to HVSS+5, HVVSS+5 to HVVDD-5 and HVVDD-5 to HVVDD respectively.

3.5 Circuit Implementation

This section will explain the implementation of critical circuit blocks that are used for making the DEM current mirror. The simulation results will be accompanied with the circuit description. These blocks are very important for achieving the target specifications (refer to section 1.5) set for the DEM current mirror.

3.5.1 Input and trim current generation

The circuit shown in figure 3.7 is used for generating two currents (I_{In1} and I_{In2}), which are an inaccurate copies of the input current I_{in}. I_{ab} is an adaptive bias current which changes with the input current level I_{in}. This biasing current is used for providing the gate bias for the cascode transistor in the calibration and the DEM mirror circuit.

An input current I_{in} is generated by dropping a voltage V_{in} over an external resistor R_{ext}. Resistance R_{ext} and an amplifier A_{ext} shown in the figure 3.7 are off-chip. The input current can be measured directly by placing a multimeter between R_{ext} and R_1 during the measurements. Thus, offset of the amplifier A_{ext} will not play an important role in determining the accuracy of the DEM current mirror. The relation between the input current (I_{in}) flowing through the circuit and the voltage (V_{in}) at the positive terminal of A_{ext} can be expressed as:

$$I_{in} = \frac{V_{in}}{R_{ext}} \tag{3.5}$$

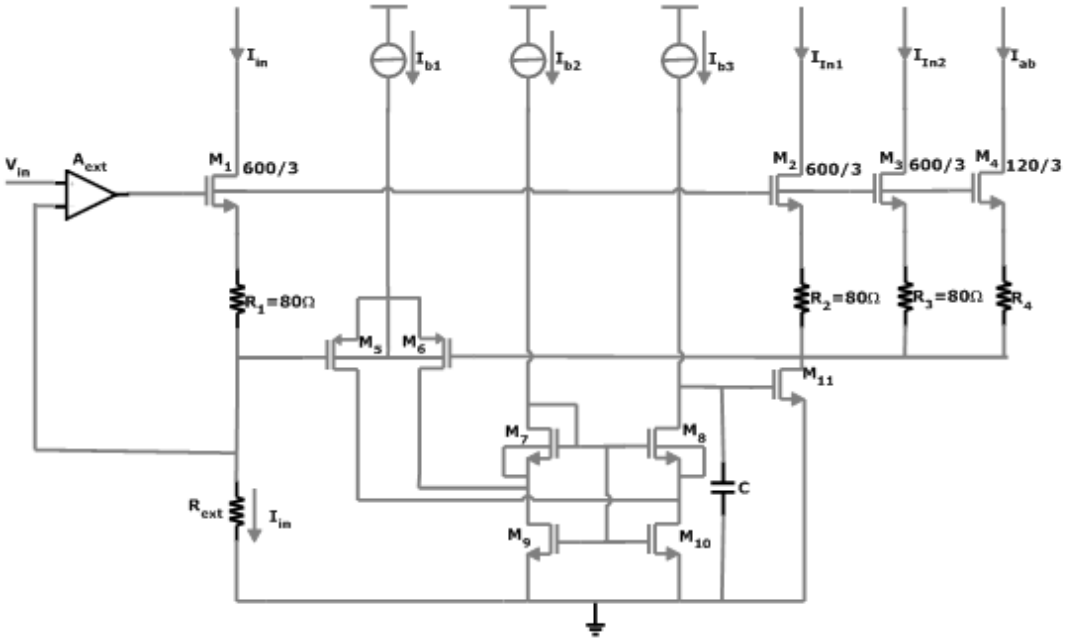


FIGURE 3.7: Input, trim and adaptive biasing current generation

M_5-M_{10} is a folded cascode opamp for regulating the node voltage, which is connected to the gate of M_6. The opamp is needed because M_2 and M_3 are mirroring the current flowing through M_1, hence source voltage of the devices should be kept same. M_5-M_{10} with M_{11} form a 2-stage amplifier which needs miller compensation. So a 4pF compensation capacitor 'C' is added for stability. Since V_{in} can nearly go up to negative rail (0V), the folded cascode amplifier (M_5-M_{10}) with PMOS input pair (M_5 and M_6) is chosen to sense the voltage up to 0V. R_1-R_4 are degeneration resistances used for improving the matching of devices M_1-M_4 [19]. The transconductance g_{m1} of M_1 after degenerating it with resistance R_1 is given by:

$$g_{m1} = \frac{g_{m'}}{1 + g_{m'} R_1} \tag{3.6}$$

where $g_{m'}$ is the initial transconductance of the device M_1 before degeneration. The devices are degenerated to improve the matching among them. I_{b1}-I_{b3} are the biasing currents for folded cascode amplifier which come from the PTAT + CTAT biasing core.

The specification of the input current (I_{in}) range is from 10μA-2.5mA for an input voltage (V_{in}) ranging from 0-5V of A_{ext}, therefore for a maximum voltage drop of 200mV at 2.5mA, the value selected for resistor R_1-R_3 is 80ohm. M_2 and M_3 are used for copying the input current and generating 2 currents I_{In1} and I_{In2}. Therefore, (W/L) of the devices M_1-M_3 are equal. I_{ab} is a bias current designed to be 5 times lower than the input current I_{in}, implying (W/L) of the M_4 is 5X less than M_1. To maintain the same voltage drop of 200mV over the degeneration resistor R_4 its value should be equal to 400Ω. It is very important to make sure that voltage drop over all the 4 resistors R_1-R_4 are the same. If the voltage drop over the degeneration resistance is not equal, the source voltage of the device M_1 will be different than the source voltages of the devices M_2, M_3 and M_4, which will produce a copy current much different from the input current. The copy currents should be as close as possible to the input current I_{in} for the new principle to work properly (refer section 3.2.2). The value of each bias current (I_{b1}-I_{b3}) is chosen to be 10uA. The maximum input-referred offset of the 2-stage amplifier is 5mV over process/corners and monte-carlo simulations. The following σ deviation formula has been used for designing the aspect ratio of the input pair and current mirror used in designing a 2-stage folded cascode amplifier.

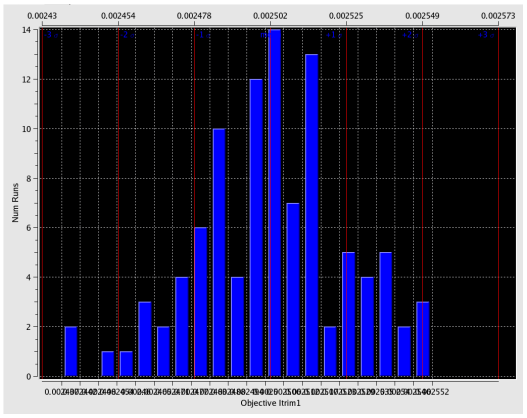
$$\sigma^2_{V_{offset,input}} = \sigma^2_{V_{T5,6}} + (\frac{g_{m9,10}}{g_{m5,6}})^2\sigma^2_{V_{T9,10}} + (\frac{g_{mI_{b2},I_{b3}}}{g_{m5,6}})^2\sigma^2_{V_{I_{b2},I_{b3}}} \tag{3.7}$$

From the equation (3.7) it is clear that $g_{m5,6}$ (transconductance of an input pair) should be greater than $g_{m9,10}$ and $g_{mI_{b2},I_{b3}}$ (transconductance of current mirrors) for getting a lower input referred offset. W/L of the devices are chosen based on the $A_{V,T}$ mismatch data from the process manual.

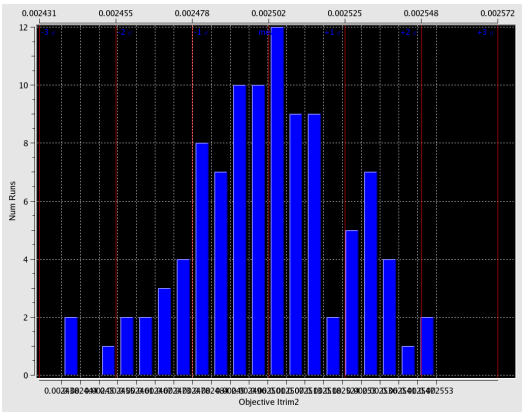
Figure 3.8 (a) and (b) shows the statistical variation in the two copy currents with respect to the input current I_{in}. For this simulation I_{in} is set at a full scale current of 2.5mA. This result includes the relative mismatch between the mirror devices (M_1, M_2 and M_1, M_3), degeneration resistances (R_1, R_2 and R_1, R_3) and the offset of the folded cascode amplifier (M_5-M_{10}). The standard deviation (σ) value of I_{In1} from the simulation at 27°C is:

$$\sigma = 23.70\mu\text{A}$$

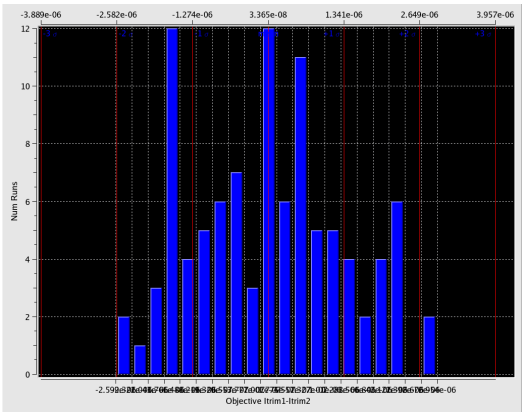
While the standard deviation (σ) values of I_{In2} from the simulation at 27°C is:



(a) I_{In1}



(b) I_{In2}



(c) I_{In1}-I_{In2}

FIGURE 3.8: 100 monte-carlo runs at 27°C for showing the variations in a) I_{In1} b) I_{In2} with respect to input current level I_{in} = 2.5mA c) Mismatch between I_{In1} and I_{In2}

$$\sigma = 23.40\mu\text{A}$$

The difference between the sigma values of I_{In1} and I_{In2} is purely caused by random statistical variation, as both the current sources are designed exactly equal.

Offset of the folded cascode amplifier will not play any role because both the degeneration resistances (R_2, R_3) are connected at the same point in the circuit. From the simulation result shown in the figure 3.8(c), the mean (μ) and the standard deviation (σ) values gives the relative mismatch between the current sources (I_{In1} and I_{In2})

$$\sigma = 1.307\text{uA}$$

3.5.2 Calibration circuit

The circuit shown in figure 3.9 is used for calibrating the DEM mirror devices. M_{std} is

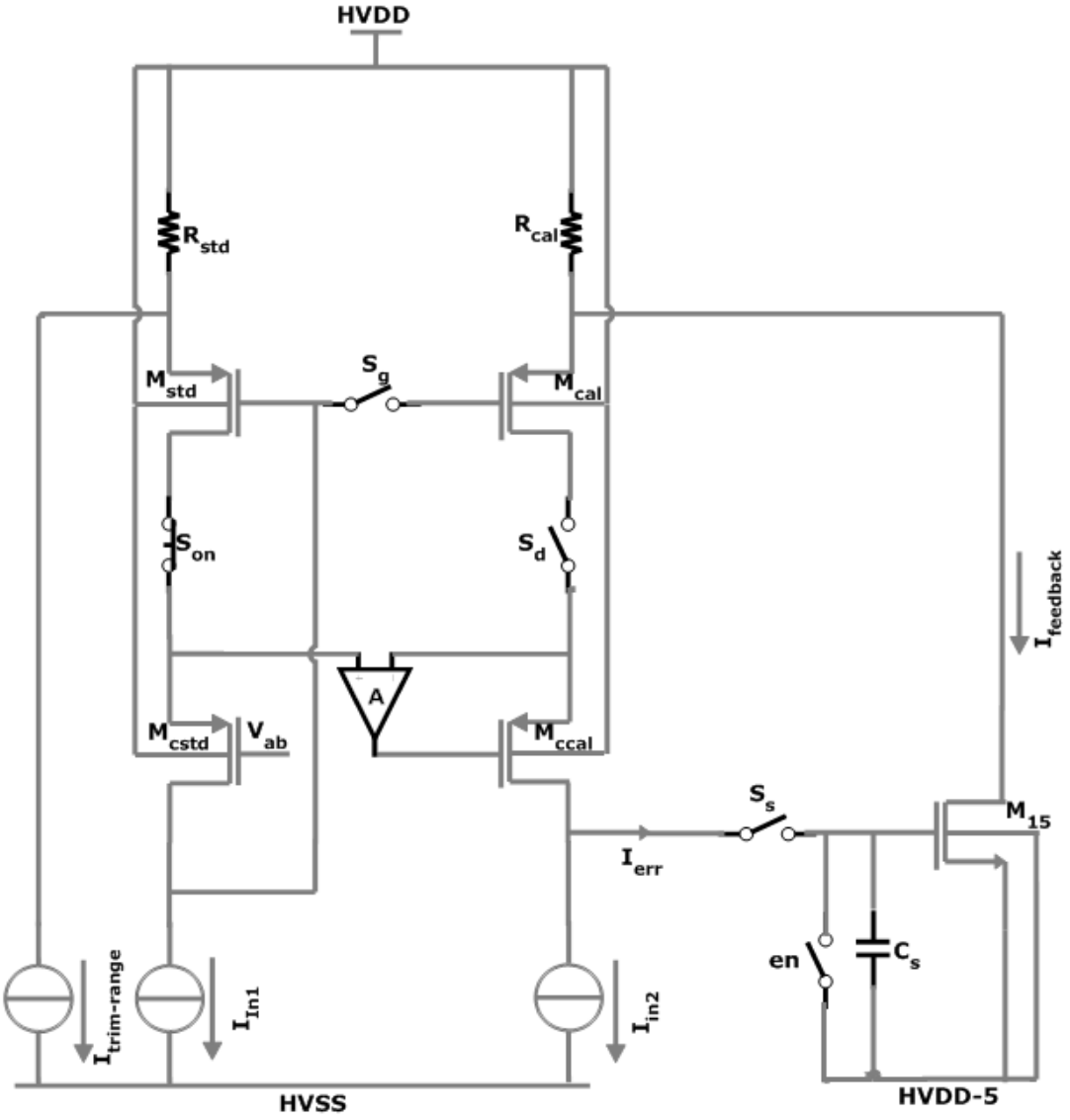
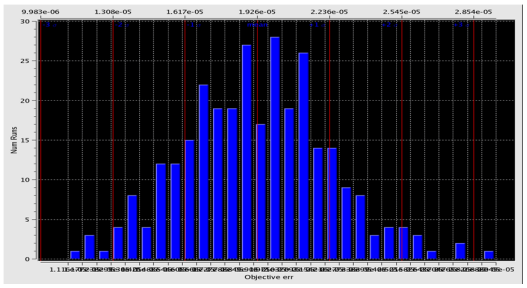
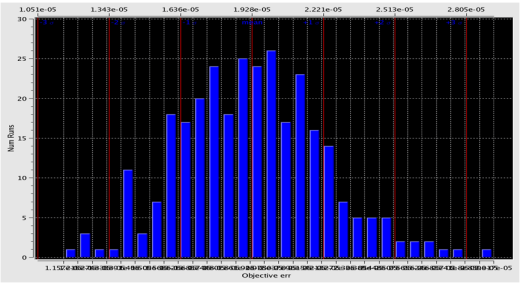


FIGURE 3.9: Calibration circuit

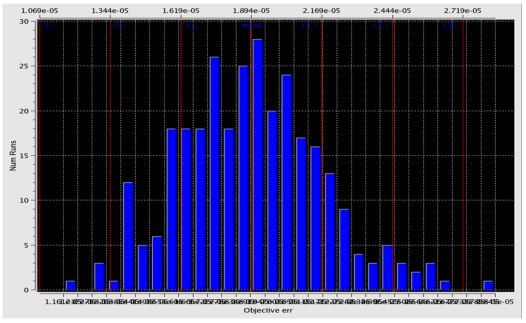
the standard device that will be used for calibrating the M_{cal} (one of the DEM mirror device among 11). The resistance R_{std} and R_{cal} serves two purposes. Firstly, these resistances are used to improve the matching of M_{std} and M_{cal} by degenerating them. Secondly, R_{std} is used convert the constant current $I_{trim-range}$ into a voltage, which adds a systematic mismatch at the source of device M_{std} with respect to M_{cal}. This is necessary to allow the calibration to work in both direction (refer to section 3.2.1). R_{cal} is used to convert the error current (due to V_{TH} and β mismatch between M_{std} and M_{cal}) into a correction voltage at the source of M_{cal} to ensure equal current flow from



(a) $I_{feedback}$ at -55°C



(b) $I_{feedback}$ at 27°C



(c) $I_{feedback}$ at 150°C

FIGURE 3.10: 300 monte-carlo runs over temperature for predicting the value of error current

both the standard and the calibrating devices. The maximum value of the degeneration resistance is limited by the specifications on the compliance voltage of the DEM current mirror as discussed in section 3.3.

M_{cstd} and M_{ccal} are the cascode transistors. I_{In1} and I_{In2} are the trimming currents, which are coming from the circuit shown in the figure 3.7. V_{ab} is an adaptive bias voltage, which changes with the input current level (or trim current, which is an inaccurate copy of the input current). 'en' is a switch that allow to switch between only DEM or calibration + DEM. When 'en' is OFF (open) calibration + DEM is enabled else DEM (only) will take place.

The amplifier 'A' is a folded cascode amplifier with NMOS input pair, which is used for regulating the source-drain voltage of the calibration device M_{cal}. The requirements for this amplifier are relaxed because the offset of the amplifier is not important as it is a common mode error. The gain of the amplifier is chosen to 50dB and maximum input-referred offset of 10mV. The amplifier 'A' with M_{cal} forms the 2 stage amplifier. The stability of the amplifier is checked for the worst case, when 2 trim currents (I_{In1}

and I_{In2}) are equal to 10uA. At the minimum current level of 10uA, the transconductance $g_{m,Mccal}$ of M_{ccal} reduces, which shifts the second pole at the lower frequency, thus causing stability problems. To make the circuit stable, a capacitor of 1.5pF is added at the output of the amplifier 'A', which improves the phase margin. The phase margin is equal to 55°.

$I_{trim-range}$ is the constant current taken out from the source of M_{std} to allow the calibration of the device M_{cal} in both the directions. The value of the $I_{trim-range}$ is chosen to be 20μA. Monte-carlo simulations are done to verify this value. It is obvious that the maximum feedback error ($I_{feedback}$) will be at the full scale input current (I_{in}) of 2.5mA, hence simulation results will be presented for only this case. The figure 3.10 shows the statistical distribution of the feedback current ($I_{feedback}$), which is pulled out from the source of M_{cal}, over monte-carlo runs and temperature sweep (-55°C - 150°C) at the full scale input current I_{in} of 2.5mA. The mean (μ) and the standard deviation (σ) values can be calculated from the simulation result. These values are listed in table 3.2. It is clear from the table that even for 6σ deviation in the feedback current, the calibration scheme will work, provided $I_{trim-range}$ is equal to 20μA.

TABLE 3.2: Mean (μ) and sigma (σ) of $I_{feedback}$ at full scale input current (I_{in}) of 2.5mA

Temperature (°C)	μ (μA)	σ (μA)
-55	19.26	3.09
27	19.28	2.92
150	18.93	2.75

It is to be noted that the source potential of device M_{15} and the bottom plate of the capacitor C_s is at HVDD-5 Volts, which is coming from a sub-regulator. This voltage should not go below 6V from the positive rail because M_{15} is a low voltage device (5V drain-source and 5V gate-source). The stability of the voltage sub-regulator is very important, which will be discussed in the next sub-section.

C_s is the sampling capacitor, which will store the error voltage (refer to section 3.2.1). This error voltage will be multiplied by the transconductance of M_{15}, resulting in a current that will be pulled out from the source of M_{cal}. The settling time of the error voltage on the capacitor C_s will depend on the error current and ON resistance of the switch S_s. There is a tradeoff between the charge injection and ON resistance of the switch. In this particular circuit, the settling time of the sampling capacitor is limited by the error current, which is used for charging it.

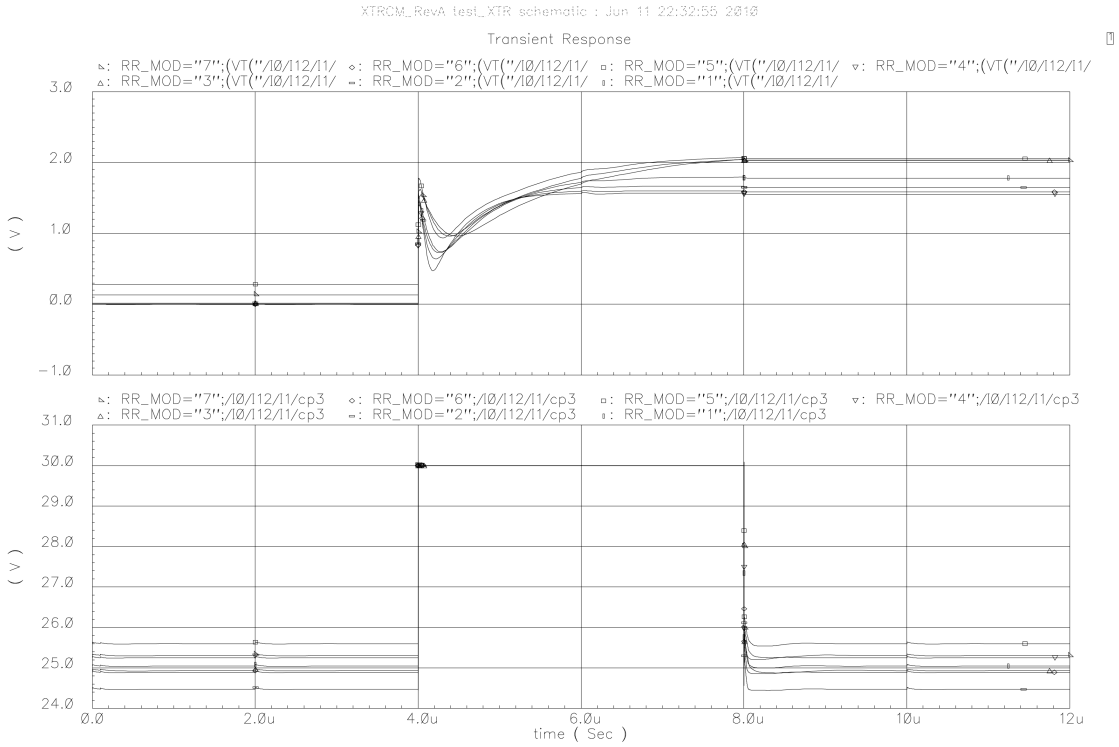


FIGURE 3.11: Voltage on the sampling capacitor C_s over process/corners and temperature

The size (W/L) of a switch S_s is chosen such that the charge injection from it is minimum. The ON resistance of the switch S_s is 1.25kΩ and the value of the sampling capacitor C_s is equal to 500fF. The RC time constant will then be 62.5ns. The circuit is running at a clock frequency of 250kHz, which means that 4μs of the time is available for every sampling capacitor to settle.

The worse case settling time of the capacitor will be at the minimum current of 10μA because the available error current (available for charging the sampling capacitor) at this point is less (although fluctuating).

It is important to verify that the voltage on the sampling capacitor is settled over all process/corners and temperature when input current (I_{in}) is equal to 10μA. Figure 3.11 shows the simulation result of the error voltage across the sampling capacitor over all corners and temperature (-55°C-150°C), when the device is in the sampling phase (when switch S_s is ON) from 4μs-8μs. The final error voltage (27°C) difference stored across the sampling capacitor C_s is 1.8V. The charge injection from the switch S_s is nearly equal to 10mV, creating an error of 0.5% on the top of the error voltage, which will

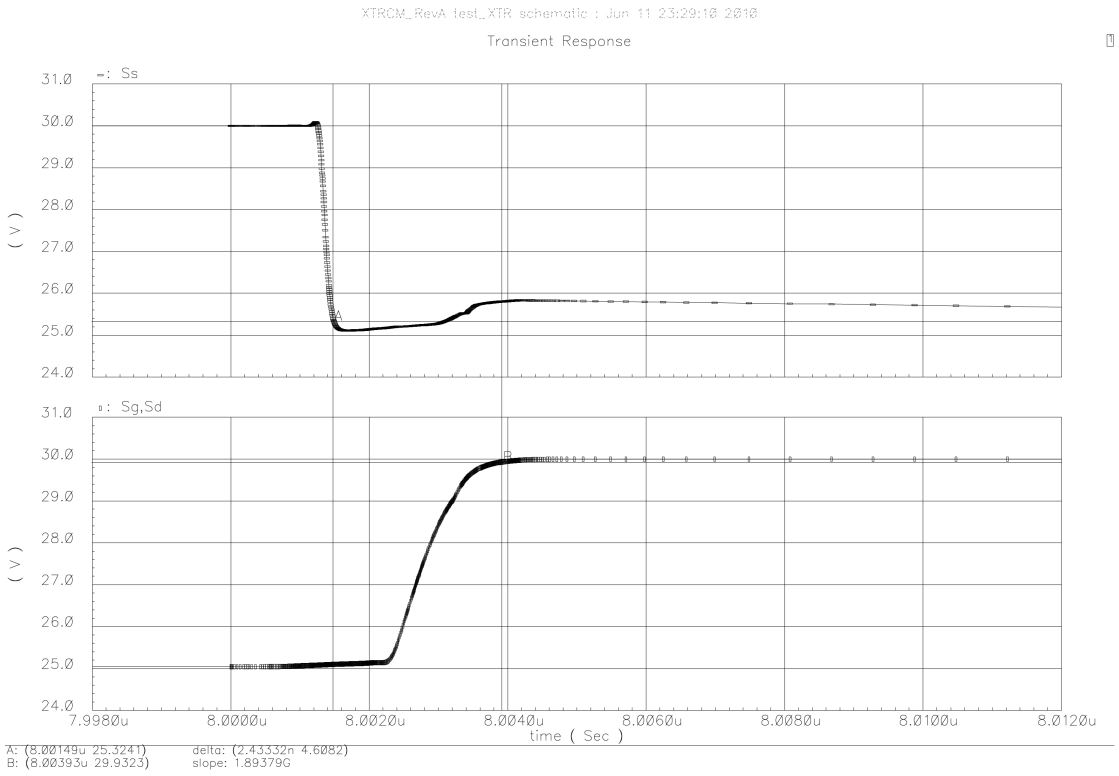


FIGURE 3.12: Switching scheme for S_s, S_g and S_d

limits the ripple reduction to 200X (1/0.5%). There is no need to further reduce the charge injection from S_s, hence dummy switches was not used.

S_s, S_g, S_d and S_{on} are the four switches used in this circuit (refer to figure 3.9). S_g, S_d and S_{on} are implemented using PMOS and S_s is implemented using NMOS transistor. S_s is the sampling switch. S_g and S_d are the switches that are used to connect and disconnect the device from the calibration circuit. S_{on} is the dummy switch which is always ON. This switch is added in the standard branch to match the voltage drop across the switch S_d in the calibration branch. Hence the size of both the switches S_d and S_{on} are kept same. It is very important to disconnect the sampling switch S_s before switching other things in the circuit. This makes sure that the sampling voltage is correctly held on the capacitor C_s. The time difference between disconnecting the switch S_s before disconnecting S_g and S_d is approximately equal to 2.5ns. The figure 3.12 shows the simulation result in which sampling switch is disconnected before other two switches.

3.5.3 Sub-regulator

Figure 3.13 shows the voltage sub-regulator circuit working from the positive rail. V_{b1} is the bias voltage going inside the clamp circuit (refer to figure 3.22).

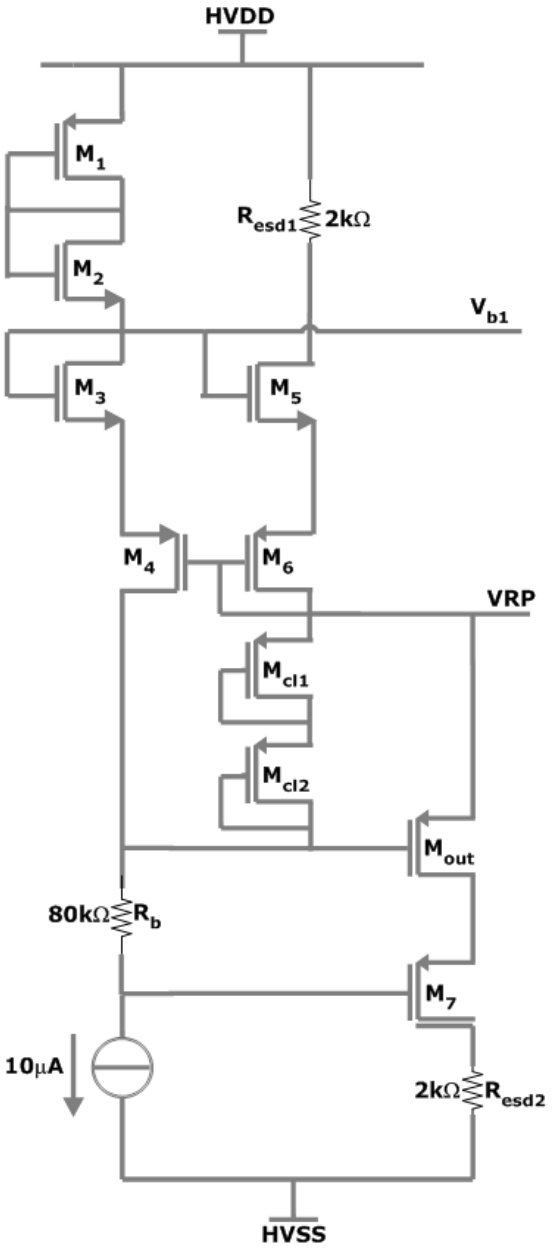


FIGURE 3.13: Voltage Sub-regulator working from positive rail

The output of the sub-regulator VRP is designed to be 5V below the HVDD. R_{esd1} and R_{esd2} are 2kΩ resistances used for the electro static discharge (esd) protection. M_5 set the bias current for M_{out}. M_{cl1} and M_{cl2} are the clamps used for protecting M_{out} from

over-voltage stress. The series connection of the diodes M_1, M_2, M_3 and M_4 sets the output voltage (VRP) of the sub-regulator to 5V below the positive rail (HVDD). It is very important to make sure that the maximum output voltage from the sub-regulator should not go below 6V from HVDD, because it is acting as a ground supply for many low voltage devices working from the positive rail. The simulated output voltage of the sub-regulator over all corners and temperature (-55°C-150°C) is between 24.5V to 25.6V. This sub-regulator was taken from another project. Only few things were modified to make it useful for the new mirror circuit.

The stability and the output impedance of the sub-regulator shown in the figure 3.13 are also very important. To ensure stability, $g_{m,M_{out}}$ should be greater than g_{m,M_4} in all conditions. Since the output of the sub-regulator is acting as a ground supply for low voltage devices, the output impedance of the sub-regulator should be designed such that the voltage fluctuations (due to current sink) at the output is within the specification (maximum 6V below HVDD). The total current that will be sinked into the output of the sub-regulator is approximately 300μA, out of which 220μA is coming from the 11 mirror segments and the remaining current is the error current and bias current for the other circuits. If the output impedance of the sub-regulator is 1kΩ, then the voltage fluctuation at the output will be 300mV for a current of 300μA. Hence, the sub-regulator is designed for an output impedance of 800Ω (27°C). M_4 and M_{out} are used in feedback to lower the output impedance of the sub-regulator. The output impedance ($R_{out,VRP}$) of the sub-regulator will depend on $g_{m,M_{out}}$, which will be

$$R_{out,VRP} = \frac{1}{g_{m,M_{out}}} \tag{3.8}$$

The requirement on the $g_{m,M_{out}}$ can be calculated from the equation above.

3.5.4 Main mirror circuit

The main current mirror circuit is shown in the figure 3.5. Since the working of this circuit is already discussed in the section 3.2.1, therefore this subsection will focus only on those parts which are very important in the design. The gate bias (Vbias) of the cascode transistor M_1 should be same in both the calibration and main mirror circuit. If the gate bias is different, then there will be some residual error in the output current (due to different source-drain voltage across the device in the calibration phase compared to when it is connected in the main mirror circuit as an input or output leg).

Figure 3.14 shows the folded cascode amplifier (A) that provides the gate drive for

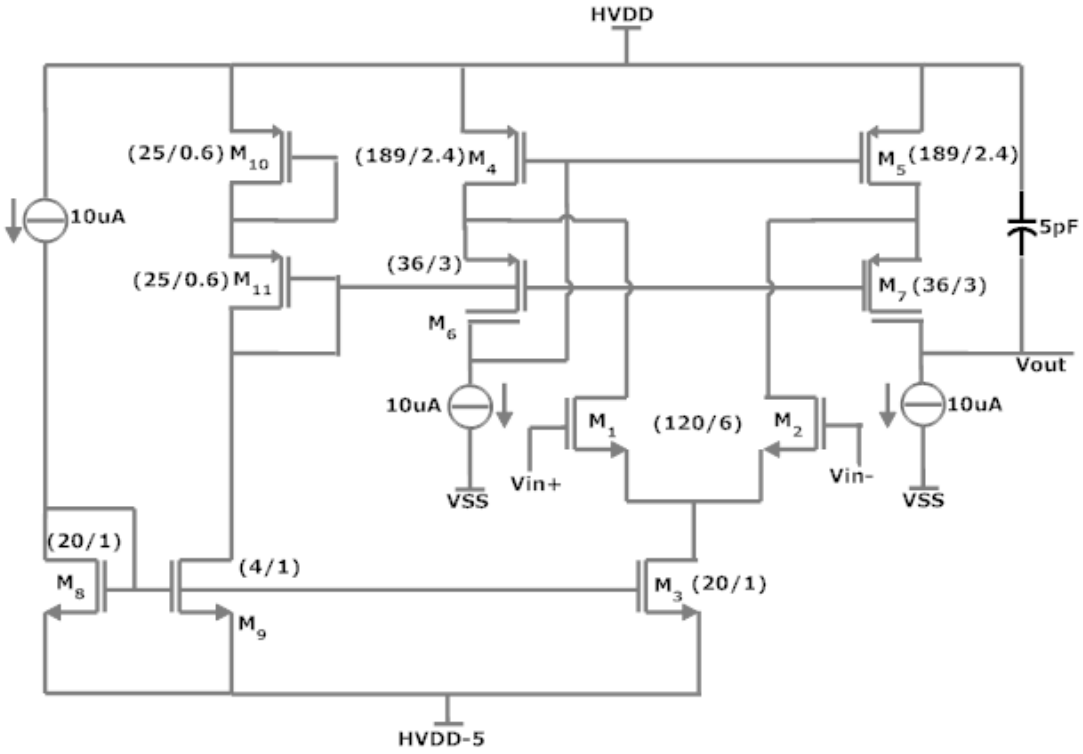
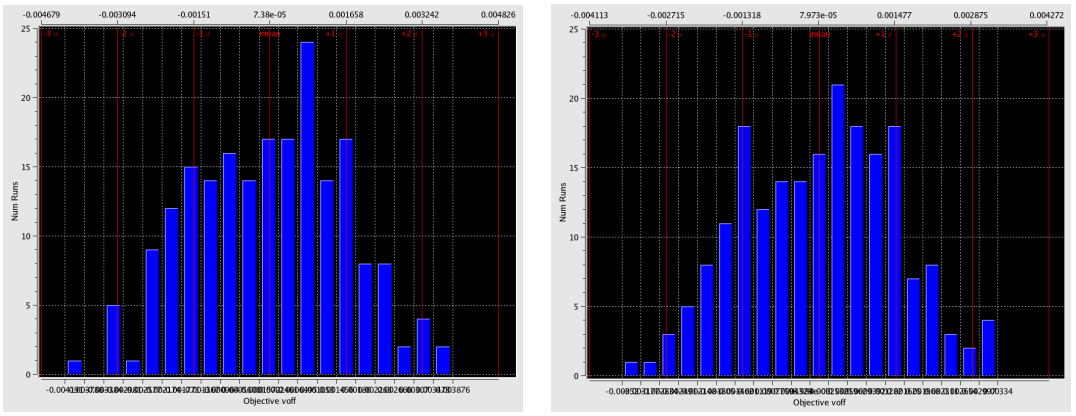


FIGURE 3.14: Amplifier for driving the gate of external cascode M_{ext}

the external power device (M_{ext}). M_1 and M_2 are the NMOS input pair having aspect ratio of (120/6) (indicated in the figure 3.14). M_4 and M_5 is the current mirror. The matching of the input pair and current mirror are very important for achieving low offset. This will be taken care in the layout design. All the currents of 10μA, M_8, M_9, M_{10} and M_{11} are used for biasing. M_6 and M_7 are high-voltage drain extended transistors. They are used because the required gate drive for external power MOSFET (M_{ext}) can go much below HVDD-5.

Figure 3.15 shows the statistical variation of the offset of the amplifier A (refer to figure 3.5) over temperature. The worst case input-referred offset is 4.83mV (3 sigma) at -55°C.

The frequency response of an unloaded amplifier (A) in open loop configuration is shown in the figure 3.16. The open loop gain of the amplifier is 100dB, GBW is 2.88MHz and phase margin is equal to 82°. Figure 3.17 shows the frequency response of the amplifier with M_{ext} at 100μA of output current (worst case). It can be seen from the plot that the speed of the amplifier is decreased because of loading. The gain of the amplifier is 100dB, GBW is 673kHz and phase margin is 90°. Hence, the amplifier (A) is stable



(a) V_{offset} at -55°C

(b) V_{offset} at 27°C

(c) V_{offset} at 150°C

FIGURE 3.15: 200 monte-carlo runs over temperature for verifying the offset of amplifier 'A'

under all conditions and all the requirements are verified.

One of the 12 main devices is shown in the figure 3.18 with 5 switches. All the switches are realized using PMOS transistors. Sg and Sg1 controls the gate connection of Mc1. Sg and Sg1 are complementary to each other. When Sg is ON (closed) the gate of Mc1 is connected to the 'cal gate' (gate of the standard transistor Ms in figure 3.4) otherwise it will be connected to the 'main mirror gate' (refer to figure 3.5). A break before make logic is used to generate these two control signals ensuring that Mc1 is connected either in the calibration circuit (figure 3.4) or in the main mirror circuit (figure 3.5). The break before make logic generates a non-overlapping clock.

Sc, So and Si are used to control the drain terminal of Mc. Sg and Sc are the same signals. This means that, when the gate of Mc1 is connected to the gate of Ms, its drain

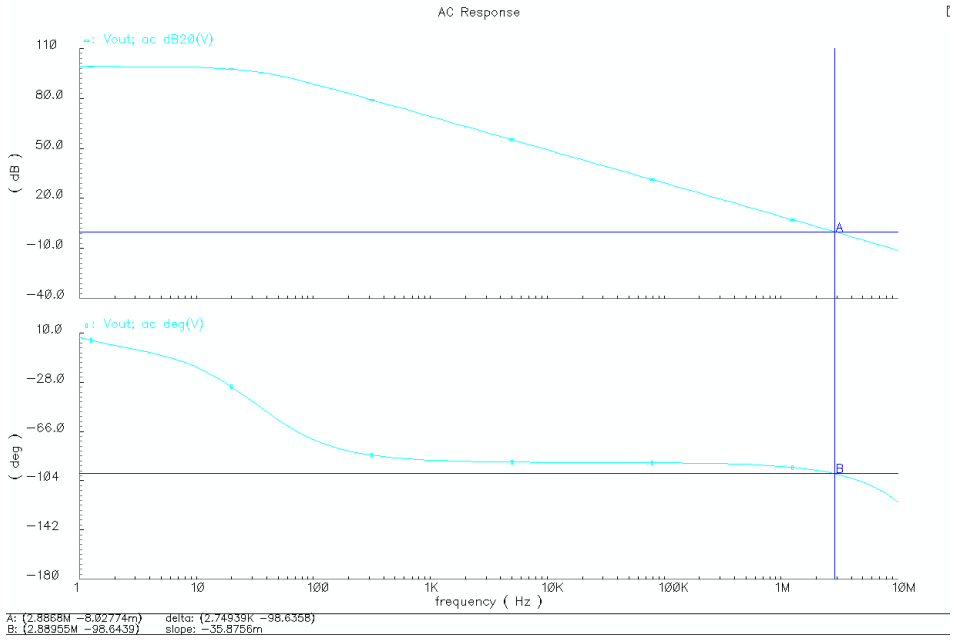


FIGURE 3.16: Frequency response of the amplifier 'A' in open loop configuration

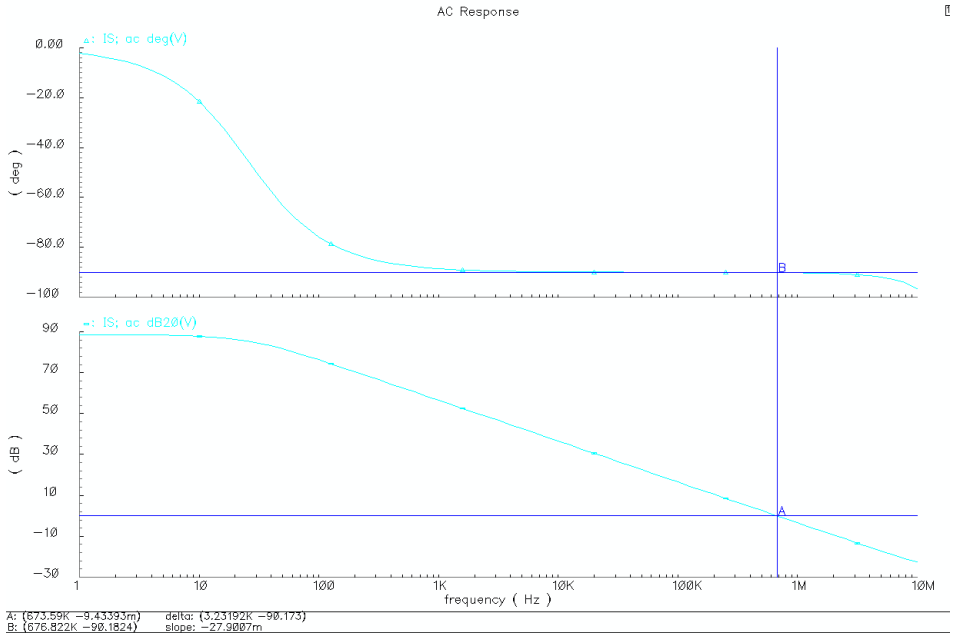


FIGURE 3.17: Frequency response of the amplifier 'A' when loaded with M_{ext} at 100μA of output current

terminal is connected with the source terminal of M2 (figure 3.4). If Si is ON (closed) then Mc1 is connected as an input leg and if So is ON (closed) then Mc1 is connected as one of the output legs in the main mirror circuit. Both of them (Si and So) cannot be ON at the same time. A break before make logic is used in generating 3 switching signals i:e Sc, So and Si. The logic behind is that the drain of Mc1 should be connected either

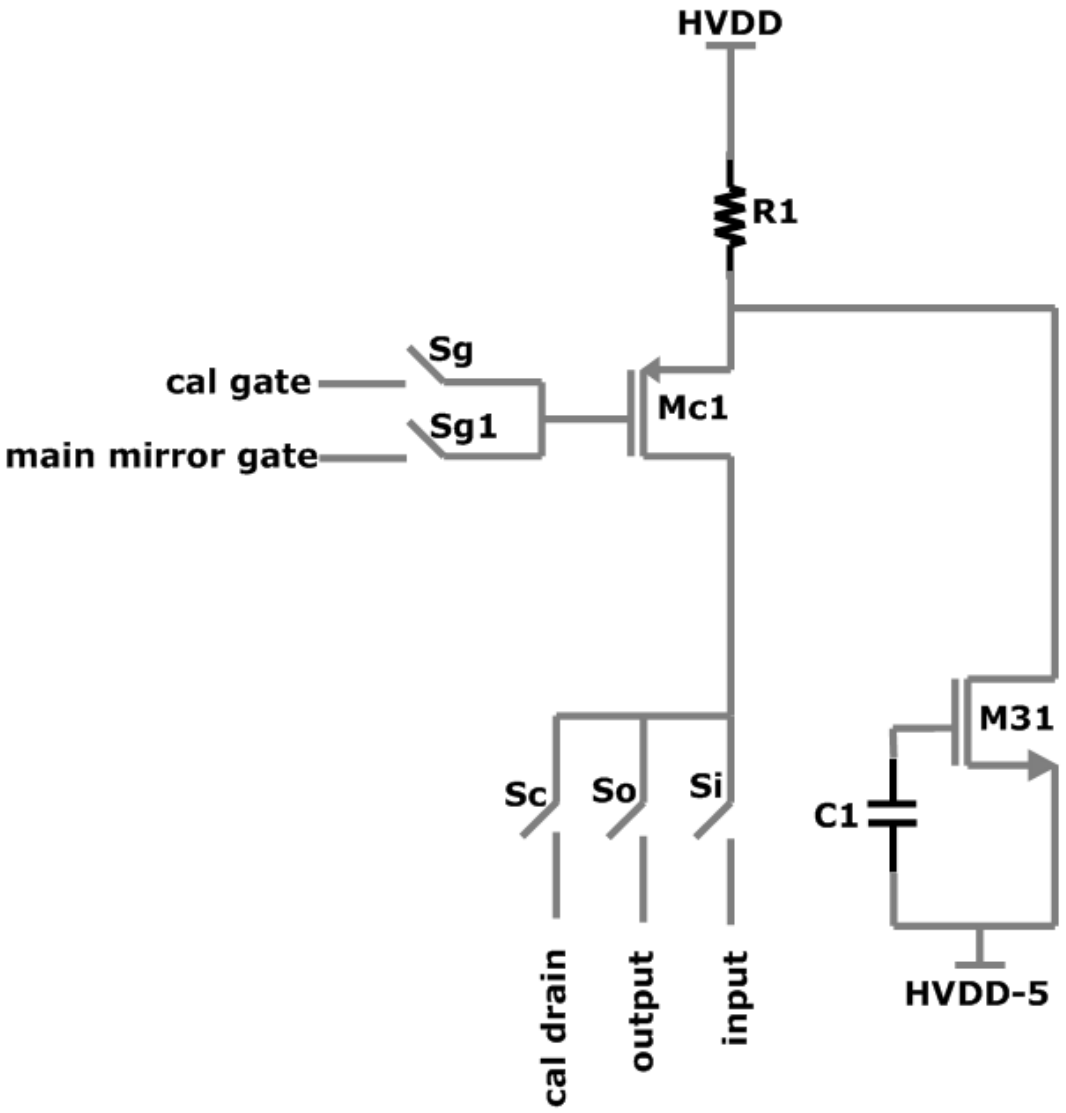


FIGURE 3.18: A single mirror device with switches

as an input, output or calibration leg. The simulation result is shown in the figure 3.19. In the figure 3.19 all the 5 control signals are shown clearly. A simulation is performed at a supply voltage (HVDD) of 30V. From 44μs-48μs Mc1 is getting calibrated. Just after the calibration gets over, Mc1 is connected as an input leg of the main current mirror from 48μs-52μs. Moreover, the gate of Mc1 is disconnected from the calibration circuit and is connected to the main mirror circuit. After 52μs Mc1 is connected as one of the output legs in the main mirror circuit.

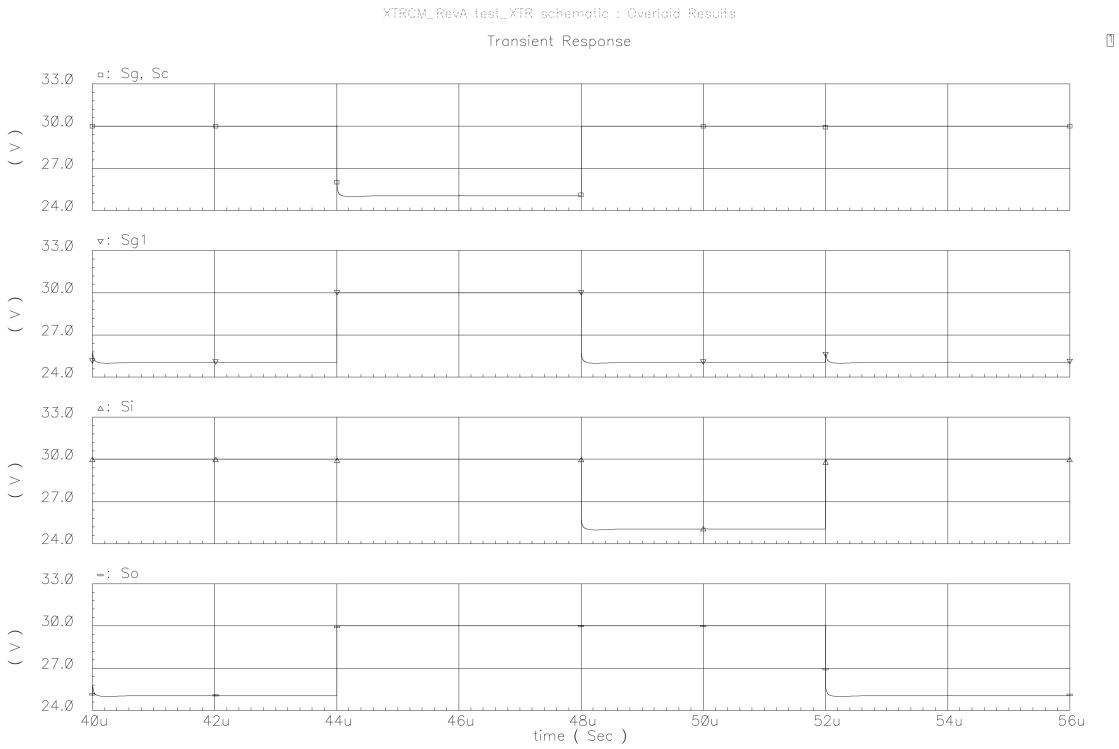


FIGURE 3.19: Timing diagram of all the 5 switches

3.5.5 Output protection clamp circuitry

Referring to the figure 1.6, XTR111 [4] does not provide internal current limit for the case when the drain of the external PMOS transistor is shorted to ground. This will be further explained in the following paragraph and finally an on-chip solution will be proposed to overcome this problem.

Initially, the switch Sout in ON (closed) as shown in the figure 3.20. The circuit does not provide internal current limit for the case when the drain of the external PMOS transistor is shorted to ground (Rout is shorted). The internal current source controls the current, but a high current from IS to HVSS forces an internal voltage clamp (esd diode D) between IS and HVDD-5 to turn on. This results in a low resistance path and the output current is limited by the load impedance and the current driving capability of the external MOS device. Large current can destroy the IC. This is explained further.

Suppose, if the load resistance disconnected (Sout is open), then external MOS (Mext) is fully turned ON with large source-gate voltage stored on the parasitic source-gate capacitance. As soon as the load is connected (Sout in closed) the current flows into

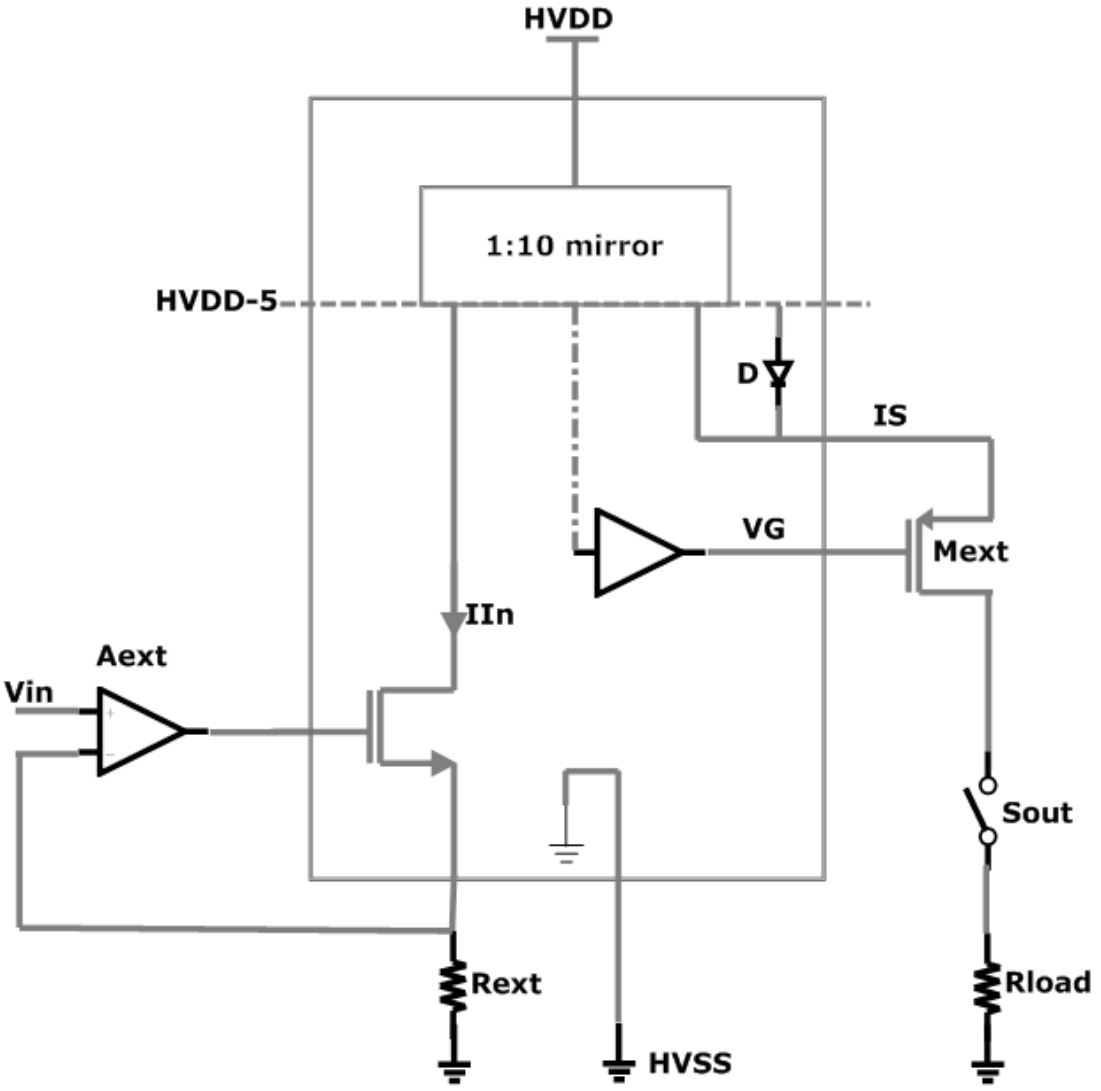


FIGURE 3.20: Top level diagram for the current mirror circuit

the load, but for the first few microseconds the Mext is still turned ON and destructive current can flow, which can damage the IC. After first few microseconds Mext will start regulating the voltage of IS, thus bringing the circuit back in a normal operating mode. Hence, an on-chip clamp was designed to overcome these problems. Firstly, VG should be clamped to a certain voltage below HVDD. Secondly, IS should be clamped to protect this node from going more than 5V below VSP.

Figure 3.21 is the clamp circuit for limiting the voltage at node VG (gate drive for Mext). 10μA of current is dropped over 1.2MΩ of resistance, resulting in a gate voltage (device M_{12}) of 12V below HVDD. If the threshold voltage of M_{12} is $V_{T,M_{12}}$, then VG is clamped to a voltage $V_{T,M_{12}}$ below the gate voltage of M_{12}. The figure 3.22 shows the clamp circuit for IS. This circuit prevents IS from going below 5V from HVDD. V_{b1}

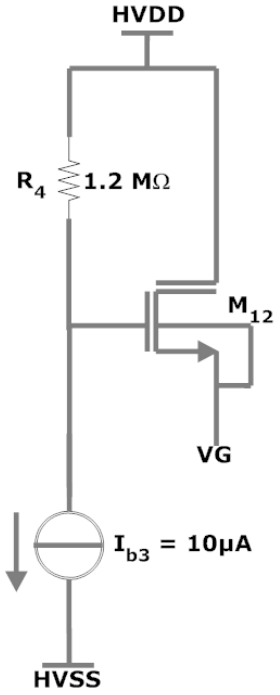


FIGURE 3.21: Clamp for VG

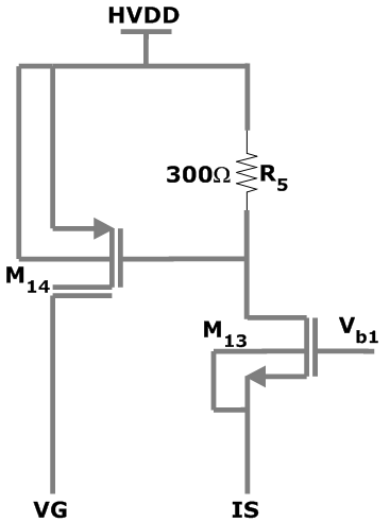


FIGURE 3.22: Clamp for IS

is the gate bias voltage of M_{13}, which is generated from the sub-regulator (figure 3.13). V_{b1} is set to one threshold voltage (of M_{13}) above HVDD-5 Volts. This means that IS can never go below 5V from the positive rail. M_{13} will turn ON if IS will go 5V below HVDD. The current flowing through this branch will flow through R_5. The voltage drop at the gate of M_{14}, will turn ON this device and VG will be pulled up, thus shorting the source and gate terminals for the external MOS device. This clamp puts a

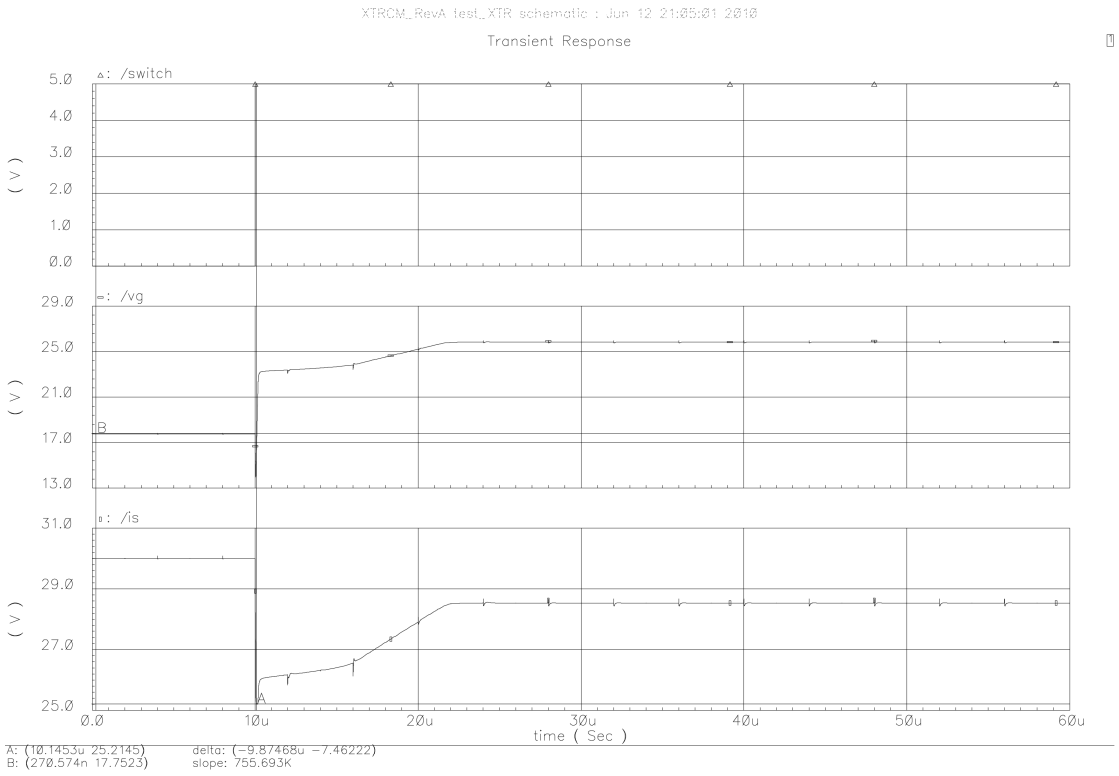


FIGURE 3.23: Simulation result of clamp circuit used for protecting IS and VG at VSP=30V

restriction on the external current which can flow from the chip, hence protecting the IC.

The simulation result presented in figure 3.23 is at a supply voltage of 30V and the full scale input current of 2.5mA. Initially, the load is disconnected when the circuit is powered up, which is visible from the switch signal shown in the figure 3.23. When the switch signal (Sout) is 0V, the load is disconnected and when the switch signal is 5V, the load is connected again. Initially, VG is clamped (approximately) 12V below the positive supply (30V in this case). As soon as the load is connected there will be a huge current (25mA) flowing through the external MOS device and voltage at IS will drop suddenly. For the first few microseconds the voltage at IS will try to go below 5V from positive rail, which is avoided by adding a clamp. It can be seen from the figure 3.23 that the voltage at IS is clamped to 25.21V, thus protecting the chip from excessive current flow.

3.6 Layout Details

A good analog layout plays a vital role in extracting the maximum performance from an analog circuit. To improve the precision of the DEM current mirror, the simplest way is to make a better layout. Common-centroid [12] and interdigitation [12] pattern should be used for lay outing a critically matched blocks. Lay outing in this way can also help in reducing the temperature gradient and other effects on the chip, which can deteriorate the performance of an analog circuit.

3.6.1 Circuit Layout

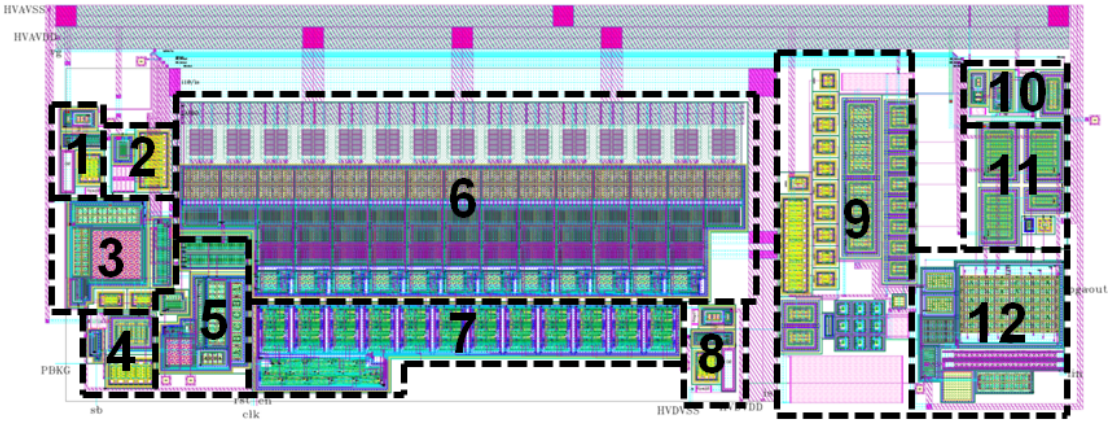


FIGURE 3.24: Chip layout without pad ring

Figure 3.24 shows the chip layout without pad ring. The different functional blocks in the layout are represented by the black dotted box surrounding it. Each box has a unique number from 1 to 12 corresponding to a unique functionality in the circuit, which is listed below:

a) **1** - Analog sub-regulator giving 5V down from positive rail.

b) **2** - Clamp for limiting the output current.

c) **3** - Amplifier for providing an external gate drive for the high power PMOS device and regulating the drain-source of the mirror devices.

d) **4** - Slew boost circuit for an external gate drive amplifier.

e) **5** - Calibration circuit.

f) **6** - Main mirror circuit with standard leg.

g) **7** - Break before make and shift register.

h) **8** - Digital sub-regulator giving 5V down from positive rail.

i) **9** - Biasing core.

j) **10** - Analog sub-regulator giving 5V up from negative rail.

k) **11** - Drain extended cascode device for input signal translation from the lower to the higher voltage domain.

l) **12** - Circuit for generating input, trim and adaptive bias currents.

The figure 3.25 shows the complete chip layout. The total chip area (without pad ring) is 1.4mm x 0.6mm.

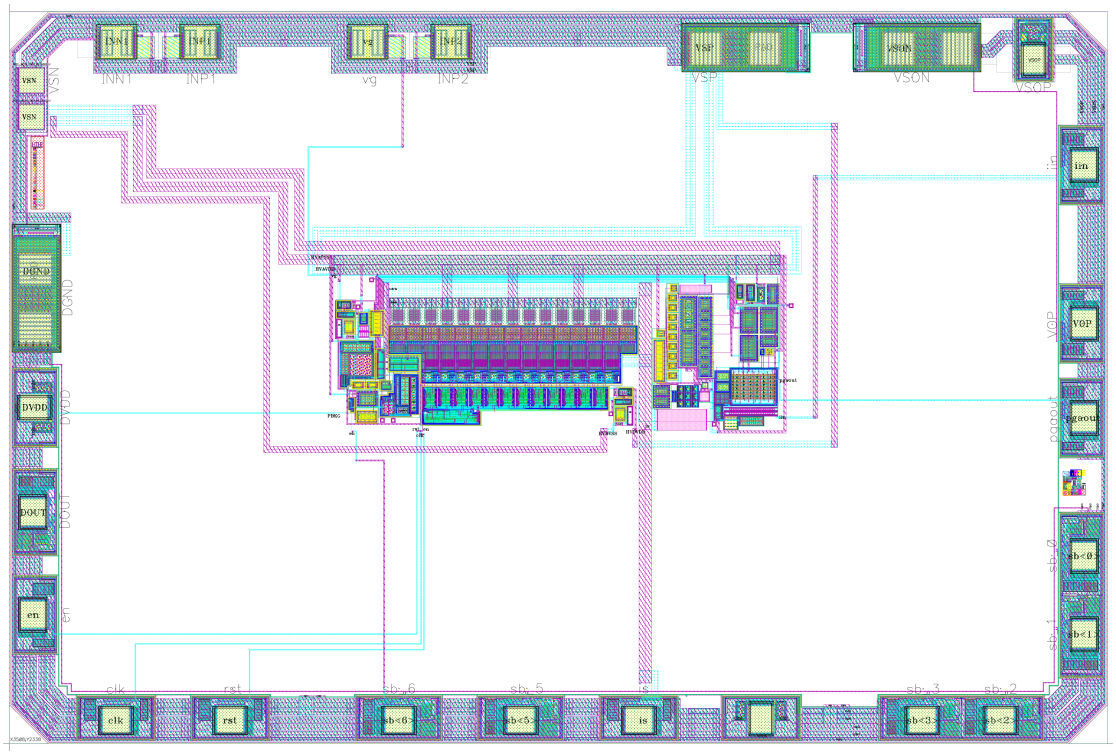


FIGURE 3.25: Layout of the complete chip

Chapter 4

Simulation and Measurement Results

4.1 Introduction

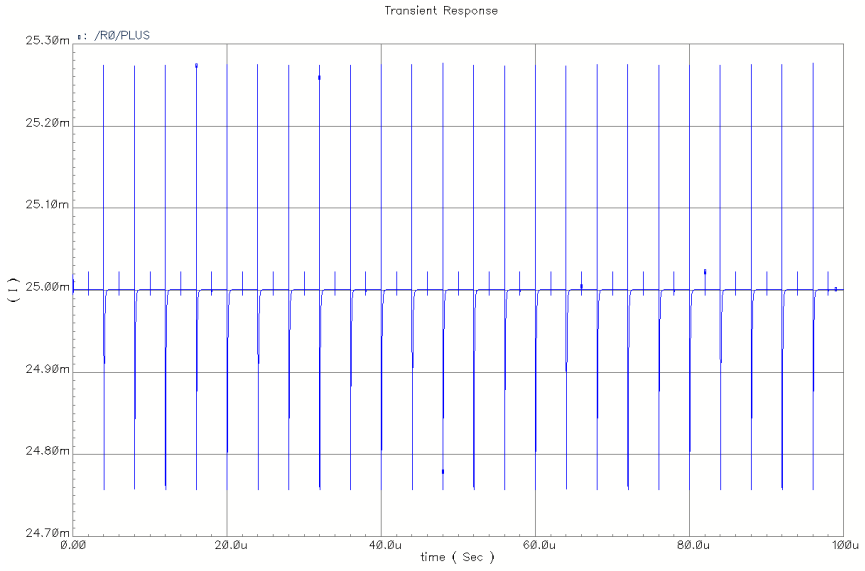
This chapter will present the simulation results which were performed on the DEM current mirror. After this the measurements on the silicon will be presented. Finally, the chip micrograph will be shown.

4.2 Simulation Results

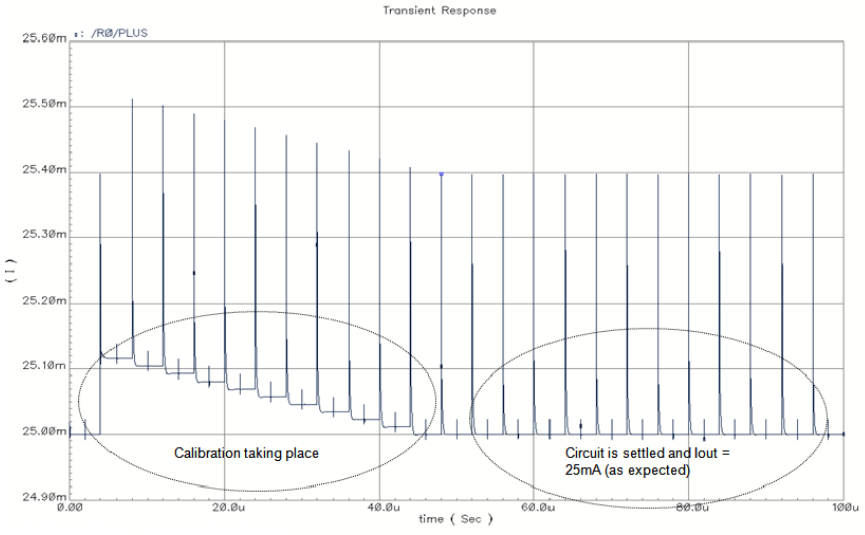
In this section the simulation results will be presented that were performed on the DEM current mirror using Cadence. The IC process in which the design is implemented is a high voltage process (50HPA07HV) from Texas Instruments (TI). Initially, the typical simulation results at the room temperature will be presented without any mismatch in the DEM mirror devices. After this, monte-carlo simulations will be shown for two cases (a) only DEM and (b) calibration and DEM. The monte-carlo simulation results will be followed by simulation results over process/corners and temperature variations. After this the step response simulation followed by the sinusoidal response will be shown. Finally PSRR, periodic steady state (PSS) and noise simulation will be presented for the 3 cases (a) without calibration and DEM, (b) without calibration and with DEM and (c) with calibration and DEM.

4.2.1 Typical performance

The figure 4.1 shows the typical simulation result at the room temperature (27°C). The input current flowing into the circuit is 2.5mA and the supply voltage is 30V. The output current flowing though an external FET (Mext) is dropped over a resistance (Rload) of 500Ω as shown in the figure 3.20. From the figure 4.1(a) it is visible that the output



(a) DEM only

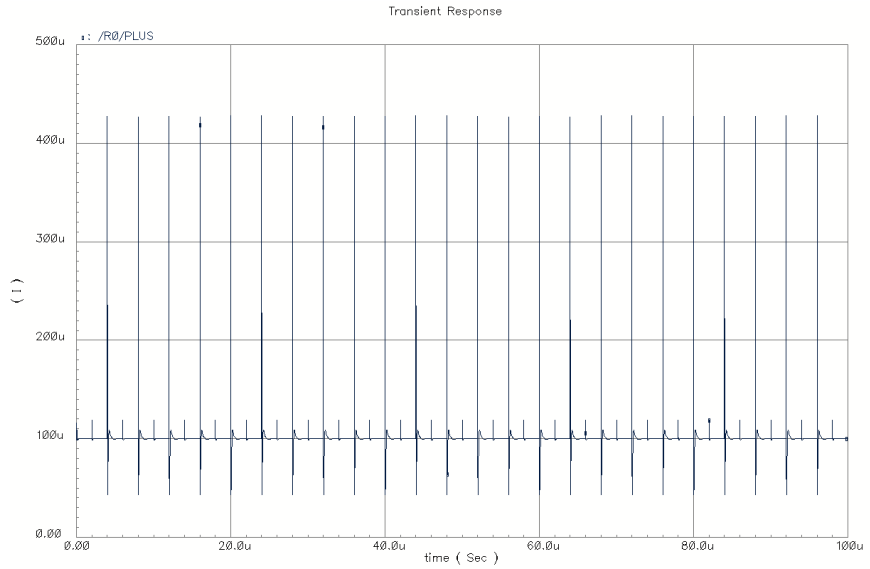


(b) Calibration and DEM

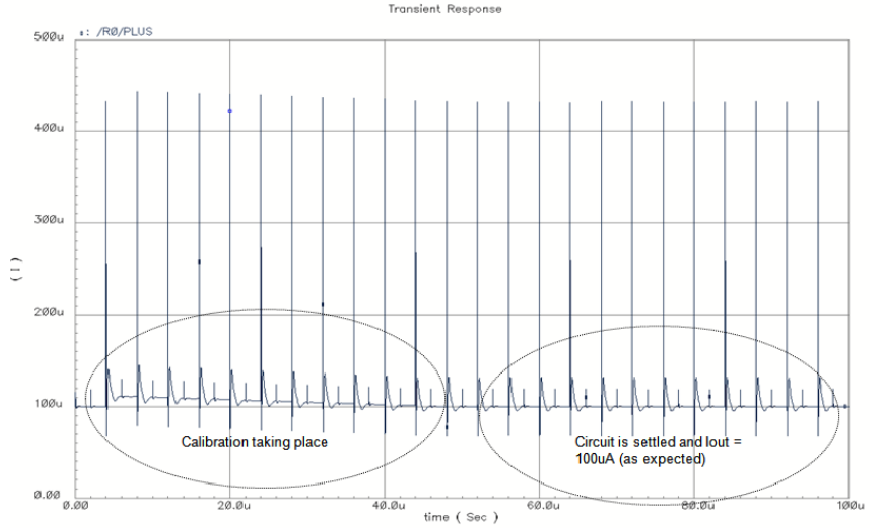
FIGURE 4.1: Output current from the mirror for 2.5mA of the input current

current from the mirror is free from DEM ripple. This result is obvious because there is no mismatch among the current mirror devices. The output current is 25mA as expected

(10X gain).



(a) DEM only



(b) Calibration and DEM

FIGURE 4.2: Output current from the mirror for 10μA of the input current

When calibration is applied along with DEM, the output current from the mirror is shown in the figure 4.1(b). It is visible from the figure that all the 12 mirror devices are getting calibrated. Since the clock frequency is 250kHz, therefore all the 12 devices will be calibrated by the end of 48μs. Once all the mirror devices are calibrated, the current mirror output is settled to 25mA. Although there is no mismatch among the

current mirror devices, still the initial calibration up to 48μs is taking place because of the systematic mismatch added in the standard leg (refer figure 3.4).

For an input current of 10μA (keeping all the other conditions same as in the previous simulation (Figure 4.1)) the output current from the mirror is shown in the figure 4.2. The output current is 100μA (as expected).

4.2.2 Monte-Carlo simulations

Figure 4.3 shows the result of a monte-carlo run (worst case result from 100 runs) of simulated mirror output at room temperature (27°C) for (a) DEM only and (b) calibration and DEM. The input current flowing through the mirror is 2.5mA. The DEM ripple at the output of the mirror is visible in figure 4.3(a), when no calibration is taking place. When the calibration is switched on, the DEM ripple is suppressed (figure 4.3(b)). The magnitude of the DEM ripple is 75μA, which is suppressed to 1μA by the calibrating the mirror devices. A current of 75μA generates a peak-to-peak voltage ripple of 37.5mV (or V_{rms} = 13.26mV) when passed through 500Ω of resistance.

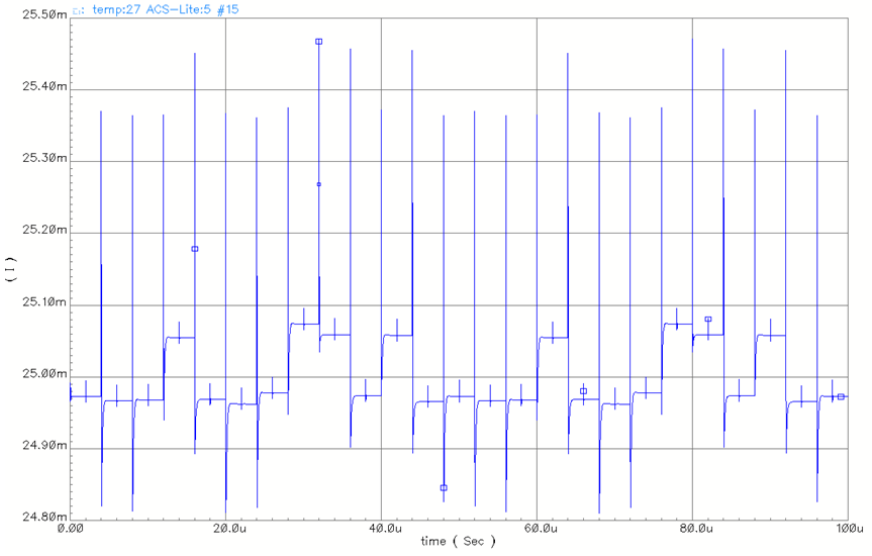
TABLE 4.1: Results of the DEM output ripple from the monte-carlo simulation for an input current of 2.5mA over temperature

Temperature (°C)	Ripple (μA) (DEM only)	Ripple (μA) (calibration and DEM)
-55	91	<1
27	75	<1
150	64	<1

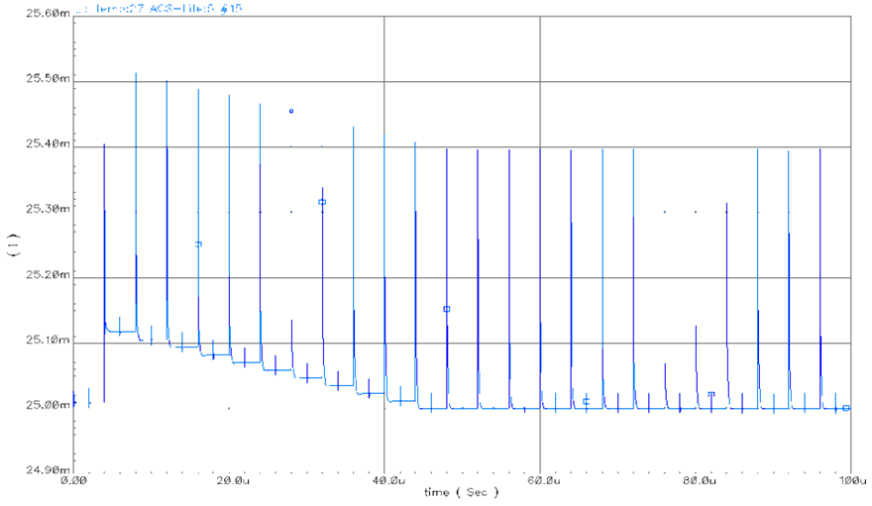
Monte-carlo simulations are also performed at the different temperature for the same input current of 2.5mA. The values obtained from simulation results are listed in the table 4.1.

Figure 4.4 shows the output current from the mirror for an input current of 10μA at 27°C (worst case result from 100 MC runs). The DEM ripple at the output is 11.2μA without calibration. A current of 11.2μA generates a peak-to-peak voltage ripple of 5.6mV (or V_{rms} = 1.98mV) when passed through 500Ω of resistance. The monte-carlo simulations are also performed at different temperature for an input current of 10μA. The results are listed in the table 4.2.

Figure 4.5 shows the DC residual error in the mirror output current over monte-carlo and temperature. The input current is 2.5mA. X-axis is the input current (in mA) and Y-axis is the residual error (in μA) in the DC output current. The DC residual error is



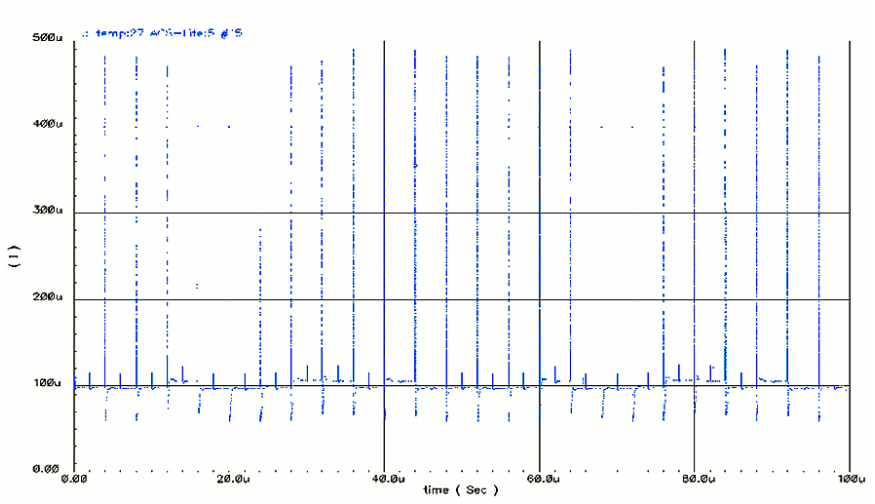
(a) DEM only



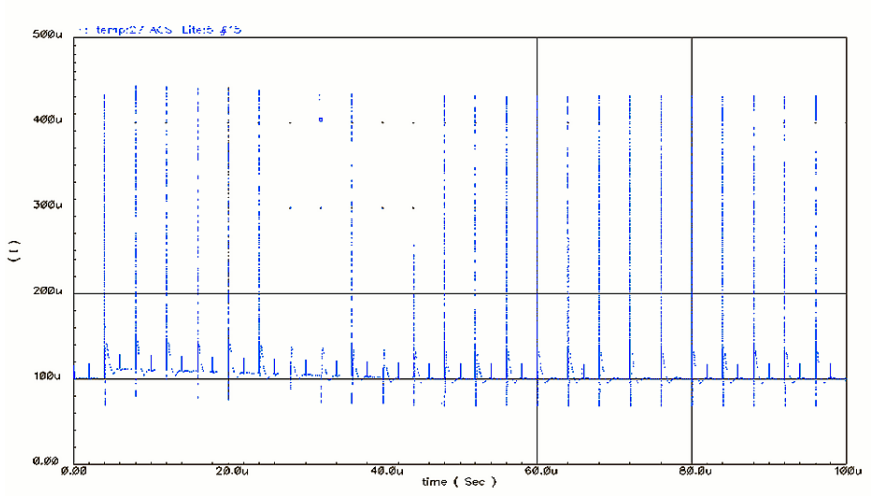
(b) Calibration and DEM

FIGURE 4.3: Output current from the mirror for 2.5mA of the input current at 27°C

calculated by taking the average of the output current over 10 complete cycles (440μs) and then subtracting it from the 10 times of the input current (25mA). The maximum DC residual error is 11.18μA for a full scale output current of 25mA. This error is equal to 447ppm or 0.0447%.



(a) DEM only



(b) Calibration and DEM

FIGURE 4.4: Output current from the mirror for 10μA of the input current at 27°C

4.2.3 Simulation over Process/Corners

The DC residual error in the output current from the mirror over corners and temperature is shown in figure 4.6. The input current is 2.5mA. The X-axis is the corner number and the Y-axis is the DC residual error (in μA). The maximum DC residual error is at the 3rd corner which is marked by the circle shown in the figure 4.6. The maximum DC residual error is 9.28μA for a full scale output current of 25mA. This means 371ppm or 0.0371% DC residual error.

TABLE 4.2: Results of the DEM output ripple from the monte-carlo simulation for an input current of 10μA over temperature

Temperature (°C)	Ripple (μA) (DEM only)	Ripple (μA) (calibration and DEM)
-55	11.7	<1
27	11.2	<1
150	17.5	<1

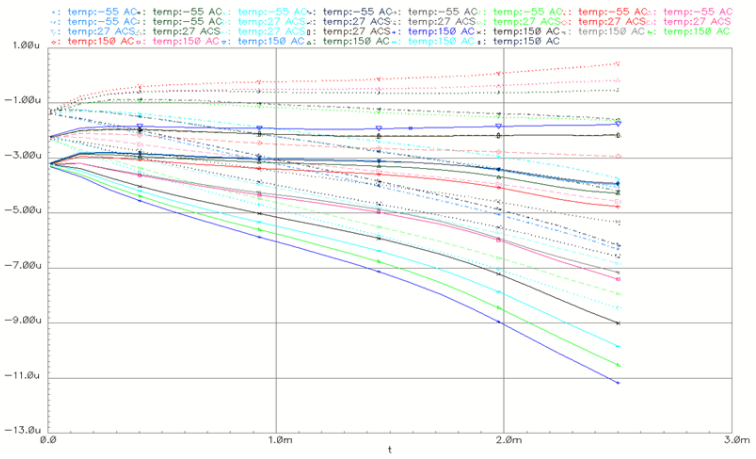


FIGURE 4.5: DC residual error in the output current of the mirror for an input current of 2.5mA over monte-carlo and temperature (-55°C - 150°C)

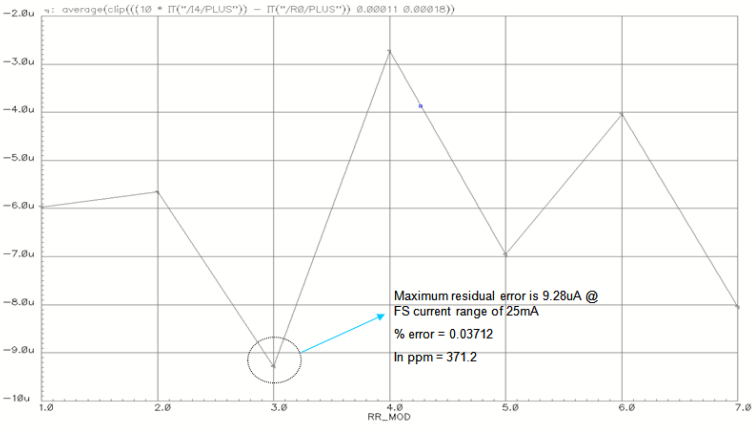


FIGURE 4.6: DC residual error in the output current of the mirror for an input current of 2.5mA over corners and temperature (-55°C - 150°C)

4.2.4 Step Response

The step response of the DEM current mirror is shown in the figure 4.7. The X-axis is the time (in μs) and the Y-axis is the current (in mA). The plot at the bottom is the step input current to the mirror, which is from 10μA - 2.5mA. The plot at the top is

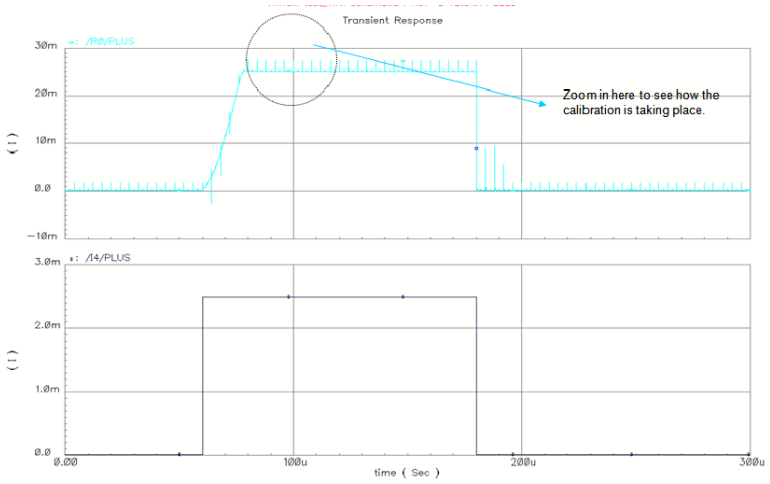


FIGURE 4.7: Step response at 27°C

the output current from the mirror, which is from 100μA - 25mA. The rise time is 17μs, which depends on the source-gate capacitance of external FET Mext (figure 3.20). The region surrounded by the circle (shown in the figure 4.7) should be zoomed in to see how the calibration of the devices is taking place. This is shown in the figure 4.8.

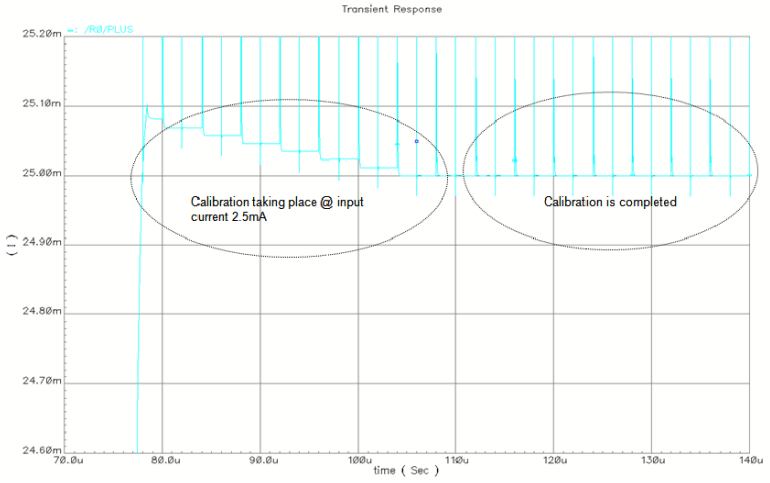


FIGURE 4.8: Zoomed in step response at 27°C

The figure 4.9 shows the step response of the DEM current mirror over corners and temperature (-55°C - 150°C). The worst case rise time is 35.4μs for the corner with a high source-gate capacitance and high temperature.

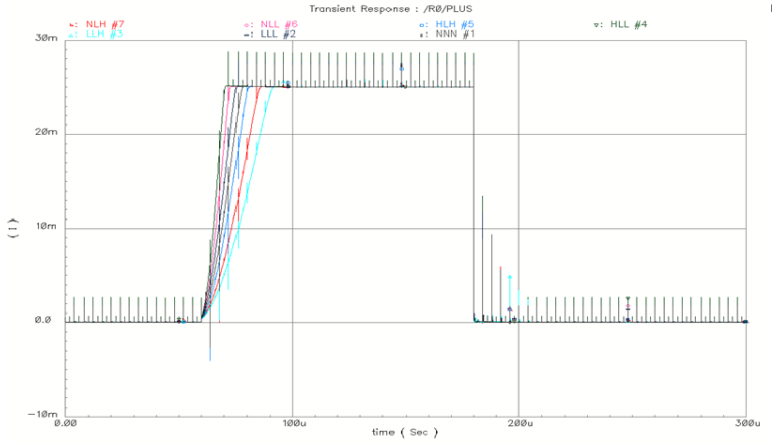


FIGURE 4.9: Step response of the DEM current mirror over corners and temperature (-55°C - 150°C)

4.2.5 Sinusoidal Response

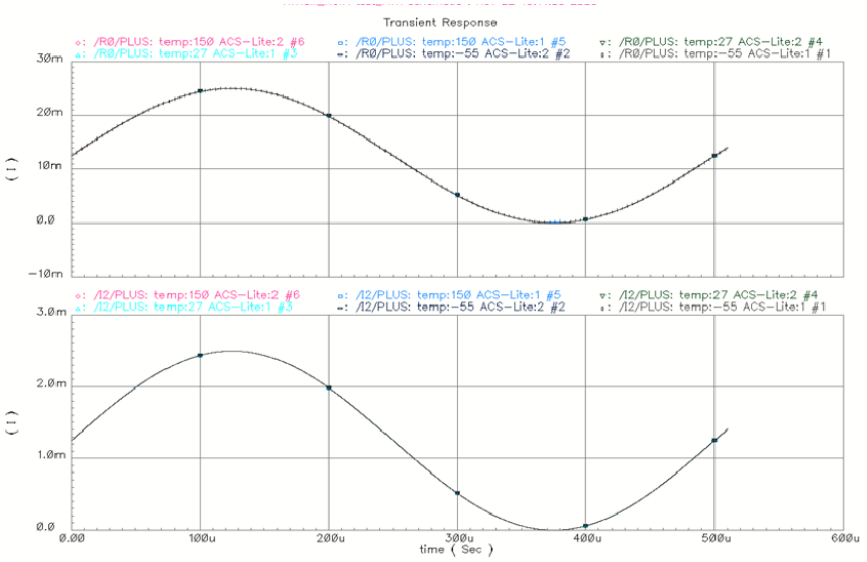
The figure 4.10(a) shows the output response of the DEM current mirror for a sinusoidal input current from 10μA - 2.5mA having a frequency of 2kHz. The output of the DEM current mirror is nicely tracking the input current. The error in the sinusoidal output current from the mirror is shown in the figure 4.10(b).

4.2.6 PSRR simulations

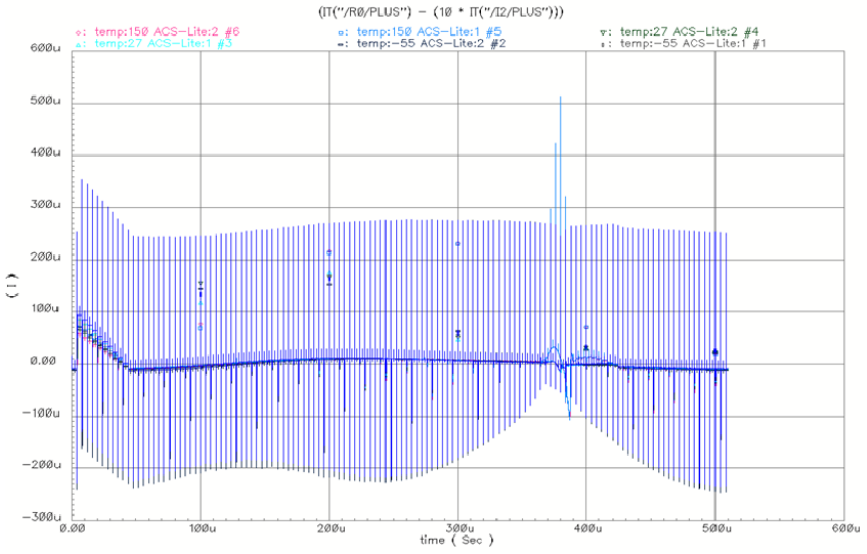
Figure 4.11(a) shows the output current from the current mirror for a varying triangular supply. The supply is varying from 29.5V to 30V at a frequency of 20kHz. It can be seen from the figure 4.11(b) (zoomed inside the circle shown in figure 4.11(a)) that the calibration is not perfect. This is due to the single-ended sample and hold circuit (refer figure 3.4) used during the implementation of the calibration circuit. The maximum error in the output current is $\pm 5\mu$A at a full current of 25mA. This error is equal to 0.04%, which is still near the target specifications that was decided for the current mirror. This problem can be fixed by using differential sampling, designing a sub-regulator having a better PSRR, etc.

4.2.7 Noise and PSS simulations

Classical noise simulations don't work in switched/sampled circuit because circuit cannot be linearized into one operating point. The only exception is the simulation without DEM. Therefore, periodic steady state (PSS) analysis should be used for switched/sampled circuits. Since this is a complicated procedure, they were unfortunately done only



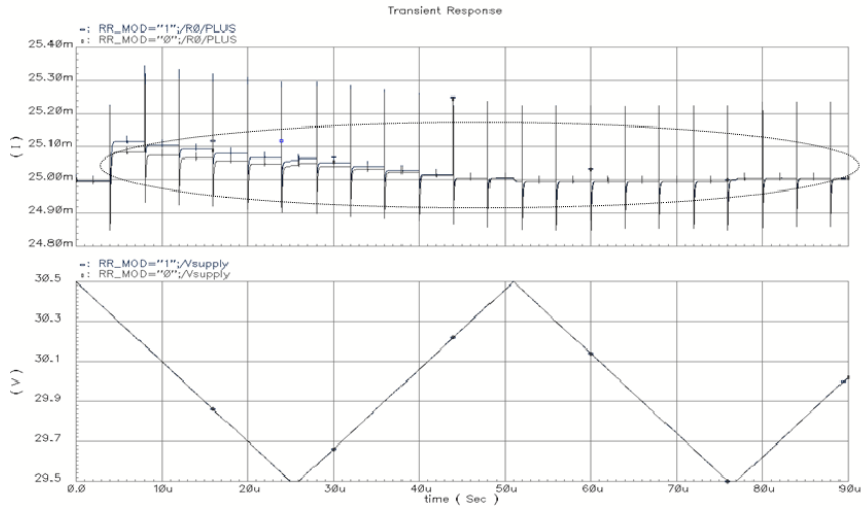
(a) Output response of the DEM current mirror for a sinusoidal input current from 10μA - 2.5mA having a frequency of 2kHz



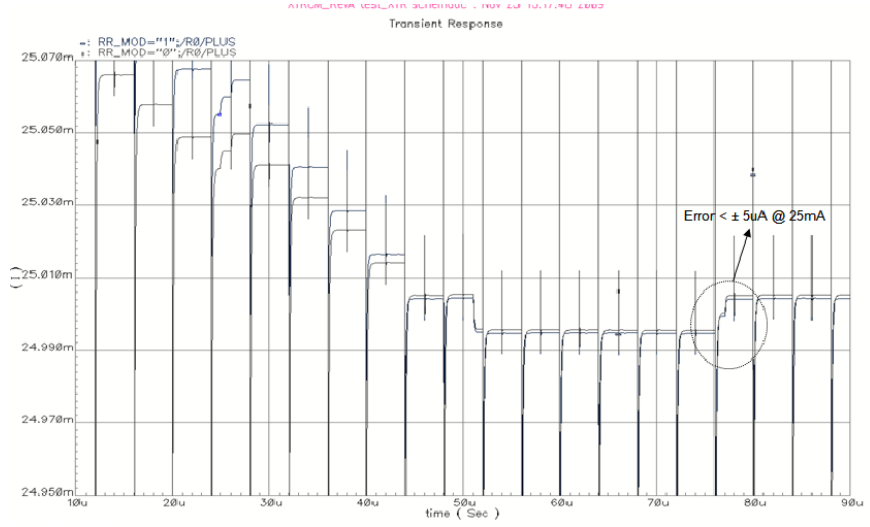
(b) Residual error in the sinusoidal output current

FIGURE 4.10: Output response of the DEM current mirror over monte-carlo and temperature (-55°C - 150°C)

after tapeout. The figure 4.12 shows the simulation of the current mirror for (a) Without DEM, (b) Only DEM and (c) calibration + DEM. When the DEM was not enabled, it is visible from the figure that $1/f$ noise at 100mHz is $15\mu V/\sqrt{Hz}$ and the noise floor is $170nV/\sqrt{Hz}$. When the DEM is switched on, $1/f$ noise at 100mHz is decreased to $3\mu V/\sqrt{Hz}$ and the noise floor stayed constant. Simulation shows that while $1/f$ noise has decreased, it does not disappear completely as theory would predict. The residual



(a) Response to a 20kHz triangular supply ripple varying from 29.5V - 30V



(b) Zoomed in plot of the output current from the DEM current mirror

FIGURE 4.11: PSRR simulation for the input current of 2.5mA over monte-carlo runs

$1/f$ noise (after DEM) from 0.1Hz-10Hz is coming from M_9 and M_{10} (refer to figure 3.7) that is the main contributor. This is obvious because the DEM operation was not performed on the bottom block (refer to figure 3.7). The sampling technique used in the proposed concept has the tendency of increasing the noise floor because of the noise folding. It can be seen from the figure 4.12, when DEM is followed by calibration, the $1/f$ noise at 100mHz remains constant ($3\mu V/\sqrt{Hz}$) but the noise floor has increased to $550nV/\sqrt{Hz}$ at 14KHz, which is undesirable. The main contributor of $1/f$ noise from 0.1Hz-10Hz is M_9 and M_{10} (refer figure 3.7). The excess noise floor seen at 14KHz is coming from three dominant sources:

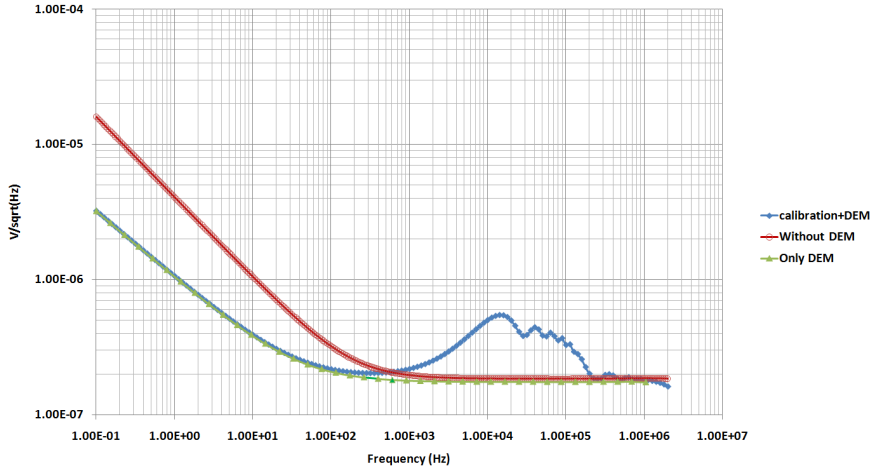


FIGURE 4.12: Noise simulations

1) The noise from the 12 switches Sg (see figure 3.18), which are responsible for connecting the current legs with the calibration circuit (see figure 3.4), are the main contributors. The total noise contributed by 12 switches is nearly equal to 60%.

2) The up-modulation of $1/f$ noise of M_2 and M_3 (refer to figure 3.7) also increases the noise floor by 20%.

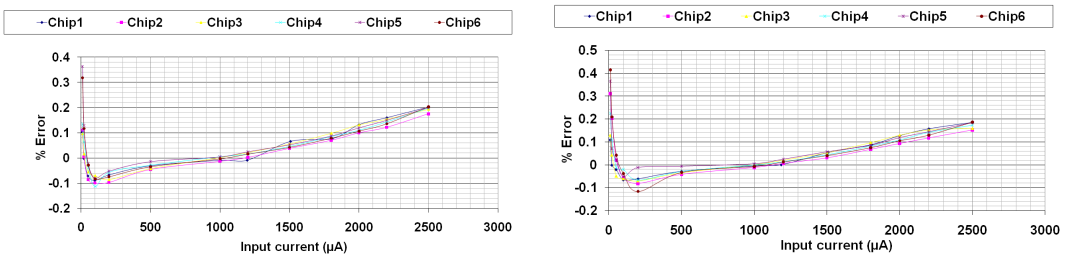
3) The noise floor of the 11 devices (among 12), that are connected in the main mirror circuit (refer to figure 3.5).

The noise contributed by 12 switches Sg1-12 (i:e 60%) is the dominant. These 12 switches Sg (see figure 3.18) were designed to be the minimum size to reduce the charge injection. This was not expected, that the noise from these switches will increase the noise floor of the circuit. In the next version of the new current mirror, the problem of the excess noise can be fixed by increasing the size of these 12 switches.

4.3 Measurement Results

This section will present the measurement results obtained from silicon. The measurements were performed on 6 chips. The supply voltage at which the measurements were performed is 30V.

4.3.1 DC accuracy



(a) DEM only

(b) Calibration and DEM

FIGURE 4.13: DC accuracy of 6 chips

Figure 4.13 shows the error in the output current from the mirror (a) DEM only and (b) Calibration and DEM. The DC error in the output current (OC) is calculated by using the formula given in the equation (4.1)

$$DCError(OC) = \frac{ActualOutputCurrent - 10 * InputCurrent}{10 * InputCurrent} * 100\% \tag{4.1}$$

The error definition given in equation (4.1) is different from the error definition of % full scale (FS), which is given in the equation (4.2)

$$DCErrorFS(OC) = \frac{ActualOutputCurrent - 10 * InputCurrent}{25mA} * 100\% \tag{4.2}$$

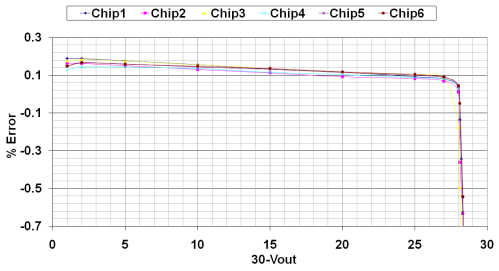
The maximum DC error is at the full scale input current of 2.5mA, which is visible in figure 4.13. Table 4.3 list the maximum DC error (in %) in the output current (for all the 6 chips) at a full scale input current of 2.5mA.

TABLE 4.3: Maximum DC error (in %) in the mirror output current for an input current of 2.5mA

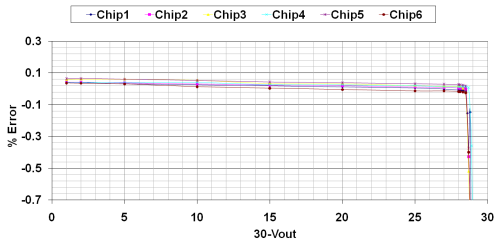
Chip no.	Max DC error(%) (DEM only)	Max DC error(%A) (calibration and DEM)
1	0.2	0.18
2	0.17	0.15
3	0.19	0.15
4	0.19	0.17
5	0.2	0.19
6	0.2	0.18

From the values shown in the table 4.3, it can be concluded that the calibration does not lead to worse DC performance.

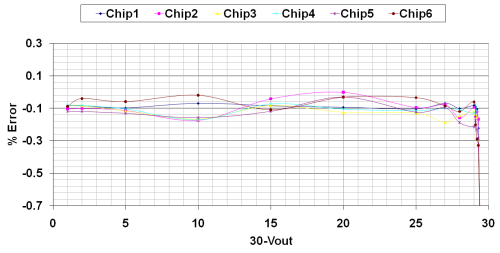
4.3.2 Output DC Error Vs Output voltage



(a) Input current of 2.5mA



(b) Input current of 1.5mA



(c) Input current of 100μA

FIGURE 4.14: DC Error in the output current for all 6 chips Vs Output voltage

The figure 4.14 shows the error in the output DC current with varying output voltage for different input currents. The output voltage (in V) is plotted along the X-axis. It can be seen from figure 4.14 that the compliance voltage required for the mirror is less, when the input current is lower. This makes sense because the required voltage drop across the mirror devices will be higher when the output current is 25mA compared to an output current of 15mA. For the minimum DC accuracy of 0.1% in the output current, the minimum compliance voltage needed across the mirror devices is listed in the table 4.4.

It can be seen from the table 4.4 that minimum compliance voltage across the mirror is 0.9V, 1.6V and 2V for an input current of 100μA, 1.5mA and 2.5mA respectively (worst case data from all the 6 chips).

TABLE 4.4: Compliance voltage (CV) across the mirror devices for a minimum accuracy of 0.1% in the output current for different input current (ic)

Chip no.	CV(100μA of ic)(V)	CV(1.5mA of ic)(V)	CV(2.5mA of ic)(V)
1	0.8	1.4	1.9
2	0.8	1.5	2
3	0.8	1.6	2
4	0.8	1.3	1.9
5	0.9	1.4	1.9
6	0.9	1.4	1.9

4.3.3 Supply current

The supply current of circuit increases with the input current. This can be seen in the figure 4.15, which plots the supply current(mA) vs the output current (mA) for all the 6 samples.

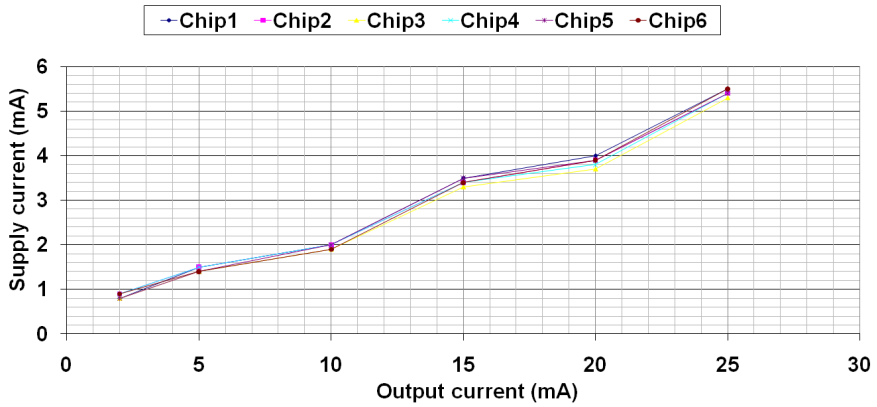
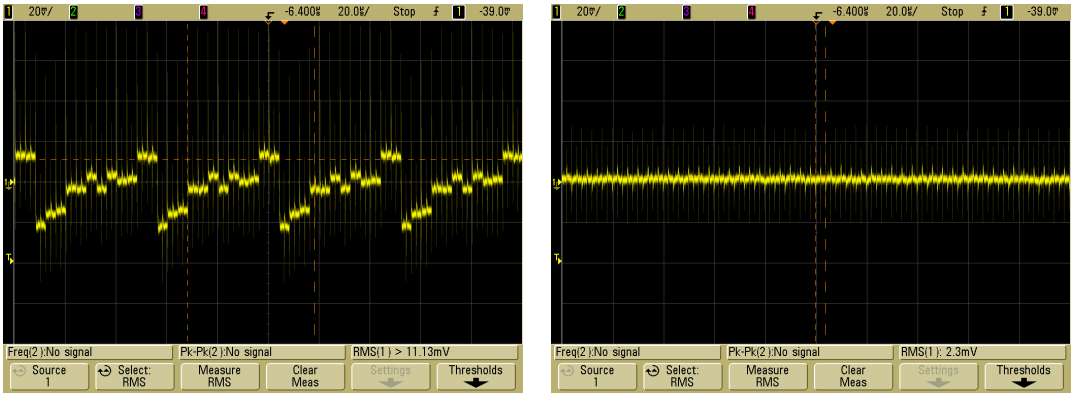


FIGURE 4.15: Supply current (mA) Vs the output current (mA)

4.3.4 AC ripple

The figure 4.16 shows the DEM ripple in the mirror output without calibration (a) and with calibration (b). The output current is passed through a resistance of 510Ω, resulting in a voltage ripple shown in the figure 4.16. The input current flowing through the mirror is 2.3mA. The result is shown only for 1 sample. It can be seen from the figure 4.16 that the root mean square voltage (V_{rms}) of the output ripple is 11.13mV in DEM only, which is suppressed to 2.3mV (limited by the scope resolution) when the

calibration is switched on. The measurement results on all the 6 samples are listed in the table 4.5. The difference in the V_{rms} value before and after calibration for chip1, chip2, chip4 and chip6 are limited by the scope resolution and is not very accurate. All these chips are working well. It is visible from the table that chip3 and chip5 are not working properly.



(a) DEM only

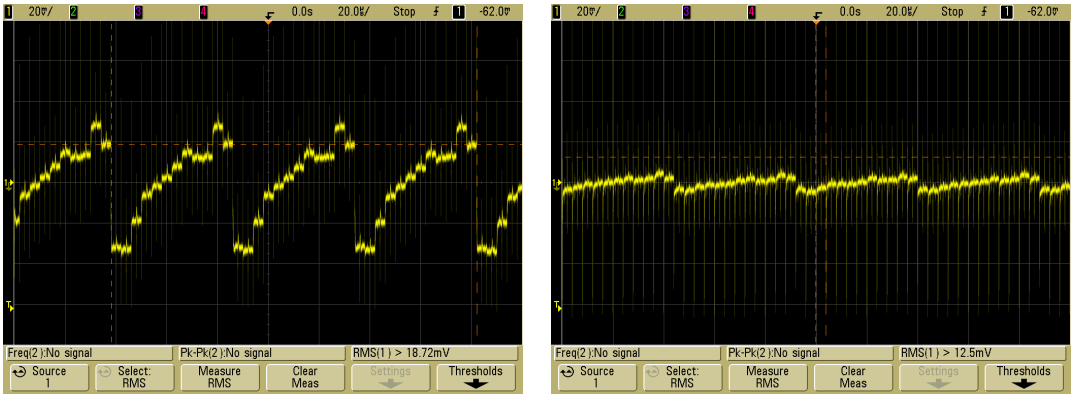
(b) Calibration and DEM

FIGURE 4.16: DEM ripple for an input current of 2.3mA (Sample 1)

TABLE 4.5: V_{rms}(mV) value of an AC voltage ripple for all the 6 samples

Chip no.	V_{rms}(mV) Ripple (DEM only)	V_{rms}(mV) Ripple (calibration and DEM)
1	11.13	2.3
2	16.77	4.4
3	18.72	12.5
4	10.94	4.2
5	14.99	6.5
6	17.67	4.2

The measurement result on the sample 3 is shown in the figure 4.17. It can be seen from the figure that the DEM ripple pattern is different from that of sample 1. This is obvious because different samples have different mismatch among its devices. After calibration the DEM ripple is still visible, the reason can be a limited trimming range or manufacturing defect.

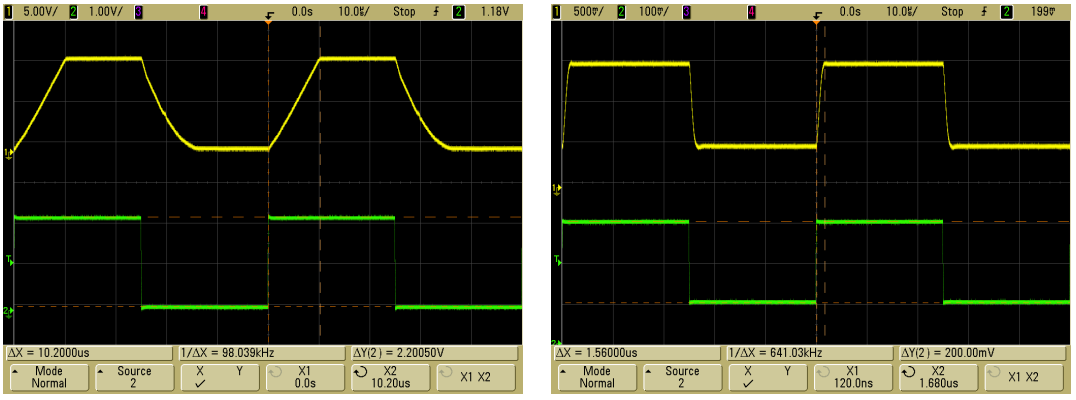


(a) DEM only (b) Calibration and DEM

FIGURE 4.17: DEM ripple for an input current of 2.3mA (Sample 3)

4.3.5 Step response

The figure 4.18 shows the large signal and small signal step response of one sample. In the figure 4.18(a) the step input is from 0.1V to 2.3V. This voltage step is dropped over a resistance of 1kΩ generating an input step current from 100μA - 2.3mA. The output current is passed through the resistance of 510Ω resulting in a output voltage shown in the figure 4.18(a) (yellow). The rise time is 10.2μs.



(a) Large signal (100μA - 2.3mA) (b) Small signal (100μA - 300μA)

FIGURE 4.18: Step response

In the figure 4.18(b) the step input is from 0.1V to 0.3V. This voltage is dropped over the resistance of 1kΩ generating an input step current from 100μA - 300μA. The output current is passed through the resistance of 510Ω resulting in an output voltage shown

in the figure 4.18(b) (yellow). The rise time is 1.56μs. The measurement results from other samples are listed in table 4.6.

TABLE 4.6: Rise time

Chip no.	Large signal (μs)	Small signal (μs)
1	10.2	1.56
2	10.2	1.8
3	10.2	1.4
4	10.2	1.8
5	10.2	1.8
6	10.2	1.8

The fall time depends on the slew rate of the amplifier 'A', output of which is acting as a gate drive for Mext (refer to figure 3.5)

4.3.6 Sinusoidal response

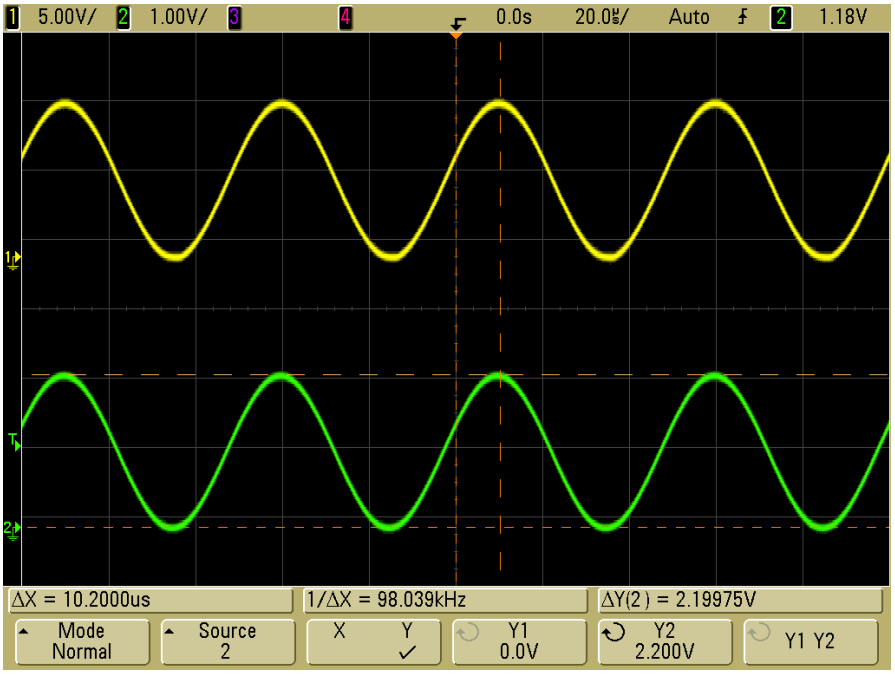
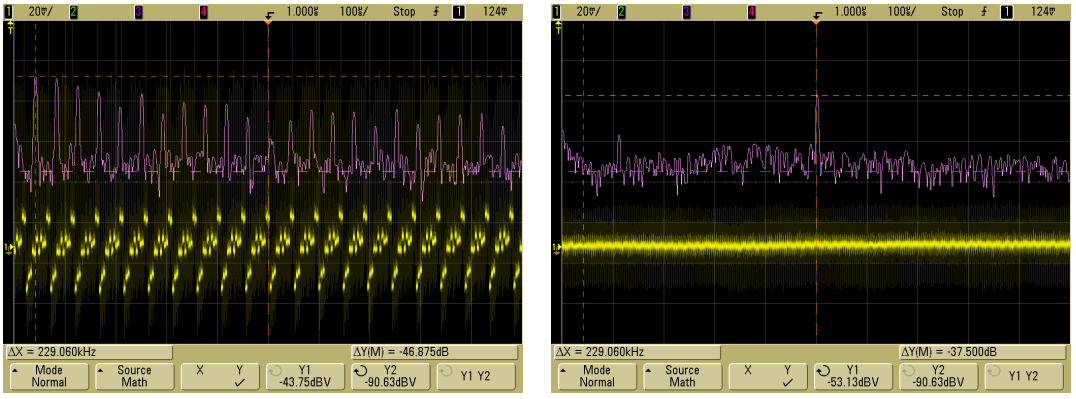


FIGURE 4.19: Sinusoid response

The figure 4.19 shows the response of the mirror for a sinusoidal input signal of 20kHz varying from 0V to 2.2V. This voltage is dropped over a resistance of 1kΩ generating a sinusoidal input current signal from 0A to 2.2mA. The output current from the mirror is passed through the resistance of 510Ω resulting in the voltage signal as shown in the figure 4.19(yellow).

4.3.7 FFT spectrum



(a) DEM only

(b) Calibration and DEM

FIGURE 4.20: FFT spectrum

The figure 4.20(a) shows the FFT spectrum of the output ripple in the DEM only mode. The clock frequency is 250kHz. In total there are 11 mirror devices, hence harmonics of (250/11)kHz are visible in the FFT spectrum. The FFT spectrum of the output ripple in the calibration with DEM is shown in the figure 4.20(b). It is visible from the FFT spectrum that the harmonics of (250/11)kHz are suppressed. The magnitude of the ripple at the DEM frequency is suppressed. For knowing the actual suppression of the DEM ripple a spectrum analyzer should be used, but due to practical limitations this measurement was not performed. It is expected that the suppression of the DEM ripple will be atleast two order of magnitude, which will be proved later by measuring it with a spectrum analyzer. The highest peak visible in the figure 4.20(b) is at 250kHz (clock frequency). The unwanted frequency component at 56kHz is coming because of some residual effect.

4.4 Chip Micrograph

Chip photo is shown in the figure 4.21.

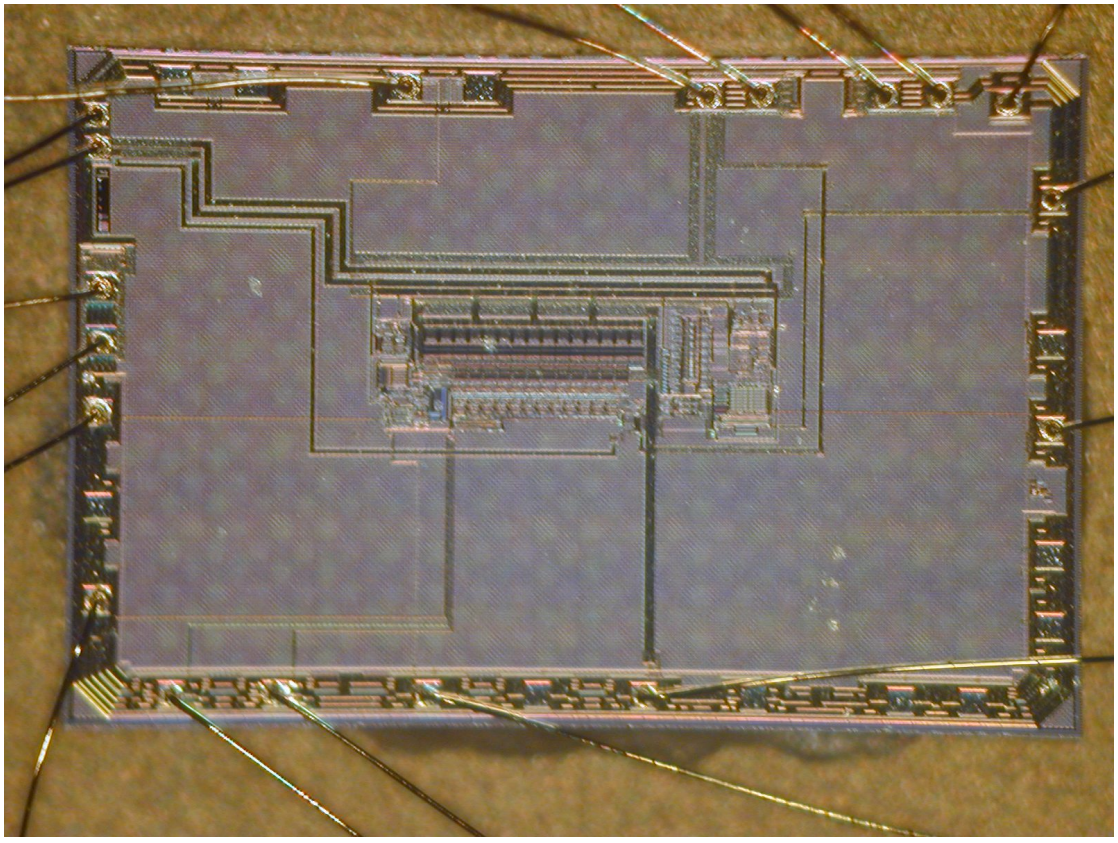


FIGURE 4.21: Chip micrograph

Chapter 5

Summary/Conclusion

5.1 Conclusion

A voltage-to-current converter is one of the most commonly used industrial current drivers. The accuracy of its output depends on the accuracy of the current mirror used in its construction. This thesis described the design steps of a precision current mirror intended for such V-I converters. To meet the stringent accuracy requirements, a new current mirror architecture based on sampling and modulation was developed. The proposed approach, which is referred to as the "precision current mirror", efficiently combines autozeroing [10] and dynamic element matching [25].

Study of state-of-the-art precision voltage-to-current converters revealed that order(s) of improvement in the output ripple caused by DEM operation, is required for an universal voltage controlled current source. The proposed approach aimed to provide a good DC and AC accuracy in the mirror output without the use of external components, thus reducing the cost and improving the resolution of state-of-the-art precision voltage to current converters. In the proposed current mirror architecture, benefits from both autozeroing and dynamic element matching were combined in a two-step scheme. In the first step, the individual device (one at a time) is compared with a standard device. The relative mismatch between the two devices generates an error current, which is sampled on the sampling capacitor. The voltage stored across the sampling capacitor is converted to a current by a gm stage, which is then pulled out from the source of the device that is being calibrated, causing a voltage change on the source node of that device. When the circuit settles, source voltage of the calibrated device is adjusted such that the mismatch (due to V_{TH} and β variations) between the standard and calibrated device is removed. In the final step, this device is connected to the main mirror circuit

that is being DEM'ed and another device is taken out for calibration. This process is repeated periodically until all the devices are calibrated. After one complete cycle (depends on the gain of the mirror), the output current from the mirror will be free from the DEM ripple, as the mismatch between the mirror devices was already calibrated out by a separate calibration circuit. A very fair question that can arise at this point is that, whether DEM is needed at all if the devices were already calibrated. The calibration is meant as an auxiliary technique to remove the ripple, but is not intended to be good enough to replace DEM. Thus, DC accuracy of the output current from the mirror is ensured by DEM and ripple is suppressed by the calibration technique. The measurement results have shown a 50X improvement in the DEM ripple compared to state-of-the-art (XTR111). The DC accuracy is $\pm 0.18\%$, which is comparable to XTR111 [4] from Texas Instruments (TI), one of the best reported state-of-the-art specifications.

A substantial improvement in the AC accuracy of the output current compared to prior voltage-to-current converters has also been achieved in this work. However the measurement results showed that the DC accuracy did not improve (when compared to state-of-the-art) even after calibrating the devices. Further improvements, however, are still possible both in circuit and topology levels. For instance, differential sampling can be used to improve the performance of the current mirror over varying supply voltage. Its performance can be further improved with the help of a new sub-regulator having better PSRR and low output impedance.

However, the key change in the next version would be to increase the size of the switch Sg (see figure 3.18) that is used for connecting the gate of the device (that needs to be calibrated) with a separate calibration circuit (see figure 3.4). It should be kept in mind that increasing the size of the gate switch will decrease the noise floor of the circuit but charge injection will increase. The excess charge from the switch will cause some residual DC error, resulting in a trade-off between DC accuracy and noise floor. Further improvement in the noise floor is also possible by increasing the size of the main mirror devices Mc1-11 (see figure 3.5). Another aspect that is still open for investigation is the up modulation of $1/f$ noise, which is coming from M_2 and M_3 (refer to figure 3.7). The up modulation of $1/f$ noise can be seen in the figure 4.12, which is approximately equal to 20% of the total noise floor at 14KHz.

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