Bulk Micromachined Electrostatic RMS-to-DC Converter

Ger de Graaf, *Member, IEEE*, Marian Bartek, *Member, IEEE*, Z. Xiao, Cees J. van Mullem, and Reinoud F. Wolffenbuttel, *Senior Member, IEEE*

***Abstract*—Bulk micromachining in silicon and glass wafers and subsequent silicon-to-glass anodic bonding have been used for the realization of an electrostatic rms-to-dc converter. A suspended membrane has been designed for: large dynamic operating range (detection limit by minimum mechanical-thermal noise and high value of the pull-in voltage), maximum bandwidth (low series resistance, high second harmonic suppression using squeeze film damping and suspension beam design), long-term stability, and a sufficient displacement-to-voltage sensitivity (membrane area and suspension arm length).**

Prototypes are typically composed of a 3 $\times$ 3 mm^2 perforated membrane area suspended by four beams of 200 μm length, 500 μm width, and 4 μm thickness micromachined out of silicon and aligned to a counter electrode on glass with 4-μm spacing in between. Measurements on realized devices show a 4.5 pF nominal capacitance. Static measurements indicate a sensitivity of 5 fF/V^2 and a voltage shift of 0.2 V. The nominal square relation is achieved within a 0.5% nonconformity error.

***Index Terms*—rms-to-dc converter, wafer-to-wafer bonding.**

I. Introduction

RMS-TO-dc conversion is conventionally realized using either a thermal technique based on the temperature increase of a heated resistor [1] or analog circuits to perform the squaring and time integrating functions [2]. Electrostatic approaches have been introduced as alternative; however, first generation devices based on surface-micromachined beams demonstrated too small a voltage-to-displacement sensitivity for practical implementation [3]. Bulk micromachining enables the fabrication of larger area devices. Wafer-to-wafer bonding offers more flexibility in the design of the gap width between the electrodes. These techniques are used in the fabrication of the practical rms-to-dc converter presented here.

The basic electrostatic rms-to-dc converter is simply a suspended movable plate electrode with a counter electrode at a fixed position, as shown schematically in Fig. 1. Upon application of a voltage V, the suspended plate is deflected to a position at which the electrostatic force is counteracted by the spring force:

$$\Delta d = \frac{\varepsilon A V^2}{2k\left(d_o - \Delta d\right)^2} \approx \frac{\varepsilon A V^2}{2k d_o^2}$$

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G. de Graaf and R. F. Wolffenbuttel are with Delft University of Technology, ITS/Et, DIMES/ Lab. EI, 2628 CD Delft, The Netherlands.

M. Bartek is with Delft University of Technology, ITS/Et, DIMES/Lab. ECTM, 2628 GB Delft, The Netherlands.

Z. Xiao is with the Microelectronics Research Center, New Jersey Institute of Technology, Newark, NJ 07102 USA.

C. J. van Mullem is with NMi/VSL, 2600 AR Delft, The Netherlands.

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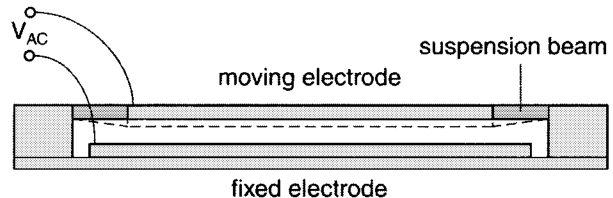

Fig. 1. Basic structure of an electrostatic rms-to-dc converter.

where

- ε permittivity;
- d_o gap width between the plates;
- A plate area;
- k spring constant of the suspension.

The deflection is therefore depending on the voltage squared. The formal definition of the V_{rms}^2 also includes the integration of the squared signal. This is realized in a micromechanical device using the squeeze film damping of the gas (air) in between the plates [4]. This damping mechanism is due to the incompressibility of the gas in between the electrodes and causes the second-order system to be highly overdamped to the extend that it can be represented by a first-order low-pass system, with a pole located in the sub-hertz range.

Squaring an ac voltage with frequency ω_{ac} results in a dc component and a component at $2\omega_{ac}$. Operation is based on capacitively measuring the slowly varying (dc) displacement and requires suppression of non-dc displacements. Squeeze film damping is not very effective at higher frequencies due to the compressibility of the gas at frequencies beyond the squeeze number [5]. In the higher frequency range, the gas behaves like a spring and other structural means have to be used to attenuate the $2\omega_{ac}$ component. The second drawback of an overdamped system is the relatively high mechanical-thermal noise level [6]. The design therefore involves an optimization of the dynamic response of the membrane deflection versus applied voltage at a required dc sensitivity.

Membrane area and suspension beam cross-sectional area and length were designed for a 5–10 pF nominal device capacitance. Membrane area, electrode spacing and suspension beam dimensions were designed for a 10 mV threshold of detectivity and a 10 V full scale and maximum attenuation of the second harmonic component. The design issues are discussed in the next section, device fabrication in Section III and the results in Section IV.

II. Design

The device presented here is composed of two wafers; one silicon wafer with a bulk-micromachined suspended membrane and one glass wafer with a fixed electrode pattern, as shown

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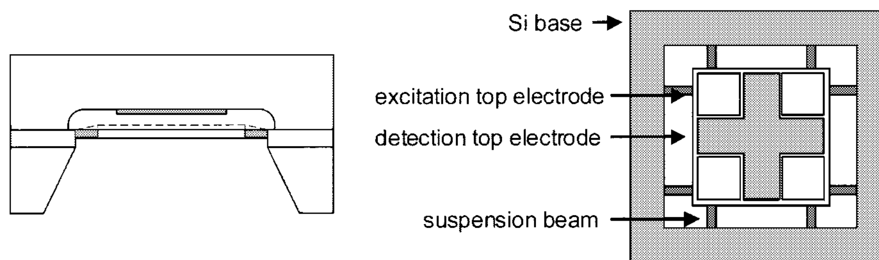

Fig. 2. Structure of the silicon bulk-micromachined electrostatic rms-to-dc converter.

in Fig. 2. Bonding results in the membrane and electrode facing each other with typically a 4-μm spacing. The electrostatic force acting on the suspended membranes is proportional to the square of the voltage. Upon applying an ac-voltage, the steady-state displacement is set by the suspension beam dimensions and the dynamics of the displacement is set by the squeeze-film damping.

The main design objective is a dynamic range of 10^3. The minimum ac voltage level than can be measured is set by the mechanical-thermal noise [6], the noise in the piezoresistive or capacitive sensing element (as scaled to the input using the sensitivity for voltage-to-deflection) and the equivalent input noise due to the readout circuits. The thermomechanical noise level is determined by fluctuations in the squeeze-film damping force and is expected to limit the performance. Disregarding compressibility yields a mean squared force noise expressed as

$$\overline{F_n^2} = 4k_B T \frac{\partial F_d}{\partial v_z} B = 4k_B T \frac{\alpha_\beta \mu A^2}{d_o^3} B$$

where

$\mathrm{k_B} = 1.38.10^{-23}$ J/K	Boltzmann constant;
$\mathrm{T} = 300$ K	operating temperature,
$\mathrm{F_d}$	damping force,
$\mathrm{v_z}$	plate velocity in the vertical direction,
B	bandwidth,
α_β	geometrical constant equal to 0.42 for a square plate,
μ	viscosity of the gaseous medium in which the plate moves (in air at atmospheric pressure $\mu = 1,8.10^{-5}$ Pa.s),
A	plate area
$\mathrm{d_o}$	nominal plate separation (at $\mathrm{V} = 0$).

The vertical electrostatic force acting on a suspended plate, when applying a voltage across this plate and a parallel plate at spacing $\mathrm{d_o}$, can for $\mathrm{A} \gg \mathrm{d_o^2}$ be expressed by

$$F_{es} = \frac{\varepsilon A V^2}{2d_o^2}.$$

Equating the expressions for the root mean squared noise force and the electrostatic force yields the mechanical-thermal noise equivalent ac voltage $\mathrm{V_{NE}}$

$$V_{NE} = \sqrt[4]{\frac{16 d_o k_B T \alpha_\beta \mu B}{\varepsilon^2}}.$$

The plate area is not in the equation due to the fact that both the damping force and electrostatic force are surface effects. The only practical design variable is the plate spacing $\mathrm{d_o}$. For fabrication convenience the spacing is set to $\mathrm{d_o} = 4\ \mu$m, which yields $\mathrm{V_{NE}} = 10$ mV for a 1 Hz bandwidth.

The damping, and thus the thermal-mechanical noise level, can be controlled by perforation of the membrane. This technique is already widely used in Si microphones to reduce squeeze film damping in order to gain bandwidth [7]. An improvement by a factor 100–1000 can be achieved without a significant loss of electrode area, due to fringe fields.

The sensitivity for voltage-to-displacement has to be sufficiently large in order to ensure that the threshold of detectivity is limited by the mechanical-thermal noise and not by piezoresistor noise or circuit noise. However, this objective is hindered by the maximum voltage that can be applied without causing pull-in. Pull-in occurs in the suspended parallel plate structure considered here in case the vertical displacement Δd exceeds $\mathrm{d_o}/3$ [8]. The vertical displacement versus force is determined by the spring constant k of the suspension beams and thus sets the maximum acceptable ac voltage level

$$k = \frac{F_{es,\max}}{\Delta d_{\max}} = \frac{3F_{es,\max}}{d_o} = \frac{3\varepsilon A V_{\max}^2}{2d_o\left(d_o - d_o/3\right)^2} = \frac{27}{8}\frac{\varepsilon A V_{\max}^2}{d_o^3}.$$

A practical value or the spring constant of a plate suspended by four beams is $k = 100$ N/m. For a pull-in voltage exceeding $\mathrm{V_{max}} = 10$ V, a plate area $\mathrm{A} = 5.10^{-6}\ \mathrm{m}^2$ results.

A second issue related to the gap width is the squeeze-film damping itself. This directly determines several aspects of the dynamic behavior. First, the low-frequency -3 dB cutoff frequency at a given membrane area and perforation density increases with gap width. For a nonperforated $3 \times 3\ \mathrm{mm}^2$ membrane of 4 μm thickness, this frequency is $\mathrm{f_{-3\,dB}} = 0.1$ Hz at a 4-μm gap and $\mathrm{f_{-3\,dB}} = 1$ Hz in the case of a 8-μm wide gap. Obviously, a very low cutoff frequency contradicts with low thermomechanical noise performance. Second, the squeezed film should attenuate the $2\omega_{\mathrm{ac}}$ component. However, due to compressibility a squeezed film acts as a damper only for the lower frequency range. Beyond a certain frequency, the film acts as a spring due to the compressibility effect. The transition frequency range in which the gas starts behaving like a compressible medium results in a peak in the frequency plot [9]. Basically, this limits the maximum frequency up to which one can rely on the squeeze film damping. For a $3 \times 3\,\mathrm{mm}^2$ membrane of 4 μm thickness, this frequency is $\mathrm{f_{max}} = 226$ kHz at a 4-μm gap and $\mathrm{f_{max}} = 150$ kHz in the case of a 8-μm wide gap. This implies that the mechanical resonance frequency should be designed at a low enough value that the

low-pass nature of the structure provides sufficient attenuation of the second harmonic component for $f_{ac} > 75$ kHz. Third, the squeeze-film damping plays an essential role in avoiding any influence of mechanical resonance of the structure. For this reason the structure should be designed for a low resonance frequency, using the number of beams and the length of each beam. Obviously, the dimensioning of the suspension is limited by the required voltage-to-deflection sensitivity. For a 4×4 mm^2 membrane of 4 μm thickness and suspended by four beams each 500 μm wide and 4 μm thick, the resonance frequency decreases from 1450 Hz to 1300 Hz in case the suspension beam length is increased from 100 μm to 300 μm.

These considerations yield a starting configuration, which has been optimized using FEM simulations. Based on those results, structures have been fabricated with: plate spacing $d_o = 4$ μm, plate area A between 3000×3000 μm^2 and 4200×4200 μm^2, and between four and eight suspension beams, typically between 300 and 600 μm length and of variable width.

III. Fabrication

The designed structure consist of anodically bonded silicon and glass wafers and has been fabricated following the sequence shown in Fig. 3.

A. Silicon Wafer

Double-side polished 100-mm p-type silicon wafers were used as the starting material. A 7-μm thick n-type epilayer is grown, in which the active mechanical structures are to be formed. A deep boron and a shallow As implantation was performed to form electrical contacts and the wafer edge isolation rim (required for the electrochemical etch stop). Subsequent field oxidation (320 nm) provides implant activation and passivation of the pn-junctions. After the field oxide was removed from the wafer back side, 300 nm of silicon nitride and 200-nm poly-Si layer stack is deposited using LPCVD. The SiN layer is used as a masking layer during anisotropic etching in KOH, while the poly-Si layer provides an effective scratch protection. The SiN/poly-Si stack is removed from the front side and a conventional Al metallization is performed. The field oxide was removed from the final structure to facilitate the anodic bonding to the glass wafer and remains below the Al metallization only.

From the front side, a 4-μm deep recess was etched using RIE and a photoresist mask, defining the future square membrane with supporting beams.

B. Glass Wafer

Pyrex #7740 glass wafers were patterned using a 200-nm thick a-Si masking layer and 10% HF etchant. In the first step shallow recess of 1.2 μm, required for press-on contact and anti-sticking bumps, was formed. In the second step, the deep recess of 4.6 μm was formed in the same way. It should be mentioned, that the etching rate of Pyrex glass is not constant and depends on etch depth.

After forming the recess, the masking a-Si layers are removed in TMAH at 60 °C. TMAH has an excellent etching selectivity between Si and glass or oxide (>1 000 : 1); therefore, even the native oxide has to be first removed in a 1% HF.

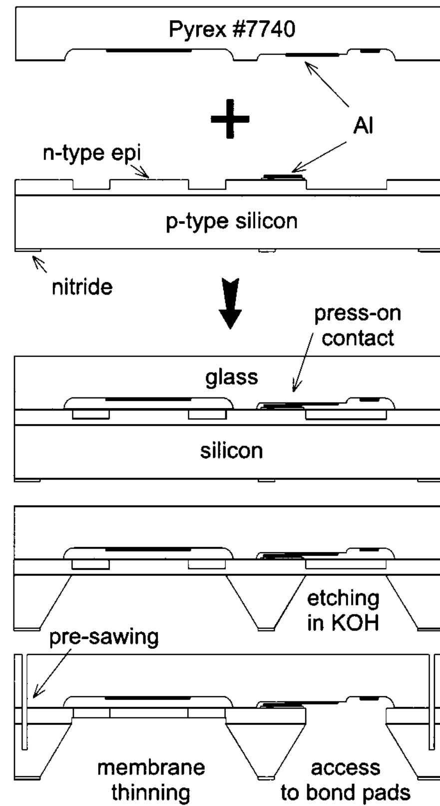

Fig. 3. Schematic fabrication sequence.

A 0.6-μm Al metal pattern was prepared in a conventional way by sputtering and wet etching using 2-μm resist mask. The structure is designed in such a way that the metal pattern is placed in one of the two recesses, so that no vertical steps have to be crossed.

As a final fabrication step a small through-wafer hole (~3 mm diameter) has to be drilled at the edge of the glass wafer. This hole is required during the an-isotropic etching to provide possibility to make an electrical contact to the epitaxial layer of the bonded silicon wafer. Before drilling, both sides of the glass wafer were coated with a protective photoresist layer to avoid any unwanted contamination and mechanical scratches. Drilling is performed under water using a diamond coated drilling tool at 20 000 r/min.

C. Bonding and Post-Bond Processing

After the silicon and glass wafers were completed, both wafers are anodically bonded at 400 °C for 30 min. The resulting wafer stack (see Fig. 4) forms a relatively rigid structure that can easily withstand further processing. Subsequent an-isotropic etching of silicon in 33 wt.% KOH solution in water was performed in a wafer holder. The wafer holder has to be modified to accommodate the increased thickness of the wafer stack. The electrochemical etch stop used ensures uniform membrane thickness (~6.5 μm) over the entire wafer.

At this stage, the wafer stack is (pre-) sawn from the side of the glass wafer into individual dies. In the final processing step,

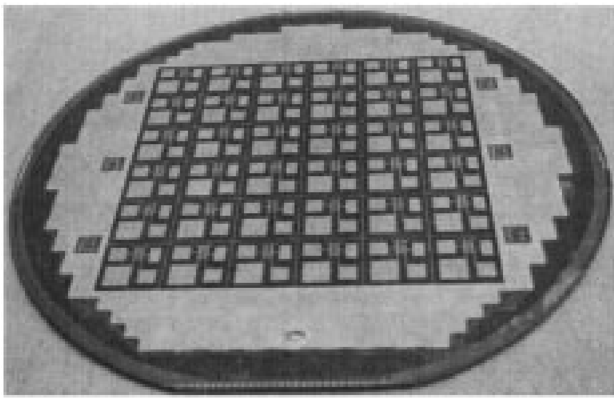

Fig. 4. Silicon–glass wafer stack (100 mm diameter) after anodic bonding and anisotropic etching in KOH. Each of the 10×10 mm^2 dies contains four devices and a common area for wire bonding.

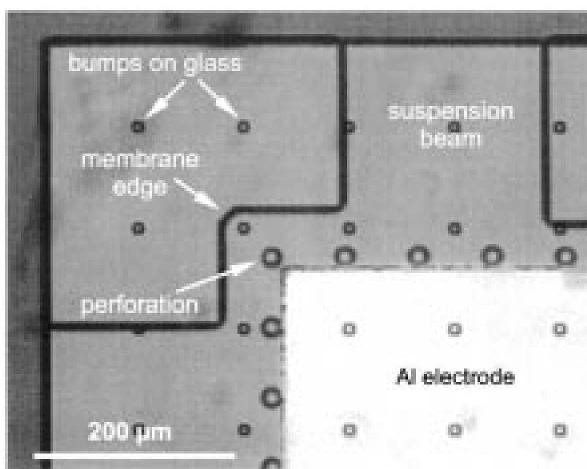

Fig. 5. Left upper corner of one of the devices (view through glass) showing its principal parts: perforated membrane, 200-μm wide suspension beams, Al electrode, and an array of anti-sticking bumps on glass.

the active structures are released by thinning the silicon membrane using plane plasma etching of silicon. The release step was performed on a die level for testing purposes only. A typical device is shown in Fig. 5, which clearly shows the perforation of the membrane area, which is included for the control of the squeeze-film damping.

Individual dies are mounted into a ceramic package (glass down) and electrical contacts are wire-bonded. The electrical interconnection between the glass and silicon wafers was realized using press-on contacts, as shown in Fig. 6.

IV. Measurement Results

The capacitance versus dc voltage characteristics of fabricated devices has been measured using the HP4191A Impedance/gain-phase analyzer in the impedance measurement mode at a frequency of 300 kHz and 500 mW oscillator power level. The bias voltage was controlled using Hp-Vee. Initially, a zero-open calibration was performed to correct for cable capacitance. A typical result is shown in Fig. 7. The squared relation is clearly visible.

More detailed analysis of the measurement results reveal a nominal capacitance of 4.516 pF and a voltage shift of about

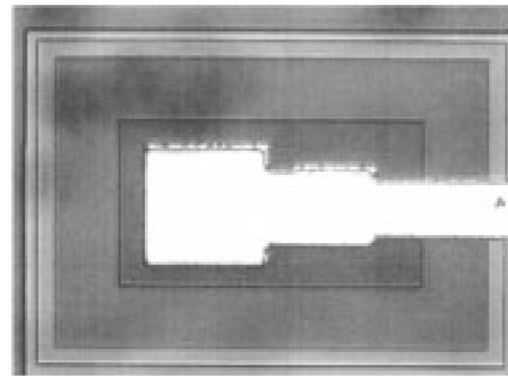

Fig. 6. Electrical interconnection between the glass and silicon wafers was realized using press-on contacts, as shown in this photograph (view through glass).

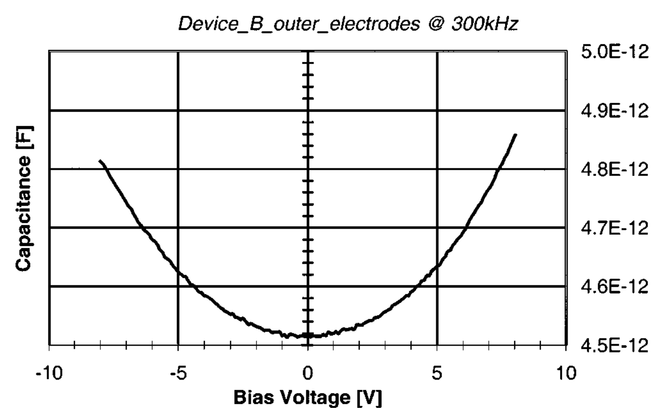

Fig. 7. Capacitance versus dc voltage of fabricated devices, measured using the HP4191A Impedance/gain-phase analyzer in the impedance measurement mode at a frequency of 300 kHz and 500 mW oscillator power level.

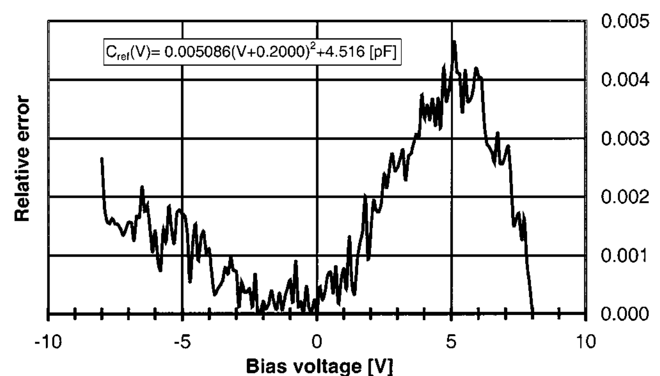

Fig. 8. Relative error between measurement results and a theoretical reference.

0.2 V. This voltage shift is assumed to be due to charging of the dielectric [10]. The maximum deviation from the ideal square relation is less than 0.5%, as is shown in Fig. 8.

V. Conclusions

The design and fabrication of an electrostatic rms-to-dc converter is presented. Bulk micromachining and anodic silicon-to-glass bonding were used for the fabrication of stable and practical devices. Prototypes are typically composed of a 3×3 mm^2 perforated membrane area suspended by four beams of 200 μm

length, 500 μm width, and 4 μm thickness micromachined out of silicon and aligned to a counter electrode on glass with 4-μm spacing in between. The dimensions and the perforation density are dictated by device specifications such as sensitivity, detection limit and frequency range. The present device was designed for a detection limit at 10 mV, a 10^3 dynamic range, and a -3 dB frequency range between 0.1 Hz and 50 kHz. Additionally, long-term stability had to be optimized.

Measurements on realized devices show a 4.5 pF nominal capacitance. Static measurements indicate a sensitivity of 5 fF/V^2 and a voltage shift of 0.2 V. The nominal square relation is achieved within a 0.5% nonconformity error.

An extensive testing program on dynamic behavior and long-term stability is forthcoming.

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Ger de Graaf (M'98) received the B.S.E.E. degree in electrical and control engineering from the Technische Hogeschool, Rotterdam, The Netherlands, in 1983.

Since 1976, he has been a staff member of the Department of Electrical Engineering, Delft University of Technology, Delft, The Netherlands. Currently, he is working on electronic circuits for silicon sensors. In 1992, he founded a consultancy company specializing in electronic design and computer-controlled measurement systems.

Marian Bartek (S'91–M'95) received the M.Sc. degree in microelectronics and optoelectronics from the Slovak Technical University, Bratislava, Slovakia, in 1988, and athe Ph.D. degree in electrical engineering from Delft University of Technology, The Netherlands, in 1995, where, between 1996 and 1999, he was a Postdoctoral fellow dealing with research on technological aspects of integrated silicon sensor systems.

Since 2000, he has been with the Electronic Components, Materials, and Technology Laboratory, Delft University of Technology, as an Assistant Professor, working in the area of RF MEMS and wafer-level packaging.

Z. Xiao photograph and biography not available at the time of publication.

Cees J. van Mullem received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1989 and 1993, respectively.

He is currently with the Department of Electricity and Magnetism, NMi Van Swinden Laboratorium (the Dutch National Standards Laboratory), Delft, The Netherlands, where he is involved in the development and maintenance of ac-to-dc transfer standards, especially in the frequency range of 100 kHz–100 MHz, dc-LF high-precision measurement techniques, sensor technology, and RF power measurements.

Reinoud F. Wolffenbuttel (S'86–M'88–SM'97) received the M.Sc. and Ph.D. degrees from the Delft University of Technology, Delft, The Netherlands, in 1984 and 1988, respectively.

Between 1986 and 1993, he was an Assistant Professor, and since 1993, an Associate Professor, at the Laboratory of Electronic Instrumentation of the Delft University of Technology, where he is involved in instrumentation and measurement in general and on-chip functional integration of microelectronic circuits and silicon sensor, fabrication compatibility issues, and micromachining in silicon and microsystems, in particular. He was a Visitor at the University of Michigan, Ann Arbor, in 1992, 1999, and 2001, at Tohoku University, Sendai, Japan, in 1995, and at EPFL, Lausanne, Switzerland, in 1997.

Dr. Wolffenbuttel was the recipient of a 1997 NWO pioneer award. He served as General Chairman of the Dutch National Sensor Conference in 1996 and Eurosensors in 1999.