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Kuruganti, V.V.

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Atmospheric Pressure Chemical Vapour Deposition for High-efficiency c-Si Solar Cells

Vaibhav Venkat KURUGANTI

Atmospheric Pressure Chemical Vapour Deposition for High-efficiency c-Si Solar Cells

Dissertation

for the purpose of obtaining the degree of doctor
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by

Vaibhav Venkat KURUGANTI

Master of Science in Sustainable Sytems Engineering,
University of Freiburg, Germany
born in Hyderabad, India

This dissertation has been approved by the promoters.

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Other members:	
Dr. V. D. Mihailetchi	ISC Konstanz, Germany

Keywords: Photovoltaic, Atmospheric Pressure Chemical Vapor Deposition, Patterning technique, Interdigitated back contact solar cells, TOPCon solar cells, In-situ annealing, Firing stability of polysilicon layers

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This dissertation is dedicated to my parents.

Two roads diverged in a wood,
I took the one less travelled by,
and that has made all the difference.
Robert Frost

Contents

Summary

The continuous expansion of global populations and economic progress leads to a corresponding surge in energy consumption. Addressing these demands with traditional fossil fuels presents a major challenge because of their substantial greenhouse gas emissions, which play a significant role in driving climate change. A viable strategy to address carbon dioxide (CO_2) emissions while meeting increasing global energy demand involves the utilization of renewable energy sources for power generation. In recent decades, the energy market has seen a noticeable increase in the proportion of renewable energy sources. Recent reports from the International Energy Agency (IEA) project that solar photovoltaic (PV) systems will outpace natural gas and coal in installed power capacity, establishing their leadership in the energy sector by the end of 2027. According to ITRPV reports, if current trends and the growth trajectory continue, maintaining a 25% annual increase in PV installations over the next decade could result in an installed capacity of 75 TW by 2050. To bolster the prevalence of PV technology on the electricity grid, it is essential to continually optimize solar cells, whether by boosting their power conversion efficiency (η) or reducing their production costs.

This thesis consists of seven chapters in total. The first chapter provides a concise overview of the need for renewable energy sources to meet the growing energy demand. It highlights significant advancements in the photovoltaic market, particularly in lowering production costs while steadily improving conversion efficiencies.

The second chapter provides a comprehensive literature review of various solar cell concepts, along with a concise history of solar cells and a brief introduction to APCVD technology.

The presence of both polarities on the rear side of Interdigitated Back Contact (IBC) solar cells necessitates implementing a patterning procedure. Chapter 3 of this thesis is dedicated to investigating a novel approach for patterning IBC solar cells. Patterning in IBC solar cells is achieved by utilizing the enhanced oxidation characteristics under the laser-doped back surface field (BSF) regions. Selective oxide growth, with a thickness 2.8 times greater in laser-doped areas compared to non-lasered areas, was achieved through optimizing $POCl_3$ diffusion, laser doping, and subsequent wet thermal oxidation parameters. This selectivity in the oxide thickness between lasered and non-lasered areas is employed to pattern the rear side of the IBC solar cell through wet bench etching. The retained SiO_2 layer beneath the laser-doped regions post patterning functions as a diffusion barrier for the subsequent boron diffusion process, during which the emitter region is formed on the non-lasered regions. This innovative patterning process was utilized to fabricate proof-of-concept solar cells, resulting in a maximum conversion efficiency of 20.41% on a M2 wafer format. This study offers a comprehensive analysis of the benefits and constraints associated with employing this methodology in passivating contact IBC solar cells.

Chapter 4 presents a compelling case for employing APCVD glass layers in the production of cost-effective yet highly efficient solar cells. This study employs APCVD doped glass layers, such as APCVD PSG and BSG layers, instead of traditional industrial furnace tube diffusions like $POCl_3$ and BBr_3 diffusion, to create all doped regions of the IBC solar cells. Unlike the conventional diffusion process, after the deposition of the doped glass layers using APCVD technology, there is a need for a high temperature annealing step. In this study, the high-temperature annealing step, carried out partially in an oxygen (O_2) environment, serves three main purposes, namely: (i) facilitate the diffusion of dopants into the c-Si substrate, (ii) prevent the formation of a boron-rich layer in the case of boron doped c-Si, and (iii) grow an in-situ SiO_2 at the Si/dopant glass interface for passivation purposes. The disparity in etch rates between the in-situ grown SiO_2 and the doped glass layer is used to entirely remove the doped glass. After etching, the remaining in-situ SiO_2 is capped with PECVD SiN_x to passivate both polarities of IBC solar cells. A full APCVD IBC solar cell achieved a conversion efficiency of 22.8% at the device level on a M2 wafer format, featuring an open-circuit voltage (V_{oc}) of 696 mV and a short-circuit current density (J_{sc}) of 41.3 mA/cm^2. These parameters are comparable to commercially available full-tube diffused ZEBRA® IBC solar cells.

Chapter 5 presents the RJ-TOPCon solar cell concept based on an n-type substrate. This solar cell features an APCVD boron-doped poly-Si rear emitter and a $POCl_3$-diffused phosphorus-doped front surface field (FSF), as well as a selectively laser-doped region with high phosphorus doping beneath the front metal contacts. In this chapter, the eectrical and passivation properties of the various doped regions are individually optimized. The $POCl_3$ diffusion process was optimized by incorporating a deposition phase without the drive-in step to create a shallow junction in the FSF regions. The following wet thermal oxidation step further reduces the surface concentration of the shallow-doped FSF, enhancing passivation. After wet thermal oxidation, an FSF with a sheet resistance of 2000 Ω/sq and a surface concentration as low as 1 x 10^{18} cm^{-3} was achieved. This lightly doped FSF region demonstrated excellent passivation quality, with an iV_{oc} of 728 mV using a PECVD SiO_x/SiN_x passivation stack. Optimal laser doping settings was chosen to minimize laser-induced damage while maintaining high conductivity. After wet thermal oxidation, the laser doped selective FSF with a sheet resistance of 85 Ω/sq and a surface concentration of 7 x 10^{19} cm^{-3} was achieved. This laser doped selective FSF region with a PECVD SiO_x/SiN_x passivation stack had iV_{oc} of 690 mV. In this study, we devised an in-situ annealing process to crystallize boron-doped amorphous silicon (p^+ a-Si) layers deposited via APCVD into boron-doped polycrystalline silicon (p^+ poly-Si) layers. The findings demonstrate successful crystallization of p^+ a-Si layers by adjusting temperature profiles in the post-deposition zones of the APCVD tool. Notably, hydrogenation processes during fast firing significantly improved the passivation quality and electrical properties of the in-situ annealed poly-Si p^+ layers. The sheet resistance of 200 Ω/sq was obtained on 150-nm thick poly-Si p^+ layers with an iV_{oc} of 718 mV upon passivating with a PECVD SiN_x layer. With this excellent electrical and passivation quality of the doped regions, the RJ-TOPCon solar cells are expected to exceed conversion efficiencies beyond 24%, making them comparable to state-of-the-art conventional TOPCon solar cells.

While significant research has been dedicated to examining the effects of firing on poly-Si passivating contacts, the origins of this issue and effective mitigation strategies

remain poorly understood. In Chapter 6 of this thesis, I examine the impact of firing on the n^+ poly-Si passivating contacts used in TOPCon solar cells, ultimately achieving blister-free n^+ poly-Si across a wide range of firing temperatures. The firing stability of n^+ poly-Si layers is evaluated by varying the doping method (in-situ versus ex-situ doping), the sequence of $POCl_3$ diffusion in ex-situ doping (i.e., $POCl_3$ diffusion followed by high temperature annealing step and vice versa), and the choice of capping layer atop the n^+ poly-Si layer. Our findings conclude that in-situ doped n^+ poly-Si layers exhibit higher stability compared to those doped ex-situ. For ex-situ doped n^+ poly-Si layers, the samples that were annealed prior to $POCl_3$ diffusion were found to more prone to firing induced depassivation. Lastly, we demonstrate that incorporating a dielectric layer with low hydrogen content, such as PECVD silicon oxide (SiO_2) or phosphosilicate glass (PSG), between the poly-Si and PECVD SiN_x layers, substantially enhances the firing stability of the passivating contacts stack.

In conclusion, this thesis focuses on developing cost-effective yet industrially viable high-efficiency solar cell concepts using APCVD technology. It comprises four main achievements. First, it demonstrates a novel patterning and masking technique for fabricating IBC solar cells, which utilizes the enhanced oxidation characteristics under the laser-doped n^+ regions. Second, by employing APCVD-doped glass layers to form the doped regions of the IBC solar cells, I have achieved similar conversion efficiency as that of commercially available full-tube diffused ZEBRA® IBC solar cells. Third, the concept of in-situ annealing of boron-doped amorphous silicon p^+ layers, deposited by APCVD, eliminates the need for the high-temperature poly-Si annealing step, thereby reducing the thermal budget of industrial TOPCon solar cells. Fourth, the use of a bi-layer stack with low hydrogen content, such as PECVD silicon oxide (SiO_2) or phosphosilicate glass (PSG), between the poly-Si and PECVD SiN_x layers, significantly improves the firing stability of the passivating contacts stack.

Samenvatting

De voortdurende groei van de wereldbevolking en de economische vooruitgang leiden tot een overeenkomstige toename van het energieverbruik. Het aanpakken van deze vraag met traditionele fossiele brandstoffen vormt een grote uitdaging vanwege de aanzienlijke uitstoot van broeikasgassen, die een belangrijke rol spelen bij klimaatverandering. Een haalbare strategie om de uitstoot van kooldioxide (CO_2) te verminderen en tegelijkertijd te voldoen aan de toenemende wereldwijde energievraag, is het gebruik van hernieuwbare energiebronnen voor elektriciteitsopwekking. In de afgelopen decennia heeft de energiemarkt een duidelijke toename gezien in het aandeel van hernieuwbare energiebronnen. Recente rapporten van het Internationaal Energieagentschap (IEA) voorspellen dat zonnefotovoltaïsche (PV) systemen tegen eind 2027 in geïnstalleerde capaciteit aardgas en steenkool zullen overtreffen, waardoor zij hun leiderschap in de energiesector zullen vestigen. Volgens rapporten van ITRPV kan het aanhouden van een jaarlijkse toename van 25% in PV-installaties, als de huidige trends en de groeicurve zich voortzetten, leiden tot een geïnstalleerde capaciteit van 75 TW in 2050. Om de prevalentie van PV-technologie op het elektriciteitsnet te versterken, is het essentieel om zonnecellen continu te optimaliseren, ofwel door hun energieomzettingsefficiëntie (η) te verhogen of door hun productiekosten te verlagen.

Deze thesis bestaat in totaal uit zeven hoofdstukken. Het eerste hoofdstuk biedt een beknopt overzicht van de noodzaak van hernieuwbare energiebronnen om te voldoen aan de groeiende energievraag. Het benadrukt belangrijke ontwikkelingen in de fotovoltaïsche markt, met name in het verlagen van productiekosten terwijl de omzettingsefficiëntie gestaag wordt verbeterd.

Het tweede hoofdstuk biedt een uitgebreide literatuurstudie van verschillende zonnecelconcepten, samen met een beknopte geschiedenis van zonnecellen en een korte introductie tot APCVD-technologie.

De aanwezigheid van beide polariteiten aan de achterzijde van Interdigitated Back Contact (IBC) zonnecellen vereist de implementatie van een patroonprocedure. Hoofdstuk 3 van deze thesis is gewijd aan het onderzoeken van een nieuwe benadering voor het patrooneren van IBC-zonnecellen. Patroonvorming in IBC-zonnecellen wordt bereikt door gebruik te maken van de verbeterde oxidatie-eigenschappen onder de lasergedoteerde rugveld (BSF) gebieden. Selectieve oxidegroei, met een dikte die 2,8 keer groter is in lasergedoteerde gebieden in vergelijking met niet-gelaserde gebieden, werd bereikt door het optimaliseren van $POCl_3$ diffusie, laserdoping en daaropvolgende natte thermische oxidatieparameters. Deze selectiviteit in de oxidedikte tussen gelaserde en niet-gelaserde gebieden wordt gebruikt om de achterzijde van de IBC-zonnecel te patrooneren door middel van natchemisch etsen. De behouden SiO_2 laag onder de lasergedoteerde gebieden na patroonering fungeert als een diffusiebarrière voor het daaropvolgende borondiffusieproces, waarbij het emittergebied wordt gevormd op de niet-gelaserde gebieden. Dit innovatieve patroonproces werd gebruikt om proof-of-concept zonnecellen te fabriceren,

resulterend in een maximale omzettingsefficiëntie van 20,41% op een M2-wafelformaat. Deze studie biedt een uitgebreide analyse van de voordelen en beperkingen die gepaard gaan met het toepassen van deze methodologie in passiverende contact-IBC-zonnecellen.

Hoofdstuk 4 bespreekt overtuigend het gebruik van APCVD-glaslagen bij de productie van kostenefficiënte en tegelijkertijd zeer efficiënte zonnecellen. In deze studie worden APCVD-gedopeerde glaslagen, zoals APCVD PSG- en BSG-lagen, toegepast in plaats van traditionele industriële ovenbuizendiffusies zoals $POCl_3$- en BBr_3-diffusie om alle gedopeerde gebieden van de IBC-zonnecellen te creëren. In tegenstelling tot het conventionele diffusieproces is na de depositie van de gedopeerde glaslagen met behulp van APCVD-technologie een hoge-temperatuur annealstap noodzakelijk. Deze annealstap op hoge temperatuur, gedeeltelijk uitgevoerd in een zuurstofomgeving (O_2), heeft drie hoofddoelen: (i) het bevorderen van de diffusie van dopanten in het c-Si-substraat, (ii) het voorkomen van de vorming van een boorrijke laag bij boor-gedopeerd c-Si, en (iii) het in-situ groeien van een SiO_2 laag op de Si/dopantglas interface voor passivatiedoeleinden. Het verschil in etsnelheden tussen het in-situ gegroeide SiO_2 en de gedopeerde glaslaag wordt gebruikt om de gedopeerde glaslaag volledig te verwijderen. Na het etsen wordt de resterende in-situ SiO_2 afgedekt met PECVD SiN_x om beide polariteiten van IBC-zonnecellen te passiveren. Een volledig APCVD-gebaseerde IBC-zonnecel behaalde een conversie-efficiëntie van 22,8% op apparaatniveau op een M2-wafelformaat, met een open-circuit spanning (V_{oc}) van 696 mV en een kortsluitstroomdichtheid (J_{sc}) van 41,3 mA/cm^2. Deze parameters zijn vergelijkbaar met commercieel verkrijgbare volledig buizengeïnjecteerde ZEBRA® IBC-zonnecellen.

Hoofdstuk 5 introduceert het RJ-TOPCon-zonnecelconcept op basis van een n-type substraat. Deze zonnecel beschikt over een APCVD boor-gedopeerde poly-Si achteremitter en een $POCl_3$-gedopeerd fosfor-frontoppervlakteveld (FSF), evenals een selectief laser-gedopeerd gebied met hoge fosfordoping onder de voorste metaalcontacten. In dit hoofdstuk worden de elektrische en passiverende eigenschappen van de verschillende gedopeerde gebieden afzonderlijk geoptimaliseerd. Het $POCl_3$-diffusieproces werd geoptimaliseerd door een depositiefase zonder de drive-in stap op te nemen om een ondiep junctie in de FSF-gebieden te creëren. De daaropvolgende natte thermische oxidatiestap verlaagt de oppervlakteconcentratie van het ondiep-gedopeerde FSF verder, waardoor de passivering wordt verbeterd. Na natte thermische oxidatie werd een FSF met een plaatweerstand van 2000 Ω/vierkant en een oppervlakteconcentratie van slechts 1 x 10^{18} cm^{-3} bereikt. Dit licht gedopeerde FSF-gebied toonde uitstekende passiveringskwaliteit, met een iV_{oc} van 728 mV met behulp van een PECVD SiO_x/SiN_x-passiveringsstapel. Optimale laserdopinginstellingen werden gekozen om laserschade te minimaliseren en tegelijkertijd een hoge geleidbaarheid te behouden. Na natte thermische oxidatie werd een selectief laser-gedopeerde FSF met een plaatweerstand van 85 Ω/vierkant en een oppervlakteconcentratie van 7 x 10^{19} cm^{-3} bereikt. Dit selectieve laser-gedopeerde FSF-gebied met een PECVD SiO_x/SiN_x passiveringsstapel behaalde een iV_{oc} van 690 mV. In deze studie hebben we een in-situ annealproces ontwikkeld om boor-gedopeerde amorfe silicium (p^+ a-Si) lagen, die via APCVD zijn afgezet, te kristalliseren tot boor-gedopeerde polykristallijne silicium (p^+ poly-Si) lagen. De resultaten tonen aan dat een succesvolle kristallisatie van p^+ a-Si-lagen mogelijk is door de temperatuurprofielen in de post-depositie zones van het APCVD-gereedschap aan te passen. Opmerkelijk is dat

waterstofprocessen tijdens snel afvuren de passiveringskwaliteit en elektrische eigenschappen van de in-situ geannealde poly-Si p^+ lagen aanzienlijk hebben verbeterd. De plaatweerstand van 200 Ω/vierkant werd verkregen op 150 nm dikke poly-Si p^+ lagen met een iV_{oc} van 718 mV na passivering met een PECVD SiN_x laag. Met deze uitstekende elektrische en passiveringskwaliteit van de gedopeerde gebieden wordt verwacht dat de RJ-TOPCon-zonnecellen een conversie-efficiëntie van meer dan 24% zullen bereiken, vergelijkbaar met de meest geavanceerde conventionele TOPCon-zonnecellen.

Hoewel er veel onderzoek is gedaan naar de effecten van snel afvuren op poly-Si-passiverende contacten, zijn de oorzaken van dit probleem en effectieve mitigatiestrategieën nog steeds onvoldoende begrepen. In hoofdstuk 6 van dit proefschrift onderzoek ik de impact van snel afvuren op de n^+ poly-Si-passiverende contacten die in TOPCon-zonnecellen worden gebruikt, waarbij uiteindelijk blistervrije n^+ poly-Si is bereikt over een breed scala aan afvuurtijden en -temperaturen. De stabiliteit van n^+ poly-Si-lagen bij snel afvuren wordt geëvalueerd door de dopingsmethode (in-situ versus ex-situ doping), de volgorde van $POCl_3$-diffusie bij ex-situ doping (d.w.z. $POCl_3$-diffusie gevolgd door hoge-temperatuur-annealstap en vice versa), en de keuze van de afdekkingslaag bovenop de n^+ poly-Si-laag te variëren. Onze bevindingen concluderen dat in-situ gedopeerde n^+ poly-Si lagen een hogere stabiliteit vertonen in vergelijking met ex-situ gedopeerde lagen. Voor ex-situ gedopeerde n^+ poly-Si lagen bleek dat de monsters die voorafgaand aan $POCl_3$-diffusie waren geanneald, gevoeliger waren voor snel afvuren veroorzaakte depassivering. Tot slot tonen we aan dat het toevoegen van een diëlektrische laag met een laag waterstofgehalte, zoals PECVD siliciumoxide (SiO_2) of fosfosilicaatglas (PSG), tussen de poly-Si- en PECVD SiN_x-lagen, de stabiliteit van de passiverende contactstapel bij snel afvuren aanzienlijk verbetert.

Samenvattend richt dit proefschrift zich op de ontwikkeling van kosteneffectieve maar industrieel haalbare zonnecelconcepten met hoge efficiëntie met behulp van APCVD-technologie. Het proefschrift omvat vier hoofdresultaten. Ten eerste demonstreert het een nieuwe methode voor patroonvorming en maskering bij de fabricage van IBC-zonnecellen, waarbij gebruik wordt gemaakt van de verbeterde oxidatie-eigenschappen onder de laser-gedopeerde n^+-gebieden. Ten tweede heb ik door het gebruik van APCVD-gedopeerde glaslagen om de gedopeerde gebieden van de IBC-zonnecellen te vormen, een vergelijkbare conversie-efficiëntie bereikt als die van commercieel verkrijgbare volledig buizengeïnjecteerde ZEBRA® IBC-zonnecellen. Ten derde elimineert het concept van in-situ annealing van boor-gedopeerde amorfe silicium p^+ lagen, afgezet door APCVD, de noodzaak van de hoge-temperatuur annealing stap voor poly-Si, waardoor de thermische belasting van industriële TOPCon-zonnecellen wordt verminderd. Ten vierde verbetert het gebruik van een bi-layer stapel met een laag waterstofgehalte, zoals PECVD siliciumoxide (SiO_2) of fosfosilicaatglas (PSG), tussen de poly-Si- en PECVD SiN_x-lagen, aanzienlijk de.

Nomenclature

Abbreviations

a-Si	Amorphous silicon
Ag	Silver
Al	Aluminium
ALD	Atomic layer deposition
APCVD	Atmospheric pressure chemical vapor deposition
AR	Aspect ratio
BB	Busbar
BiPV	Building integrated photovoltaics
BRL	Boron rich layer
BSF	Back surface field
BSG	Borosilicate glass
c-Si	Crystalline silicon
COO	Cost of ownership
CTM	Cell-to-module
Cu	Copper
Cz-Si	Czochralski silicon
DH	Damp heat
ECA	Electrically conductive adhesive
ECV	Electrochemical capacitance-voltage
EL	Electroluminescence
EVA	Ethylene vinyl acetate
FBC	Front and back contact
FFE	Front floating emitter

FSF Front surface field

FWHM Full width half maximum

GW Gigawatt

HBC Heterojunction back contact

i-PERC Industrial passivated emitter and rear contact

IBC Interdigitated back contact

ICECREM Integrated Circuits and Electronics group Computerized Remedial Education And Mastering

IEA International energy agency

ITRPV International technology roadmap for photovoltaic

IV Current voltage

L&C Laser and cleave

LCOE Levelized cost of electricity

LPCVD Low pressure chemical vapor deposition

mono-Si Monocrystalline silicon

NOAA National oceanic and atmospheric administration

NREL Natural renewable energy laboratory

OIFC Oxidation-induced stacking faults

OPEC Organization of the petroleum exporting countries

PCB Printed circuit board

PECVD Plasma-enhanced chemical vapor deposition

PERC Passivated emitter and rear cell

PERC Passivated emitter and rear cells

PL Photoluminescence

POE Polyolefin elastomer

PSG Phosphosilicate glass

QE Quantum efficiency

QSSPC Quasi-steady-state photoconductance

RJ-TOPCon Rear junction Tunnel oxide passivating contact

RTA Rapid thermal annealing

SDE Saw damage etching

SHJ Silicon heterojunction

SSE Single side etching

TC Thermal cycling

TLS Thermal laser separation

TOPCon Tunnel oxide passivating contact

TW Terawatt

USG Undoped silicate glass

XRD X-ray diffraction

Symbols

η Efficiency

d Thickness

E_a Activation energy

FF Fill factor

H_p Laser pulse energy density

iV_{oc} Implied open-circuit voltage

J Saturation current density

J_{0met} Metal induced recombination current density

J_{ob} Saturation current density of base

J_{os} Saturation current density of surface

J_{sc} Short-circuit current density

N_s Dopant surface concentration

pFF Pseudo fill factor

R_{sh} Sheet resistance

V_{oc} Open-circuit voltage

r_b Base resistivity

r_c Contact resistivity

1

Introduction

1.1. Motivation

With the ongoing expansion of global populations and economic progress, there comes a corresponding surge in the demand for energy. This surge is propelled by factors such as urbanization, industrialization, technological advancements, and improvements in living standards [1]. Fulfilling the energy needs using traditional fossil fuels like coal, oil, and natural gas presents a significant challenge due to their heightened emissions of greenhouse gases, which are primary contributors to climate change [2]. Reports from the National Oceanic and Atmospheric Administration (NOAA) indicate that both land and ocean temperatures have been steadily increasing at an average rate of 0.14 °C per decade since 1880. However, since 1981, this rate has more than doubled, reaching 0.32 °C per decade. The extent of future global warming hinges on the amount of carbon dioxide (CO_2) and other greenhouse gases released into the atmosphere in the coming decades [3]. Given the finite nature of fossil fuels, their eventual depletion may lead to supply disruptions and raise concerns regarding energy security. The Middle East and Latin America and Africa possess the largest share of global oil reserves [4]. Over time, it has been consistently observed that the Organization of the Petroleum Exporting Countries (OPEC) has exerted control over oil prices due to its monopoly position [5] [6]. Also, nations rich in fossil fuel resources often contribute to global energy crises during periods of political instability [7].

An effective mitigation strategy to address the issue of CO_2 emissions while fulfilling the growing global energy demand is to utilize renewable energy sources for electricity generation [10]. According to the main projection of the International Energy Agency (IEA), the annual increase in global renewable power capacity is expected to remain at an average of approximately 305 GW per year from 2021 to 2026 [8]. The fact that global installed PV capacity reached 1 TW by the end of 2022 shows that the IEA's forecast was conservative compared to ITRPV's, which presented a more realistic scenario. According to ITRPV reports, recent trends and the current growth trajectory indicate that if a 25% annual growth rate in PV installations is maintained over the next decade, it could result in an installed capacity of 75 TW by 2050. [11].

1

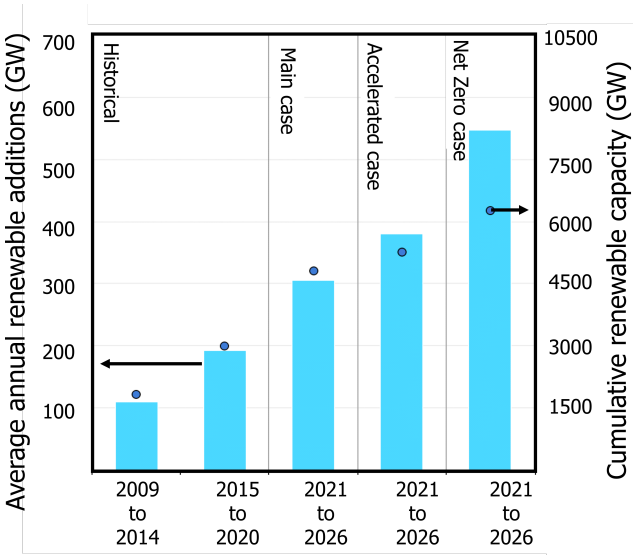

Figure 1.1: Average annual renewable capacity additions and cumulative installed capacity, historical, forecasts and IEA Net Zero Scenario in the period between 2009 to 2026. Figure adopted from [8].

Data presented in Figure 1.1 clearly indicates a significant increase of approximately 60% in the growth rate of renewable energy sources over the past five years. The widespread adoption of renewable energy is driven by several factors, including strong legislative support in over 130 countries, the commitment of countries representing nearly 90% of

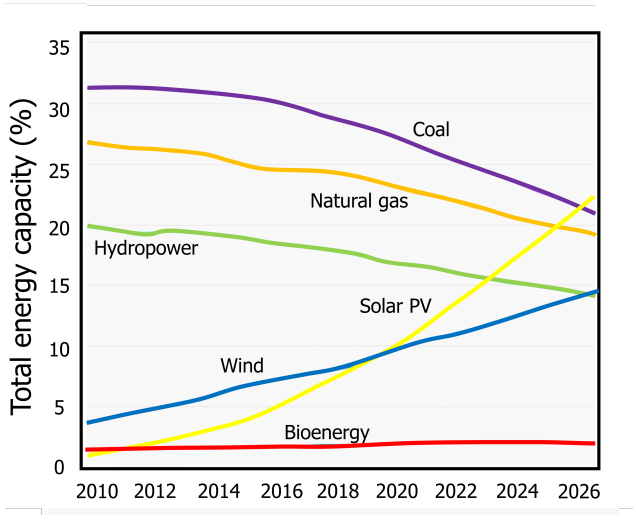

Figure 1.2: Share of cumulative power capacity by technology, in the period between 2010 to 2027. Figure adopted from [9].

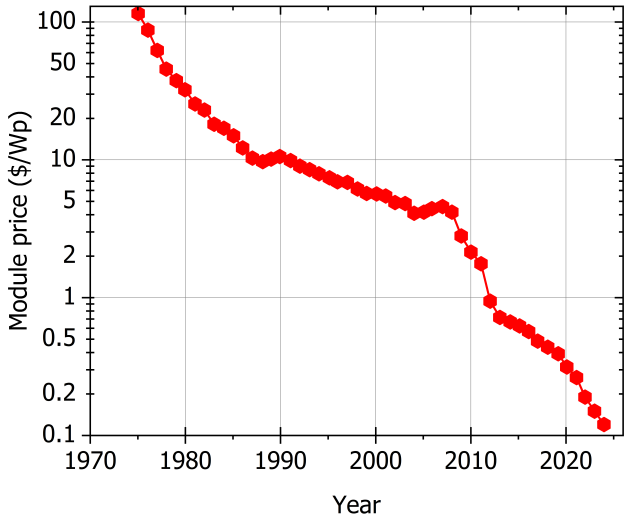

Figure 1.3: Photovoltaic panel prices expressed in US dollar per Watt peak (W_p), adjusted for inflation for the time spam of four decades [15].

global GDP to ambitious net zero goals, and the growing competitiveness of wind and solar photovoltaic (PV) technologies [12].

Figure 1.2 illustrates the distribution of total energy capacity forecasted by the IEA across various technologies from 2010 to 2027 [9]. According to predictions, solar photovoltaic (PV) systems are expected to surpass natural gas by 2026 and coal in terms of installed power capacity by 2027, establishing themselves as the "emperor of the energy market". During this period, there will be a significant increase in the cumulative capacity of solar PV systems, with a projected growth of about 1,500 GW, approximately three times the current capacity. Utility scale solar PV remains the most economically viable option for new energy generation in many countries worldwide, despite increased investment costs due to rising commodity prices [13]. The increasing adoption of distributed solar PV systems, such as rooftop solar installations on buildings, is anticipated to accelerate due to rising retail power costs and increased government support aimed at helping consumers achieve energy cost savings [14].

Figure 1.3 depicts the price of photovoltaic modules per watt peak (W_p) [1] over the time span of 4 decades. In 1975, the initial expense of solar panels was approximately \$115.3 per W_p. However, by 2010, this figure had dropped to \$2.15 per watt, and as of 2021, it has plummeted to a mere \$0.27 per W_p. The latest results from July 2024 show that prices have decreased further to \$0.13 per W_p [16]. This represents a remarkable decline in the cost of a pivotal green technology by nearly 90% over the past decade. The success of PV technology over the years can be attributed to the rapid reduction in solar energy costs, driven by a combination of technological advancements, increased production volume, innovative financing models, and government policies and incentives [17]. With

[1] A watt-peak (W_p) is the maximum electrical energy that a photovoltaic panel can supply under standard test conditions.

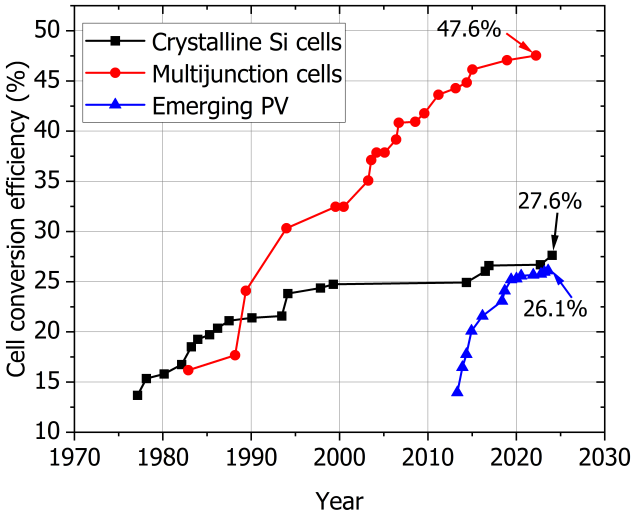

Figure 1.4: The highest confirmed conversion efficiencies of crystalline silicon solar cells, multijunction solar cells and emerging PV solar cells concepts over the last four decades. The data points adapted from National Renewable Energy Laboratory [19].

solar energy becoming more affordable and accessible, it is evident that this renewable energy source will play an increasingly vital role in the global transition to a low-carbon economy [18].

Over the same time span, the conversion efficiencies of various solar cell and module technologies have also improved considerably. Figure 1.4 displays the highest confirmed conversion efficiencies for research cells for a range of photovoltaic technologies, plotted from 1976 to the present as recorded by the National Renewable Energy Laboratory (NREL). While multijunction cells and emerging PV technologies exhibit higher conversion efficiencies and faster learning rates respectively, the predominant technology in the PV industry still relies on crystalline silicon. This is due to their industrial scalability, abundant availability, bankability, and cost-effectiveness [20]. To show the maturity of the technology at industrial level, currently, Longi Company in China produces Heterojunction Back Contact (HBC) solar cells with a recorded efficiency of 27.6% [21], which is only 2.3% lower than the theoretical efficiency of 29.4% for monocrystalline silicon solar cells [22]; while Maxeon company in Canada has reported 24.9% module conversion efficiency also based on the back contacted c-Si technology [23].

To expand the contribution of PV technology to the electricity grid and accommodate rising energy needs, ongoing optimization of solar cells is imperative. This involves either boosting their power conversion efficiency (η) or reducing production costs. This work focuses on developing and optimizing the fabrication of high-efficiency solar cell concepts such as RJ-TOPCon and diffused junction IBC solar cells using cost-effective and industrially viable APCVD technology.

1.2. Dissertation structure

This thesis is divided into 7 chapters:

- Chapter 1: The chapter summarizes the need of renewable energy sources, especially photovoltaic technology to meet the growing energy demands in a sustainable and efficient manner. It also sets the stage for the reminder of the dissertation.
- Chapter 2: The chapter provides an overview on the literature review on various crystalline silicon solar cell concepts. It delves into the working principle and advantages of Atmospheric Pressure Chemical Vapor Deposition (APCVD) technology for depositing doped glass layers and silicon layers. In addition to providing a concise overview of the history and operational principles of solar cells, this section elaborates on the merits and demerits of various crystalline silicon solar cell designs, ranging from conventional AL-BSF to advanced fully passivated contact IBC solar cells.
- Chapter 3: This chapter focuses on investigating and implementing a novel approach for patterning the rear-side of interdigitated back contact (IBC) solar cells using the enhanced oxidation characteristics under the laser doped back surface field (BSF) regions with high phosphorous surface concentrations.
- Chapter 4: In this chapter, high-efficiency IBC solar cells are fabricated using APCVD technology and are compared to the state of the art full-tube diffused industrial ZEBRA® IBC solar cells.
- Chapter 5: This chapter provide insights about the efficiency potential and optimized fabrication process sequence of a TOPCon front-back contact n-type cell concept with a rear junction topology. Also, a novel concept of in-situ annealing of boron doped amorphous silicon layers using APCVD technology is presented.
- Chapter 6: In this chapter, the origin and the effective mitigation strategies for firing-induced depassivation of phosphorous doped n^+ poly-Si layers are studied in detail.
- Chapter 7: This chapter draws the main conclusions from this work and presents a future outlook.

1.3. Author's contribution to photovoltaic community

This doctoral dissertation focuses on developing a cost-effective and yet industrially viable high efficiency solar cells. The following significant contribution to the field have been realised:

- A novel patterning and masking technique for the fabrication of IBC solar cells. The patterning technique capitalizes on the enhanced oxidation properties present under the laser-doped n^+ BSF regions. Post patterning, the retained oxide under laser doped n^+ BSF regions is also utilized as a masking layer for the high temperature BBr_3 diffusion during which the emitter and front floating emitter of the IBC

solar cell are formed. The advantages and drawbacks of employing this patterning technique in fully passivating contact IBC solar cells are also discussed.

- By using the APCVD doped glass layers for forming the doped regions of the IBC solar cells, I was able to demonstrate similar conversion efficiencies as that of the commercially available full-tube diffused ZEBRA® IBC solar cells. The high temperature annealing step in an oxygen (O_2) environment was optimized to perform three functions: (i) drive in dopant of both polarities, (ii) prevent the formation of a boron-rich layer in the case of p^+ doped c-Si, and (iii) grow an in-situ SiO_2 at the Si/dopant glass interface which was later used as an universal passivation stack when capped with a PECVD SiN_x layer for both polarities of the IBC solar cells.

- This work presents an in-situ annealing process to crystallize boron-doped p^+ a-Si layers deposited by APCVD to form boron-doped p^+ poly-Si layers. The in-situ annealing of the p^+ a-Si layers is achieved by fine-tuning the temperature profiles in the post-deposition zones of the APCVD tool. The study demonstrated that the hydrogenation processes during the fast firing play a significant role in enhancing the passivation quality as well as electrical properties of the in-situ annealed p^+ poly-Si layers. The use of this novel in-situ annealing process to form p^+ poly-Si layers layers opens a new horizon for a lean process sequence without the additional high-temperature annealing step for fabricating solar cells concepts based on passivating contact.

- While extensive research has focused on investigating the effects of firing on poly-Si passivating contacts, the origins of this issue and effective mitigation strategies are not well understood. In this chapter, I examine the impact of firing on the n^+ poly-Si passivating contacts used in TOPCon solar cells, ultimately achieving blister-free n^+ poly-Si across a wide range of firing temperatures. For the ex-situ doped n^+ poly-Si, the sequence of annealing followed by doping or vice versa determines the firing stability of the layers. Further I demonstrate that by use of bi-layer stack with low hydrogen content, such as PECVD silicon oxide (SiO_2) or phosphosilicate glass (PSG), between the poly-Si and PECVD SiN_x layers significantly improves the firing stability of the phosphorous doped n^+ poly-Si layers.

2

Review of c-Si solar cell concepts and APCVD technology

This chapter delves into the brief history of crystalline silicon solar cells, their working principle and a review on the various crystalline silicon solar cell concepts that have entered the mainstream photovoltaic industry. The first section briefly describes the evolution of the solar cells from its origin of photovoltaic effect from Alexandre-Edmond Becquerel in 1839 to the first ever silicon solar cells made by D.M. Chapin, C.S. Fuller, and G.L. Pearson in 1954. The second section explains the simplified working principle of solar cells. The third section discusses the dominant architectures of crystalline silicon solar cells. It outlines four specific designs: aluminum Back Surface Field (Al-BSF), Passivated Emitter Rear Cell (PERC), Tunnel Oxide Passivated Contacts (TOPCon) cells, and Interdigitated Back Contact (IBC) cells. In the forth section, the working principle of chemical vapor deposition technique is explained followed by the use of APCVD technology for the deposition of glass and silicon layers.

2.1. Brief history of solar cells.

The history of photovoltaics spans several centuries, but the modern development of solar cells began in the mid-19th century and has since experienced significant advancements [24]. The photovoltaic effect, which is the process of generating electricity from light, was initially observed by French physicist Alexandre-Edmond Becquerel in 1839 while studying electrical phenomena between two electrodes immersed in electrolytes [25]. Thirty years later, during the expansion of electrical communication networks worldwide, W. Smith discovered photo-conductivity in selenium rods [26] and subsequently enabled the premises of an operating solar cell by W. Adams and R. Days [27]. The first functional solar cell based on a copper/selenium film/gold junction was created by C. Fritts in 1883 [28]. Albert Einstein provided a theoretical explanation of the photoelectric effect and photovoltaic effect in 1905 [29], for which he later received the Nobel Prize in Physics. His work helped to lay the groundwork for the understanding of how light interacts with materials to generate electricity. Russel Ohl at Bell telephone's laboratory in the United States discovered the superior performances of silicon with reaching photopotentials up to 0.5 V, much more that selenium or copper oxide previous materials. The first solar cells and modules based on his finding were patented in 1941 [30]. Subsequently extensive research was carried out in Bell Labs over the next decade to further enhance the conversion efficiency of the solar cells [31] based on silicon substrate. The key milestone of efficiencies higher than 5% fixed by the Bell's management for industrial credibility was thus presented in the 6% efficiency famous paper authored in 1954 by D.M. Chapin, C.S. Fuller, and G.L. Pearson [32], which is considered worldwide as the birth of the modern silicon solar cell.

2.2. Working principle of solar cells.

The solar cell operates on the principle of the photovoltaic effect, wherein a potential difference is generated at the junction of two different materials in response to electromagnetic radiation. Figure 2.1 demonstrates the fundamental working principle of solar cells. The functionality of a silicon solar cell can be understood through three primary processes [33]:

1) Generation of charge carriers due to absorption of photons in the materials that form a junction: When photons with energy greater than the absorber's band gap for silicon is 1.12 eV strike on such material, electron-hole pairs are created (point 1 in Figure 2.1). Without an external field, these pairs typically recombine. This phenomenon occurs in the bulk of the absorberer material and at its surfaces (point 2 in Figure 2.1).

2) Separation of the generated charge carriers within the junction: To utilize the energy of electron-hole pairs, semipermeable membranes are essential on both sides of the material, allowing electrons to flow through one membrane and holes through the other. Conventional solar cells achieve this through n and p-type materials (point 3 in Figure 2.1). This phenomenon occurs in the space charge region.

3) Collection of the generated charge carriers at the junction's terminals: Electrical contacts are necessary to extract charge carriers from the solar cells, converting the chemical energy of electron-hole pairs into electrical energy. Electrons that pass through the external circuit (point 4 in Figure 2.1) eventually recombine at the metal-absorber

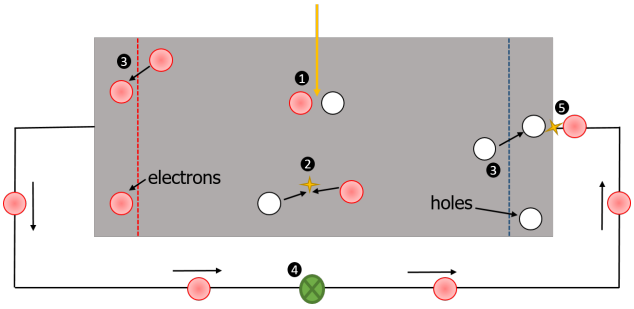

Figure 2.1: A simple solar cell model. Figure adapted from [33]

interface (point 5 in Figure 2.1) . This phenomenon occurs at the terminals.

2.3. Review on crystalline silicon solar cell concepts

This section elucidates the various solar cell concepts that have emerged within the photovoltaic industry. It provides a concise overview of each concept along with their respective significant advancements that have contributed to enhancing conversion efficiency.

2.3.1. Aluminium Back Surface Field (Al-BSF) cell

As early as the 1970s, researchers invented the first Al-BSF solar cells [34]. Due to its relatively simple and cost-effective manufacturing process the standard aluminum back surface field (Al-BSF) technology dominated the photovoltaic market for four to five decades [35]. A simplified cross-section of an industrial Al-BSF solar cell is depicted in Figure 2.2. It consist of a p-type multicrystalline (mc) or monocrystalline (Cz) silicon substrate with a $POCl_3$ tube diffused phosphorous doped n^+ emitter layer on the front side and sintered aluminium on the rear side acting as a p^{++} doped Al-BSF layer. The textured front side of the solar cells is passivated with plasma enhanced chemical vapor deposition (PECVD) silicon nitride (SiN_x) layer and contacted using screen printing and firing-through silver (Ag) pastes.

There has been a steady improvement in the conversion efficiencies of Al-BSF solar cells. Key advancements made in research and development are highlighted in this discussion. Although the initial silicon solar cells were produced on an n-type substrate, the photovoltaic industry shifted to p-type substrates primarily due to their widespread use in space applications [36]. It was noted that lightly doped p-type substrates exhibited better space radiation hardness than n-type substrates [37]. In the early 1970s, the technique of sintering Al at high temperatures was introduced, leading to the formation of highly doped p^{++} regions beneath the metal contacts at the silicon/metal interface, known as Al-BSF [34]. The boundary between the heavily doped and lightly doped regions forms a high-low junction. This interface generates an electric field, creating a barrier to the flow of minority carriers towards the rear surface. As a result, the concentration of minority carriers stays elevated within the device's bulk, effectively passivating the rear surface and consequently boosting the open-circuit voltages at device level. Afterward, by

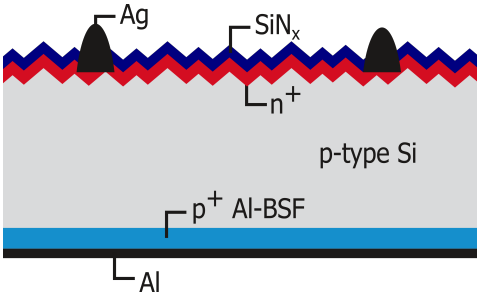

Figure 2.2: Schematic representation of Al-BSF solar cell.

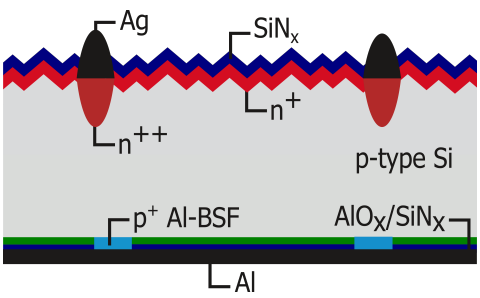

Figure 2.3: Schematic representation of PERC solar cell.

integrating photolithography technology and improvements in the silver paste properties, thinner fingers could be printed in closer proximity, thus obviating the necessity for a heavily phosphorus-doped n^{++} emitter on the front side, consequently enhancing the short wavelength response. Surface texturing through anisotropic etching significantly increased solar cell conversion efficiencies by reducing reflection losses and enhancing light trapping [38]. Various passivation layers were tested to serve as the antireflection coating (ARC) such as thermally grown silicon oxide (SiO_2) and titanium oxide (TiO_2). Eventually, hydrogenated PECVD SiN_x layer was chosen due to its capability to provide field effect passivation, along with hydrogenation of the substrate layer, thereby enhancing solar cell voltages [39]. All the above mentioned process optimizations contributed in improving the conversion efficiency in Al-BSF cells. However, only the cost-effective and scalable methods were implemented in industrial devices.

Although Al-BSF cells may be easily manufactured on a large scale and have demonstrated efficiencies as high as 20.3% [40], their efficiency is fundamentally constrained by the comparatively high recombination rate at the rear metal contact caused by the presence of full-area aluminum and the parasitic absorption of infrared radiation at the aluminum contact.

2.3.2. Passivated Emitter and Rear Cell (PERC)

The inception of the Passivated Emitter and Rear Cell (PERC) technology, pioneered by the University of New South Wales (UNSW), can be traced back to 1983 [41]. Since 2015, PERC solar cells have risen to prominence as the primary photovoltaic technology [42]. The widely recognized rear side passivation plays a crucial role in reducing recombination and enhancing the open-circuit voltage, thus facilitating further efficiency improvements. The unique characteristics of the PERC design effectively tackle optical and recombination losses associated with the rear side. The combination of surface passivation using dielectric layers and a reduction in the metal/semiconductor contact area leads to decreased rear surface recombination. A simplified cross-section of the industrial PERC solar cell is depicted in Figure 2.3, consisting of a p-type monocrystalline silicon substrate with a textured front side and a polished rear side. A lightly phosphorus-doped n^+ emitter is present on the non-metallized front side, while a selective laser phosphorus-doped n^{++} emitter lies beneath the metallized front side. The front side is passivated with a PECVD

SiN_x layer and metallized using screen printing fired through Ag pastes. The rear side is passivated with an AlO_x and SiN_x stack. Laser ablation locally opens the dielectric stack, forming local Al-BSF upon contact with Al paste.

Since the early 1980s, there has been a consistent enhancement in the conversion efficiencies of PERC solar cells. Key advancements made in research and development are highlighted in this discussion. Techniques such as inverted pyramids via photolithography and random pyramid texturing were introduced to minimize reflection losses and enhance light trapping by scattering light across three dimensions through pyramid facets [43]. Initially, thermally generated SiO_2 was utilized to passivate the rear side in early PERC solar cells [41]. Reflection enhancement on the rear side was achieved by introducing a dielectric layer with a low refractive index between the silicon (Si) and metal. Further reduction in recombination current density on the rear side was achieved by integrating an aluminum oxide (AlO_x) and SiN_x dielectric layer stack, capitalizing on the low defect level at the interface [44]. Photolithography is used to locally open the dielectric layer, with evaporated Al contacts formed in these regions, constituting only 1% of the rear side area. The fraction and spacing of the rear contacts counteract recombination and resistance losses [43]. In the early 20^{th} century, the process of local opening for Al-BSF formation shifted from complex photolithography to laser processing [45], while industrially feasible screen printing replaced evaporated contacts for metallization [46]. The significant drop in wafer prices prompted a shift from multi-crystalline to mono-crystalline substrates. Subsequently, thinning the silicon wafer well below the industry-standard 160 μm , in principle reduced both manufacturing cost and Capital expenditures (Capex) [47]. The incorporation of the selective emitter (SE) approach [48], utilizing laser doping [49], is beneficial for enhancing the passivation and contact properties on the front side of PERC solar cells. With selective emitter, two key issues are addressed: firstly, a heavily diffused emitter just beneath the screen-printed metal contact reduces contact resistance and metallization-induced recombination losses; secondly, a lightly doped phosphorus emitter in the non-metallized regions ensures a favorable blue response and lowers emitter recombination. All the above mentioned process optimizations contributed in improving the conversion efficiency in PERC solar cells. However, only the cost-effective and scalable methods were implemented in industrial devices.

With the integration of selective emitter on the front side and an AlO_x passivation layer on the rear side, coupled with high-quality Gallium (Ga) doped substrate material [50], PERC solar cells have showcased efficiencies exceeding 23.5% at the industrial level [51]. Nonetheless, the efficiency of PERC technology is constrained by recombination losses at the metal-semiconductor interface and under the heavily doped emitter regions [52].

2.3.3. Tunnel Oxide Passivated Contacts (TOPCon) cells

Since the early 21^{st} century, there has been steady annual progress in cell efficiency, typically increasing by 0.5% to 0.6% per year [53]. To meet the growing demands for efficiency and tackle design challenges in PERC solar cells, the industry has shifted towards concepts like carrier-selective passivating contact solar cells such as TOPCon solar cells. These concepts involve physically separating the heavily doped regions and metal contacts from the silicon substrate [54]. Though the concept of using polysilicon layer under the contacts

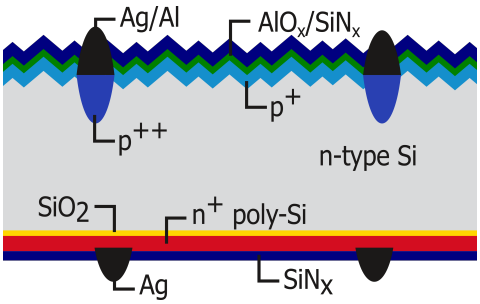

Figure 2.4: Schematic representation of a front junction (FJ) TOPCon solar cell.

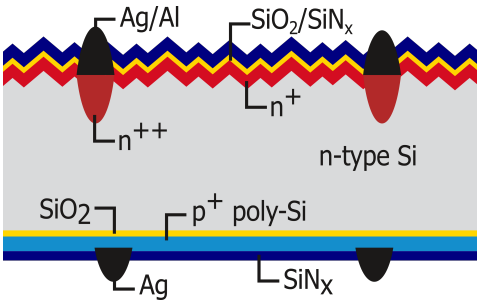

Figure 2.5: Schematic representation of a rear junction (RJ) TOPCon solar cell.

to reduce recombination in the silicon solar cells was established in the early 1980's in Van Overstraeten et al. [55], Green et al. [56] and Yablonovitch et al. [57] it was actually SunPower company in the year 2010 that utilized this concept on their industrial third generation high-efficiency IBC solar cells [58]. Subsequently the first hybrid cell structure with a diffused front emitter and poly-Si/SiO_2 rear contact was published by Feldmann et al. [59] in 2013 and coined this cell concept as TOPCon. Since the inception of the TOPCon solar cell concept, a phosphorus-doped polysilicon layer has been traditionally used due to its excellent passivation quality and low contact resistivity.

A simplified cross-section of an industrial TOPCon solar cell, as illustrated in Figure 2.4, comprises an n-type monocrystalline silicon substrate with a textured front side and polished rear side. To create the boron-doped p^+ emitter on the front side, tube-diffused BBr_3 diffusion is utilized, along with a selectively heavily doped p^{++} region under the front metal contacts formed using laser doping. The front side is passivated with an AlO_x) and SiN_x stack and metallization using screen printing fired through silver-aluminum (Ag-Al) paste. On the rear side, there is a thin interfacial oxide capped by a phosphorus-doped n^+ poly-Si layer acting as a BSF layer. This SiO_2/poly-Si stack serves as a passivating contact layer, topped with a PECVD SiN_x layer and contacted using firing-through Ag paste. The Figure 2.5 depicts the cross-sectional view of the RJ-TOPCon solar cells. In this study, we employ an n-type substrate for the RJ-TOPCon configuration, meaning the cell has a p^+ poly-Si/SiO_2 stack on the rear side acting as a rear emitter and a $POCl_3$ diffused n^+ front surface field (FSF), along with a selectively laser-doped n^{++} region under the front metal contacts. Further details about the advantages of this architecture over conventional TOPCon solar cells are elucidated in chapter 5.

There has been a consistent enhancement in the conversion efficiencies of TOPCon solar cells. Key advancements made in research and development are highlighted in this discussion. The TOPCon process routes consist of the process steps that are either fully/partly transferable from its predecessor i.e. PERC cell, with inclusion of few extra process steps that are necessary to increase the conversion efficiency [54]. TOPCon solar cells have showcased remarkably high conversion efficiencies, surpassing 25% at both laboratory and industrial scales [51]. Some distinctive features of TOPCon solar cells are outlined herein. In contrast to its predecessor, TOPCon solar cells utilize phosphorous-doped n-type substrate material. Several driving factors for this transition include reduced sensi-

tivity to metal contaminants, higher minority carrier lifetimes, decreased degradation, improved low-light performance, and a lower temperature coefficient[60]. A passivating contacts concept consists of two primary components: (i) a heavily doped polysilicon layer, and (ii) a thin interfacial oxide layer. The heavily doped polysilicon layer, typically with active doping concentrations ranging from 1 x 10^{20} to 1 x 10^{21} cm^{-3}, diminishes metal-polysilicon recombination current density and enhances passivation of field-effect phenomena. The interfacial oxide, ranging in thickness from 1 to 3 nm provides the chemical passivation, effectively shields the silicon substrate surface, preventing dopant movement from the polysilicon layer into the c-Si absorber [59]. These characteristics enhance the passivation quality of the polysilicon/SiO_2 stack, resulting in reduced recombination current density and consequently higher V_{oc} values compared to the PERC concept.

The TOPCon solar cell efficiency potential is majorly limited by the front side metal induced recombination. To address this, the concept of laser-doped selective emitter has been introduced, aiming to separate passivation regions from contact regions on the front side [61]. These selective emitter layers can be achieved either through selective laser doping on the BBr_3 boron diffused junction [62] or by patterning heavily doped p^+ poly-Si layers [63] beneath the front contacts.

More recently, laser-enhanced contact optimization (LECO) has been used as a post-firing treatment to improve the fill factor (FF) of solar cells while maintaining high open-circuit voltage (V_{oc}) and short-circuit current (J_{sc}). Laser-Enhanced Contact Optimization (LECO), was patented by Cell Engineering GmbH in 2016. LECO is an advanced laser sintering technique designed to enhance the contact between metal electrodes and silicon wafers in solar cells. During the LECO process, the laser is used for non-destructive carrier injection, with the process driven by the current induced by LECO. This treatment takes place after the rapid firing of the screen-printed solar cell. As a result of LECO treatment, the contact resistance of the solar cell is significantly reduced, allowing for effective contact even on low-doping emitters [64].

The as-deposited amorphous silicon layers require a high temperature annealing step for crystallizing into poly-Si layers [65] and simultaneously active the dopants within the poly-Si layer [66]. While certain recent findings have shown that annealing of the poly-Si layer can also be carried out through in-situ annealing during APCVD layer deposition [67], flash lamp annealing [68], and annealing during fast-firing [69], thus negating the necessity for a high thermal budget annealing step and reducing the cost of ownership (COO) for TOPCon solar cells.

TOPCon solar cells represent a notable success story within the photovoltaics industry, transitioning from laboratory to industry in less than a decade, primarily due to their exceptional passivation quality on the rear side, consequently elevating the solar cell's V_{oc} beyond 710 mV. As TOPCon solar cells remain in the early stages of development, further optimization is anticipated to enhance efficiency and reduce costs. Despite being considered the front-runner in the PV industry, one of the primary drawbacks associated with TOPCon is its dual-sided contacts. These contacts lead to optical shading losses and parasitic absorption losses in the front metallization, consequently diminishing the short-circuit current density J_{sc} at the device level [70].

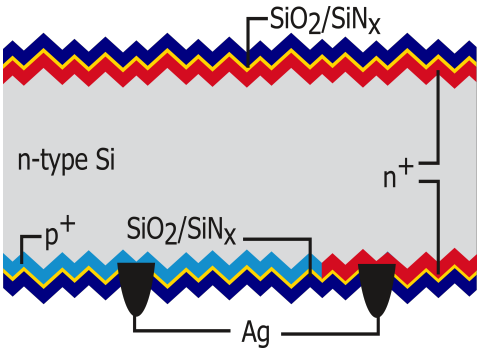

Figure 2.6: Schematic representation of diffused junction IBC solar cell.

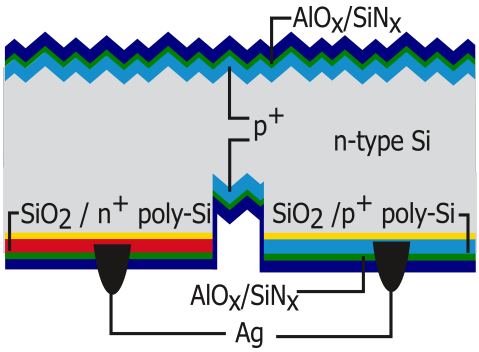

Figure 2.7: Schematic representation of passivating contacts IBC solar cell.

2.3.4. Interdigitated back contact (IBC) cells

The first silicon solar cell was produced in 1954 was a back contact solar cell concept. It was realized on an n-type substrate and had an efficiency of 6.35% [32]. Due to the high fabrication costs, in the nascent stages, IBC cell design was optimized for concentrator application to cope with the high intensities of incoming energy fluxes and the related high current densities [71]. Due to its inherent advantages, this cell architecture was later adapted for 1 sun applications [72]. In the IBC cell architecture, contacts for both positive and negative electrical polarities are placed on non-illuminated side of the solar cell. The most obvious advantage of IBC cells over conventional both sides contact solar cells is the elimination of any optical shading losses caused by the metal finger and busbars on the front side, allowing the solar cells to boost a higher J_{sc}. A more comprehensive range of front surface texturing and light trapping schemes could be adopted on the front surface of the IBC structure, as there is no need for heavily doped regions as is the case for the both sides contacted solar cells [73]. Another considerable advantage is the reduced complexity of cell interconnection inside the module [74]. Also the design architecture is perfect for mechanically stacked tandem cells with higher bandgap technologies, like perovskites, in a three and four-terminal configuration [75].

The ZEBRA technology is a diffused junction IBC solar cell developed in ISC Konstanz. A simplified cross-section of the ZEBRA solar cell is demonstrated in Figure 2.6, comprising an n-type monocrystalline silicon substrate. The front-surface-field (FSF) and the back-surface-field (BSF) as well as the emitter regions are formed using industrial-size quartz tube furnace diffusion utilizing $POCl_3$ and BBr_3 source respectively. A Laser is used in order to locally ablate the SiN_x diffusion barrier on the rear side in order to form the p^+/n^+ patterning. The in-situ grown SiO_2 during the high temperature $POCl_3$ and BBr_3 diffusion is subsequently capped with a PECVD SiN_x layer to passivate both p^+ and n^+ doped regions of the solar cells. Contact formation is achieved using screen printed firing through Ag paste. Due to the diffused junction configuration, ZEBRA solar cell is technology is limited to 705 mV.

The poly-ZEBRA technology is a fully passivating contact IBC solar cell developed in ISC Konstanz. A simplified cross-section of the poly-ZEBRA solar cell is depicted in

Figure 2.7, features an n-type monocrystalline silicon substrate. It consists of a lightly boron-doped diffused junction p^+ front floating emitter (FFE) on the textured front side. Passivating contacts stack, comprising both p^+ and n^+ doped carrier-selective layers (SiO_2/p-poly Si and SiO_2/n-poly Si stacks), are deposited on the flat etched Si substrate, with the textured gap region etched in-between, which is subsequently lightly boron diffused to form a n-p^+ c-Si junction that separates the differently doped poly-Si regions. The patterning on the rear side is accomplished using laser processing. Both p^+ and n^+ polarities are capped with a PECVD AlO_x/SiN_x stack, while rear-side metallization is realized through screen-printed firing of Ag pastes.

IBC solar cells, whether with diffused junctions or featuring passivating contacts, have demonstrated remarkably high conversion efficiencies, surpassing 26.5% at both laboratory [76] and industrial scales [77]. Some distinctive features of IBC solar cells are highlighted here. Since both polarities are present on the rear side there is a definite need for patterning step. The early IBC solar cells, developed in the 1980s and 1990s utilized photolithography techniques for rear-side patterning, while alternative methods such as inkjet patterning, aerosol jet printing, PECVD deposition on glass-based shadow masks, and laser patterning are now widely adopted, with the industry favoring laser patterning for its high throughput and cost-effectiveness. Despite having diffused junctions, IBC solar cells benefit from a higher short-circuit current density (J_{sc}) compared to industrial TOPCon solar cells. However, these IBC cells are limited in open-circuit voltage (V_{oc}), with the best values ranging from 700 to 705 mV, even with optimal passivation stacks. Therefore, the ultimate evolution for industrial crystalline single-junction solar cells would involve passivating contacts realized on the IBC architecture (TOPCon IBC solar cells) to achieve V_{oc} exceeding 720 mV. Meanwhile, all the developments mentioned for TOPCon solar cells, such as flash lamp annealing, LECO, and in-situ annealing, could also be incorporated into TOPCon IBC solar cells.

To fabricate the doped regions in the various solar cell concepts discussed earlier, a diverse range of deposition processes can be utilized. This study focuses on employing APCVD technology to deposit doped glass and doped silicon layers for high-efficiency solar cell concepts, such as diffused junction IBC solar cells and RJ-TOPCon solar cells. Table 2.1 illustrates the distinct characteristics of different chemical vapor deposition (CVD) and physical vapor deposition (PVD) methods used for depositing amorphous silicon films. Compared to the LPCVD method, the PECVD approach has advantages in superior deposition rates, less wrap-round deposition, and equipment-related consumables [78]. Though the potential of APCVD technology is to be tested at industrial level, Table 2.1 clearly shows that APCVD technology presents a superior alternative to PECVD technology because it offers lower fabrication cost [54] and yields a higher level of crystallinity in the as-deposited layer.

2.4. Deposition of glass and silicon layers using APCVD

Chemical vapor deposition (CVD) is a deposition process in which vapor precursors undergo dissociation and/or chemical reaction to form a stable solid product in an activated environment, such as heat, plasma, or light. If the reaction occurs in the gas phase, known as a homogeneous reaction, it results in the formation of fine particles. Conversely, if the reaction takes place on or near a heated substrate, termed a heterogeneous reaction, it

Property	LPCVD	PECVD	APCVD	PVD	Evaporation
In-situ doping	Possible but lowers the deposition rate	Possible and reaction rate is not hindered	Possible and reaction rate is not hindered	Possible but lowers the deposition rate	Not possible
Single sided deposition	Not possible	Pseudo single sided	Pseudo single sided	Conformal single sided	Conformal single sided
Deposition mode	Batch mode	Both modes	Inline mode	Inline mode	Batch mode
Ease to integrate in industry	Historically used	Currently used	Has potential	Has potential	Not industrial
Nature of deposited layers	Nano crystalline poly-Si	Amorphous	Nano/micro crystalline poly-Si	Amorphous	Amorphous

Table 2.1: Comparison of different silicon layer deposition techniques based on various characteristics.

produces a dense film. A combination of homogeneous and heterogeneous reactions typically results in the formation of a porous film. In general, the CVD technique comprises three main components: i)Chemical vapor precursor supply system: This system is responsible for generating vapor precursors and delivering them to the reactor. ii) CVD reactor: The primary role of the CVD reactor is to heat the substrate or the environment to the deposition temperature. The reactor includes a reaction chamber, often equipped with a load-lock for transporting and placing the substrate, a substrate holder, and a heating system with temperature control for depositing films and coatings. iii) Effluent gas handling system: This component consists of a section for neutralizing exhaust gases and a vacuum system to maintain the required reduced pressure for CVD processes performed at low pressure or high vacuum during deposition.

The operational principle of all CVD techniques can be outlined as follows [79]:

- Generating gaseous reactants/precursors through evaporation or sublimation.
- Transporting gaseous reactants to the reactor.
- Initiating a gas-phase reaction of the precursor in the reaction zone to generate reactive intermediates.
- Adsorbing the reactants onto the heated substrate surface and facilitating heterogeneous chemical reactions at the gas-solid interface, resulting in deposit formation or by-product generation.
- Facilitating surface diffusion of the deposits along the heated substrate to establish nucleation and crystallization centers, and promoting film growth through additional surface chemical reactions.

- Removing gaseous by-products from the boundary layer via diffusion and convection.
- Desorbing and transporting the by-products and remaining fragments of unreacted species away from the reaction zone.

Historically, APCVD technology was regarded as the best suited technology for the deposition of doped and undoped glass layers due to its large reaction rates and simplicity of the deposition technique. Companies such as Sunpower and LG used APCVD technology extensively in their mass-production of the high efficiency IBC solar cells [58]. A simplified cross-section of APCVD system and the APCVD nozzle is depicted in Figure 2.9. APCVD technology has demonstrated deposition rates exceeding 100 nm/min making the process very attractive. Also since, APCVD depositions take place at atmospheric pressure their operational and maintenance costs are also lower. In this work, we utilized the SCHMID APCVD Belt-Transport System [80] for depositing boron doped amorphous/polycrystalline silicon layers while SCHMID APCVD Roller-Transport System for depositing silicon oxide, phosphosilicate glass and borosilicate glass layers. The SCHMID APCVD systems are designed to have multiple deposition chambers, thereby enabling more than one layer in a single pass. Both Belt and Roller-Transport system of an APCVD system can be categorized into three main zones, namely: pre-deposition zones, deposition zones and post-deposition zones. The wafers are gradually heated in the pre-depositon zones to reach the desired temperature by the time it reaches the deposition zone. Subsequently the temperature profile gradually ramps-down in the post-deposition zones before the samples come out. The injector head which is present in the deposition zone consists of a line source with supply of (SiH_4, B_2H_6, PH_3 and N_2) gases. The N_2 gas flow in the deposition chamber assures an atmosphere with minimal oxygen (O_2) content.

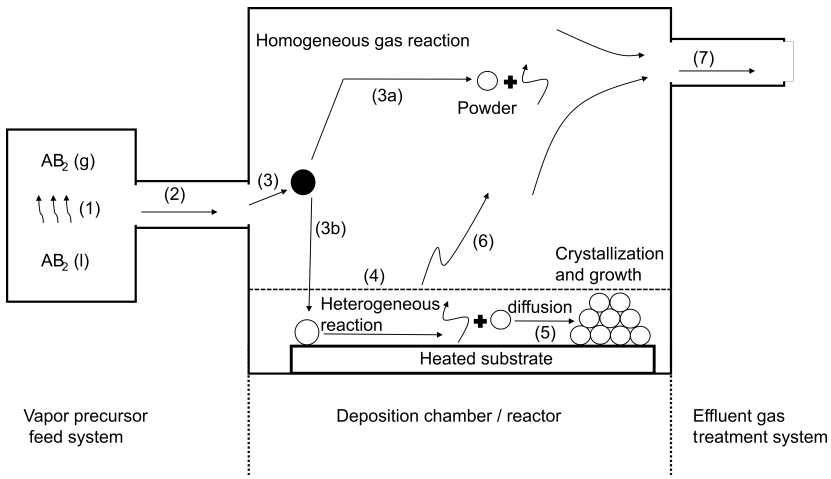

Figure 2.8: A schematic illustration of the key CVD steps during the deposition process. Figure adopted from [79]

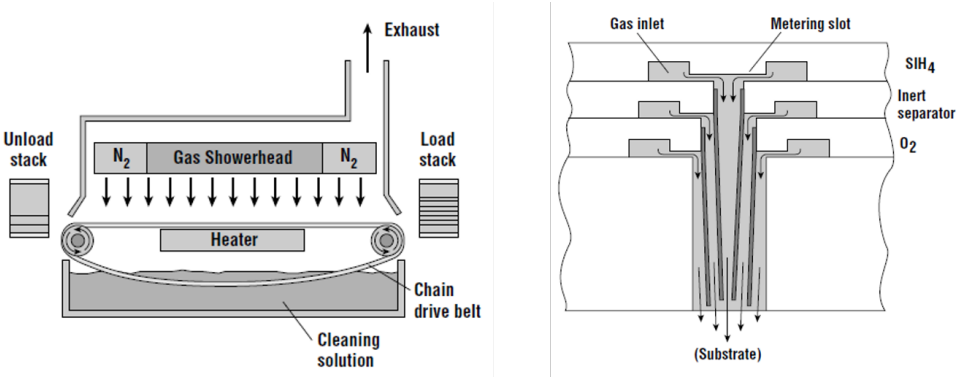

Figure 2.9: (a) Simple continous-feed atmospheric pressure reactor (APCVD). (b) Showerhead design used to minimize deposition at the nozzle by maintaining an inert curtain between the reactants.

One of the major drawback of APCVD technology is the particle formation during the chemical reaction. The particle formation in the gas phase can be regulated by adding a sufficient amount of inert gases such as nitrogen. Though studies have shown that growth rate of the particle is slow, upon processing of hundred's of wafers, the particles eventually become large enough to flake off and fall on the wafer surface [81].To avoid such scenarios, shower heads are installed, which may be segmented to keep the reactant gases separated until they are injected into the chamber. Figure 2.9b shows a shower head arrangement designed to reduce this problem.

Some of the earliest CVD processes were done at atmosphere pressure (APCVD) because of the large reaction rates and the simplicity of the CVD system, particularly for the deposition of dielectrics [81]. When the O_2 to SiH_4 gas flow is at least 3:1 stoichiometric, SiO_2 layer can be deposited at a substrate deposition temperature of 600-650 °C. The interaction between SiH_4 and O_2 is highly reactive and produces very volatile mixture. Without sufficient flow of N_2 gas, a homogeneous gas phase reaction would occur, resulting in poor morphology of the deposited layer. In this work the APCVD SiO_2 was used for a capping layer to prevent the doped glass layers from interacting with the environment due to their hygroscopic nature. Also the APCVD SiO_2 was used as a passivation layer for both p^+ and n^+ polarities as presented in chapter 3 and 4.

Phosphosilicate glass (PSG) films, or phosphorus-doped SiO_x films, can be deposited by adding phosphine (PH_3) to the process described above for SiO_2. The substrate temperatures are similar to that of the APCVD SiO_2 i.e. 600-650 °C. The phosphorus concentration within APCVD PSG films is controlled by varying the temperature, gas flow rates and roller belt deposition speed. The PSG layer with different thickness and phosphorous dopant concentration (wt.%) were studied in this thesis and shortlisted based on the optimal electrical and passivation properties. Depending of the cell architecture, the PSG layer was used to form the n^{++} back surface field (BSF) and n^+ front surface field (FSF) in case of IBC solar cells 4 and n^+ FSF in case of RJ-TOPCon solar cell as presented in chapter 5.

Borosilicate glass (BSG) films, or boron-doped SiO_x films, can be deposited by adding diborane (B_2H_6) to the process described above for SiO_2. The substrate deposition tem-

perature was lower for the BSG deposition in the range of 450-500 °C. And similar to PSG, the boron concentration within these glass and silicate films is highly controllable. In this work, BSG is considered as a boron dopant source for c-Si solar cells. The BSG layer was used to form the p^{++} emitter and p^{+} front floating emitter (FFE) in case of diffused junction IBC solar cells as presented chapter 3 and 4.

The deposition of boron doped amorphous/polycrystalline silicon layers is carried out in the thermal dissociated SiH_4 and B_2H_6 in the deposition chamber which would precipitate as an amorphous silicon layer on the hot moving substrate [82]. The substrate deposition temperatures are in the range of 700-750 °C, comparatively higher than that for the glass layers. The boron concentration within the boron doped amorphous silicon films is controlled by varying the temperature, gas flow rates and roller belt deposition speed. The crystallinity of the boron doped amorphous silicon films is controlled by altering the temperature profiles mainly in the post-deposition zones. The boron doped p^{+} poly-Si layer forms the emitter layer in our RJ-TOPCon solar cell fabrication as presented in chapter 5.

3

Novel approach for structuring IBC solar cells

Interdigitated back contact (IBC) architecture can yield among the highest silicon-wafer-based solar cell conversion efficiencies. Since both polarities are realized on the rear side, there is a definite need for a patterning step. Some of the most common patterning techniques involve photolithography, inkjet patterning, and laser ablation. This work introduces a novel patterning technique for structuring the rear side of IBC solar cells. Laser doping is performed utilizing phosphosilicate glass (PSG) as a precursor layer to form local n^{++} c-Si regions with high phosphorous surface concentration (N_s). *Upon wet thermal oxidation, we grow 2.6 times thicker SiO_2 under the laser-doped regions than the non-laser-doped regions due to enhanced oxidation characteristics. A step etching in an acidic solution is performed, and the etching process is interrupted when the thin SiO_2 layer under the non-laser-doped regions is removed completely. The thick SiO_2 under the laser-doped BSF region acts as an etch stop layer due to the high etch selectivity of SiO_2 compared to c-Si in an alkaline texturing bath, thereby patterning the rear side of the IBC solar cells. After texturing, the remaining SiO_2 layer beneath the laser-doped regions is utilized as a diffusion barrier for the subsequent boron diffusion process, during which the emitter region is formed on the non-lasered regions. Proof-of-concept solar cells were fabricated using this novel patterning technique with a maximum conversion efficiency of 20.41 %.*

This chapter is based on the following publications: **V. V. Kuruganti**, O. Isabella, and V. D. Mihailetchi, "Structuring Interdigitated Back Contact Solar Cells Using the Enhanced Oxidation Characteristics Under Laser-Doped Back Surface Field Regions", physica status solidi (a) (2024): 202300820.

3.1. Introduction

The first silicon solar cell was produced in 1954 with IBC architecture. It was realized on an n-type substrate and had an efficiency of 6.35% [32]. In the nascent stages, IBC cell design was optimized for concentrator application to cope with the high intensities of incoming energy fluxes and the related high current densities [71]. Due to its inherent advantages, this cell architecture was later adapted for one solar application [72]. In the IBC cell architecture, contacts for both types of polarities are placed on the non-illuminated side of the solar cell. The most obvious advantage of IBC cells over conventional both-side contact solar cells is the elimination of any optical shading losses caused by the metal finger and busbars on the front side, allowing the solar cells to boast a higher short-circuit current density (J_{sc}). A more comprehensive range of front surface texturing and light trapping schemes could be adopted on the front surface of the IBC structure, as there is no need for heavily doped regions like in the case of both side-contact solar cells [73]. Another considerable advantage is the reduced complexity of cell interconnection inside the module [74]. The design architecture is perfect for mechanically stacked tandem cells with higher bandgap technologies, like perovskites as top cells, in a three-terminal configuration [75]. Research groups and companies use IBC architecture worldwide to make high-efficiency solar cells because of the above-mentioned benefits. In research and development, Kaneka Corporation has reported a conversion efficiency of 26.7 % [83] for its heterojunction IBC, and ISFH has reported a conversion efficiency of 26.1 % on its POLO IBC solar cells [84]. At the industrial scale, Longi has reported a recorded efficiency of 27.1% on its Heterojunction Back Contact (HBC) solar cells [21] while SunPower has reported an efficiency of 25% [85] on the SunPower X-Series technology, and SPIC reported an efficiency above 23.5% on its low-cost bifacial IBC ZEBRA technology [86].

Since both polarities are located on the rear side of the IBC solar cell concept, there is a definite need for a patterning step. Some of the first IBC solar cells developed in the early 1980s and 1990s [87] used photolithography techniques for patterning on the rear side. Photolithography is a well-established technique that uses light to produce minutely patterned thin films of suitable material over a substrate to protect selected regions (mask) during the subsequent etching, deposition, or implantation process. Using photolithography for patterning the IBC solar cells, Franklin et al. [88] have reported an efficiency of 24.4%. The fabrication of this cell had as many as four Photolithography steps. Besides photolithography, alternative patterning techniques include inkjet patterning [89] of a resist layer followed by wet chemical etching and aerosol jet printing [90]. All the methods mentioned above require multiple wet bench processing steps and sophisticated equipment making them not viable for application in the PV industry. In recent years, Mertens et al. [91] have shown an elegant way of locally depositing one polarity of the poly-Si layer using Plasma enhanced chemical vapour deposition (PECVD) through a glass-based shadow mask.

Laser ablation has been one of the most successful approaches for patterning the rear side in IBC solar cells [86], [92]. The use of the laser ablation technique for the fabrication of IBC solar cells has been reported by Engelhart et al. [92] and O'Sullivan et al. [93] using a picosecond laser for the ablation of dielectric layers like Silicon oxide (SiO_2). In addition, Kronz et al. [94] demonstrated Silicon Nitride (SiN_x) ablation using a nanosecond laser. However, laser ablation can cause unintentional laser-induced damage such as surface

melting, heat-affected Zone, microcracks, and point defects on the underlying silicon layer, negatively affecting solar cell performance [95]. Hence an additional wet bench step is introduced for laser-induced damage removal before the subsequent high-temperature step.

Morris et al. [96] presented an innovative technique using laser doping [97] to enable local doping of IBC cells without masking layers. The laser doping was used to form the local n^{++} BSF and a local p^{++} emitter with high spatial resolution without the necessity of any masking. Alternatively, Franklin et al. [88] and Zieliński et al. [98] have used laser doping to form one polarity and laser ablation for the patterning and aligned contact formation using the nanosecond *(ns)* laser.

In this work, we use the enhanced oxidation rates under locally laser-doped regions for patterning the rear side of IBC solar cells. We perform laser doping on $POCl_3$ diffused samples using PSG glass as a precursor layer. Due to the higher oxidation rates under the heavily doped n^{++} regions [99, 100], upon wet thermal oxidation at 850 °C for 30 minutes, we were able to grow a thick SiO_2 layer of 125 nm under laser-doped regions, as compared to a thin SiO_2 layer of only 48-nm under on the non-laser doped regions. The selectivity in the thickness of the SiO_2 layer under lasered and non-lasered regions was used for patterning the rear side of the IBC solar cells. It was also observed that the remaining SiO_2 layer under the laser-doped regions after patterning had sufficient thickness to act as a dopant barrier for the subsequent boron diffusion process, making the processing of the IBC solar cells robust and streamlined.

3.2. Experimental and characterization

All the process equipment used was industrial or industrial-like, such as Centrotherm tube diffusion furnaces for BBr_3 diffusion, $POCl_3$ diffusion and thermal oxidation. Hydrofluoric acid etching was performed in a 2% HF solution, and alkaline etching was carried out on a batch-type RENA wet bench. Local laser treatment was performed on a frequency-doubled Nd:YVO_4 nanosecond *(ns)* pulse laser with a wavelength = 532 nm industrially feasible high throughput tools. The SiN_x layers were deposited using the Centrotherm PECVD system and firing in a Centrotherm fast-firing furnace.

3.2.1. Sheet resistance control samples

The R_{sh} samples were used to investigate the influence of different laser parameters on the electrical properties and the subsequent oxide growth rates under the laser-doped areas. We used the M2 wafer format, <100> p-type Czochralski wafer (Cz) with a thickness = 180 ± 10 µm and a base resistivity = 1 ± 0.5 Ω.cm. The samples underwent saw damage etching and Piranha cleaning before the high-temperature $POCl_3$ tube diffusion. For this study, the $POCl_3$ recipe was optimized only to have a deposition phase without any high-temperature drive-in. Due to the lack of the drive-in phase in $POCl_3$ diffusion, most of the phosphorous is present in the PSG layer. All samples were then laser-treated by a frequency-doubled Nd:YVO_4 nanosecond *(ns)* pulse laser with a wavelength = 532 nm. A pulse duration = 60 *ns* - 160 *ns* is used to create the laser-doped regions with various laser settings. The laser has a flat top profile with a rectangular spot size = 300 x 600 μm^2. The samples were cleaned in a 2-vol% HF solution to remove the precursor glass layer before

the subsequent high-temperature wet thermal oxidation process for a duration of 30 minutes at 850 °C. The thickness of the SiO_2 layer under the different laser doping settings was carried out with an SE800-PV ellipsometer. The SiO_2 was etched in a 2-vol% HF acid solution at room temperature to evaluate the electrical characteristics of the laser-doped regions, namely R_{sh} and doping profile. GP Solar's 4Tests PRO was used to measure the R_{sh} using a four-point probe method, and a WEP electrochemical capacitance-voltage (ECV) tool was used to measure the active dopant profile.

3.2.2. Silicon oxide thickness control samples

The SiO_2 thickness control samples consisted of c-Si wafers with different SiO_2 thicknesses ranging from 5 nm to 65 nm. These samples were used to investigate the required thickness of SiO_2 for functioning as a diffusion barrier against boron diffusion in the BBr_3 tube diffusion step. For these samples, we used <100> p-type Cz-Si wafers with a base resistivity = 5 ± 0.5 Ω.cm and a nominal thickness = 180 µm. The samples underwent saw damage etching and Pirahna cleaning before the high-temperature wet thermal oxidation step. The wet thermal oxidation was done for 45 minutes at 950 °C to grow 185 ± 2 nm SiO_2 on the wafers. To investigate the etch rate of the thermally grown SiO_2, the wafers were immersed in a 2-vol% HF acid solution for a defined period, followed by thickness measurement. The etching rate was determined from the slope of the thickness versus etching time graph. Using this etching rate, each wafer was then thinned from 185 nm to specific thicknesses ranging from 5 nm to 65 nm. These samples with different SiO_2 thicknesses were processed in the BBr_3 tube diffusion. Like sheet resistance control samples, the glass layers on the c-Si substrate were completely removed in a 2-vol% HF solution to monitor the electrical properties.

3.3. Results and Discussion

3.3.1. Deal-Grove model simulation study

Silicon oxide has a profound place in the fabrication of photovoltaics and the IC industry. The SiO_2 is primarily a passivation layer to passivate the surface dangling bonds on c-Si. It is also used as an insulator between semiconductor devices and a masking layer to act as a dopant barrier [101]. Due to its high etch selectivity in alkaline solutions compared to c-Si [102], it is also used in the semiconductor industry for patterning purposes.

The SiO_2 is grown in a furnace by supplying oxygen (O_2) to the c-Si surface and reacting at high temperatures. Bruce Deal and Andy Grove (of Fairchild Semiconductor) developed the first straightforward kinetic model for SiO_2 growth in the early 1960s [100]. Ho et al. [103] studied the enhanced oxidation effects in the heavily doped n^{++} c-Si substrate. The observed phenomenon is attributed to the shifting of Fermi level towards the conduction band in heavily doped n^{++} c-Si substrate, causing an increase in the equilibrium concentration of point defects or vacancies in the silicon. These point defects act as reaction sites for the chemical reaction converting Si to SiO_2, enhancing the linear rate constant, which is interface reaction dependent. Hence the oxidation rates are much higher for a heavily doped n^{++} c-Si substrate than for a lightly doped c-Si substrate.

In this study, simulations were performed to understand the influence of phosphorous surface concentration (N_s) on the growth dynamics of SiO_2 layer using Integrated Circuits

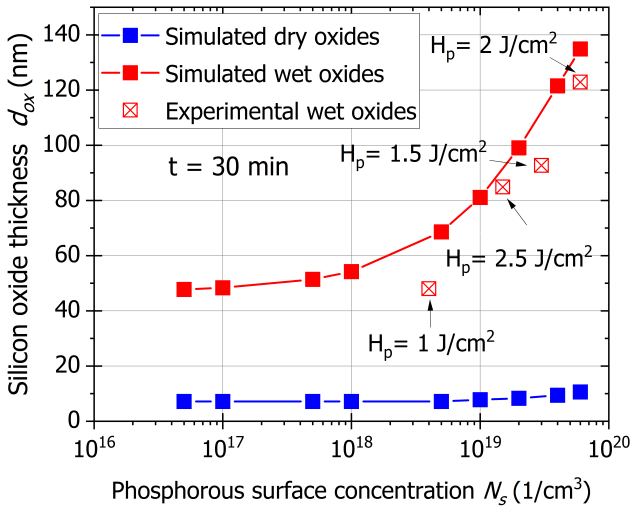

Figure 3.1: Influence of phosphorous surface dopant concentration N_s on the oxide thickness d_{ox} for wet and dry thermal oxidation simulated using the Deal-Grove model represented by solid squares and the actual measured d_{ox} after wet thermal oxidation at different laser pulse energy density H_p as a function of different N_s represented with open squares.

and Electronics group Computerized Remedial Education And Mastering software [104] which uses the Deal-Grove model. Simulations of wet and dry oxidation were done by varying the substrate doping from 1 x 10^{15} to 7 x 10^{19} cm^{-3} for 30 minutes at 850 °C as represented in Figure 3.1.

During dry oxidation, the silicon wafer reacts in a pure oxygen gas atmosphere (O_2) at elevated temperatures. Based on the data presented in Figure 1, it is evident that increasing the N_s results in a sufficient selectivity in SiO_2 thickness during dry oxidation. However, it is important to note that the oxide growth rate is significantly low, rendering it unsuitable for selective etch back in an acidic solution. Additionally, the retained oxide after patterning is insufficient to serve as a masking layer during the subsequent BBr_3 diffusion. During wet oxidation, the silicon wafer reacts in a water vapour atmosphere (H_2O) at elevated temperatures. Compared to dry thermal oxidation, much thicker oxides can be formed using wet thermal oxidation. The observed phenomenon is due to the higher solubility of H_2O in SiO_2 than the O_2 molecule [100]. Hence the thicker oxides obtained using wet thermal oxidation can be used for our patterning application. In theory, we observe high selectivity (1:3) of SiO_2 thickness between lightly 1 x 10^{15} cm^{-3} and heavily doped 7 x 10^{19} cm^{-3} silicon substrates. Increasing the substrate phosphorus level strongly affects the interface reaction rate [105].

3.3.2. Influence of laser doping (LD) settings on the sheet resistance and oxidation rates of LD BSF regions.

Figure 3.2 depicts the influence of the (H_p) on the (R_{sh}) of the laser-doped n^{++} c-Si (left) and the SiO_2 thickness *(d_{ox})* under laser-doped regions after wet-thermal oxidation (right).

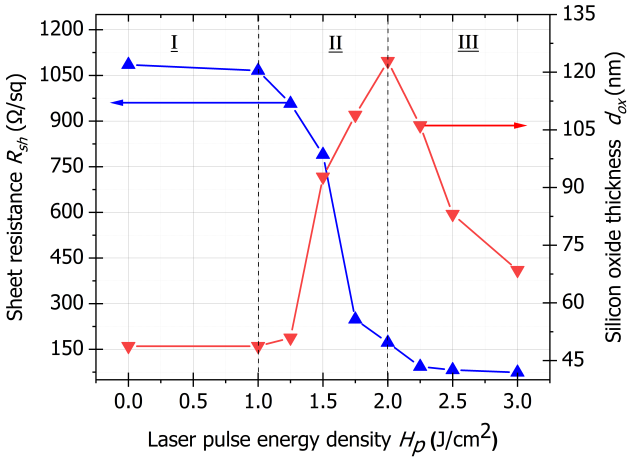

Figure 3.2: Influence of laser pulse energy density (H_p) on the sheet resistance (R_{sh}) and thickness(d_{ox}) of SiO_2 layer after wet thermal oxidation.

It can be observed that the resulting curves can be interpreted into three distinct zones, as observed in Hassan et al. [106] for laser doping of crystalline silicon from boron precursor layers. In the zone - I (0 J/cm^2 < H_p < 1 J/cm^2), the laser energies are below the melting thresholds of Si; therefore, doping is not possible. Hence in this zone-I, we observe no change in R_{sh} and d_{ox} values.

In zone-II (1 J/cm^2 < H_p < 2 J/cm^2), a linear decrease in R_{sh} with increasing H_p is seen, which indicates the number of phosphorous atoms in the doped layer also increases linearly. Interestingly, also in zone -II, we observe a linear increase in the d_{ox} from 48-nm at 1 J/cm^2 to almost 123-nm at 2 J/cm^2. This increase in the d_{ox} after wet thermal oxidation is attributed to increased N_s. From Figure 3.3, it can be observed that the N_s increases from 4 x 10^{18} cm^{-3} at 1 J/cm^2 to 6 x 10^{19} cm^{-3} (more than one order of magnitude) at 2 J/cm^2. Hence we can conclude that the decrease in R_{sh} of Zone-II can be mainly attributed to the alteration of the dopant concentration at the surface and marginally due to a deeper junction.

Progressing to zone III (H_p > 2 J/cm^2), the R_{sh} decreases marginally and then saturates at 75 Ω/sq with increasing laser H_p. In this zone, we observe that the decrease in R_{sh} is dominantly due to the deeper junction and whereas the N_s gradually starts to decrease with increasing laser H_p. The d_{ox} after wet thermal oxidation starts to decrease compared to zone-II. The decrease in d_{ox} can be explained by decreased N_s. Indeed, as seen in Figure 3.3, we observe the decrease in the N_s from 6 x 10^{19} cm^{-3} at 2 J/cm^2 to 1.5 x 10^{19} cm^{-3} at 2.5 J/cm^2. In this Zone, we start evaporating the precursor layers and partially evaporating parts of the doped silicon surface, lowering the N_s at the silicon interface. A similar observation was seen in Hassan et al. [6].

The experimental measured d_{ox} after laser doping and wet thermal oxidation were compared to the simulated wet thermal oxidation d_{ox} and are depicted in Figure 3.1 with an open red box. We observe that all the experimental measured d_{ox} is lower than that of the simulated d_{ox}. One explanation for the observed discrepancy is the phosphorous

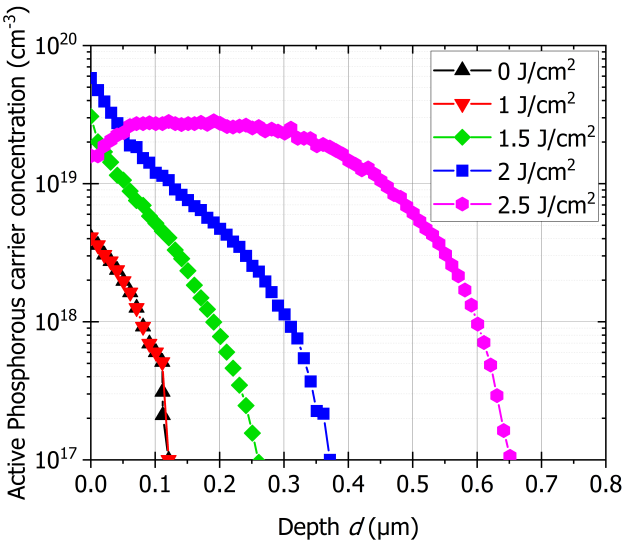

Figure 3.3: Active dopant concentration profiles of the n^{++} regions, determined from ECV measurements, for different H_p

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active concentration doping profile being different for experimental and simulated results. All the simulated d_{ox} are calculated assuming a uniform rectangular doping profile, while the experimental laser-doping has an ERFC doping profile. During oxidation, silicon is partially consumed to form SiO_2. According to literature, 54% of SiO_2 grows on the c-Si substrate, and the remaining 46% grows below the original c-Si substrate, thereby partially consuming Si during oxidation [100]. Hence for a very shallow laser-doped profile with a steep decrease in the dopant concentration (like 1 J/cm^2), we observe a much higher deviation between simulated and measured d_{ox}. In comparison, deeper laser-doped profile with a uniform doping profile (like 2.5 J/cm^2), we observe good agreement with the simulated values.

3.3.3. The process sequence of IBC solar cells using the novel patterning technique

The previous section established that we could increase the phosphorous concentration N_s at localized regions by fine-tuning the laser doping parameters. The enhanced oxidation rates under these selectively laser-doped regions can be used for patterning IBC solar cells. To investigate the feasibility of this patterning approach, a process sequence was formulated and is depicted in Figure 3.4.

The phosphorous-doped Cz-Si wafers used for solar cell fabrication were 180 ± 10 µm thick with a base resistivity (ρ_b) = 4 ± 0.5 Ω.cm and M2 size. The process sequence starts with saw damage removal and Piranha chemical cleaning. Conventional tube diffusion at atmospheric pressure using $POCl_3$ liquid precursor was used to deposit a phosphosilicate glass (PSG) layer on the c-Si substrate, which will be later used as a precursor for laser

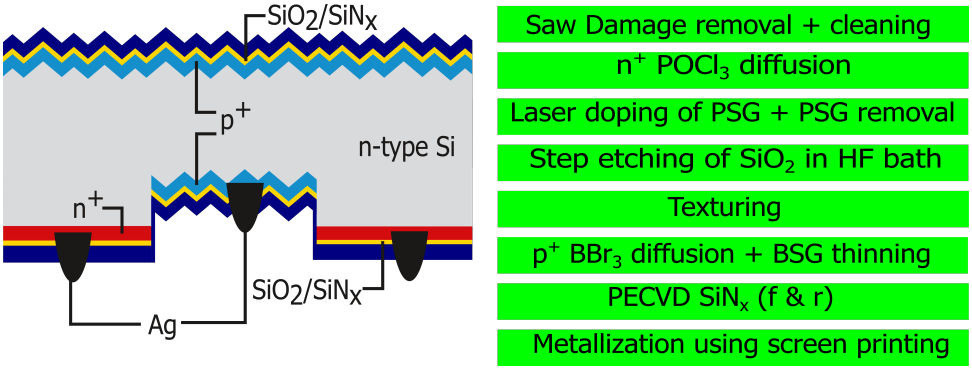


Figure 3.4: Fabrication steps of IBC solar cells using the novel patterning technique and resulting solar cell schematic representation

doping. The best laser doping settings obtained from the previous section were used to laser dope 33% of the area on the back side of the wafer, forming the 75 Ω/sq n^{++} back surface field (BSF) region. The precursor PSG layer is removed in the acidic HF bath before wet thermal oxidation at 850 °C for 30 minutes. After the high-temperature step, we grow a thick SiO_2 under the BSF regions and a thin SiO_2 under non-laser-doped regions. The SiO_2 is controllably etched back in the HF solution in the subsequent etching step. The process is interrupted when the thin SiO_2 layer under non-laser-doped regions is completely removed. The samples then undergo a texturing step during which the non-lasered regions on the rear side and the complete front side get textured, whereas, under the laser-doped BSF regions, the thick SiO_2 acts as an etch stop. A standard tube diffusion system at atmospheric pressure using BBr_3 liquid precursor was used to form the 150 Ω/sq p^+ emitter on the rear and 150 Ω/sq p^+ front floating emitter (FFE) on the front. The thick SiO_2 under the laser-doped regions prevents the boron from reaching the BSF interface and acts as a self-making layer. The BBr_3 drive-in phase is done in a partial oxygen environment, thereby growing a homogeneous in-situ thermal SiO_2 at the Si interface. In Kuruganti et al. [107], we demonstrate that this in-situ grown thermal SiO_2 can be used as a buffer layer to etch back the BSG layer entirely in an HF wet bench step due to the selectivity in the etching rates of the dopant glass layer and in-situ grown thermal glass layer [108]. The remaining in-situ thermal SiO_2 was capped with a PECVD SiN_x to passivate both p^+ and n^{++}polarities. The metallization of these solar cells was achieved using our best-known method of screen printing and firing through a process from ZEBRA technology [22]. The schematic representation of the IBC solar cells fabricated using the novel patterning sequence is depicted in Figure 3.4

3.3.4. Optimization of the process sequence and solar cell results

Successful implementation of this process sequence to fabricate solar cells critically depends on the two key steps after wet thermal oxidation, during which the SiO_2 under non-lasered regions has to be completely removed. At the same time, under the laser-doped regions, one has to retain sufficient SiO_2 thickness to withstand the texturing step and the subsequent BBr_3 diffusion. Hence these two processing steps are studied in

detail.

HF etching of SiO_2 and KOH texturing

The goal during the etching step in acidic HF solution is to completely etch the 48-nm thick SiO_2 under the non-laser-doped regions and still retain a thick enough SiO_2 under laser-doped regions to act as a masking layer for the subsequent texturing and BBr_3 diffusion processes. Since we have a difference in the oxidation rates under lasered and non-lasered regions for the same wet thermal oxidation duration, the etching rates of the SiO_2 under both regions were tested. To investigate the etch rate of the different SiO_2 layers, the wafers were immersed in 2-vol% HF acid solution for a defined period, followed by thickness measurement. The thickness *vs* etching time slope was used to determine the etching rate. The etching rate of laser-doped regions was determined to be 0.13 nm/s, whereas that of non-laser-doped regions was 0.12 nm/s, which are quite comparable. SiO_2 obtained etching rates were comparable with Spierings et al. [29] at an etchant concentration of 2-vol%. Using the knowledge of the etching rates, the samples underwent a wet bench processing in an HF bath for 420 seconds, during which the SiO_2 under the non-lasered part is completely etched and retained 75-nm thick SiO_2 under the laser doped BSF regions. The subsequent texturing step happens in the batch-type RENA wet bench. The etching rate of thermally grown SiO_2 is 200-400 times slower than that of c-Si in an alkaline texturing bath. Hence, the non-lasered regions on the rear and the complete front side are textured, leaving the laser-doped BSF region protected from texturing using the SiO_2 etch stop layer. Prior to the standard batch-type RENA wet bench texturing, the samples undergo a short HF dip. The texturing step removed approximately 3.5 µm of c-Si under non-laser-doped regions. In contrast, only 20 nm of SiO_2 under the laser-doped regions was etched. Hence during the texturing process, using the self-masking SiO_2 under laser-doped BSF regions, we pattern the rear side and texture the front side of the IBC solar cells.

BBr_3 diffusion and BSG thinning

BBr_3 diffusion step was used to form the p^+ emitter on the rear as well as on the front side (FFE) of the solar cells. To obtain shunt-free solar cells, the 55-nm thick SiO_2 under the laser-doped BSF regions should block the boron from reaching the BSF interface. To study the thickness of SiO_2 needed to function as a blocking layer for our BBr_3 tube diffusion recipe, we use the SiO_2 thickness control samples specified in the experimental section.

Figure 3.5 shows the results of the R_{sh} as a function of d_{ox}, and Figure 3.6 shows the boron active doping concentration profile measured using ECV on samples with different d_{ox} masking layer thicknesses that underwent the BBr_3 diffusion. An eddy current sensor was used to measure the layer stack's sheet resistance (i.e., the parallel summation of the emitter and base R_{sh}. The as-cut bare wafer used in this study was a p-type wafer with a base resistivity = 5 ± 0.5 Ωcm, corresponding to a doping concentration = 2.5-3 x 10^{15} cm^{-3} and the R_{sh} = 350 ± 10 Ω/sq. For samples without SiO_2, there is no blocking layer; hence, a heavily doped p^+ region with high boron surface concentration (N_s) = 2 x 10^{19} cm^{-3} and a junction depth (D_p) = 0.6 µm is formed. Due to the heavy doping of the emitter layers, the R_{sh} of the layer stack decreases to 60 Ω/sq, as seen in Figure 3.5.

For 1 nm < d_{ox} < 10 nm, the total R_{sh} of the layers increases linearly from 60 Ω/sq to 250 Ω/sq with the increase in d_{ox}. In this regime, the dopant penetrates through the SiO_2,

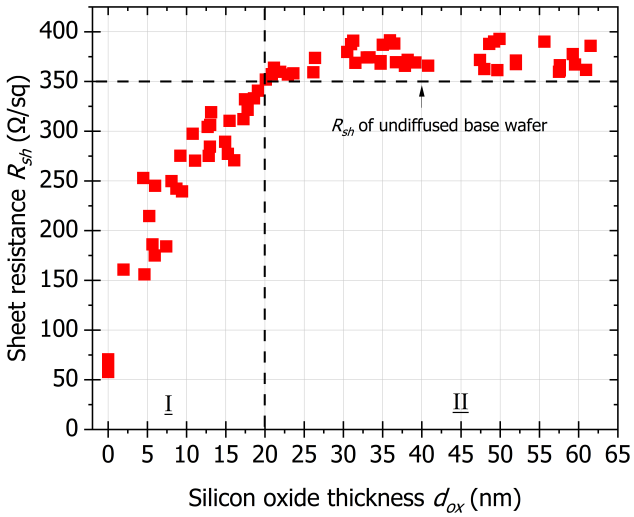


Figure 3.5: Influence of the masking SiO_2 thickness *(d_{ox})* on the sheet resistance *(R_{sh})* of the wafers after BBr_3 diffusion.

forming a heavily doped emitter region. The increase in the R_{sh} values with increasing d_{ox} indicate that with thicker oxide, we tend to block boron from reaching the c-Si interface though not completely. For this thickness range, as shown in Figure 3.6, the N_s decreased from 2 x 10^{19} cm^{-3} at 0 nm of SiO_2 to 9 x 10^{18} cm^{-3} at 10 nm of SiO_2, with no significant change in the junction depth.

For d_{ox} in the range between 10−20 nm, the total R_{sh} increases from 250 Ω/sq to 350 Ω/sq. After a further increase in the thickness of SiO_2, the total R_{sh} saturates at 350 Ω/sq, which is then limited by the R_{sh} of the undiffused wafer. Another important observation from Figure 3.6 is for the measurements with SiO_2 thickness of 15 nm; the dopant penetrates through the SiO_2 layer. It decreases the overall dopant N_s by three orders of magnitudes to almost 2 x 10^{16} cm^{-3} with a very shallow doping profile. However, there is no detectable boron doping profile for the samples with a SiO_2 thickness of more than 20 nm, indicating a complete diffusion blocking and confirming the R_{sh} measurements shown in Figure 3.5. Hence, we can conclude that the 50-nm thick SiO_2 under the laser-doped BSF region is sufficiently thick to block the boron from reaching the BSF interface.

The proof of concept solar cells were fabricated using the process sequence depicted in Figure 3a. The (current-voltage) I-V parameters were measured using a HALM flash tester and are listed in Table 1. A median cell efficiency of 20.09%, with a maximum efficiency of 20.41%, was obtained. The results obtained from the injection-dependent lifetime measurements conducted using quasi-steady-state photoconductance (QSSPC) on symmetrical lifetime samples revealed a lower bulk lifetime under the phosphorous laser-doped back surface field (BSF) was employed, as compared to the boron emitter regions with comparable emitter saturation current density (J_{0e}) values. The observed decrease in bulk time in the phosphorous laser-doped BSF sections is speculated to be

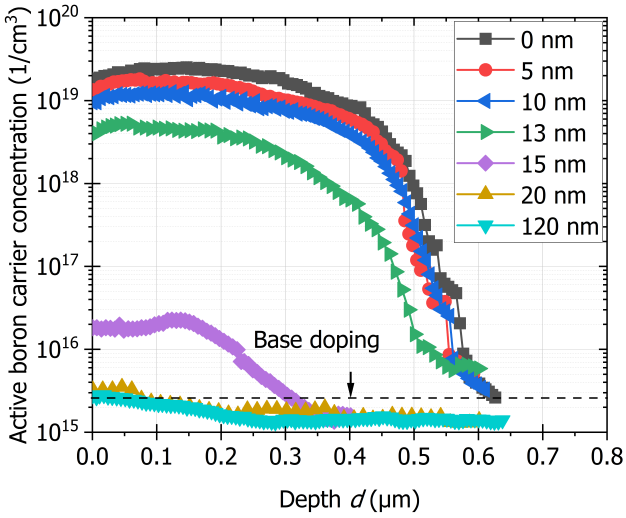


Figure 3.6: Influence of the masking SiO_2 thickness (d_{ox}) on the active boron carrier concentration profiles.

Table 3.1: Summary of (current–voltage) I–V characteristics namely: open-circuit voltage (Voc), short-circuit current (Jsc), fill factor (FF), and conversion efficiency (η) of the IBC solar cells

Group	V_{oc} (mV)	J_{sc}(mA/cm^2)	FF (%)	η (%)
Median	652.0 ±1.2	40.21 ±0.07	76.79 ±0.34	20.08 ±0.16
Maximum	654.6 ±1.2	40.38 ±0.05	77.39 ±0.28	20.41 ±0.10

due to two potential factors: laser-induced bulk damage during the laser doping step and the formation of oxidation-induced stacking faults (OISFs) in the subsequent wet thermal oxidation step [95][109]. Although the achieved cell efficiency is not particularly high, as the fabrication process was not optimized, it demonstrates the functionality of the novel patterning method to fabricate IBC solar cells.

The utilization of the increased oxidation characteristics of n^{++} Si layers in the novel patterning technique is not limited solely to diffused junctions, as demonstrated in this study. It may also be applied to the state of the art passivating contact interdigitated back contact (IBC) solar cells. There are several fundamental distinctions that must be considered when implementing this method on poly-Si layers, namely: i) Grain boundaries have a crucial role in facilitating the diffusion of phosphorous atoms, hence enabling a high dopant diffusivity in case of poly-Si compared to crystalline silicon [110]. Hence, the phosphorous diffusion should be optimized such that low phosphorous ($< 5 \times 10^{18}$ cm^{-3}) should be incorporated in the poly-Si layer during $POCl_3$ diffusion and then using the laser doping we can selectively increase the phosphorous concentration ($> 7 \times 10^{19}$ cm^{-3}) such that we can get enough selectively in the oxide thickness post wet thermal oxidation. ii) The anticipated threshold fluence required for laser doping is expected to be lower for poly-Si layers in comparison to the c-Si substrate, owing to the higher absorption coefficient exhibited by the former [111]. Furthermore, it is essential to carefully adjust the

laser doping settings in order to avoid any potential damage to the interfacial oxide layer and hence maintain the desired passivation quality [63]. iii) During oxidation, due to the stress induced by the grain boundaries the oxidation rates of the poly-Si is initially faster than the crystalline silicon [112]. Also during oxidation, silicon is partially consumed to form SiO2. As a result, it is necessary to start with thicker poly-Si layers in order to end with poly-Si layer thicknesses that can be contacted without the metal paste spiking through [113].

3.4. Summary

This chapter presents a novel patterning technique for fabricating IBC solar cells. We have demonstrated that using the enhanced oxidation rates under the local laser-doped n^{++} regions, we can pattern the rear side of the IBC solar cells and mask the laser-doped BSF regions from the subsequent BBr_3 diffusion.

We have investigated the influence of the laser pulse energy density (H_p) on the sheet resistance (R_{sh}) of the laser-doped n^{++} c-Si and the SiO_2 thickness (d_{ox}) under laser-doped regions after wet-thermal oxidation. It was concluded that upon fine-tuning the laser pulse energy density (H_p), we could locally enhance the phosphorous N_s by more than one order of magnitude. Wet thermal oxidation would yield thicker and thinner SiO_2 under laser- and non-lasered regions, respectively, with a selectivity of (2.8:1). This property can be used to an advantage if the SiO_2 is then controllably etched back in HF solution. After removing the thin SiO_2 layer beneath the non-laser-doped regions, the etching process is interrupted. The remaining SiO_2 layer under the laser-doped regions can be used as an etch stop layer under the BSF regions from the texturing step, during which the rear side is patterned and subsequently acts as a dopant barrier for the BBr_3 diffusion step, during which the emitter is formed on the front and rear side. The proof-of-concept solar cells were fabricated with novel patterning techniques and have demonstrated a conversion efficiency of 20.41%.

4

IBC solar cells using APCVD technology

Even though interdigitated back contact (IBC) architecture produces the most efficient solar cells, it is difficult to make them cost-effective and industrially viable. Therefore, single-sided atmospheric pressure chemical vapour deposition (APCVD) is investigated for the fabrication of IBC solar cells because it reduces the overall thermal budget, simplifies wet bench processing, and requires no additional masking layer. For the fabrication of a full APCVD IBC solar cells, a very lightly doped front surface field (FSF) of 650 Ω/sq, a heavier doped back surface field (BSF) of 100 Ω/sq, and a moderately doped emitter of 250 Ω/sq were used. The high-temperature annealing step is partially done in an oxygen (O_2) environment to (i) drive in dopants, (ii) prevent the formation of a boron-rich layer in the case of p^+ doped c-Si, and (iii) grow an in-situ SiO_2 at the Si/dopant glass interface. The etch rate difference between the in-situ grown SiO_2 and the doped glass layer is utilized to etch the doped glass completely. The retained in-situ SiO_2 after etching is capped with plasma-enhanced chemical vapor-deposited (PECVD) SiN_x for the passivation of both polarities of IBC solar cells. A full APCVD IBC solar cell precursor (i.e., before metallization) obtained an implied open-circuit voltage (iV_{oc}) of 714 mV and an emitter saturation current density (J_{0s}) of 17 fA/cm^2. A full APCVD IBC solar cell had a conversion efficiency of 22.8% at the device level, with an open circuit voltage (Voc) of 696 mV and a short-circuit current density (Jsc) of 41.3 mA/cm$_2$. These parameters are comparable to the commercially available full-tube diffused ZEBRA® IBC solar cells.

This chapter is based on the following publications: **V. V. Kuruganti**, D. Wurmbrand, T. Buck, S. Seren, M. Zeman, O. Isabella, F. Geml, H. Plagwitz, B. Terheiden, and V. D. Mihailetchi, "Industrially viable diffused IBC solar cells using APCVD dopant glass layers", Solar Energy Materials and Solar Cells 2023, 251 112111.

4.1. Introduction

In the early 1950s, the first silicon solar cells were fabricated on an n-type substrate using an interdigitated back contact (IBC) architecture [32]. IBC solar cells are the optimal choice for fabricating high-efficiency solar cells since all metallization can be placed on the non-illuminated side of the solar cells, enhancing the incident light absorption on the front side [114]. Other benefits of IBC architecture include lower series resistance due to a higher metal fraction, simple module integration, and its potential in building integrated photovoltaics (BIPV) due to the module's visually pleasant look [115]. Silicon heterojunction (SHJ) technology has enabled crystalline silicon (c-Si) solar cells with an IBC configuration to achieve a world-record conversion efficiency of 27.1% [21]. Sunpower Corporation, the most successful company commercially manufacturing large area passivating contacts IBC solar cells, have reported efficiencies of 25.2% [85]. Lastly, the ISC Konstanz-developed ZEBRA® technology is a bifacial IBC solar cell concept based on a typical industrial low-cost manufacturing method that has exhibited mass production efficiencies surpassing 23.5% [86].

IBC architectural cell technologies are still a niche industry due to their intricate processing sequence and expensive production costs [116]. First, because of the inherent nature of the IBC architecture, the rear side must be patterned using photolithography [117][72], inkjet patterning [89] or a laser process [118][96] in conjunction with multiple wet bench cleaning processes. Secondly, since all charge carriers need to be collected on the rear side, the wafer bulk should have a high minority carrier lifetime. Thirdly, the fabrication of the three different doped regions, the so-called FSF or front floating emitter (FFE), the BSF, and the emitter would necessitate multiple high-temperature steps that would significantly increase the thermal budget and process complexity. Finally, passivation of IBC architecture is cumbersome as locally doped opposite polarities are located at the rear side and hence would require a universal passivation stack for both polarities. In this study, using laser technology and high-quality n-type substrate materials, the latter two constraints are addressed for fabricating industrially viable IBC solar cells [115].

Using doped glass layers based on atmospheric pressure chemical vapour deposition (APCVD) [119] instead of conventional gas tube diffusion, where the doped glass is grown and driven in, would decrease the process complexity of IBC solar cells. Additionally, APCVD dopant glass layers are deposited before diffusion; therefore, little or no spacing is required in the diffusion furnace, which can significantly increase throughput [120]. Furthermore, by using APCVD layers, we can decouple the deposition step from the diffusion step, allowing us to perform laser processing steps before a high-temperature step or co-annealing to reduce the overall thermal budget [121][54]. Some other advantages of APCVD processing include lower operational and maintenance costs and high throughput [54].

This study investigated the effect of varying APCVD dopant concentrations on layers' electrical properties after high-temperature annealing. The annealing recipe was optimized for three purposes, namely: drive in the dopants, prevent boron-rich layer (BRL) [122] formation in case of p^+ doped c-Si, and grow an in-situ SiO_2 at the interface between glass and Si for passivation purpose [108]. Furthermore, the in-situ grown SiO_2 at the interface serves as an etch barrier for the controlled etch back of APCVD borosilicate

glass (BSG) and phosphosilicate glass (PSG) layers with varying dopant concentrations in a single wet bench HF glass removal step. The passivation quality was measured on symmetrical lifetime samples and solar cell precursors with a SiO_2/SiN_x passivation stack. Finally, all learnings were integrated for a streamlined and cost-effective approach to fabricating high-efficiency APCVD IBC solar cells.

4.2. Experimental and characterization

4.2.1. Sheet resistance and symmetrical lifetime samples preparation

For our sheet resistance (R_{sh}) samples, we used pseudo-square 180 ± 10 µm thick M2 Czochralski (Cz) wafers with opposite doping to that of doped layers to investigate, that is, <100> n-type Cz-Si wafers with base resistivity ρ_B = 3 Ω.cm and <100> p-type Cz-Si wafers with base resistivity ρ_B = 0.95 Ω.cm. All samples underwent an alkaline etch to remove saw-cutting-induced damages, followed by a piranha cleaning process to remove organic and inorganic impurities before the APCVD dopant glass deposition. The APCVD equipment is a SCHMID APCVD Roller-Transport System with multiple deposition chambers enabling more than one layer in a single pass. The layers of borosilicate glass (BSG) and phosphosilicate glass (PSG) were 40 nm thick. In addition, to prevent the doped layers underneath from reacting with the environment [123], an additional 20 nm thick undoped silicate glass (USG) capping layer was deposited. Finally, the doped glass layers were annealed in a partial O_2 environment to form the p^+ and n^+ doped regions. The glass layers on top of c-Si were etched in an HF solution to measure the doped regions' electrical properties. R_{sh} was measured using the four-point probe tool from GP Solar, and the active dopant profile was determined using an electrochemical capacitance-voltage (ECV) tool from WEP. For our symmetrical lifetime samples, we used only <100> n-type Cz-Si wafers with base resistivity ρ_B = 3 Ω·cm and nominal thickness of 180 ± 10 µm. The processing sequence of symmetrical lifetime samples was similar to that of the above-mentioned R_{sh} samples until the high-temperature annealing step, except that both sides of the wafer had the same dopant glass layer deposited. Then, the in-situ grown SiO_2 is used as a buffer layer to completely etch the APCVD dopant glass layer. A detailed description of this systematic etching procedure using SiO_2 as a buffer layer can be found in [108]. Finally, on both sides, these samples received 75 nm-thick plasma-enhanced chemical vapour deposition (PECVD) SiN_x. Then, the samples were fired in a belt-type rapid-firing furnace for hydrogenation using our best-known in-house settings [74]. For measuring the iV_{oc} and J_{0s} of the doped regions, we have used a WCT-120 lifetime tester from Sinton Instruments. For the QSSPC measurements, we have used a base resistivity of ρ_B = 3 Ω.cm and a thickness t of 170 µm. For the flat passivated symmetrical lifetime samples, an optical constant of 0.95 was selected, whereas an optical constant of 1.1 was chosen for the passivated textured solar cell precursor samples. The lifetime measurements were carried out in generalized mode.

4.2.2. Full APCVD IBC solar cells

Figure 4.1 indicates the schematic fabrication process and corresponding structure of the full APCVD IBC solar cell. The substrate is <100> Cz-Si M2 wafers with a base resistivity of ρ_B = 3 Ω.cm and a thickness of 180 ± 10 µm. First, all samples underwent alkaline etching

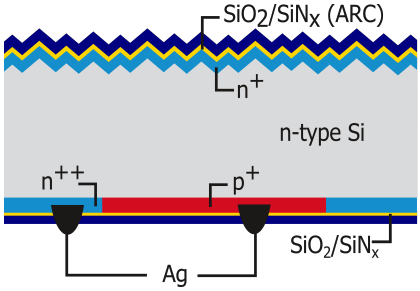
to remove the saw-cutting-induced damage, followed by the piranha cleaning process. An APCVD BSG layer was deposited on the rear side of the wafers and subsequently annealed in an O_2 environment to form the emitter region. The samples then received a PECVD SiN_x masking layer on the rear side. After laser patterning, the rear side of the wafers was alkaline etched and cleaned. An APCVD PSG layer with a low doping concentration was deposited on the front side, and a high doping concentration was deposited on the rear side and subsequently annealed in an O_2 environment to form the BSF region on the rear and the FSF region on the front side of the substrate. Similarly to lifetime samples, the in-situ grown SiO_2 was used as a buffer layer to completely etch the APCVD BSG and PSG layers after annealing. For passivation purposes, both sides received a PECVD SiN_x layer. The metallization of these samples was achieved using our best-known method of screen printing and firing through the process from ZEBRA® technology [74].

To investigate the passivation quality of the solar cell before metallization, we have also fabricated solar cell precursors. It is essential to account for numerous artefacts that might induce an overestimation of the carrier lifetime when interpreting photoconductance based lifetime measurements. One such scenario involves samples with a conductive layer disrupted by lines of opposing polarity doping, resulting in laterally alternating p^+/n^+ doping areas [124]. This structure often appears in the emitter region of samples that monitor the lifetime of interdigitated back contact cells. To avoid overestimating passivation quality, the processing sequence for the solar cell precursor samples follows that shown in Figure 4.1, except for the PECVD masking, laser patterning processes and rear side PSG deposition. As such, the final structure of the solar cell precursor samples has a full area emitter on the flat rear and a full area FSF on the textured front side.

To compare our novel full APCVD IBC solar cells and solar cell precursors, we have fabricated three groups: full tube diffused, hybrid-1 and hybrid-2. The doped regions (i.e. BSF, FSF and emitter) in all these solar cell concepts are formed by either annealing the APCVD glass layer or using the standard industrial tube diffusion. Table 4.1 summarizes how the doped regions in different solar cell groups were fabricated. In addition, the full tube diffused precursor cells are manufactured using the ZEBRA best-known method and are used here as a process reference.

Table 4.1: Different techniques for forming the doped regions and their corresponding R_{sh} values of the four IBC solar cell types investigated in this chapter.

Solar cell group	FSF (n^+)	BSF (n^{++})	Emitter (p^+)
Full APCVD	APCVD PSG 650 Ω/sq	APCVD PSG 100 Ω/sq	APCVD BSG 250 Ω/sq
Hybrid-1	$POCl_3$ diffusion 150 Ω/sq	$POCl_3$ diffusion 80 Ω/sq	APCVD BSG 250 Ω/sq
Hybrid-2	APCVD PSG 650 Ω/sq	APCVD PSG 100 Ω/sq	BBr_3 diffusion 150 Ω/sq
Full tube diffused ZEBRA® [86]	$POCl_3$ diffusion	$POCl_3$ diffusion	BBr_3 diffusion



Alkaline etching + cleaning
APCVD BSG (r) + Annealing + BSG thinning
PECVD masking (r) + base region ablation
Alkaline etching + cleaning
APCVD PSG (f & r) + annealing + BSG thinning
PECVD SiNx (f & r)
Metallization using screen printing

Figure 4.1: Main process steps to fabricate the full APCVD IBC solar cell (a) and a schematic cross-section view of the resulting IBC cell (b).

4

4.3. Results and Discussion

4.3.1. Electrical properties of doped regions

The electrical properties of the doped regions were analyzed using sheet resistance samples specified in the experimental section. This study investigated the electrical characteristics of annealed APCVD BSG and PSG with three different dopant concentrations. The minimum and maximum temperatures in the annealing recipe were 810 °C and 995 °C, respectively. At the peak temperature of 995 °C, annealing was done in a 100% O_2 environment. The presence of APCVD BSG or PSG layers on the silicon surface offers almost no hindrance for the O_2 reaching the Si surface because of the high diffusivity of O_2 in doped glass layers compared to pure SiO_2 [99]. Similar studies were carried out by Mihailetchi et al. [108], where the BSG layer grown from the tube-diffused BBr_3 offered

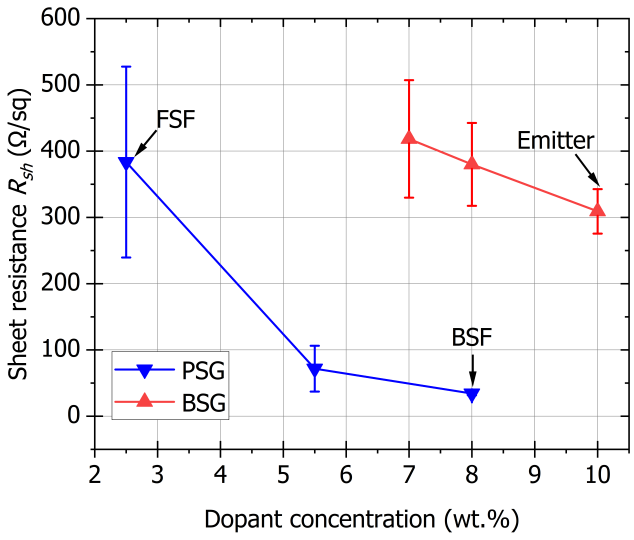


Figure 4.2: Sheet resistance R_{sh} after high-temperature annealing of APCVD layers with different dopant concentrations and dopant types.

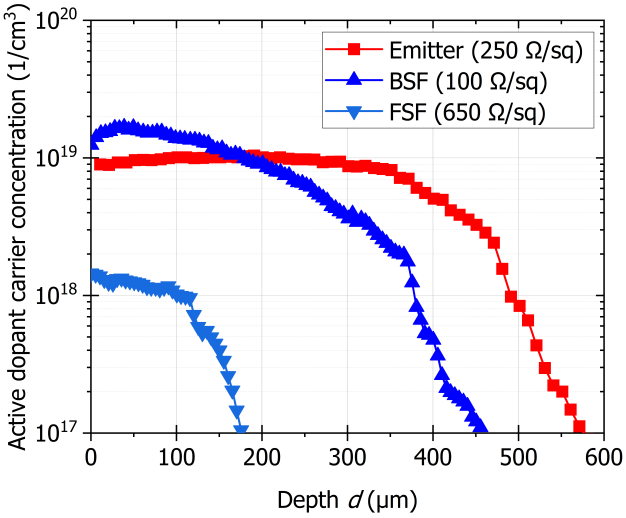


Figure 4.3: Carrier concentration profiles of the p^+ doped emitter layer, lightly doped n^+ FSF layer and heavily doped n^{++} BSF layer used in the full APCVD IBC cell process.

little resistance for the oxygen to diffuse to the silicon interface. Also, Mihailetchi et al. [108] demonstrated that irrespective of the BSG thickness uniformity across the wafer or along the diffusion boat, the in-situ grown thermal SiO_2 was very homogeneous, making it an attractive option for being used as passivation and ARC layers. Moreover, boron has a higher segregation coefficient in SiO_2 than Si [125]. Hence the post-oxidation ensures that the higher concentration of boron at the surface segregates into the SiO_2, thereby preventing the formation of BRL, which has proven to degrade bulk lifetime and cause very high emitter saturation current densities [126].

Figure 4.2 shows the R_{sh} data of the boron and phosphorous-doped regions after annealing as a function of the APCVD glass dopant concentration. With increasing dopant concentration, we observe a decrease in R_{sh} for both polarities and an increase in the homogeneity of the R_{sh}. For the operating temperatures (810 °C and 1100 °C) used in this study, activation energies of phosphorous and boron are 2.74 ± 0.007 eV and 3.12 ± 0.004 eV, respectively [127]. Hence, for a similar dopant concentration of 8.0 wt %, we observe higher doping of phosphorous (80 Ω/sq) compared to boron (320 Ω/sq).

When selecting the electrical properties of the p^+ and n^+ regions on the rear side of IBC solar cells, three crucial parameters, i.e. J_{0pass}, J_{0met}, and ρ_c should be minimized to increase the cell efficiency [128]. Here, the knowledge gained from our tube-diffused ZEBRA IBC technology was used to select optimal electrical properties of emitter and BSF for APCVD IBC solar cells [74]. Accordingly, a 230 Ω/sq emitter and 100 Ω/sq BSF were selected. Due to the flexibility of single-sided APCVD deposition technology, we chose a very lightly doped FSF (650 Ω/sq) in this study. Figure 4.3 shows the carrier concentration profiles of the shortlisted layers. The low surface concentrations of 9.5×10^{18} cm^{-3} for the p^+ emitter layer show that the annealing in an oxygen environment has successfully prevented the formation of BRL. Also, very lightly doped FSF with R_{sh} of 650 Ω/sq and

a surface concentration of 2.5×10^{18} cm^{-3} with a shallow junction depth of 0.18 µm was used in this work. Since there is no need for any metallization at the front side of the IBC solar cells, having a lightly doped front surface field can be well passivated, reducing the surface recombination while augmenting the spectral response in the ultraviolet range (280 nm to 400 nm) and thus improving the V_{oc} and J_{sc} [92].

4.3.2. Etch rate study of doped oxide glass stack

During the high-temperature annealing step, apart from driving dopants into the bulk, we grow a homogeneous SiO_2 of 32 nm at the doped glass/Si interface. In this section, we show that the in-situ grown thermal SiO_2 can be used as a buffer layer due to the difference in the etching rate of doped glass layers compared to thermally grown SiO_2. In the following section, we show that the partially etched back SiO_2, when capped with PECVD SiN_x, offers excellent surface passivation for both p^+ and n^+ doped regions, thereby acting as a universal passivation scheme with fewer processing steps in IBC solar cell concepts. To investigate the etch rate of different layers, the wafers were immersed in 2-vol% HF acid solution for a defined period, followed by thickness measurement. The thickness of BSG, PSG and SiO_2 were measured using a Sentech SE-800PV ellipsometer, assuming the refractive index of n = 1.46 for all glass layers [129].

Figure 4.4 shows the thickness variation across the wafer at different processing stages of the samples. During the as-deposited stage, we deposit 40 ± 7.2 nm of BSG and 60 ± 7.7 nm of PSG + USG layer. We observe a high inhomogeneity of thickness across the wafer. Upon annealing these layers in the O_2 atmosphere, we grow a 32 nm thick uniform in-situ SiO_2 layer at the interface of c-Si and the dopant glass. Upon thinning the layer stack in HF solution, the dopant glass layer is etched completely, and a 13.6 ± 1.4 nm (in case of

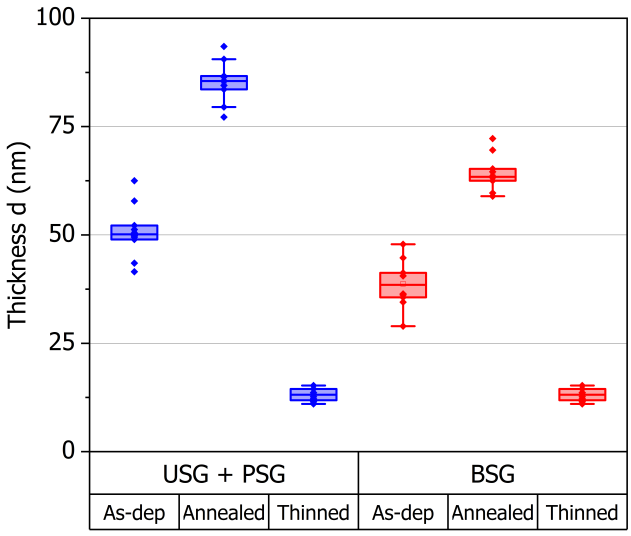


Figure 4.4: Thickness of the USG + PSG layer stack and BSG layer measured after APCVD deposition, directly after annealing the samples in an O2 environment, and after HF thinning.

USG + PSG) and 11.2 ± 1.4 nm (in case of BSG) in-situ grown SiO_2 layer remains on Si surface, which served as a passivation layer. The significant improvement in thickness uniformity across the wafer, as measured by the standard deviation value after thinning in HF, is attributable to the slower etching of in-situ grown SiO_2 compared to dopant glass layers. Figure 4.5 depicts the thickness of the different layers stacks as a function of etching time in 2-vol% HF solution. As indicated by the arrows, the etching rate of each layer was calculated using the slope of thickness versus etching time. The green rhombus represents the thermally grown SiO_2, which was used as a reference to compare the etching rates of the in-situ grown SiO_2 after annealing in an O_2 environment; the inverted red triangle represents the annealed "APCVD BSG + in-situ grown SiO_2" stack, and the blue triangles represent the "APCVD USG + PSG + in-situ grown SiO_2" stack. The USG capping layer was necessary to protect the otherwise hygroscopic PSG layer [123].

The wafers were immersed in the 2-vol% HF solution, followed by the immersion in deionized water, to stop the etching process. Uncertainty in estimating the etching rate could arise due to the unintended slow etching during the transportation of the wafers from the HF solution beaker to the DI water beaker. Due to the short etching times, the relative measurement error of the etching rate is approximately 15%. The etching rate of thermally grown SiO_2 was determined to be 0.18 ± 0.02 nm/s, equivalent to Spierings et al. [130] at an HF concentration of 2 wt.%. The stack etch rate findings for co-annealed "APCVD BSG + in-situ grown SiO_2" were separated into the BSG zone and the in-situ grown SiO_2 zone. Like Mihailetchi et al. [108], the BSG layer exhibited a much higher etching rate of 0.46 nm/s than thermally produced SiO_2 (0.18 nm/s). The difference in etching rate is because the breaking rate of B-O bonds in HF solution is significantly

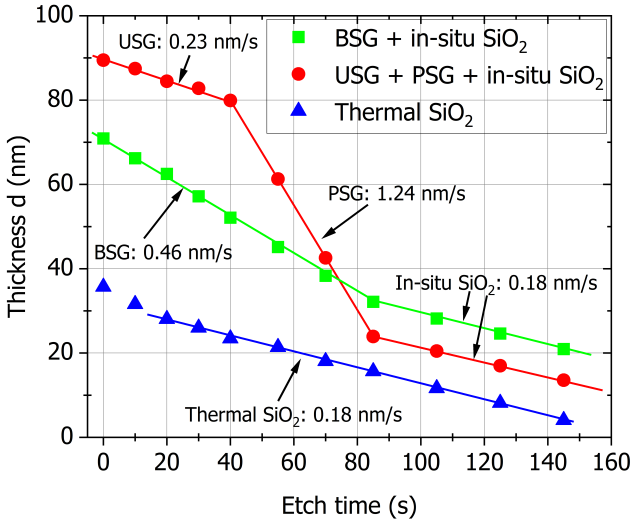


Figure 4.5: The thickness of the different annealed oxide stacks (see legend) used in this study as a function of etching time in 2-vol% HF solution. The arrows represent the etching rates of the different layers within the stack. To compare the etching rate of the in-situ grown SiO2, a reference samples with 32 nm of thermally grown SiO2 was used in this study.

higher than that of Si-O bonds [101]. After 100 seconds of etching in HF solution, we have already reached the in-situ grown SiO_2 regime, and the etching rate drops by almost 2.5. In this zone, we see the etching rate being equal to that of thermal SiO_2 (blues triangles), pointing out that the properties of the in-situ grown oxide are comparable to that of the thermally grown oxide without any dopant layer on top. Finally, etch rate findings for the co-annealed "APCVD USG + PSG + in-situ grown SiO_2" stack was separated into three regimes: USG capping zone, PSG zone, and in-situ SiO_2 zone: USG capping zone, PSG zone and in-situ SiO_2 zone. The etching rate of the APCVD annealed USG layer is determined to be 0.24 ± 0.03 nm/s which is marginally higher than that of thermally grown SiO_2. The observed disparity in etching speeds can be due to CVD and thermal oxides' different compositions and porosities [101]. The APCVD PSG layer exhibited the maximum etching rate in this investigation, with an etching rate as high as 1.24 ± 0.12 nm/s, which is over 7.7 times greater than thermally produced SiO_2. Hence, it can be said that the breakage rate of P-O bonds in HF solution is faster than (>) B-O bonds, which in turn exceeds that of > Si-O bonds. After 100 sec of HF etching, we enter the third phase of the in-situ SiO_2 and see similar behaviour to that of the annealed BSG stack. Hence, we have demonstrated that by using a single HF etching step (in this case of 145 seconds) for our annealed doped glass layers, we can completely get rid of both BSG and PSG by using their selective etching compared to in-situ grown SiO_2 in HF solution. Mojrova et al. [131] have demonstrated that for the optimal passivation quality of the SiO_2/SiN_x passivation stack, we need at least 10 nm of the SiO_2 and a SiN_x layer with a low refractive index. Hence in this work, the etching time was adjusted such that at least 10 nm of the in-situ grown silicon oxide remained on the doped c-Si surface. This partly etched-back SiO_2 is subsequently covered with PECVD SiN_x to passivate both polarities of the IBC solar cells.

4.3.3. Passivation quality and IV results at the device level

As described in the experimental section, Symmetrical lifetime samples were used to study the passivation quality of the doped APCVD layers. Figure 4.6b shows the iV_{oc} and J_{0s} of the doped regions, whereas Figure 4.6a shows their corresponding injection-dependent lifetime results. Table 4.2 shows the individual saturation current density (J_0) contributions and iV_{oc} of the symmetrical lifetime structures and the solar cell precursor groups. The J_{0s} contribution was extracted at an injection level of 5 x 10^{15} cm^{-3} using the Kane and Swanson method [132]. The measured J_{0s} values displayed in Figure 4.6b, Figure 4.6d and Table 4.2 indicate the J_0 contributions from both sides of the doped regions. At one sun illumination, since the effective lifetime (τ) and J_{0s} of the doped region can be measured, bulk lifetime (τ_{bulk}) can be calculated using Equation 4.1, and subsequently, the saturation current density of the bulk region (J_{0b}) can be calculated using Equation 4.2. Finally, the total saturation current density (J_{0t}) was found by summing up J_{0b} and J_{0s}. Here N_{dop} is the background dopant density, W is the thickness of the samples, (Δn) is the injection level at one-sun condition, and n_i is the intrinsic carrier concentration of silicon.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{\text{bulk}}} + \frac{J_{0s}\left(N_{\text{dop}} + \Delta n\right)}{q \times n_i^2 \times W} \tag{4.1}$$

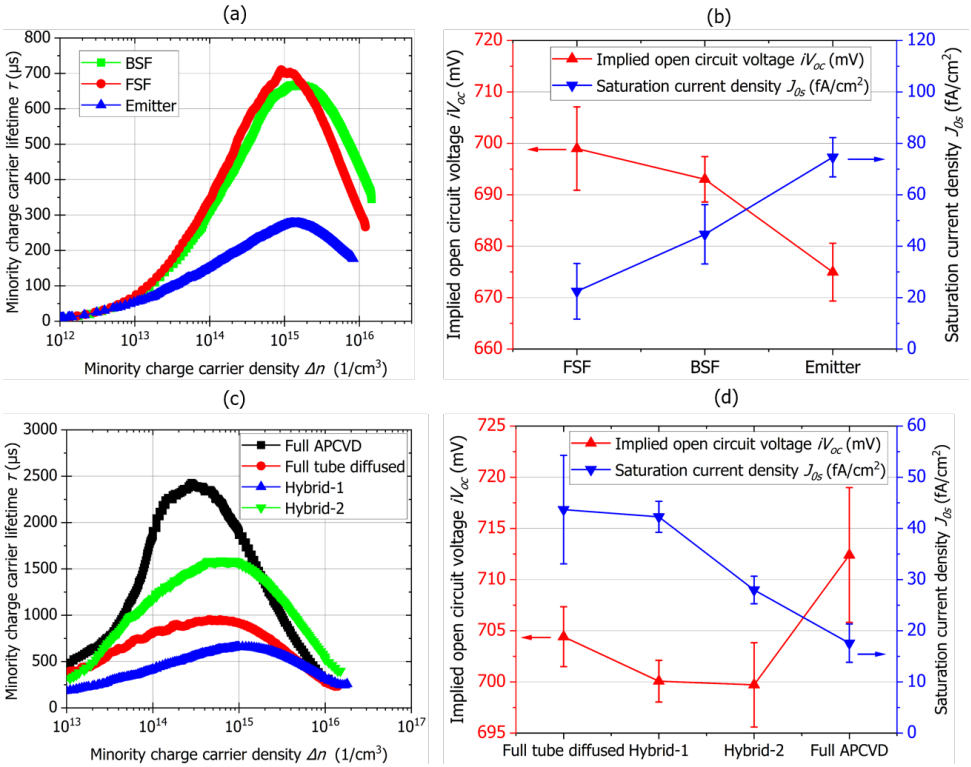


Figure 4.6: (a) Injection-dependent lifetime results of the symmetrical BSF, emitter and FSF lifetime samples. (b) iV_{oc} and J_{0s} of symmetrical FSF (n^+), BSF (n^{++}) and emitter (p^+) lifetime samples formed by annealing of APCVD layers. (c) Injection-dependent lifetime results of full APCVD, full tube diffused, hybrid-1 and hybrid-2 solar cell precursors. (d) iV_{oc} and J_{0s} of solar cell precursor as follows: Full tube diffused, hybrid-1, hybrid-2 and full APCVD solar cells precursors.

$$J_{0b} = \frac{q \times n_i^2 \times W}{N_{dop} \times \tau_{bulk}} \tag{4.2}$$

FSF and BSF layers have iV_{oc} values above 690 mV, whereas the emitter layer has a much lower iV_{oc}, around 675 mV. A lower J_{0b} of n^+ doped areas is attributable to the enhanced gettering efficacy of APCVD PSG compared to APCVD BSG at the same annealing temperature [133]. Secondly, the lightly doped FSF layer has higher iV_{oc} and lower J_{0s} than the heavily doped BSF layer. We estimated the influence of Auger recombination on the J_{0s} values of the BSF and FSF-doped areas using EDNA 2 [134]. The overall two sides Auger recombination contribution for the weakly doped FSF region is just 0.6 fA/cm^2 compared to 25 fA/cm^2 for the BSF region. Hence, the observed difference in J_{0s} is attributed mainly to the difference in their Auger recombination.

The passivation quality of the four solar cell precursor groups (i.e. before metallization) and their corresponding injection-dependent lifetime curves are depicted in Figure 4.6d

Table 4.2: Average individual J_0 contributions due to recombination in the wafer bulk J_{0b}, doped regions (including Auger) surface J_{0s}, and their corresponding average iV_{oc} values. The J_{0t} is the total saturation current density of symmetrical lifetime samples or solar cell precursors estimated by adding the relevant individual contributions.

Group	J_{0b} (fA/cm^2)	J_{0s} (fA/cm^2)	J_{0t} (fA/cm^2)	iV_{oc} (mV)
Emitter (LT)	50	72	122	679
BSF (LT)	25	45	70	692
FSF (LT)	33	17	51	702
Full tube diffused (Precursor)	5	42	47	706
Hybrid-1 (Precursor)	21	42	63	698
Hybrid-2 (Precursor)	39	29	68	696
Full APCVD (Precursor)	19	17	36	712

and Figure 4.6c, respectively. As a reference group, full-tube diffused precursors had a mean iV_{oc} of 704 mV and a mean J_{0s} of 47 fA/cm^2, respectively. Despite having the highest J_{0s} in the group, the full tube diffusion precursor gives the second-best iV_{oc}. As evidenced by the injection-dependent lifetime curves (Figure 4.6c at lower injection levels and from the estimated J_{0b} in Table 4.2, $POCl_3$ and BBr_3 tube diffusions were highly effective in gettering the bulk layer, hence enhancing the iV_{oc} of this cell precursor group. In Figure 4.6d, hybrid-1 and hybrid-2 precursor cells displayed comparable iV_{oc} but distinguishable J_{0s}. Lower J_{0s} seen in the hybrid-2 precursor result from the lightly doped FSF (680 Ω/sq) created by annealing the APCVD PSG as opposed to the heavily doped FSF (150 Ω/sq) formed via $POCl_3$ tube diffusion in the hybrid-1 precursor. Due to the improved gettering efficiency of $POCl_3$ diffusion (also found in full diffused precursors) in hybrid-1 precursors, the J_{0t} of both hybrid precursors is comparable, which explains their comparable iV_{oc}.

Complete APCVD precursors have shown the best passivation quality among all the groups, with mean iV_{oc} of 714 mV and J_{0s} as low as 17 fA/cm^2. Such high passivation quality is generally observed in solar cells endowed with carrier-selective junctions [131]. The excellent passivation quality of complete APCVD precursors is attributed to the high quality of the APCVD dopant glasses, the difference in electrical properties such as sheet resistance and surface dopant concentrations, and the difference in sample preparation and the optimized high-temperature annealing steps. Compared to the symmetrical lifetime samples, the higher iV_{oc} is due to improved gettering of the bulk layer during the second high-temperature annealing, as shown by the J_{0b} values in Table 4.2. Combining the J_{0s} contributions from the single-sided emitter and FSF yields a J_{0s} of 45 fA/cm^2, whereas the J_{0s} measured for the full APCVD precursor (which is formed by single-sided emitter on the rear and FSF on the front) was considerably lower. This observed discrepancy is unknown and needs deeper investigation. However, we suspect it to be caused by a combination of the three factors: 1) The second high-temperature annealing process, which might getter the emitter layer; 2) Additional hydrogenation from the PECVD capping SiN_x layer, which was deposited for masking and patterning purposes, and 3) Higher number of cleaning steps. As a result, to achieve a J_{0s} of 17 fA/cm^2 in solar cell precursor, the J_{0s} on the emitter layer should also be about 17 fA/cm^2. Nevertheless, J_{0s} values of the emitter in the full APCVD precursor reported in this work were comparable

Table 4.3: Parameters of the best solar cells extracted from current-voltage characteristics of the different groups of solar cells as mentioned in Table 3, namely: Full tube diffused cells (ref.), hybrid-1 cells, hybrid-2 cells and Full APCVD cells.

Group	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eta (%)
Full tube diffused (ref.)	41.3	690	80	22.8
Hybrid-1	40.7	686	78.3	21.9
Hybrid-2	41.3	693	79.1	22.6
Full APCVD	41.3	696	79.3	22.8

and in good agreement with literature-reported values of SiO_2/SiN_x-based passivation methods commonly used in the industry for the passivation of p^+ regions of solar cells [108] [135].

Table 4.3 presents the solar cell performance parameters of the best solar cells extracted from current-voltage characteristics of the different groups of solar cells studied in this work. The J_{sc} of the hybrid-1 solar cells was 0.6 mA/cm^2 lower than hybrid-2 solar cells. The spectral response measurements (data not shown) showed lower internal quantum efficiency response in the UV region (280 nm to 400 nm) caused by the higher doping of the FSF layer in hybrid-1 compared to hybrid-2 solar cells. The full tube diffused (ref.) IBC solar cells and full APCVD IBC solar cells have comparable conversion efficiencies. In the case of full APCVD IBC solar cells, even after having a very lightly doped FSF on the front side, we obtain a similar J_{sc} and a boost of 6 mV in V_{oc} compared to the full tube diffused IBC solar cells, as also observed with the solar cell precursors. The lower FF observed in full APCVD IBC solar cells is attributed to the higher sheet resistance of the emitter layer in comparison to full tube diffused IBC solar cells (R_{sh} = 150 Ω/sq). By further optimizing the APCVD dopant concentration of the emitter layer and fine-tuning of high- temperature annealing step, obtaining efficiencies exceeding 23% is feasible.

4.4. Summary

This chapter presents a systematic study of using the APCVD technology as a low-cost fabrication of high-efficiency IBC solar cells. We have demonstrated that a full APCVD-based IBC solar cell flowchart can produce similar power conversion efficiencies as those based on commercially available ZEBRA® [6], which is fabricated using industry-standard BBr_3 and $POCl_3$ tube diffusion systems. We have investigated the influence of APCVD dopant concentrations on the electrical properties of the doped regions. The annealing recipe chosen in this study had three primary purposes: drive-in of dopants into the substrate, growth of a thermal SiO_2 at the silicon glass interface for passivation purposes, and preventing the formation of a BRL. Based on the electrical properties after annealing the individual APCVD glass layers (i.e. R_{sh} and J_{0s}), a 250 Ω/sq emitter, 100 Ω/sq BSF and 650 Ω/sq FSF were chosen for the fabrication of the full APCVD IBC solar cells. We show that the in-situ grown thermal SiO_2 formed during the annealing in a partial O_2 environment can be used as a buffer layer to etch back partially or entirely the APCVD PSG or BSG in a single HF wet bench step. The remaining in-situ oxide, when capped with PECVD SiN_x, gave excellent surface passivation on both p+ and n^+ doped regions. On full APCVD solar cell precursors (i.e., without metallization), we obtained an iV_{oc} of

714 mV and a J_{0s} as low as 17 fA/cm^2, which are outstanding values for diffused junctions. At the device level, for metallized large-area IBC cells, we have demonstrated conversion efficiencies approaching 23% for a process entirely based on the APCVD-doped glass deposition technique.

5

Rear junction TOPCon solar cells using APCVD technology

In this chapter, we explore the efficiency potential and optimize the fabrication process of a TOPCon front-back contact (FBC) n-type cell concept with a rear junction (RJ) topology, i.e., the cell has an APCVD p^+ poly-Si rear emitter and a $POCl_3$ diffused n^+ front surface field (FSF) and selectively laser doped n^{++} region under the front metal contacts. In order to optimize the passivation quality under the non-laser doped FSF regions a wide range of $POCl_3$ diffusion profiles were studied. Subsequently, a systematic study was carried out to optimize the laser doping parameters in order to obtain the desired electrical properties with minimal laser induced damages under the laser doped FSF regions. For the boron doped p^+ poly-Si emitter, we developed an in-situ annealing process to crystallize boron-doped amorphous silicon p^+ a-Si layers deposited by atmospheric pressure chemical vapour deposition (APCVD) to form boron-doped polycrystalline silicon p^+ poly-Si layers emitter layers. The influence of the temperature profiles during a p^+ a-Si inline deposition on structural, electrical, and passivation properties was studied in detail.

This chapter is based on the following publication:

1. **V. V. Kuruganti**, A. Mazurov, S. Seren, O. Isabella, and V. D. Mihailetchi, "In Situ Annealing of Boron-Doped Amorphous Silicon Layers Using APCVD Technology", IEEE Journal of Photovoltaics,14(1),74-79 (2023).
2. **V. V. Kuruganti**, T. Buck, S. Veerman, C. Ebert, S. Seren, R. Kopecek and V. D. Mihailetchi, "Rear-Junction Tunnel Oxide Passivated Contact Silicon Solar Cells with Selective Front Surface Field", in 40th European Photovoltaic Solar Energy Conference and Exhibition. 2023 020047001-004.

5.1. Introduction

Impressive high conversion efficiency in crystalline silicon (c-Si) solar cells has been achieved in mass production in the past few years [136][137], which resulted from a steady improvement in production technology and the implementation of some advanced technologies such as passivating contacts. Among passivating contact approaches, two technologies are dominating the market: a low-temperature approach based on hydrogenated amorphous silicon (a-Si:H) used in silicon heterojunction cell concepts (SHJ) [138], or a high-temperature approach based on polycrystalline silicon thin films (also known as TOPCon - tunnel oxide passivating contact) [59]. The application of these passivating contact technology led to conversion efficiencies up to 26.7% for an interdigitated back contact (IBC) cell architecture [139], and up to 26% for a front and back contact (FBC) cell topology [140].

The TOPCon design is based on the principle of separating the carrier extraction zone from the carrier generation zone using a thin interfacial silicon dioxide layer and highly doped polycrystalline silicon (SiO_2/poly-Si) layer [54]. The first report on the development of TOPCon solar cells was published in 2013 by Fraunhofer ISE [141] in which an ultra-thin SiO_2 layer along with a phosphorous-doped poly-Si layer at the metal-semiconductor interface was used to significantly reduce the surface recombination at the rear side of n-type crystalline silicon solar cells. Ever since the inception of the TOPCon solar cell concept, a phosphorous-doped polysilicon layer has been used for historic reasons, including excellent passivation quality and low contact resistivity [142].

In this chapter, we present the TOPCon front-back contact (FBC) n-type cell concept with a rear junction (RJ) topology, i.e., the cell has a p^+ poly-Si rear emitter and a diffused n^+ front surface field (FSF). Some of the advantages of this cell concept over the traditional TOPCon front junction n-type cell concept topology include:

- Lower the thermal budget of the process sequence due to a lack of high-temperature boron diffusion.
- Because of the RJ configuration, very lightly doped FSF can be used in the non-metallized areas, thereby decreasing parasitic absorption and improving passivation quality.
- Selective n^{++} FSF laser doping under the front contacts is performed using the well-known PERC technology.
- Reducing the silver consumption by decreasing the metal fraction (by increasing the finger pitch) on the front side.
- Using the novel concept of in-situ annealing of APCVD p^+ poly-Si layer during APCVD deposition, thereby omitting the need for an additional high temperature step for crystallization and dopant activation.

The intended industrial TOPCon process routes consist of process steps that are either entirely or partially transferable from the PERC cell, along with a few additional process steps such as the formation of tunnel oxide and the deposition of intrinsic or doped amorphous silicon layers that are required to increase the conversion efficiency [54].

The tunnel oxide layer can be deposited by thermal oxidation, ozone oxidation, chemical oxidation, or plasma-enhanced chemical vapour deposition (PECVD) techniques [143], though in industry thermal oxide is preferred due to its higher thermal stability and structural integrity [144]. The intrinsic/doped silicon layers can be deposited by sputtering [145], low-pressure chemical vapour deposition (LPCVD) [146], atmospheric pressure chemical vapour deposition (APCVD) [82] or PECVD technique [147]. Currently, the industry is transitioning from LPCVD to PECVD technology due to its high deposition rates, single-sided depositions, lower thermal budget and lower equipment and maintenance costs [148]. Irrespective of the deposition technology, all the intrinsic/doped amorphous silicon layers need a high-temperature annealing step, either combined in the diffusion step in case of ex-situ doping of poly-Si layers [149] or a separate annealing step at temperatures of 800-1000 °C, with dwell times typically in the range of 10-30 minutes in case of in-situ doping of poly-Si layers [150]. During the high-temperature annealing step, the deposited amorphous silicon layer crystallizes to form a polycrystalline silicon layer [65], and dopants get activated and homogeneously distributed in the poly-Si layer [66]. Studies have shown that during the high-temperature annealing step, the passivation quality of the layer stack is improved due to interfacial oxide restructuring [151] and the formation of subnanometer pits through the interfacial oxide [152] [153].

Though the high-temperature annealing step is found to be benevolent in many ways, it does increase the overall thermal budget of the process sequence thereby increasing the levelized cost of electricity (LCOE) of TOPCon solar cells in comparison to PERC solar cells [54]. Driessen et al. [154] have presented streamlined processing of TOPCon solar cells by reducing the number of high-temperature process steps, using simultaneous boron emitter diffusion and annealing of tunnel oxide passivated contacts via rapid vapour-phase direct doping. Similar work was also presented by Du et al. [155] where front emitter and rear passivating contacts via continuous PECVD deposition were concurrently prepared in a single high-temperature step. Arpan et al. [156] have shown that rapid thermal annealing (RTA) can be used for annealing purposes in a-Si(p^+) layers. RTA has the fundamental advantage of a short period of annealing time as compared to tube-furnace annealing. Alternatively, Ingenito et al. [69] have demonstrated an innovative fired silicon-based heterojunction (FlaSH) contact formed by a tunnel silicon oxide (SiO_2) capped with a doped silicon-based layer in which the long and slow thermal post-annealing is replaced by a quick fast-firing treatment. In this chapter, we present a new and novel way to anneal amorphous silicon layers using APCVD technology. This method is called "in-situ annealing" where the layer is annealed in the APCVD tool during deposition, thereby avoiding additional high-temperature steps. Solar cell architectures such as rear junction TOPCon (RJ-TOPCon) [140] or fully passivated IBC solar cells [157] can be fabricated in a cost-effective way using the APCVD in-situ annealed p^+ poly-Si layers.

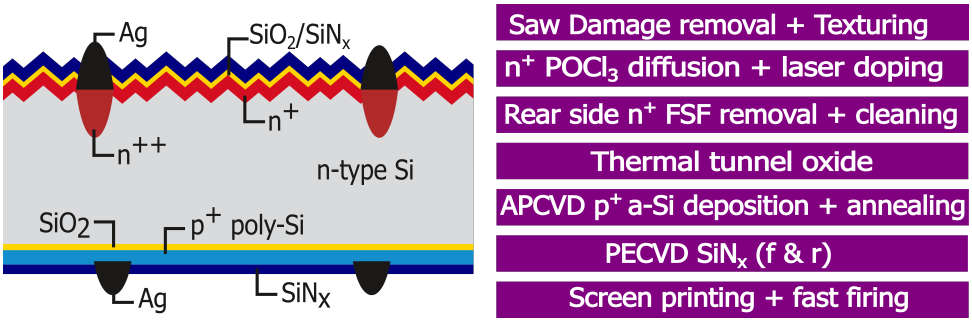


Figure 5.1: A schematic cross-section view of the resulting TOPCon RJ solar cell and process sequence of TOPCon RJ with APCVD-deposited and annealed p+ a-Si emitter.

5.2. Experimental and characterization

5

The cross-section view of the RJ-TOPCon solar cell and its corresponding process sequence is depicted in Figure 5.1. This study was carried out on an industrial-type Cz-Si <100> n-type wafer. All the process equipment used was industrial or industrial-like, such as Centrotherm tube furnaces for thermal interface oxide and $POCl_3$ diffusion. APCVD deposition of p^+ poly-Si layer was carried out on the SCHMID APCVD system. The wet-bench processes were carried out on RENA inline and batch tools. Local laser doping for selective FSF was performed using a frequency-doubled Nd:YVO_4 nanosecond *(ns)* pulse laser with a wavelength = 532 nm. The laser has a flat top profile with a rectangular spot size = 300 x 600 μm^2. The PECVD SiN_x deposition was carried out on Centrotherm PECVD system and fired in a Centrotherm fast firing furnace.

5.2.1. Sample preparation for phosphorous doped FSF and laser doped FSF

Sample preparation for sheet resistance and lifetime measurements

We use 180 µm thick M6 wafer format 5 Ω·cm phosphorous-doped <100> n-type Cz c-Si wafers for lifetime samples while 1 Ω·cm boron-doped p-type Cz c-Si were used for sheet resistance samples. The samples are saw-damage etched in alkaline NaOH solution to remove the saw-cutting-induced damages followed by texturing in an alkaline KOH solution. In order to obtain a lightly doped FSF regions, the $POCl_3$ recipe was optimized only to have a deposition phase without any high-temperature drive-in. Due to the lack of the drive-in phase in $POCl_3$ diffusion, most of the phosphorous is present in the PSG layer. The $POCl_3$ deposition parameters such as deposition temperature, deposition time and the gas flow rates were optimized in order to obtain different $POCl_3$ diffusion profiles with varying dopant surface concentration and junction depths. Subsequntly the LD-FSF samples were then laser-treated to form the laser doped n^{++} FSF regions. The PSG was etched in a 2-vol% HF acid solution at room temperature to evaluate the electrical characteristics of the laser-doped regions, namely R_{sh} and doping profile. The lifetime samples receive a 75-nm thick plasma-enhanced chemical vapour deposition (PECVD) SiN_x layer. The hydrogenation of these samples is done with a peak set temperature of

820°C and at the belt speed of 3 m/min.

5.2.2. Sample preparation for boron doped poly-Si emitter layer

Sample preparation for XRD measurements

We use 100 Ω·cm phosphorous-doped n-type polished 5-inch <100> FZ wafers with a thickness of 250 µm. After the standard piranha cleaning, the samples are coated with a 75-nm thick PECVD SiN_x layer on both sides. The p^+ a-Si layers with the three different temperature profiles (T1, T2 and T3) are deposited symmetrically on both sides using the SCHMID APCVD equipment. The as-deposited APCVD layers without any subsequent high-temperature step are referred to as in-situ annealed samples in this work. Post APCVD layer deposition, half of the samples undergo an additional high-temperature annealing step in a quartz tube furnace at a temperature of 950 °C for 30 minutes and are referred to as ex-situ annealed samples. The native oxide on p^+ poly-Si is removed in HF solution before performing the XRD measurements.

Sample preparation for sheet resistance and lifetime measurements

Figure 5.2 indicates the schematic fabrication process of the *LT* and R_{sh} samples. We use 30 Ω·cm phosphorous-doped <100> n-type Cz c-Si M6 format substrate wafers with a thickness of 180 µm. The samples are saw-damage etched in alkaline NaOH solution followed by Pirahna cleaning to remove the saw-cutting-induced damages and organic and inorganic impurities respectively. To obtain a 1.6-nm thick interfacial SiO_2 layer, dry thermal oxidation is performed in a quartz tube furnace at a temperature of 600 °C for 10 minutes in a 100% oxygen environment followed by 15 minutes of annealing in a 100% nitrogen environment. The in-situ doped p^+ poly-Si layer is deposited using the SCHMID APCVD system. The thickness of the layers and the dopant concentrations can be controlled by adjusting the temperature, gas flows, and belt speed. The APCVD in-situ doped poly-Si(p^+) layer's process parameters are tabulated in Table 1. In order to perform in-situ annealing of the p^+ a-Si layers during the deposition, three different temperature profiles (T1, T2 and T3) are chosen, while the gas flow rates and belt speeds are kept constant in all the recipes. Similar to XRD measurements samples, half of the

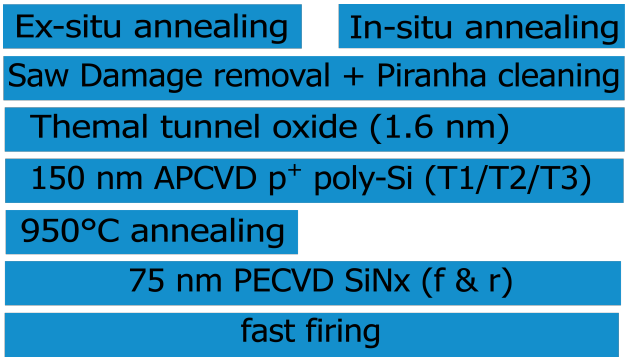


Figure 5.2: A simplified process sequence for the sheet resistance and lifetime measurement samples.

samples from each temperature profile group are externally annealed in a quartz tube furnace at a temperature of 950 °C for 30 minutes i.e. ex-situ annealed samples. The native oxide grown on the poly-Si layers during the APCVD deposition and external annealing is removed in an HF solution to measure the electrical properties of the p^+ poly-Si layers. The sheet resistance is measured using the four-point probe tool from GP Solar.

The process sequence of the symmetrical lifetime samples is similar to that of the above-mentioned R_{sh} samples until the removal of the native oxide after annealing, except that the APCVD p^+ poly-Si layers are deposited on both sides of the wafer. Subsequently, the samples receive a 75-nm thick plasma-enhanced chemical vapour deposition (PECVD) SiN_x layer. The hydrogenation of these samples is done with a peak set temperature of 820°C and at the belt speed of 3 m/min.

5.2.3. Characterization

The GP Solar's 4 Tests PRO was used to measure the R_{sh} using a four-point probe method, and a WEP electrochemical capacitance-voltage (ECV) tool was used to measure the active dopant profile. For measuring the iV_{oc} and J_{0s} of the doped regions, we have used a WCT-120 lifetime tester from Sinton Instruments. For the QSSPC measurements, the actual measured base resistivity and thickness were inputted as input parameter. For the flat passivated symmetrical lifetime samples, an optical constant of 0.95 was selected, whereas an optical constant of 1.1 was chosen for the passivated textured phosphorous-doped FSF symmetrical lifetime samples. The XRD measurements were performed on the Rigaku D/MAX X-ray diffractometer in the θ - 2θ mode with a CuK α source (λ = 0.15418 nm).

5.3. Results and discussion

In this section, the electrical and passivation quality optimization of the different doped regions present in the RJ-TOPCon solar cells i.e. lightly doped n^+ FSF, laser doped n^{++} FSF under the front metallization and SiO_2/p^+ poly-Si passivating contact stack on the rear are studied in detail.

5.3.1. Phosphorous diffused FSF optimization

Due to the presence of a phosphors-doped n^+ front FSF (FSF) in a parallel circuit with the n-type substrate, the effective sheet resistance combing both n-type layers is very low. Hence, unlike convectional TOPCon solar cells with a heavily doped emitter (100–150 Ω/sq), in the RJ-TOPCon configuration, we can afford to have lightly doped FSF regions in the non-metallized regions, provided we have laser-doped FSF regions under the contacts. Hence, in this work, we investigate the influence of the high sheet resistance of n^+ FSF regions on the electrical and passivation quality.

Figure 5.3a shows the typical carrier profile of the FSF n^+ $POCl_3$ diffusion process, and their corresponding sheet resistance are depicted in the legend. A wide range of $POCl_3$ diffusion recipes without the subsequent high drive-in step were studied in this work. The $POCl_3$ deposition was carried out at 760°C for a duration of 20 minutes that yielded 240 Ω/sq FSF with 8 x 10^{19} cm^{-3} surface concentration and junction depth of 100 nm,

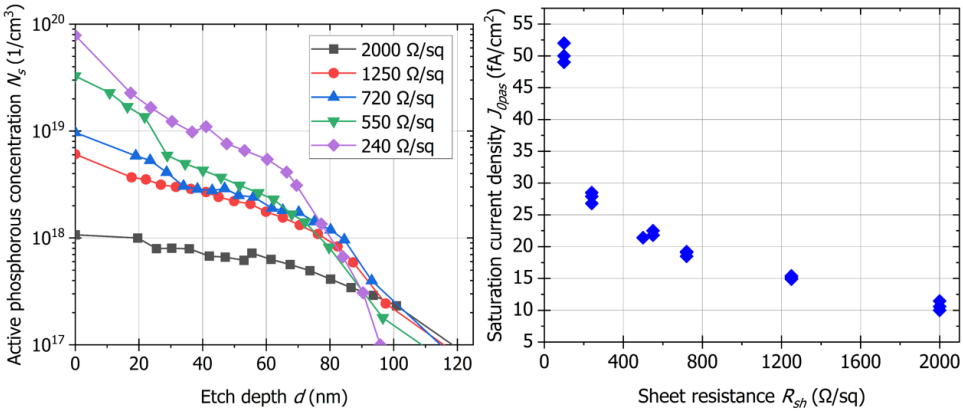


Figure 5.3: (a) Active dopant concentration profiles of the n^+ FSF regions determined from ECV measurements for different $POCl_3$ diffusion recipes. (b) J_{0pas} of n^+ regions measured on symmetric diffused/passivated lifetime samples.

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as depicted by violet line in Figure 5.3a. In order to lower the surface concentration, we performed wet thermal oxidation at 820°C for 15, 30, 40 and 60 minutes (green, blue, red and black lines, respectively, in Figure 5.3a) which led to a gradual decrease in the surface concentration, thereby increasing the sheet resistance from 240 Ω/sq to as high as 2000 Ω/sq. Moving from 240 Ω/sq to 2000 Ω/sq sheet resistance on the n^+ FSF layer lowers the parasitic absorption on the front side of the solar cells, thereby increasing the short circuit current density (J_{sc}) at device level [158].

Figure 5.3b depicts the influence of sheet resistance on the saturation current density of the lifetime structures with symmetrically n^+ doped FSF regions passivated with PECVD SiO_x + SiN_x layer. It can be observed that by increasing the sheet resistance form 240 to 2000 Ω/sq, we can decrease the J_{0s} values from 28 fA/cm^2 to as low as 10 fA/cm^2. The observed results were found to be in good agreement with literature [159]. Hence 2000 Ω/sq would be ideal n^+ FSF layer to be incorporated in RJ-TOPCon solar cells benefiting from low saturation current density and low parasitic absorption.

5.3.2. Phosphorous diffused laser doped FSF optimization

The RJ-TOPCon architecture studies in this work utilizes selective FSF technology which has two major advantages: First, it has low sheet resistance because the high doping concentration under the electrodes lowers the contact resistance, leading to an improvement in the fill factor (FF). Second, better surface passivation on the high sheet resistance area enhances the short-circuit current density (J_{sc}) and open-circuit voltage (V_{oc}) [160]. Figure 5.4a depicts the influence of the (H_p) on the (R_{sh}) of the laser-doped n^{++} c-Si regions. Until 1 J/cm^2, the laser energies are below the melting thresholds of Si; therefore, doping is not possible. In the range of 1 to 2 J/cm^2 we observe sheet resistance decreases with increasing laser fluence and with subsequent increase in the laser fluence after 2 J/cm^2 the sheet resistance saturates.

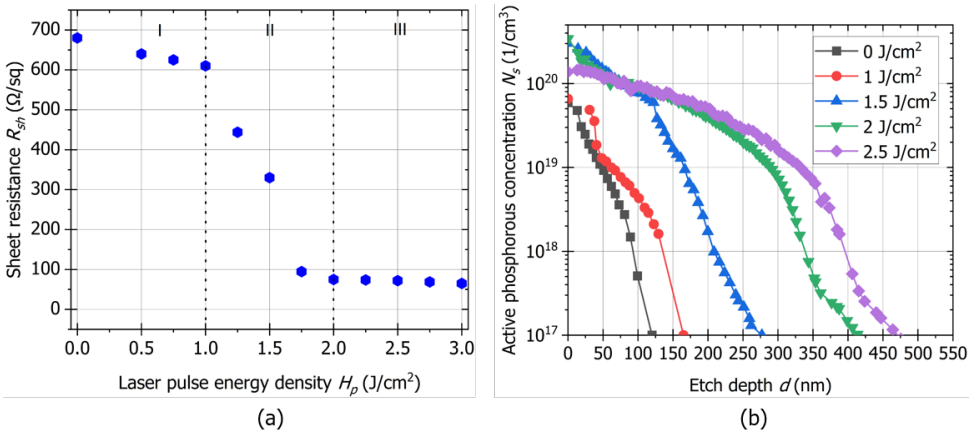

Figure 5.4: (a) Influence of laser pulse energy density (H_p) on the sheet resistance (R_{sh}).(b) Active dopant concentration profiles of the n^{++} selective FSF regions, determined from ECV measurements, for different laser fluence (H_p).

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Figure 5.4b shows the corresponding doping profiles of the laser-doped regions. We observed that for laser fluence below 2 J/cm^2 the surface concentration increases from 8 x 10^{18} cm^{-3} to 7 x 10^{19} cm^{-3} with a slight increase in the junction depth. For higher laser fluence, such as 2.5 J/cm^2, the surface concentration decreases due to evaporation, and a substantial increase in the junction depth is observed from 100 nm to almost 480 nm. Hence 70 Ω/sq obtained by laser doping at 2 J/cm^2 would be ideal n^{++} FSF layer to be incorporated in RJ-TOPCon solar cells benefiting minimal laser-induced damages while maintaining low contact resistivity under the metallized regions.

5.3.3. Boron doped poly-Si emitter optimization

The APCVD equipment used in this study is a SCHMID belt transport system with multiple deposition chambers. The injector head consists of a line source with a separated supply of (SiH_4, B_2H_6 and N_2). The N_2 gas flow in the deposition chamber assures an atmosphere with minimal oxygen (O_2) content. The fundamental principle governing the APCVD silicon layer depositions relies on the fact that thermally dissociated SiH_4 in the deposition chamber would precipitate as an amorphous silicon layer on the hot moving substrate [82]. The belt transport system APCVD system can be categorized into three main zones, namely: pre-deposition zones, deposition zones and post-deposition zones. A systematic study was carried out to understand the influence of each zone on the crystallinity of the as-deposited silicon layers, with the results showing that the post-deposition zone temperature profile is the main parameter that influences layer crystallinity. Using this knowledge, in this study three temperature profiles (T1, T2 and T3) for the layer deposition were shortlisted, in which the pre-deposition temperature profiles were kept constant and the post-deposition temperature profiles were altered keeping the belt speed constant at 12 ipm and are depicted in Figure 5.5.

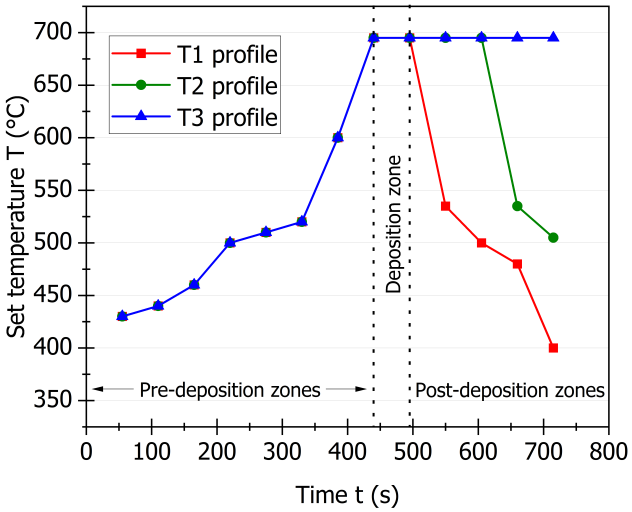

Figure 5.5: The T1, T2 and T3 temperature profiles (see legend) of APCVD p^+ poly-Si layers studied in this work. The set temperature in pre-deposition and deposition zones was kept constant while only the post-deposition set temperature was varied in the T1, T2 and T3 temperature profiles.

Table 5.1: APCVD deposition parameters used in this study.

Process parameter	Input
B_2H_6 flow	48 sccm
SiH_4 flow	120 sccm
Deposition belt speed	12 ipm
Temperature in deposition zone	695°C
Overall deposition time	12 minutes

Crystallization Assessment by XRD measurements

To study the crystal structure of p^+ a-Si/poly-Si layers, X-ray diffraction (XRD) has been performed in a θ - 2θ configuration, using the CuK α radiation. All measurements were performed with 2θ values between 20° and 50° in a continuous mode of 5° per minute with a step size of 0.02° on an X-ray tube operating at 40 kV and 30 mA. In Figure 5.6, the XRD pattern of in-situ annealed APCVD silicon films deposited using the different temperature profiles (T1, T2 and T3) is presented alongside an ex-situ annealed APCVD silicon films deposited at the T3 temperature profile and background pattern coming from the bare FZ wafer with SiN_x. There are two major peaks observed on the bare substrate FZ wafers with SiN_x at 2θ values of 33·06° and 47·74° which correspond to (200) and (220) silicon crystallographic planes respectively [161]. The XRD pattern after the APCVD layer deposition and annealing (in-situ/ex-situ) in most cases, shows three dominant peaks at 2θ values of 28·4°, 33·0° and 47·7° which correspond to (111), (200) and (220) silicon crystallographic planes respectively. The annealed APCVD layers tend to show

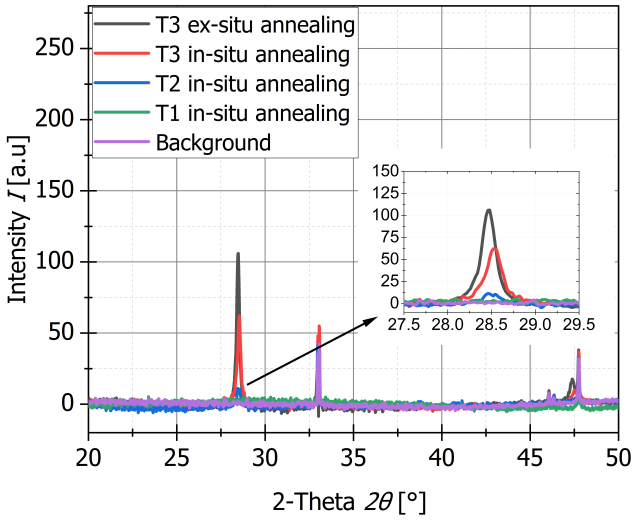

Figure 5.6: The XRD spectra of in-situ and ex-situ (see legend) annealed p^+ poly-Si) layers deposited with T1, T2 and T3 temperature profiles alongside the background measurements on bare FZ wafer.

a (111) preferential orientation attributed to the anisotropic crystallization [162]. This additional peak at 28·4° 2θ was observed for T3 ex-situ annealing APCVD layers, T3 in-situ annealing APCVD layers, T2 in-situ annealing APCVD layers with decreasing order of the peak intensity owing to its decreasing crystallinity order [163]. In the case of T1, in-situ annealed APCVD layers, we do not observe any peak at 28·4° 2θ and the overall profile resembles that of the background, proving that the T1 in-situ annealed APCVD layers are

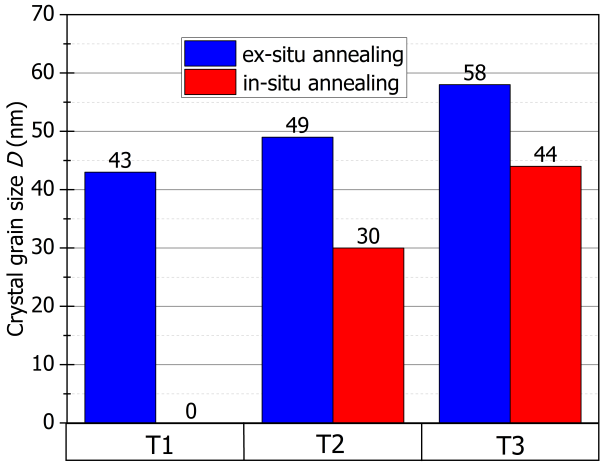

Figure 5.7: The particle size of in-situ and ex-situ (see legend) annealed p^+ poly-Si) layers as a function of deposition temperature profiles T1, T2, and T3 respectively.

amorphous in nature and the overall thermal budget of the T1 profile was not sufficient to crystallize the APCVD amorphous silicon layers.

From the full width at half maximum (FWHM) of the XRD peaks and the wavelength of the X-Ray, the crystallite grain size can be determined using the Debye Scherrer equation [164]. The calculated crystallite grain size from the in-situ and ex-situ annealed APCVD layers deposited at T1, T2 and T3 temperature profiles are depicted in Figure 5.7. In the case of ex-situ annealed APCVD poly-Si layers, due to the additional annealing, we observe a formation of crystal sizes in the range of 43 nm to 58 nm for the deposition temperature profiles T1 and T3 respectively. In the case of in-situ annealing of APCVD silicon layers, the T1 temperature profile remains amorphous whereas for the T2 and T3 temperature profiles, a detectable crystal size from 30 nm to 44 nm was observed respectively. The enhanced crystallization of the T3 temperature profile is due to the higher thermal budget in the post-deposition zones.

Electrical properties of the polysilicon layers

As described in the experimental section, sheet resistance samples were used to study the electrical properties of the p^+ poly-Si layers. Figure 5.8 depicts the R_{sh} data of in-situ annealed p^+ poly-Si layer, ex-situ annealed p^+ poly-Si layer and in-situ annealed p^+ poly-Si layer after fast-firing as a function of the APCVD layer's deposition temperature profiles. Since the R_{sh} values of the ex-situ annealed p^+ poly-Si layer upon fast firing does not change, they were not presented in Figure 5.8. The additional extensive annealing in the quartz tube furnace for 30 minutes at 950 °C for the ex-situ annealed layers leads to better crystallization and dopant activation yielding high-conductive and homogeneous layers in comparison to in-situ annealed layers[149].

Progressing from T1 to T3 temperature profiles, the overall thermal budget during the deposition increases and it strongly influences the in-situ annealed layers (prior to fast-

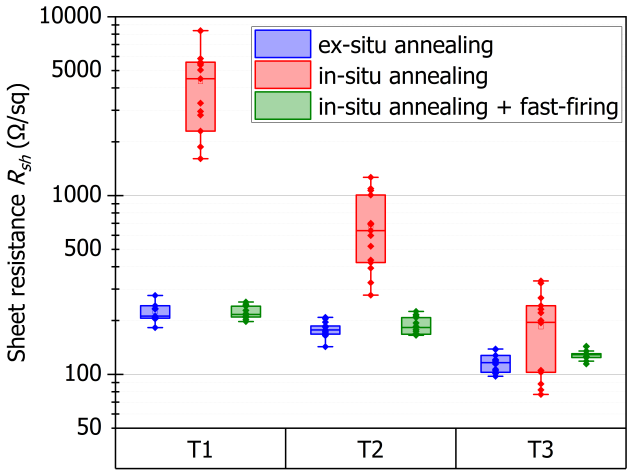

Figure 5.8: Sheet resistance (R_{sh}) of in-situ and ex-situ annealed p^+ poly-Si layers and in-situ annealed p^+ poly-Si layers after fast-firing (see legend) as a function of deposition temperature profiles T1, T2, and T3 respectively.

firing) when compared to ex-situ annealed layers. We obtain highly non-conductive layers with mean R_{sh} of 4000 Ω/□ at the T1 temperature profile to very conductive 195 Ω/□ layers with the T3 temperature profile in the case of in-situ annealed layers. The substantial decrease in the R_{sh} in order of magnitude explains the influence of the temperature in the post-deposition zones of the APCVD system on the deposited layer's crystallinity and electrical properties. The higher mean R_{sh} values and higher standard deviation of the in-situ annealed p^+ poly-Si over the ex-situ annealed p^+ poly-Si layer deposited with the T3 temperature profile can be explained by its lower crystallinity, as also observed from the XRD peaks at 28·4° 2θ in Figure 5.6. The crystallinity of this in-situ annealed p^+ poly-Si layers can further be enhanced by increasing the thermal budget in the post-deposition zones by either increasing the set temperature values in the post-deposition zones or by increasing the total number of post-deposition zones.

Interestingly, the difference in the conductivity and homogeneity of the in-situ annealed p^+ poly-Si layer and ex-situ annealed p^+ poly-Si layer diminishes upon fast-firing. The observed phenomenon implies that the thermal budget used in the fast-firing was sufficient for the dopant activation and crystallization of the in-situ annealed p^+ poly-Si layer. This significant improvement in the in-situ annealed p^+ poly-Si layer's conductivity is speculated to be due to higher peak set temperature (820°C) during fast-firing as compared to the set temperature in the APCVD deposition zone (695°C).

Passivation study on the symmetrical LT samples

As described in the experimental section, symmetrical LT samples were used to study the passivation quality of the p^+ poly-Si layers. Figure 5.9 compares the measured iV_{oc} of the samples with in-situ and ex-situ annealing and their influence on fast firing as a function of the APCVD deposition temperature profiles T1, T2, and T3 respectively. Regardless of the temperature profile, very low iV_{oc} values of 610-645 mV are observed for

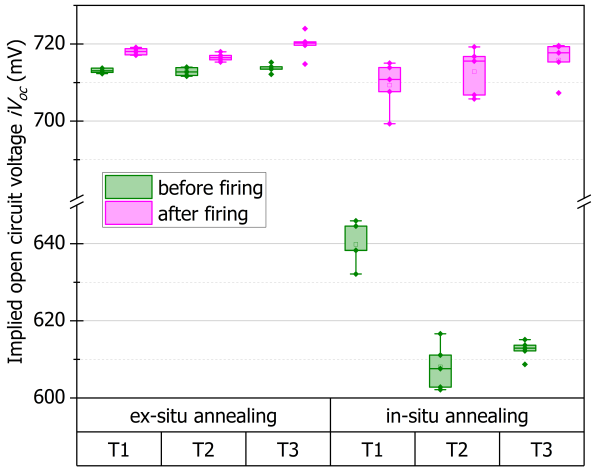

Figure 5.9: Implied open circuit voltage (iV_{oc}) of in-situ and ex-situ annealed poly-Si(p^+) layers before and after fast firing as a function of deposition temperature profiles T1, T2, and T3 respectively.

all in-situ annealed samples prior to fast-firing, whereas samples with ex-situ annealing exhibit much superior passivation quality with iV_{oc} value in the range of 710–715 mV. The difference in the passivation quality prior to fast-firing is speculated to be due to the additional high-temperature step at 950 °C for 30 minutes in the case of ex-situ annealed poly-Si layers. It was demonstrated in Liu et al. [151] and Peibst et al. [152] that during the high-temperature annealing step, the chemical passivation quality is enhanced due to interfacial oxide restructuring thereby reducing acceptor-like state density and the formation of subnanometer pits on the interfacial oxide improves the field-effect passivation. Interestingly, after firing, there is a substantial increase in the passivation quality of the in-situ annealed p^+ poly-Si layers in comparison to the ex-situ annealed p^+ poly-Si layers. This enhancement of the passivation quality is expected to be attributed to the hydrogen diffusion from the in-situ annealed p^+ poly-Si layer and the SiN_x layer in passivating defects at the c-Si/SiO_2 interface [165] during the firing process, as also observed in the fired passivating contacts [69]. Consequently, we obtained the same passivation quality with iV_{oc} of 715–720 mV after fast-firing for both in-situ and ex-situ annealed poly-Si layers deposited with T3 temperature profiles. Besides the high passivation quality demonstrated in this study, recently Okker et al. [166] reported excellent contact resistivity values below 1 mΩ/.cm^2 for such in-situ annealed p^+ poly-Si layers. The combination of low contact resistivity and high passivation quality of these in-situ annealed polysilicon layers makes them an ideal candidate to be used as a cost-effective passivating contact layer.

In this work, we have demonstrated excellent passivation and electrical properties of in-situ annealed p^+ poly-Si layers. The in-situ annealing concept described here for boron-doped poly-Si p^+ poly-Si layers can also be applied to phosphorous-doped poly-Si(n^+) layers. The diffusion/annealing and metallization represent a significant fraction of TOPCon solar cell product costs [54]. By using the novel in-situ annealing of poly-Si layers using APCVD technology, the additional high-temperature annealing step currently used in industry for crystallization of amorphous layer and dopant activation [65] can be omitted from the process sequence thereby lowering the production costs and simplifying the process sequence of the solar cells concepts based on passivating contact.

5.4. Summary

In this work, we present the results of process optimization of our n-type TOPCon RJ solar cell concept. For the fabrication of the TOPCon RJ solar cells, we present the optimizations performed for selecting the suitable $POCl_3$ diffusion recipe that provides less parasitic absorption and good passivation quality. The laser doping settings were optimized to obtain a highly doped n^{++} c-Si layer under the metal contacts with minimal laser-induced damage. APCVD technology can be used to perform in-situ annealing on boron-doped amorphous Si layers to obtain highly conductive and crystallized poly-Si with good passivation quality. The temperature profile in the post-deposition heat zones of the SCHMID APCVD system was found to be the most important parameter of the in-situ annealing process. In this work, three different deposition temperature profiles were studied. The in-situ/ex-situ annealed APCVD layers showed a (111) preferential silicon crystallographic orientation with increasing peak intensity owing to its increasing crystallinity order progressing from T1 to T3 deposition temperature profiles. Similar to

the structural properties, the sheet resistance measurements show an increase in conductivity when progressing from T1 to T3. It was observed that both, in-situ and ex-situ, annealed poly-Si layers deposited with T3 temperature profile yield comparable crystal sizes and sheet resistance values. It was also observed that fast-firing plays a vital role in enhancing the crystallinity and conductivity of the in-situ annealing poly-Si layers. Prior to fast-firing, the in-situ annealed poly-p^+ poly-Si layers exhibited poor passivation quality but post-fast-firing both in-situ and ex-situ annealed poly-Si layers exhibit excellent passivation quality with an iV_{oc} of 715–720 mV. This enhancement in the passivation quality especially for in-situ annealed p^+ poly-Si layers post fast-firing is expected to be attributed to the hydrogen diffusion from the p^+ poly-Si layer and the SiN_x layer in passivating defects at the c-Si/SiO_x interface. In conclusion, we have demonstrated a novel method for annealing amorphous silicon layers during layer deposition with comparable structural, electrical, and passivation quality to that of ex-situ annealing of poly-Si silicon layers in a quartz tube furnace at 950 °C for 30 minutes. These in-situ annealed layers deposited with APCVD technology can be used for lean process sequence and cost-effective way for fabricating solar cell concepts like RJ-TOPCon and fully passivated IBC solar cell. Incorporation of the individual optimized process parameters in Quokka3 simulation model demonstrated efficiency exceeding 24% for this cell concept.

6

Firing-induced depassivation of phosphorous doped poly-Si layer

TOPCon (Tunnel Oxide Passivated Contact) solar cells are making significant strides in the photovoltaic (PV) market due to their high efficiency and potential for cost reduction. Their ability to work seamlessly with established production methods, like screen printing, renders them an appealing choice for manufacturers. Recently, studies have demonstrated that the passivation quality of the phosphorus-doped n^+ TOPCon structures that are capped with a PECVD silicon nitride (SiN_x) layer degrades upon fast-firing. In this work, we compare the firing stability of n^+ polysilicon (poly-Si) layers by varying the method of doping (i.e., in-situ vs. $POCl_3$ diffused ex-situ doped layers), the process sequence of $POCl_3$ diffused ex-situ doping (i.e., $POCl_3$ diffusion followed by high temperature annealing step and vice versa) and the capping layer (i.e. PECVD SiN_x, PECVD SiO_2 + SiN_x, $POCl_3$ PSG + PECVD SiN_x) on top of $POCl_3$ diffused ex-situ doped n^+ poly-Si layer. Our experiments revealed that in-situ doped n^+ poly-Si layers capped with PECVD SiN_x were found to be more stable in comparison to the $POCl_3$ diffused ex-situ doped n^+ poly-Si layers. Secondly, for $POCl_3$ diffused ex-situ doped n^+ poly-Si layers capped with PECVD SiN_x, the samples that were annealed prior to $POCl_3$ diffusion were found to more prone to firing induced depassivation. Finally, we found that by having a dielectric layer with low hydrogen content, such as PECVD silicon oxide (SiO_2) or phosphosilicate glass (PSG), between the poly-Si and PECVD SiN_x layers significantly improves the firing stability of the passivating contacts stack.

This chapter is based on the following submitted manuscript submitted to IEEE Journal of Photovoltaics, (Manuscript ID: JPV-2024-02-0062-R) : **V. V. Kuruganti**, O. Isabella, and V. D. Mihailetchi, "Firing-induced depassivation of n^+ polysilicon layers used in passivated contact solar cells".

6.1. Introduction

To meet the growing efficiency demands and to address PERC solar cell design challenges, the industry is transitioning toward carrier-selective passivating contact solar cell concepts. These concepts involve physically decoupling the heavily doped regions and metal contacts from the silicon substrate [54]. There are two primary methods for achieving carrier-selective passivating contacts: low-temperature Heterojunction with Intrinsic Thin Layer (HIT) cells [167] also known as silicon heterojunction (SHJ), or high-temperature Tunnel Oxide Passivated Contact (TOPCon) cells [59]. The HIT solar cells utilize a thin intrinsic amorphous silicon layer to isolate heavily doped and metal contact regions from the silicon substrate, whereas TOPCon cells employ a thin tunnel oxide for this purpose. TOPCon solar cells are currently favored over HIT solar cells for mass production due to their streamlined processes, compatibility with existing PERC infrastructure, reduced capital expenditure [54], and superior thermal stability. These characteristics facilitate the ongoing utilization of cost-effective traditional screen-printing methods for the metallization of solar cells [168]. In screen-printed solar cells, a fast-firing step is crucial for contact formation [169]. During this step, the fluidized glass frit in the paste etches through the anti-reflection coating layer and reacts with the doped silicon (Si), facilitating the formation of silver (Ag) crystallites at the glass-Si interface. This formation of Ag crystallites is essential for establishing superior ohmic contact, a critical aspect of solar cell performance [170]. Therefore, the primary objective of the fast-firing step is to ensure a strong metal-semiconductor contact while preserving the good passivation quality and long-term stability of the solar cells [171].

However, recent studies have raised concerns about the impact of high-temperature fast-firing steps on the passivation quality of n^+ poly-Si layers. Kang et al. [172] examined various factors affecting the firing stability of n^+ poly-Si passivating contacts, including peak firing temperature, type of interfacial SiO_2, method of poly-Si deposition, variations in dielectric coating, and diffusion conditions. Their findings suggest that hydrogen diffusion is responsible for the changes in the surface passivation quality of the poly-Si/SiO_2 passivating contacts. Conversely, Hollemann et al. [173] proposed that the degradation of n^+ poly-Si layers during firing stems from thermally-induced stress at the poly-Si/SiO_2 interface. More recently, Linke et al. [174] demonstrated that the firing stability of the poly-Si/SiO_2 stack is influenced by the annealing temperature of the n^+ poly-Si layer.

While extensive research has focused on investigating the effects of firing on poly-Si passivating contacts, the origins of this issue and effective mitigation strategies are not well understood. This study aims to address this gap by providing a comprehensive analysis of the impact of firing on the n^+ poly-Si passivating contacts. The aim is to evaluate how firing influences surface passivation, taking into account factors such as the method of phosphorus doping (i.e., in-situ and $POCl_3$ diffused ex-situ doping), variations in the process sequence of $POCl_3$ diffused ex-situ doping (i.e., $POCl_3$ diffusion followed by high temperature annealing step and vice versa), and the variation in the capping layer structure.

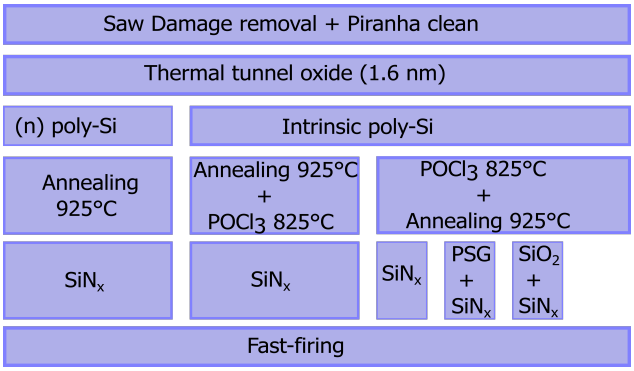

Figure 6.1: Simplified representation of the process flow and the different groups studied in this work, namely: i) Method of doping (i.e. in-situ and $POCl_3$ ex-situ doped n^+ poly-Si layers; ii) Variation in the process sequence of $POCl_3$ diffused ex-situ doping (i.e. Poly Doping Annealing (PDA) and Poly Annealing Doping (PAD) n^+ poly-Si layers); and finally, iii) Variation in the capping layer (i.e. PECVD SiN_x, PECVD SiO_2 + SiN_x, $POCl_3$ PSG + PECVD SiN_x) and without any capping layer.

6.2. Experimental and characterization

6.2.1. Sample preparation for sheet resistance and symmetrical lifetime samples.

The various groups studied in this work and their corresponding process flow are depicted in Figure 6.1. We prepare symmetric *LT* samples on M6 wafer format 180 µm thick n-type (phosphorous-doped) <100> Cz, 4-Ω.cm Si wafers. The saw damage etching (SDE) and piranha cleaning are carried out on RENA batch tools. All the high temperature thermal processes are carried out on an industrial-like centrotherm tube furnaces. To obtain 1.6-nm thick interficial oxide, dry thermal oxidation in a quartz tube furnace at a temperature of 600 °C for 10 minutes in a 100% oxygen (O_2) atmosphere, followed by 15 minutes of annealing in a 100% nitrogen (N_2) atmosphere. Both intrinsic and in-situ n^+ doped 150-nm thick poly-Si layers are deposited using LPCVD technology. The in-situ n^+ doped poly-Si were prepared by LPCVD technology using silane (SiH_4) as the Si precursor, phosphine (PH_3) as the dopant precursor, and N_2 as the carrier gas whereas the intrinsic poly-Si layer is deposited in the absence of PH_3. The intrinsic poly-Si layers are subsequently ex-situ doped using $POCl_3$ tube diffusion. Two different $POCl_3$ ex-situ doped n^+ poly-Si layers are studied in this work: 1) Poly Doping Annealing (PDA), which involves $POCl_3$ diffusion of the intrinsic poly-Si layer at 825 °C for 20 minutes followed by annealing in a 100% N_2 environment at 925 °C for 30 minutes, and 2) Poly Annealing Doping (PAD) ex-situ doping, where the intrinsic poly-Si layer is first annealed at 925 °C for 30 minutes in a 100% N_2 atmosphere followed by $POCl_3$ diffusion at 825 °C for 20 minutes. In case of in-situ n^+ doped poly-Si layers, separate annealing step is performed in a 100% N_2 environment at 925 °C for 30 minutes. The phosphosilicate glass (PSG) layer formed during the $POCl_3$ diffusion is preserved in some samples while removed for all other samples in a 2% HF solution. Subsequently, different capping layers were deposited on the samples; such as PECVD SiN_x, PECVD SiO_2 + SiN_x, and $POCl_3$ PSG + PECVD SiN_x are deposited using centrotherm PECVD system. Finally, firing is carried out

in a centrotherm fast-firing furnace.

In order to accurately measure the electrical properties of the doped poly-Si layers, we use 180-µm thick 1-Ω.cm p-type (boron-doped) Cz Si wafers. The processing sequence of R_{sh} samples was similar to that of the above-mentioned *LT* samples up to the high-temperature annealing step. The phosphosilicate glass (PSG) layer formed during the $POCl_3$ diffusion is completely etched back in a 2% HF solution.

6.2.2. Characterization tools

A four-point probe tool from GP Solar and an electrochemical capacitance-voltage (ECV) tool from WEP were used to measure the electrical properties of the doped regions, such as R_{sh} and the active doping profile. A WCT-120 lifetime tester from Sinton Instruments was used to measure the implied open circuit voltage (iV_{oc}) and saturation current density (J_0) of the n^+ poly-Si regions. The spatial homogeneity of the passivation quality is measured using an in-house voltage calibrated photoluminescence (PL) tool. The extracted iV_{oc} values from Quasi Steady State Photoonductance (QSPPC) are used to convert the PL images into iV_{oc} mapping. The Oypmpus OLS 400 LEXT laser scanning microscope (LSM) is used for analysing the surface topology of the samples.

6.3. Results and Discussion

6.3.1. Electrical properties of phosphorous-doped poly-Si layers

As described in the experimental section, R_{sh} samples were used to study the electrical properties of the n^+ poly-Si layer. The electrically active phosphorous doping profiles and their corresponding R_{sh} (see legend) for the in-situ and the $POCl_3$ diffused ex-situ doped n^+ poly-Si layers are shown in Figure 6.2. The R_{sh} for both in-situ and PDA doped n^+ poly-

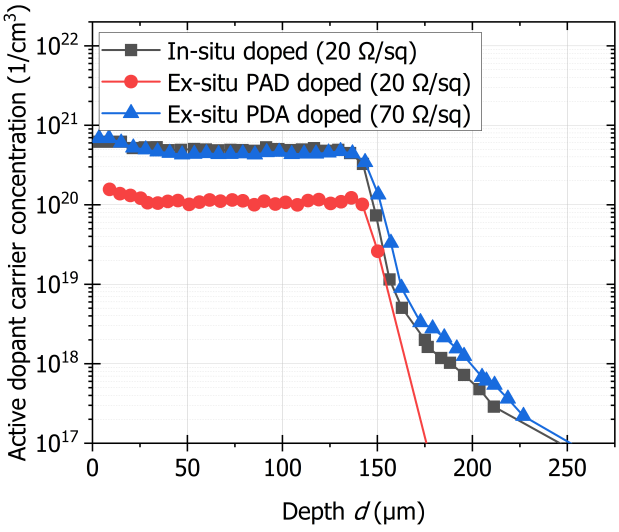

Figure 6.2: Carrier concentration profiles and their corresponding R_{sh} (see legend) of the in-situ and the $POCl_3$ diffused ex-situ doped n^+ poly-Si layers used in this study.

Si is 20 ohm/sq, and they have similar carrier concentration profiles. This suggests the annealing temperature following dopant deposition, rather than the doping method itself, that limits dopant diffusion within the poly-Si layer. The measured dopant concentration aligns with the phosphorous solubility limit in silicon at the annealing temperature of 925°C [175].

When comparing the Poly Annealing Doping (PDA) and Poly Doping Annealing (PAD) doped n^+ poly-Si layers, it is evident that the PAD n^+ poly-Si layer has at least four times lower electrically active dopant than the PDA poly-Si layer. Although both $POCl_3$ diffused ex-situ doped n^+ poly-Si layers were subjected to identical $POCl_3$ deposition conditions in terms of gas flow and temperature, and received the same overall thermal budget, the PDA doped n^+ poly-Si are annealed at 925°C for 30 minutes after dopant incorporation subsequently leading to better dopant activation in comparison to that of the PAD doped n^+ poly-Si [176]. Consequently, this resulting in an increased in the concentration of electrically active phosphorus within the n^+ poly-Si layer. Moreover, strong in-diffusion in the case of PDA doped n^+ poly-Si layer is observed due to high temperature annealing post-dopant deposition [174].

6.3.2. In-situ vs. Ex-situ phosphorous-doped poly-Si layers

Figure 6.3 illustrates the variation of J_0 with increasing temperature of peak firing zones for both in-situ and PDA ex-situ doped n^+ poly-Si layers. Before fast firing step, we observed a very good passivation quality with J_0 ranging from 3-4 fA/cm^2 and iV_{oc} values between 738–740 mV for both poly-Si layers. The screen-printed solar cells are typically fired at a set peak temperature ranging from 750°C to 825°C, depending on the metallization paste used [171], [177]. The in-situ doped n^+ poly-Si layers remained stable upon firing within

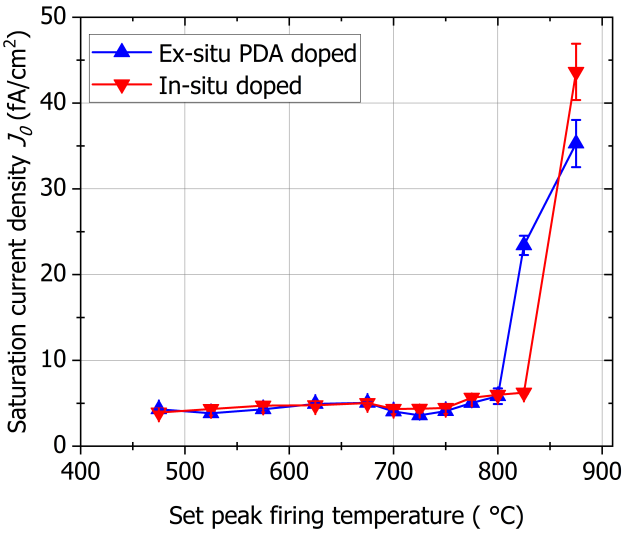

Figure 6.3: The QSSPC determined saturation current density J_0 of in-situ doped and PDA ex-situ doped n^+ poly-Si layers as a function of set peak firing temperature.

this temperature range. However, the PDA ex-situ doped n^+ poly-Si layers exhibited a loss in passivation quality at 825°C, evidenced by an increase in J_0 values from 3 to 10 fA/cm^2. Figure 6.7 displays iV_{oc} converted PL images for all the various n^+ poly-Si groups studied in this research. At 825 °C, lower passivation quality was observed in the wafer corners for the PDA ex-situ doped n^+ poly-Si layers. However, at fast firing temperatures ranging from 850–900 °C, a significant increase in J_0 was observed for both in-situ and PDA ex-situ doped n^+ poly-Si layers, consistent with findings by Kang et al. [172] at such high firing temperature ranges attributed to stress-induced defect formations at the SiO_2/poly-Si interface.

Within the industrial firing range, although the passivation loss in PDA ex-situ doped n^+ poly-Si layers was not excessively high, it could impact the V_{oc} at the device level [178]. Hence, in the section 6.3.4, we investigated several variations in the capping layers to enhance the firing stability of $POCl_3$ diffused ex-situ PDA doped n^+ poly-Si.

6.3.3. Process sequence variation of ex-situ phosphorous-doped of poly-Si layers

Figure 6.4 depicts the J_0 variation with respect to increasing temperature of peak firing zones for both $POCl_3$ diffused ex-situ doped n^+ poly-Si layers. Excellent passivation quality with J_0 as low as 4 fA/cm^2 were obtained for both $POCl_3$ diffused ex-situ doped n^+ poly-Si layers before firing. The passivation loss difference between PAD and PDA ex-situ doped n^+ poly-Si layers continues to increase as the firing temperature increases. In the industrial firing range, the PDA ex-situ doped n^+ poly-Si layers is found to be firing stable until 825 °C, while the PAD ex-situ doped n^+ poly-Si layers have very high J_0 values throughout the firing range. Images of in-situ n^+ poly-Si layers and both $POCl_3$ diffused

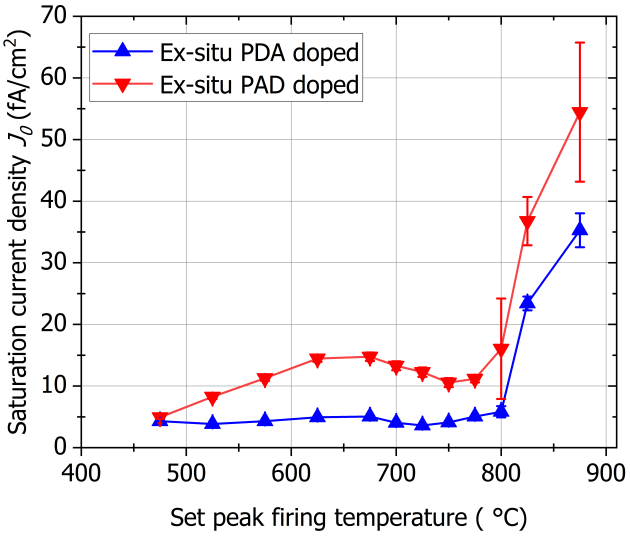

Figure 6.4: Saturation current density , measured by QSSPC, of PAD vs. PDA ex-situ doped n^+ poly-Si layers as a function of set peak firing temperature.

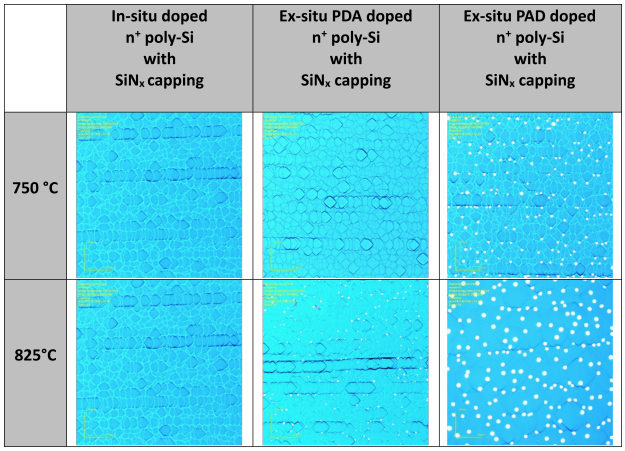

Figure 6.5: LSM images of the wafer surface topology for in-situ and $POCl_3$ diffused ex-situ doped n^+ poly-Si layers after fast firing at 750 °C and 825 °C.

ex-situ doped n^+ poly-Si layers fired at industrial temperatures are shown in Figure 6.5. Already at 750 °C, we observe PAD ex-situ doped n^+ poly-Si layers blisters. At 825 °C, the blister density and blister size increase in the case of the PAD ex-situ doped n^+ poly-Si layers, as also confirmed by its high J_0 values, whereas the PDA ex-situ doped n^+ poly-Si layers shows much lower blistering.

The PDA ex-situ doped n^+ poly-Si layers are much more firing stable across the range of firing temperatures compared to PAD ex-situ doped n^+ poly-Si layers. Linke et al. [174] have highlighted the significant impact of annealing temperature on the firing stability of poly-Si layers. Observations revealed that reducing the annealing temperature below the optimal value results in a more pronounced deterioration in passivation quality post-fast-firing. However, the study did not explicitly state whether this optimum annealing step is crucial before or after the deposition of dopants in the poly-Si layer, as the study was carried out on in-situ doped n^+ poly-Si layers. From the observed passivation quality and LSM images in Figure 6.4 and Figure 6.5, we hypothesized that the annealing step post-dopant deposition plays a vital role in determining the firing stability of the n^+ poly-Si layer. In order to confirm this hypothesis, the sister samples from the PAD ex-situ doped n^+ poly-Si layers before deposition of the PECVD-SiN_x capping layer were annealed again at 925 °C for 30 minutes (i.e., the PADA ex-situ doped n^+ poly-Si layers). Upon performing a similar firing variation study, the PADA ex-situ doped n^+ poly-Si layers showed no signs of firing-induced passivation losses until 825 °C, as was also observed for the PDA ex-situ doped n^+ poly-Si layers 6.4. As a result, we draw the conclusion that the annealing temperature post-dopant deposition affects the firing stability of the $POCl_3$ diffused ex-situ doped n^+ poly-Si layer.

6.3.4. Capping layer variation of ex-situ phosphorous-doped of poly-Si layers

Figure 6.6 compares the effect of fast firing on the PDA ex-situ doped n^+ poly-Si samples with different capping layers. The samples fired without any capping layer exhibit the most pronounced degradation in the surface passivation quality, with J_0 values gradually increasing from 7 fA/cm^2 before firing to 70 fA/cm^2 already at 700 °C and 100 fA/cm^2 at 850 °C. The samples fired with SiN_x were not strongly impacted by firing up to 800 °C but exhibit degradation in J_0, increasing from 4 to 10 and 25 fA/cm^2 after firing at 825 °C and 850 °C, respectively. The samples that have PSG + PECVD SiN_x stack and PECVD SiO_2 + PECVD SiN_x dual stack maintain excellent passivation quality throughout the range of the set peak firing temperature.

We observed that samples without a capping layer displayed the most significant passivation loss among all the groups, as shown in the Figure 6.6. The occurrence of blister formation in the uncapped samples after firing cannot be attributed to hydrogen-induced effects. This is due to two main factors: firstly, the absence of an external hydrogen source in the form of a capping layer, and secondly, the poly-Si layer is deposited using LPCVD at 690 °C followed by annealing at 925 °C for 30 minutes. During this annealing process, any hydrogen atoms present should have diffused out of the layers. We speculate that the observed phenomenon is likely caused by stress-induced defect formation, possibly triggered by the difference in thermal expansion coefficients between the interfacial SiO_2 (0.5×10^{-6}/K) [179] , c-Si (2.6 to 4.3×10^{-6}/K) [180], and poly-Si (2.7 to 2.9×10^{-6}/K) layers [181]. This difference is more pronounced during the firing process compared to tube furnace annealing, as shown in Hollemann et al. [173] research.

In comparison to samples without any capping layer, the samples with capping layers

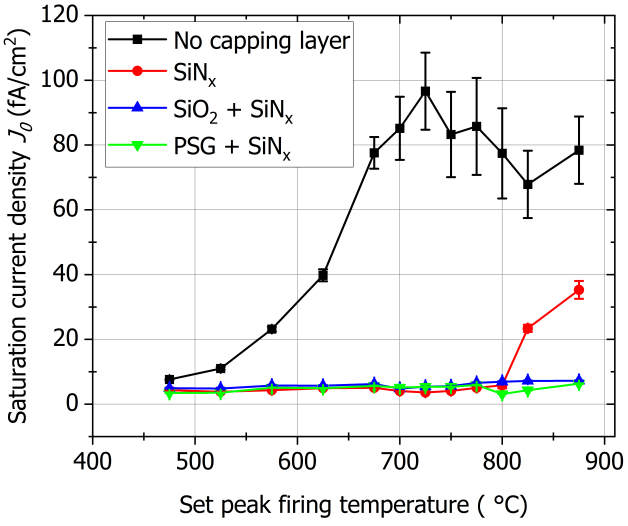

Figure 6.6: Saturation current density , measured by QSSPC, of PDA ex-situ doped n^+ poly-Si samples with various capping layer as a function of set peak firing temperature.

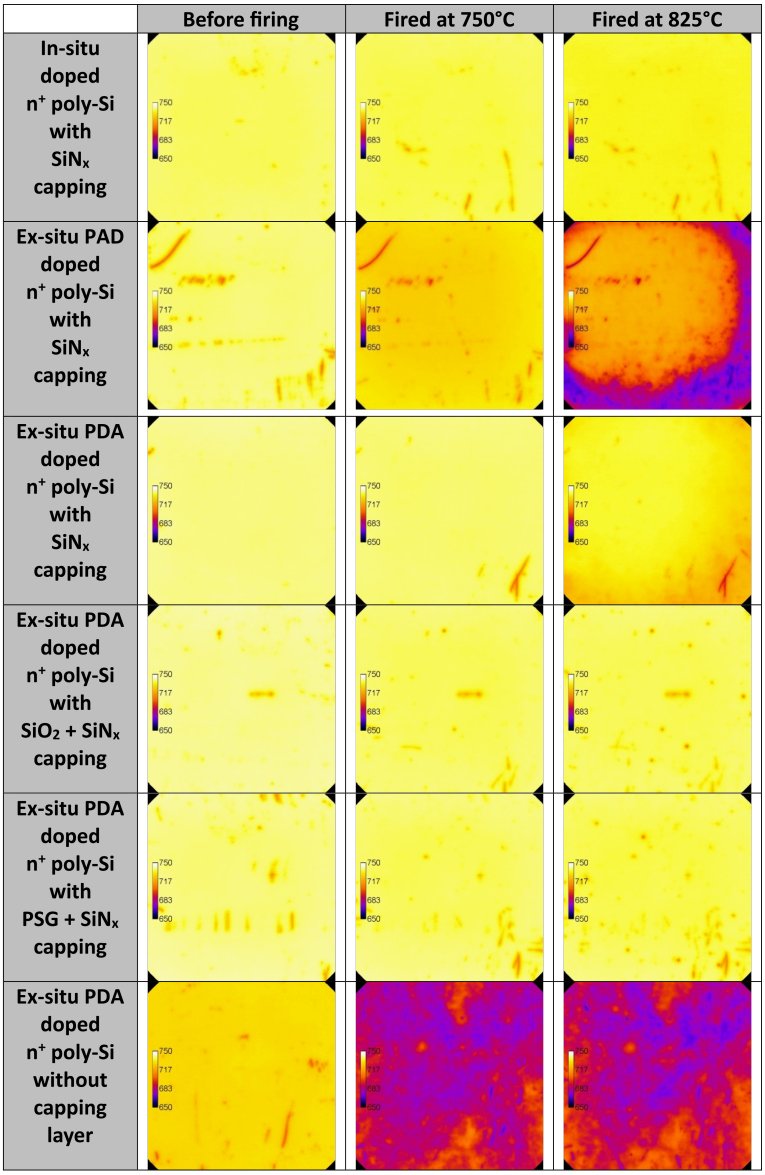

Figure 6.7: Implied open circuit voltage calibrated photoluminescence images for the different n^+ poly-Si groups studied in this work

are found to be much more firing stable, which implies that hydrogen passivates interface defects resulted from the thermal stress at the interface during firing [182]. Though the samples capped with PEVCD SiN_x were found to be firing stable until 800 °C, from 825 °C we started to observe a gradual decrease in the passivation quality. This degradation

behaviour depends strongly on the processing conditions, such as the dielectric coating layers and the firing temperature. Kang et. al. [172] hypothesized that the amount of hydrogen at the c-Si/SiO_2 interface could be the decisive factor for the depassivation by blistering in the SiO_2 n^+ poly-Si stack. It was found that an excess amount of hydrogen around the interficial SiO_2 can deteriorate the passivation quality of the poly-Si stack. An effective approach to reducing the hydrogen concentration at the interface between SiO_2 and n^+ poly-Si is to include an intermediate layer with minimal hydrogen content between the two layers. Kang et al. [172] demonstrated that the AlO_x layer effectively impedes the diffusion of excessive hydrogen from reaching the c-Si/SiO_2 interface. In this investigation, we illustrate that alternative intermediate layers, such as a PECVD SiO_2 or a $POCl_3$ PSG layer, can enhance the firing stability of ex-situ phosphorous-doped poly-Si layers. These layers have the potential to prevent excess hydrogen from reaching the c-Si/SiO_2 interface.

PECVD SiO_2 + SiN_x dual stack offers additional benefits when used in the TOPCon solar cells. Studies have shown that increasing the thermal budget during co-firing enhances the contact formation between the Ag/Al paste and the front-side p^+ TOPCon emitter [183]. However, in standard industrial co-firing, a relatively low temperature is employed to prevent the Ag paste from penetrating the SiO_2 n^+ poly-Si passivating contact stack on the rear side [184]. Moreover, an increased thermal budget during co-firing leads to surface-related degradation on the n^+ poly-Si layer covered with a SiN_x layer, as documented in the research by Liu et al. [185] and validated in our own investigations. The utilization of an intermediate PECVD SiO_2 or PSG layer between the n^+ poly-Si layer and SiN_x layer provides an elegant solution to overcome all the aforementioned drawbacks, thus further enhancing the efficiency of TOPCon solar cells.

6.4. Summary

We showed that upon fast firing the poly-Si/SiO_2 stack undergoes depassivation. This observed loss of passivation after fast firing could negatively impact the performance of solar cells. Therefore, this study delves into the different factors influencing the passivation quality of the n^+ poly-Si layer stack after fast firing.

We compared the firing stability of in-situ and PDA ex-situ doped n^+ poly-Si layers based on the method of doping and they exhibited similar passivation quality for the majority of the firing range. However, for peak firing temperatures above 825 °C, the PDA ex-situ doped n^+ poly-Si layers's poly-Si/SiO_2 stack began to blister, resulting in a significant reduction in passivation quality. In contrast, a similar phenomenon for the in-situ doped n^+ poly-Si layer occurred from 900 °C onwards, pointing out its enhanced firing stability.

We compared the firing stability of PAD and PDA ex-situ doped n^+ poly-Si layers based on the process sequence of $POCl_3$ diffused ex-situ doping. It was observed that the PDA ex-situ doped n^+ poly-Si layers exhibited significantly better firing stability across the entire firing temperature range compared to the PAD ex-situ doped n^+ poly-Si layers. Furthermore, as firing temperatures increased, the disparity in passivation loss widened. This discrepancy in firing stability was attributed to the absence of an annealing step post-dopant deposition in the case of PAD ex-situ doped n^+ poly-Si layers. However, an additional annealing step post-dopant deposition in PAD ex-situ doped n^+ poly-Si layers

demonstrated comparable firing stability to that of PDA ex-situ doped n^+ poly-Si layers.

We compared different capping layers, such as PECVD SiN_x, PECVD SiO_2 + SiN_x, $POCl_3$ PSG + PECVD SiN_x, and samples without any capping layer on the PDA ex-situ doped n^+ poly-Si layers and it was observed that samples lacking a capping layer experienced the most significant degradation in passivation quality. This degradation after firing is thought to be due to thermally-induced stress at the poly-Si/SiO_2 interface, as demonstrated by Hollemann et al. Samples with SiN_x demonstrated firing stability up to 800 °C; however, a substantial decrease in passivation quality was observed thereafter. We speculate that is caused by an excess of hydrogen at the SiO_2 layer interface, as shown by Kang et al. To mitigate the excess hydrogen reaching the SiO_2 interface, an intermediate layer such as PECVD SiO_2 or $POCl_3$ PSG layer with low hydrogen content is placed between the poly-Si layer and the SiN_x layer. The use of this intermediate layer stack extended the firing temperature range up to 900 °C.

In conclusion, we demonstrated that there are multiple factors that can influence the fast-firing stability of phosphorus-doped poly-Si layers used in passivating contacts solar cells. Though we have demonstrated that in-situ doped n^+ poly-Si have better firing stability in comparison to PDA ex-situ doped n^+ poly-Si layers, industry favours the latter. This is due to $15\%_{abs}$ higher cost of ownership (COO) of the LPCVD step as a consequence of lower deposition rates for the in-situ doped poly-Si layers [54]. Among the two different routes of ex-situ doping (i.e. PAD and PDA) studied in this work, the process sequence involving doping followed by high-temperature annealing, which aligns with the conventional method of ex-situ doping, demonstrated better firing stability. Finally the use of bi-layer stack with low hydrogen content, such as PECVD silicon oxide (SiO_2) or phosphosilicate glass (PSG), between the poly-Si and PECVD SiN_x layers significantly improves the firing stability of the passivating contacts stack.

7

Conclusions and outlook

7.1. Conclusions

This chapter marks the conclusion of this dissertation. After having framed in Chapter 1 the societal motivation and technical challenges of this research, Chapter 2 addressed the historical development of c-Si solar cells alongside the fundamentals of APCVD technology.

Chapter 3 of the thesis outlines the fabrication process of IBC solar cells incorporating an innovative patterning technique. Although the enhanced oxidation characteristics of heavily doped n^{++} c-Si substrates are well-established in the literature, the novelty of this study is in utilizing this property to actively structure the rear side of IBC solar cells. Laser doping is utilized to selectively enhance the phosphorus surface concentration by more than an order of magnitude in the locally lasered regions. This selectivity in the phosphorus surface concentrations results in a 2.8-fold increase in oxide thickness under the laser-treated regions compared to non-lasered regions during wet thermal oxidation. We exploit this selectivity in oxide thickness to pattern the rear side of the IBC solar cells. Additionally, this research shows that after patterning, if the residual oxide beneath the laser-doped n^{++} BSF regions is thicker than 20 nm, it can serve as a diffusion barrier during the BBr diffusion process, which forms the emitter layer on the non-lasered regions. Proof-of-concept solar cells were fabricated using this patterning technique.

The work presented in Chapter 4 provides a compelling case for adopting APCVD-doped glass layers instead of the conventional industrial tube furnace diffusion methods involving BBr_3 and $POCl_3$, with the goal of developing cost-effective and industrially feasible IBC solar cells. Following the deposition of doped glass layers, a high-temperature annealing step becomes necessary. In this study, the high-temperature annealing process was optimized to achieve several objectives: driving dopants of both polarities, preventing the formation of a boron-rich layer in p^+ doped c-Si, and growing in-situ SiO_2 at the Si/dopant glass interface. A systematic investigation of the etching rate of glass layers in an acidic solution was performed. By exploiting the differential etch rates between in-situ grown SiO_2 and the doped glass layer, complete removal of the doped glass was

achieved. The residual in-situ SiO_2 post-etching was subsequently encapsulated with PECVD SiO_x to function as a universal passivation stack for both polarities. At the device level, conversion efficiencies comparable to those of state-of-the-art ZEBRA solar cells were achieved.

Chapter 5 of this study introduces n-type substrate RJ-TOPCon solar cells, known as HoBIT solar cells, developed by ISC Konstanz. This cell design features an APCVD p^+ poly-Si rear emitter and a $POCl_3$ diffused n^+ FSF, along with selectively laser-doped n^{++} FSF regions under the front metal contacts. The chapter systematically optimizes each doped layer in terms of their electrical and passivation properties and outlines the potential process fabrication route for the HOBIT solar cells. The $POCl_3$ diffusion and subsequent wet thermal oxidation were fine-tuned to achieve a very lightly doped FSF under the non-metallized FSF regions. Laser doping settings was optimized to minimize laser-induced damages while maintaining high conductivity under the laser doped n^{++} FSF regions under the front contact. Additionally, an in-situ annealing process was developed to crystallize boron-doped amorphous silicon layers deposited by atmospheric pressure chemical vapor deposition (APCVD) into boron-doped polycrystalline silicon layers. The results demonstrate successful crystallization of boron-doped amorphous silicon layers can be achieved by fine-tuning the temperature profiles in the post-deposition zones of the APCVD tool. It was observed that the hydrogenation processes during fast firing significantly enhance the passivation quality as well as electrical properties of the in-situ annealed poly-Si(p^+) layers.

Chapter 6 delves into a detailed examination of the impact of fast-firing on the passivation quality of phosphorus-doped n^+ poly-Si. This research compares the firing stability of n^+ poly-Si layers by varying the method of doping (i.e., in-situ versus $POCl_3$ diffused ex-situ doping), the process sequence of $POCl_3$ diffused ex-situ doping (i.e., $POCl_3$ diffusion at 825 °C followed by high-temperature annealing step at 925 °C on the intrinsic poly-Si layer and vice versa), and the capping layer on top of n^+ poly-Si layer. Our findings demonstrate that in-situ doped n^+ poly-Si layers exhibit greater stability compared to the $POCl_3$ diffused ex-situ doped n^+ poly-Si layer. Regarding the ex-situ doped n^+ poly-Si, the sequence of annealing and doping plays a pivotal role in determining the firing stability of poly-Si layers. It was observed that annealing at high temperature prior to dopant incorporation leads to higher induced depassivation. Finally, we demonstrate that incorporating a dielectric layer with low hydrogen content, such as PECVD silicon oxide (SiO_2) or phosphosilicate glass (PSG), between the poly-Si and PECVD SiN_x layers significantly enhances the firing stability of the passivating contacts stack.

7.2. Outlook

Drawing from the findings outlined in this thesis, the following suggestions are proposed for future research:

- The utilization of the increased oxidation characteristics of n^{++} Si layers in the novel patterning technique is not limited solely to diffused junctions, as demonstrated in this study. It may also be applied to the state of the art passivating contact interdigitated back contact (IBC) solar cells. This work has also highlights the fundamental differences to be expected when working on patterning of polysilicon

solar cell concepts based on passivating contact.

- In this study, we illustrate the application of in-situ annealing for crystallizing boron-doped amorphous silicon layers utilizing APCVD technology. Similar research avenues can explore implementing in-situ annealing for phosphorus-doped amorphous silicon layers, thereby reducing the cost of ownership (COO) and the overall thermal budget in the current industrial standard TOPCon solar cells.

- A systematic study was carried out to optimize all the doped regions and process sequence of the RJ-TOPCon solar cells realized on the n-type substrate material. With optimized process parameters, simulation results indicate conversion efficiencies exceeding 24%. The HOBIT project, financed by the German Federal Ministry for Economic Affairs and Climate Action and coordinated by ISC Konstanz and SCHMID, is currently advancing further research to achieve such high conversion efficiencies at the device level. The author of this thesis will continue to contribute to the progress and development of this project aimed at fabricating RJ-TOPCon solar cells as an alternative to the industrial standard conventional TOPCon solar cells.

- The expertise acquired in using APCVD glass layers for diffused junction IBC solar cells and APCVD doped silicon layers for RJ-TOPCon solar cells could be merged to fabricate the ultimate evolution structure in c-Si solar cells – passivating contact IBC solar cells utilizing APCVD technology.

- This research opens up the viability of low-cost, high-efficiency c-Si bottom cells for future tandem solar cell architectures.

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Curriculum Vitæ

Vaibhav Venkat KURUGANTI

Vaibhav Venkat Kuruganti studied Mechanical Engineering at The Gandhian Institute of Technology and Management, Hyderabad, India, and graduated in 2016. Afterwards, he completed the Master of Science programme in Sustainable Systems Engineering at the University of Freiburg, Freiburg, Germany, in the year 2019. Prior to pursuing his PhD, he worked as a researcher at the Fraunhofer-Institut für Solare Energiesysteme ISE. In 2020, he started his PhD program at TU Delft and ISC Konstanz, under the supervision of Prof. Olindo Isabella and Prof. Miro Zeman, with Dr. Valentin D. Mihailetchi as his daily advisor. His research focuses on the fabrication of high-efficiency solar cell concepts using APCVD technology. Vaibhav Venkat Kuruganti has significant experience working on industrial production lines and has contributed to various publicly and industry-funded projects. He has a strong record of successfully transitioning innovative technology from the laboratory to large-scale manufacturing.

Education

2012–2016	GITAM University (Bachelors of Technology) Mechanical Engineering
2016-2019	University of Freiburg (Masters of Science) Sustainable Systems Engineering *Thesis:* Temperature dependent resistivity and mobility analysis in silicon wafers *Promoter:* Prof. Dr. Stefan Glunz *Promoter:* Prof. Dr. Anke Weidlich *Supervisor:* Dr. Jonas Haunschild
2020-2024	Delft University of Technology (PhD.) Electrical Engineering *Thesis:* Atmospheric Pressure Chemical Vapour Deposition for high-efficiency c-Si solar cell concepts *Promoter:* Prof. Dr. Olindo Isabella *Promoter:* Prof. Dr. Miro Zeman *Supervisor:* Dr. Valentin Dan Mihailetchi

List of Publications

Peer-reviewed journal articles

1. **V. V. Kuruganti**, D. Wurmbrand, T. Buck, S. Seren, M. Zeman, O. Isabella, F. Geml, H. Plagwitz, B. Terheiden, and V. D. Mihailetchi, "Industrially viable diffused IBC solar cells using APCVD dopant glass layers", Solar Energy Materials and Solar Cells 2023, 251 112111.

2. **V. V. Kuruganti**, A. Mazurov, S. Seren, O. Isabella, and V. D. Mihailetchi, "In Situ Annealing of Boron-Doped Amorphous Silicon Layers Using APCVD Technology", IEEE Journal of Photovoltaics,14(1),74-79 (2023).

3. **V. V. Kuruganti**, O. Isabella, and V. D. Mihailetchi, "Structuring Interdigitated Back Contact Solar Cells Using the Enhanced Oxidation Characteristics Under Laser-Doped Back Surface Field Regions", physica status solidi (a) (2024): 202300820.

4. **V. V. Kuruganti**, O. Isabella, and V. D. Mihailetchi, "Firing stability of phosphorous-doped poly-Si layers used in passivated contact solar cells", manuscript submitted to IEEE JPV.

Conference contributions

1. **V.V. Kuruganti**, R. Kopecek, S. Seren, and V. D. Mihailetchi,"Process fabrication of cost-effective IBC solar cells using APCVD glass layers", in 38^{th} European Photovoltaic Solar Energy Conference and Exhibition, 2021, 293–297.

2. H. Chu, **V. V. Kuruganti**, R. Roescu, C. Peter, and V. D. Mihailetch, "Interplay of IBC cell's front surface doping, passivation quality, and stability under ultraviolet light exposure", in 38^{th} European Photovoltaic Solar Energy Conference and Exhibition, 2021, 311–316.

3. **V. V. Kuruganti**, R. Kopecek, S. Seren, O. Isabella, and V. D. Mihailetchi, Investigation on the Passivation Quality of Ex-Situ Doped (p^+) and (n^+) Poly-Si Layers for IBC Solar Cells,in 39^{th} European Photovoltaic Solar Energy Conference and Exhibition, 2022, 98–101.

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Selected contributions prior PhD study

1. **V. V. Kuruganti**, J. Haunschild, A. Brand, S. Al-Hajjawi, . Rein, and S. Glunz, "Non-destructive approach for measuring base resistivity of emitter-diffused, partially-processed wafers using temperature-stage QSSPC", in 36^{th} European Photovoltaic Solar Energy Conference and Exhibition, 2019 361-365.

2. M. Pengerla, S. Al-Hajjawi, A. Brand, **V. V. Kuruganti**, J. Haunschild, N. Schuler, K. Dornich, and S. Rein,, "Comparing microwave detected photoconductance, quasi steady state photo-conductance and photoluminescence imaging for iron analysis in silicon", in 37^{th} European Photovoltaic Solar Energy Conference and Exhibition, 2020 317-321.