

Photonic hybrid assembly through flexible waveguides

Wörhoff, Kerstin; Prak, Albert; Postma, F.; Leinse, A; Wu, Kai; Peters, T. J.; Tichem, M.; Amaning-Appiah, B.; Renukappa, V.; Vollrath, G.

DOI

[10.1117/12.2227814](https://doi.org/10.1117/12.2227814)

Publication date

2016

Document Version

Final published version

Published in

Proceedings Silicon Photonics and Photonic Integrated Circuits V

Citation (APA)

Wörhoff, K., Prak, A., Postma, F., Leinse, A., Wu, K., Peters, T. J., Tichem, M., Amaning-Appiah, B., Renukappa, V., Vollrath, G., Balcells-Ventura, J., Uhlig, P., Seyfried, M., Rose, D., Santos, R., Leijtens, X. J. M., Flintham, B., Wale, M., & Robbins, D. (2016). Photonic hybrid assembly through flexible waveguides. In L. Vivien, L. Pavesi, & S. Pelli (Eds.), *Proceedings Silicon Photonics and Photonic Integrated Circuits V* (Vol. 9891). Article 98911P (Proceedings of SPIE; Vol. 9891). SPIE. <https://doi.org/10.1117/12.2227814>

Important note

To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Copyright

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy

Please contact us and provide details if you believe this document breaches copyrights.
We will remove access to the work immediately and investigate your claim.

PROCEEDINGS OF SPIE

[SPIDigitalLibrary.org/conference-proceedings-of-spie](https://spiedigitallibrary.org/conference-proceedings-of-spie)

Photonic hybrid assembly through flexible waveguides

K. Wörhoff
A. Prak
F. Postma
A. Leinse
K. Wu
T. J. Peters
M. Tichem
B. Amaning-Appiah
V. Renukappa
G. Vollrath
J. Balcells-Ventura
P. Uhlig
M. Seyfried
D. Rose
R. Santos
X. J. M. Leijtens
B. Flintham
M. Wale

SPIE.

Photonic Hybrid Assembly Through Flexible waveguides

K. Wörhoff*^a, A. Prak^a, F. Postma^a, A. Leinse^a, K. Wu^b, T.J. Peters^b, M. Tichem^b, B. Amaning-Appiah^c, V. Renukappa^c, G. Vollrath^c, J. Balcells-Ventura^d, P. Uhlig^d, M. Seyfried^e, D. Rose^e, R. Santos^f, X.J.M. Leijts^f, B. Flintham^g, M. Wale^g, D. Robbins^h

^aLioniX BV, P.O. Box 456, 7500 AL Enschede, The Netherlands;

^bDelft University of Technology, Department of Precision and Microsystems Engineering, Mekelweg 2, 2628CD Delft, The Netherlands;

^cAifotec AG; Herpfer Str. 40, 98617 Meiningen, Germany;

^dIMST GmbH, Carl-Friedrich-Gauss-Str. 2, D-47475 Kamp-Lintfort, Germany;

^eficonTEC Service GmbH, Rehland 8, 28832 Achim, Germany;

^fCOBRA Research Institute, Eindhoven University of Technology, PO Box 513, 5600 MB Eindhoven, The Netherlands;

^gOclaro Technology Ltd., Caswell, Towcester NN12 8EQ, UK;

^hWillow Photonics LTD., 4, Wappenham Road, Abthorpe, Towcester, Northants, NN12 8QU, UK

ABSTRACT

Fully automated, high precision, cost-effective assembly technology for photonic packages remains one of the main challenges in photonic component manufacturing. Next to the cost aspect the most demanding assembly task for multi-port photonic integrated circuits (PICs) is the high-precision ($\pm 0.1 \mu\text{m}$) alignment and fixing required for optical I/O in InP PICs, even with waveguide spot size conversion. In a European research initiative – PHASTFlex - we develop and investigate an innovative, novel assembly concept, in which the waveguides in a matching TriPleX interposer PIC are released during fabrication to make them movable. After assembly of both chips by flip-chip bonding on a common carrier, TriPleX based actuators and clamping functions position and fix the flexible waveguides with the required accuracy.

Keywords: Photonic assembly, photonic integrated circuit, MEMS, eutectic bonding, InP, TriPleX, LTCC, flip-chip

1. INTRODUCTION

In this paper we report on the development of a fully automated, high precision, cost-effective assembly technology for next generation hybrid photonic packages. Multiple Photonic ICs (PICs) will be assembled in hybrid packages combining the best of different material platforms for a wide range of applications and performance. InP^{[1],[2]} PICs with active functions will be combined with passive low-loss, low-cost TriPleX^[3] PICs.

PIC fabrication can now be done using generic foundry-based processes^[4], bringing the cost of a large application specific PIC (ASPIC), into the range ~10-100€, which is within the budget of many applications developers. However, current assembly and packaging technology^[5] still leads to custom-engineered solutions thereafter; packaging is an order of magnitude more expensive, and this is a major bottleneck to further market penetration.

The most demanding assembly task for multi-port PICs is the high-precision ($\pm 0.1 \mu\text{m}$) alignment and fixing required for efficient optical coupling to high contrast waveguides such as InP or silicon photonics, even with waveguide spot size conversion. The PHASTFlex EU initiative^[6] proposes an innovative and novel concept, in which the waveguides near the chip facet of a matching interposer TriPleX PIC are released during fabrication to make them movable^[7]. Actuators and fixing functions, integrated in the same PIC, position and fix the flexible waveguides in the optimal position (peak out-coupled power). Although this approach can be considered to be a high-end, high-tech solution, low-cost implementation may be achieved through automation of design tools and assembly processes.

(* k.worhoff@lionixbv.nl; <http://www.lionixbv.nl/>)

For the proof of concept of this novel fully automated assembly approach, InP and TriPleX photonic chips with test circuits have been designed and realized.

Both chips, InP and TriPleX, are flip chip bonded onto a multi-layer LTCC carrier enabling 3D routing of DC and RF signals over a wide range of density and complexity levels. A fiber array unit can be connected to the mode size matched input ports of the TriPleX chip. An exploded view of the assembly is depicted in Figure 1. The assembly is carried out in two steps: (1) alignment with moderate precision using flip-chip bonding on a dedicated assembly machine and (2) flexible waveguide actuation and fixing using the on-chip micro-mechanical functions.

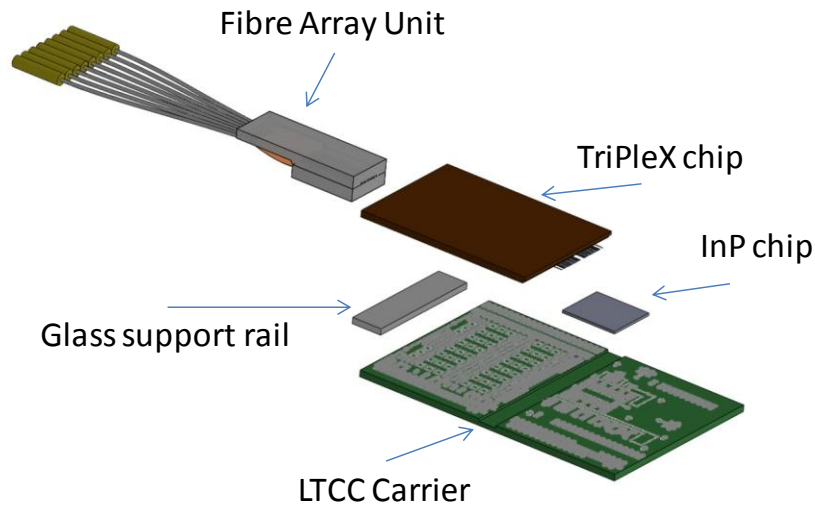


Figure 1. Exploded drawing of assembly showing the piece parts required - Fiber array unit (FAU), TriPleX chip (backside view), glass rail for mechanical FAU support, InP chip (backside view), LTCC carrier (top view).

2. ASSEMBLY CONCEPT

2.1 PIC coupling

A widely applied approach to low-loss coupling from photonic waveguides with small mode field diameters (MFD), such as is case for an InP PIC platform, to standard optical fibers (MFD $\sim 10 \mu\text{m}$), is the introduction of an interposer chip at the InP – fiber interface. The TriPleX photonic platform has been demonstrated to be well-suited for interposer functionality^[8], as the size of the mode field can be widely adapted on-chip by tailoring the waveguide geometry through adiabatic tapering sections. Typical mode sizes in the in-plane (MFD_x) and out-of-plane (MFD_y) directions are summarized in Table 1, which distinguishes InP technology platforms with and without vertical spot-size convertors (SSC).

Table 1. Typical Gaussian $1/e^2$ mode field diameters of InP photonic waveguides.

With vertical SSC		Without vertical SSC	
MFD _x [μm]	MFD _y [μm]	MFD _x [μm]	MFD _y [μm]
3.0	2.6	3.0	0.9

Besides matching the modal field sizes of the waveguides, control of the axial separation between chips is of importance for good coupling efficiency. The axial coupling sensitivity for typical mode sizes is indicated in Figure 2, where for reference the standard single mode fiber to fiber sensitivity is also shown. From this plot we can easily see that with the present SSC a reasonable working distance for passive chip placements exists whereby a separation of $1.5\mu\text{m} \pm 0.5\mu\text{m}$

results in an acceptable coupling penalty (< 0.4 dB/facet). This target gap value sets the required placement accuracy of the assembly machine, since waveguide separation in this direction cannot be controlled by the on-chip alignment functions.

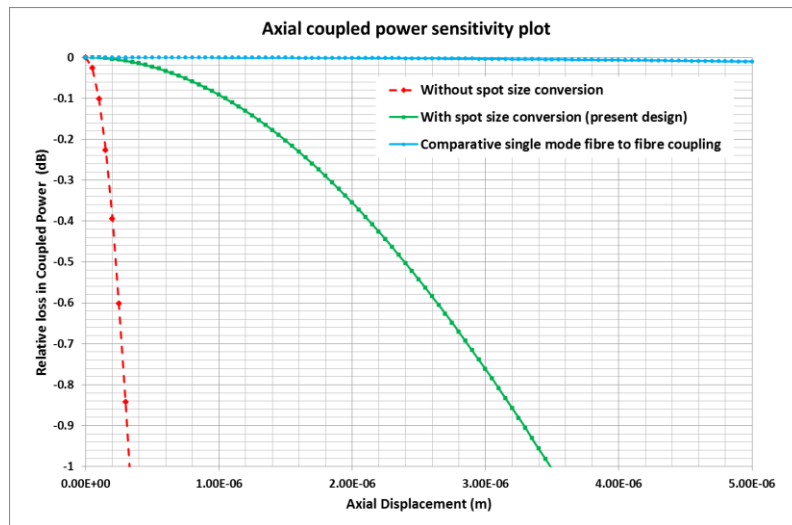


Figure 2. Relative coupled power sensitivity to axial separation of InP PIC and TriPleX waveguides with and without SSC's (Single mode fibre to fibre sensitivity given for reference).

2.2 Flexible waveguide actuation and fixing

To enable the active alignment several mechanical functions, as depicted schematically in Figure 3, are integrated on the TriPleX chip: (1) flexible waveguides connected by a cross-bar, (2) integrated MicroElectroMechanical Systems (MEMS) actuators for in-plane and out-of-plane motion, and (3) fixing function to lock the waveguides in their final location once the alignment is optimized. Integration of these functions in the TriPleX photonic platform, which is composed of SiO_2 - Si_3N_4 layer stacks, is a highly innovative aspect as the stress in these materials - opposed to classical silicon-based MEMS - has a significant impact on design and fabrication.

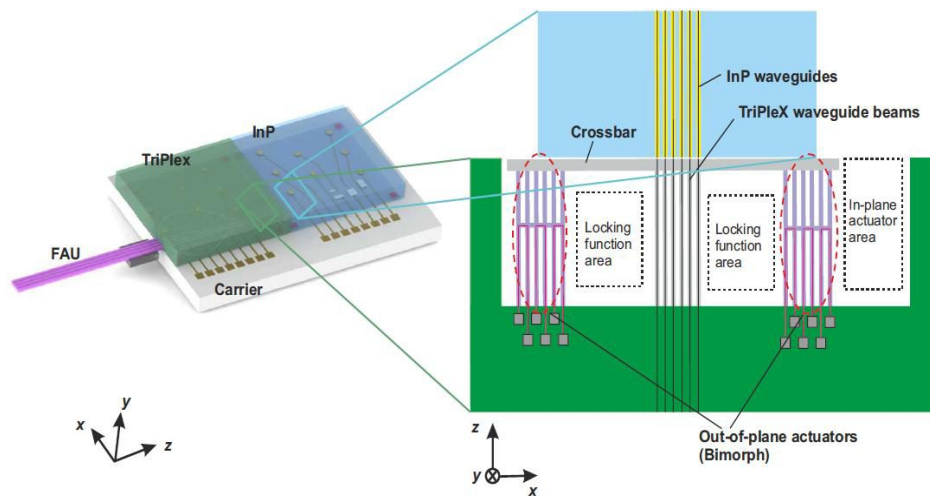


Figure 3. 3D-schematic overview of the photonic assembly (left) and 2D-top-view drawing of the waveguide alignment scheme (right) including coordinate definition. TriPleX and InP chips are flip-chip bonded on a common carrier. The waveguide beams on the TriPleX chip and two sets of bimorph actuators are connected at their free ends by a crossbar structure. In the fine alignment step the cross bar is actuated in the in-plane (x) and out-of-plane (y) directions, positioning the waveguide beam array with respect to the InP waveguide channels. Space allocation for the in-plane actuator and locking functions is schematically shown.

The proposed MEMS alignment features will allow three degrees of freedom in translation (T) and in rotation (R) in their movement driven by electrical heating. The active alignment functions cover the translational movement in both x and y directions as well as rotation in z-direction. The three degrees of freedom are achieved by: in-plane actuation (T_x) out-of-plane actuation of both actuators (T_y) and tilt of waveguide plane by motion of single out-of-plane actuator (R_z). Demonstrated motion ranges are of the order of several microns^[9] implying that the pre-alignment accuracy of the flip-chip assembly in the plane normal to the optical axis can be set at typically 2-4 μm . Sufficiently high initial placement accuracy in the other directions (T_z , R_x and R_y) has to be established by the passive pre-alignment, i.e. a more stringent requirement on the assembly machine capacity.

2.3 Passive alignment and flip-chip bonding

The pre-alignment accuracy required for the coarse alignment step derives from an analysis of the optical coupling as well as the MEMS functional boundaries. For the spacing between the two optical chips a maximum gap of 2 μm (i.e. $1.5 \pm 0.5\mu\text{m}$) is the target. Chip bonding accuracy in the in-plane and out-of-plane directions has to be within up to 4 μm to ensure overlap with the MEMS motion range in the fine alignment step. For meeting the assembly accuracy criteria appropriate choices have to be made on the assembly machine as well as for the flip-chip bonding process. Moreover the assembly process has ultimately to be capable of volume fabrication.

For the assembly machine the placement accuracy requirement mainly translates into choices for mechanical movement and for the viewing principles, cameras and pattern recognition, in combination with appropriate fiducials implemented on both the chips and carrier. A fully automated assembly including the fine-tuning level of the MEMS actuators will be achieved through a probe card integrated in the assembly machine.

In the case of the flip-chip process a eutectic bonding scheme based on thin film metallization has been chosen. This metallization approach is well suited for sequential chip assembly and high alignment accuracy. The eutectic bonding process is based on fluxless AuSn solder with an 80-20 weight composition and requires a soldering temperature around 280°C. Thin film metallization terminated with an 80-20 Au-Sn film of 2-5 μm -thickness is usually applied onto the carrier. The fabrication of the thin film metallization stack being terminated by AuSn was carried out by sputtering in combination with lithography based patterning. This approach combines a volume manufacturing capability^[10] with high placement accuracy^[11] ($\pm 3 \mu\text{m}$). On the other hand the thin film method places requirements on the carrier flatness and smoothness, which should be within 2 μm over the carrier area. Therefore the carrier tiles are lapped and polished prior to the application of the top metallization stack.

3. REALIZATION AND TESTING

3.1 Photonic chips and carrier

InP chips have been designed and fabricated on both TU/e and Oclaro technology. The TU/e chips contain modulators for testing of RF performance of the transition between the LTCC carrier and the on-chip modulators. Moreover, investigation of the MEMS alignment using 250 μm and 50 μm waveguide pitch configurations is enabled by a rotation-symmetric layout of the TU/e chip. The InP chips from Oclaro contain an array of monitor photo-detectors along six functional and two monitoring waveguides. This layout is well suited for testing the alignment mechanism of the MEMS actuators using various loopback waveguide arrangements on the TriPleX chip in combination with an external light source.

The photonic functionality of the TriPleX chip layout focuses on the interposer functionality including various optical feed-back loops for alignment control at the InP as well as fiber interface. Pictures of all realized chips are shown in Figure 4.

The LTCC carrier (Figure 4, right) has been designed to accept all combinations of the matching InP and TriPleX chips, and provides for the necessary DC and RF interconnects between the probe cards and the active circuit elements. In order to accommodate the complexity of the combined optical, electrical DC and electrical RF connectivity the carrier electrical layout is distributed over five interconnecting LTCC layers (of which only the top metallization is visible in the picture of the carrier). The LTCC and conductor materials are DuPont951 and gold, respectively. On the LTCC carrier in

Figure 4 the two InP chip bonding areas to the left, the TriPleX area to the right, and the probe card contact arrays at the top are visible.

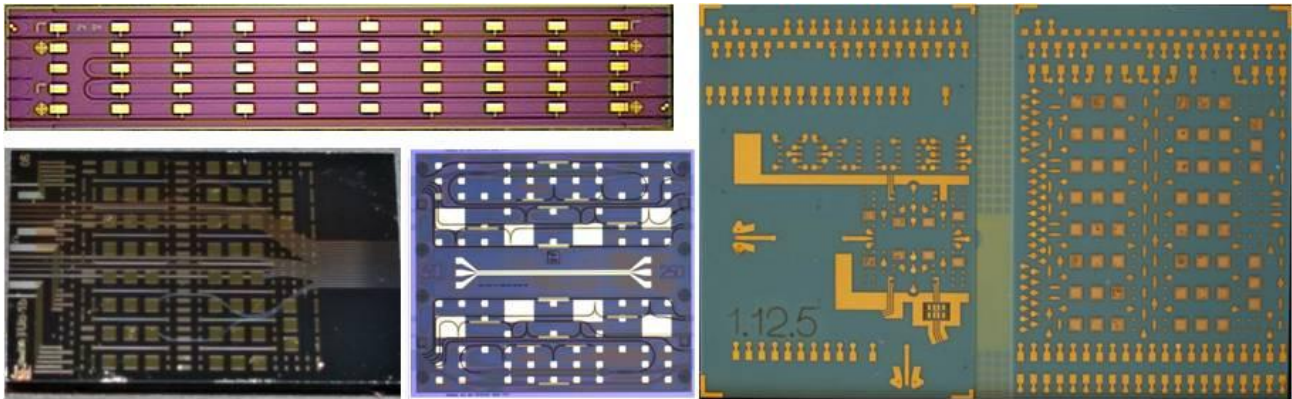


Figure 4. Pictures of fabricated piece parts: Oclaro InP chip (top left), TriPleX chip (bottom left), TU/e InP chip (bottom middle), LTCC carrier (right).

3.2 Flexible waveguide actuation

The principle of the fabrication scheme for MEMS-based flexible waveguides and actuators is depicted in Figure 5. The starting point is the TriPleX waveguide stack with silicon nitride (Si_3N_4) channel waveguides buried in a 16- μm thick silicon oxide (SiO_2) cladding. On this waveguide stack a 2-5 μm thick poly-silicon film is deposited. The distinct mechanical properties of the silicon film on top of the free-standing silicon oxide MEMS structures result in bimorph actuation upon heating. The actuation is initiated through heater elements in a metallization stack on top of the poly-Si film. The MEMS structures are patterned into the front side of the wafer by etching through the dielectric waveguide stack. Finally, the free-standing structures are obtained by locally removing the silicon from the back side of the wafer.

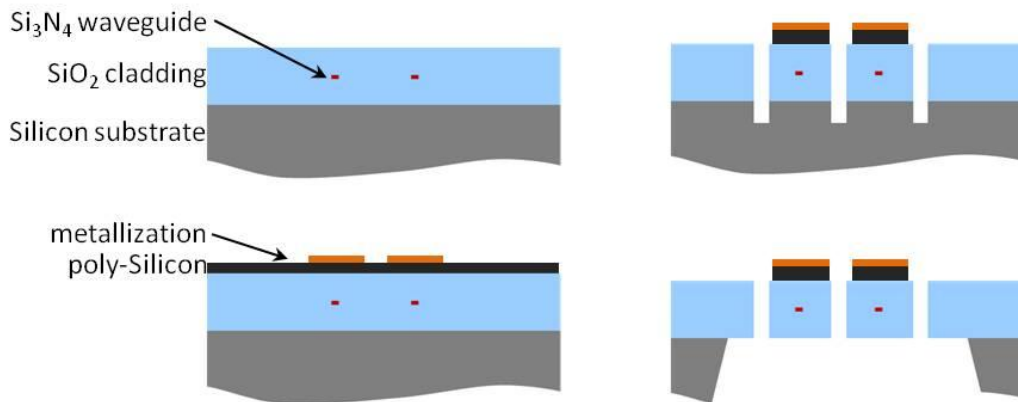


Figure 5. MEMS fabrication scheme: TriPleX waveguide cross-section (top left), deposition of poly-silicon and metal heaters on actuation sections (bottom left), MEMS patterning into wafer front side (top right), MEMS release from wafer backside (bottom right).

Examples of the MEMS design as well as realized structures are shown in Figure 6. In these designs, so-called short-loop bimorph actuators are utilized, *i.e.* the SiO_2 actuator beams are provided with a poly-Si section partially covering the beam length. The double material layer poly-Si and SiO_2 leads to post-fabrication deformation, for the major part due to thermal stresses. The length of the poly-Si section is chosen such that the post-fabrication deflection of the waveguide and actuator beams compensates the nominal waveguide height difference between the InP and TriPleX PICs (being

inherent to the PIC fabrication) and, at the same time, provides sufficient motion range for the waveguide alignment tuning after chip assembly^[9].

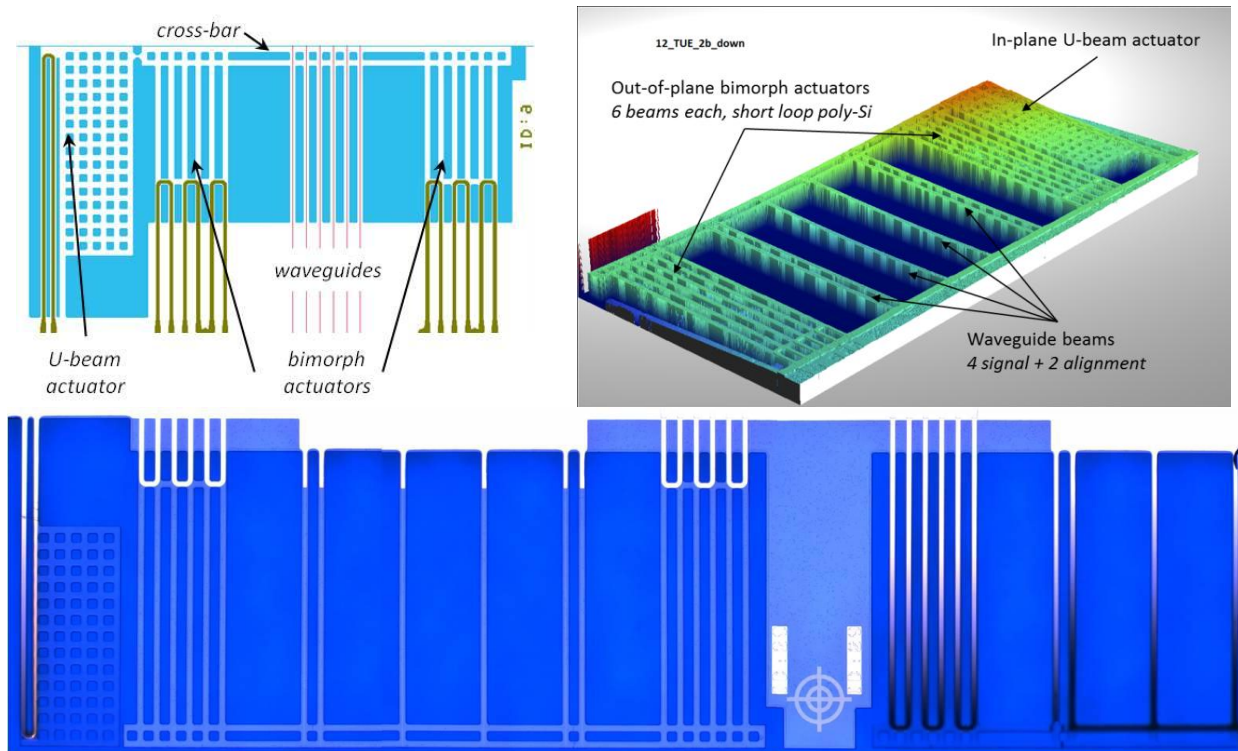


Figure 6. MEMS design on a TriPleX chip with flexible waveguides (50- μm pitch) connected through the cross-bar to the actuators (top left), white light interferometer plot of fabricated structure (top right) and stitched microscope image of MEMS structure matching the TU/e 250 μm pitch layout, two MEMS layout variants and an alignment fiducial can be seen (bottom).

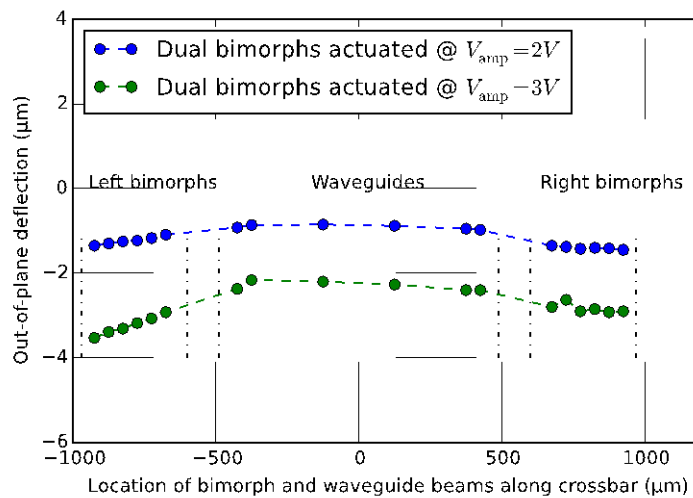


Figure 7. Out-of-plane measurement results of bimorph actuator – flexible waveguide structure driven by two different actuation voltages on a 250- μm pitch layout. Both bimorph actuators are operated.

Figure 7 shows the out-of-plane deflection of a waveguide structure when driving the left and right bimorph actuator sets simultaneously with the indicated voltages. The positions of the waveguide and actuator beams ends were measured with laser-Doppler vibrometry. The waveguide beams are not provided with actuators in this design; hence their stiffness leads to less in-plane travel compared to the actuators. Also, the stiffness of the cross-bar plays an obvious role. The end positions of the waveguides in Figure 7 vary along the cross-bar; they will end up in a certain range of positions (out-of-plane), and control of this range is essential to meet the eventual precision demanded for each of the optical I/Os at the same time. The measured min-max difference between these positions in current designs is within 150nm for the design with the widest pitch (and hence most complaint cross-bar) between the waveguides.

3.3 Assembly

A dedicated assembly machine has been designed and built (Figure 8). The nominal alignment accuracy requirement for the chips is in the range of 2-5 μm . Alignment principles utilizing a novel in-situ top-bottom viewing system have been chosen to enable the placement of the second chip with respect to the first-bonded chip targeting a $1.5 \pm 0.5 \mu\text{m}$ gap between the optical interfaces. The assembly, based on eutectic AuSn bonding, is carried out in an integrated bonding oven on the machine, with the chips held in position and under pressure during the soldering cycle. Examples of chips bonded to the carrier are shown in Figure 9. Initial shear tests have confirmed bond strengths for force equivalents up to 5 kg.

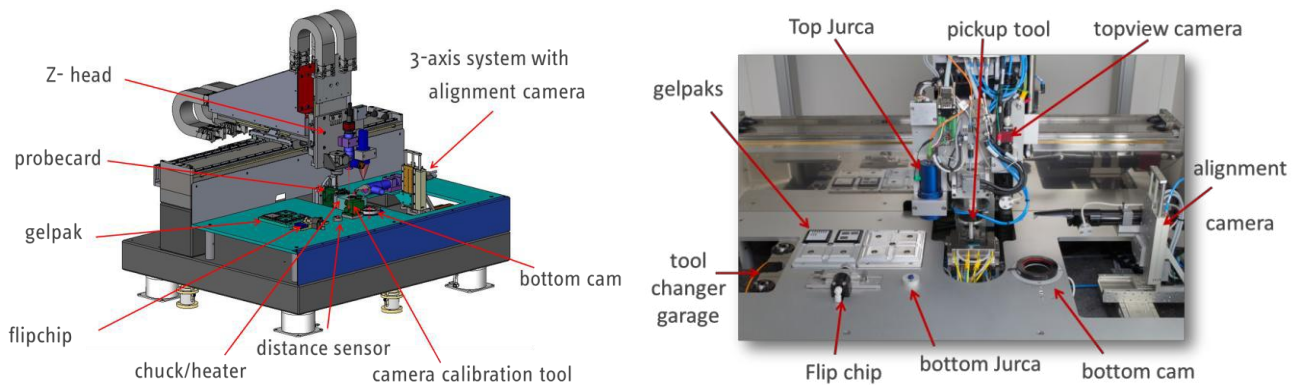


Figure 8: 3D-drawing of assembly machine (left) and photograph of the interior of the assembly machine (right).

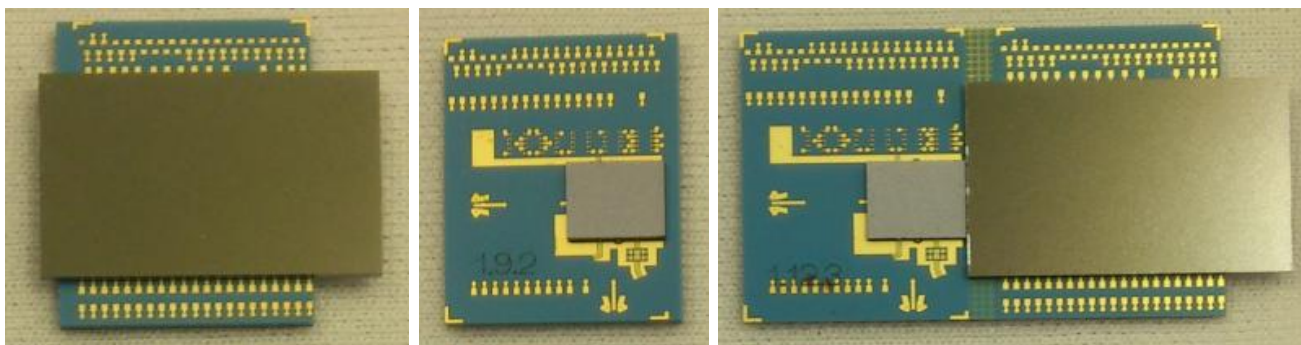


Figure 9: Photographs of first TriPleX (left) and InP (middle) test chips assembled on LTCC carriers, assembly of two chips on same carrier (right).

4. CONCLUSIONS

A novel concept for high-precision ($\pm 0.1\mu\text{m}$) optical waveguide alignment has been introduced, aiming to standardize and automate the design and assembly of new generations of hybrid photonic packages. The first series of piece parts – photonic chips, carriers and assembly tools – has been designed and realized. Dual chip flip-chip assembly on a common multi-layer ceramic carrier with RF routing, capable of GHz operation has been realized in a mass fabrication compatible assembly tool. Design and technology development of integrated MEMS-based fine alignment features has been presented. Flexible waveguide structures and bimorph actuators connected through a cross-bar were fabricated and tested. Detailed MEMS characterization, optical measurements of waveguide motion and the realization of the fixing functions are all aspects currently under active investigation in the project. So far actuator motion ranges up to several μm have been measured. Waveguide height differences at the chip output facet across the waveguide array as low as 150 nm were demonstrated. Based on these preliminary characterization results we can conclude that this MEMS-based alignment approach has a high potential for meeting the precision requirements of multi-port photonic chip assemblies.

ACKNOWLEDGEMENT

The research leading to these results has received funding from the European Community's Seventh Framework Programme FP7/2007-2013 under grant agreement n°619267, PHASTFlex.

REFERENCES

- [1] <http://www.oclaro.com/technology/photonic-integration>
- [2] Ławniczuk, K., Augustin, L.M., Grote, N., Wale, M.J., Smit, M.K. and Williams, K.A., "Open access to technology platforms for InP-based photonic integrated circuits", *Advanced Optical Technologies* 4 (2), 157–165 (2015).
- [3] Wörhoff, K., Heideman, R.G., Leinse, A. and Hoekman, M., "TriPleX: a versatile dielectric photonic platform", *Advanced Optical Technologies* 4 (2), 189–207 (2015).
- [4] www.jeppix.eu
- [5] Tekin, T., "Review of packaging of optoelectronic, photonic, and MEMS components", *IEEE J on Selected Topics in Quantum Electronics* 17(3), 704–719 (2011).
- [6] <http://www.phastflex.eu/>
- [7] Peters, T.-J. and Tichem, M., "Fabrication and characterization of suspended beam structures for SiO₂ photonic MEMS", *Journal of Micromechanics and Microengineering* 25 (10), 105003 (2015).
- [8] Watanabe, K., Leinse, A., Van Thourhout, D., Heideman, R. and Baets, R., "Silica-based Optical Interposer for Si photonics", *CLEO/Europe and EQEC 2009 Conference Digest* (Optical Society of America, 2009), paper CK_P15.
- [9] Wu, K., Peters, T.-J., Tichem, M., Postma, F., Prak, A., Wörhoff, K. and Leinse A., "Bimorph actuators in thick SiO₂ for photonic alignment", presented at SPIE Photonics West, February 16-18, 2016, San Francisco, USA.
- [10] McNulty, J., "Processing and Reliability Issues for Eutectic AuSn Solder Joints", 41th International Symposium on Microelectronics (IMAPS), Providence, Rhode Island, November 2-6, 2008, Proceedings pp.909-916.
- [11] Greitmann, G., Burkard, H. and Link, J., "AuSn Thin Film Solder Layers for Assembly of Opto-Electronic Devices", 14th European Microelectronics and Packaging Conference & Exhibition, Friedrichshafen, Germany, June 23-25, 2003, Proceedings pp. 1-5.