Process Integration for Graphene Tunnel Field Effect Transistors

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Process Integration for Graphene Tunnel Field Effect Transistors

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ABSTRACT

CMOS scaling over the years has brought great improvements in the computational speed, density and cost of microprocessors. However, scaling is approaching its limits owing to the difficulty in reducing the supply voltage with conventional MOSFETs having at best a subthreshold swing of 60mv/decade. A possible alternative is Tunnel FETs (TFETs) where carrier transport happens through band-to-band tunneling as opposed to thermal injection in MOSFETs. While silicon and III-V semiconductors have been investigated in this context, carbon-based and the large family of transition metal dichalcogenides offer more material flexibility and better electrostatic control.

Bilayer Graphene (BLG) has the interesting property that an appreciable band gap can be induced electrostatically. Additionally, its low effective mass (0.05me), direct bandgap and ultra-thin body make it highly suitable for TFETs. Theoretical studies for BLG TFETs have shown promising results, although practical implementation requires several technical hurdles to be overcome.

To address some of these, process modules for realization of BLG TFET have been developed in this dissertation.

Channel-Length Scaling: To replace conventional Si MOSFETs, graphene and other 2D materials should demonstrate superior behavior in the short-channel devices. Thus, a recipe for fabricating devices with a channel length down to 40nm was developed

and demonstrated in the lab. Also, MoS_2 devices were fabricated with this recipe and their electrical properties were compared over a range of channel-lengths.

Contact-doping on Single-Layer Graphene (SLG): BLG TFET architectures exploiting the effect of charge transfer between metal and graphene to realize abrupt P-i-N structure has been proposed in literature. An experimental study towards quantifying doping by metal on large area SLG was performed with Transfer Length method (TLM). Coupled with the scaling module, CVD graphene was used to obtain a statistical variation of various electrical parameters crucial for realization of logic devices. Also, an evaluation using a model based on Landauer-Buttiker formalism was performed to understand the electrostatic and geometric factors for designing P-N junctions. Further, suggestions regarding extending the results to BLG has been proposed.

Gate-Stack on Graphene: Gate-dielectric scaling is very important for enabling overall device scaling. Due to weak Vander Waals' interaction between graphene layers, growing a reliable oxide on graphene channel has been a challenge. In this work, a low temperature Atomic Layer Deposition (ALD) recipe for high k-dielectrics - Aluminum oxide (Al_2O_3) - over graphene has been developed and investigated through physical and electrical characterization.

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CONTENTS

ABSTRACTv
ACKNOWLEDGEMENT vii
LIST OF FIGURES xii
LIST OF TABLESxvi
1 INTRODUCTION1
1.1 Background1
1.2 Motivation2
1.2.1 TFETS with 2D materials4
1.3 Organization Of Report
2 CHANNEL LENGTH SCALING7
2.1 Introduction7
2.2 Test Structure And Process Flow
2.3 Contact Patterning
2.3.1 Lift-Off10
2.4 Case Study20
2.4.1 Fabrication of devices
2.4.2 Results

2.5	Conclusion	27
3 CON	TACT DOPING OF GRAPHENE	29
3.1	Introduction	29
3.2	Test Structure	30
3.3	Measurement	32
3.4	Results And Discussion	33
3.5	Simulation	39
3.6	PN Junction By Landaeur Approach	42
3.7	Short Channel Regime	47
3.8	Conclusion	51
4 GAT	E STACK	52
4.1	Introduction	52
4.2	Atomic Layer Deposition	53
4.	2.1 ALD Growth on Graphene	55
4.	2.2 ALD Recipe	55
4.3	Fabrication	56
4.4	Results	60
4.	4.1 Physical characterization	60
4.	4.2 Electrical Characterization	62

4.5	Conclusion	71
5 CO	ONCLUSIONS	73
5.1	Contact scaling with MoS ₂ FETs	73
5.2	Doping Graphene With Contact Metal	73
5.3	ALD High-K Dielectric For Graphene	75
REFEF	RENCES	76
APPEN	NDIX I	82
APPEN	NDIX II	87
APPEN	NDIX III	89
APPEN	NDIX IV	90

LIST OF FIGURES

Figure 2-1 TLM structure with contact width (W_C) and length (L_C)
Figure 2-2 Effect of misaligned contacts (a) Ideal Current flow (b) current flow of
misaligned contacts [4] (c) Current transfer under metal-semiconductor contact
[56]9
Figure 2-3 Layout of pin structure10
Figure 2-4 Process flow for back gated devices
Figure 2-6 SEM images for TLM with optimum dose of (225+335) showing the
dimensions18
Figure 2-5 SEM images of fine structures of TLM for different doses (fine+coarse)
(a)195+290 (b)205+305 (c)215+320 (d)225+335 (e)235+350 (f)245+365
(g)255+380 (h)265+39518
Figure 2-7 44nm, 129nm device - (a) TLM layout on MoS_2 flake (b) Optical image of
devices (c) SEM image showing measured dimensions (d) AFM data showing
flake thickness
Figure 2-8 300nm devices - (a) TLM layout on MoS_2 flake (b) Optical image of devices
Figure 2-9 45nm HfO_2 substrate: (a) (b) Transfer (semi-log scale) and output
characteristics of 300nm device (c) (d) Transfer (semi-log scale) and output
characteristics of 129nm device (e) (f) Transfer (semi-log scale) and output
characteristics of 44nm device23

Figure 2-10 45nm SiO ₂ substrate :(a) (b) Transfer (only for $V_D=0.5V$ shown) and output
characteristics of 480nm device(c) (d) Transfer (only for $V_D=0.5V$ shown) and
output characteristics of 230nm device24
Figure 2-11 Contact resistance (R _C) modulation with back-gate bias
Figure 3-1 TLM mask with layer legend
Figure 3-2 Total resistance (left) and R _{odd} (right) for the TLMs measured35
Figure 3-3 Schematic view of bottom-gated graphene device [23]
Figure 3-4 Bottom-gated device with charge densities induced by gate and metal contact
Figure 3-5 Band structure at different regions of the device for different back-gate biases
Figure 3-6 Energy band diagram of graphene for differently doped regions [24]43
Figure 3-7 (a) Simulated conductance for abrupt junction (red) (b) Conductance from
NEGF simulation [24]44
Figure 3-8 (a) Simulated conductance for different lengths of Dw: red- 0nm, brown -
10nm, orange-50nm (b) Transmission coefficient for Dw=0nm (red) and 20nm
(blue)44
Figure 3-9 Resistance Vs Vpn (a) Simulated (b) NEGF [24]45
Figure 3-10 V _{NP} shift with channel length
Figure 3-11 Band structure for Lch <2Wc and Lch>2Wc
Figure 3-12 Normalized resistance asymmetry between N branch and P branch49

Figure 3-13 $I_{\text{on}}/I_{\text{off}}$ ratio v/s Channel length (a) 500nm wide sheet (b) 200nm wide sheet

Figure 4-1 Schematic representation of two-step ALD reaction [41]54
Figure 4-2 SEM images of graphene samples before ALD
Figure 4-3 (a)Raman Spectroscopy of the graphene sample before ALD (b) $I_{\rm 2D}/I_{\rm G}$ and
(c) I_D/I_G mapping for an area of $36\mu m^2$ of the sample
Figure 4-4 E-beam mask for overlapping top-gate TLM structures
Figure 4-5 Process flow for top-gated TLM structures
Figure 4-6 Raman spectroscopy for samples of the six recipes after ALD (a) 100°C short
(b) 100°C long (c) 125°C short (d) 125°C long (e) 150°C short (f) 150°C long
Figure 4-7 SEM images of Al_2O_3 on graphene (a) $100^{\circ}C - S$, (b) $100^{\circ}C - L$, (c) $125^{\circ}C - C$
S, (d) 125° C – L, (e) 150° C – S, (f) 150° C – L63
Figure 4-8. Typical IV curves for each of the six samples (a) 100°C short (b) 100°C long
(c) 125°C short (d) 125°C long (e) 150°C short (f) 150°C long recipes64
Figure 4-9 (a) I-V curves for voltage stress test done on Sample 6 (b) I-V showing the
behavior around V_{NP} for different stress
Figure 4-10 Ion/Ioff, Vcn (Neutrality point), Peak transconductance for electrons, Peak
transconductance for holes plotted for different ALD samples
Figure 4-11Band diagram for top-gated graphene FET (V _G >0)69
Figure 4-12Equivalent circuit for top-gated (a) graphene FET (b) Si-MOSFET69

Figure 4-13(a) Graphene surface potential v/s $V_{topgate}$ (b) Voltage drop across oxide v/s

Vtopgate (c) Threshold shift v/s Vtopgate (Red-Graphene, Green-Si)......71

LIST OF TABLES

Table 1 Resist parameters for shaping and contacts patterning	14
Table 2 Exposure parameters	14
Table 3 Lift-off parameters	14
Table 4 MoS2 device details	21
Table 5 MoS ₂ device electrical parameters	27
Table 6 TLM device dimensions	31
Table 7 DFT calculation for type of doping by metal	32
Table 8 Design parameters for PN junctions	45
Table 9 Top gate TLM device dimensions	60

1 INTRODUCTION

1.1 BACKGROUND

CMOS scaling over the years has brought great improvements in the computational speed, transistor density and cost of microprocessors. But, at the same time, the active power of microprocessors has been shooting up due to high CMOS circuit density. This dramatic growth in the semiconductor industry can be attributed to the properties of Silicon. Silicon based metal-oxide-semiconductor field effect transistors (MOSFETs) were engineered over decades to meet the performance requirements, along with cost effectiveness. Such transistors operate by injection of electrons (or holes) over a potential barrier which is electrostatically controlled by the "gate" terminal. In an ideal system, the voltage applied to the gate completely results in modulation of this barrier. This transport by diffusion of charge carriers from source to drain through channel depends on the electrons which are filled according to Fermi-Dirac distribution in the "source" terminal. While the transistor switches from OFF state (weak inversion) to ON state (strong inversion), electrons with energies in the Boltzmann tail of Fermi distribution are involved in current conduction. This results in current dependence of the form $I \sim \exp[qV/K_BT]$ in the weak inversion, where V is the gate voltage. Therefore, the current cannot be changed steeper than $S \sim (K_B T / q) \ln 10 \sim 60 \,\text{mV}/\text{dec}$ at room temperature. In other words, to achieve ON and OFF state of the transistor with $I_{ON} / I_{OFF} = 10^4$, a minimum supply voltage of 4*60mV = 0.24V is required [1]. This prevents the supply voltage scaling which accompanies device scaling to reduce power consumption and also reliability of the devices. Thus, device concepts to operate beyond the 60mV/dec limit are being explored extensively. A possible alternative is Tunnel FETs (TFETs) where carrier transport happens through band-to-band tunneling. Although TFETs promise sub-threshold slopes (S.S.) of less than 60 mV/dec, maximum ON currents (I_{ON}) in TFETs are typically well below that of the MOSFET. Emerging materials with low charge carrier effective mass and small bandgap opening promise increased I_{ON}. In this context, the new family of 2D crystals such as graphene and transition metal dichalcogenides (TMDs) offer an interesting case to investigate. Apart from their material properties, their planar geometry offers several advantages over the 3D bulk.

1.2 MOTIVATION

The conducting channel of Si FETs were scaled down over the years for improved performance. This led to weakening of the gate control over the charge carriers on the channel. Due to several short channel effects which arise because of weak gate control, the device cannot be switched ON and OFF efficiently. This necessitated new device geometry such as FINFETs [2] which had gate-all-around the channel for better electrostatic control of gate. Due to complexities of non-planar process methods involved in FINFETs, ultra-thin-body (UTB) MOSFETs are also studied for better electrostatic control with conventional CMOS planar process. UTB MOSFETs provide additional benefit of threshold voltage control using the back-gate of the transistor. Interestingly, 2D materials are intrinsically thin, about few atoms thick making them ideal for such UTB short channel devices with good control by gate.

The building block for 2D crystals is its planar 2-D lattice. For graphene, the basis consists of carbon atoms attached to a hexagonal planar lattice. TMDs share the same lattice, except that now the basis consists of one M and two X atoms, where M is the metal and X corresponds to the chalcogenide atoms. Theoretically, these materials are expected to be defect free due to their hexagonal planar lattice with sp2 bonds.

The smooth surface of 2D materials provides yet another advantage. Mobility in thinned down 3D semiconductors drop drastically due to carrier scattering from surface roughness [1]. Pure 2D crystals do not suffer from such effects and provide superior carrier transport. Due to intrinsic defect free property of 2D materials, several heterojunction vertical TFETs structures are also being researched.

Further, carrier mobility is affected by interaction with charged impurities. While this interaction depends solely on the bulk properties in 3D semiconductors, most of the electric field lines in 2D crystal lie outside and hence depend on the surrounding dielectric. This provides an additional degree of freedom to tune the carrier interaction and hence the mobility [1].

These properties of 2D materials make them highly suitable as Si replacement for future nodes.

1.2.1 TFETS with 2D materials

Tunneling FETs (TFETs) promise significant reduction in power consumption as mentioned in section 1.1. Further, to mitigate low ON currents in TFETs, a choice of material is crucial due to the dependence of tunneling probability on material parameters given by: $I \sim exp(-B * \sqrt{m}\sqrt{EG} \lambda)$. Here, m and E_G represents carrier effective mass and bandgap opening of the material respectively[3]. Interestingly, tunability of these material parameters is observed in emerging 2D materials with applied electric field and number of layers [1]. A detailed evaluation of 2D materials for tunneling FET has been presented in [1]. Moreover, different tunneling phenomenon such as in-plane tunneling and interlayer tunneling is evaluated for lateral and vertical devices [1].

Out of plane (or inter-plane) tunneling devices are under scrutiny now and in-plane tunneling ON currents are estimated to be low with large bandgap 2D materials. However, it is observed that the bandgap of 2D materials can be tuned with vertical electric field and number of stacked layers [put reference] which shows promise for low power 2D materials based TFETs. Additionally, the symmetry in band structure of these materials [1] allows for symmetric performance of nTFETs and pTFETS, essential for complementary (CMOS) logic circuits.

Graphene seems to show the highest ON-state inter-band tunneling [1] amongst other materials. This is due to the absence of bandgap in single layer graphene. However, this degrades the OFF state required for digital logic circuits. Bilayer graphene (BLG) has been proposed as an alternative for this shortcoming [4]. Theoretical calculations and experimental measurements [2][3] show that a direct band-gap of few hundred meV can be created by applying vertical electric field or chemical doping. Recently [4], a bandgap of 170 meV has been achieved with double gated architecture. A relatively small bandgap opening and small effective mass (~ $0.03 m_0$) in BLG makes BLG interesting to evaluate for TFETs.

With finite bandgap opening, several FETs based on bilayer graphene have been demonstrated in literature to boost I_{ON}/I_{OFF} in graphene FETs [5]. However, these experiments have been shown for larger devices. There are several technological hurdles to enable scaling which is essential to integrate on very large scale integrated circuits. These challenges need to be tackled for any device architecture:

- 1. Elimination of Short channel effects
- 2. Fabrication of low resistivity metal-semiconductor to be used as device contacts.
- 3. High quality top gate dielectric on 2D crystal

This work focuses on solving the specific processing hurdles mentioned above which has been described in detail in each chapter.

1.3 ORGANIZATION OF REPORT

In the chapter 2, the issue of short channel effects (SCE) for these materials have been investigated. In this dissertation, transmission line model (TLM) structures have been used as the test vehicle for various studies. TLM design methodology and a process flow for fabricating the same with 2D materials have been defined. Further, the lithography process has been optimized to pattern sub-50nm devices in the lab. Also, MoS₂ devices have been fabricated with this recipe and their immunity to SCE have been investigated. In chapter 3, the phenomenon of surface charge transfer between contact metal and large area single layer graphene has been probed with electrical measurements. A model, based on Landaeur- Buttiker formalism, has been developed to further understand the operating principle behind this charge transfer and device design parameters has been extracted to design PN junctions with graphene. Short channel devices have been realized with the process developed in chapter 1 and a comprehensive study on graphene device performance in the short channel regime has been performed.

In chapter 4, the process flow developed of chapter 1 has been augmented to realize top-gated devices. A scalable ALD oxide recipe has been developed to grow high k dielectrics on graphene without much damage to the material. This has been achieved by optimizing ALD temperature and precursor pulse times. The recipe has finally been evaluated with physical and electrical characterization.

Finally, we conclude with certain remarks in the light of the experiments presented in the preceding chapters and scope for future work.

2 CHANNEL LENGTH SCALING

2.1 INTRODUCTION

Following Moore's Law, microelectronics industry has seen a tremendous growth over the past five decades by the continuous scaling of transistors. This downscaling was achieved with scaling rules such as Dennard's scaling rule of constant electric field. Though it proposed a proportional scaling of all device dimensions, [6] shows that industry did not strictly adhere to it. Nevertheless, mere scaling improved performance of the devices without compromising on reliability. Beyond certain technology node, innovations such as strain engineering and high-k dielectric supplemented this downscaling. However, dimension scaling faces problems of parasitic capacitances and resistances which don't scale [7], [8].

Along with dimension scaling, threshold voltage (V_t) scaling is necessary to bring down the overdrive voltage ($V_{supply} - V_t$) and hence the power consumption. However, this increases the off-current and standby power, thus limiting further reduction in V_t . Therefore, silicon based transistors cannot support further downscaling and this has created a need to explore alternative channel materials with improved transport properties such as MoS₂ and novel logic devices such as TFETs. To investigate the performance of these materials in the short channel regime, a reliable way to fabricate these devices needs to be developed. Following this, a lab recipe has been developed to fabricate MoS_2 based field effect transistors with a channel length down to 40nm. The electrical performance of these devices is studied over different channel lengths.

2.2 TEST STRUCTURE AND PROCESS FLOW

In this work, transmission line model (TLM) structures were extensively used to study various electrical parameters. TLM structures have simple device design and allow for more throughput and straightforward characterization. A typical TLM consists of rectangular region of homogenous semiconducting channel (in our case graphene/MoS₂). A set of contacts with varying channel lengths (L_{ch}) is formed over the strip (Figure 2-1). In 2D materials, source and drain regions are simply defined by metals deposited on the semiconductor as its ultra-thin body (single atom thick to few nm) prohibits doping via ion-implantation or diffusion. Hence, the set of TLM contacts (Figure 2-1) represents the source and drain terminals of different-sized FETs. The channel or device width (W_{ch}) is preferably shaped to be equal to the contact width of TLM (W_c). Misalignment of contacts can lead to current flow as in (Figure 2-2 (b)), introducing error to the resistance measurement. Length of each metal contact (L_c) is another parameter of interest. Usually, carriers travel in the semiconductor beneath the contact before being conducted to the metal. The carrier conduction (current density) is high at the edge of the contact and drops off as one moves away from that edge. The average distance over which this transfer happens is defined as the effective transfer length (L_T) (Figure 2-2). For an accurate TLM design, L_c needs to be at least twice the L_T [9] to avoid effects of current crowding at the contacts which could cause thermal hotspots thereby increasing resistance and affect the actual performance of the device. From previous experiments on MoS_2 using TLM method, L_T was estimated to be around 200-300nm (Section 3.4). Hence a value of $L_c = 500$ nm ($> 1.5L_T$) was chosen for the layout of the TLM structure.



Figure 2-1 TLM structure with contact width (W_C) and length (L_C)



Figure 2-2 Effect of misaligned contacts (a) Ideal Current flow (b) current flow of misaligned contacts [9] (c) Current transfer under metal-semiconductor contact [62]

For a reasonable study of 2D materials in the short channel regime, it is preferred to pattern 500nm wide metal lines (source and drain) with sub-100nm pitch grating. Besides TLM structures, also, pin-like structure (Figure 2-3) were designed and fabricated. The fabrication flow is similar to the TLM structures and the pin structures are designed for even shorter channel lengths (than TLMs). This is made plausible due to well-isolation of these structures from one another (separated by ~100um) and suffer less from secondary electron-beam (e-beam) effects such as proximity effect.



Figure 2-3 Layout of pin structure

2.3 CONTACT PATTERNING

2.3.1 Lift-Off

Despite the various advantages that ultra-thin structure of 2D materials offer to lateral FET design, conventional doping techniques such as diffusion and ion-implantation to create source and drain terminals are difficult. Therefore, a good Ohmic contact is ensured only by deposition of metals with appropriate work function.

Lift-off is then a simple and easy method for patterning such metal film deposits. It doesn't involve any subtractive step such as etching which could damage the thin semiconductor channel.

The patterning consists of following process steps for back-gated devices (Figure 2-4):

- 2D material is available in the form of flake or CVD layer supported on SiO₂ or HfO₂ substrate. A pre-bake is performed before any processing to remove adsorbed moisture.
- 2- An adhesive such as Ti-prime further renders the surface hydrophobic. Negative resist Ma-n2400 is spin-coated on a rotating chuck. E-beam exposure defines the active region. Following development of the resist (areas unexposed are removed), O₂ plasma is used to etch rest of the resist and 2D material (flake/CVD sheet).
- 3- PMMA (Poly methyl methacrylate), a long chain polymer, in chlorobenzene (solvent) is used as positive resist. The resist thickness is optimized for good lift-off and usually this requires that the resist is three times the thickness of metal film deposited. A resist thickness of 180nm is therefore spin-coated for a maximum of 60nm thick metal film. Though a bilayer resist scheme would be most favorable for lift-off with its overhanging side-walls profile, we opted to use single layer as it allows [10],
 - a- To use thinner resist and thus achieve higher resolution.
 - b- Easy optimization of exposure dose and development time.



Figure 2-4 Process flow for back gated devices

A post-bake is performed little over the transition temperature of the resist to enable a homogenous layer.

- 4- Areas exposed by e-beam are removed after development (positive resist). A 1:1 mixture of MIBK (Methyl IsoButyl Ketone) and IPA (IsoPropyl Alcohol) is used as the developer. This is the optimum ratio as suggested by Microchem [11] (PMMA vendor) for both good resolution and sensitivity to the development time. The forward scattering of electrons in e-beam exposure creates the undercut profile in the resist.
- 5- Metal film is deposited by e-beam evaporation all over the substrate, covering the resist and regions where the resist have been cleared. Lift-off is then done by immersing in hot/cold acetone for sufficient time. This time usually depends on the quality of film being deposited with high quality film requiring more time. Later, gentle agitation in a sonic-bath removes the resist (and hence the metal film) leaving the film on the substrate/active region. For some noble metals (such as Au,Pd) a thin adhesion layer of Ti or Cr is first deposited.

In order to reliably pattern devices with sub-100nm pitch, several parameters in the above process flow can be optimized. In this work, a process module was developed upon an already existing in-house recipe by tuning the exposure dose to realize up to 40nm devices. Exposure dose and development time are two key factors that allows for easy optimization in a single resist scheme.

	Shaping	Contacts Patterning
Resist	Ma-N2400	РММА
Туре	Negative	Positive
Thickness	50nm	180nm
Developer	MaD 525 (Microchem	1:1 MIBK:IPA
	[11])	
Development Temperature	21°C	21°C
Development Time	50s	Till complete development of "18 th " reference marker

Table 1 Resist parameters for shaping and contacts patterning

Table 2 Exposure parameters

Lithography	Electron beam
Focus	Fixed
Exposure Energy	Set at 50KeV
Exposure Dose	Optimized with PMMA development time
	for "18 th " contrast marker

Table 3 Lift-off parameters

Metal deposition	E-beam evaporation
Film thickness	50nm contact metal or 2nm Adhesive
	layer (Ti/Cr) + 50nm contact metal
Lift-off solvent	Acetone
Lift-off temperature	Cold/ hot (50°C)

Development time: Usually 24 wide isolated lines referred to as contrast markers are written with every batch of devices. They are exposed in increasing order of certain standard dose. The development time was defined arbitrarily as the time it takes to completely develop the "18th" marker in the array. Then structures written with same exposure dose as the 18th marker would be fully developed.

Exposure dose: The e-beam tool used in this work is a Vistec VB6. Before optimizing for dose, exposure energy needs to be set. Exposure energy refers to the voltage applied across the source of electron gun and the target substrate. This determines the forward scattering of electrons in a resist [12]. The electron beam broadens less for a higher exposure energy and hence improves the applicable dose window for a required pitch. Though it renders the resist less sensitive to patterning different pitches, a broader dose window makes the process highly robust and achieve better controllability of the metal line width. To facilitate this, the tool allows for a maximum acceleration voltage of 100KeV. However, for reliable operation, it was operated at 50KeV. A downside to high exposure voltage could be backscattering of electrons (proximity effect) [13] exposing resist of nearby feature, causing pattern distortion. This effect is pronounced in large structures where the backscattered electron can re-emerge exposing the features more than once. Therefore, fine features receive multiples of the assigned dose and the large features less than the assigned dose. This pattern dependent dose correction factor was calculated using exposure tool related software.

Exposure dose is defined as the charge delivered per unit area (Coulomb/cm²). Though the pattern would be well resolved for a given energy, dose determines the aspect ratio (height/width) of the features. The solubility of the resist is enhanced with increase in dose (in case of positive resist) and hence plays a crucial role in determining the quality of the structure [14]. With an acceleration energy of 50 kV, and development time fixed as described above, a dose test was carried out with a matrix (3*5) of TLM structures each exposed to slightly different doses. The doses span from values less than the dose value for development of "18th" contrast marker to several multiples of it. The E-beam layers were further split into fine and coarse structures. Fine structures comprise the densely packed features (for example, the array of contacts on the graphene strip) while coarse structures (like bond pads) are sufficiently spaced out. The two layers then allow for further split in the doses and hence different currents to be used - the lower dose is written with low current (1nA) and higher dose with higher current (48nA). The strategy allows to speed up writing process by using step sizes of 10nm and 40nm for 1nA and 48nA writing, respectively. This reduces the writing time by 16 times.

The dose value for the well-defined structure was chosen after SEM inspection of the metal lines deposited after lift-off. Usually a lithographic process is optimized by measuring resist line widths after development [10]. But, as we are interested in the short channel devices, we use the final structure with metal contacts as the deciding factor for dose.















Figure 2-5 SEM images of fine structures of TLM for different doses (fine+coarse) (a)195+290 (b)205+305 (c)215+320 (d)225+335 (e)235+350 (f)245+365 (g)255+380 (h)265+395



Figure 2-6 SEM images for TLM with optimum dose of (225+335) showing the dimensions

In the SEM images, well developed gratings are identified by strong contrast with its adjacent region as in Figure 2-5. It should be noted that using PMMA, the metal lines are written in the exposure process and the channel is defined by the lift-off process. It is observed that most of the TLMs have their second and subsequent pitches opened. This implies that the dose window used in above test is favorable for 60nm pitch and above (Figure 2-6). The broad dose range is also the result of using high EBL voltage making the recipe quite robust to process variations especially resist (aging). However, we certainly lose the sensitivity by doing so. Closer inspection of the structures reveal the pitch deviation from the designed value. At the lower doses (Figure 2-5 (a), (b)), the 50nm, 60nm and 75nm pitch show partial clearance. As the dose increases, the 50nm pitch remains closed but the 60nm pitch and above show complete clearance. Bad lift-off is likely the cause of partial clearance in the 60nm, 75nm pitches at lower doses. At higher doses, morphological damage similar to 50nm pitch (of lower dose) is noticed for the 60nm channel. This is because of overexposure of the metal lines for the smallest feature. It results in broadened metal line widths leading to collapse of interline resist (in other words, complete channel closure). This observation holds true for both 500nm and 1µm line widths. The other pitches are well defined and don't reveal any excessive clearance with higher doses. The dose which yielded best quality grating (close to the designed value) was used for further processing of devices. Also, as expected, the pin-structures were open with even smaller channel lengths for similar doses used for TLM.

2.4 CASE STUDY

The recipe developed above enables testing of 2D materials such as graphene, MoS₂ and WSe₂. Although graphene has high carrier mobility, absence of bandgap makes it unsuitable for logic operations. MoS₂, unlike its isomorph graphene, possess a large bandgap (~1.2eV for monolayer MoS₂[15]) and is considered to be a promising candidate [16].

As part of the case study, MoS₂ based FETs have been fabricated with the recipe developed above and its electrical performance is compared for different channel lengths.

2.4.1 Fabrication of devices

Two set of devices, one on 45nm HfO₂ substrate and another on 45nm SiO₂ substrate were fabricated. MoS₂ flakes on HfO₂ (high-K) substrate provided good optical contrast and were expected to have better electrostatic control than SiO₂ substrate. The flakes were mechanically exfoliated from bulk crystal and transferred to the respective substrates. Monolayer MoS₂ with its large bandgap reduces electron mobility [12] and therefore flakes of 15nm thickness (~23 layers) were identified for our study. TLM structures were fabricated on the flakes (Figure 2-7) using the recipe developed in section 2.2. The shaping step was skipped by using more or less rectangular flakes for fabrication. For the metal, e-beam evaporated Titanium (2nm adhesion) + Gold (40nm) (as demonstrated in [17]) was used for the flake on HfO₂ substrate. This metal split showed large Schottky barrier (Figure 2-9) on electrical characterization and later only gold (40nm) was deposited for the SiO₂ sample. This reduced the Schottky barrier between


MoS₂ and the contacts as seen in section 2.4.2. For both the metal splits, the contact width

Figure 2-7 44nm, 129nm device - (a) TLM layout on MoS_2 flake (b) Optical image of devices (c) SEM image showing measured dimensions (d) AFM data showing flake thickness

The heavily doped Si was used as the global back gate for both the samples. No passivation or annealing was done before the measurement. All the measurements were performed at room temperature.

Batch No	Channel Length	Substrate	Source/Drain Contacts
Ι	300nm, 129nm, 44nm	45nm HfO ₂	Ti/Au
II	480nm, 230nm	45nm SiO ₂	Au

Table 4 MoS₂ device details



Figure 2-8 300nm devices - (a) TLM layout on MoS₂ flake (b) Optical image of devices

2.4.2 Results

Transfer characteristics (I_D-V_G) and output characteristics (I_D-V_D) of the various devices were obtained.

The transfer characteristics of the long channel and short channel devices are examined. The batch I devices show lower order of drain current compared to batch II. This is due to the poor Source/Drain contacts of batch I with Ti/Au. Owing to its ultrathin body, the I_{on}/I_{off} ratio for batch I devices remain constant with different channel lengths at about 10⁵ showing good immunity to short channel effects. Batch II devices with the improved contacts show even higher ON/OFF ratio of 10⁸. Unlike graphene (investigated later in the thesis), the large bandgap of these devices allow for a good "OFF" state. The OFF state current is in few pA contributed mainly by back-gate leakage. Interestingly, one of the 300nm devices fabricated exhibited ambipolar conduction. Since batch I devices didn't undergo any special surface treatment (like PMMA support in [18]), the observed ambipolarity was suspected to be result of unsymmetrical contacts (for source and drain) or variation in flake thickness locally (thin flakes exhibit ambipolar conduction [19]).



Figure 2-9 **45nm HfO₂ substrate**: (a) (b) Transfer (semi-log scale) and output characteristics of 300nm device (c) (d) Transfer (semi-log scale) and output characteristics of 129nm device (e) (f) Transfer (semi-log scale) and output characteristics of 44nm device



Figure 2-10 **45nm SiO₂ substrate** :(a) (b) Transfer (only for $V_D=0.5V$ shown) and output characteristics of 480nm device(c) (d) Transfer (only for $V_D=0.5V$ shown) and output characteristics of 230nm device

It is interesting to note from Figure 2-9 (a) that MoS_2 shows similar transport properties for both holes and electrons. The I_{off} (Figure 2-9 (a)) was severely degraded unlike its unipolar counterparts. This again could be the result of unsymmetrical Schottky contacts explained later. The transfer curve of 44nm device show significant shift with increased drain bias similar to drain induced barrier lowering (DIBL) in silicon.

Following the transfer curves, output characteristics are examined. Batch I devices clearly show non-linearity. The total resistance (R_{on}) was extracted from the output characteristics at low field (V_D = 50mV) for the three channel lengths. The resistances thus obtained were very high (Figure 2-9 (b) (d) (f)) and decreased with increase in gate bias

(R_{on} in Figure 2-9 for highest gate bias). This R_C dependence on gate bias could be attributed to,

- 1. Schottky barrier between the metal and MoS₂ interface.
- Doping that is accompanied with gate bias, as these are accumulation based devices.

The TLMs directly allow for separating the contact resistance from the channel resistance, as detailed in Section 3.4. However, the flake used in 300nm being different from the 129nm and 44nm devices, it is difficult to make conclusive calculation. Much of the resistance was suspected to be from Schottky contacts formed between the metal and MoS_2 . The upward bend in I_D-V_D of fairly long channel 300nm (Figure 2-9 (b)), 129nm (Figure 2-9 (d)) support the claim made above. The high gate bias would then, change the tunneling efficiency across metal-semiconductor Schottky barrier by band bending, and gives rise to non-linear dependency of current with drain bias. A temperature dependent study could further be used to evaluate the Schottky barrier. Similar upward bending is seen at high drain voltage of 44nm device, but this is more likely due to degraded electrostatic control from the gate (DIBL is observed in its transfer curves). Batch II devices show ohmic contacts (linear ID-VD)) and orders of current higher than batch I. At high lateral fields, they tend to saturate. Both the batches showed symmetrical behavior of ID for positive and negative drain biases. However, it was noticed that the ambipolar device exhibited an asymmetry with the drain currents being roughly half for negative VD. It is proposed that this asymmetry could be due to Schottky barriers formed with the conduction and valence band of MoS2 at the source and drain terminals respectively. Then the barriers are modulated for positive and negative biases of VG exhibiting ambipolarity.

 R_c for different VG was extracted using TLM method (Section 3.4) for batch II devices to compare it against the channel resistance modulation Figure 2-11.



Figure 2-11 Contact resistance (R_C) modulation with back-gate bias

Other electrical parameters of the devices have been listed in Table 5. Transconductance (G_m) and carrier mobilities were calculated. Transconductance was calculated as $\frac{\delta I_D}{\delta V_{topgate}}$ and mobility as $\frac{\delta I_D}{\delta V_{topgate}} \frac{L}{W.CV_{DS}}$ where L, W are the length and

width of the channel and C is the graphene to top-gate capacitance. Mobility is calculated at the steepest point of the I_{drain}-V_{topgate} ($\frac{\delta I_D}{\delta V_{topgate}}$ is maximum) curve. However, the

mobility values are extrinsic meaning includes the contact resistance. Naturally, the values are better for SiO_2 devices with less contact resistance. Threshold voltages were obtained by extrapolating the linear region of G_m to intercept with gate bias VG.

Device	Ion (A/um)	Ion/Ioff (at VD=0.5V)	$\mu_n (cm^2/V.S)$	Vth (V)
300nm (HfO ₂)	1.1*10 ⁻⁷	533	3	1.36
129nm (HfO ₂)	625*10 ⁻⁹	10 ⁶	4	-0.51
44nm (HfO ₂)	73*10 ⁻⁹	10 ⁵	0.39	-4.06
480nm (SiO ₂)	1.43*10 ⁻⁵	3*10 ⁸	17.87	15.79
230nm (SiO ₂)	3*10 ⁻⁵	4*10 ⁷	14	12.36

Table 5 MoS₂ device electrical parameters

2.5 CONCLUSION

Process vehicle to realize 40nm pitch devices was developed. This was put to use by studying MoS₂ FETs, a prospective candidate for alternative Si channel. Performance parameters were captured over different channel lengths. Particularly,

- 1. An extrinsic mobility of $17 \text{cm}^2/\text{V.S}$ for SiO₂ supported device is a good comparison to the state of the art devices reported in literature [17].
- 2. The HfO₂ substrate devices performed poor compared to SiO₂ devices. Though, Schottky barrier was identified as the main reason for the degraded performance of these devices, the substrate could also contribute to the device performance. These 2D materials are known to be affected by the supporting substrate [18]. Further experiments on HfO₂ substrate with good ohmic contacts could help understand the substrate effects.
- 3. Nevertheless, the mobilities for batch I devices were still comparable and in certain cases better than devices reported in [20] without any passivation or annealing.

- 4. Short channel effects particularly loss of gate control and DIBL was observed in 40nm device similar to [17]. This is much better compared to III-V material where SCE is observed at 150nm [21]. Thinning down the dielectric or with a top gate device, we are convinced that better performance could be achieved.
- 5. Contact resistance plays quite a crucial role with these devices. Schottky barrier was greatly reduced when the metal stack was changed from Ti/Au to Au only. Further metal splits need to be tested to achieve even lower Schottky barrier contacts. Ultimately, this will play a key role in scaling the source and drain regions with shorter transfer lengths for the contacts.

3 CONTACT DOPING OF GRAPHENE

3.1 INTRODUCTION

Graphene and the family of transition metal dichalcogenides are considered promising candidates for replacing Si transistors. Material properties such as low effective mass (high mobility), direct band-gap for monolayers and ultra-thin body (good electrostatic control) make them immune to short channel effects (SCE) and hence suitable for technology nodes beyond 10nm. One of the technological hurdle to realize these devices is fabrication of device contacts [17].

Contacts to these materials are established through metal films deposited on regions designated as source and drain. Their ultra-thin body prevents ion implantation and hence resistance at metal-2D material interface plays a crucial role in determining the performance of the device. Considerable work function difference between the metal/alloy and the semiconductor energy bands (like Ti and MoS₂ in section 2.4.2) resulted in Schottky barriers which dominated the overall behavior of the device.

Contacts on single-layer graphene (SLG) are quite unique. The system resembles a metal-metal interface because of the absence of bandgap. The work function difference between metal and graphene results in surface charge transfer (SCT), where electron is transferred from system with lower function to the higher one at the interface. This SCT results in doping effect of graphene under the contacts. Moreover, the low density of states (DOS) with non-linear screening of electric field [22] amplifies the SCT, determining the contact resistance and transport especially for short channel devices. This chapter aims to study doping effect of metals on SLG and based on it, understand PN junctions formed in a MOSFET-like device. First section deals with definition of the test structures used for the study followed by electrical measurements and analysis. The next section describes a model, based on Landaeur- Buttiker formalism, developed to understand the operating principles behind these devices. This model was also used to extract parameters to design PN junction with graphene. Lastly, a brief study of the performance of graphene devices under the short channel regime has been presented.

3.2 TEST STRUCTURE

Transmission line models (TLM) are being used for graphene contact study. The e-beam mask of Section 2.2 was used for patterning the contacts.

The material used in the experiments is CVD graphene purchased from a commercial vendor. They are grown and transferred on to a heavily P doped Si substrate with 90nm thermally grown SiO₂. The doped Si acts as gate which modulates the channel. The back-gate, being global, additionally modulates graphene under the contacts.

The devices were fabricated using the process flow developed in Section 2.3.For the contacts, 2nm Titanium (Ti) and 40nm Palladium (Pd) were used. Ti provides adhesion and Pd is the metal of contact.

Details of the design dimensions are provided in Table 6 (refer Figure 2-1 for device design parameters).



Figure 3-1 TLM mask with layer legend

Table 6 T	LM dev	vice dir	nensions
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	TLM
Lch	100 nm – 10um
Lc	500nm
W _{ch}	500nm,200nm

For the source and drain contacts, it is natural to expect P and N doping depending on the work function difference between free-standing graphene and the metal. However, DFT study [23] shows two cases of metal-graphene interaction. Graphene can be chemisorbed on metals such as Co,Ni,Ti. It perturbs graphene band-structure leading to loss of the conical dirac point. This makes it difficult to deduce the type of doping. For the case of physisorbed graphene, there is no perturbation of band-structure. The Dirac points are intact and SCT causes Fermi-level shifts in graphene. But for such systems, type of doping is dependent on the potential profile at the metal-graphene interface. This could vary significantly with the equilibrium position of dipole at the interface. Detailed calculations [23] predicts the following doping for the different metals,

 Table 7 DFT calculation for type of doping by metal

Metal	Ti	Pd	Al	Cu	Au
Doping	n	р	n	n	р

For the metal stack of Ti + Pd , the work function is predominantly that of Pd as the thickness of Ti << thickness of Pd [22]. Therefore, from Table 7 the metal stack (Ti +Pd) is expected to p dope the graphene under the contacts.

3.3 MEASUREMENT

To investigate the devices, two probe measurements were carried out with different set of TLM contacts. TLM contacts are "invasive probes" and therefore the measurements include metal contact induced effects (e.g. SCT) and intrinsic graphene sheet properties [24]. Room temperature measurement was followed by low temperature measurement at 77K (liquid nitrogen) for obtaining sharper I-Vs. This helps in observing other contact effects such as double peaks in the I-V characteristics and allows for precisely identifying the crossing of Dirac point in the channel (neutrality point V_{NP}). The double peaks could indicate crossing of Dirac points in the graphene under the contacts and graphene in the channel (). Hysteresis due to ambient doping (polar resists, H₂O, O₂) and charge trapping in SiO₂ [25] are also reduced with the low temperature measurements. The bottom gate voltage $V_{bottomgate}$ was swept from -10V to 30V (forward) and back from 30V to -10V (reverse). The gate voltage was limited to this range in order to avoid dielectric breakdown and increased gate leakage currents. Further, V_{NP} was consistently around 7-15V for the samples and the above sweep range comfortably provides the behavior of the device for both the hole and electron conduction.

3.4 RESULTS AND DISCUSSION

Total resistance for long channel devices is the sum of channel and contact resistances. The channel resistance is determined by graphene sheet properties. The contact resistance results from the interaction of the metal-2D material system as discussed in section 3.2. Also, the entire graphene sheet undergoes charge modulation with back-gate voltage resulting in variation of the above quantities. Therefore, total and contact resistances as function of back-gate voltages become quantities of interest for the study.

Total resistance (R_{total}) was extracted from the I_{drain}-V_{bottomgate} data. It is plotted as a function of back-gate for three TLM structures (Figure 3-2). It reaches a maximum at V_{NP} and stays relatively constant for large gate-voltages. Due to graphene's ambipolarity, the total resistance plot exhibits two types of conduction: P-branch (V_{bottomgate} < V_{NP}) where the conduction is dominated by holes and N-branch (V_{bottomgate} > V_{NP}) where the conduction is determined by electrons.

Contact resistance (R_c) was evaluated using TLM method [9] for different backgate voltages. In the limit of diffusive transport (valid in our case, as the channel lengths are much larger than the mean free path of carriers), the total resistance can be written as,

$$R_{total} = \frac{R_{sheet}}{W_{ch}} L_{ch} + 2R_c \tag{3.1}$$

As the channel length approaches zero, R_{total} yields the contact resistances at different back-gate biases. R_c values of $1K\Omega.\mu m$ and $2K\Omega.\mu m$ extracted at V_{NP} is in good agreement to the values reported in literature [26].

A closer inspection of R_{total} reveals an asymmetry - the P-branch resistance is lower than the N-branch resistance. This is even more prominent in case of short channel devices with the P-side resistance decreasing faster than the N-side. Assuming similar metalgraphene interface for the different channel lengths of a TLM (not a bad assumption for a sample that is not too large), this asymmetry could be understood by formation of PN junctions between the channel and the graphene under contact [8].



Figure 3-2 Total resistance (left) and R_{odd} (right) for the TLMs measured

It becomes clearer with the following picture (Figure 3-3): The graphene strip can be segmented into three regions, (I) graphene underneath the contact metal being doped P or N by SCT, (II) transition or screening region controlled by both the metal contact and back-gate, and (III) region far from contact whose carrier density is independently determined by the back-gate. Then, for biases V_{bottomgate} >> V_{NP} and V_{bottomgate} << V_{NP}, region-3 is electrostatically doped by the gate to N-type and P-type, respectively. The observed asymmetry of Figure 3-2 (a) (c) (e) could be explained if P- doping by the contact is assumed for region-1 and region-2 as it results in the formation of P-N junction (for V_{bottomgate} >> V_{NP}) and P-P junction (for V_{bottomgate} << V_{NP}) with the channel. The presence of PN junction then contributes to the enhanced resistance [27] on one branch (here N branch). Thus resistance asymmetry acts as an indirect evidence for contact-doping of graphene. Further understanding of this phenomenon and rigorous calculation for the resistances with different energy bands is discussed in section 3.5.



Figure 3-3 Schematic view of bottom-gated graphene device [28]



Figure 3-4 Bottom-gated device with charge densities induced by gate and metal contact

The effect of contact doping is usually studied by extracting the odd part of the resistance[28]. Apart from various quantities that could be derived, R_{odd} immediately helps to determine the type of doping by contact. A brief derivation of this extraction is provided below.

Consider one unit of a TLM as shown in Figure 3-4. The contact doping is indicated by n_1 (contact induced charge) and the gate-induced doping by n_2 . They are given by,

$$n_2(Induced by back - gate) = \frac{C_b(V_{bottomgate} - V_{NP})}{e}$$
(3.2)

Where C_b – the back-gate capacitance.

The total resistance for fixed contact doping n_1 is given as,

$$R_{n1}(n_2) = R_{n1}^{even}(n_2) + R_{n1}^{odd}(n_2)$$
(3.3)

Depending on the sign of the carriers in the channel, each component of total resistance can be given as

$$R_{n1}^{even}(n_2) = R_{n1}^{even}(-n_2), R_{n1}^{odd}(-n_2) = -R_{n1}^{odd}(n_2)$$
(3.4)

Then the asymmetry observed in resistance depends on the sign of the carrier and it could be quantified by the odd part of the resistance as,

$$R_{n1}^{odd}(n_2) = \frac{1}{2} [R_{n1}^{odd}(-n_2) - R_{n1}^{odd}(n_2)]$$
(3.5)

From (1.4) it can be inferred that,

If $R_{n1}^{odd}(n_2) > 0$, n₂ (electrons experience more resistance) or n₁ is P-doped.

If $R_{n_1}^{odd}(n_2) < 0$, n_2 (holes experience more resistance) or n_1 is N-doped.

Graphically, this translates to R_{odd} saturating (for higher gate voltages) at positive value for P-doping contacts and negative value for N-doping contacts.

Figure 3-2 (b) (d) (f) shows R_{odd} plots for the three TLMs. Two distinct characteristics are observed. For low carrier density (< 2*10¹² cm⁻²), Rodd fluctuates to negative values and spikes (to negative/positive resistance) at certain charge density. However, at high charge densities, R_{odd} shows saturation similar to the case discussed above. It saturates to positive value here indicating P-doping contacts. The results are consistent with previous reports [24], [28]. The spikes occur close to the V_{NP} and hence indicate the crossing of Dirac point in the graphene channel as pointed out in [29]. The fluctuations at low carrier density result from charge inhomogeneity across the graphene plane. It is also observed that the saturation of Rodd to positive value is spread in Figure 3-2 (b) (d) then in Figure 3-2 (f).

3.5 SIMULATION

The experimental study indicated that even identical TLMs show significant variation. In other words, the doping by contacts could be highly susceptible to ambient conditions (moisture, chemicals etc.), fabrication process and measurement conditions. Though the process parameters are more controlled in fab lab, contact deposition to the extent of ensuring constant interface dipole equilibrium position (in the order of Å) for fixed doping by metal is impractical. A variation of 1-3Å could already change the doping by a factor of 4 [26]. As a result, realizing PN junctions through dissimilar metal contacts as in [30] would be prone to variability. A more robust way requires that the operating principle be understood in detail and suitable device design parameters be identified.

The following section reinterprets the resistance asymmetry with electron transport and band structure of graphene. Finally, a model based on Landaeur-Buttiker formalism is being developed to identify various design parameters for PN junctions.

Band structure at different regions of the device and for different back-gate biases are drawn in Figure 3-5. At the source and drain contacts, DOS is represented with a broadened E-K dispersion contrary to the linear dispersion for graphene. This is due to contact induced states present usually at metal-semiconductor interface. In graphene this effect is pronounced with invasive contacts and the induced states spread over longer distance into the channel, in the order of contact widths [31]. This increases the available states in graphene under the contacts [31].





Figure 3-5 Band structure at different regions of the device for different back-gate biases

Low field transport (small drain-source voltage) is assumed and therefore conduction along the Fermi-level (dashed line) is shown in Figure 3-5. Electron transport is being traced from drain to source terminal by the arrows. The transmission is favored whenever there are available states/channels (in the valence and conduction band) of graphene. Analogy of lanes in a road available for vehicle movement can be drawn upon to understand the electron transport here. Figure 3-5 (a), shows the case when electron conducts through the valence band from drain to source. It sees continuous states/channels for conduction and hence the low resistance. Close to the Dirac point Figure 3-5 (b), a high resistance is seen due to the non-availability of channels for conduction. The asymmetry in conductance/resistance plot refers to the energy bands as shown in Figure 3-5 (c). It arises out of electron transport from valence band in graphene under contacts to conduction band of the channel (interband tunneling). Though there is no bandgap as

tunneling barrier and the electron sees continuous channels for conduction, the transport across bands experiences more resistance due to electron wave function mismatch between the bands [29] Figure 3-5 (c). Figure 3-5 (d) shows yet another case where the asymmetry is greatly suppressed due to modulation of Fermi-level for graphene under the contacts using the global back-gate. This makes it possible for same band conduction (here valence band).

3.6 PN JUNCTION BY LANDAEUR APPROACH

The band picture developed above qualitatively explains the asymmetry in resistance plots. This understanding is further augmented with electrostatics of a device, using Landaeur-Buttiker (LB) model. In order to completely quantify the resistance plots, one needs to account for (a) back-gate modulation of Fermi-level under contacts (b) nonlinear E-K dispersion under the metal (C) electron and hole puddles. In this work, only (a) has been taken into account and also transport is assumed ballistic (i.e. no inelastic scattering of carriers). Therefore, the resistance values cannot be directly compared ti experiments but helps to determine the variables determining the operation.

Fig () shows two pair of P-N junctions in the device. For simplicity, a pair of P-N junction with equal hole and electron densities on either side of the junction (symmetrical junction) has been considered. Linear dispersion for DOS is assumed throughout. The conductance using Landaeur approach is given as [32],

$$G = \frac{4e^2}{h} \sum_{M} T(E)$$
(3.6)

Where M is the number of modes or conduction channels in the device and T is the electron transmission probability/coefficient, e and h are electron charge and Planck's constant, respectively.





To evaluate transmission coefficient, different electric field profile can be assumed for the transition region between P and N doped graphene. However, a simple case to evaluate has been done in [29],[33], assuming a linear potential drop V_{PN} over a length D_w . This allows for approximating the junction with WKB probability and gives per mode, a transmission coefficient of

$$T(\mathbf{K}_{y}) = (1 - \frac{K_{y}^{2}}{K_{f}^{2}}) e^{-\pi K_{f} D_{W}(\frac{K_{y}^{2}}{K_{f}^{2}})/2}$$
(3.7)

Where K_f is the fermi wave vector, K_y is the quantized transverse momentum.

The conductance plot can be obtained by integrating over all modes. Figure 3-7 - Figure 3-9 compares the simulated result with the NEGF simulation of [29].



Figure 3-7 (a) Simulated conductance for abrupt junction (red) (b) Conductance from NEGF simulation [29]



Figure 3-8 (a) Simulated conductance for different lengths of Dw: red- 0nm, brown -10nm, orange-50nm (b) Transmission coefficient for Dw=0nm (red) and 20nm (blue)



Figure 3-9 Resistance Vs Vpn (a) Simulated (b) NEGF [29]

Figure 3-7 - Figure 3-9 show the good agreement of our results with the one reported in literature [29]. A more detailed derivation is provided in APPENDIX I

From the above exercise, we have identified various design parameter and their physical analogues.

Case	Physical parameter	Design parameters
Ι	Ef	Global back-gate
Π	V _{pn}	Top gate / Embedded gates / Adsorbate / Voltage stress [34], contact doping
III	D _w	Electrostatic parameters of top gate [35]
IV	θ (incident angel w.r.t normal to junction)	Geometry variation
V	Transmission coefficient	Several scattering centers

Table 8 Design parameters for PN junctions

The total resistance given as,

$$G^{-1} = \frac{\hbar}{2e^2 MT} \tag{3.8}$$

Can be re-written as,

$$G^{-1} = \frac{\hbar}{2e^2 M} + \frac{\hbar(1-T)}{2e^2 MT}$$
(3.9)

Case I, II, III are parameters related to electrostatics of a device i.e. top gate and back-gate. The gates allow to modulate the junction width and it can be noticed that increasing the width few nm significantly increases the resistance asymmetry (Figure 3-8). The P and N regions could also be realized by adsorbates, contact-doping (different metals) or more interestingly using embedded gates. This dopes graphene electrostatically similar to case I, III but allows for more controllability over the region it dopes. Appendix () provides a new graphene PN junction using embedded gates. Case IV points out to filtering electrons which are incident at certain angle to the junction. It significantly alters the transmission probability. In Figure 3-8 (b), it can be seen that making the junction less steeper ($D_w=0$ nm to $D_w=20$ nm) significantly filters the incident electrons. An analogous way would be to use angled source and drain contacts. This again varies the angle at which electrons are injected w.r.t a fixed junction profile. Case V provides yet another possibility where the number of conducting channels/modes M is fixed and the transmission coefficient be increased with several scattering junctions (Equation(3.9)). However, inclusion of several scattering centers makes the device longer and adversely increase the footprint.

3.7 SHORT CHANNEL REGIME

Neutrality point shift: A significant effect of short channel in SI MOSFETs is the variation in threshold voltage. Similar to threshold voltage in Si FETs, the neutrality point defines the "off-state" of graphene. However, due to the absence of bandgap in graphene this "off" state is quite conducting. Figure 3-10 shows the variation of NP with length. As the channel was scaled down to 100nm, V_{NP} showed shift towards more positive voltages.



Figure 3-10 V_{NP} shift with channel length

In our case, the contact P dopes graphene and hence V_{NP} shifts towards more positive voltage for the charge neutral position (or Dirac point). Further, the V_{NP} for the 200nm wide channel was lesser in magnitude to the 500nm wide channel. This was suspected to be due to better electrostatic control in the 200nm wide device as the electric field should be more confined. Recent electromagnetic simulation [36] confirmed this observation.



Figure 3-11 Band structure for Lch <2Wc and Lch>2Wc

The trend of increasing V_{NP} as the channel length is decreased could be readily explained with the band structure as in section 3.5.

Two regions could be noticed.

(I) Length_{channel} > 2Width_{contact} – There is no change in V_{NP} . The contact doping doesn't extend in to the channel and NP is largely determined by the channel.

(II) Length_{channel}<2Width_{contact} – The doping of the contact extends well into the channel and here it P dopes graphene. This doping pushes the Fermi level far from Dirac point and hence the higher V_{NP} .

Further, there was no shift in V_{NP} observed over low source/Drain bias. However, at higher drain bias it is expected to reduce the control of gate over the channel.

Resistance asymmetry: The asymmetry between the P-branch and N-branch of resistance increases with scaling down of the channel length. It is expressed as $(R_n-R_p)/R_p$ where R_n is measured at $V_G-V_{NP}= 18V$ and R_p measured at $V_G-V_{NP}= -18V$.



Figure 3-12 Normalized resistance asymmetry between N branch and P branch

From Equation (3.9), resistance contribution could be from both the number of modes available for conduction under the contact and transmission probability across the P-N junction. Assuming only a large junction width (for e.g. D_w =50nm Figure 3-8 (a)) one could obtain strong asymmetries as seen above (~80% asymmetry for Wc=500nm comparing Figure 3-8 and Figure 3-12). But in [28] it has been experimentally demonstrated that this large asymmetry is the effect of both junction width (affecting the transmission probability) and the modulation of Fermi-level under the contacts (APPENDIX I).





Figure 3-13 I_{on}/I_{off} ratio v/s Channel length (a) 500nm wide sheet (b) 200nm wide sheet

The I_{on}/I_{off} ratio has been plotted as another parameter for the scaled down devices. The on and off ratio is calculated at $V_G-V_{NP}= 18V$ and V_{NP} for N-FET and at $V_G-V_{NP}= -18V$ and V_{NP} for P-FET. Naturally the P-doping contacts allow for better on/off ratio for the P-FETs. The degrading ratio has been interpreted as the transition from diffusively operated device to ballistic [28].

3.8 CONCLUSION

Process module of Chapter 2 was used to realize short channel Graphene FET devices. Contacts with graphene are quite unique. In that, the surface charge transfer results in doping graphene under contacts and this can be put to use in forming P and N doped regions. Following this, a methodical study using DC I-Vs, were used to determine type of doping by different metal. The observation was in good agreement with experiments by other groups [24],[28],[34]. The channel length scaling allowed to observe variation of device parameters such as V_{NP} , I_{on}/I_{off} and percentage asymmetry over different channel lengths, previously observed on graphene flakes [28]. Insights into the operating principle of the device was gained through simulation study. It immediately allowed to replicate various effects observed by other groups. Furthermore, more robust design parameters for PN junction were identified with these insights particularly making use of the unique properties of graphene – Veselago lens effect and new design with embedded gates has been proposed (APPENDIX II, APPENDIX III).

The observed trend in the performance parameters was in agreement with the physical picture developed. This clearly shows the various limitations that could be expected with scaled down graphene devices.

4 GATE STACK

4.1 INTRODUCTION

Si field effect transistors were highly successful partially because of its native oxide - SiO₂ which was used as gate dielectric [37]. SiO₂ provided a stable interface between the semiconducting channel and the top gate, with low, interface trap densities and carrier scattering, key in the performance of Si field effect transistors [37],[38]. Following Moore's law, downscaling of MOSFETs required the oxide to be scaled as well. However, below SiO₂ thicknesses of 1.3nm, direct tunneling from gate to silicon created large leakage currents. To reduce these leakage currents, high-k dielectric materials such as Al₂O₃, HfO₂, and TiO₂ were applied. They provided the same performance for physically thicker dielectric (2-10nm), while reducing the tunneling probability [39].

Integration of dielectrics on graphene would enable realization of high frequency transistors and also alternative logic devices such as TFETs. To grow such thin high-k dielectrics with good level of uniformity Atomic Layer Deposition (ALD) is a promising technique [40]. However, the absence of dangling bonds and hydrophobic nature of graphene prevents direct growth of ALD oxides. To overcome this issue, various surface treatments have been developed such as Ozone pretreatment [41], chemical pretreatment, polymer deposition [42] or e-beam metal deposition [43] as seed layers etc. But in the process, they inevitably damage the basal plane of graphene leading to loss in the carrier mobility.

In this chapter, direct ALD growth technique with H₂O precursors has been investigated following a recent study which had showed that within a low temperature ALD window, physical adsorption of ALD precursors (instead of chemical) can assist in uniform growth of oxides [44]. ALD recipe in line with [44] was developed and dualgated (Si bottom gate and top gate) graphene FETs were fabricated. Electrical characterization of these devices supported with SEM and AFM inspection of the deposited oxide have been presented.

4.2 **ATOMIC LAYER DEPOSITION**

ALD uses two self-limiting surface reactions sequentially for a controlled material deposition in each reaction cycle. The reactants, often called precursors, are never pulsed simultaneously to prevent gas phase reactions and hence prevent any parasitic depositions. The precursors are selected such that they are volatile but thermally stable at ALD temperature and undergo a self-terminating reaction [45]. ALD temperature would then refer to the temperature when deposition rate is uniform – layer by layer deposition. Typically, it is lower than 300°C and the window could be as narrow as 50°C.

ALD cycle includes four steps:

- 1- First precursor exposure: The metal precursor (e.g. TMA trimethyaluminum (Al(CH₃)₃) reacts with the –OH groups (reaction sites) adsorbed on the surface. The reaction stops when all the reaction sites are exhausted and they are terminated by -CH₃ groups.
- 2- **First purge step**: Usually Nitrogen or Argon gas is used to flush away the byproducts and un-reacted products of the first surface reaction.

- 3- Second precursor exposure: Precursor such as H₂O is then introduced to react with the –CH₃ groups forming methane gas and also replenish –OH groups for further reaction.
- 4- Second purge step: N₂/Ar removes the methane gas formed and unreacted H₂O precursor.

Reactions can be given as [46]:

$$AlOH * + Al(CH_3)_3 \rightarrow AlOAl(CH_3)_2 * + CH_4$$

$$(4.1)$$

$$AlCH_3^* + H_2O \to AlOH^* + CH_4 \tag{4.2}$$

Surface species are represented as *.





The exposure and purge times could be in milliseconds and several seconds, respectively, depending on the precursors [6]. As is evident from the above mechanism,

exposure and **purge times** along with **temperature** need to be optimized for uniform deposition.

4.2.1 ALD Growth on Graphene

Direct ALD growth on graphene with H₂O precursor has been quite challenging owing to graphene's chemical inertness and lack of bonds normal to its plane. Previous study [47] showed Al₂O₃ and HfO₂ growths along broken edges of graphene layer for temperatures ranging from 200°C to 300°C. Other works [48],[49] on epitaxial graphene grown on SiC substrate show similar behavior where nucleation sites are formed at the edges and terraces of SiC. Yet another study on mechanically exfoliated graphene [50], demonstrated ~30nm HfO₂ deposited at 110°C. They achieved good layer closure on single layer graphene (SLG) for oxide thickness > 10nm.

Recent work [44] has demonstrated uniform and pin-hole free deposition of Al₂O₃ with H₂O precursor through temperature optimization. It has been shown that at temperatures above 100°C a single layer of water molecule is physically adsorbed (instead of chemical) on the graphene surface [44][51][52]. For a narrow temperature window, this layer stays stable enough till the TMA pulse and a uniform oxide layer is being formed. Also, using long N₂ purge times after TMA and H₂O pulses, [44] has established that H₂O adsorption plays more important role than TMA in oxide growth on graphene.

4.2.2 ALD Recipe

The method suggested in [44], briefly described above, has been adopted in this work for developing top-gate dielectric. ALD was done on CVD graphene samples at 100°C, 125°C and 150°C. Temperature below 100°C wasn't tried as water may condense

on the surface leading to small island growth of oxides. On the contrary, temperatures above 150°C may evaporate parts of the adsorbed water layer leading to discontinuity in the oxide layer. The deposition scheme follows the sequence: TMA pulse/N₂ purge/H₂O pulse/N₂ purge. For each temperature run, two recipes – one with short TMA and H₂O pulses (called 'Short recipe (S)') and another with long TMA and H₂O pulses (called 'long recipe (L)') were adopted. The pulse and purge times for the short recipe, keeping the purge times constant, pulse time for TMA was increased four-fold while that for H₂O was set slightly higher than four-fold (limited by the system's maximum allowed pulse time). The longer recipe was expected to allow for more physical adsorption of TMA and H₂O precursor and hence achieve different uniformities within a given ALD temperature. This low temperature ALD on complete closure could then act as good seed layer for further growth of gate dielectrics at higher temperature.

4.3 FABRICATION

Graphene used in this work was purchased from the graphene vendor 'Graphenea'. This graphene is transferred on to a 4" thermally grown SiO₂ (300nm)/Si wafer. The wafer was diced and 6 chips of dimension 1cm*1cm were used for each of the recipe. SEM inspection before the ALD, reveals single layer graphene (SLG) with cracks and wrinkles (mostly from graphene transfer) and patches of bi- or even multiple layers Figure 4-. The quality of the SLG was further inspected with Raman Spectroscopy. An area of $36\mu m^2$ for one of the samples was mapped and the integrated intensity ratios (2D peak to G peak and D peak to G peak) plotted Figure 4-3. G-band arises from the stretching of the C-C bond
in graphitic materials, and is common to all sp² carbon systems. The D-mode is caused by disordered structure of graphene. Ratio of the D to G peak intensities varies inversely with the crystallite size, La i.e. level of disorder. 2D-band is a second-order two-phonon process which can be used to determine the number of layer of graphene. Monolayer graphene shows one strong 2D peak which broadens with number of layers and splits into two in bulk graphite.

The ratio $I_{2D}/I_G \sim 1$ was observed. The significant deviation from ideal ratio of 2 could be because of the wider laser beam size used for Raman spectroscopy and hence the reading of the SLG peaks could be convoluted with the contribution of the bi/multi-layer patches adjacent to them. Also, the lower value could indicate doping of the monolayer by the substrate [18]. From the ratio I_D/I_G , distance between Raman active defect sites La could be evaluated [53]. This implies that there could be defects within the graphene strip used as the channel material [54]. Carrier mobility for these devices are therefore low compared to exfoliated graphene.

To fabricate FETs, Electron-Beam lithography mask similar to section 2.2, was designed. TLM structures was used for the Source/Drain design. The top gates are laid out as shown in Figure 4-4 overlapping completely with the rectangular graphene strip below (red in the figure)



Figure 4-2 SEM images of graphene samples before ALD



Figure 4-3 (a)Raman Spectroscopy of the graphene sample before ALD (b)I_{2D}/I_G and (c)I_D/I_G mapping for an area of $36\mu m^2 of$ the sample



Figure 4-4 E-beam mask for overlapping top-gate TLM structures

The process flow for top-gated devices is as follows,

- 1- Al₂O₃ is deposited on the back-gated devices using the commercially available ASM international Polygon ALD fab tool. Recipes same as mentioned in Section 4.2.2 are being used. The ALD temperature mentioned in the recipe refers to the chamber temperature and not the substrate temperature. A complete layer closure is targeted at ~4nm thickness.
- 2- The above layer acted as seed layer for further growth of oxide. A second ALD oxide layer of 10nm Al₂O₃ was deposited using standard 300°C recipe in the Cambridge Nanotech Savannah 200 thermal ALD system.
- 3- Finally the top gates are defined by layer 2; PMMA recipe section 2.3 was used for defining the patterns. 1nm Titanium and 30nm Gold are evaporated and patterned by the acetone lift-off process to form the top gate electrode.

The above steps have been summarized in the process flowchart Figure 4-5. Device dimensions of the top-gated TLM is provided in Table 9.



Figure 4-5 Process flow for top-gated TLM structures

	TLM
L _{ch}	100 nm -1 mm
TG	overlapping
Wch	0.5-1-0.2 mm

Table 9 Top gate TLM device dimensions

4.4 **RESULTS**

4.4.1 Physical characterization

Raman inspection was carried out on the samples after the low temperature ALD to check for any change in graphene quality. Figure 4-6 shows the Raman spectroscopy of the samples after ALD.



Figure 4-6 Raman spectroscopy for samples of the six recipes after ALD (a) 100°C short (b) 100°C long (c) 125°C short (d) 125°C long (e) 150°C short (f) 150°C long

No significant deviation was observed between the characteristic peaks before Figure 4-3(a) and after ALD Figure 4-6 (a) for the short recipe at 100°C. This observation holds true for the other samples as well. Thus the quality of graphene was not degraded by the ALD process. Further SEM inspection helped to estimate morphological detail of the oxide layer (Figure 4-7). It can be seen that ALD at 100°C (Figure 4-7 (a) and (b)) has large cracks for the different pulse times. It was probably because the substrate was below 100°C, and water clusters could have formed due to surface tension similar to 50°C (substrate temperature) run in [44]. It can also be concluded that the substrate temperature is not too different from the chamber temperature as the clusters are not quite distinct as in [44] and rather closed. 125°C and 150°C runs show better films with the long recipes showing almost closed films with few pin-holes (Figure 4-7(d) and (f)). Thus, the longer pulse times with higher temperatures (125°C and 150°C) especially for H₂O has indeed helped in attain a uniform adsorption of the precursors on graphene sheet. Naturally, 125°C and 150°C, "Long recipes" showed better yield than the others.

4.4.2 Electrical Characterization

Two types of electrical measurements are performed: DC- IV measurement for the FETs and CV measurement for the MOSCAPs. DC- IV involved top gate voltage sweep $V_{topgate}$ with two drain voltages $V_d = 5mV$, 10mV. The sweep range for top-gate varied from chip-to-chip due to different quality of the oxide film. However, for consistency in measurements, top-gate sweep was always performed from most negative to most positive voltage bias and then reversed. The bottom gate was grounded for all measurements.



Figure 4-7 SEM images of Al_2O_3 on graphene (a) $100^{\circ}C - S$, (b) $100^{\circ}C - L$, (c) $125^{\circ}C - S$, (d) $125^{\circ}C - L$, (e) $150^{\circ}C - S$, (f) $150^{\circ}C - L$



Figure 4-8. Typical IV curves for each of the six samples (a) 100°C short (b) 100°C long (c) 125°C short (d) 125°C long (e) 150°C short (f) 150°C long recipes

Modulation depth (I_{max}/**I**_{min}) was better in the long recipes of 125°C and 150°C compared to other samples (Figure 4-8 (d) and (f)). This is in fact the result of well closed films as seen in Figure 4-7 (d) and (f), and hence better electrostatic control of the gate over the channel.

Neutrality point (NP): Though graphene is ambipolar, NP of the forward sweep was well shifted to positive/negative gate voltages and hence the channel exhibited predominantly hole (PFET)/electron (NFET) conduction within the sweep window. The shift results from doping of the channel. The P-doping (positive NP) was quite common and this could result from doping by ALD precursor H₂O. Especially, the long recipes may accumulate more than a mono-layer of precursor material and the successive surface reactions would then leave certain amount of precursors in the graphene-oxide interface. This usually P-dopes graphene as seen in Figure 4-8 (a), (c) and (f). However, it was difficult to conclusively comment on the source of doping as certain devices within the same sample showed opposite behavior (N-type). These local fluctuations could also result from resist residues in the process [25] or from carrier inhomogeneity along the graphene plane [55].

Gate voltage sweep range varied from chip-to-chip. Variation in film thickness and also the quality of the film itself – pin-holes and accumulation of unreacted precursors resulted in gate leakage currents and variations in breakdown voltage, The gate voltage was limited the ranges shown in Figure 4-8 in order to avoid electric breakdown and increased gate leakage currents. The range was widest at -8V to 8V (Electric field of 0.57V/nm) and narrow at -4V to 4V (electric field of 0.28V/nm). **Hysteresis** behavior was observed in the all the I-V curves. This could originate from capacitive coupling by polar molecules (such as H₂O, e-beam resists etc.) or charge trapping in the gate dielectric [21]. It is noted that the NP for the backward sweep shifts in the positive direction for all the samples and this is particularly due to the fixed negative charges in the Al₂O₃ [56]. However, this shift varies between samples and also increases with increase in the top-gate sweep range. For the sample of 125°C, the NP shift was studied by applying different ranges of top gate voltage (stress).



Figure 4-9 (a) I-V curves for voltage stress test done on Sample 6 (b) I-V showing the behavior around V_{NP} for different stress

When the voltage is in the range -3 to 3 V (for 15nm Al₂O₃), NP shifts by 0.75 V and it increases to 2.7 V for a sweep of -5 to 5 V. As mentioned in [21], the oxide with its distribution of interface and bulk traps in the oxide band gap are continuously populated as the gate potential is tuned, changing the oxide charge and hence the threshold voltage of the device. But unlike [21], the electric field in our devices is sufficiently high to charge the bulk traps in the oxide.

Transconductance and carrier mobilities were calculated. Transconductance was

calculated as
$$\frac{\delta I_D}{\delta V_{topgate}}$$
 and mobility as $\frac{\delta I_D}{\delta V_{topgate}} \frac{L}{W.CV_{DS}}$ where L, W are the length and

width of the channel and C is the graphene to top-gate capacitance. Mobility is calculated at the steepest point of the I_{drain}-V_{topgate} ($\frac{\delta I_D}{\delta V_{topgate}}$ is maximum) curve. Electron mobility for

 $V_{topgate}\!>\!\!0$ and Hole mobility for $V_{topgate}\!<\!\!0$ are reported.







Figure 4-10 Ion/Ioff, Vcn (Neutrality point), Peak transconductance for electrons, Peak transconductance for holes plotted for different ALD samples (D01-100°C 'short', D02 – 100°C 'Long', D05- 125°C 'short', D06- 125°C 'Long', D09- 150°C 'Short', D10- 150°C 'Long'

The hysteresis in the transfer I-V characteristics was accompanied by peaking and broadening of DC Transconductance (G_m) for the devices. This was again related to the presence of interface traps being charged and discharged as the channel is modulated. This in turn suppresses the electric field and degrades the I-V curves. Following this proposition, electrostatics of top-gated graphene device was investigated.



Figure 4-11Band diagram for top-gated graphene FET ($V_G>0$)

As pointed out in [57], the depletion layer capacitance of Si-MOSFET is replaced by quantum capacitance of graphene. Then an equivalent circuit model would look like in



Figure 4-12Equivalent circuit for top-gated (a) graphene FET (b) Si-MOSFET [57]

Where C_Q- quantum capacitance

C_{it}-interface trap capacitance

Cox - gate oxide capacitance

Detailed derivation of the various capacitances and a methodology to extract surface potential change ($\phi_{graphene}$) with top-gate bias is provided in APPENDIX IV.

The potential $\phi_{graphene}$ was extracted from C-V measurements of Graphene MOSCAPs with 15nm Al₂O₃ oxide using the methodology in APPENDIX IV. Further, the potential drop across the oxide was evaluated from this data. Using an in-house simulator, an approximate evaluation of the threshold shift was calculated for graphene with a defect band previously known for Al₂O₃.





Figure 4-13(a) Graphene surface potential v/s V_{topgate} (b) Voltage drop across oxide v/s V_{topgate} (c) Threshold shift v/s V_{topgate} (Red-Graphene, Green- Si)

It is noted that the threshold voltage reaches an early saturation in case of graphene compared to silicon. This is due to the considerable shift in graphene surface potential with top-gate bias. It enhances the injection of electrons into the traps with oxide band bending whereas in silicon the traps are filled only with oxide band bending at high fields. The discharge is also expected to happen fast with such device and this could explain the behavior of transconductance obtained for these devices. Pulse measurements could help understand these devices better.

4.5 CONCLUSION

High-k top gate dielectric is required for scaling down of devices with reasonable leakage currents. In case of bilayer graphene this becomes even more important as vertical electric field with dual-gates is necessary to open a band-gap. In this chapter, we have demonstrated a scalable ALD process to realize high-k dielectrics on SLG. This has been achieved by optimizing ALD temperature and precursor especially H_2O pulse time. Also, the process damage to graphene is very minimal (from Raman inspection). However, from the electrical characterization, it can be seen that the neutrality point V_{NP} shifts drastically with applied top gate sweep. This could pose serious problems for logic devices realized with bi-layer graphene.

5 CONCLUSIONS

Following the technical hurdles presented in realizing 2D logic devices, we have tried to address few of them in this dissertation. The observations, learnings and scope for future work have been summarized for each topic dealt.

5.1 CONTACT SCALING WITH MOS₂ FETS

The case study on MoS₂ showed that performance for the short channel devices is dominated by the source/drain contacts. It was observed that Au contacts resulted in lower Schottky barrier compared to Ti/Au contacts on 15nm thick MoS₂ flake, boasting the performance of the devices by several orders (section 2.4.2). Further drop in channel resistance with sub-50nm devices require that the contact resistivity be reduced even further. Shrinking of the source and drain regions for these materials to reduce the overall footprint of the devices translates to reducing the transfer length for the contacts. This again necessitates evaluation of Schottky barrier formed by different metals with MoS₂. Conventional ways to create low resistivity contacts by doping source and drain region with ion implantation or diffusion is rather difficult with the ultra-thin nature of MoS₂. Recent demonstrations such as surface chemical doping or doping of defective sites replacing the sulphur with chlorine atoms [58] (similar to substitution doping in Si) could be good alternatives to overcome the Schottky junction.

5.2 DOPING GRAPHENE WITH CONTACT METAL

Doping of graphene through contacts has been suggested in literature [] as a way to realize logic devices. However, the variability in electrical behavior between samples prepared in the same lot is discouraging. Though the process parameters are more controlled in fab lab, dependence of the variability on equilibrium position of metal-graphene interface dipole usually in the order of 1^{0} A- 3^{0} A could already vary the doping by 4-5 times [26]. Thus device architectures based on contact doping would be prone to considerable variability.

The shift of neutrality point and enhanced resistance asymmetry with channel length shrinking clearly indicated the extent of metal induced states in the graphene channel. This results in non-linear E-K dispersion and hence loss of ultra-relativistic character of electrons near the Fermi level. This in turn leads to loss of field mobility for these devices.

The I_{on}/I_{off} ratio is low for SLG due to the absence of bandgap. It is observed that Ion/Ioff ratio for SLG drops with channel shrinking and this is attributed to the transition from diffusive to ballistic transport in the downscaled devices section 3.7. In BLG the absence of bandgap is overcome through chemical doping [4] or dual gated architecture [59]. But trend similar to SLG due to change in transport could be a roadblock for FET based device architecture.

For a TFET architecture, abruptness of source –channel junction is also important as the contact-induced doping. In case of SLG, it is observed that the low density of states enhances non-linear screening of charges close to the metal contacts. For architectures utilizing metal doping, this screening length would refer to the abruptness of doping profile. Then, the enhanced resistance asymmetry for short channel (section 3.7), which was associated with PN junction resistance, point out that this profile was altered with downscaling (for same back-gate bias). The increment in junction resistance can result from increase in the transition length of potential drop D_w (section 3.6) or the junction profile close to the contacts by presence of similarly doped graphene channel [60]. Either way, it results in loss of abrupt junctions or it is discouraging for TFET.

5.3 ALD HIGH-K DIELECTRIC FOR GRAPHENE

ALD growth on CVD graphene by optimizing temperature and pulse times has been demonstrated. The growth was achieved through physical adsorption of precursors on graphene (vander waals' interaction) and this could result in traps close to the interface [61]. It would be most natural to use isomorph insulators such as hBn with 2D materials for less interface traps. However, equivalent oxide thickness (EOT) scaling to improve device performance with a reasonable level of gate leakage is difficult with the low dielectric of hBn.

Presence of interface traps in the oxide and inherent quantum capacitance limit graphene devices were identified as the key reasons for the large threshold shifts with applied gate potential. Graphene in "inversion" experience large surface potential change unlike Si or III-V FETs where the gate voltage completely drops across the oxide. The surface potential change enhances charge trapping in high k dielectrics with band bending of oxide, severely altering the threshold voltages and the transconductance of the device as demonstrated in section 4.4.2. More detailed experiments with pulse-measurements needs to be done.

REFERENCES

- [1] D. Jena, "Tunneling transistors based on graphene and 2-D Crystals," *Proc. IEEE*, vol. 101, pp. 1585–1602, 2013.
- [2] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, F. Jeffrey Bokor, and C. Hu, "FinFET-A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, pp. 2320–2325, 2000.
- [3] F. Schwierz, "Graphene transistors.," *Nat. Nanotechnol.*, vol. 5, no. 7, pp. 487–96, Jul. 2010.
- [4] A. J. Samuels and J. D. Carey, "Molecular doping and band-gap opening of bilayer graphene," *ACS Nano*, vol. 7, pp. 2790–2799, 2013.
- [5] A. Nourbakhsh, A. Klekachev, I. Asselberghs, M. Cantoro, C. Huyghebaert, M. Heyns, and S. De Gendt, "High performance, chemically enhanced, dual-gate bilayer graphene FET with neutral channel for logic applications," vol. 951, no. 2006, pp. 4–6, 2011.
- [6] M. Raghu, Graphene Nanoelectronics. .
- [7] A. Khakifirooz and D. A. Antoniadis, "MOSFET Performance Scaling—Part I: Historical Trends," *Electron Devices, IEEE Trans.*, vol. 55, pp. 1391–1400, 2008.
- [8] A. Khakifirooz and D. A. Antoniadis, "MOSFET Performance Scaling—Part II: Future Directions," *Electron Devices, IEEE Trans.*, vol. 55, pp. 1401–1408, 2008.
- [9] D. K. Schroder, Semiconductor Material and Device Characterization: Third Edition. 2005, pp. 1–779.
- [10] L. Landau, "Nanofabrication Techniques and Principles," *Zhurnal Eksp. i Teor. Fiz.*, 1937.
- [11] "http://www.microchem.com/pdf/PMMA_Data_Sheet.pdf." [Online]. Available: http://www.microchem.com/pdf/PMMA_Data_Sheet.pdf. [Accessed: 09-Sep-2014].
- [12] Y.-H. Lee, "Low voltage alternative for electron beam lithography," J. Vac. Sci. Technol. B Microelectron. Nanom. Struct., vol. 10, no. 6, p. 3094, Nov. 1992.

- [13] L. Ren, "Proximity Effect in Electron Beam Lithography," pp. 579–582, 2004.
- [14] M. A. Mohammad, T. Fito, J. Chen, S. Buswell, M. Aktary, M. Stepanova, and S. K. Dew, "Systematic study of the interdependence of exposure and development conditions and kinetic modelling for optimizing low-energy electron beam nanolithography," *Microelectron. Eng.*, vol. 87, pp. 1104–1107, 2010.
- [15] S. Lebègue and O. Eriksson, "Electronic structure of two-dimensional crystals from ab initio theory," *Phys. Rev. B Condens. Matter Mater. Phys.*, vol. 79, 2009.
- [16] K. Mak, C. Lee, J. Hone, J. Shan, and T. Heinz, "Atomically Thin MoS_{2}: A New Direct-Gap Semiconductor," *Physical Review Letters*, vol. 105. 2010.
- [17] H. Liu, A. T. Neal, and P. D. Ye, "Channel length scaling of MoS2 MOSFETs.," ACS Nano, vol. 6, no. 10, pp. 8563–9, Oct. 2012.
- [18] W. Bao, X. Cai, D. Kim, K. Sridhara, and M. S. Fuhrer, "High mobility ambipolar MoS2 field-effect transistors: Substrate and dielectric effects," *Appl. Phys. Lett.*, vol. 102, 2013.
- [19] Y. Zhang, J. Ye, Y. Matsuhashi, and Y. Iwasa, "Ambipolar MoS 2 thin flake transistors," *Nano Lett.*, vol. 12, pp. 1136–1140, 2012.
- [20] B. Radisavljevic, a Radenovic, J. Brivio, V. Giacometti, and a Kis, "Single-layer MoS2 transistors.," *Nat. Nanotechnol.*, vol. 6, no. 3, pp. 147–50, Mar. 2011.
- [21] J. J. Gu, Y. Q. Wu, and P. D. Ye, "Effects of gate-last and gate-first process on deep submicron inversion-mode InGaAs n-channel metal-oxide-semiconductor field effect transistors," J. Appl. Phys., vol. 109, 2011.
- [22] P. A. Khomyakov, A. A. Starikov, G. Brocks, and P. J. Kelly, "Nonlinear screening of charges induced in graphene by metal contacts," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 82, 2010.
- [23] P. a. Khomyakov, G. Giovannetti, P. C. Rusu, G. Brocks, J. van den Brink, and P. J. Kelly, "First-principles study of the interaction and charge transfer between graphene and metals," *Phys. Rev. B*, vol. 79, no. 19, p. 195425, May 2009.
- [24] B. Huard, N. Stander, J. Sulpizio, and D. Goldhaber-Gordon, "Evidence of the role of contacts on the observed electron-hole asymmetry in graphene," *Phys. Rev. B*, vol. 78, no. 12, p. 121402, Sep. 2008.

- [25] H. Wang, Y. Wu, C. Cong, J. Shang, and T. Yu, "Hysteresis of electronic transport in graphene transistors.," *ACS Nano*, vol. 4, no. 12, pp. 7221–8, Dec. 2010.
- [26] F. Xia, V. Perebeinos, Y. Lin, Y. Wu, and P. Avouris, "The origins and limits of metal-graphene junction resistance.," *Nat. Nanotechnol.*, vol. 6, pp. 179–184, 2011.
- [27] B. Huard, J. Sulpizio, N. Stander, K. Todd, B. Yang, and D. Goldhaber-Gordon, "Transport Measurements Across a Tunable Potential Barrier in Graphene," *Phys. Rev. Lett.*, vol. 98, no. 23, p. 236803, Jun. 2007.
- [28] Y. Wu, V. Perebeinos, Y. M. Lin, T. Low, F. Xia, and P. Avouris, "Quantum behavior of graphene transistors near the scaling limit," *Nano Lett.*, vol. 12, pp. 1417–1423, 2012.
- [29] T. Low, S. Hong, J. Appenzeller, S. Member, S. Datta, and M. S. Lundstrom, "Conductance Asymmetry of Graphene p-n Junction," vol. 56, no. 6, pp. 1292– 1299, 2009.
- [30] G. Fiori, G. Iannaccone, and I. Elettronica, "Ultra-low-voltage bilayer graphene tunnel FET," pp. 1–10, 2009.
- [31] R. Golizadeh-mojarad and S. Datta, "Effect of contact induced states on minimum conductivity in graphene," vol. 1, no. 1, pp. 0–4, 2007.
- [32] S. Datta, *Quantum Transport : Atom to Transistor*.
- [33] V. V. Cheianov and V. I. Fal'ko, "Selective transmission of Dirac electrons and ballistic magnetoresistance of n-p junctions in graphene," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 74, 2006.
- [34] H.-Y. Chiu, V. Perebeinos, Y.-M. Lin, and P. Avouris, "Controllable p-n junction formation in monolayer graphene using electrostatic substrate engineering.," *Nano Lett.*, vol. 10, no. 11, pp. 4634–9, Nov. 2010.
- [35] L. M. Zhang and M. M. Fogler, "Nonlinear screening and ballistic transport in a graphene p-n junction," *Phys. Rev. Lett.*, vol. 100, 2008.
- [36] M. J. Hollander, N. Shukla, N. Agrawal, H. Madan, J. A. Robinson, and S. Datta, "Reduction of Charge Transfer Region Using Graphene Nano-ribbon Geometry for Improved Complementary FET Performance at Sub-Micron Channel Length Long Channel," pp. 151–152, 2013.

- [37] E. A. Irene, "SiO2 Based MOSFETS: Film Growth and Si—SiO2 Interface Properties," in *High Dielectric Constant Materials SE - 3*, vol. 16, H. R. Huff and D. C. Gilmer, Eds. Springer Berlin Heidelberg, 2005, pp. 45–90.
- [38] E. Kooi[†] and A. Schmitz, "Brief Notes on the History of Gate Dielectrics in MOS Devices," in *High Dielectric Constant Materials SE - 2*, vol. 16, H. R. Huff and D. C. Gilmer, Eds. Springer Berlin Heidelberg, 2005, pp. 33–44.
- [39] Q. Lu, D. Park, A. Kalnitsky, C. Chang, C. C. Cheng, S. P. Tay, T. J. King, and C. Hu, "Leakage current comparison between ultra-thin Ta2O5 films and conventional gate dielectrics," *IEEE Electron Device Lett.*, vol. 19, pp. 341–342, 1998.
- [40] A. Deshpande, R. Inman, G. Jursich, and C. Takoudis, "Atomic layer deposition and characterization of hafnium oxide grown on silicon from tetrakis(diethylamino)hafnium and water vapor," *J. Vac. Sci. Technol. A*, vol. 22, pp. 2035–2040, 2004.
- [41] B. Lee, G. Mordi, M. J. Kim, Y. J. Chabal, E. M. Vogel, R. M. Wallace, K. J. Cho, L. Colombo, and J. Kim, "Characteristics of high-k Al2O3 dielectric using ozonebased atomic layer deposition for dual-gated graphene devices," *Appl. Phys. Lett.*, vol. 97, 2010.
- [42] D. B. Farmer, H. Y. Chiu, Y. M. Lin, K. A. Jenkins, F. Xia, and P. Avouris, "Utilization of a buffered dielectric to achieve high field-effect carrier mobility in graphene transistors," *Nano Lett.*, vol. 9, pp. 4474–4478, 2009.
- [43] A. Pirkle, R. M. Wallace, and L. Colombo, "In situ studies of Al2O3 and HfO2 dielectrics on graphite," *Appl. Phys. Lett.*, vol. 95, 2009.
- [44] Y. Zhang, Z. Qiu, X. Cheng, H. Xie, H. Wang, X. Xie, Y. Yu, and R. Liu, "Direct growth of high-quality Al 2 O 3 dielectric on graphene layers by low-temperature H 2 O-based ALD," J. Phys. D. Appl. Phys., vol. 47, no. 5, p. 055106, Feb. 2014.
- [45] R. L. Puurunen, "Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process," *J. Appl. Phys.*, vol. 97, no. 12, p. -, 2005.
- [46] S. M. George, "Atomic layer deposition: an overview.," *Chem. Rev.*, vol. 110, no. 1, pp. 111–31, Jan. 2010.
- [47] Y. Xuan, Y. Q. Wu, T. Shen, M. Qi, M. A. Capano, J. A. Cooper, and P. D. Ye, "Atomic-layer-deposited nanostructures for graphene-based nanoelectronics," *Appl. Phys. Lett.*, vol. 92, 2008.

- [48] F. Speck, M. Ostler, J. Rohrl, K. V. Emtsev, M. Hundhausen, L. Ley, and T. Seyller, "Atomic layer deposited aluminum oxide films on graphite and graphene studied by XPS and AFM," in *Physica Status Solidi (C) Current Topics in Solid State Physics*, 2010, vol. 7, pp. 398–401.
- [49] N. Y. Garces, V. D. Wheeler, J. K. Hite, G. G. Jernigan, J. L. Tedesco, N. Nepal, C. R. Eddy, and D. K. Gaskill, "Epitaxial graphene surface preparation for atomic layer deposition of Al2O3," *J. Appl. Phys.*, vol. 109, no. 12, p. 124304, 2011.
- [50] K. Zou, X. Hong, D. Keefer, and J. Zhu, "Deposition of high-quality HfO2 on graphene and the effect of remote oxide phonon scattering," *Phys. Rev. Lett.*, vol. 105, 2010.
- [51] P. Solís-Fernández, J. I. Paredes, S. Villar-Rodil, A. Martínez-Alonso, and J. M. D. Tascón, "Determining the thickness of chemically modified graphenes by scanning probe microscopy," *Carbon N. Y.*, vol. 48, pp. 2657–2660, 2010.
- [52] M. J. Allen, V. C. Tung, and R. B. Kaner, "Honeycomb carbon: A review of graphene," *Chem. Rev.*, vol. 110, pp. 132–145, 2010.
- [53] L. G. Canado, K. Takai, T. Enoki, M. Endo, Y. A. Kim, H. Mizusaki, A. Jorio, L. N. Coelho, R. Magalhães-Paniago, and M. A. Pimenta, "General equation for the determination of the crystallite size la of nanographite by Raman spectroscopy," *Appl. Phys. Lett.*, vol. 88, 2006.
- [54] J. C. Koepke, J. D. Wood, D. Estrada, Z. Y. Ong, K. T. He, E. Pop, and J. W. Lyding, "Atomic-scale evidence for potential barriers and strong carrier scattering at graphene grain boundaries: A scanning tunneling microscopy study," ACS Nano, vol. 7, pp. 75–86, 2013.
- [55] J. Martin, N. Akerman, G. Ulbricht, T. Lohmann, J. H. Smet, K. von Klitzing, and A. Yacoby, "Observation of electron-hole puddles in graphene using a scanning single-electron transistor," *Nature Physics*, vol. 4. pp. 144–148, 2008.
- [56] S. A. Imam, T. Deshpande, A. Guermoune, M. Siaj, and T. Szkopek, "Charge transfer hysteresis in graphene dual-dielectric memory cell structures," *Appl. Phys. Lett.*, vol. 99, no. 8, 2011.
- [57] G. Zebrev, "Using capacitance methods for interface trap level density extraction in graphene field-effect devices," ... (MIEL), 2012 28th ..., 2012.

- [58] Y. Du, H. Liu, A. T. Neal, M. Si, and P. D. Ye, "Molecular doping of multilayer mos2 field-effect transistors: Reduction in sheet and contact resistances," *IEEE Electron Device Lett.*, vol. 34, pp. 1328–1330, 2013.
- [59] F. Xia, D. B. Farmer, Y. M. Lin, and P. Avouris, "Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature," *Nano Lett.*, vol. 10, pp. 715–718, 2010.
- [60] M. Ghaznavi, Z. L. Miskovic, and F. O. Goodman, "Non-linear screening of charged impurity by graphene," *cond-mat/0910.3614*, 2009.
- [61] Y. G. Lee, C. G. Kang, U. J. Jung, J. J. Kim, H. J. Hwang, H.-J. Chung, S. Seo, R. Choi, and B. H. Lee, "Fast transient charging at the graphene/SiO[sub 2] interface causing hysteretic device characteristics," *Appl. Phys. Lett.*, vol. 98, no. 18, p. 183508, 2011.
- [62] "http://tuttle.merc.iastate.edu/ee432/topics/metals/tlm_measurements.pdf." [Online]. Available: http://tuttle.merc.iastate.edu/ee432/topics/metals/tlm_measurements.pdf. [Accessed: 09-Sep-2014].

APPENDIX I

Wave function mismatch in the bands contributes to the asymmetry. Band-to-Band tunneling isn't quite evident as electron sees a continuous DOS throughout the device.



Figure A 1 Bandstructure of graphene FET

Tracing electron through the various bands following from Source to Drain terminal. Group Velocity from the E-K relation defined as

$$VG = \frac{\partial E}{\hbar \partial K}$$

Injection from the contacts assumed ideal. The momentum change along the propagation direction is brought about by the potential barrier/Field. Momentum along transverse direction conserved (No field along that direction). Conduction assumed along Fermilevel (low bias transport) and no scattering.

$$eEfield = \frac{\partial P (crystal momentum)}{\partial t}$$

 $Ky \ conserved \ or \ Ey = 0$

Energytotal Conserved = EF

Linear E-K relationship assumed. Dirac point (w.r.t E_F) shifted with global Back-gate and V_{PN} is set by contact/adsorbate/electrostatic doping.

 $Ky = Kfsin\theta (Ky momentum conserved)$ $E = \hbar V f \sqrt{Kx^2 + (Kfsin\theta)^2} (Total Energy)$ $Kx(x) = \sqrt{(\frac{E(x)}{\hbar V f})^2 - (Kfsin\theta)^2}$ E(x) = EDIRAC (X) - EF (X)

 θ – Angle of incident electron w.r.t normal drawn to junction



Figure A 2 Graphene PN junction

 $Ey = \hbar V f K f sin \theta$ (Transverse Energy)

 $Ebandgap = 2\hbar V f K f sin \theta$

$$Kx(x) = \sqrt{\left(\frac{E(x)}{\hbar V f}\right)^2 - \left(Kfsin\theta\right)^2}$$

 $T: e^{-2i \int_{-l}^{+l} Kx(X) dx} (WKB approximation)$

$$l = \hbar V f K f sin \theta D w / V P N$$

With symmetrical junction approximation, the transmission coefficient can be written as,

T: $e^{-\pi K f D w s i n 2\theta/2}$

(Or)

T: $e^{-\pi E2bandgap/(CVPN)}$



Figure A 3Quantum junction

Non-interacting Scatterer (no inelastic collisions – tunneling barrier/impurity etc.). Mode - conserving scattering is assumed. Transverse modes are conserved.

$$JL - R = e \sum_{n} \int TL - R(n, Kx) VL(n, Kx) \cdot fL(n, Kx) \frac{\partial Kx}{2\pi}$$

Tunneling Barrier with Transmission coefficient obtained previously. Mode - conserving scattering. Transverse modes conserved by minimum number of modes assumed for both N and P side. Sufficiently wide Graphene strip considered so that a periodic boundary condition for transverse modes be assumed.

$$EF = \hbar VFKF$$
$$D(E) = \frac{2E}{\pi(\hbar VF)^2}$$
$$M(E) = \frac{2W.E}{\pi\hbar VF}$$

. . .

$$JL - R = e \sum_{n} \int TL - R(n, Kx) VL(n, Kx) \cdot fL(n, Kx) \frac{\partial Kx}{2\pi}$$



Figure A 4 I-V characteristics of PN junction

- 1. Ef Bottom gate (Global)
- Vpn Electrostatic doping (Top gate)/embedded gates/Adsorbate/Voltage stress/Contact doping
- 3. Dw depends on charge densities on N & P side, Tox, k (dielectric constant)
- 4. $\boldsymbol{\theta}$ depends on the normal to junction (Geometry variation)
- 5. Several Scattering centers (transmission coefficient additive)

$$G - 1 = \frac{\hbar}{2e2MT} (Total Conductance)$$
$$G^{-1}c = \frac{\hbar}{2e2M} (contact resistance)$$
$$G^{-1}s = \frac{\hbar(1 - T)}{2e2MT} (Junction resistance)$$

T - transmission coefficient engineering to achieve better rectification

APPENDIX II



Figure A 5 Resistance plot of PN junction with SLG



Figure A 6 Resistance plot with double peak and different drain bias



Figure A 7Embedded gate design for PN junction

APPENDIX IV

Quantum Capacitance

Density of states for graphene is given as,

$$D(E) = \frac{2|E|}{\pi\hbar^2 V_F^2}$$

Then electron concentration $n_e(E)$ can be calculated as follows,

$$n_{e}(E) = \int_{0}^{\infty} D(E) \cdot f(E - E_{F}) \cdot dE$$
$$n_{e}(E) = \frac{2(K_{B}T)^{2}}{\pi \hbar^{2} V_{F}^{2}} \int_{0}^{\infty} \frac{E}{1 + \exp^{\frac{E - E_{F}}{K_{B}T}}} \cdot dE$$

Similarly,

For the holes concentration $n_h(E)$,

$$n_h(E) = -\frac{2(K_B T)^2}{\pi \hbar^2 V_F^2} \int_{-\infty}^0 \frac{E}{1 + \exp^{\frac{E - E_F}{K_B T}}} dE$$

With the carrier concentrations, quantum capacitance can be calculated as Cq,

$$\frac{dn_e(E)}{dE} = \frac{2(K_BT)}{\pi\hbar^2 V_F^2} \ln(1 + \exp^{E/K_BT}) , \frac{dn_h(E)}{dE} = \frac{2(K_BT)}{\pi\hbar^2 V_F^2} \ln(1 + \exp^{-E/K_BT})$$
$$C_q(E) = e \frac{d(n_e - n_h)}{dE} = \frac{2(K_BT)}{\pi\hbar^2 V_F^2} \ln(2 + 2\cosh(E/K_BT))$$

Electrostatics of Graphene- Oxide- Metal structure

Band diagram with VG>0 is shown in .

Then assuming zero current flow across the oxide, the electric potentials can be equated as,

$$eV_G = e(\varphi_{gate} - \varphi_{graphene}) + e\varphi_{graphene} + \Delta W.fn$$

The charge neutrality can be given by,

$$\begin{split} \varphi_{gate} - \varphi_{graphene} &= \frac{Q_m}{C_{ox}} \\ Q_m + Q_{ox} &= Q_{graphene} \\ eV_G &= \frac{e(Q_{graphene} - Q_{ox})}{C_{ox}} + e\varphi_{graphene} + \Delta W.fn \end{split}$$

Where Q_m – charge on the gate

 Q_{ox} – charge on the oxide

 $Q_{graphene}$ – charge on the graphene

 $\Delta W. fn$ - work function difference between gate and graphene.

At V_G=V_{NP}

$$eV_{NP} = \frac{e(Q_{ox})}{C_{ox}} + \Delta W.fn$$
$$e(V_G - V_{NP}) = \frac{e(Q_{graphene} - (Q_{ox} - Q_{ox}(0)))}{C_{ox}} + e\varphi_{graphene}$$

Or,

$$e(V_G - V_{NP}) = \frac{eQ_{graphene}}{C_{ox}} + \frac{eC_{it}\varphi_{graphene}}{C_{ox}} + e\varphi_{graphene}$$

Where C_{it} is defined as the interface trap capacitance.

Using,

$$Q_{ox}(\varphi_{graphene}) - Q(0) = C_{it} \cdot \varphi_{graphene}$$

The total capacitance is therefore obtained as,

$$C_{G} = \frac{dQ_{m}}{dV_{G}} = \frac{d(Q_{graphene} - Q_{ox})/dE}{dV_{G}/dE}$$

From

$$\frac{edV_G}{d\varphi_{graphene}} = 1 + \frac{C_{it}(E_F) + C_q(E_F)}{C_{ox}}$$

$$C_G = \left(\frac{1}{C_{ox}} + \frac{1}{C_q + C_{ii}}\right)^{-1}$$

Then,

$$C_{ox}\left(\frac{edV_G}{d\varphi_{graphene}}-1\right) = C_{it}(E_F) + C_q(E_F)$$

And also using Berglund integral [],

$$\varphi_{graphene} = \int_{V_{np}}^{V_G} \left(1 - \frac{C_G^{LF}}{C_{ox}} \right) dV_G$$

The above equation can be used to evaluate the surface potential with top-gate bias.