Design of a Baseband Section for LTE-Advanced Mobile Communication

By

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Abstract

In the upcoming 4G era, wireless communication systems are required to sustain the ever-increasing data-rate, which should go up to several hundred Mbps or even 1Gbps, as well as to support more flexibility and intelligence. Wireless standards such as LTE (long term evolution) and LTE-A (LTE-Advanced) have been developed and standardized. To achieve the required data-rate, several techniques will be employed, i.e. multiple antenna, carrier aggregation (CA) and relaying, where bandwidth will go up to 100MHz. Consequently, the analog baseband section should support variable channel bandwidths covering all the channels in the LTE-A.

In this thesis, a flexible G_m-C channel filter with variable bandwidth changing from 0.7MHz to 50MHz is designed, which can be used in the future reconfigurable radio. Main specifications include high linearity, low input referred noise (IRN), low power consumption, and low chip area. This design is implemented using UMC 130nm technology, and zero-IF receiver structure is used as the test-bench. Simulation results show that the filter has an IRN of 28.76 μ V (at 50MHz) and IIP3 of approximate 13dBm (measured at the middle of the filter bandwidth). With the supply voltage of 1.2V, this filter consumes the power of 0.847mW. Finally, layout shows that this filter has a chip size of 0.38mm×0.3mm.

Acknowledgment

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Chapter 1
Introduction

Living in a wireless-centric world, we have been enjoying the convenience of wireless telecommunication thanks to the rapid development of wireless and silicon IC technologies. The presence of the mobile phone, which has evolved from early bulky communicators suffered from high power consumption and low data-rate, to the present mobiles equipped with multimedia capabilities integrated on one single chip, has greatly shortened the distance between people and is becoming an indispensable tool in our daily lives. Now, we are on the way to the fourth generation (4G) communication era [1, 2], in which, the mobiles can support more aggressive performance with low power consumption and low cost. The latest wireless standards, i.e., long term evolution (LTE) [3] and LTE-Advanced (LTE-A) [4], are proposed and frozen for the coming 4G mobile systems, which aims to supply a seamless roaming across existing heterogeneous networks as well as high data-rate. Since 4G is a collection of existing wireless standards, the software-defined radio (SDR) technique has been proposed for 4G realization [5, 6].

1.1 Motivation

Since the first generation (1G) wireless communication system was launched in 1976 in Japan [8], wireless communication has changed the way we live our lives and interact with our relatives and friends. GSM (2G), UMTS/WCDMA (3G) and beyond (3G+) wireless systems were developed to satisfy ever-increasing data-rate requirements. As shown in Fig. 1.1, which gives us an overview of wireless standards evolution, the data-rate has been increased from below 10 kbps (1G) to 100 Mbps (3G+), while in the upcoming 4G systems, the data-rate is required to go up to 1 Gbps.

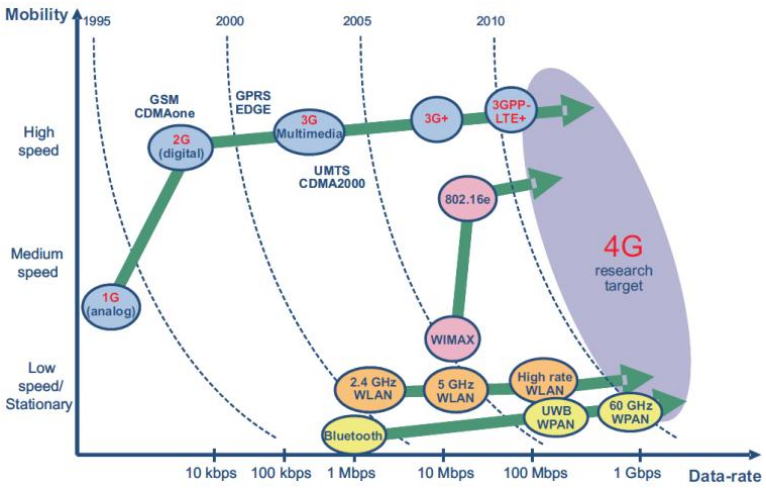


Figure 1.1: Wireless standards evolution versus data-rate [7]

Since data-rate or channel capacity is proportional to the channel bandwidth, a large increase in the effective bandwidth is required in the 4G systems.

In addition to the insatiable demand for large data-rates, multimedia capabilities have been improved to provide the aggressive performance, as shown in Fig. 2. The upcoming 4G technology also requires mobile terminals to support more flexibility (multiband/multimode connectivity) and intelligence (offer users the best quality of experience in heterogeneous environment).

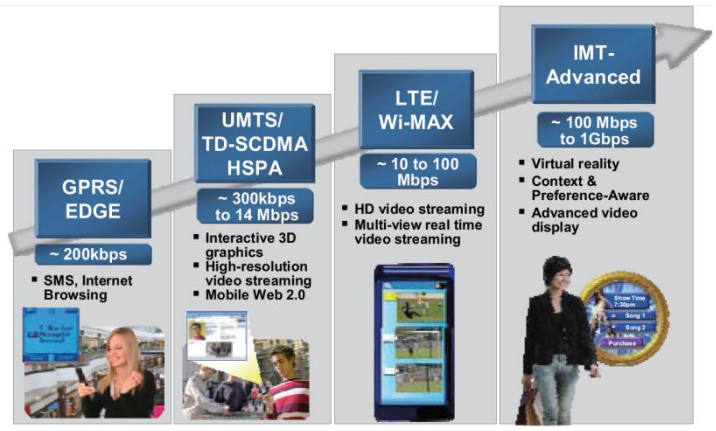


Figure 1.2: Wireless application evolution over wireless generations [2].

In order to standardize 4G systems, the LTE-A standard has been developed [4]. According to this standard, data rates up to several hundred Mbps or even 1Gbps should be supported. To achieve this, several techniques will be utilized, of which the

most visible to the analog/RF part of a 4G smartphone will be the utilization of multi-antennas and signal paths in parallel, and the use of bandwidths up to 100MHz in each path. Therefore, we have to design a corresponding analog baseband section which can sustain such a high bandwidth to achieve the anticipated performance.

1.2 4G Wireless standards: LTE and LTE-Advanced

Although the third-generation mobile communication system has supplied us with much better services than 2G system has done, e.g., wider bandwidth and multimedia service, the conflict between the ever-increasing number of mobile users and limited bandwidth resources drives many countries and organizations to exploit the next generation systems (4G), such as China Communication Standardization Association (CCSA) and ITU (International Telecommunication Union). Defined by ITU's Radio-communication sector (ITU-R), a 4G terminal should accommodate the following objectives [8]:

- Data-rate of 1Gb/s and 100 Mb/s for stationary and high mobility
- Flexible channel bandwidth from 5 MHz to 20 MHz, optionally up to 40 MHz
- Smooth handoff and seamless connectivity and global roaming
- High Quality of Service (QoS)
- An all-IP (internet protocol) packet switched network with IP based femtocells
- Interoperability with existing wireless standards

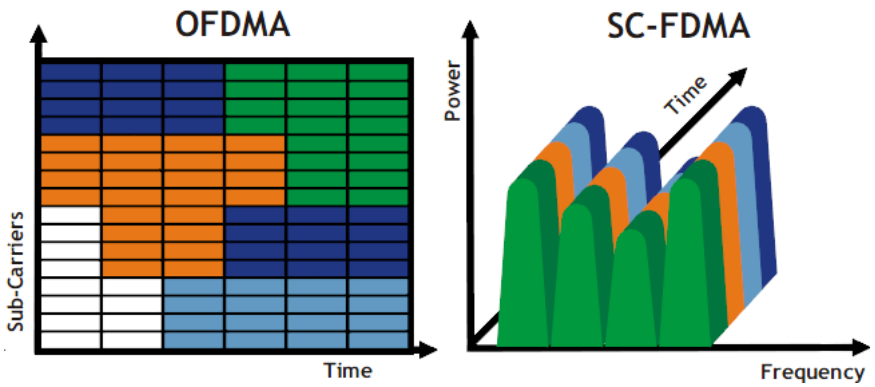
Establishing 4G systems from existing developed wireless systems is more feasible than developing new ones. Currently, there are just two candidate technologies for 4G systems: 3GPP LTE-Advanced and IEEE 802.16m. Industry has adopted to LTE technology as the underpinning of 4G systems, so we will focus on the LTE technology and its evolution LTE-A in the following section, which is the backbone of the coming 4G system.

1.2.1 LTE

LTE is an improvement to the current universal mobile telecommunications system (UMTS) developed by the third generation partnership project (3GPP) [3]. It is designed to carry high-speed data as well as support high-capacity voice traffic. It was standardized in the form of release 8 of the 3GPP evolution. LTE is classified as a 4G technology although it does not meet all the requirements for 4G. A variety of techniques are utilized in the LTE systems [9]: multicarrier technology, multiple antenna technology and packet-switched only network. We will briefly discuss the first two techniques since they are more related to the thesis.

A. Multicarrier technology

3GPP prescribes orthogonal frequency division multiple access (OFDMA) for downlink (DL) transmission and single-carrier frequency division multiple access (SC-FDMA) for the uplink (UL) in order to increase the mobile terminal power efficiency, as shown in Figure 1.3. Modulation schemes for the data transmission can be QPSK, 16QAM and 64QAM (only supported by the user category 5 for the uplink) for the uplink and downlink [9].



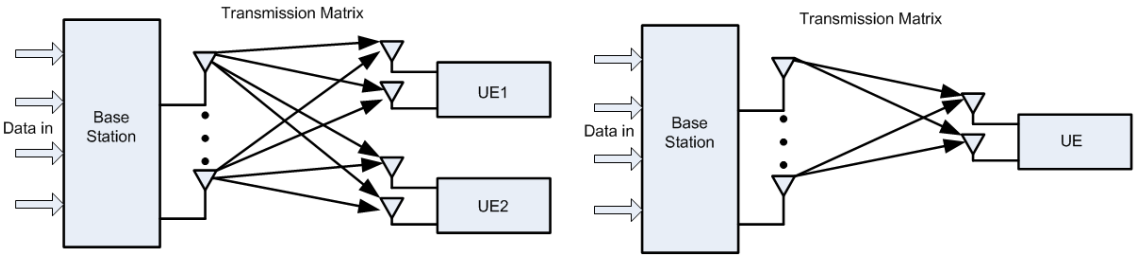
(a) (b)

Figure 1.3: LTE (a) DL and (b) UL multiple access schemes (each color stands for one user) [10].

B. Multiple antenna technology

To improve data-rate and spectral efficiency, LTE employs multiple input multiple output (MIMO) technology. As the name suggests, more than one antenna is used in

the transmitter and in the receiver. One direct benefit is that multipath interference is reduced, resulting in high data throughput. Figure 1.4 presents two applications of the MIMO technique.



(a) (b)

Figure 1.4: MIMO system diagrams of (a) Multi-User (b) Single User [9].

In table 1.1 the key parameters of the LTE (release 8) are summarized.

Table 1.1: LTE release 8 key parameters [3]

LTE release 8		
Access scheme	DL	OFDMA
	UL	SC-FDMA
Scalable BW [MHz]	1.4/3/5/10/20	
Modulation	QPSK/16QAM/64QAM	
Duplexing	FDD/TDD	
Spatial multiplexing	Single layer for UL Up to 4 layers for DL MU-MIMO support	

* assume 4×4 MIMO

1.2.2 LTE-A

LTE should be considered as the pre-4G rather than 4G, since it cannot fulfill the data-rate requirement of 4G. Table 1.2 illustrates us the data-rates and spectra efficiency achieved by LTE and LTE-A. Clearly, LTE-A [11] can fulfill the requirements of 4G.

Table 1.2: Data-rates comparison [12]

		LTE	LTE-A	IMT-A (4G)
Peak data-rate	DL	300 Mb/s	1Gb/s	Stationary: 1Gb/s
	UL	75 Mb/s	500 Mb/s	high mobility: 100Mb/s
Spectra efficiency [bps/Hz]	DL	15	30	15
	UL	3.75	15	6.75

Compared with LTE, new technologies have been exploited for LTE-A [12]: carrier aggregation (CA), enhanced multi-antenna transmission, coordinated multiple point transmission and reception (CoMP) and relaying. We will pay attention to the carrier aggregation technique, which is used for bandwidth extension and is closely related to our design. For more details about the LTE-A, please refer to [13].

To achieve a 4G system's peak data-rate target, it is necessary to extend the transmission bandwidth used in LTE. The proposed technique is termed carrier aggregation or channel aggregation, which means two or more contiguous or non-contiguous carriers, can be aggregated into one transmission channel. For instance, Fig 1.5(a) presents a transmission channel of 100MHz obtained by five contiguous channels in LTE release 8, while Fig. 1.5(b) shows the non-contiguous approach.

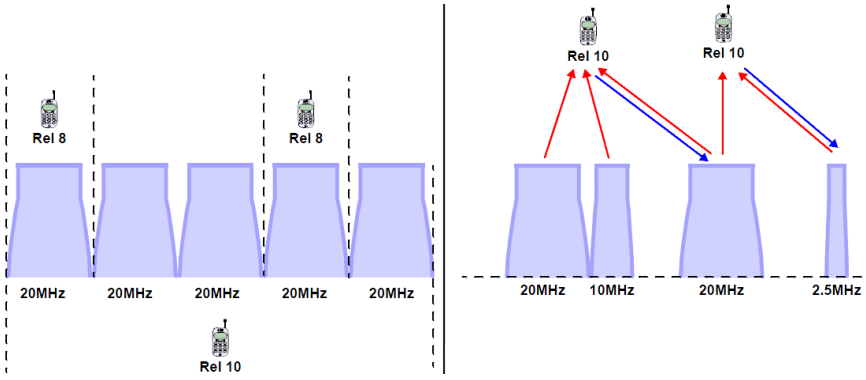


Figure 1.5: (a) Contiguous and (b) non-contiguous carrier aggregation [14]

1.3 Software defined radio

A software defined radio (SDR) system is defined as a radio in which some or all of the physical layer functions are defined in software [15]. It is a reconfigurable system use a collection of hardware and software technologies. SDR enabled devices and equipment be dynamically programmed to reconfigure their characteristics. As a result, the network can employ any standard, any frequency band and any channel bandwidth, which would support conduction to the 4G era. If succeed, it would become the dominant technology in wireless communications.

1.4 Design challenge and objectives

In the direct conversion (zero-IF) transceiver, the analog baseband section is responsible for adjacent channel selectivity, anti-aliasing and dynamic range maximization. A channel filter with low input referred noise (IRN) and high linearity is important for the performance of the whole RF front-end. The subject of this thesis is to design a baseband channel filter that can be used as part of a LTE-A system. It will be required to achieve the same linearity and noise performance as is needed in current-generation phones, but now combined with a very high bandwidth.

Design objectives in this work are: 1) design of a low pass filter with variable bandwidth (0.7MHz~50MHz) to cover the bandwidth range of LTE-Advanced, 2) a channel filter with high in-channel and out-of-channel linearity : at least 20 dBm at the middle of the filter bandwidth and blockers attenuation of 10dB in the adjacent channels), 3) a channel filter with low IRN, i.e., input noise density of 2nV/$\sqrt{}$Hz, 4) low power consumption of a few mW, 5) small chip area (defined by maximum capacitor value of 50pF).

However, trade-offs exist between design parameter such as linearity, noise and power consumption [16]. The design challenge in this work is realizing the high linearity and low IRN and low power. For instance, linearity benefits from a large overdrive voltage, however, this would result in high power consumption.

1.5 Thesis organization

This work is a part of the research on reconfigurable radio front-ends which would be used in SDR systems in the future. This thesis consists of 6 chapters and is organized as follows.

In the first two sections of chapter 2, some basic theories about the zero-IF RF front-end and analog baseband section, including the LNA, mixer and channel filter are

provided. Among the four different types of filters (i.e., active-RC filter, MOS-C filter, Gm-C filter and active-R-Gm-C filter), the *Gm-C* filter is selected for our design due to its advantage of high bandwidth. In the third section, we briefly review the filter design procedure, active inductor and resistor realization techniques, and transconductance linearization technique utilized in the G_m-*C* filter.

In chapter 3, two published G_m-*C* low pass filters are investigated. These filters are distinguished by their working regions (voltage domain and current domain). A dedicated section (3.2 and 3.3) is given to these two modes. Circuit simulation is done using UMC's 130nm technology. After analyzing each filter's advantages and drawbacks, the voltage mode LPF is selected due to its low noise as well as good linearity performance. In the fourth section, different RF front-ends for the voltage-mode filter and current-mode filter are discussed.

A tunable G_m-*C* filter is realized in chapter 4. According to the G_m-*C* filter's feature, one tuning algorithm is proposed in the first section. Then, according to the tuning algorithm, a flexible transconductance G_m and capacitor array are implemented using MOS switches in the second section. The impact of the finite on resistance of the MOS switch on the filter performance is also discussed. Finally, to cope with low out-of-channel linearity, a zero-IF front-end with passive mixer loaded by a tunable capacitor is utilized to attenuate the out-of-channel blockers.

In chapter 5, the noise figure simulation results of the total receiver are presented in the first section. Then, layout and post simulation result of the flexible filter are given, in which the impacts of processing corners, supply voltage variation and temperature on the filter bandwidth are discussed.

Finally, general conclusions are drawn in chapter 6. Some suggestions for improving the filter's performance are proposed for future work.

Chapter 2
Background

This chapter focuses on the theoretical background required for better understand the following chapters. In the first section, we briefly review some basics about the zero-IF RF front-end, analog baseband section and channel filter. Then, emphasis is put on the G_m-C filter design, in which the filter design procedure, passive component realization, and transconductance linearization technique are discussed.

2.1 RF front-end basics

The RF front-end plays an important role in one mobile terminal. Basics about the zero-IF receiver, including its LNA, mixer components are reviewed in this section.

2.1.1 Zero-IF receiver

There are several architectural options available as far as receiver front-end design is concerned, i.e., heterodyne receivers, zero-IF receivers, digital low-IF receivers, bandpass sampling receivers and direct RF sampling receivers [16, 17]. These receivers all have the potential to be chosen as the candidates of the SDR systems based on their own features. However, to simultaneously achieve multi-mode and multi-standard capabilities with cost and power savings, the zero-IF receiver wins out thanks to its overwhelming advantage of simplicity, although several problems also exist.

Fig. 2.1 shows us the common architecture of the zero-IF receivers. In this architecture, the received RF signal is directly translated to baseband, which is accomplished by setting the local oscillator (LO) frequency equal to the RF signal. Therefore, no intermediate frequency (IF) stages are needed, making this architecture quite suitable for low power, a high level of integration as well as better flexibility to suit various applications. In addition, there is no image rejection problem [16] as appears in

heterodyne receivers, which relaxes the requirements for extra filters (e.g., SAW filter), and a low pass filter in the baseband is critical for channel selectivity.

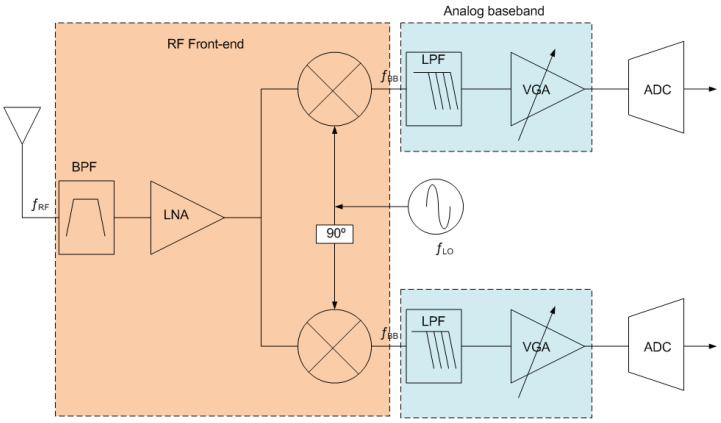


Figure 2.1: Zero-IF receiver architecture

On the other hand, several problems exist in this topology, i.e., DC offset, even-order distortion, I/Q mismatch, flicker noise and LO-leakage. Solutions have been developed to cope with these problems. The DC offset problem can be alleviating by using DC-free coding, and differential LNAs and mixers suppress the even-order distortion [16].

In conclusion, simplicity gives zero-IF receiver flexibility and the potential to reduce power, cost and area, making it is a suitable candidate for SDR systems. However, due to its simplicity and the flexibility requirement, more challenges are imposed on the RF and baseband section design: high performance LNAs, high linearity mixers, flexible channel filters and state of the art ADCs. In later chapters, we will use this architecture as our test bench for design and simulation.

2.1.2 Receiver sensitivity and linearity

Sensitivity is defined as the minimum signal level that can be detected by the RF front-end with acceptable signal-to-noise (SNR) ratio [16], which usually is determined by the receiver noise figure (NF). The minimum input power can be estimated using this equation

$$P_{\text{in,min}} = -174dBm/Hz + \text{NF} + 10\text{logB} + \text{SNR}_{\text{min}}, \qquad (2.1)$$

where B is the channel bandwidth. In a radio receiver, the noise figure is calculated

according to Friis' equation (2.2)

$$NF_{tot} = \mathrm{NF}_1 + \frac{\mathrm{NF}_2 - 1}{\mathrm{G}_1} + \frac{\mathrm{NF}_3 - 1}{\mathrm{G}_1\mathrm{G}_2} + \frac{\mathrm{NF}_4 - 1}{\mathrm{G}_1\mathrm{G}_2\mathrm{G}_3}\cdots, \tag{2.2}$$

where NF_i and G_i (i=1,2,3⋯) stand for the noise figure and gain of each stage respectively. It denotes that the NF of the first stage of the receiver dominants the total noise figure if the gain of the first stage is sufficiently large. Therefore, as the first stage of the RF front-end, the LNA is required to have a low noise figure as well as high gain.

Receiver linearity is measured using the two-tone test in terms of input third-order intercept point (IIP3) and denoted by

$$\frac{1}{\mathrm{IIP3_{tot}}} = \frac{1}{\mathrm{IIP3}_1} + \frac{\mathrm{G}_1}{\mathrm{IIP3}_2} + \frac{\mathrm{G}_1\mathrm{G}_2}{\mathrm{IIP3}_3} + \frac{\mathrm{G}_1\mathrm{G}_2\mathrm{G}_3}{\mathrm{IIP3}_4}\cdots, \tag{2.3}$$

where $\mathrm{IIP3}_i$ and G_i (i=1,2,3⋯) represent each stage's noise figure and gain, respectively. Equation 2.3 predicts that receiver linearity is mainly determined by the stages after the LNA due to its gain, i.e., the mixer and channel filter linearity. Therefore, a high linearity mixer and filter are desired in the receiver.

2.1.3 LNA and mixer basics

When designing a LNA, apart from the high gain and low noise figure requirements described above, input matching is another important specification. Theoretically, impedance matching and noise matching are required simultaneously for maximum power delivery and low noise. In reality, the LNA input impedance is designed so that the input return loss (S11) is less than 10dB with an acceptable noise figure.

Linearity and noise are two main specifications when designing a mixer. An active mixer has lower noise due to its gain; however, it suffers from lower linearity compared with the passive mixer. In the zero-IF receiver, where flicker noise is important, the passive mixer is popular due to its zero DC biasing current as well as its better linearity.

2.2 Analog baseband section basics

In the zero-IF receiver, the analog baseband section normally consists of a LPF and VGA in series. It plays an important role in channel selectivity, anti-aliasing filtering and dynamic range maximization. A typical baseband section permutation is illustrated in Figure 2.2, in which signals are amplified by the VGA after its blockers are firstly filtered by a LPF. The presence of the VGA block keeps the signal level constant no matter how the signal changes, in order to relax the requirements (i.e., resolution, dynamic range) on the following ADC. However, if a state-of-the-art ADC is employed, such as high performance ΣΔ, the VGA can be removed to reduce power consumption.

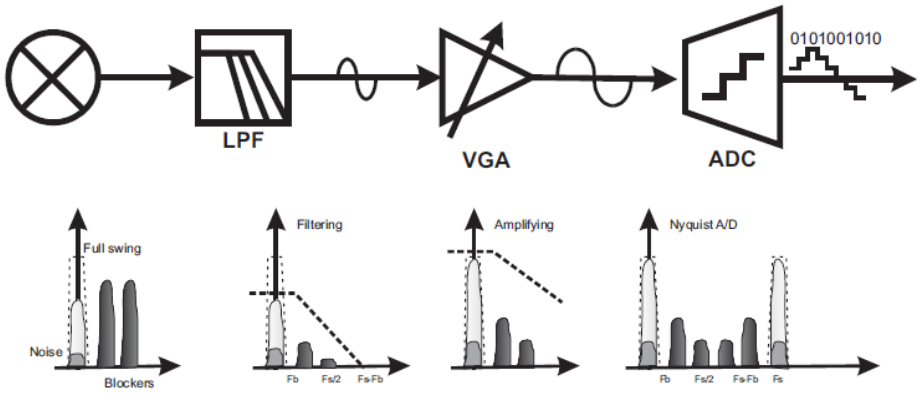


Figure 2.2: Signal processing in the analog baseband section [18]

Careful design of each baseband block is required because: (1) noise figure and linearity in the baseband circuit could deteriorate the whole performance of the receiver, and (2) majority of the chip area and power is consumed by the baseband components. Since the objective of this thesis is to design a flexible and high performance LPF, we will focus on its analysis and implementation in this section.

2.2.1 Channel filter specifications

In baseband section, the input spectrum includes interferers from adjacent channels, in-band, and out-of-band blockers in addition to the wanted signal. Usually, power level of these interferers is much higher (around 20dBm) compared to the signal. For this reason, the LPF should possess high in-band dynamic range (DR), out-of-band linearity

and anti-aliasing filtering.

In-band dynamic range of the filter is determined by its input referred noise (IRN) and acceptable maximum input signal level. It denotes the filter's ability of signal handling with required SNR. In wideband systems, where thermal noise is dominant, IRN is calculated by integrating the thermal noise in the whole band and then dividing the result by the filter gain. With signal power increases, distortion at the filter output becomes worse and worse. The upper limit occurs when the minimum SNR is achieved. If an increase in dynamic range is desired, we have to lower the noise floor or increase the filter in-channel linearity. The two-tone test to measure the filter is in-channel linearity is shown in Fig. 2.3(a).

Excellent out-of-channel linearity is another important requirement to the channel filter; otherwise intermodulation (IM) of two out-of-channel signals would fall into the wanted signal band and corrupt the SNR. Sufficient attenuation of the out-of-channel signals can lighten the burden, which usually is done by using a higher order filter. The out-of-channel linearity measurement is shown in Fig. 2.3(b).

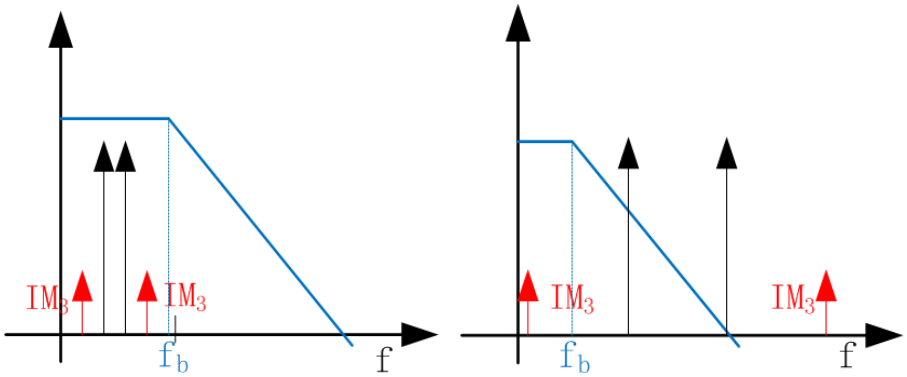


Figure 2.3: (a) in-channel linearity and (b) out-of-channel linearity two-tone test.

Anti-aliasing filtering is illustrated in Fig. 2.4. The channel filter should have the ability of limiting the signal bandwidth to avoid the aliasing problem caused by the folding back of out-of-channel noise and interferers. In this figure, passband and stopband are denoted by F_b and F_s-F_b, respectively, and F_s is the sampling frequency used in ADC.

When the input spectrum is limited below F_s-F_b, no aliasing into the signal band occurs. Therefore, the channel filter should meet the desired attenuation in the stopband. Attenuation of the blockers in transition band (between passband and stopband) is also expected in order not to saturate the subsequent stages after amplification by VGAs.

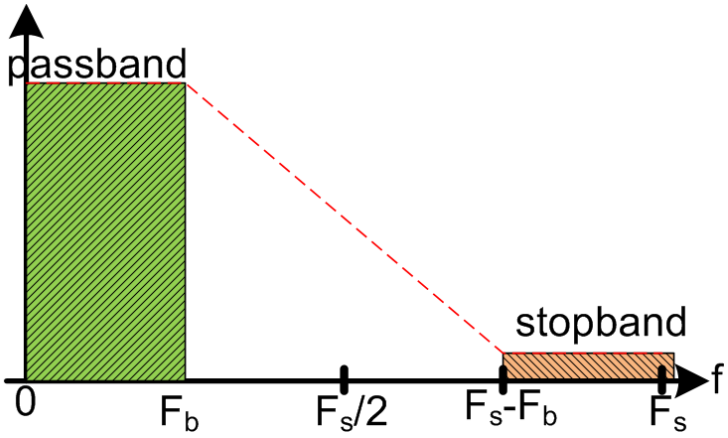


Figure 2.4: Anti-aliasing filtering

2.2.2 Channel filter architectures

Theoretically, the active filter could be either a switched-capacitor (SC) filter or continuous time (CT) filter depending on system requirements. In a system where high cut-off frequency filters are required, the CT filter is superior to the SC filter which has to use two high frequency non-overlap clock signals, and would consume too much power [19]. Therefore in our wideband system, we focus mainly on the implementation of CT filters.

Fig. 2.5 presents four configurations of continuous time filters [20]. From the linearity point of view, (a), (b) and (d) offer higher linearity owing to their closed feedback loop structures compared to the open loop structure (c). However, this advantage does not exist anymore at high frequency due to the decrease of loop gain. From the tuning accuracy perspective, topology (b) is the simplest one since it can be tuned by changing the control voltage V_b, instead of using resistor or capacitor banks or extra tuning circuits as in other three topologies. However, if filters with high frequency and low power consumption are desired, as is the case of the SDR, topology (c) would be the

best choice if linearization techniques also can be used.

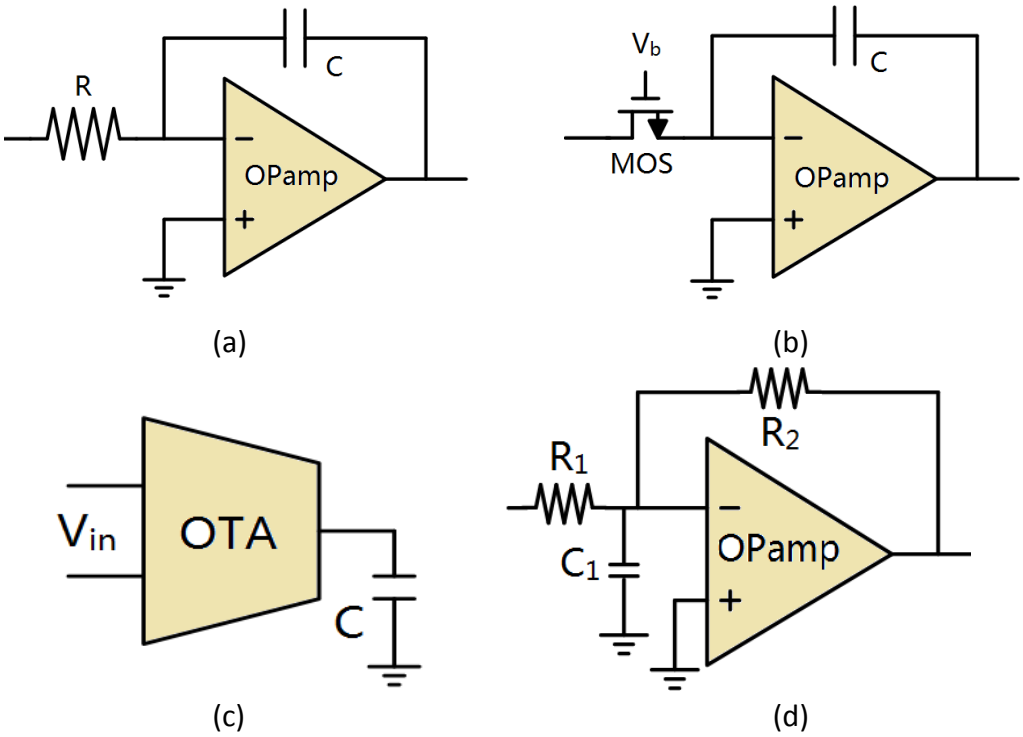


Figure 2.5: Four types of continuous time active filter (a) active-RC filter (b) MOS-C filter (c) g_m-C filter (d) active g_m-RC filter

To sum up, the g_m-C filter is the best candidate for channel filtering although its linearity is not good enough. Low power consumption and wide bandwidth are its main advantages compared to other types of filters. That is why designing a g_m-C filter is the objective of this thesis.

2.3 Gm-C low-pass filter design basics

In this section, filter design basics of filter design methodology, passive component realization and Gm linearization techniques are briefly discussed.

2.3.1 Filter design methodology

As described in [18], there are a few steps utilized to design a filter: filter mask estimation, filter type selection and filter parameter determination.

In the presence of the adjacent channels, the channel filter should have the ability to pick up the signal from the assigned channel with high accuracy. The system adjacent channel selectivity (ACS) specification defines the minimum attenuation demanded at the frequency offset from the assigned channel, thereby defining the filter mask. However, ACS is usually achieved by the analog filter (channel filter) and digital filter together, and the selectivity for the analog filter is assigned given the filter power and ADC performance.

Having known the filter mask, we define a polynomial approximation whose frequency response fits the mask curve precisely. Generally, there are four types of filters, i.e., Butterworth, Chebeyshev, Bessel and Elliptic, and each type has its own advantages and drawbacks. The most suitable filter is selected according to the system specifications. For instance, a Bessel filter is the best candidate if good phase response is demanded, while Butterworth filter is used for in-channel maximum magnitude flatness in the frequency domain [21, 22].

With the filter mask and the selected filter, the filter parameters such as the order, gain, and cutoff frequency can be determined easily.

2.3.2 Passive component realization

In a typical G_m-C filter, passive components such as the resistor and inductor are barely used. Usually, we can implement them with the assistance of a G_m cell. As can be seen in Fig. 2.6 (a), it is easy to obtain one active resistor of $1/g_m$ when connecting the output node to the minus input node of the g_m cell, as is the case of diode connected MOS transistor. Therefore, we put the emphasis on the active inductor realization.

The on-chip inductor is avoided in integrated circuits nowadays due to its drawbacks such as large chip area consuming and low quality factor. Thus, the active inductor approach has been developed to realize an inductor. The active inductor usually is

realized using general impedance converter (GIC) circuit or gyrator [21]. A gyrator is a component which consists of two transconductors connected back-to-back, and is usually employed to transform a capacitor load into a floating or single-ended inductance when looking into the input node, and vice-versa, as shown in Fig. 2.6(b).

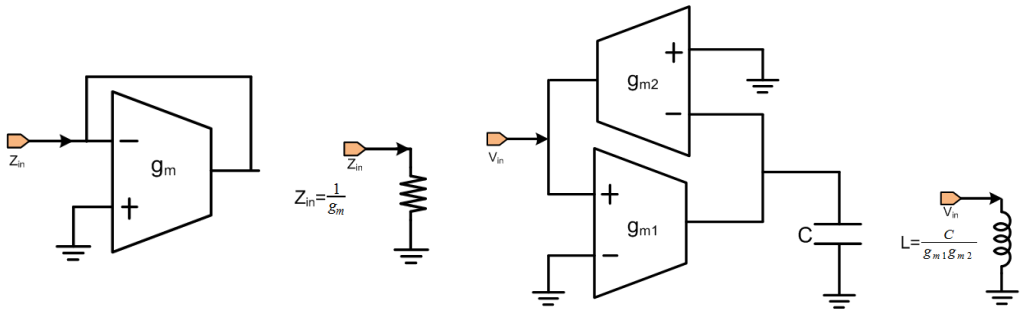


Figure 2.6: Passive components realization of (a) active resistor, (b) active inductance with the assistant of Gm cell

There are various approaches can be used to realize the active inductor based on gyrator theory [23]. We just discuss one approach utilized in our design, as shown in Fig. 2.7(a).

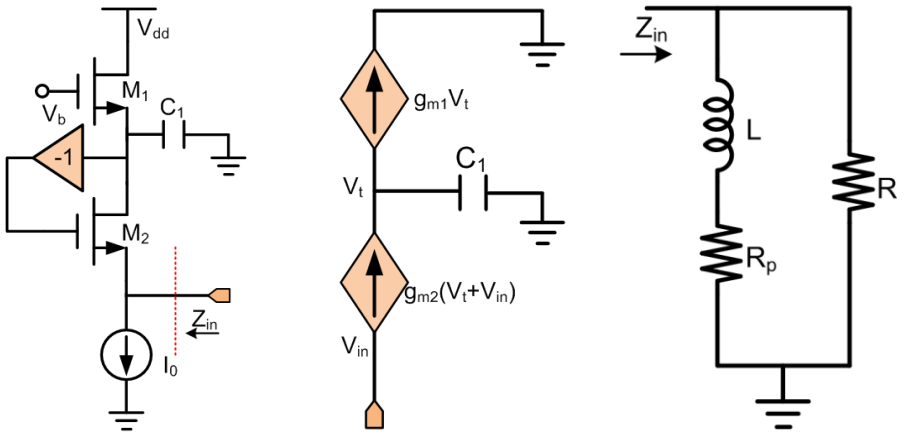


Figure 2.7: (a) active inductor gyrator (b) small-signal model (c) equivalent impedance circuit

$$L = \frac{C_1}{g_{m1}g_{m2}} \tag{2.2}$$

$$R = \frac{1}{g_{m2}} \tag{2.3}$$

$$R_p = \frac{g_{m1}-g_{m2}}{g_{m2}^2} \tag{2.4}$$

According to the small signal model of Fig. 2.7(b), we can calculate the equivalent input impedance versus frequency. Each value of the components in Fig. 2.7(c) is given in equations (2.2-2.4). With equal g_m in the two transistors, a parallel equivalent circuit analyzing of inductor $L=C_1/g2m$ with resistor $R=1/g_m$ is realized. Note that the minus sign can be realized by a cross-coupled differential pair.

2.3.3 *Gm* linearization techniques

A differential pair is the simplest transconductor, whose distortion comes from the odd-terms due to its odd-symmetric transfer function. Under the small input signal condition, third order distortion HD_3 dominants given by (2.5)

$$HD_3 = \frac{V_{in}^2}{32(V_{GS}-V_{TH})^2} \ , \tag{2.5}$$

where V_{in} is the differential input signal amplitude. Therefore, one way to improve the linearity is to increase the overdrive voltage V_{ov} ($V_{ov}=V_{GS}-V_{TH}$) of the differential pair. However, this approach is not popular due to higher power consumption and limited linearity improvement. Several approaches [19, 24] have been developed to improve the linearity of the transconductance G_m.

Local feedback is one popular technique to achieve better linearity. One practical circuit is shown in Fig. 2.8 with source degeneration resistor. The third order harmonic is suppressed due to g_m linearization

$$HD_3^{'} = \frac{HD_3}{(1+g_m R_s)^2} \tag{2.6}$$

$$g_m^{'} = \frac{g_m}{1+g_m R_s}, \tag{2.7}$$

where Rs is the degeneration resistor. However, the disadvantage is the parasitic capacitance of the current source may degrade the filter's performance at high frequency. Moreover, noise is introduced by the degeneration resistor. In order to make a tunable transconductor, the resistor can be replaced with MOS transistor working in the linear region.

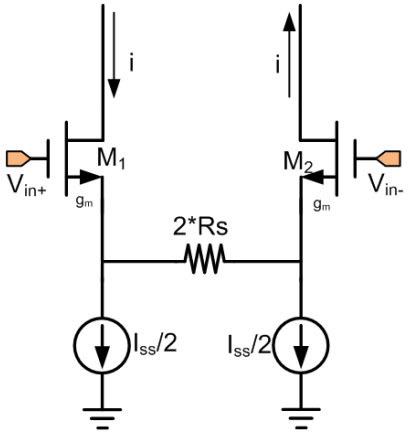


Figure 2.8: Source degeneration technique for g_m linearization

Parallel differential pair technique is another one effective way of improving linearity, as shown in Fig. 2.9. Theory behind is that this circuit has a slower slope in I/V curve than that of the single differential pair. Best results (reduced distortion and extent input range) are achieved when the transistor ratio in one pair is 5:1 [24]. However, good performance is achieved at the expensive of transconductance. Moreover, power consumption is higher compared with the single differential pair.

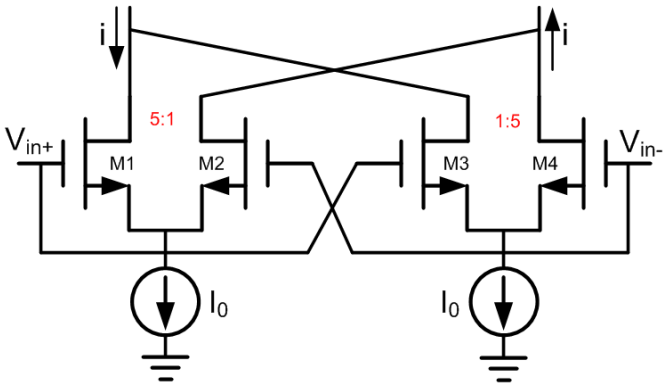


Figure 2.9: Parallel differential pair for g_m linearization

Apart from the linearization techniques mentioned above, there are some other attractive ways which take the advantages of the inherent linear behavior of the invertor or the biased in the linear region differential pair. The Nauta transconductor shown in Fig. 2.10 is such a circuit employing the invertors. High frequency behavior is the main advantages since there are no internal nodes. In addition, it is suitable for low supply voltage application. However, common mode feedback circuit is desired.

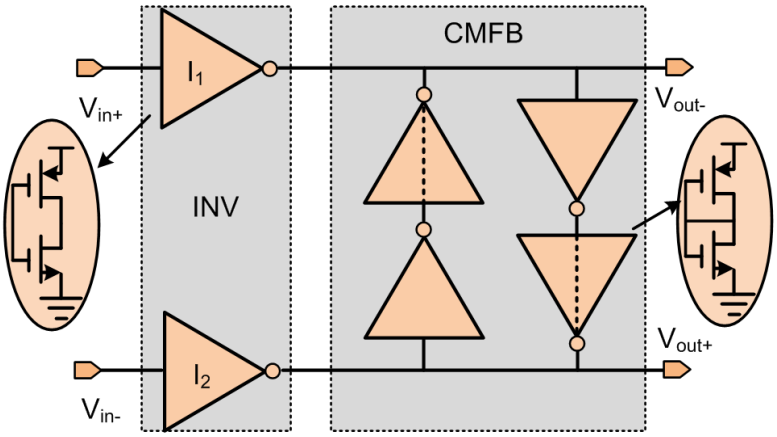


Figure 2.10: The Nauta transconductor

2.4 Summary

In this chapter, we briefly reviewed the theory background about the zero-IF receiver front-end and the analog baseband section, including their sub-blocks such as LNA, mixer and channel filter. Then, based on the G_m-C type filter, we discussed the filter design procedure, passive components realization and the transconductance linearization techniques. In the following chapters, our objective is to design and test a G_m-C filter based on this discussion.

Chapter 3

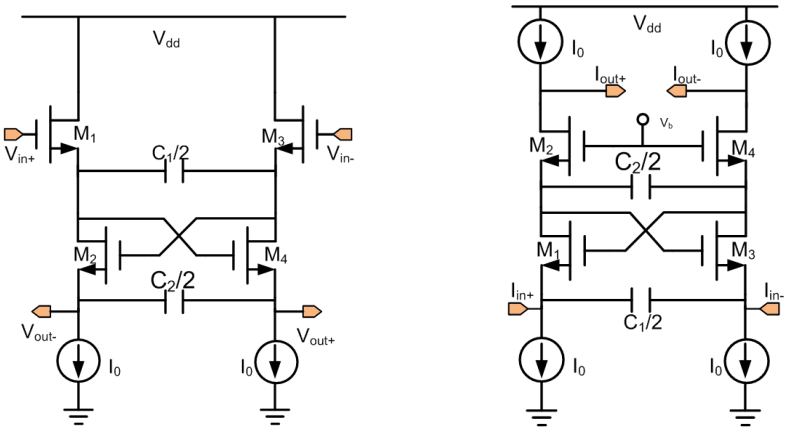
Gm-C Biquad Design and Simulation Results

A biquad, defined as one circuit who can realize the biquadratic transfer function, is very useful because higher order filter systems may be realized by simply cascading them [21]. Therefore, our objective in this chapter is to investigate the way of designing a simple biquad with good performance, i.e., in-channel linearity of 20dBm, power consumption of a few mW, input referred noise density of 2nV/√Hz, and dynamic range of at least 60dB.

This chapter starts with the analysis of two published G_m-*C* biquads based on the *RLC* networks, which can be classified into voltage mode and current mode. In the following two sections, we discuss the advantages and drawbacks for each type, and simulations are done in the UMC 130nm technology. Then, different zero-IF structures for these two filters are presented. Conclusions are drawn in the last section.

3.1 Two G_m-*C* biquads

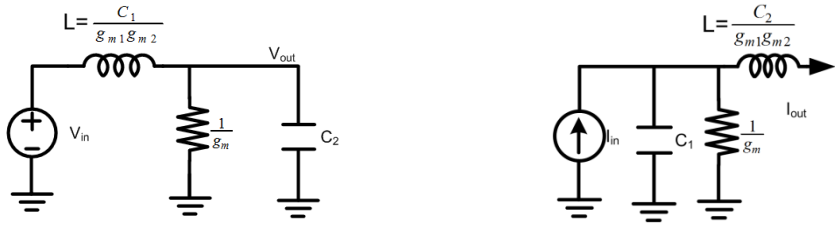
As described in last chapter, the classical G_m-*C* filter suffers from low linearity due to its open loop structure. Therefore, efforts have been made to improve the linearity of the transconductance [27-29]. However, these posted structures either consume high power (several mW) or require high supply voltage (greater than 1.8V), which prevents them from use in a low power application such as the LTE-A system. In this section, we discuss two novel structures published in [30-31], as shown in Fig. 3.1.



(a) (b)

Figure 3.1: Two types of biquads (a) voltage mode [30], (b) current mode [31] classified by their working regions.

Fig. 3.2 presents Thevenin equivalent circuits corresponding to each circuit in Fig. 3.1. Clearly, the voltage-mode biquad is actually based on the series RLC network while the current-mode biquad is from the parallel RLC network model. The active inductor *L* is realized by way of GIC approach described in chapter 2. We will analyze these two biquads with their advantages and drawbacks in the following sections.



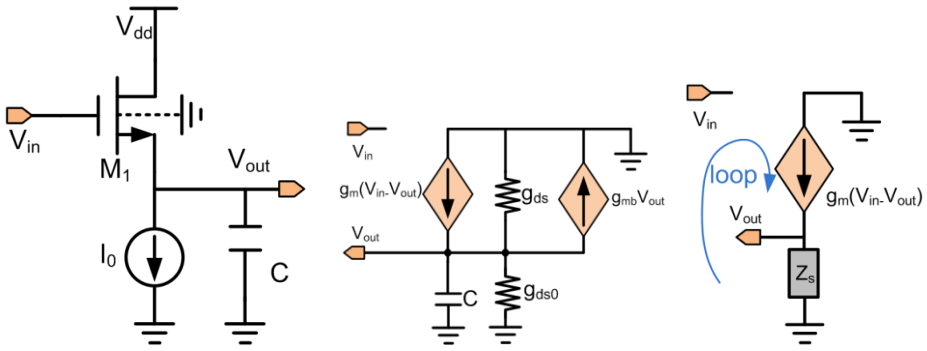
(a) (b)

Figure 3.2: Thevenin equivalent circuits of (a) voltage-mode biquad, (b) current-mode biquad

3.2 Voltage-mode Gm-C filter

As can be seen from Fig. 3.1(a), the voltage-mode G_m-C biquad is based on the source follower (i.e., M_1 and M_3). We will investigate the first-order filter before the biquad, in order to see what benefits we can obtain from the source-follower based structure.

3.2.1 Source-follower based first-order filter



(a) (b) (c)

Figure 3.3: Source-follower based LPF (a) schematic (b) small-signal model (c) loop gain model.

Fig. 3.3 presents the source-follower based first-order low-pass filter with its small-signal models shown in Fig. 3.3(b) and (c). The latter one is used to calculate the loop gain of the source follower.

A. Transfer function

Taking the body effect (g_{mb}) and the channel length modulation effect (g_{ds}) into account, the transfer function of this first-order filter is given in (3.1),

$$H(s) = \frac{g_m}{sC+g_m+g_{mb}+g_{ds}+g_{ds0}}. \tag{3.1}$$

where g_{ds0} is the output conductance of the current source I_0. The filter's pole ω_0 and DC-gain K_{DC} are

$$\omega_0 = \frac{g_m+g_{mb}+g_{ds}+g_{ds0}}{C} \tag{3.2}$$

$$K_{DC} = \frac{g_m}{g_m+g_{mb}+g_{ds}+g_{ds0}}. \tag{3.3}$$

Equation (3.3) shows that the filter gain is always less than 1, even if the body effect and channel modulation effect are negligible, equation (3.2) reveals that g_{mb}, g_{ds} and g_{ds0} together shift the filter pole away from the designed value. Therefore, triple well technology (to cancel the body effect g_{mb}) and longer channel length (to lower g_{ds} since $g_{ds} \propto 1/L$) are expected.

B. Linearity consideration

A source follower is relatively linear thanks to its intrinsic feedback loop formed by M_1

and its load impedance Z_s. According to Fig. 3.3(c), the loop gain *LG* is written as

$$LG = \frac{g_m}{(sC+g_{mb}+g_{ds}+g_{ds0})}. \quad (3.4)$$

In a differential circuit where HD_3 is dominant, HD_3 can be suppressed by a factor equal to the loop gain *LG*:

$$HD_{3,SF} = \frac{HD_3}{(1+LG)^2}. \quad (3.5)$$

Besides, given the same g_m, compared with other G_m-*C* filters which get high linearity by increasing the overdrive voltage, the source follower based filter requires a low overdrive voltage (V_{gs}-V_{th}) thus consumes less power according to (3.6):

$$g_m = \frac{2I_0}{V_{gs}-V_{th}}. \quad (3.6)$$

Low power consumption with high linearity is the main advantage of this filter.

Body effect (g_{mb}) plays an important role in this source follower based filter [24]. In our above calculations, we assume the g_{mb} is linear and can be treated as one conductance. This is true when the amplitude of V_{bs} is small and has a negligible impact on the threshold voltage, Vth. However, in the large signal case, this filter shows severe distortion problem due to the nonlinearity of g_{mb}.

In addition, from (3.4) we can see that *LG* has one pole at low frequency ω_p

$$\omega_p = \frac{g_{mb}+g_{ds}+g_{ds0}}{C} \quad (3.7)$$

compared with (3.2), which means *LG* decreases in the filter bandwidth. Consequently, filter linearity decreases with increasing filter bandwidth, which is one drawback of this filter.

C. Noise

The output noise contributed by the transistor M_1 and current source I_0 is calculated as

$$V_{out,n}^2 = 4kT\gamma(g_m + g_{m0}) \left|\frac{1}{sC+g_m+g_{mb}+g_{ds}+g_{ds0}}\right|^2, \quad (3.8)$$

where k is the Boltzmann constant and T is the absolute temperature, γ is the transistor

channel thermal noise factor. According to (3.8), the output noise has the same pole as of the transfer function. In order to decrease the output noise, we have to make the current source transconductance g_{m0} as small as possible. Meanwhile, high g_m is desired.

From the above analysis we can get a conclusion: the main advantage of the source-follower based filter is its high linearity with low power consumption, which makes this filter very suitable for the channel filter in the baseband.

3.2.2 Source-follower based biquad filter

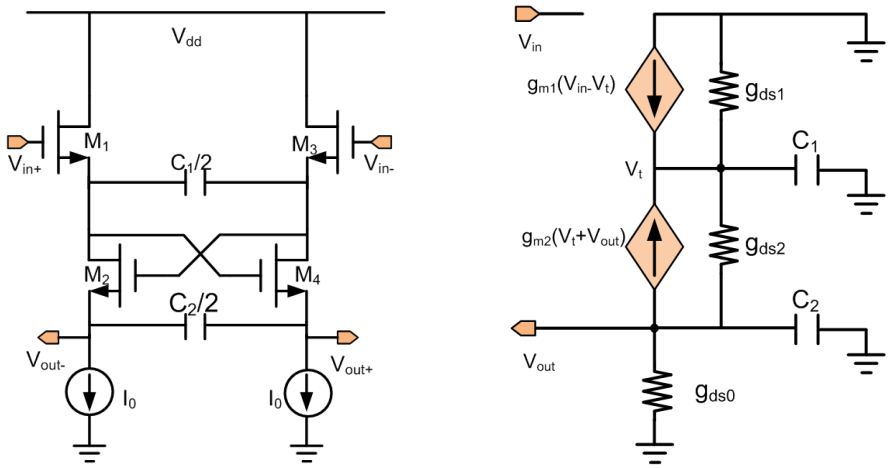


Figure 3.4: Source-follower based biquad (a) filter circuit, (b) its half circuit small-signal model

As a matter of convenience, we redraw the source-follower based biquad here as well as its small-signal model in Fig. 3.4 (b). Analysis in detail is given next.

A. Filter parameters

According to the small signal model Fig. 3.3(b), we can calculate the transfer function assuming g_{ds} is negligible compared with g_m. The transfer function H(s), quality factor Q and the cutoff frequency ω_0 are given by equations (3.9)-(3.11). In the case of equal gm, Q is simply determined by the ratio of C2 to C1.

$$H(s) = \frac{-1}{s^2\frac{C_1C_2}{g_{m1}g_{m2}} + s\left(\frac{C_1-C_2}{g_{m1}} + \frac{C_2}{g_{m2}}\right) + 1} \xrightarrow{g_{m1}=g_{m2}} \frac{-1}{s^2\frac{C_1C_2}{g_m^2} + s\frac{C_1}{g_m} + 1} \tag{3.9}$$

$$Q = \frac{1}{\sqrt{\frac{g_{m2}}{g_{m1}}}\left(\sqrt{\frac{C_1}{C_2}} - \sqrt{\frac{C_2}{C_1}}\right) + \sqrt{\frac{g_{m1}}{g_{m2}}}\sqrt{\frac{C_2}{C_1}}} \xrightarrow{g_{m1}=g_{m2}} \sqrt{\frac{C_2}{C_1}} \tag{3.10}$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \xrightarrow{g_{m1}=g_{m2}} \frac{g_m}{\sqrt{C_1C_2}} \tag{3.11}$$

Note from (3.9), the DC gain is ideally -1. When taking into account the finite output conductance and body effect, the filter will suffer from a few dB loss. The loss can be estimated according to

$$K_{DC} = \left(\frac{g_m}{g_m + g_{mb} + g_{ds} + g_{ds0}}\right)^2 . \tag{3.12}$$

B. Noise performance

There are 6 noise sources in total in the voltage-mode biquad as shown in Figure 3.5. When referred them to the input node, we can obtain the input-referred noise (IRN).

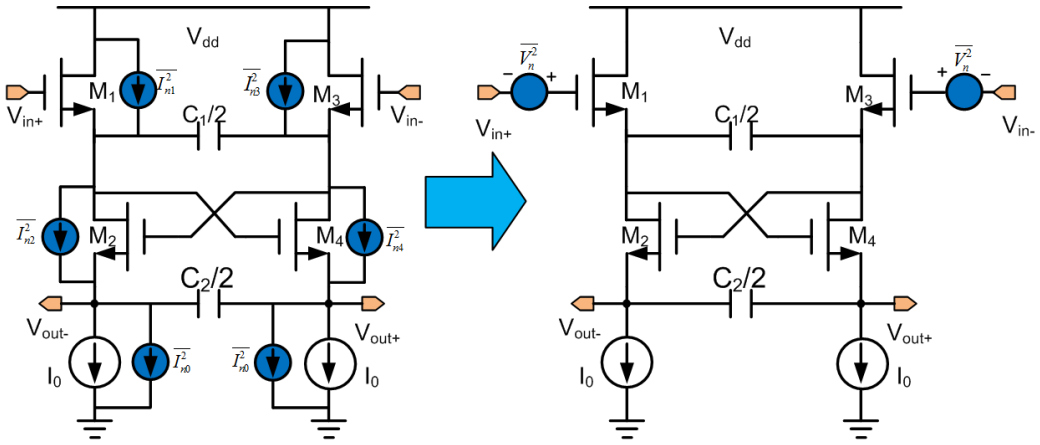


Figure 3.5: (a) noise sources of the biquad and (b) its equivalent input noise.

Equation (3.13) indicates us the total IRN and the responding each contributor (labeled by names) of the biquad.

$$\mathrm{IRN}^2 = 8kT\gamma\left[\underbrace{\frac{1}{g_m}}_{M1,3} + \underbrace{\frac{1}{g_m}\left|1 + j\frac{f}{Qf_0}\right|^2}_{M2,4} + \underbrace{\frac{g_{m0}}{g_m^2}\left|j\frac{f}{Qf_0}\right|^2}_{I_0}\right], \tag{3.13}$$

where Q and f_0 are the quality factor and cutoff frequency, respectively. Flicker noise is omitted here because it is assumed that a large transistor is used. It is obvious from (3.13) that the noise introduced by the current sources I_0 is shaped by high pass

transfer function as well as $M_{2,4}$. Given certain values of bandwidth f_0 and quality factor Q and assuming that g_{m0} equals g_m, we can plot the IRN in different g_m as shown in Fig. 3.6.

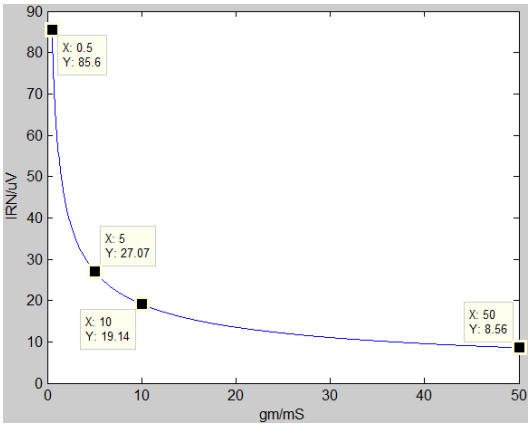


Figure 3.6: Input noise value (integrated from 100 kHz to 50 MHz) versus gm when Q=0.71 and f_0=50MHz.

According to Fig. 3.6, larger transconductance g_m leads to smaller IRN which is what we expect. However, we cannot increase g_m too much, since according to (3.11) g_m is proportional to the square value of the capacitor product. Therefore a large g_m demands a large capacitor, and a trade-off exists between noise and the filter area on-chip.

C. Linearity performance

This filter biquad has good linearity for the following reasons: (1) differential structure cancels out the even-order harmonics and HD_3 is dominant, (2) the intrinsic negative feedback loop of the source follower can suppress harmonics at low frequency, (3) this filter merely operates in the voltage domain and there are no V/I or I/V conversions. However, when the frequency approaches the cut-off frequency, the linearity drops because of the decrease in the loop gain.

A longer channel length is beneficial to the linearity because distortion can also result from transistor conductance variation. However, it cannot be arbitrary large due to the parasitic capacitance of a large area transistor.

D. Stability

Care should be taken of the stability problem due to the positive feedback formed by the cross-coupled differential pair. Breaking the loop at the gates of M2 and M4, we can get the loop gain shown in equation (3.14),

$$\mathrm{LP} = \frac{\frac{g_{ds0}}{gm} + s \cdot \frac{Q}{\omega_0}}{\frac{s^2}{\omega_0^2} + s \cdot \frac{Q+1/Q}{\omega_0} + 1}, \tag{3.14}$$

where g_{ds0} is the current source transconductance. Clearly, it shows a band pass response. Simulation results will be given in following section to check the stability.

E. Filter supply voltage requirement

The minimum supply voltage is estimated in this section. According to Fig. 3.7, assume that the current source has the same overdrive voltage (Vov) as transistors M_1-M_4 and the signal amplitude (differential zero to peak) is V_{swing}. The minimum required supply voltage is,

$$V_{dd,min} = 2V_{ov} + V_{gs} + V_{swing} = 3V_{ov} + V_{th} + V_{swing}. \tag{3.15}$$

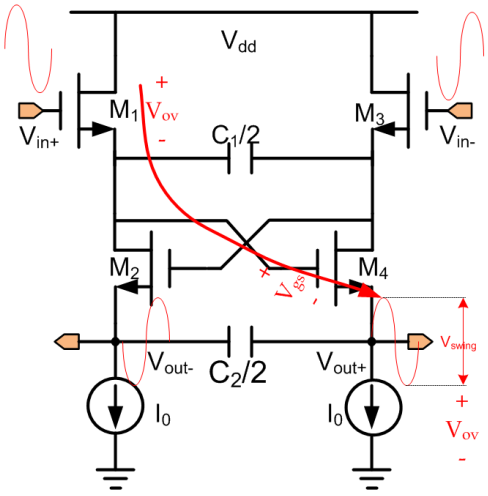


Figure 3.7: Supply voltage estimation

Note that in this structure, the maximum voltage swing (V_{swing}) is limited by the threshold voltage of M_2 and M_4 since large V_{swing} will drive these transistors into triode region.

F. Power consumption

As mentioned in last section, low power consumption is considered to be the main advantage of this biquad cell because we can bias the transistors at low overdrive

voltage. In addition, no common mode feedback (CMFB) circuit is required, since the output biasing point is fixed by the gate-source voltage and the input DC point. Therefore, there is no power budget for a CMFB circuit. Finally, there are no passive resistors, since in this biquad no DC power is dissipated. In total, the power consumption is $2I_0*V_{DD.}$

3.2.3 Voltage-mode biquad design procedure and simulation results

In this section, a design example of the voltage-mode biquad filter is presented as well as the simulation results. The technology library used is the 130nm UMC technology with a supply voltage of 1.2 V.

A). Channel length (*L*) selection

With the scaling of CMOS technology, transistor can handle faster and faster signals due to the short channel length. At the minimum channel length in 130nm technology, the cutoff frequency f_T can go up to 100GHz. In the zero-IF baseband section, however, such frequency is not needed. Therefore, we can use longer channel length transistors in the baseband. In addition, as mentioned above, a long channel transistor is desired to reduce the channel modulation effect. From the matching perspective, the long channel length transistor has a better matching property which is beneficial to filter's sensitivity. Fig. 3.8 shows f_T of the PMOS and NMOS at different V_{gs} and *L.* channel length for M_1-M_4 is fixed at L=500nm. As for the current sources I_0, L=1um is used.

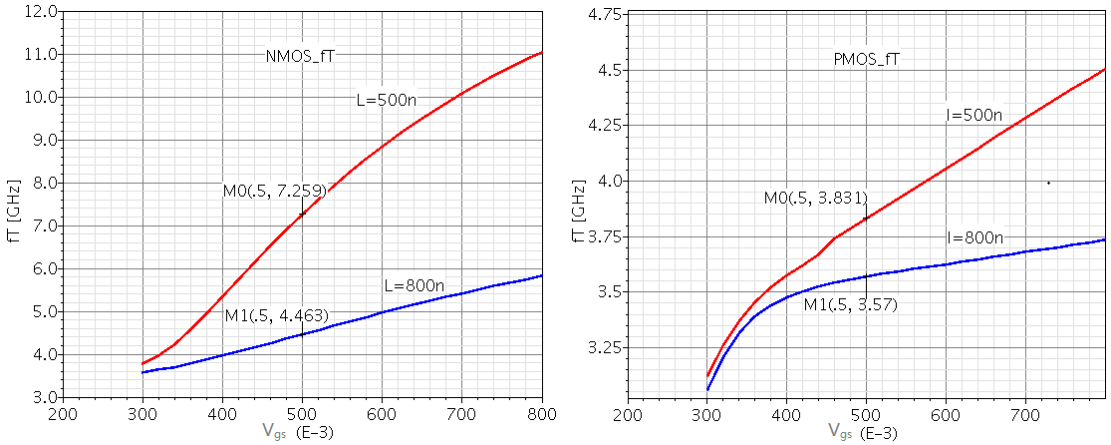


Figure 3.8: NMOS and PMOS cutoff frequency versus Vgs at different channel length L: Red line for L=500nm and blue line for L=800n.

B). Selecting the g_m value

As mentioned in Chapter one, the LTE mobile communication system employs a multi-antenna transceiver architecture with zero-IF I/Q detection. Thus, there are at least two receiver paths. In the baseband section, there would be at least four variable bandwidth filters. The filter size, mainly occupied by the capacitors, becomes a critical problem in the LTE system. In order to confine the baseband section into a reasonable chip area, we expect each capacitor to be reasonable small. According to equations (3.10-3.11), a small g_m value indicates small capacitor area given certain a Q. On the other hand, according to Fig. 3.6, g_m determines the input noise value given a certain quality factor Q and cutoff frequency f_0. A large g_m is expected to result in a IRN as small as possible. Therefore, a tradeoff exists between the chip area and IRN.

In the end, g_m= 5mS is selected since in this case C is around 10pF and the IRN is acceptable (i.e., a V_{swing} of 300mV gives a dynamic range of 67dB). In the following part, NMOS biquads with Q=0.71 and g_m=5mS is used in our design.

C). Biasing condition

For the NMOS at L=500nm, threshold voltage V_{thn} varies between 0.27V~0.34V when source bulk votalge V_{sb} changes between 0 and 0.7V. With the supply voltage of 1.2V, high overdrive voltage might does not work according to equation (3.15). Since low overdrive voltage is beneficial to the filter linearity based on our previous analysis, in this circuit, M1~M4 are biased at around 100mV. As for the current sources, 120mV is used.

D). Stability

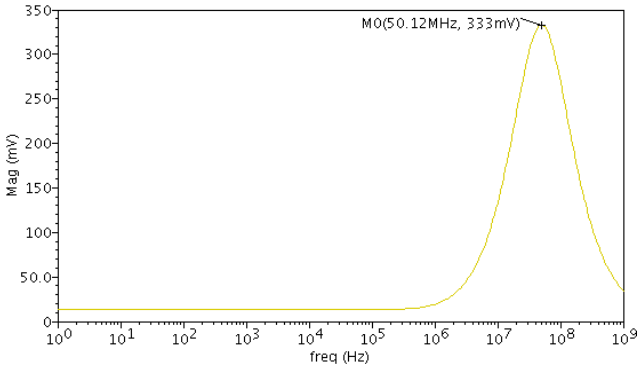


Figure 3.9: Loop gain simulation

According to equation (3.14), loop gain of the biquad cell shows band pass response. This agrees very well with the simulation result (Fig. 3.9). As can be seen from the curve, the loop gain peaks at 50MHz with 0.33. Therefore, the loop gain is always less than one and stability is guaranteed.

E). AC response

According to equation (3.12), the estimated biquad DC gain of -1.6dB (g_{mb}=0.5mS in this case) is obtained when neglecting g_{ds}. This value agrees with the simulation result (-1.97dB) shown in Fig. 3.10. The graph also shows that beyond the cutoff frequency of 50MHz the roll-off is around -20dB/dec, which is expected for the all-pole second-order filter. Finally, this filter does not suffer from the parasitic zero since it is at a very high frequency (higher than 5GHz).

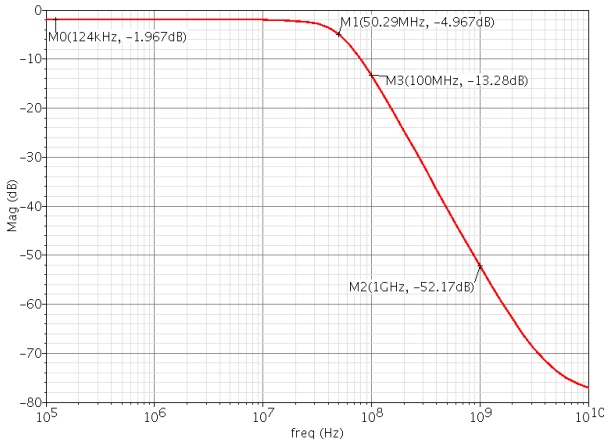


Figure 3.10: Biquad gain simulation (|H(s)|)

F). Input referred noise (IRN)

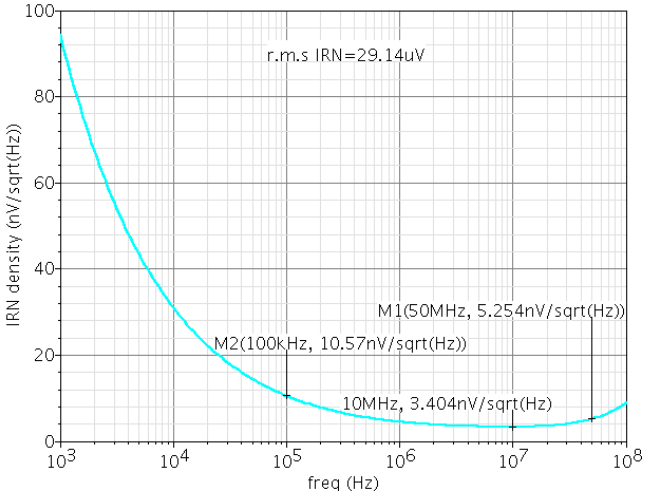


Figure 3.11: Input referred noise (IRN) simulation

Fig. 3.11 presents the noise performance of the biquad. According to the curve, the minimum input referred noise density is about 3.4nV/√Hz at 10MHz, mainly from thermal noise. At low frequency, flicker noise is dominant and the flicker corner frequency (intersection point between flicker noise and thermal noise [16]) is around 10 kHz. When the frequency approaches and exceeds the cutoff frequency, the noise density rises up, as predicted by equation (3.13). After Integrating from 100 kHz to 50MHz, we can obtain the total input equivalent noise of 29.14 μV, which is in accordance with the value calculated according to Fig. 3.6.

G). In-channel linearity

In-channel linearity (IIP3) is simulated through the two-tone test with a tone spacing of 1MHz. The simulation result of IIP3 versus frequency is shown in Fig. 3.12. Clearly, IIP3 becomes worse and worse as the frequency increases, which is predicted by our previous analysis (loop gain of the source follower decreases with increasing frequency). At the cutoff frequency of 50MHz, the IIP3 is degraded to around 3dBm. The degradation of in-channel linearity versus frequency is the main defect of this filter.

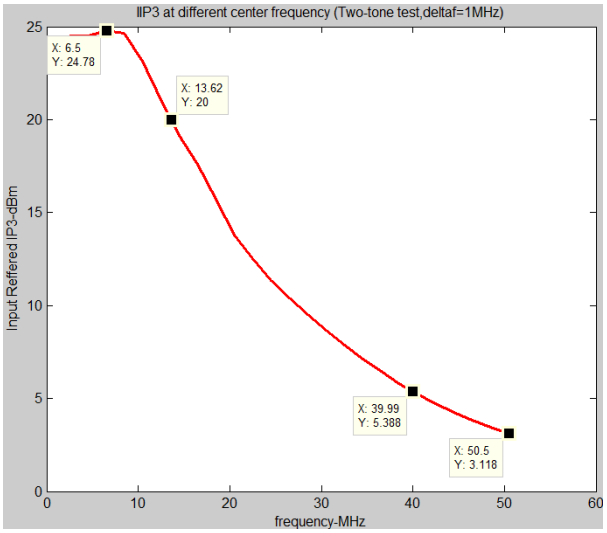


Figure 3.12: IIP3 vs. the center frequency of the two-tone test with frequency space of 1MHz

H). Out-of-channel linearity

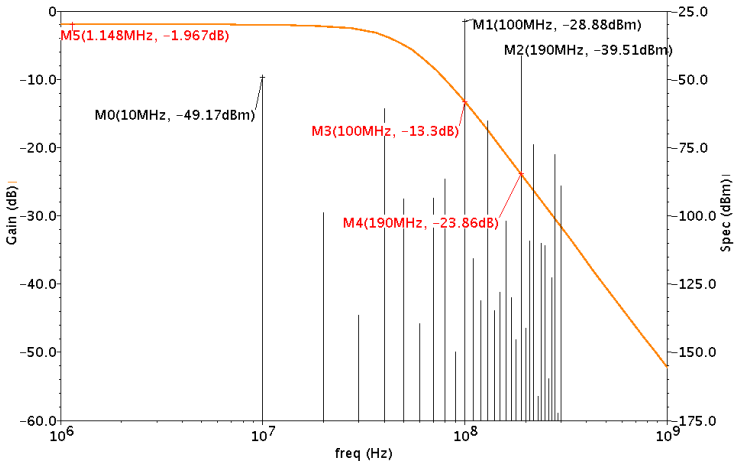


Figure 3.13: Out-of-channel linearity two-tone test with one frequency at 100MHz and the other at 190MHz. Input signal power used for simulation is -15dBm, and the output spectrum power is shown on the right y-axis.

Fig. 3.13 shows the two-tone simulation result in out-of-channel linearity. The third order IM product falls into the filter passband at 10MHz. according to Fig. 3.13 and the calculated out-of-linearity is around 3dBm. This biquad is not a good filter for the LTE communication system as it cannot reject the strong out-of-channel blockers.

I). Dynamic range

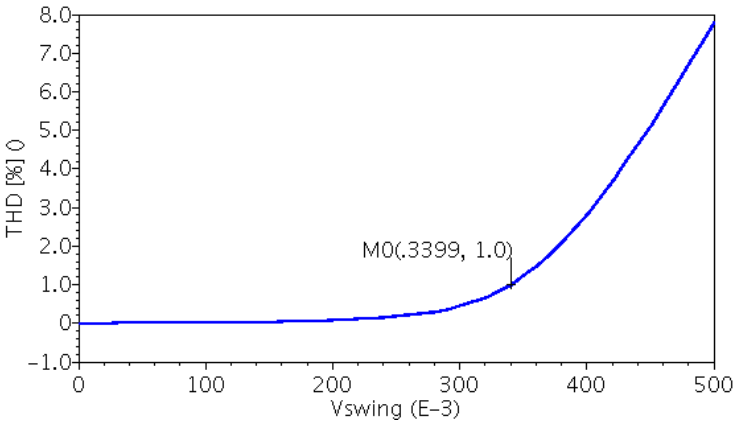


Figure 3.14: THD simulation with input signal frequency of 10MHz.

According to Fig. 3.14 (at 10MHz), the total harmonic distortion (THD) of -40dB is obtained when the input signal swing is about 340mV$_{peak}$. Given the input noise of 29.14 μ V, the dynamic range of the filter is 78.3 dB at this frequency.

To sum up, we list all the filter parameters in the tables 3.1 and 3.2. Table 3.1 shows

the filter general information, and table 3.2 presents the filter performance. As can be seen from these tables, the voltage-mode filter has a dynamic range of 78.3dB with power consumption of 0.847mW. However, the in-channel linearity degrades with increasing frequency; moreover, the out-of-channel linearity is very poor.

Table 3.1: Voltage-mode biquad filter parameters

	g_m [mS]	g_{mb} [mS]	overdrive voltage[mV]	W/L [μ m]	I_0 [μ A]	Cap [pF]
$M_{1,3}$	5	0.4	94	54.4/0.5	353	$C_1/2$=11.25 $C_2/2$=5.625
$M_{2,4}$	5	0.5	94	55.04/0.5		
I_0	4.35	--	124	79.36/1		

Table 3.2: Voltage-mode filter performance

Power consumption [mW]	0.847
DC gain [dB]	-1.967
IRN [μ V]	29.14
IIP3 from DC to 50MHz [dBm] Δf=1MHz	24.7-3.12
Out-of-channel IIP3 [dBm] @100, 190MHz	3
Differential Input signal $V_{dd,zp}$ @THD=-40 dBc [mV]	340
Dynamic Range [dB]	78.3

3.3 Current-mode filter

As shown in Fig. 3.2(b), the equivalent circuit of Fig. 3.1(b) is a paralleled *RLC* network which works in current domain. This current mode filter actually is based on the common-gate stage, and can be utilized at the output stage of current mixer. In this section, the first-order common-gate filter will be discussed first, and then we turn to its biquad schematic.

3.3.1 Common gate based first order filter

The common gate stage, known as the current buffer due to its unity current gain, can also be employed for the filter just like the source follower. A first-order filter is shown in Fig. 3.15.

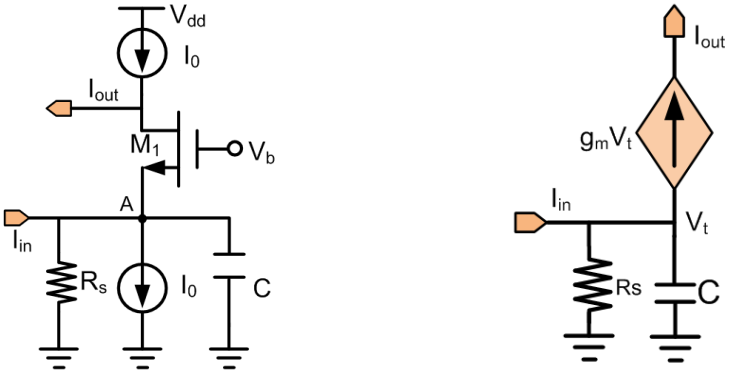


Figure 3.15: Current-mode first-order LPF with its small-signal model

A. Transfer function

Neglecting the transistor output conductance and body effect, the transfer function is written as (3.16) taking into account the current source impedance Rs.

$$H(s) = \frac{i_{out}}{i_{in}} = \frac{g_m}{sC+g_m+1/R_s} \tag{3.16}$$

The filter pole ω_0 and DC gain K_{DC} are

$$\omega_0 = \frac{g_m+1/R_s}{C} \tag{3.17}$$

$$K_{DC} = \frac{g_m}{g_m+1/R_s} \tag{3.18}$$

From equations (3.17-3.18), the source impedance Rs affects the filter pole frequency and DC-gain.

B. Linearity consideration

In general, for one MOS transistor, drain current is expressed by (3.19) [32]

$$i_d = f(v_{gs}, v_{ds}, v_{bs}) \tag{3.19}$$

v_{ds} and v_{bs} influence the drain current to some degree through g_{ds} and g_{mb}. In order to reduce the distortion resulting from v_{ds}, a longer channel length transistor is always desired. Besides, due to each internal node is low impedance, i.e., node A in Fig. 3.6, common-gate stage shows little distortion since voltage variation at node A is very small. And better linearity is obtained if we use a larger source impedance R_s.

C. Noise consideration

The main advantage of this current-mode filter is its noise shaping feature, as shown in Fig. 3.16. At low frequency, the noise current of M_1 re-circulates in itself (red arrow in Fig. 3.16(a)), thus contributes nothing to the output current, while most of the noise current of I_0 goes to the output.

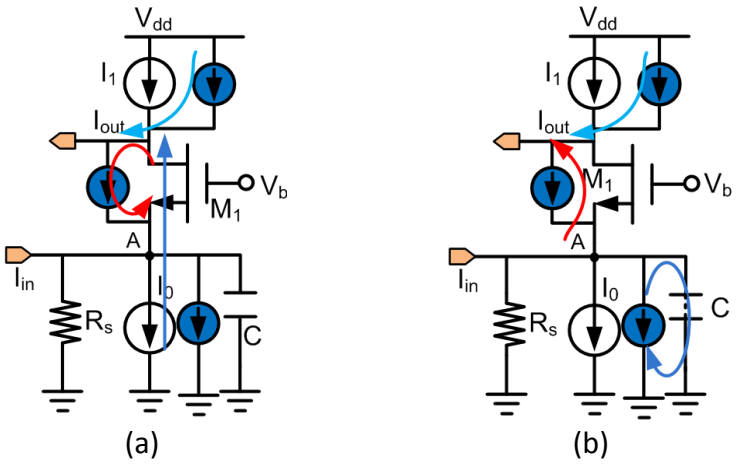


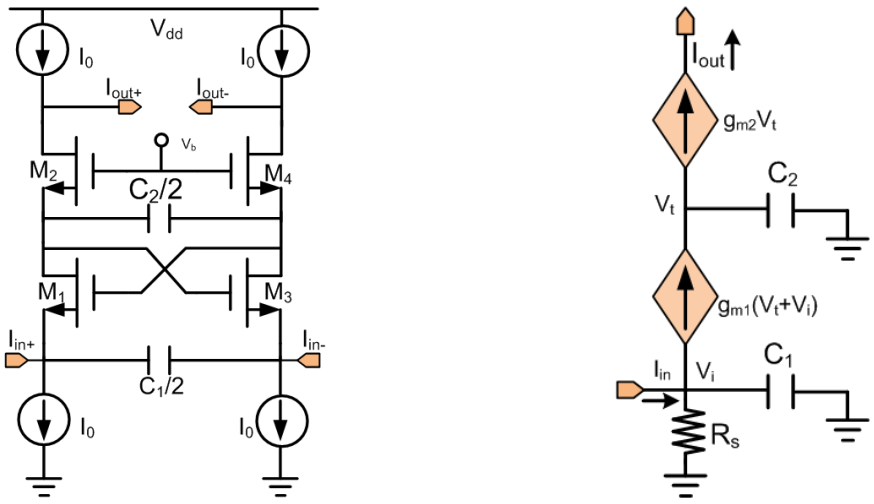
Figure 3.16: Output noise contributed by each of the noise sources at (a) low frequency, (b) high frequency

Above the pole frequency, the noise current of M_1 flows out of the output node, but noise produced by I_0 is shorted by the capacitance C_1 to ground. Therefore, the noise current of M_1 shows a high pass transfer function, which means in-band noise of M_1 is pushed out of the filter bandwidth. And noise produced by I0 follows the same transfer function as the signal. As for the noise source of I_1, since it appears directly at the output, an ultra-low $g_{m,I1}$ is necessary to decrease the noise.

In conclusion, the main merit of this common-gate filter is its noise shaping feature if the noise contributed by the current sources are negligible.

3.3.2 Common-gate based biquad filter

In this part, we consider the low pass biquad filter based on the common gate shown in Fig. 3.17 with respect to filter parameters, noise, linearity and power consumption.



(a) (b)

Figure 3.17: (a) common gate based biquad filter, (b) small signal model

A. Filter parameters

According to the small signal model of Fig. 3.17(b), the filter parameters of transfer function, cutoff frequency ω_0 and quality factor Q are given by

$$H(s) = \frac{1}{s^2\frac{C_1C_2}{g_{m1}g_{m2}} + s\left(\frac{C_2-C_1}{g_{m2}} + \frac{C_1}{g_{m1}}\right) + 1} \xrightarrow{g_{m1}=g_{m2}} \frac{-1}{s^2\frac{C_1C_2}{g_m^2} + s\frac{C_2}{g_m} + 1}, \tag{3.20}$$

$$Q = \frac{1}{\sqrt{\frac{g_{m1}}{g_{m2}}}\left(\sqrt{\frac{C_2}{C_1}} - \sqrt{\frac{C_1}{C_2}}\right) + \sqrt{\frac{g_{m2}}{g_{m1}}}\sqrt{\frac{C_1}{C_2}}} \xrightarrow{g_{m1}=g_{m2}} \sqrt{\frac{C_1}{C_2}}, \tag{3.21}$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \xrightarrow{g_{m1}=g_{m2}} \frac{g_m}{\sqrt{C_1C_2}}. \tag{3.22}$$

Compared with the voltage mode biquad, they have the same filter parameters.

B. Noise performance

As mentioned previously, noise shaping is the main advantage of this current-mode biquad. Each noise source of the biquad is shown in Fig. 3.18(a) as well as its equivalent input noise in Fig. 3.18(b). After a careful calculation, we can obtain the total input referred noise current density in (3.23).

$$IRN^2 = 8kT\gamma\left[\underbrace{g_{m,I0}}_{I_{0,b}} + g_m\underbrace{\left|Q\frac{jf}{f_0}\right|^2}_{M_{1,3}} + \underbrace{g_m\left|\frac{jf}{f_0}\frac{1-Q^2}{Q} - \left(\frac{f}{f_0}\right)^2\right|^2}_{M_{2,4}} + \underbrace{g_{m,I0}\left|\frac{jf}{f_0Q} + 1 - \left(\frac{f}{f_0}\right)^2\right|^2}_{I_{0,u}}\right]. \tag{3.23}$$

From the annotation in equation (3.23), we can clearly see the noise contributed by

each transistor in the biquad.

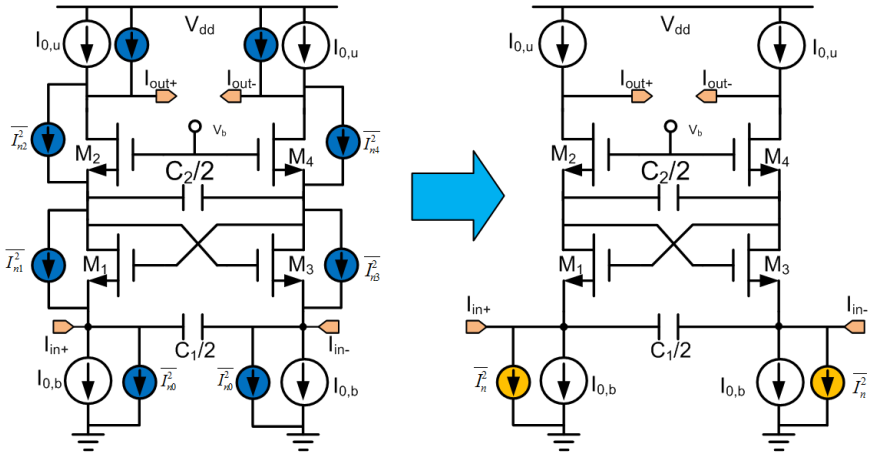


Figure 3.18: (a) noise sources of the biquad and (b) its equivalent input noise.

As expected, the noise behavior of $M_{1,3}$ and $M_{2,4}$ shows a frequency dependent property. In order to decrease the noise associated with the current sources, we should make sure that the transconductance $g_{m,I0}$ is very small according to equation (3.23). Assume $g_{m,I0}$ is one-half of g_m, the integrated value of IRN (from 100KHz to 50MHz) versus g_m is shown in Fig. 3.19 (red curve). The blue curve in Fig. 3.19 is the noise associated with the current sources. Clearly, current sources are the main noise sources in this filter if $g_{m,I0}$ is comparable with g_m.

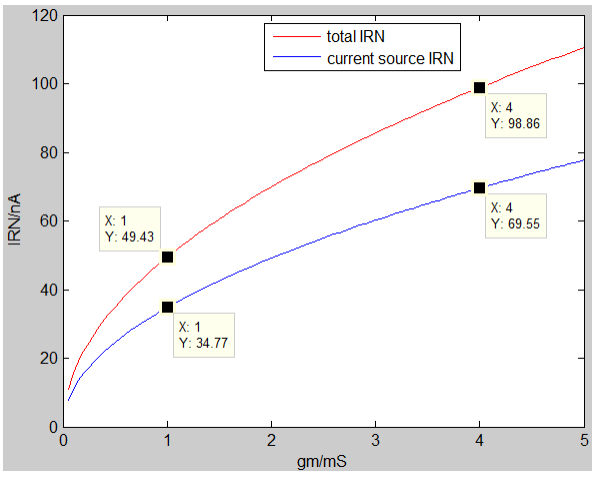


Figure 3.19: Integrated input noise value (from 100kHz to 50MHz) versus gm at Q=0.71, f_0=50MHz and g_m, $I_0=g_m/2$

C. Linearity performance

Linearity is checked through the input impedance of this biquad (Fig. 3.17), as

described by equation (3.24);

$$Z_{in}(s) = \frac{s\frac{C_2}{g_m^2}}{\frac{s^2}{\omega_0^2}+\frac{s}{\omega_0 Q}+1}. \tag{3.24}$$

Inserting the values of g_m=5mS, Q=0.71 and f_0=50MHz, we can get the simulation result shown in Fig. 3.20.

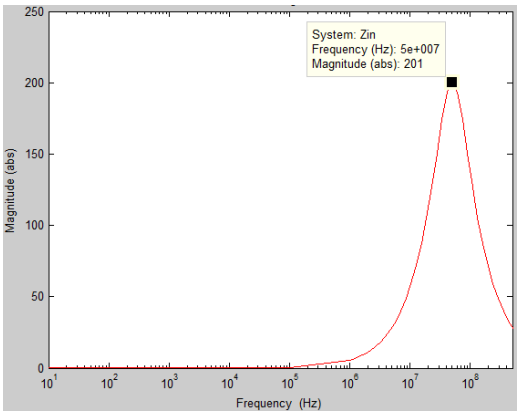


Figure 3.20: Current-mode filter input impedance versus frequency at g_m=5mS, Q=0.71 and f_0=50MHz.

According to the graph, high linearity can be achieved at low frequency due to the low input impedance. However, when the frequency goes up the input impedance also increases and peaks at the cutoff frequency. Therefore, the in-channel linearity of the current-mode filter will decrease as the frequency approaches f_0, as in the case of voltage-mode filter. After exceeding f_0, the impedance reduces, thus high linearity is obtained outside of the filter bandwidth.

D. Minimum supply voltage estimation

One advantage of current-mode circuit over its voltage-mode counterpart is the former one can provide the opportunity for low power supply application, since voltage swing at each internal node is small. The biquad minimum supply voltage can be estimated according to Fig. 3.21,

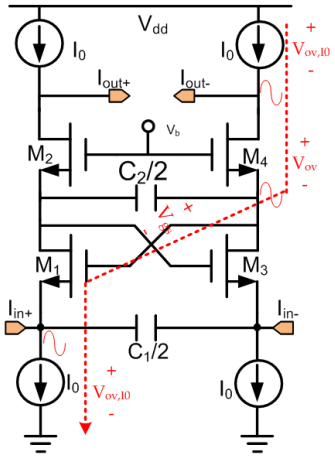


Figure 3.21: Current mode biquad supply voltage estimation

in which V_{ov} is the overdrive voltage of M_1-M_4, V_{th} is the transistor threshold voltage and *X* is the voltage margin for the internal nodes. The required supply voltage can be written as:

$$V_{dd,min} = 2V_{ov,I0} + V_{gs} + V_{ov} + X = 2V_{ov,I0} + 2V_{ov} + V_{th} + X \qquad (3.25)$$

Note that In order to reduce the current source noise, we have to make sure $V_{ov,I0}$ is as large as possible. Therefore, the minimum required supply voltage is determined from the noise considerations.

E. Power consumption

As with the voltage-mode filter, this filter also has the advantage of low power consumption. If noise is not the first consideration, the power consumption can be reduced further.

3.3.3 Current-mode biquad design procedure and simulation results

The current-mode filter design procedure is similar to that of the voltage-mode filter. Thus, we will put the emphasis on the current-mode filter performance merits of gain, noise linearity and dynamic range for brevity.

A). Gain simulation

The small-signal frequency response of the current mode filter is shown in Fig. 3.22. The DC gain is -0.37dB. At high frequency, this filter has a roll-off of 40dB/dec, as

expected.

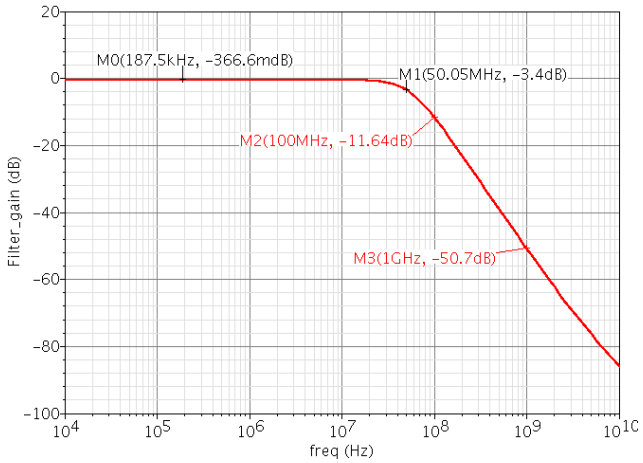


Figure 3.22: Current mode biquad filter gain simulation

B). Input-referred noise

Fig. 3.23 (a) presents the IRN simulation result with a minimum noise current density of 5.93pA at 7MHz. After integration from 100 kHz to 50MHz, the input-referred noise is 50.03nA.

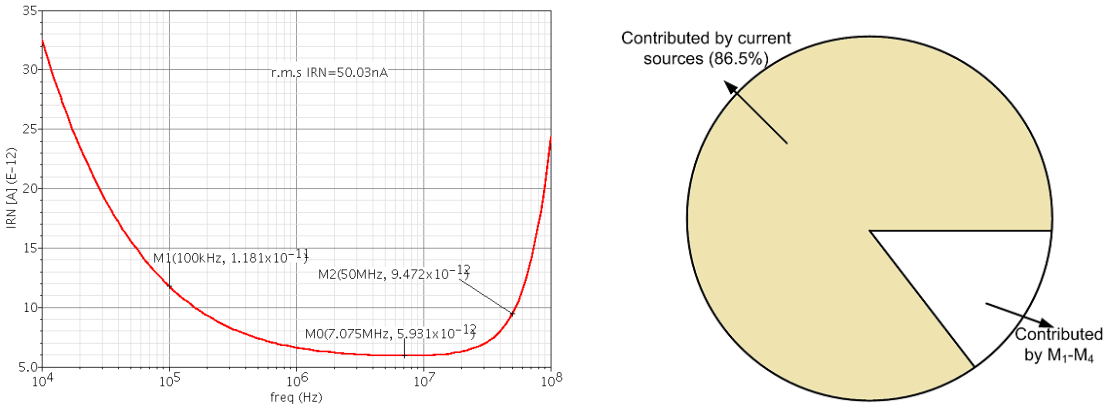


Figure 3.23: Current-mode biquad noise simulation of (a) IRN density, (b) proportion of spot noise at 7MHz.

The pie chart shown in Fig. 3.23(b) shows that at 7MHz, the noise contributed by current sources is 86% of the total noise, which is consistent with Fig. 3.19.

C). In-channel linearity

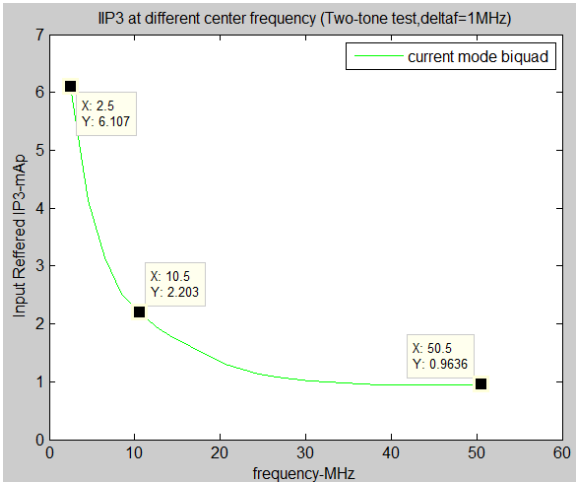


Figure 3.24: Current-mode biquad channel IIP3 versus frequency (two-tone test with spacing of 1 MHz). Note that IIP3 is expressed in the form of input current amplitude (zero-to-peak) in mA_p.

In-channel linearity of the current mode filter is plotted in Fig. 3.24. According to this graph, in-channel linearity decreases from 6.1mAp to 0.96mAp with increasing frequency, as pointed out previously.

D). Out-of-channel linearity

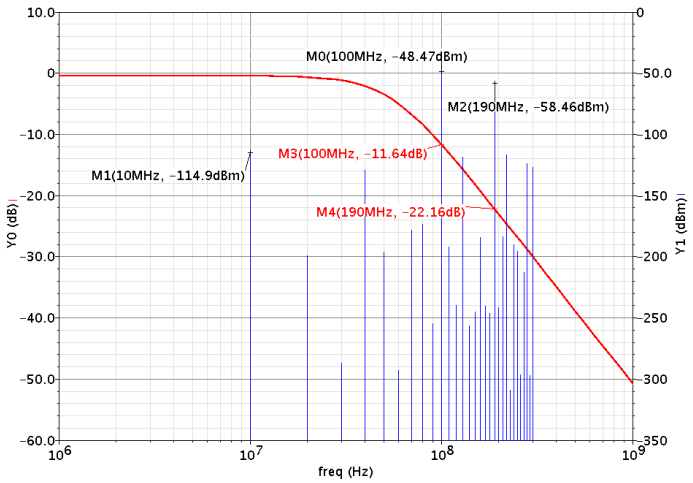


Figure 3.25: Current-mode biquad out-of-channel linearity two-tone test with one frequency at 100MHz and the other at 190MHz. Input signal power is -16dBm. Note that the presence of the others spurs is due to the beat frequency used in our simulation.

Filter out-of-channel linearity is measured by two-tone test with one frequency at 100MHz and the other at 190MHz (the beat frequency used is 10MHz). The third-order IM product falls in band at 10MHz. According to the output spectrum shown in Fig.

3.25, we can calculate the out-of-channel linearity is around 4.55mAp, which indicates the current-mode filter has good out-of-channel linearity, meaning the out-of-channel blockers can be attenuated greatly.

E). Dynamic range

The dynamic range is calculated when the signal frequency is 10MHz. For a THD of -40dBc, the input current magnitude is 168.7uA (Fig. 3.26), which gives us a dynamic range of 67.5dB with IRN of 50.03nA. Compared to the voltage-mode filter, this dynamic range is lower by 11dB.

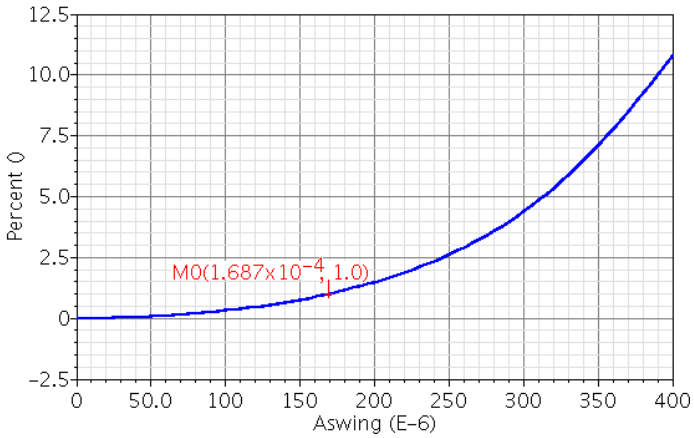


Figure 3.26: THD simulation with input signal frequency of 10MHz.

In conclusion, tables 3.3 and 3.4 list all the parameters of the current mode filter. Compared with the voltage-mode filter, power consumption is nearly equal for both of them. However, the advantage of the current-mode filter is its better out-of-channel linearity although its dynamic range is poor (10dB lower).

Table 3.3: Current-mode biquad filter parameters

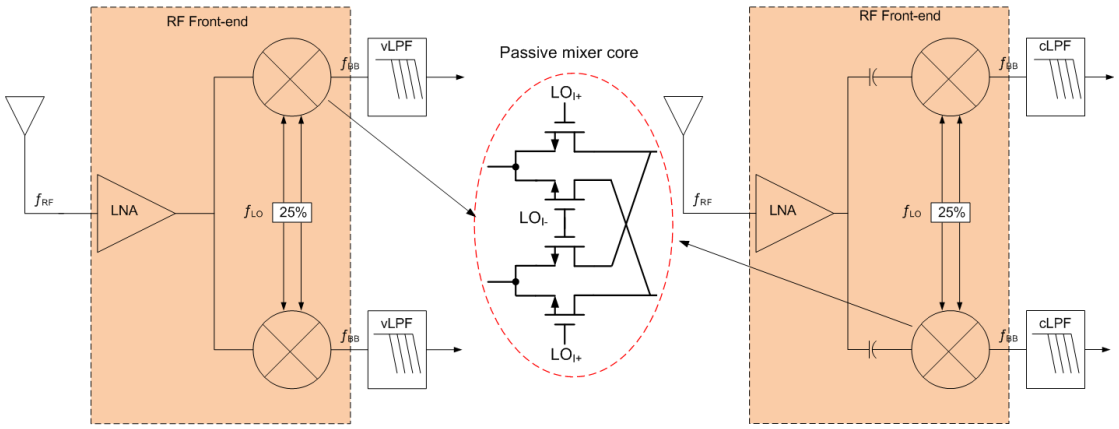
	g_m[mS]	Vov[mV]	W/L[μ m]	I_{bias}[μ A]	Cap[pF]
$M_{1,3}$	5	100	47.2/0.5	364	$C_1/2$=5.6 $C_2/2$=11.2
$M_{2,4}$	5	100	52/0.5		
$PM_{1,2}$	1.64	320	99.84/1		
$NM_{1,2}$	3	200	39.68/1		

Table 3.4: Current-mode filter performance

Power consumption [mW]	0.874
DC gain [dB]	-0.37
IRN [nA]	50.03
IIP3 from DC to 50MHz [mA_p] Δf=1MHz	6.11-0.96
Out-of-channel linearity [mA_p] @100, 190MHz	4.55
$A_{dd,zp}$ @THD=-40 dBc [μ A]	168.7
Dynamic Range [dB]	68.5

3.4 RF front-ends for voltage-mode and current-mode filters

There are two different receiver structures for each filter, as shown in Fig. 3.27. In these two structures a passive mixer core is used as an example. In Fig. 3.27(a), since the input impedance of the filter is capacitive, voltage is the mixer output (no current flows into the filter at baseband frequency). While in Fig. 3.27(b), due to the low input impedance of the current-mode filter, the mixer output current drives the filter. Note that two AC coupling capacitors are used in Fig. 3.27(b) to block the DC current flowing through the mixer.



(a) (b)

Figure 3.27: RF front-ends for (a) voltage-mode filter (b) current-mode filter.

3.5 Conclusion and Summary

To sum up, we list the advantages and disadvantages of the both filters in table 3.5. By comparing these two filters, we can see they dissipate almost the same power. However, with 1.2V as the supply voltage, the current-mode filter is less attractive due to the noise problem resulting from the bias current sources. Moreover, its dynamic range is smaller by 10dB. Although it has good out-of-channel linearity, we have decided to use the voltage-mode filter in our following design. Therefore, Fig. 3.27(a) will be the test bench for our further simulations.

Table 3.5: Comparison between the voltage-mode and current-mode filters

	Advantages	Disadvantages
Voltage-mode filter	(1) Dynamic range: 78.3dB (2) Power consumption:0.847mW	(1) Poor out-of-channel linearity (2) In-channel linearity decreases with increasing frequency
Current-mode filter	(1) Good out-of-channel linearity (2) Power consumption:0.874mW	(1) Dynamic range: 68.5dB (2) In-channel linearity decreases with increasing frequency (3) Current source noise is critical (1.2V supply voltage)

In this chapter, we analyzed and simulated two different G_m-C biquads distinguished by their working domains: a voltage-mode filter and a current-mode filter. Simulations were carried out in 130nm UMC technology. According to the analysis and simulation results, each of them has its own advantages and disadvantages. For instance, the voltage-mode filter has higher dynamic range while it suffers from poorer out-of-channel linearity than the current-mode filter. However, the in-channel linearity for both of them drops with increasing frequency. By comparing their performance with respect to power consumption, linearity, noise and dynamic range, we decide to use the voltage-mode filter in our design.

Chapter 4

Flexible Gm-C filter realization and simulation results

In this chapter, we focus firstly on the design of a flexible G_m-C filter such that it can cover the entire channel bandwidth required in LTE-Advanced systems. In our case, the filter with variable bandwidth of changing from 0.7MHz to 50MHz is designed. MOS switches are used to turn on or off the g_m and capacitor units for tuning. In the second section, we discuss how to solve the out-of-channel linearity problem present in this voltage-mode filter.

4.1 Flexible G_m-C biquad design

For a G_m-C type filter, parameters such as DC gain, cutoff frequency ω_0 and quality factor Q are determined by G_m and capacitors. Therefore, we can tune the value of G_m and C to realize the flexibility.

4.1.1 Tuning algorithms

Fig. 4.1(a) illustrates a way of implementing a flexible G_m-C filter in which transconductance and capacitors arrays are used. The paralleled array is digitally controlled by MOS switches, i.e., one differential capacitor shown in Fig. 4.1(b). Theoretically, the presence of switches should not degrade the filter's performance (i.e., linearity, noise and quality factor). Therefore, the switches should have low on-resistance as well as high linearity. This tuning algorithm allows us to tune the cutoff frequency (ω_0) and quality factor (Q) independently, if for example, ω_0 is proportional to g_m while Q is determined by the capacitor ratio.

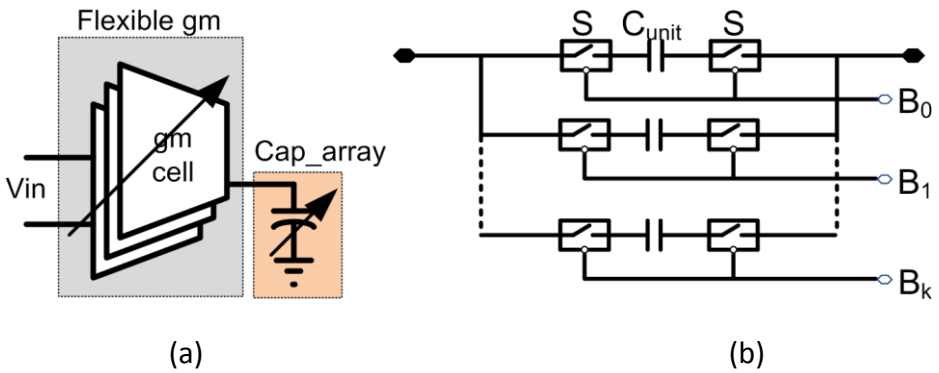


Figure 4.1: Flexible Gm-C filter (a) realization diagram (b) capacitors array

Given the fact that capacitors consume the majority of the filter area, we prefer to change G_m instead of increasing capacitor area to cover the required channels. In addition, there are several advantages when tuning G_m: (1) theoretically, changing G_m would not influence the integrated input noise since it is determined by kT/c, (2) the frequency step can be linearly controlled, and (3) power dissipation is saved at smaller G_m.

However, when G_m is scaled down for smaller bandwidth, the integrated noise rises due to the increase of flicker noise from the smaller transistor size. Therefore, capacitor tuning is utilized to cope with the noise problem when smaller bandwidths are desired. In our case, for chip area consideration, the maximum tunable value of the capacitor is up to four times the original value ($C_1/2$=11.25pF and $C_2/2$=5.625pF). As for G_m, a 6-bit control bus is selected for G_m tuning, which means there are 64 transconductance units in total, and one unit is 78 μ S.

Therefore, a combination of Gm tuning and capacitor tuning algorithm is used in this design. According to equations (3.8-3.10), we propose one tuning approach to achieve the flexibility with Q=0.71, meanwhile keeping the input integrated noise as small as possible as illustrated in table 4.1.

Table 4.1: Tuning algorithm for variable bandwidth LPF

Desired bandwidth [MHz]	Tuning algorithm(C_1/2=11.25pF, C_2/2=5.625pF)
50→25	**Gm**: 5mS→2.5mS; keep C_1 and C_2 constant
25→16.6	**Gm**: 5mS→3.3mS; make C_1 and C_2 doubled
16.6→12.5	**Gm**: 5mS→3.7mS; make C_1 and C_2 tripled
12.5→0.7	**Gm**: 5mS→0.28mS; make C_1 and C_2 fourfold

4.1.2 Flexible transconductance design

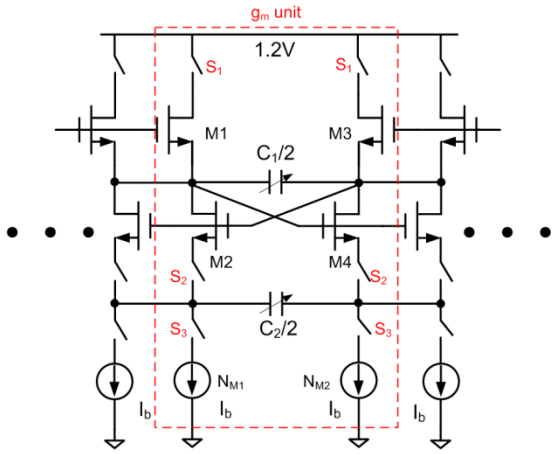


Figure 4.2: Flexible G_m schematic with 64 units in total.

Fig. 4.2 shows us the 6-bit controlled flexible G_m schematic, which consists of 64 g_m units. To turn "on" or "off" one unit completely, 6 switches are inserted according to the figure. In order to reduce the switches' impact on the filter performance, there is one principle guiding placement of the switches: make sure the switches in the signal path are as few as possible. In this circuit, only S_2 is in the signal path.

When designing a switch with MOS transistors, the on-resistance is expected to be as small as possible. According to the on-resistance equation,

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{gs}-V_{th})}, \tag{4.1}$$

a large aspect ratio transistor is desired to reduce R_{on} when the overdrive voltage (V_{gs}-V_{th}) is fixed. However, a large transistor results in more leakage current (when the switch is off) and greater parasitic capacitance. Therefore, a trade-off exists when designing the switch size.

It is worthwhile to investigate the effect of switches S_2 since they are in the signal path. Analysis of Fig. 4.3 yields the new filter parameters (e.g., 4.2-4.4) including R_{on}.

$$H(s)_{new} = \frac{g_m^2}{s^2 C_1 C_2 (1+g_m R_{on}) + s g_m (C_1 + C_2 g_m R_{on}) + g_m^2} \tag{4.2}$$

$$\omega_{new} = \sqrt{\frac{g_m^2}{C_1 C_2 (1+g_m R_{on})}} \tag{4.3}$$

$$Q_{new} = \frac{\sqrt{C_1 C_2 (1+g_m R_{on})}}{(C_1 + C_2 g_m R_{on})}. \tag{4.4}$$

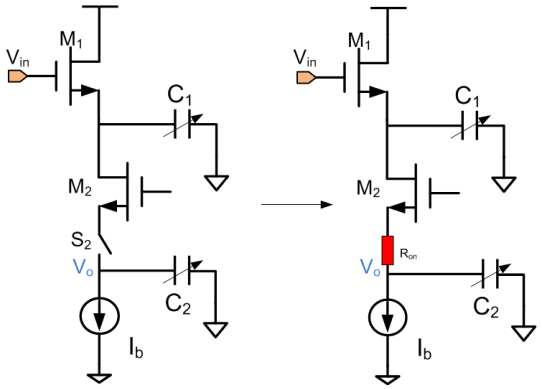


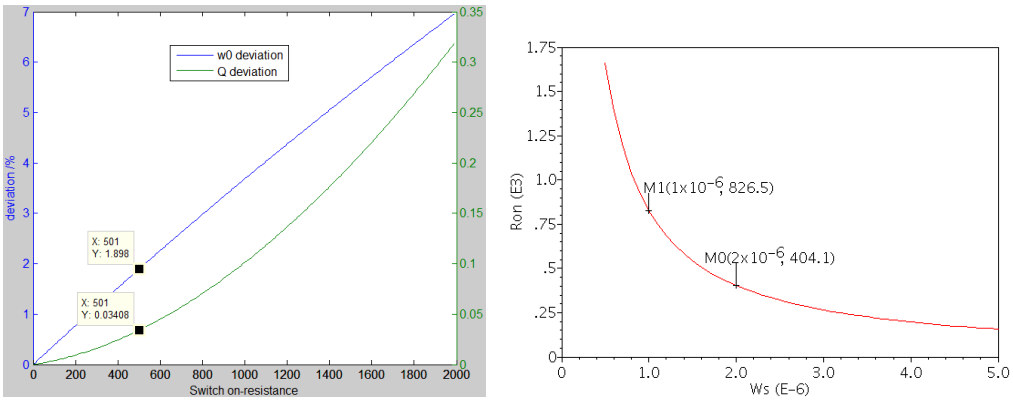
Figure 4.3: The impact of switch S2 on-resistance on the filter performance.

Compared with equations (3.8-3.10), the filter DC gain is kept constant while the cutoff frequency and quality factor deviate from the design value. The deviations are given by (e.g., 4.5-4.6):

$$\frac{\Delta\omega}{\omega_0} = \frac{\omega_0 - \omega_{new}}{\omega_0} = 1 - \frac{1}{\sqrt{1+g_m R_{on}}} \tag{4.5}$$

$$\frac{\Delta Q}{Q} = \frac{Q_0 - Q_{new}}{Q_0} = 1 - \frac{\sqrt{1+g_m R_{on}}}{1+g_m R_{on} Q^2}\ . \tag{4.6}$$

After inserting the values (g_m=78 μ s and Q=0.71) and sweeping R_{on} in Matlab, we can obtain the result as shown in Fig. 4.4(a), from which, lower R_{on} promises smaller deviation. For instance, when R_{on}=500 Ω, the deviations are 1.898% and 0.034% for cutoff frequency and quality factor, respectively. Fig. 4.4(b) presents the Spectre simulation result of switch on-resistance versus channel width W (channel length L=120nm). According to these two graphs, W_{s2}=2um is selected for S_2.



(a) (b)

Figure 4.4: (a) Matlab simulation result of deviation versus S2 on-resistance, (b) Spectre simulation result of S2 on-resistance versus the channel width W (L=120nm).

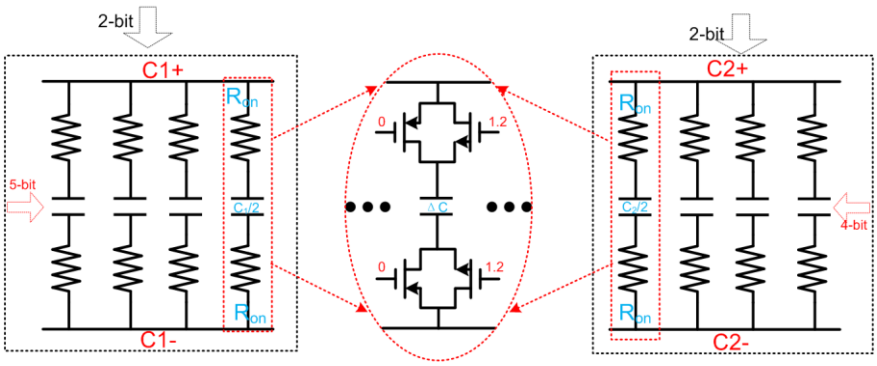
For S_1 and S_3, since they are not in the signal path, we can use relative small transistors compared to S_2. Finally, W_{s1}=2 μ m (S_1 is PMOS) and W_{s3} =1 μ m are used for S_1 and S_3 respectively. Table 4.1 lists all of the parameters for one g_m unit.

Table 4.2: gm unit parameters

gm unit parameters (6-bit)			
	W/L [μ m/ μ m]	g_m[μ S]	I_b [μ A]
$M_{1,3}$	0.85/0.5	78.16	5.5
$M_{2,4}$	0.86/0.5	78.17	5.5
N_{M1},N_{M2}	1.24/1	67.86	5.5
Switch size [μ m/ μ m]			
S_1=2/0.12, S_2=2/0.12, S_3=1/0.12			

4.1.3 Capacitor array design

Tuning algorithm of the capacitors array is shown in Fig. 4.5, from which, C_1 and C_2 are controlled by 7-bit and 6-bit, respectively. For narrow channel tuning, 2-bits are allocated to control the 4 parallel connection capacitors, while the rest of the bits are used to cope with the capacitor processing variation problem. Because all of the switches carry the signal, transmission gate switches are utilized for better linearity and lower on-resistance.



(a) (b)

Figure 4.5: (a) 7-bit controlled capacitor array C1 and (b) 6-bit controlled capacitor array C2.

Before investigating the influence of R_{on}, let us consider how to transfer N-parallel units (series RC circuit) to one simple series RC circuit. As illustrated step by step in Fig. 4.6, N-parallel units are firstly converted to their equivalent circuit with a constant quality factor $Q_{\Delta C}$. Simplifying and making a parallel to series, we can get its series RC circuit. Therefore, the relationship between R_{on} and R_{sw} (one single on-resistance of the transmission gate) can be written as $R_{on}=R_{sw}/N$.

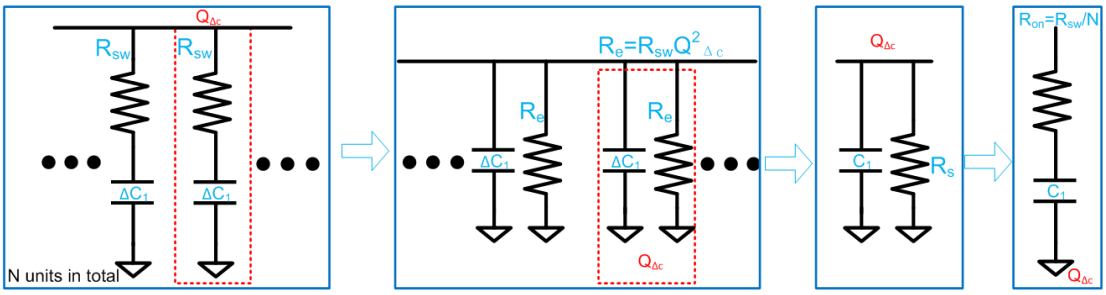


Figure 4.6: impedance transformation diagram.

Evaluating the influence of R_{on} on the filter function is similar to that of designing switch S_2. The equivalent circuit is shown in Fig. 4.7, and from its analysis we can write the equation in 4.7-4.8:

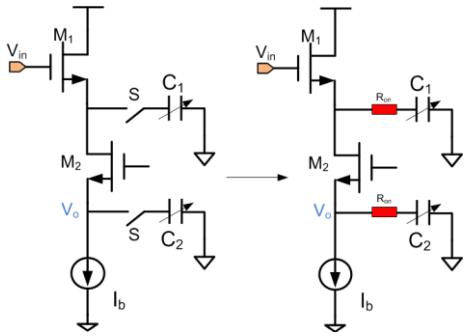


Figure 4.7: The impact of the on-resistance of switches on the filter performance.

$$\frac{\Delta\omega}{\omega_0} = 1 - \frac{1}{\sqrt{1+g_m R_{on}+(g_m R_{on})^2}} \tag{4.7}$$

$$\frac{\Delta Q}{Q} = 1 - \frac{\sqrt{1+g_m R_{on}+(g_m R_{on})^2}}{1+g_m R_{on}+g_m R_{on} Q^2}. \tag{4.8}$$

Inserting the values of G_m=5ms and Q=0.71, we obtain the simulation results shown in Fig. 4.8. Compared with Fig. 4.4(a), it can be seen that switches in the capacitor array have more impact on the filter performance: for instance, the deviations of cutoff frequency and quality factor are 5.3% and 8.7% respectively when R_{on}=20 Ω, which gives R_{sw}=320 Ω for N=16 (4-bit). According to the simulation results, it is clear that large switches result in low on resistance and low deviations. However, due to parasitic capacitance, we select W_s= 2 μ m (NMOS) as a compromise.

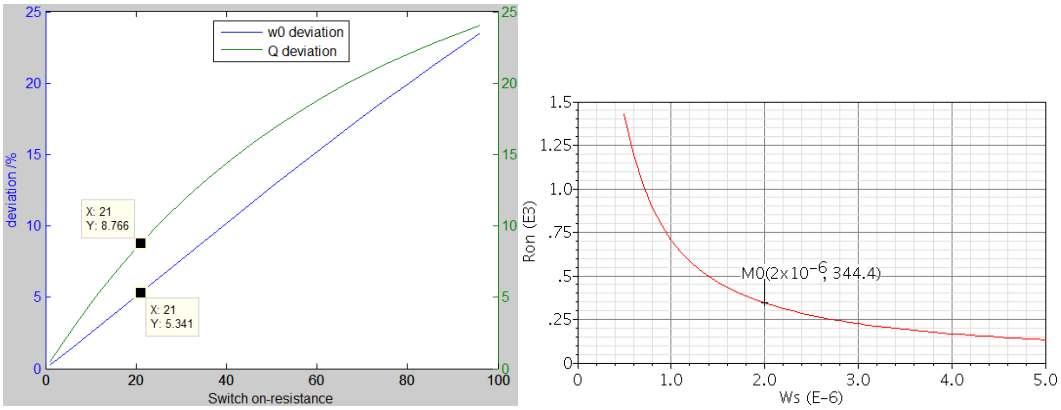


Figure 4.8: (a) Matlab simulation result of deviation versus switch on-resistance, (b) Spectre simulation result of on-resistance for one transmission gate versus the channel width W (L=120nm), assume Wp/Wn=2.

We list the parameters of the capacitor arrays in detail in table 4.3.

Table 4.3: Capacitor array parameters

	Δ C	Transmission gate switches
C1(7-bit)	350fF	NMOS: 2u/0.12u PMOS: 4u/0.12u
C2(6-bit)		

4.1.4 Simulation results

Simulation results of the flexible G_m-C filter are given in this section, including the variable bandwidth and quality factor, the IRN and the in-channel linearity.

A). Cutoff frequency calibration

As illustrated above, finite switch on-resistance shifts the filter frequency from the designed value. To solve this problem, we can tune the capacitor unit to calibrate the frequency. As shown in Fig. 4.9, the blue and red lines represent the filter frequency before and after capacitor tuning, respectively. When the capacitor value is 350fF, the filter's maximum and minimum frequencies are 43.24MHz and 0.61MHz, respectively. After changing the capacitor value to 300fF, the 50MHz cutoff frequency can be covered, and the minimum cutoff frequency now is 0.72MHz.

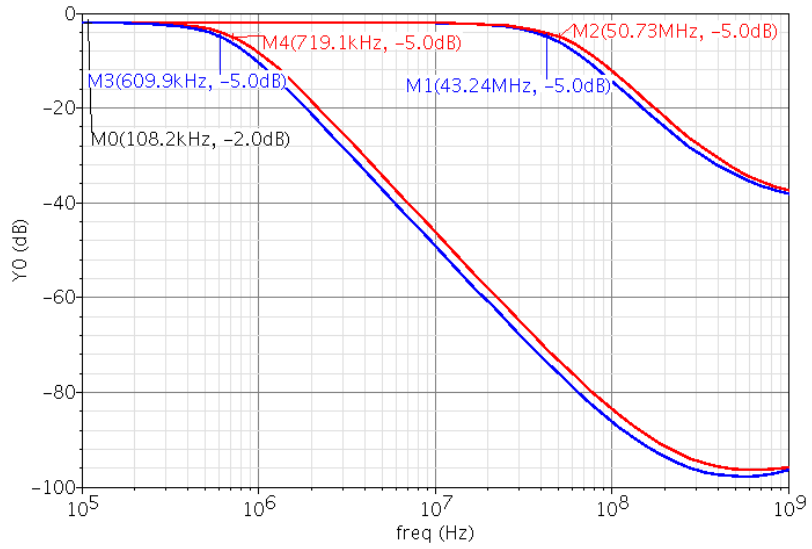


Figure 4.9: Cutoff frequency calibration by tuning capacitor unit ΔC

B). AC simulation

Spectre AC simulation results for the flexible filter are shown in Fig. 4.10. The frequency range is divided into four subsections according to the different capacitor values for the low noise consideration. Capacitor values are increased several-fold from Fig. 4.10(a) to Fig. 4.10(d), while Gm tuning is utilized to cover the required frequency

range. Due to this tuning algorithm, frequency steps are different for each frequency subsection, i.e., frequency steps are around 0.78MHz, 0.39MHz, 0.26MHz and 0.2MHz from Fig. 4.10(a) to Fig 4.10(b), respectively.

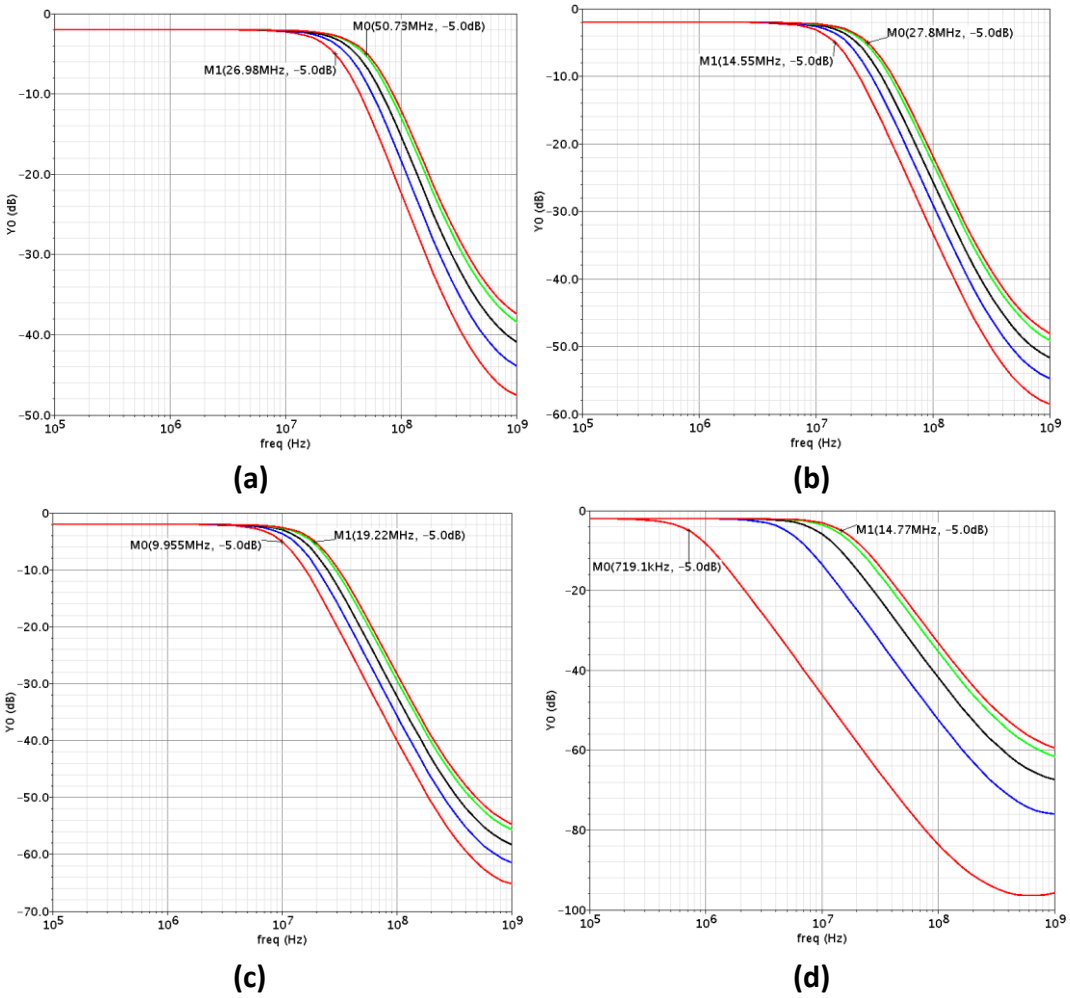


Figure 4.10: Flexible filter bandwidth simulation by tuning Gm when the values of the two capacitors are (a) kept unchanged, (b) doubled, (c) tripled, (d) quadrupled.

In addition, this flexible biquad enables filter quality factor (Q) tuning because the capacitors are tunable. Fig. 4.11 presents one example when the filter pole frequency is 14.51MHz. The filter quality factor can be tuned to 0.35, 0.7 or 1.4.

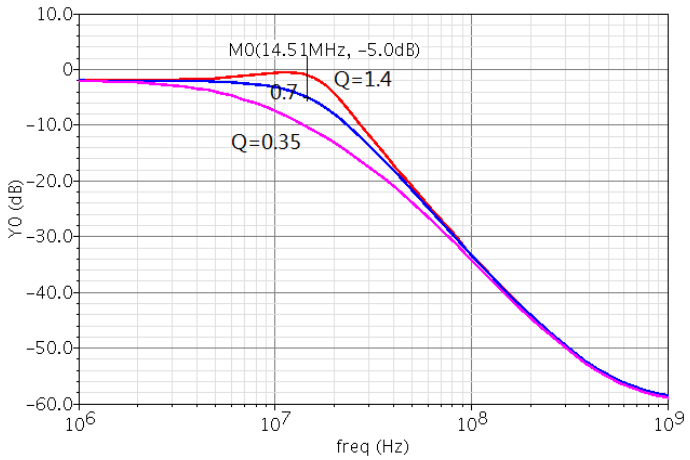


Figure 4.11: Flexible filter quality factor (Q) tuning.

C). IRN simulation

The input integrated noise simulation for the filter is shown in Fig. 4.12. As expected, the noise curve shows a step change with frequency due to the capacitor tuning. For each of the segments the integrated noise goes up because G_m is decreased. However, the worst-case happens when the filter cutoff frequency changes from 14.5MHz to 0.72MHz, where the corresponding integrated noise increases dramatically from 17.09 μ V to 31.27 μ V. Two reasons leads to the high noise at low frequency: one is the high thermal noise from smaller G_m for a smaller bandwidth, and the other is high flicker noise due to small transistor size at smaller G_m.

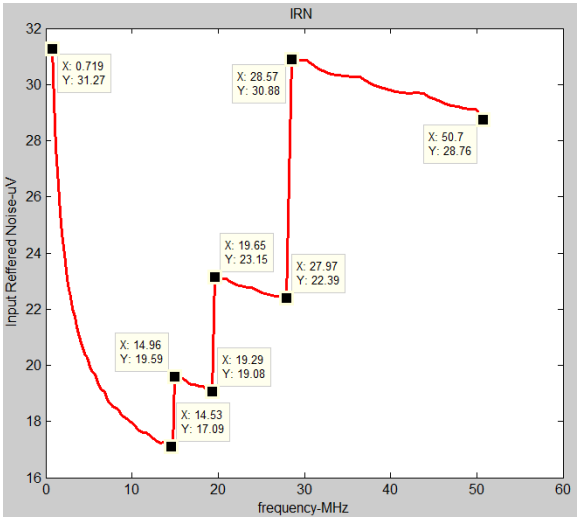


Figure 4.12: Filter input integrated noise (μV) at different filter bandwidths.

D). In-channel linearity simulation

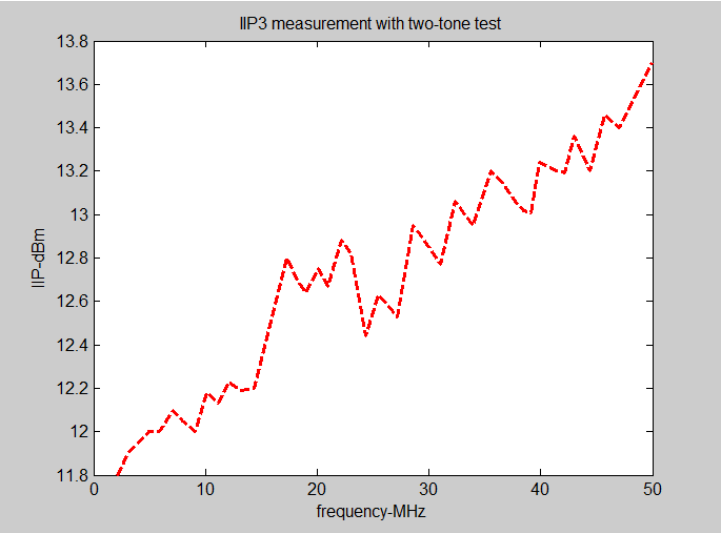


Figure 4.13: Flexible filter IIP3 versus cutoff frequency with two-tone test frequency at the middle of the filter frequency. The two-tone spaces used are 100 kHz, 500 kHz and 1 MHz for frequency ranges of below 1MHz, 10MHz and 50MHz, respectively.

A figure plotting IIP3 as a function of frequency is shown in Fig. 4.13. IIP3 is measure using the two-tone test with the frequency located at the center of the filter cutoff frequency. According to this simulation result, IIP3 of this flexible filter is between 12dBm and 14dBm.

4.2 Out-of-channel linearity

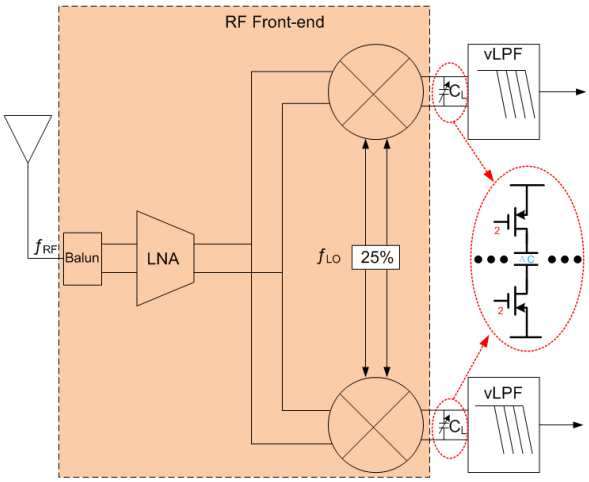


Figure 4.14: Zero-IF RF front end with large capacitor CL as the load of the mixer to realize the filtering ability.

As illustrated in chapter 3, the poor out-of-channel linearity of this voltage-mode filter

must be addressed. The out-of-channel blockers need to be attenuated sufficiently before entering the baseband section. Therefore, stages in front of the LPF are required to supply filtering. Based on the zero-IF RF front end, we can use the structure shown in Fig. 4.14 to perform the filtering. Capacitor C_L is used to load the mixer. In this section, we will discuss how the filtering function is realized.

4.2.1 LNA with cross-coupled capacitor technique

Usually, common-source and common-gate stages are widely employed in LNA design. Compared with the common-source LNA, the common-gate LNA can show better linearity and can be impedance matched more easily at the input but suffers from higher noise. When just considering the channel thermal noise, the noise figure *NF* of the common-gate LNA under impedance matching is given by (4.9) [33]

$$\mathrm{NF}_{\min} = 1 + \frac{\gamma}{\alpha}, \tag{4.9}$$

where γ is the transistor channel thermal noise coefficient and α is a bias-dependent parameter. In the case of short channel device with $\gamma / \alpha = 2$ [33], NF_{min} of the common gate stage is 4.8dB, which is 3dB higher than the common-source stage. Usually, noise figure of the common-gate stage can be reduced by increasing the transistor transconductance, g_m. However, we cannot change g_m arbitrarily because of impedance matching considerations. The tight link between noise and impedance matching prevents us from achieving a NF less than 3dB.

One technique to reduce the NF of the common-gate stage has been developed, named the capacitive cross-coupling technique [34, 35]. In this design, noise matching and impedance matching are separated, thus, a low NF is available with reasonable impedance matching (S11<-10dB). In our design, a differential common-gate stage with cross-coupled capacitors LNA is utilized, as shown in Fig. 4.15. C_0 is the cross-coupled capacitor, M_2 and M_4 are used for higher gain and isolation between the input and output nodes.

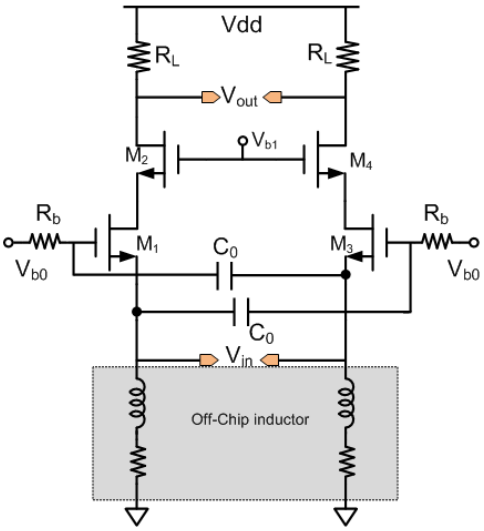


Figure 4.15: Common gate input low noise amplifier using capacitor cross-coupled technique to decrease the noise figure (NF).

Since the design details of the LNA is not this thesis's objective, we thereby give the biasing and performance directly (design procedure is in Appendix A), as listed in table 4.4, from which, we can see that, this topology shows good noise performance and linearity.

Table 4.4: LNA parameters

LNA biasing								
V[V]			R[Ω]		C[fF]	W/L [um/um]		G_m [mS]
V_{dd}	V_{b1}	V_{b0}	R_b	R_L	C_0	$M_{1,3}$	$M_{2,4}$	17.57
2	1	0.5	5k	480	500	41.44/0.12	40/0.12	
LNA performance @1GHz								
S11[dB]	S21[dB]		NF[dB]		IIP3 [dBm]	1dBcp [dBm]		Power [mW]
-11.78	21.05		1.86		5	-7.68		3.3

4.2.2 Switching pair passive mixer

Two reasons contribute to the decision of using a passive mixer instead of its active counterpart. From the linearity perspective, passive mixers show better linearity. Also, a passive mixer does not suffer from flicker noise since there is no DC-current flowing through the transistors [36]. Fig. 4.16 presents a typical passive mixer with capacitor C_L as the load, consisting of two switching pairs. Rail-to-rail square-wave local oscillator (LO) signals with a duty-cycle of 25% are used for quadrature mixing in the I/Q channels. Notice that a large transistor size is required to reduce the on resistance of

the switching pair.

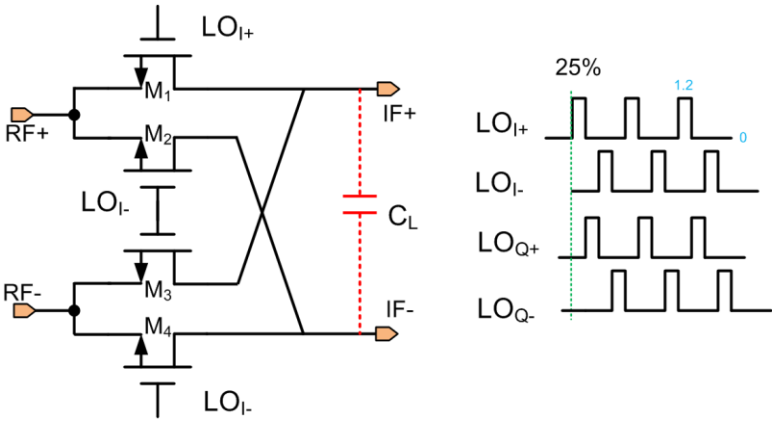


Figure 4.16: Switching pair passive mixer driven by large amplitude local oscillator (LO) signals with duty cycle of 25%.

One feature of the passive mixer is its impedance transformation [37] as illustrated in Fig. 4.17. Baseband impedance $Z_{BB}(s)$ is shifted to the RF frequency when looking into the input nodes of the passive mixer $Z_{in}(s)$, where R_{on} is the switch on resistance.

$$Z_{in}(s) = R_{on} + \frac{2}{\pi^2}[Z_{BB}(s - j\omega_0) + Z_{BB}(s + j\omega_0)]. \text{ [37]} \qquad (4.10)$$

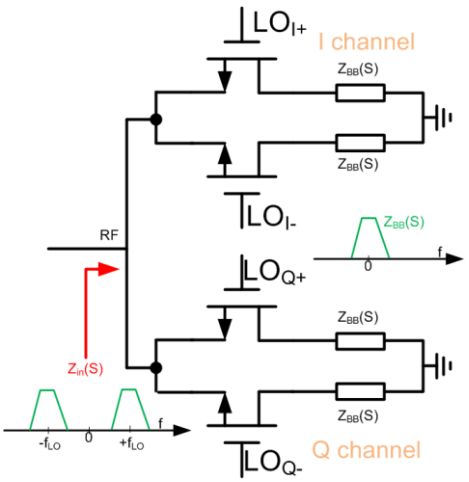


Figure 4.17: Passive mixer impedance transformation diagram

In our case, $Z_{BB}(S)$ consists of the capacitance from C_L and the input parasitic capacitance of the LPF. After transformation, one real pole is generated centered at the RF frequency, which can be used to attenuate the out-of-channel interferes. If C_L is tunable, then we can vary the pole's position for multi-standard applications.

To sum up, Table 4.5 presents the biasing parameters of the mixer (design procedure is in Appendix B), and in next section, co-simulation will be done with tunable C_L.

Table 4.5: Mixer parameters

Mixer biasing			
V_g [v]	LO [v]	W/L [µm/µm]	DC current [µA]
1.2	1.2	20/0.12	0

4.2.3 Simulation result

Using the test bench of Fig. 4.14 and the biasing parameters of tables 4.4 and 4.5, the simulation result with a tunable C_L is shown in Fig. 4.18. Two typical simulation results are given with C_L=1pF and C_L=32pF. It is can be seen from the graph that the blocker located at 10MHz can be attenuated around 9dB in the low channel width case.

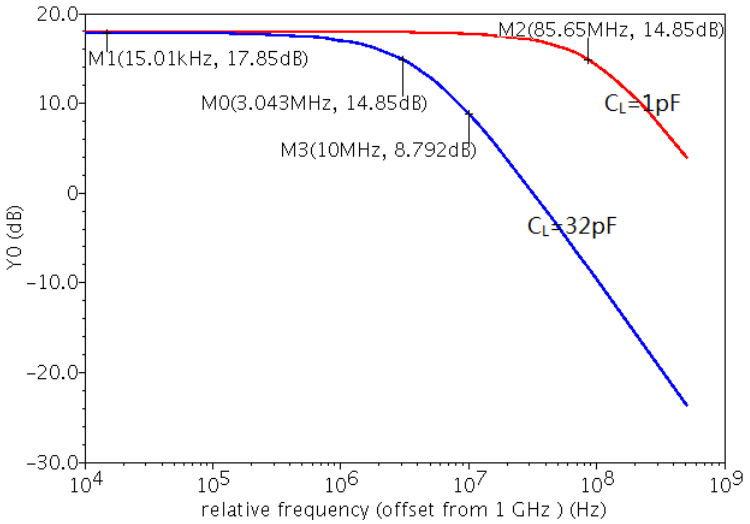


Figure 4.18: Out-of-channel blocker attenuation with CL=1pF (red line) and CL=32pF (blue line).

Finally, in our design, variable capacitor C_L with a maximum value of 32pF is used and controlled by a 5-bit control bus. In one capacitor unit, the PMOS switch size (in Fig. 4.14) is 6um/0.12um for low on-resistance.

4.3 Summary

This chapter focuses on the realization of the flexible voltage-mode filter. Design of the flexible transconductance Gm and capacitor array were discussed in the first section,

followed by the simulation results of noise and linearity. In the second section, we took the advantage of passive mixer's impedance transformation feature to introduce one pole before the signal entering the baseband to attenuate the out-of-channel blockers In order to cope with filter's low out-of-channel linearity problem.

Chapter 5

Top-view, layout and post-layout simulation results

In this chapter, the noise figure simulation result for the entire receiver is presented in the first section, followed by the layouts and post simulation results of the zero-IF RF front-end with the low pass filter.

5.1 Receiver noise figure simulation

A top-level schematic of the zero-IF receiver with I/Q modulation is shown in Fig. 5.1.

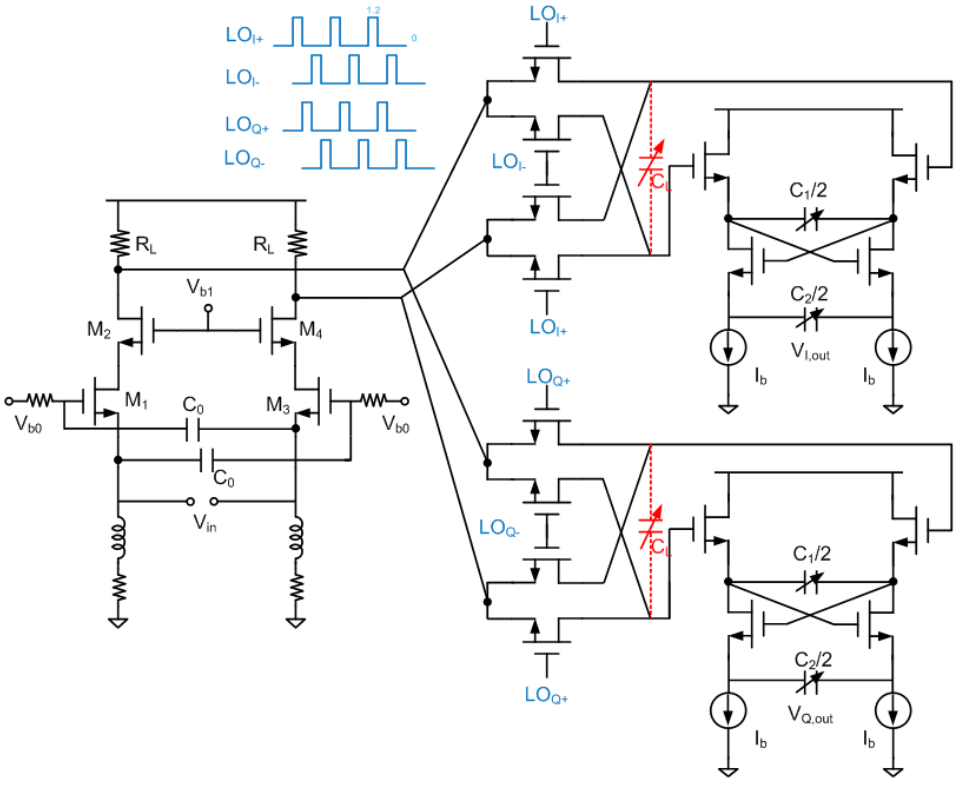


Figure 5.1: Receiver schematic

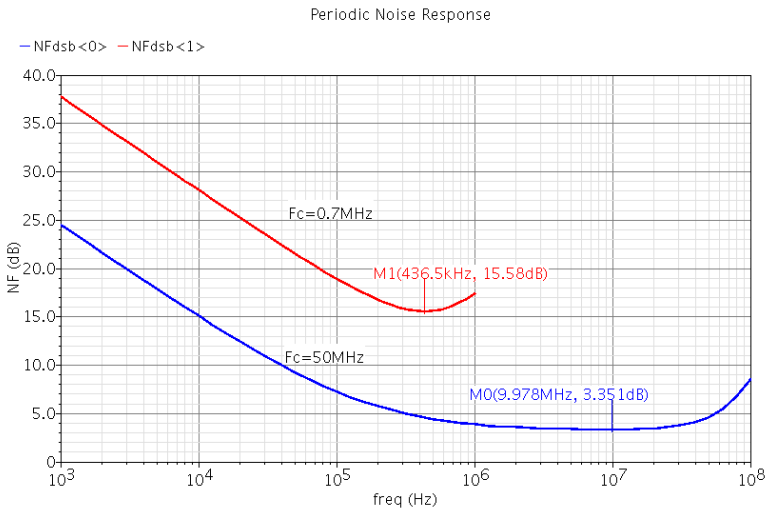


Figure 5.2: Receiver noise figures at filter bandwidths of 0.7MHz and 50MHz.

The receiver noise figure is simulated at two frequency points: 50MHz (blue line) and 0.7MHz (red line). The result is shown in Fig. 5.2, from which, the receiver noise figures at the filter bandwidths of 0.7MHz and 50MHz are 15.5dB and 3.35dB, respectively.

According to the simulation results, the receiver shows very poor noise performance at 0.7MHz. When checking the Spectre spot noise simulation, we find the rise of the flicker noise results in the high NF. Therefore, future efforts are required to solve this problem.

5.2 Layout and post simulation result

Physical layouts of the filter and the entire receiver are presented in this section. Due to our interest is in the flexible filter, processing variation, voltage variation and temperature variation (PVT) simulation is just done in this case.

5.1.1 Filter layout and post-layout simulation result

The layout of one flexible low pass filter is presented in figure 5.3. As can be seen from the layout, the majority of the low pass filter area is occupied by capacitors C_1 and C_2. The total filter size is around 0.38mm×0.3mm. Due to the filter's flexible feature, it is very difficult to do the post-layout simulation at every filter bandwidth. Therefore, post-layout simulation results including the filter bandwidth, linearity and noise are

checked at only the maximum filter bandwidth of 50MHz.

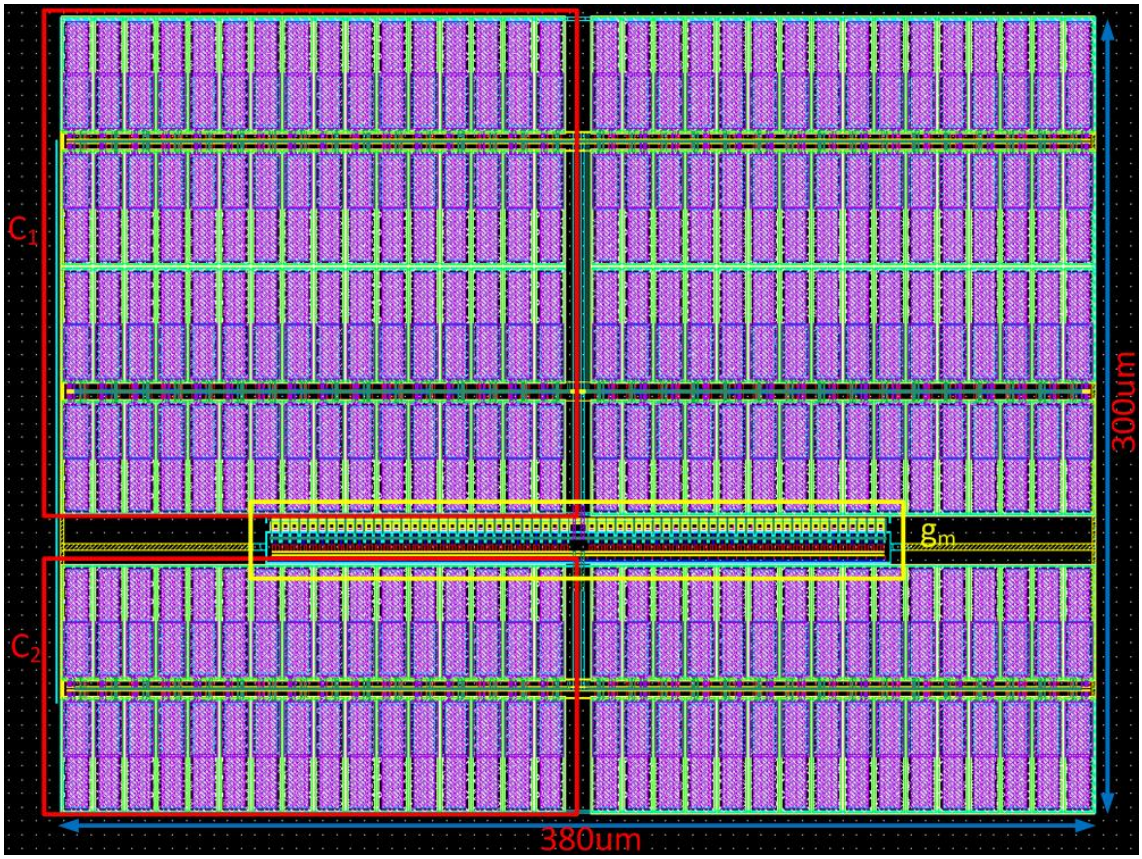


Figure 5.3: Flexible low pass filter layout

Table 5.1 presents the simulation results of the flexible filter, including the schematic simulation and post-layout simulation results. Since no PMOS transistors are used in our circuit, processing, supply voltage and temperature (PVT) simulations are performed at three processing corners: FF, TT and SS.

Table 5.1: PVT simulation results for schematic and layout

	Process corner	V_{DD} [V]	Temp [°C]	V_{O_DC} [mV]	G_m [mS]	Gain [dB]	BW [MHz]
Schematic	FF	1.32	0	373	6.66	-2.11	66.79
	TT	1.2	27	354	5.0	-2.0	50.72
	SS	1.08	80	330	2.86	-1.99	29.83
Layout	FF	1.32	0	377	×	-2.11	61.06
	TT	1.2	27	356	×	-2	47.22
	SS	1.08	80	331	×	-1.99	28.39

5.1.2 Total receiver layout

The total layout including the LNA, Mixer and the LPF (with I/Q channels) is present in Fig. 5.4. The total layout area is 0.76mm×0.43mm.

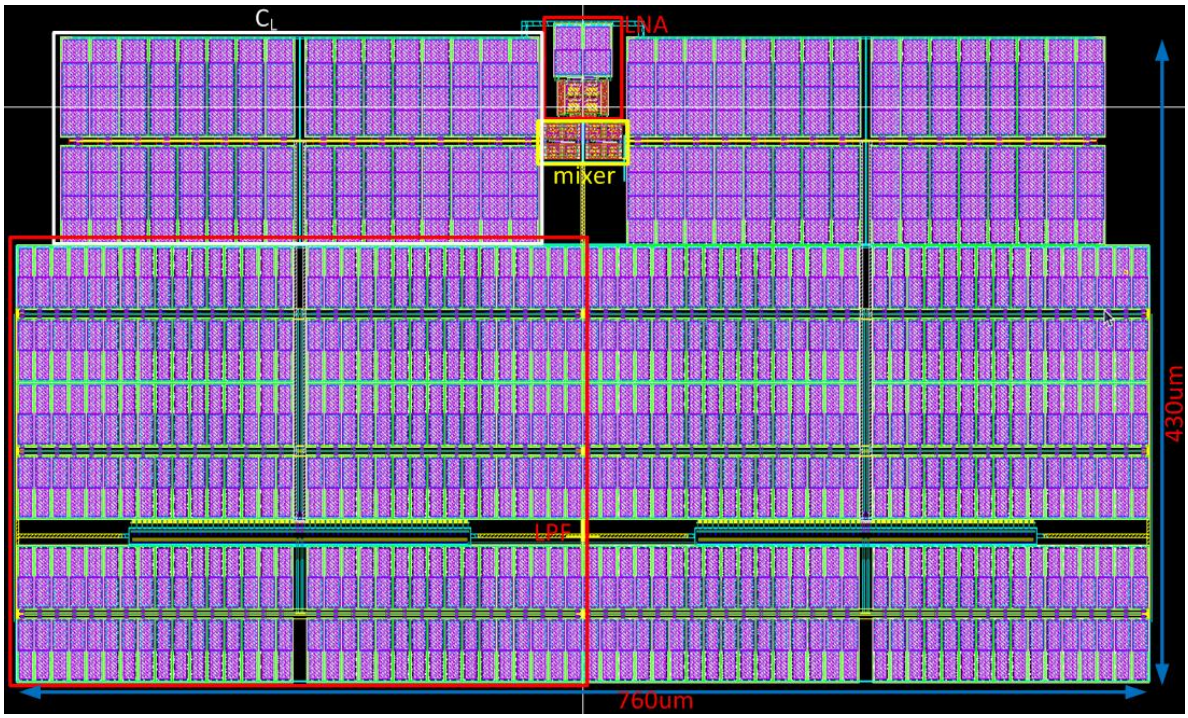


Figure 5.4: Total layout including the zero-IF RF front end and the low pass filter

5.3 Summary

In order to get a general idea about how is this design, we compare the achieved filter parameters with the objectives set in chapter 1, as shown table 5.2.

Table 5.2: Performance comparison with the objectives

	Objectives	Achieved
Supply voltage [V]	1.2	1.2
Variable bandwidth	0.7MHz-50MHz	0.7MHz-50MHz
In-channel IIP3 @ BW/2	>20dBm	13.7dBm
Out-of-Channel linearity	10dB	9dB
IRN density	2 nV/√Hz	3.4 nV/√Hz
DR @ [THD=-40dB]	>60dB	78.5dB
Power	A few mW	0.847mW
Maximum capacitor value	<50pF	38.4pF

It is clear that the designed filter cannot achieve the objectives of linearity and input referred noise density. Nonetheless, it is a good filter because of its high dynamic range,

low power and small chip size.

Table 5.3 also compares this work with some other similar designs published in the recent literature.

Table 5.3: Performance comparison with the similar designs

	[27]	[38]	This work
Technology	0.13um	0.18um	0.13um
Filter order	2nd	2nd	2nd
Supply voltage [V]	1.2	1.2	1.2
Variable bandwidth	100KHz-20MHz	100KHz-20MHz	0.7MHz-50MHz
IIP3 @ BW/2 [dBm]	>20dBm	>20dBm	13.7dBm
IRN[μV_{rms}]	36	55	29
DR @ [THD=-40dB]	68dB	66dB	78.5dB
Power	14.2mW	0.95mW	0.847mW

As can be seen from this table, our design shows several advantages: (1) a wide frequency tuning range of from 0.7MHz to 50MHz, (2) a smallest input referred noise of 29µV, (3) the highest dynamic range of 78.5dB, and (4) the lowest power consumption of 0.847mW. However, relative low linearity of 13.7dBm is its main disadvantage.

Chapter 6
Conclusions and Recommendations

This thesis focuses on how to design a flexible low pass channel filter with high linearity, low input referred noise and low power consumption, to be utilized in the LTE-Advanced mobile systems. Hereby, we draw some conclusions in this last chapter. Some suggestions are proposed for future work to improve the performance of the designed filter.

6.1 Summary

This thesis starts with the design motivation introduced in chapter 1. Due to the high channel bandwidth requirement in the upcoming 4G systems, flexible low pass filter with the maximum bandwidth of 50MHz is desired for the channel filter in the baseband section. Apart from that, High linearity, low input referred noise and low power are three main specifications when designing one channel filter.

In chapter 2, some pre-required theories about the channel filter design were reviewed, including the zero-IF structure, analog baseband section, LNA, passive mixer and filter. A G_m-C type channel filter is desired for wide channel bandwidth systems, such as the LTE-Advanced system, but it suffers from low linearity and high power consumption. To improve the filter linearity, some Gm linearization techniques are required.

In order to design a high performance channel filter, two low pass filters distinguished by their working modes: voltage-mode and current mode were considered. A detailed analysis followed by simulation results carried out in the 130nm UMC technology shows that each type has its own advantages and drawbacks. Finally, the voltage-mode filter was selected due to its high dynamic range (78.3dB) compared with its current-mode counterpart (68.5dB), although it suffers from poor out-of-channel

linearity. In addition, two receiver topologies for these voltage and current mode filters were given in the last section of chapter 3.

Using the selected filter structure in chapter 3, we made the filter flexible in chapter 4. MOS transistors are used as switches with a large size for low on resistance. Based on tuning the flexible transconductance G_m as well as capacitor array, the influence of switches' finite on-resistance upon the filter performance were also studied. To cope with the low out-of-channel linearity, we took advantage of the passive mixer's impedance transformation to attenuate the potential blockers before they enter the low-pass filter.

The receiver layout and post-layout simulation results were shown in chapter 5. The receiver noise figure at filter bandwidth of 0.7MHz is poor due to the high transistor flicker noise. PVT simulation result also show that filter parameters are sensitive to the processing corners, supply voltage and temperature variations.

6.2 Recommendations

In order to improve the filter's performance, some suggestions are proposed to cope with the flicker noise and G_m variation issues. A modified filter structure for better out-of-channel linearity is also discussed in this section.

6.2.1 Flicker noise problem at lower bandwidth

Based on the simulation result and analysis from Fig. 4.12, some efforts need to done to cope with the high input integrated noise problem in the case of smaller filter bandwidth. Since the majority of the noise comes from flicker noise, one effective way is to use a larger transistor size to decrease the noise. Therefore, in a future design, one suggestion is to use a few large transistor size transconductance units at the low filter bandwidth. However, the disadvantage is the larger capacitance caused by the increasing transistor size, which may introduce a zero in the filter response.

6.2.2 G_m control circuit

According to the PVT simulation results, an extra g_m control circuit is required to help us obtain the designed filter cutoff frequency. Several types of g_m tuning circuits are discussed in [21, 24, 39, 40]. The circuit used in [40] is recommended due to its simplicity.

6.2.3 Proposed structure for high linearity

One main drawback of the voltage-mode filter is that it suffers from decreasing in-channel linearity as well as low out-of-channel linearity. Therefore, we propose one structure to improve the linearity performance as shown in Fig. 6.1, which is obtained by substituting the input transistors with two resistors (R), whose value equal $1/g_m$. The proposed filter now has a resemblance to the active-R *Gm-C* filter.

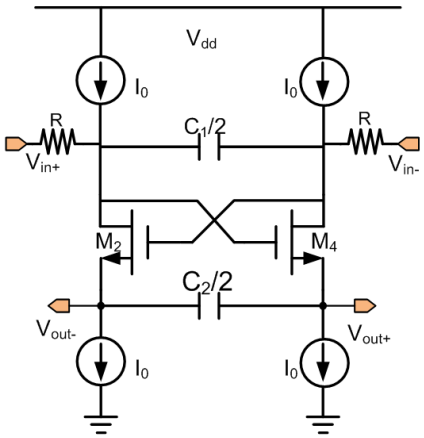


Figure 6.1: Modified voltage mode filter with input transistors substituted by two resistors R, where R=1/gm.

Under the same biasing conditions, linearity including the in-channel linearity and out-of-channel linearity were simulated for this modified filter. The in-channel linearity simulation result is shown in Fig. 6.2.

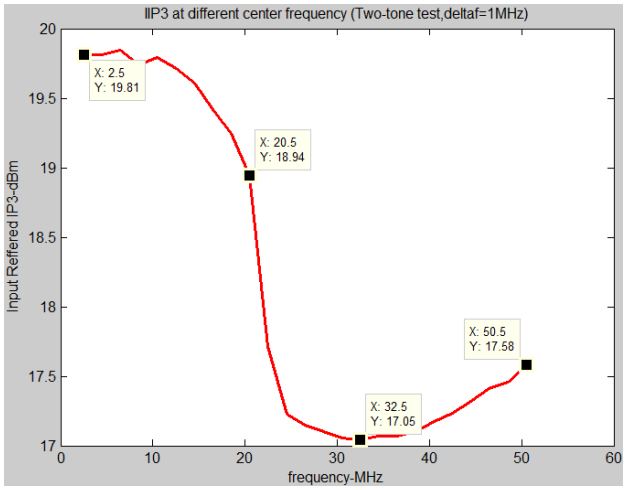


Figure 6.2: Modified structure IIP3 two-tone test with a frequency spacing of 1MHz

Although the linearity degrades with increasing frequency, the minimum IIP3 is 17.05dBm at 32.5MHz, which is much better than that of the previous voltage-mode structure. This modified filter also shows a better out-of-channel linearity. A linearity of 21dBm is achieved with one input signal frequency at 100MHz and the other at 190MHz.

Although better linearity can be achieved using this modified structure, future work is still needed to cope with the following problems: (1) a common mode feedback circuit is required for this modified filter, and (2) an input buffer stage with high linearity is needed since the input impedance decreases, as shown in Fig. 6.3.

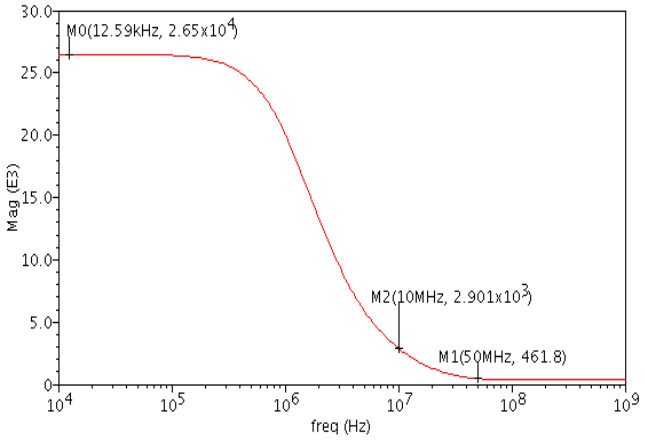


Figure 6.3: Input impedance characteristic of the modified structure of Fig. 6.1.

Appendix A
LNA Design

Since the zero-IF test bench used in this work is just for testing the filter purpose, there are no exact specifications for the LNA and mixer. Table A.1 list the general requirements of the LNA, and all its parameters are listed in Fig. A.1. We will briefly discuss its design procedure in this appendix.

Table A.1: LNA general specifications

LNA Performance @1GHz				
S11[dB]	**S21[dB]**	**NF[dB]**	**IIP3[dBm]**	**Power [mW]**
<-10	**~20**	**<2**	**--**	**as small as possible**

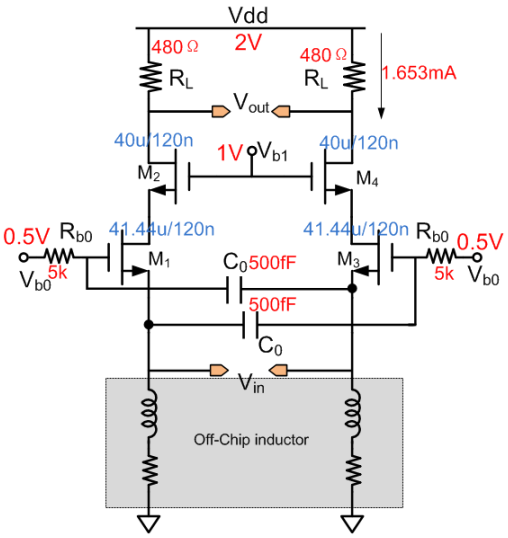


Figure A.1: LNA circuit with all parameters

A.1 DC biasing

Minimum channel length transistors are used in this LNA for speed and low parasitic capacitance consideration. The threshold voltage V_{th} in this case is around 380mV, and the biasing voltage of V_{b0} and V_{b1} are fixed at 0.5V and 1V, to biasing the transistor at a overdrive voltage of 0.12V. Supply voltage in this circuit is 2V.

A.2 Input matching and noise matching

Compared to the normal common-gate stage, the main advantage of this capacitive

cross-coupling LNA is its low NF [33]. Noise figure is changed from equation (A.1) to be (A.2).

$$\mathrm{NF} = 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_S} \tag{A.1}$$

$$\mathrm{NF} = 1 + \frac{\gamma}{\alpha}\frac{1}{(1+A)^2 g_m R_S}, \tag{A.2}$$

where γ, α, g_m and R_s represent the channel thermal noise coefficient, bias-dependent parameter, the transistor transconductance and source impedance, respectively. And A= C_0/ C_0+C_{gs}. Larger C_0 is beneficial to low noise and power. In this work, a C_0 of 500fF is used.

The requirement of S11 less than -10dB indicts that perfect input matching is unnecessary. According to the simulation result, S11 of -11.78 is obtained at 1GHz when the transistor widths are 40µm and 41.44µm for M_2, M4 and M_1, M3, respectively. The corresponding transconductance and the current are 17.57mS and 1.653mA, respectively. Finally, In order to make sure the output voltage is 1.2V, which is the LPF DC input, a load resistance of 480Ω is obtained.

A.3 Simulation result

The simulation results of the LNA are shown in Fig. 4.2 and Fig. 4.3. As can be seen from these two graphs, general specifications are achieved.

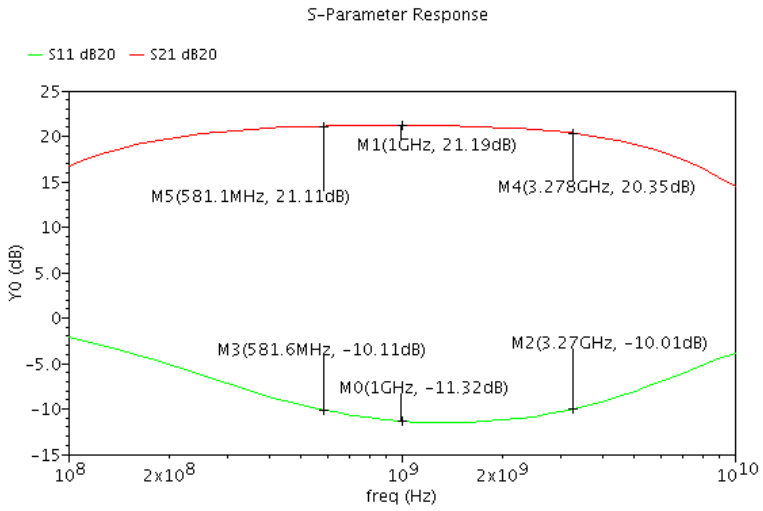


Figure A.2: S-parameter simulation results: the red line represents the S21, and the green line is the S11.

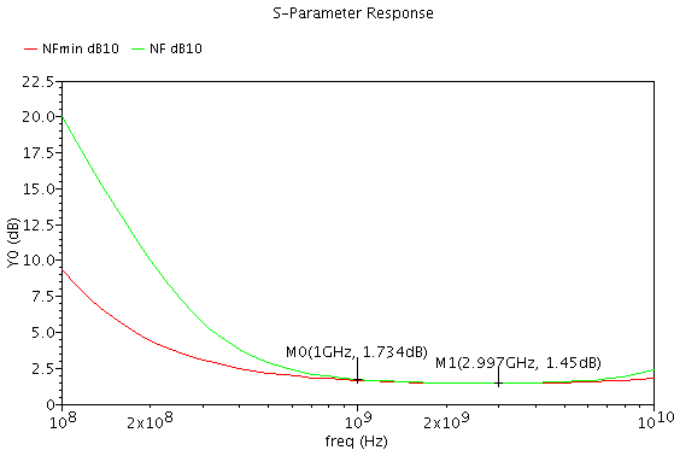


Figure A.3: Noise figure simulation results: red curve is the minimum noise figure, and green one is the noise figure.

Appendix B
Mixer Design

A passive mixer consists of four large MOS transistors, as shown in Fig. B.1. A proper design requires that the MOS transistor has a very low on-resistance at the on-state, while can be completely turned off at the off-state. Therefore, large size transistor and amplitude driving signal are desired.

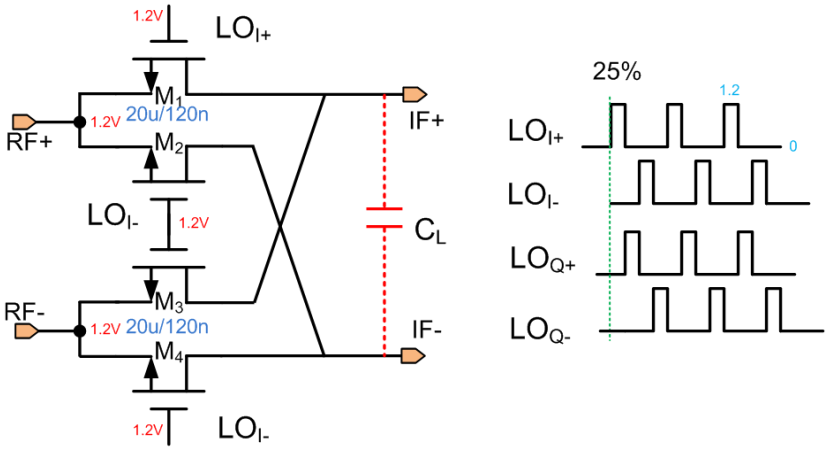


Figure B.1: Mixer circuit with all parameters

Thus, a biasing voltage of 1.2V for the transistor gate is selected, where each transistor has an overdrive voltage of 0V. And the transistor width of 20µm is used according to the on-resistance simulation, which is not shown here.

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