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A Wideband Two-Way Digital Doherty Transmitter in 40nm CMOS

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***Abstract*— A 40nm CMOS wideband digital Cartesian push-pull inverted Doherty operating in class-E is presented. Wideband Doherty operation is achieved over a 1.9-to-3GHz frequency band, using an off-chip power combining network. The fully digital transmitter (DTX) provides 25.3dBm peak power with a drain/DTX line-up efficiency (DE/SE) of 58.7%/44.9%, respectively, at 2.4GHz. When operated with a 160MHz 256-QAM OFDM signal, it achieves 46.1%/32.7% average DE/SE, with an ACLR and EVM better than -40.6dBc and -33.9dB, respectively, using a simple memory-less digital pre-distortion (DPD).**

***Keywords*— Cartesian, class-E, Doherty, efficient, wideband, digital power amplifier, RF-DAC, DPD, DTX, Balun, CMOS.**

I. Introduction

To fully benefit from the progress in nanoscale CMOS technology, digital transmitters (DTXs) receive high interest due to their potential to achieve excellent TX-system efficiencies while handling modern wideband modulated signals with high peak-to-average power ratios (PAPR). The most promising DTX architectures use arrays of controlled digital PA (DPA) cells in a polar or Cartesian configuration. In a polar DPA realization [1], [2], the nonlinear Cartesian to polar data conversion yields a notorious bandwidth expansion. This drawback, combined with the requirement that the phase and amplitude paths must perfectly recombine without any delay mismatch at the output stage to replicate the original signal at RF, limits the maximum achievable modulation bandwidth for practical polar-TX implementations. In contrast, Cartesian DTXs do not suffer from these drawbacks due to their linear I and Q summation, making them attractive for wideband applications [3]. The high PAPR of modern communication signals compel a DTX to operate in deep power back-off (PBO), degrading its average efficiency if no efficiency enhancement technique is applied. A Doherty topology can provide this efficiency enhancement at low complexity while handling wideband complex modulated signals [2]–[5]. In this regard, utilizing a low-loss off-chip Doherty power combiner increases the overall system efficiency, especially in PBO [4], [6]. This paper presents a wideband energy-efficient Cartesian inverted push-pull two-way Doherty DTX employing a reactance compensated parallel-circuit class-E DPA. The off-chip Marchand balun-based Doherty power combiner uses re-entrant coupled lines with independent second-harmonic control.

II. Design of a Wideband Doherty Cartesian DTX

The proposed wideband Doherty Cartesian DTX comprises two Cartesian DTX chips and an off-chip power combiner operating over a 1.9-to-3GHz frequency band.

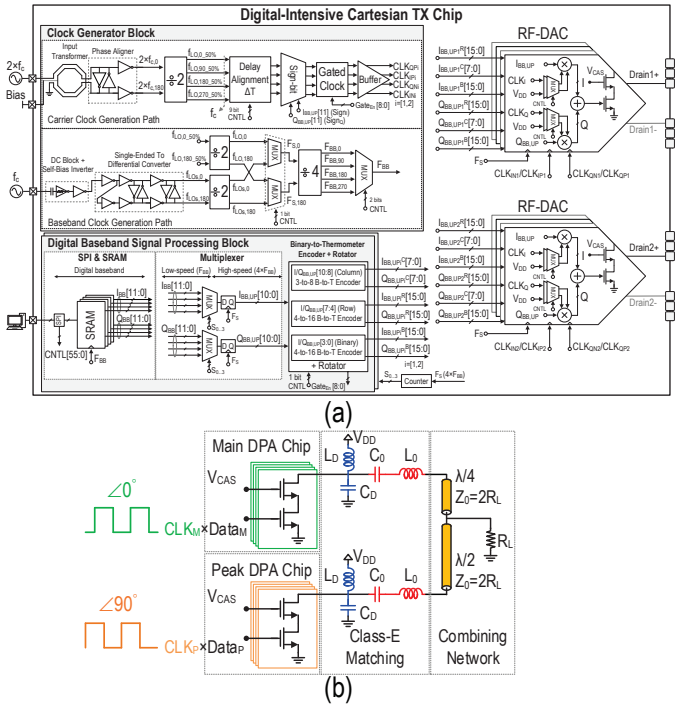

Fig. 1. (a) Detailed block diagram of the DPAs. (b) Single-ended representation of the push–pull class-E Doherty DPA.

A. CMOS Digital Cartesian Class-E DPA

Fig. 1(a) exhibits the implemented chip's block diagram [7]. The baseband I/Q signals are upsampled by a factor of 4 using four parallel time-multiplexed SRAMs. The 50% quadrature clocks at f_C, needed for the I/Q upconversion and the implementation of the Doherty phase relations, are generated using a (single-ended) external reference clock at $2\times f_C$, which is fed to an on-chip transformer followed by a divider. A 4-bit phase aligner is optionally utilized to fine-tune the clock phases, followed by an I/Q sign-bit mapper that utilizes 50% quadrature clocks [3]. A data-aware clock-gating circuitry is employed to reduce power consumption at PBO. An additional sampling clock generated from another off-chip clock source can be optionally employed to set the baseband modulation bandwidth independently. At the DTX chip frontend, there are two RF digital-to-analog converters (RF-DAC), comprising 4-bit binary (LSB) and 7-bit unary (MSB) segmented sub-cells, each consisting of a bit-wise NAND upconverter. This chip is combined with

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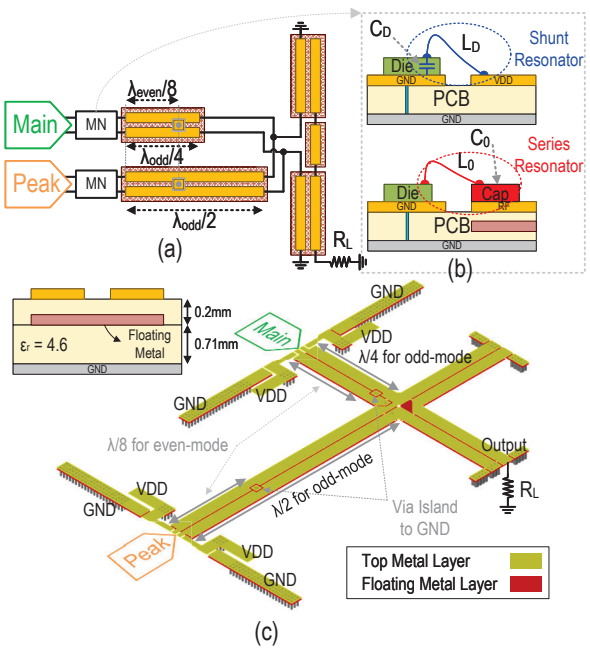

Fig. 2. (a) Doherty combining network structure (b) side view of the shunt and series resonators bondwiring connections (c) realization of the Doherty combining network.

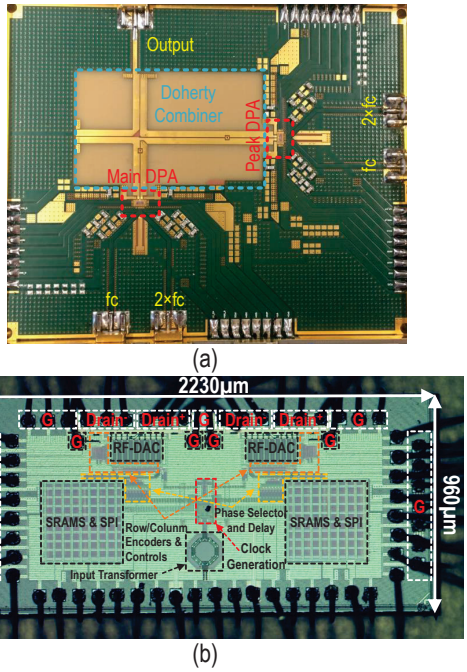

Fig. 3. (a) Fabricated PCB (b) Die micrograph.

an off-chip class-E matching network. Since in class-E, the drain voltage can go up to 2-to-3 times the supply voltage, a cascode power cell topology is exploited in this design to prevent reliability issues. The single-ended representation of the push-pull class-E DPA matching network topology with finite DC-feed inductance is shown in Fig. 1(b). This structure, known as parallel-circuit load insensitive class-E, has a higher maximum operating frequency and higher load resistance [8]. To perform a wideband RF operation, the load reflection coefficient angle seen by the intrinsic drain should remain constant over the required bandwidth. This feature accomplishes through reactance compensation [9]. By properly choosing the parameters of the series resonator (L_0, C_0), a constant load reflection coefficient angle over a wide frequency band can be achieved, resulting in a wideband RF operation.

B. Wideband Doherty Power Combining Network

1) Compensated Impedance Inverter

To widen the bandwidth of the conventional Doherty amplifier, an inverted Doherty topology is used in a push-pull configuration [4], as shown in Fig. 2(a). In the inverted Doherty approach, the additional $\lambda/2$ transmission line (TL) in the output of the peak amplifier compensates for the considerable variation of the magnitude and phase of the impedance seen by the main amplifier over frequency.

2) Compensated Marchand Balun With Re-entrant Coupled Lines and Second-Harmonic Control

The push-pull inverted Doherty DPA is connected to a Marchand balun to form the wideband balanced-to-unbalanced operation of the power combiner. The layout of the Marchand balun adopted from [4] is shown in Fig. 2(b). Tight differential coupling with a high even-mode impedance is required to realize the wideband Doherty load network with sufficiently low impedance. This feature is realized by employing re-entrant type coupled lines with a proper dielectric constant and dielectric layer thickness between and underneath the conductors, yielding a low-loss wideband balun. A well-controlled wideband 2nd harmonic termination for class-E operation can be achieved by utilizing the orthogonality between the fundamental (differential) signal and the in-phase (common-mode) behavior of the 2nd harmonic signals. Consequently, the required open 2nd harmonic for a digital class-E DPA can be realized by providing an even-mode short-circuited condition at $\lambda/8$ distance of the DPAs. Something that can be practically achieved by placing a simple via to ground in the center of the floating center plate conductor. Due to the tight coupling between the three conductors, the top metals are inherently forced to ground for their even-mode signals, thus seen as open-circuit by the DPA at the 2nd harmonic. In the odd-mode, the center of the floating metal is virtually ground, barely affecting the odd-mode impedance levels.

III. Fabrication and Measurement Results

A prototype of the DPA is fabricated in 40nm bulk CMOS (Fig. 3(b)), occupying $2.23\times0.96\text{mm}^2$, including pads and SRAMs. The realized chip is wire-bonded to the off-chip two-way Doherty power combiner (Fig. 2(b)). L_0 indicates bondwires from the drain of the transistors to the off-chip passive combiner. Chip capacitors (C_0) are used to complete the implementation of the series resonator. The DC-feed

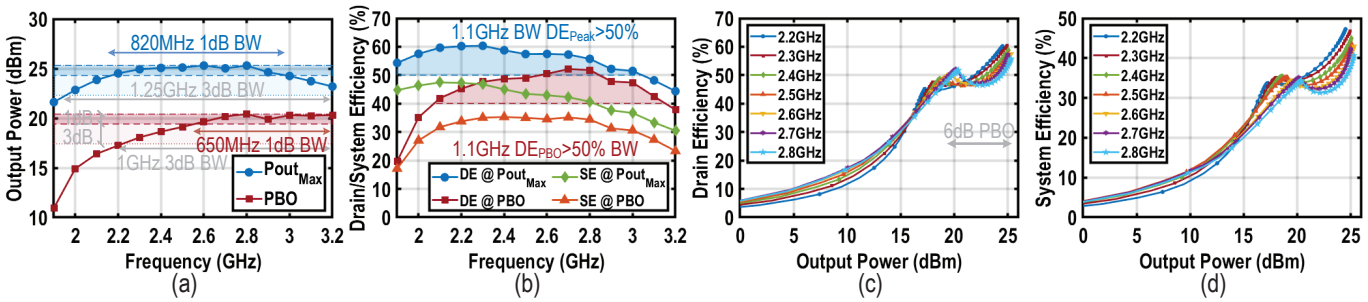

Fig. 4. Measured (a) output power, and (b) drain/system efficiencies at full power and power back-off vs. frequency, (c) drain, (d) system efficiency vs. output power at different frequencies.

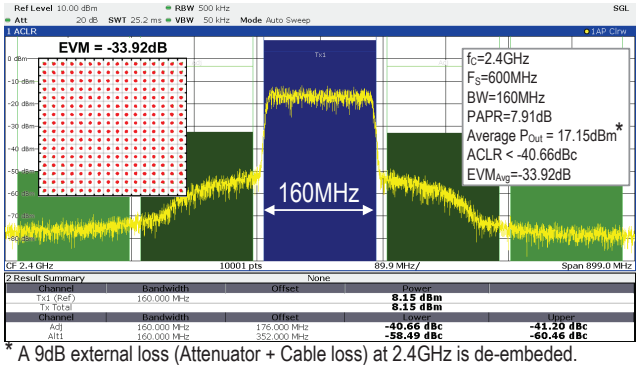

Fig. 5. Measured results of a single-channel 160MHz 256-QAM OFDM signal at 2.4GHz.

inductance L_D, is also implemented using bondwires and connected to the bias lines. The baseband data of each DPA is independently applied to the DTX using four parallel on-chip 1-K SRAMs running at 600MHz. The measured peak and back-off output power over a 1.9-to-3.2GHz range are shown in Fig. 4(a), ranging from 21.6-to-25.3dBm, and 10.9-to-20.4dBm, respectively, operating from a 1.1V supply. The measured peak and back-off drain and system (bits-in-RF-out) efficiency (DE/SE) over the 1.9-to-3.2GHz range are shown in Fig. 4(b). As can be seen, DE at peak power is more than 50% within the 1.9-to-3GHz frequency range. The DE at back-off power is more than 40% over a 1.1GHz span, equivalent to 43% relative bandwidth. The DE and SE are plotted versus output power in Fig. 4(c) and (d), respectively, illustrating a significant efficiency enhancement over the PBO range. Utilizing a simple 2×one-dimensional memory-less DPD, a 160MHz single-channel 256-QAM OFDM signal at 2.4GHz is generated. The average delivered output power is 17.15dBm (8.15dBm plus 9dB loss of attenuator/cable), while the ACLR and EVM are better than -40.6dBc and -33.9dB, respectively. The performance of the proposed two-way DTX is summarized in Table 1. Compared to the DTXs with efficiency enhancement techniques, the proposed architecture exhibits the highest data rate, high average efficiency, and reasonable peak output power, suitable for wireless communication systems.

Table 1. Performance Summary and Comparison with State-of-the-Art Works.

Specifications	This Work	[2]	[3]	[4]	[5]	[6]
Technology	CMOS 40nm	CMOS 28nm	CMOS 40nm	CMOS 40nm	CMOS 65nm	CMOS 65nm
DPA Architecture	Cartesian Class-E	Polar	Cartesian CMCD	Polar Class-E	Analog Doherty	Voltage Mode Doherty
Matching Network	Off-Chip	On-Chip	On-Chip	Off-Chip	On-Chip	Off-chip
Die Area (mm²)	2.1 (0.72 ‡)	4¥	3.55 (1.5 ‡)	0.45	6	1.62
Supply (V)	1.1	1.4	1	0.7	5.5	1.2/2.4
3dB RF Bandwidth	1.25GHz	N/A	1.3GHz	900MHz	800MHz	400MHz
Relative RF BW	52.08%	N/A	24%	36%	13.7%	44.4%
Frequency (GHz)	2.4	2.5	5.4	2.5	5.8	0.9
Peak P_{out} (dBm)	25.3	27	27.4	17.5	27.2	24
DE/SE (%) Peak	58.7 / 44.9	53 / N/A	47.4 / 30.6	54 / 34	N/A / 24.5	N/A / 45
DE/SE (%) 6dB PBO	48.6 / 35.2	33 / N/A	43.4 / 26.3	52 / 25	N/A / 13**	N/A / 34
Modulation scheme	256-QAM OFDM	MCS11	256-QAM OFDM	64-QAM OFDM	256-QAM	256-QAM 802.11ac
Bandwidth (MHz)	160	40	240	32	80	40
PAPR (dB)	7.91	6.9	9.6	N/A	6.3	9
Avg. P_{out} (dBm)	17.15	20.1	17.8	N/A	17	14.7
Avg. DE/SE (%)	46.1 / 32.7	N/A / 28.9	41.2 / 22.1	N/A	N/A / 5.3%	N/A / 22
EVM (dB)	-33.92	-35	-32.2	-48	-34.8	-34.8
ACLR (dBc)	-40.6/-41.2	N/A	-39/-39	-48.5/-48.3	-36.6/-36.3	-40 / -40**
Linearization	Memory-less DPD	Memory-effect DPD	Static DPD	ILC DPD	MGTR+2nd Harmonic	Memory-less LUT

• ** Estimated from reported figures and plots. ‡ Core area. ¥ Area including Digital front end, DPLL, and LB/HB DTX.

IV. Conclusion

A wideband Cartesian push-pull inverted Doherty DTX has been presented. The off-chip power combiner provides wideband Doherty operation over the 1.9-to-3GHz frequency band with 25.3dBm peak output power while maintaining more than 50%/37% drain/system efficiency. Delivering 17.15dBm average output power with 46.1%/32.7% average drain/system efficiency for a 160MHz 256-QAM OFDM signal, the EVM and ACLR performance are better than -40dB and -33dB, respectively, employing a simple DPD.

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