CMOS Bandgap References and Temperature Sensors and Their Applications

CMOS Bandgap References and Temperature Sensors and Their Applications

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PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof. dr. ir. J. T. Fokkema,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen

op dinsdag 11 januari 2005 om 10:30 uur

door

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Published and distributed by: Optima Grafische Communicatie

Pearl Buckplaats 37
Postbus 84115, 3009 CC, Rotterdam
Phone: +31 10 220 11 49
Fax: +31 10 456 63 54

ISBN: 90-9018727-8

Keywords: CMOS technology, substrate bipolar transistors, temperature sensor, bandgap reference, voltage-to-period converter, three signal auto-calibration, dynamic element matching.

Printed in The Netherlands

For Xiujun

For my children

For my parents

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Chapter 1 Introduction

1.1 Silicon Temperature Sensors and Bandgap References

Silicon temperature sensors and bandgap references have been developed for a long time, together with the development of semiconductor industry. The semiconductor temperature sensors take a large part of the temperature-sensors market. There are several types of semiconductor temperature sensors: thermistors, which use the resistive properties of a semiconductor composite (consisting of different types of metal) to measure temperature; semiconductor thermocouples, which use a very large Seebeck effect to measure temperature differences; and temperature sensors based on diodes or transistors, which use the temperature characteristics of junctions. Thermistors need specific fabrication processes. As single sensing elements, thermistors and silicon thermocouples are widely used in the industry for measuring temperature and temperature difference, but they need extra interface circuitry for signal processing and data display. For users, it is much easier to have temperature sensors employing the temperature characteristics of junctions integrated with the interface circuit on the same chip. Because the junctions are part of the basic components of the integrated circuit, no effort is needed for process compatibility. In such smart temperature sensors, the temperature behaviour of the junction characteristics is applied to generate the basic sensor signal.

Presently, the most frequently used semiconductor materials are silicon (Si), germanium (Ge) and gallium arsenide (GaAs). Compared to Ge and GaAs, silicon has many advantages. Firstly, silicon is one of the most abundant elements on earth. Secondly, as a good isolator, SiO_2 is used as carrier for the interconnecting metallization and ensures excellent passivation of the surface. Thirdly, the band gap of silicon is 1.12 eV, higher than that of germanium (~0.72 eV), so the maximum operation temperature of silicon is 200 °C, while that of germanium is only about 85 °C. For these reasons, most semiconductors are produced in silicon.

For the design of bandgap references, the temperature behaviour of junctions is also applied, but in a different way. For temperature sensors, the temperature dependence of the output signal must be maximized, in order to get larger temperature sensitivities. For bandgap references, on the other hand, the temperature dependence of the output signal must be minimized, in order to get a temperature-independent output whose value is related to the bandgap energy of the semiconductor material. The temperature behaviour of the junctions determines the performance of the temperature sensors and bandgap references.

1.2 Why CMOS Technology?

Bipolar technology was originally developed for commercial IC products. Many types of integrated temperature sensors and bandgap references have been on the market, for instance, the temperature-sensor series LM135 [1.3], the AD590 series [1.4], etc, and the bandgap-reference series ADR390 [1.5], the LM113 [1.6] series and REF1004 series [1.7] etc.

The development of IC technology has been driven by the ever smaller size and higher performance required of IC products. The technologies used are the bipolar technology, MOS technology, CMOS technology, and BiCMOS technology.

Nowadays, the CMOS technology is becoming more and more important in the IC market. Compared to those fabricated using a bipolar technology, the ICs fabricated in CMOS have some advantages. Firstly, CMOS is a cheap technology, because of the higher integration grades. With the same amount of components, the chip size of IC fabricated in CMOS technology is much smaller than that fabricated in a bipolar technology. Secondly, some options in circuit design, such as using analog switches, and switched capacitors, are only offered by CMOS [1.8], which allows for a more flexible circuit design. This makes it easier to design CMOS temperature sensors that do not only have a continuous analog output, but also a modulated output in the time domain. Thirdly, in CMOS technology, temperature sensors and bandgap references can be integrated with digital ICs, such as a microcontroller and a CPU; no external components are required for temperature detection and/or a reference signal.

For these reasons, temperature sensors and bandgap references fabricated in CMOS technology are preferred.

1.3 Problem Statement

Both bipolar transistors and MOS transistors can be used for temperature sensors and bandgap references. The temperature characteristics of the transistors are applied in the circuit design. Since it is easier to model and control the temperature characteristics of bipolar transistors, these transistors have been used as the basic components of integrated temperature sensors and bandgap references.

Much research work has been done on characterizing the temperature dependence of the properties of bipolar transistor [1.1, 1.2]. These dependencies can be used to design temperature sensors and bandgap references. They can also be used in other IC designs to reduce temperature effects. As we have seen in section 1.2, many types of integrated temperature sensors and bandgap references have been on the market for a relatively long time, for instance, the temperature-sensor series LM135 [1.3], the AD590 series [1.4], SMT160 [1.9], etc, and the bandgap-reference series ADR390 [1.5], the LM113 [1.6] series and REF1004 series [1.7] etc.

There are some problems specific to realizing temperature sensors and bandgap references in CMOS technology, which can be classified in two groups: device and circuit level problems.

The performance of temperature sensors and bandgap references strongly depends on the kind of bipolar transistors implemented in CMOS technology. To design temperature sensors or bandgap references, we have to know the temperature characteristics of these bipolar

transistors. Although many interesting designs of CMOS temperature sensors and bandgap-reference circuits have been presented in the literature [1.10, 1.11], very little is known about the basic limitation of the accuracy of these circuits and their long-term stability.

Also problems in circuit design have to be solved in CMOS technology. The poor matching of MOSFETs causes op-amps and comparators to have large offsets. This results in systematic errors in temperature sensors and bandgap references. Moreover, because MOSFETs are surface-channel devices, they have much higher $1/f$ noise (flicker noise) than transistors fabricated in bipolar technology. This causes larger random errors.

Through the application of advanced techniques in circuit design, these non-idealities can be minimized. For instance, by applying chopping techniques, one can significantly reduce the offset and $1/f$ noise of the op-amps [1.12]. By applying Dynamic Element Matching (DEM) techniques, one can eliminate the errors caused by the mismatch between components to the second order [1.3, 1.4]. Thus we can obtain accurate voltage amplification and division without trimming with good long-term stability. An auto-calibration technique can be applied to reduce the inaccuracy of the systematic parameters of the circuits significantly, so that high accuracy and good long-term stability can be guaranteed.

1.4 The Objectives of the Project

The accuracy of CMOS temperature sensors and bandgap references is limited by two things: by the accuracy of the bipolar components, which generate the basic signals, and by the accuracy of the processing circuit. Thus, the objectives are to characterize the behaviour of the bipolar device and to design a high-performance CMOS circuit.

In temperature sensors and bandgap references, the basic signals are the base-emitter voltage V_{BE} and the difference between two base-emitter voltages under different bias-current densities ΔV_{BE}. The performance of a well-designed temperature sensor or bandgap-reference circuit depends on the accuracy of these two basic signals.

Here, the device characterization is used to investigate the temperature dependencies of the base-emitter voltage V_{BE} and the voltage difference ΔV_{BE}. Effects affecting the ideal values of these voltages V_{BE} and ΔV_{BE} are studied.

Care must be taken in circuit design to maintain the accuracy of the basic signals V_{BE} and ΔV_{BE} based on the characterization results. For instance, the accuracy of ΔV_{BE} depends on the matching of two bipolar transistors, as well as the accuracy of the bias-current ratio. The circuit should be carefully designed to eliminate errors due to mismatching of the bipolar transistors and device mismatch in the current-ratio-generating circuit.

The process tolerance results in a certain spread in the value of the saturation current, thus results in the spread in the value of base-emitter voltage under a determined temperature. Thus an appropriate trimming technique is necessary to reduce this error. Single-point trims are discussed later.

1.5 The Outline of the Thesis

Chapter 2 gives a brief theoretical description of bipolar transistors. In this chapter, the properties of the base-emitter voltage versus temperature and bias current are described. Also,

two types of bipolar transistors available in CMOS technology are presented. It is shown that the vertical substrate transistors are preferable for temperature sensors and bandgap references.

Chapter 3 characterizes vertical substrate transistors fabricated in CMOS technology. A measurement set-up has been built to measure the base-emitter voltage and the ΔV_{BE} voltage difference over the temperature range from -40°C to 160°C, with biasing currents from 5 nA to 1 mA. The characterization results show that the base-emitter voltage of a vertical substrate transistor fits the well-known Gummul-Poon model quite well. This means that the base-emitter voltage of the substrate transistors can be well predicted by applying the extracted model parameters V_{g0} and η. The measurements show that the ΔV_{BE} voltage can be generated with an inaccuracy of less than 0.1%, by optimisation of the bias current and the emitter size of the transistors.

Chapter 4 describes some advanced technologies in circuit design. The main focus is on the circuit design technologies, such as DEM techniques, the chopping technique and auto-calibration techniques. The architecture considerations in circuit design are also discussed in this chapter.

Chapter 5 discusses some architecture considerations. It is possible to obtain the temperature-sensing signal and bandgap-reference signal sequentially from a single bipolar transistor under different bias currents or from multiple transistors. Features of the different architectures such as circuit complexity, noise performance, power consumption, etc. have been investigated.

Chapter 6 presents the application of the device characteristics in an advanced circuit design. A CMOS integrated interface circuit for thermocouples has been designed. In this circuit, the basic voltage signal V_{BE}, ΔV_{BE}, the offset voltage V_{off} and the unknown thermocouple voltage V_x are converted into the time domain, using a voltage-to-time converter. The combinations of V_{BE} and ΔV_{BE} form a bandgap-reference voltage and a temperature-sensing voltage. The bandgap-reference voltage and the offset voltage are used for auto-calibration. Auto-calibration is applied to eliminate the additive and multiplicative errors of the voltage-to-time converter. The temperature-sensing voltage represents the chip temperature, enabling cold-junction compensation for thermocouples. The measurement results are also presented here.

Chapter 7 presents a switched-capacitor (SC) instrumentation amplifier with Dynamic-Element-Matching (DEM) feedback. This instrumentation amplifier can be applied in combination with the thermocouple interface to pre-amplify accurately the extreme small thermocouple voltage before this signal is converted to the time domain.

Chapter 8 gives the main conclusions of the thesis.

Chapter 9 gives the summary of the thesis

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Chapter 2 Bipolar Components in CMOS Technology

2.1 Introduction

This chapter mainly focuses on the basic characteristics of bipolar transistors and the bipolar transistors available in CMOS technology.

The basic characteristic of bipolar transistors is the base-emitter voltage versus the bias current and the temperature $V_{BE}(I_C, \vartheta)$. The properties of $V_{BE}(I_C, \vartheta)$ are applied to generate the temperature-sensor signal and the bandgap-reference signal.

The chapter describes two types of bipolar transistors available in CMOS technology: lateral and vertical substrate transistors. A comparison of these two types of structures shows that vertical substrate transistors are more suitable for designing high-performance temperature sensors and bandgap references.

2.2 Basic Theory of Bipolar Transistors

2.2.1 Ideal Case

Under forward biasing, the collector current depends exponentially on the base-emitter voltage:

$$I_C = I_S \left(\exp^{\frac{qV_{BE}}{k\vartheta}} - 1 \right), \tag{2.1}$$

where I_C = the collector current of the bipolar transistor,
I_S = the saturation current of the bipolar transistor,
V_{BE} = the forward-biased base-emitter voltage,
k = the Boltzmann's constant,
q = the electron charge, and
ϑ = the absolute temperature.

If the base-emitter voltage $V_{BE} > 3k\vartheta/q$, equation (2.1) can be simplified, yielding:

$$I_C \approx I_S \exp^{\frac{qV_{BE}}{k\vartheta}}. \tag{2.2}$$

The saturation current I_S amounts to:

$$I_S = \frac{q^2 n_i^{\,2} A_E D_B}{Q_B}, \tag{2.3}$$

where A_E = the emitter-junction area,
n_i = the intrinsic carrier concentration in the base,
D_B = the effective minority-carrier diffusion constant in the base, and
Q_B = the charge represented by the net number of doping atoms in the neutral base per unit area.

The charge Q_B is obtained by using the integration equation:

$$Q_B = q\int_{x_E}^{x_C} N_B^+ \, dx, \tag{2.4}$$

where N^+_B represents the majority density, x_E and x_C represent the boundaries of the neutral base region on the emitter side and the collector side, respectively.

At moderate temperatures, the dopant is fully ionised, and the intrinsic carrier concentration is much less than the doping concentration. In this case, it holds that:

$$Q_B \approx q\int_{x_E}^{x_C} N_B dx, \tag{2.5}$$

where N_B represents the base-doping density.

The temperature dependency of I_S is based on the temperature dependency of the parameters n_i and D_B [2.1], according to:

$$n_i^{\,2} \propto \vartheta^3 \exp^{-\frac{qV_g}{k\vartheta}} \tag{2.6}$$

$$D_B = \frac{k\vartheta}{q}\overline{\mu}_B, \tag{2.7}$$

where $\overline{\mu}_B$ = the effective value of the mobility of the minority carriers in the base,
V_g = the bandgap voltage of the base material.

The net base charge Q_B also changes with temperature, because the boundaries x_E and x_C depend on temperature, and N_B^+ also changes with temperature at very low and high temperatures. At very low temperatures, the dopant is not fully ionised due to the freeze-out effect. And at very high temperatures, the intrinsic carriers become dominant. However, in the moderate temperature range, we can neglect the temperature dependence of Q_B.
The mobility $\overline{\mu}_B$ and the bandgap voltage V_g are related to the temperature in a non-linear way. By approximation, they can be expressed as:

$$\overline{\mu}_B \propto \vartheta^{-n}, \tag{2.8}$$

$$V_g = V_{g0} - \alpha\vartheta, \tag{2.9}$$

where n and α are constants. n depends on the doping concentration and profile in the base, and thus n is a process-dependent constant. V_{g0} is the extrapolated value of the bandgap voltage $V_g(\vartheta)$ at 0 K.

Taking together all the temperature dependencies of equation (2.2) yields the equation:

$$I_C = C\vartheta^{\eta} \exp\left[\frac{q\left(V_{BE} - V_{g0}\right)}{k\vartheta}\right], \tag{2.10}$$

where C is a constant, and $\eta = 4 - n$.

According to measurement results of Meijer [2.2], the values of the parameters V_{g0} and η differ from those one would expect on the basis of physical considerations. This is due to the poor approximation in equation (2.9) for $V_g(\vartheta)$ [2.3]. With empirical values for V_{g0} and η, equation (2.10) can perform rather accurately.

To find out the equation for $V_{BE}(\vartheta)$, we consider two temperatures: an arbitrary temperature ϑ and a reference temperature ϑ_r. Applying equation (2.10) for both temperatures, we can derive the temperature dependence of base-emitter voltage $V_{BE}(\vartheta)$ from the expression of $I_C(\vartheta)/I_C(\vartheta_r)$

$$V_{BE}(\vartheta) = V_{g0}\left(1 - \frac{\vartheta}{\vartheta_r}\right) + \frac{\vartheta}{\vartheta_r}V_{BE}\left(\vartheta_r\right) - \eta\frac{k\vartheta}{q}\ln\left(\frac{\vartheta}{\vartheta_r}\right) + \frac{k\vartheta}{q}\ln\left(\frac{I_C(\vartheta)}{I_C(\vartheta_r)}\right). \tag{2.11}$$

When, for practical reasons, the collector current is made proportional to some power of the temperature ϑ:

$$I_C \propto \vartheta^m, \tag{2.12}$$

equations (2.11) and (2.12) give:

$$V_{BE}(\vartheta) = V_{g0}\left(1 - \frac{\vartheta}{\vartheta_r}\right) + \frac{\vartheta}{\vartheta_r}V_{BE}\left(\vartheta_r\right) - (\eta - m)\frac{k\vartheta}{q}\ln\left(\frac{\vartheta}{\vartheta_r}\right). \tag{2.13}$$

For convience, in circuit designs, it is better to express $V_{BE}(\vartheta)$ as the sum of a constant term, a term proportional to ϑ, and a higher-order term. In such way, the linear terms represent the tangent to the $V_{BE}(\vartheta)$ curve at the reference temperature ϑ_r, as shown in Figure 2.1 .

The new expression is:

$$V_{BE}(\vartheta) = \underbrace{\left[V_{g0} + (\eta - m)\frac{k\vartheta_r}{q}\right]}_{\text{constant}} - \underbrace{\lambda\vartheta}_{\text{linear}} + \underbrace{(\eta - m)\frac{k}{q}\left(\vartheta - \vartheta_r - \vartheta\ln\frac{\vartheta}{\vartheta_r}\right)}_{\text{high-order}}. \tag{2.14}$$

where

$$\lambda = \frac{\left\{V_{g0} + (\eta - m)\frac{k\vartheta_r}{q}\right\} - V_{BE}\left(\vartheta_r\right)}{\vartheta_r}. \tag{2.15}$$

The first term in (2.14) is defined as V_{BE0}, which is an important parameter in bandgap references.

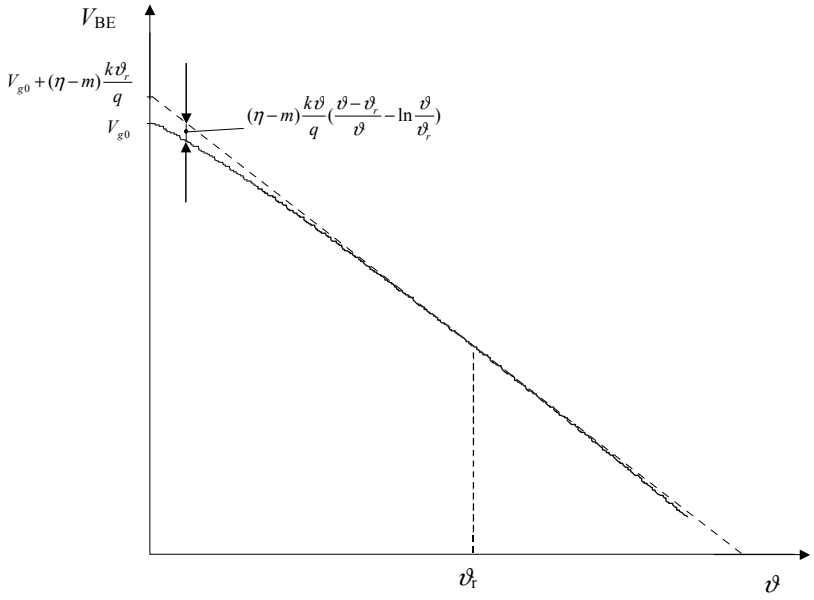


Figure 2.1 The base-emitter voltage versus temperature.

Under the condition of a small temperature change, (ϑ - ϑ_r) << ϑ, taking the first three terms of the Taylor expansion of the last term in (2.14) results in

$$V_{BE}(\vartheta)=\left\{V_{g0}+(\eta-m)\frac{k\vartheta_r}{q}\right\}-\lambda\vartheta-\frac{1}{2}(\eta-m)\frac{k\vartheta_r}{q}\left(\frac{\vartheta-\vartheta_r}{\vartheta_r}\right)^2, \tag{2.16}$$

which is widely used to design circuits for temperature sensors and bandgap references.

2.2.2 Low-Level Injection

Equation (2.1) is the approximation of a complex expression for the collector current, where the other terms are neglected. When the collector current is small (under a low bias base-emitter voltage or at high temperatures), other effects cannot be neglected. If they are all considered, the collector current amounts to

$$I_C=I_S\left(e^{\frac{qV_{BE}}{k\vartheta}}-1\right)+I_S\left(e^{\frac{qV_{BC}}{k\vartheta}}-1\right)+\frac{I_S}{B_R}\left(e^{\frac{qV_{BC}}{k\vartheta}}-1\right)+I_{gen}-I_{rec}, \tag{2.17}$$

where V_{BC} = the voltage across the base-collector junction, which is always reverse biased,
B_R = the reverse current gain,
I_{gen} = the generation current in the base-collector junction, and
I_{rec} = the recombination current in the base-collector junction.

In CMOS technology, the voltage across the base-collector junction V_{BC} is set to be zero. As a result the generation current I_{gen} is balanced by the recombination current I_{rec}, and only the first term in equation (2.17) remains. So one can counteract the effect of low-level injection by keeping V_{BC} equal to zero.

2.2.3 High-Level Injection

If the injected minority carrier concentration is in the order of the base-doping concentration, the collector current deviates from (2.1). If the injected carrier concentration is above the base-doping concentration, (2.1) becomes:

$$I_C = I_S' \left(e^{\frac{qV_{BE}}{2k\vartheta}} - 1 \right), \tag{2.18}$$

where $I_S' = \dfrac{q^2 n_i N_B A_E D_B}{Q_B}$.

Figure 2.2 shows the I_C - V_{BE} curve for two base-collector voltages.

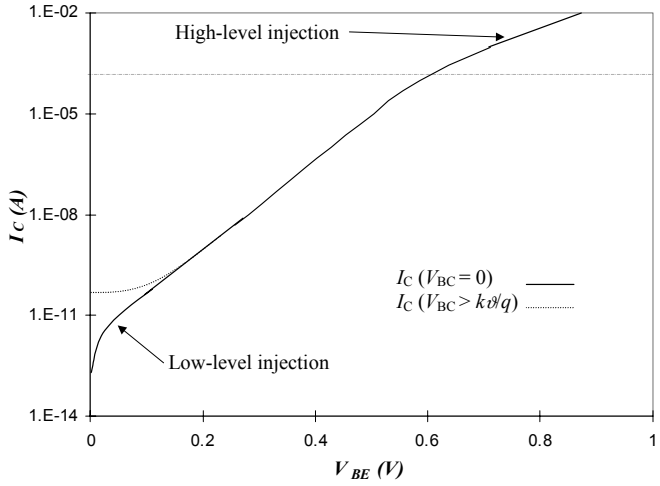


Figure 2.2 The I_C versus V_{BE} for two values of V_{BC}.

2.2.4 The Temperature-Sensor Signal and the Bandgap-Reference Signal

The temperature-sensor signal and the bandgap-reference signal are realized by the linear combinations of the base-emitter V_{BE} voltage and a voltage ΔV_{BE}, which is proportional to the absolute temperature

$$V(\vartheta) = \pm\left(V_{BE}(\vartheta) - C_1 \Delta V_{BE}\right), \tag{2.19}$$

$$V_{ref} = V_{BE}(\vartheta) + C_2 \Delta V_{BE}, \tag{2.20}$$

where ΔV_{BE} is generated from two base-emitter voltages under different bias current densities. According to (2.2), ΔV_{BE} can be expressed as:

$$\Delta V_{BE} = \frac{k\vartheta}{q} \ln\left(\frac{I_{C2}}{I_{C1}} \frac{I_{S1}}{I_{S2}} \right) = \frac{k\vartheta}{q} \ln \gamma, \tag{2.21}$$

The symbol ± in (2.19) represents the negative and the positive temperature coefficient, respectively. We call the voltages $C_1\Delta V_{\mathrm{BE}}$ or $C_2\Delta V_{\mathrm{BE}}$ PTAT (Proportional to the Absolute Temperature) voltages.

The value of the bandgap-reference voltage at a reference temperature ϑ_r is equal to

$$V_{ref} = V_{g0} + (\eta - n)\frac{k\vartheta_r}{q}. \tag{2.22}$$

The parameters C_1 and C_2 are determined by

$$C_1 = \frac{V_{BE}(\vartheta_Z)}{\Delta V_{BE}(\vartheta_Z)} = \frac{V_{BE}(\vartheta_Z)}{\frac{k\vartheta_Z}{q}\ln\gamma}, \tag{2.23}$$

$$C_2 = \frac{V_{ref} - V_{BE}(\vartheta_r)}{\frac{k\vartheta_r}{q}\ln\gamma}. \tag{2.24}$$

Figure 2.3 shows how the signals are combined for the temperature sensor and the bandgap reference.

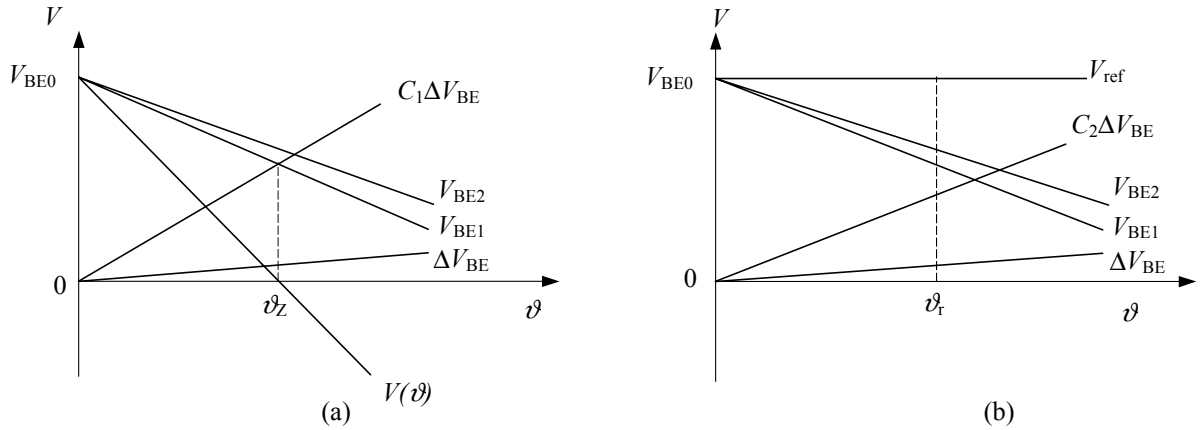


Figure 2.3 The linear combinations of V_{BE} and ΔV_{BE} for (a) temperature sensors, (b) bandgap references.

The higher-order term in equation (2.14) is not considered in the linear combinations (2.19) and (2.20). It causes a non-linear error in temperature sensors and bandgap references, as shown in Figure 2.4. The circuit design technique used to compensate for this error is called curvature correction.

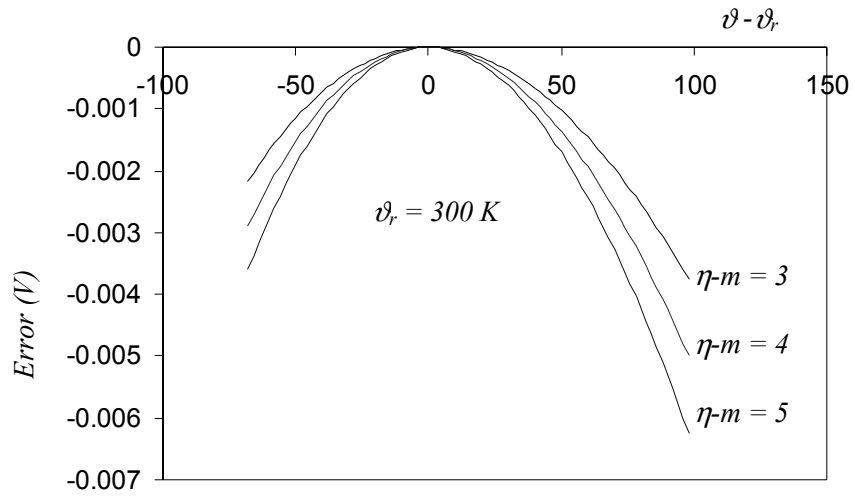


Figure 2.4 The non-linearity $\frac{k}{q}(\eta - m)(\vartheta - \vartheta_r - \vartheta\ln(\frac{\vartheta}{\vartheta_r}))$ *versus temperature.*

2.2.5 Calibration of Bandgap-References and Temperature Sensors

There are two reasons to calibrate bandgap references and temperature sensors: Firstly, at the ambient temperature the base-emitter voltage may deviate from the nominal value $V_{BE}(\vartheta_A)$; this is due to process spread. Secondly, the amplification factor C_1 or C_2 may deviate from the design values due to a mismatch. Figure 2.5 shows the deviation of a bandgap reference due to deviations in the base-emitter voltage $V_{BE}(\vartheta)$ and in the voltage $C_2\Delta V_{BE}$.

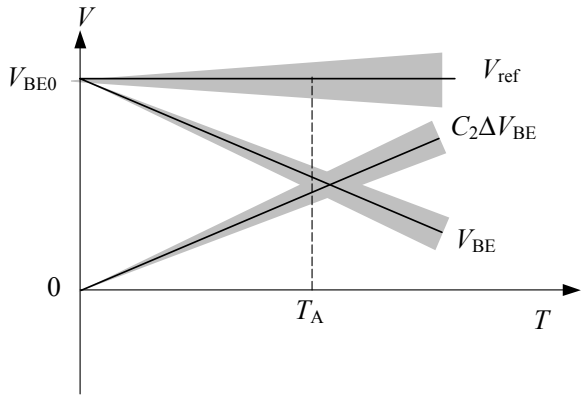
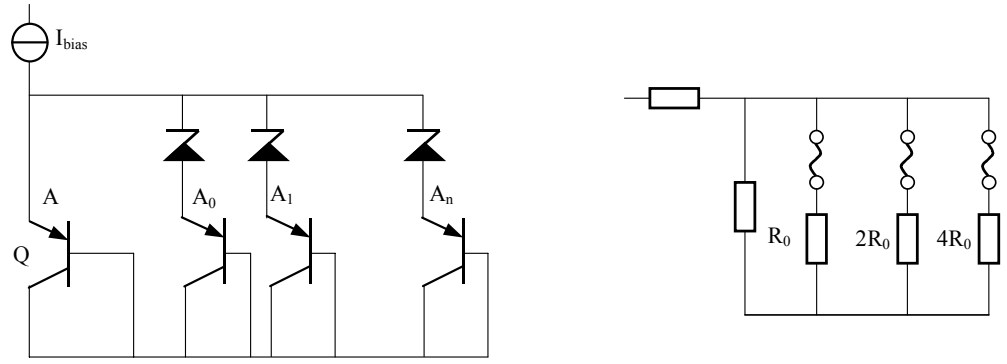


Figure 2.5 The spreading in the base-emitter voltage and in the PTAT voltage results in spreading in the bandgap reference.

Trimming can be performed to adjust the base-emitter voltage or to adjust the resistors as shown in Figure 2.6. In Figure 2.6(a) the base-emitter voltage is adjusted by trimming the emitter area of the transistor. In Figure 2.6(b) the resistance is adjusted using fusible links.



(a) (b)

Figure 2.6 (a) Adjusted emitter area, (b) adjusted resistor.

Several trimming techniques can be applied. The most commonly used are:

- Zener zapping (Figure 2.6(a)), to short-circuit connection,
- Fusible links (Figure 2.6(b)), to blow up connections, and
- Laser trimming, to adjust resistors.

The advantage of using fusible links is that for trimming a rather low voltage (5 V) can be used. For zener zapping, voltages up to 100 V are required. Therefore, special precautions have to be taken to protect the circuit during trimming. On the other hand, the zener-zapped components are usually highly reliable and show good long-term stability. With fusible links, special precautions have to be taken to avoid deterioration of the wafer-test probes. Furthermore, care has to be taken to avoid metal regrowth due to on-chip electro migration [2.4] during the whole lifetime of the chip.

The spreading in the base-emitter voltage Δ_{VBE} and the adjustment tolerance of the base-emitter voltage δ_{VBE} determine how many bit of trimming should be designed and the minimum area of the emitter, according to the following equations

$$\begin{aligned} \frac{k\vartheta_r}{q}\ln\left(\frac{A+(2^n-1)A_0}{A}\right) &\geq \Delta_{VBE} \\ \frac{k\vartheta_r}{q}\ln\left(\frac{A+A_0}{A}\right) &\leq \delta_{VBE} \end{aligned}, \tag{2.25}$$

where A represents the minimum area of the emitter, A_0 represents minimum area of the emitter that can be adjusted and n represents the bit number of the trimming system. The emitter area can be adjusted from the minimum value A to the maximum value (A+(2^n-1)A_0). For instance, with ϑ_r = 300 K, Δ_{VBE} = 20 mV, and δ_{VBE} = 0.5 mV. Substituting the value into equation (2.25) yields

$$\begin{aligned} (2^n-1)A_0 &\geq 1.158A \\ A_0 &\leq 0.0194A \end{aligned},$$

where n = 6 and $A = 52A_0$ can meet the above requirements. In this case, a 6-bit trimming structure is required. The area A is determined by the value of the base-emitter voltage at the reference temperature $V_{BE}(\vartheta_r)$.

2.3 Bipolar Transistors in CMOS Technology

There are two types of CMOS processes: the n-well CMOS and the p-well CMOS process. The two types of bipolar transistors available thus differ for these two processes. For an n-well CMOS process, lateral pnp and vertical substrate pnp transistors are available. In addition, for a p-well CMOS process, lateral npn and vertical substrate npn transistors are available. In this thesis, bipolar transistors in an n-well CMOS process are described.

2.3.1 Lateral Transistor

Figure 2.7 shows a cross section of a lateral bipolar transistor implemented in a standard n-well CMOS process [2.4]. Two implanted p+ regions in the same n-well are used as the emitter and collector, while the n-well is used as the base. A gate is used to obtain a thin oxide layer, which makes it easier to etch the holes for the emitter and collector diffusions. Compared to lateral pnp transistors fabricated in a bipolar process, those fabricated in CMOS have the following special properties:

- There is no buried layer, and as a result quite a lot of the injected holes are collected by the substrate, which gives rise to a relatively high substrate current I_{sub}.
- They do not show one-dimensional behaviour, and as a result, the $I_C(V_{BE})$ characteristic deviates from the ideal exponential relation.
- Even at rather low current level, high-level effects occur because especially transistors made using an n-well CMOS process have a low surface doping concentration.

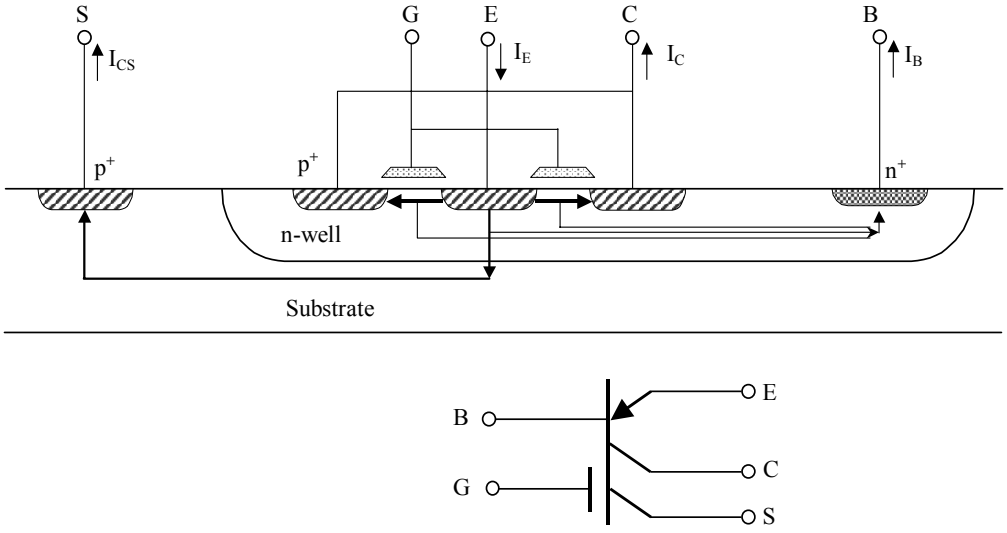


Figure 2.7 The cross section of a lateral PNP-transistor in an n-well CMOS process.

The effective emitter area in the expression of the saturation current I_S for the lateral transistor depends on the length along the emitter and the collector and on the depth of the p-diffused emitter, as shown in Figure 2.8. The change in the depletion layer between the emitter-base junctions that is caused by the change in the base-emitter voltage will change the effective emitter area. It causes $I_C(V_{BE}, \vartheta)$ to deviate from the ideal exponential relation. Since the depletion layer also changes with temperature, $V_{BE}(\vartheta)$ deviates from (2.11) as well.

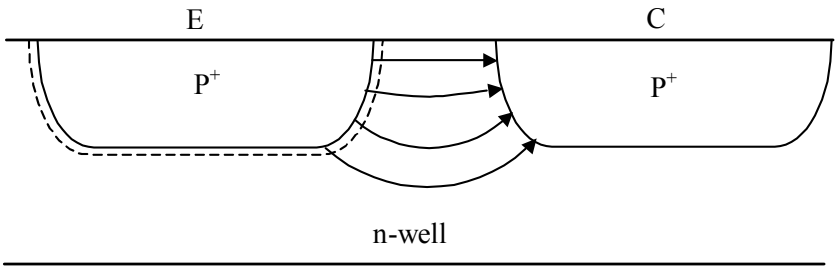


Figure 2.8 The cross section of a lateral PNP-transistor in an n-well CMOS process.

Figure 2.9 shows the $I_C(V_{BE})$ characteristic of a lateral pnp transistor fabricated in the 1.2 µm n-well CMOS process of Alcatel Microelectronics [2.5]. With the decrease in device size to submicron level, the depths of the n^+, p^+ and n-well become smaller, and the $I_C(V_{BE}, \vartheta)$ characteristics becomes worse.

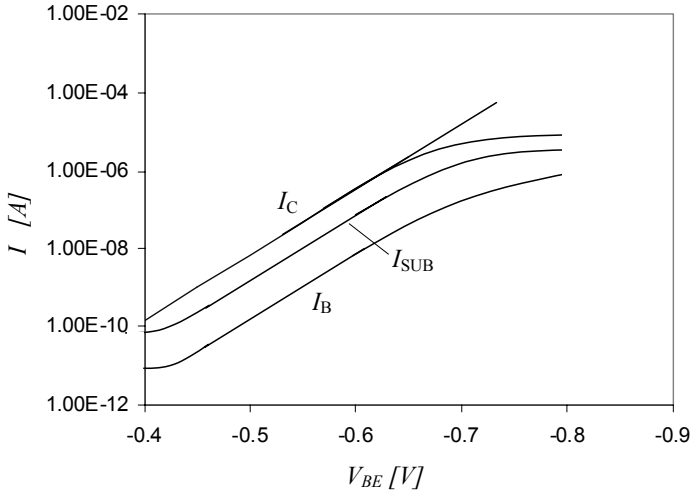


Figure 2.9 The I(V_{BE}) characteristics of a lateral pnp transistor fabricated in an n-well CMOS process (courtesy of Alcatel Microelectronics).

The gate G in the 5-terminal structure can be used to improve the performance of the lateral bipolar transistors. By biasing the gate G properly, one can push the injected emitter current below the surface; thus:

- Noise due to surface effects is reduced.
- Current flow is repelled under the surface of the n-well, where the doping concentration is lower than that at the surface, which results in a larger forward current gain.

2.3.2 Vertical Substrate Transistor

Figure 2.10 shows a cross section of a vertical pnp transistor implemented in a standard n-well CMOS process. Some special properties of the vertical bipolar transistors are:

- The base width, typically a few microns, is determined by the distance between the bottom of the p+ regions and that of the n-well.

- The base-width modulation effect is relatively weak due to the larger base width, resulting in a large early voltage. The base resistance is also relatively high.
- The collector (substrate) is lightly doped, and therefore the series collector resistance is high.

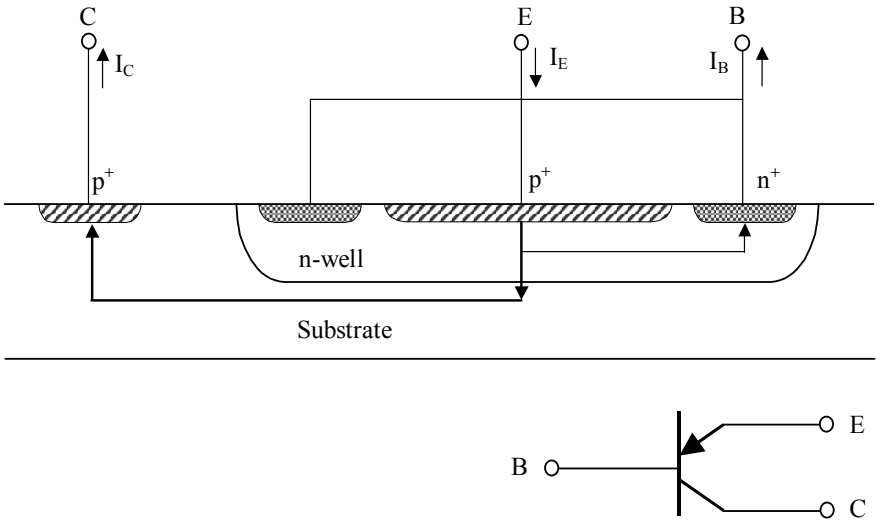


Figure 2.10 The cross section of a vertical PNP-transistor in an n-well CMOS process.

Although its junction depths and doping are not optimized for bipolar operation, the vertical bipolar transistor exhibits good performance with respect to the ideality of the $I_C(V_{BE})$ characteristic, because it shows better one-dimensional behaviour than the lateral transistor. However, the substrate collector limits the circuit design to only common-collector configurations.

2.3.3 Comparison of Two Types of the Bipolar Transistors

Lateral [2.5] [2.6] and vertical [2.7]-[2.11] bipolar transistors have been applied in the designs of temperature sensors and bandgap references.

With respect to the $I_C(V_{BE})$ characteristic, vertical substrate transistors are superior, because they perform much better than lateral transistors.

With respect to the circuit design, circuits based on lateral transistors are more flexible, because they allow the use of configurations from bipolar technology in CMOS technology. Designing circuits based on vertical transistors in CMOS poses a problem however, as there the common-emitter structure, which is the conventional circuit used in bipolar technology to generate and amplify the signal ΔV_{BE}, cannot be applied. Therefore, special amplifier configurations are required to amplify the voltage ΔV_{BE}. Figure 2.11 shows two basic circuits for a CMOS bandgap reference using lateral and vertical transistors.

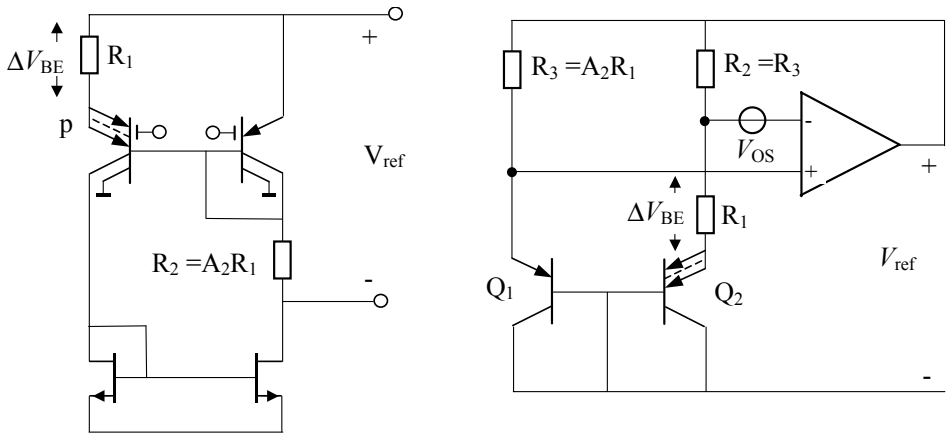


Figure 2.11 Two simple schematics of bandgap references in CMOS technology using (a) lateral, and (b) vertical transistors.

In Figure 2.11(b), the offset voltage of the operational amplifier must be taken into account in the expression of the output voltage:

$$V_{ref} = V_{BE1} + \frac{R_3}{R_1} V_{R1} \approx V_{BE1} + A_2 \left(\frac{k\vartheta}{q} \ln \frac{I_{S2}}{I_{S1}} + V_{OS} \right), \tag{2.26}$$

where V_{R1} represents the voltage across the resistor R_1. The non-zero offset voltage V_{OS} and its temperature dependence deteriorate the performance of the bandgap voltage output. For this reason, circuits using vertical transistors show worse results than those using lateral transistors [2.5] –[2.11].

In order to design high-performance bandgap references and temperature sensors, one must first develop advanced circuit design techniques that overcome the disadvantages of circuits employing vertical transistors, as the performance of temperature sensors and bandgap references is mainly limited by imperfection of the device characteristics.

In this thesis, it is shown that by the use of advanced circuit design techniques, one can obtain circuits generating a highly accurate ΔV_{BE} signal. In these high-performance temperature sensors and bandgap references, vertical bipolar transistors are used, which perform much better than lateral ones.

2.4 Conclusions

This chapter described the basic theory of bipolar transistors, especially the $I_C(V_{BE}, \vartheta)$ for the purpose of circuit design for temperature sensors and bandgap references. Two types of bipolar transistors, lateral and vertical substrate transistors, fabricated in CMOS technology were discussed. With respect to the $I_C(V_{BE})$ characteristic, vertical substrate transistors are preferred for generating the signals V_{BE} and ΔV_{BE} in our high-precision temperature sensors and bandgap references. However, advanced circuit design techniques should be developed to overcome the disadvantages of circuits employing vertical transistors.

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Chapter 3 Characterization of the Temperature Behavior

3.1 Introduction

This chapter deals with the device characterization of vertical substrate bipolar transistors. To investigate the characteristics of vertical bipolar transistors, and to identify the non-ideal effects that limit the accuracy of the voltages V_{BE} and ΔV_{BE}, we measured the voltages V_{BE} and ΔV_{BE} versus the temperature and the collector current I_C. We derived the parameters V_{g0} and η, the effective emission coefficient m, the forward current gain B_F, and the base resistances R_B. Non-ideal effects were analysed too.

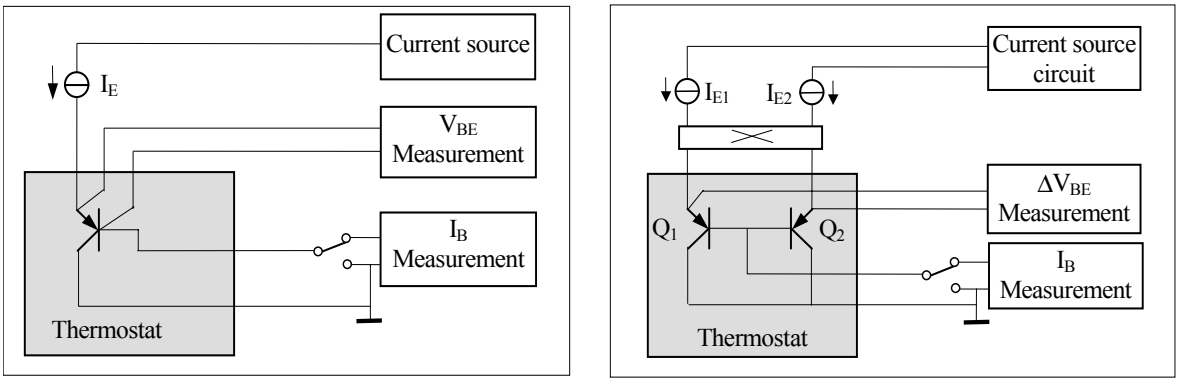
For vertical substrate bipolar transistors, it is easier to control the emitter current I_E than the collector current I_C. Therefore, not only the $V_{BE}(I_C, \vartheta)$ characteristics must be characterized, but also the base-current effect: due to the low current gain of the vertical substrate bipolar transistors, the base current has a significant effect on the voltages V_{BE} and ΔV_{BE}. The non-idealities that affect the accuracy of ΔV_{BE}, such as the base resistance, the effective emission coefficient and the low injection effect were investigated by measuring ΔV_{BE}. We investigated how the geometry and biasing current of the transistors can be optimized.
Devices fabricated in two CMOS processes, 0.7-µm and 0.5-µm, were characterized.

3.2 Measurement Set-ups.

Figure 3.1 shows the schematics of the measurement set-ups for the $V_{BE}(I_C, \vartheta)$ and $\Delta V_{BE}(I_C, \vartheta)$ characterizations. The emitter currents I_E, the base currents I_B and the voltages V_{BE} and ΔV_{BE} are measured for different temperatures.

For our investigations and experiments, we selected a temperature range of –40 °C to 160 °C. For the biasing current range, we chose the range of 5 nA to 1 mA for the base-emitter voltage measurement and that of 5 nA to 100 µA for the ΔV_{BE} measurement, respectively. The current range was chosen based on practical constraints. These are due to the low-current effects, interference, and $1/f$ noise at the low end of the range, and to the high-current effects and power dissipation at the high end. The target for the desired accuracy of all measurements corresponds to a temperature error of less than 0.1 K.

To realize accurate voltage and current measurements, we applied an auto-calibration technique to eliminate the additive and multiplicative effects of the measurement set-ups [3.1].



(a) (b)

Figure 3.1 The measurement set-ups for the (a) $V_{BE}(I_C, \vartheta)$, and (b) $\Delta V_{BE}(I_C, \vartheta)$ characterisation.

By using an appropriate thermal design, we could control and measure the temperature accurately. In this design, particular care has been taken to minimize the self-heating, the temperature gradients and drift during the measurement.

The test device for the ΔV_{BE} characterization consists of a pair of transistors of identical emitter size. Mismatching of the transistors will introduce an error in the ΔV_{BE} measurement. This error has been eliminated by employing the dynamic element matching technique. This was realized by interchanging the two transistors and taking the average of the measured ΔV_{BE} voltages under the same biasing condition [3.2].

Figure 3.2 shows a photograph of the test chip. On this chip, a single bipolar substrate transistor and a pair of transistors in a quad configuration are used to characterize the $V_{BE}(I_C, \vartheta)$ and $\Delta V_{BE}(I_C, \vartheta)$ behaviour. The emitter size of all transistors is 10 μm × 20 μm.

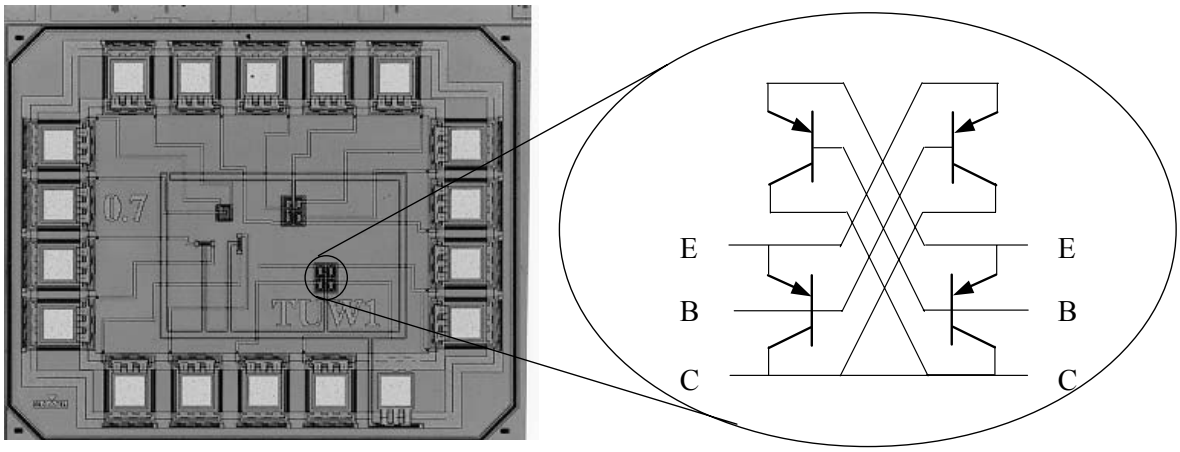


Figure 3.2 (a) A photograph of the test chip; (b) The transistor pairs under tested are configured in a quad configuration.

3.3 Parameter Characterizations

For the temperature range from -40 °C to 160 °C, we measured the base-emitter voltage V_{BE} under a emitter current I_E varying from 5 nA to 1 mA. The corresponding base current I_B was measured as well. The collector current I_C was derived by subtracting the measured base current from the measured emitter current. The measured $V_{BE}(I_C, \vartheta)$ is plotted in Figure 3.3.

For the same temperature range, we measured the voltage ΔV_{BE}, under a emitter current (I_{E1}) varying from 10 nA to 100 µA, with the emitter current ratio (I_{E2}/I_{E1}) of 3. The measured $\Delta V_{BE}(I_C, \vartheta)$ is plotted in Figure 3.4. The emitter currents and the corresponding base currents were measured as well.

These measurement results were used to derive the transistor parameters, as described in the next paragraphs.

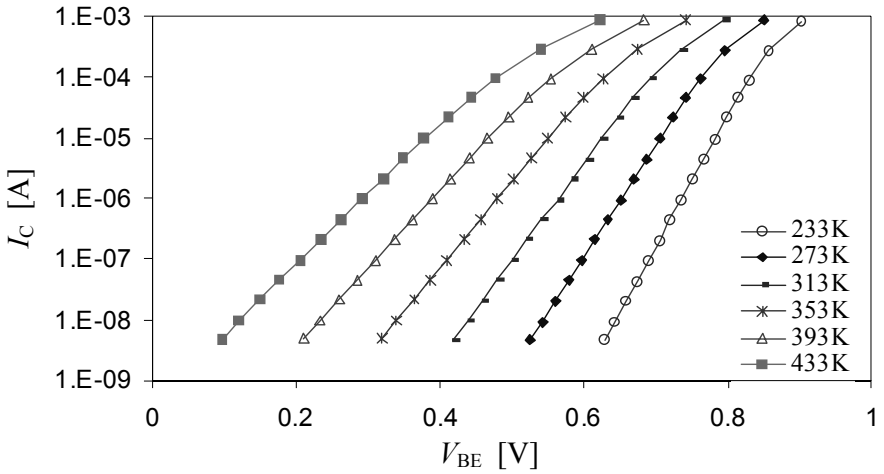


Figure 3.3 The measured results for $V_{BE}(I_C, \vartheta)$ for 0.7-µm CMOS.

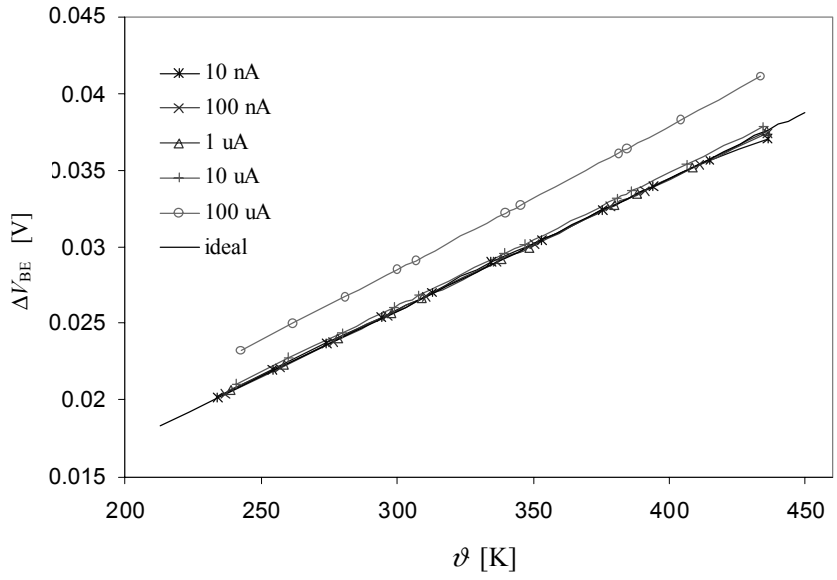


Figure 3.4 The measured $\Delta V_{BE}(\vartheta)$ for different emitter currents (I_{E1}).

3.3.1 The Saturation Current I_S

Figure 3.3 shows the measured results for the $V_{BE}(I_C, \vartheta)$ of a substrate bipolar transistor. A good exponential relation was found between V_{BE} and I_C over several decades of collector current. The deviation at high current levels is due to the contributions of the base resistance and the high injection effect.

The saturation current I_S was derived by curve fitting of the measured I_C-V_{BE} characteristic over the current range of 10 nA to 4 μA. Table 3.1 lists the extracted saturation current I_S of the devices fabricated in 0.7-μm and 0.5-μm CMOS with an emitter area of 10 μm × 20 μm.

	I_S (A) (0.7-μm CMOS)	I_S (A) (0.5-μm CMOS)
ϑ = 233 K	1.26×10^{-22}	3.04×10^{-23}
ϑ = 293 K	3.49×10^{-17}	9.13×10^{-18}
ϑ = 433 K	3.98×10^{-10}	1.08×10^{-10}

Table 3.1 The extracted saturation currents for three temperatures (emitter size: 10 μm × 20 μm).

Note that the saturation currents of a substrate bipolar transistor fabricated in 0.7-μm CMOS technology were roughly 3.8 times of those of a transistor fabricated in 0.5-μm CMOS technology. According to equations (2.3), (2.5) and (2.7), the saturation current depends on the mobility of the minority in the base and the doping concentration in the base. We can conclude that the heavier doping concentrations and mobility of the minority in the base result in the lower saturation current in 0.5-μm CMOS.

3.3.2 The Knee Current I_{KF}

The parameter I_{KF} represents the behaviour of the transistor at high injection, when the injected minority carrier concentration is in the order of the base doping concentration. In this case, $I_C(V_{BE})$ deviates from the exponential relation $I_C = I_S \exp(qV_{BE}/k\vartheta)$:

$$I_C = -\frac{I_{hl}}{2} + \frac{I_{hl}}{2}\sqrt{1 + \frac{4I_S}{I_{hl}} e^{\frac{qV_{BE}}{k\vartheta}}}\ , \tag{3.1}$$

where the current I_{hl} is defined as the current when the injected minority concentration equals the base doping concentration:

$$I_{hl} = qD_B F_{geo} N_B \tag{3.2}$$

which also equals the value of the knee current I_{KF}. When

$$I_S e^{\frac{qV_{BE}}{k\vartheta}} >> I_{hl}, \tag{3.3}$$

equation (3.1) becomes:

$$I_C = \sqrt{I_{hl} I_S}\, e^{\frac{qV_{BE}}{2k\vartheta}}, \tag{3.4}$$

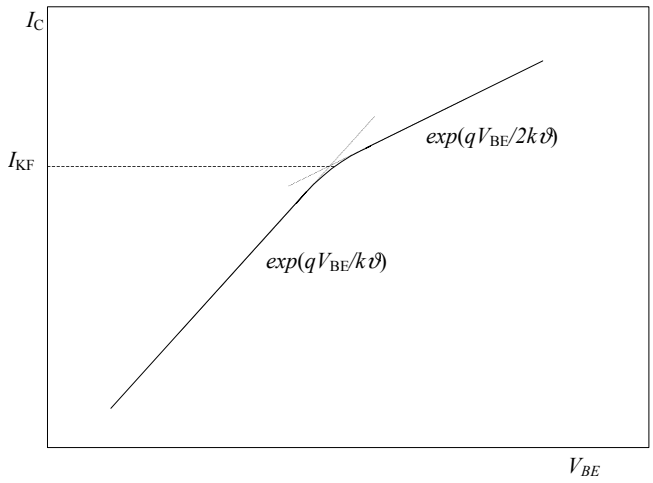


Figure 3. 5 The I_C-V_{BE} including high injection effect.

In the area where the curve starts to bend from $\exp(qV_{BE}/k\vartheta)$ to $\exp(qV_{BE}/2k\vartheta)$, the knee current I_{KF} can be approximately calculated by

$$I_{KF} = I_{hl} = \frac{I_{C,m}^2}{I_S e^{\frac{qV_{BE}}{k\vartheta}} - I_{C,m}}, \tag{3.5}$$

where $I_{C,m}$ is the measured collector current and I_S is derived from the measured I_C-V_{BE} at lower current range. The calculated I_{KF} at room temperature is listed in Table 3.2, where the effect of the base resistance is neglected. It is shown that with the same emitter area, the high injection occurs earlier in devices fabricated in 0.7-µm CMOS than in the devices fabricated in 0.5-µm CMOS.

	I_{KF} (A) (0.7-µm CMOS)	I_{KF} (A) (0.5-µm CMOS)
ϑ = 293 K	~1.5 mA	~4.3 mA

Table 3.2 The calculated knee current I_{KF} at room temperature (*emitter size: 10 µm × 20 µm*).

3.3.3 Parameters V_{g0} and η

As described in chapter 2, the temperature dependence of the base emitter voltage $V_{BE}(\vartheta)$ can be expressed as:

$$V_{BE}(\vartheta) = V_{g0}\left(1 - \frac{\vartheta}{\vartheta_r}\right) + \frac{\vartheta}{\vartheta_r} V_{BE}(\vartheta_r) - \eta \frac{k\vartheta}{q} \ln\left(\frac{\vartheta}{\vartheta_r}\right) + \frac{k\vartheta}{q} \ln\left(\frac{I_C(\vartheta)}{I_C(\vartheta_r)}\right), \tag{3.6}$$

where V_{g0} is the extrapolated bandgap voltage at 0 K, η is a material-dependent and process-dependent parameter, and ϑ_r is the reference temperature.

The parameters V_{g0} and η can be derived from the measured results of V_{BE} at three temperatures ϑ_1, ϑ_r and ϑ_2 ($\vartheta_1 < \vartheta_r < \vartheta_2$) [3.3], by solving the equation:

$$\begin{cases} V_{BE}(\vartheta_1) = V_{g0}\left(1-\dfrac{\vartheta_1}{\vartheta_r}\right) + \dfrac{\vartheta_1}{\vartheta_r}V_{BE}(\vartheta_r) - \eta\dfrac{k\vartheta_1}{q}\ln\left(\dfrac{\vartheta_1}{\vartheta_r}\right) + \dfrac{k\vartheta_1}{q}\ln\left(\dfrac{I_C(\vartheta_1)}{I_C(\vartheta_r)}\right) \\ V_{BE}(\vartheta_2) = V_{g0}\left(1-\dfrac{\vartheta_2}{\vartheta_r}\right) + \dfrac{\vartheta_2}{\vartheta_r}V_{BE}(\vartheta_r) - \eta\dfrac{k\vartheta_2}{q}\ln\left(\dfrac{\vartheta_2}{\vartheta_r}\right) + \dfrac{k\vartheta_2}{q}\ln\left(\dfrac{I_C(\vartheta_2)}{I_C(\vartheta_r)}\right) \end{cases} \tag{3.7}$$

The parameters V_{g0} and η have been calculated based on the measured base-emitter voltages for –40 °C (ϑ_1), 20 °C (ϑ_r), and 80 °C (ϑ_2). The results are shown in Figure 3.6(a). There is a strong negative correlation between V_{g0} and η, which is similar to that found by Meijer and Vingerling, and by Ohte and Yamahata, for transistors fabricated in bipolar technology [3.3], [3.4].

An important parameter in designing a bandgap reference is $V_{BE0}(\vartheta_r)$, which is the intersection of the tangent of the curve $V_{BE}(\vartheta)$ at the point ϑ_r with the vertical axis (ϑ = 0 K). The parameter $V_{BE0}(\vartheta_r)$ is calculated as:

$$V_{BE0}(\vartheta_r) = V_{g0} + \eta\frac{k\vartheta_r}{q}. \tag{3.8}$$

It was found that at 293 K, $V_{BE0} \cong 1.252$ V for transistors fabricated in 0.7-µm CMOS technology, and $V_{BE0} \cong 1.250$ V for transistors fabricated in 0.5-µm CMOS technology. The value of V_{BE0} versus the collector current is plotted in Figure 3.6(b). At high current levels, due to the effects of the base resistance and the high injection, I_C-V_{BE} deviates from the exponential relationship, resulting in a large deviation in the parameter extraction.

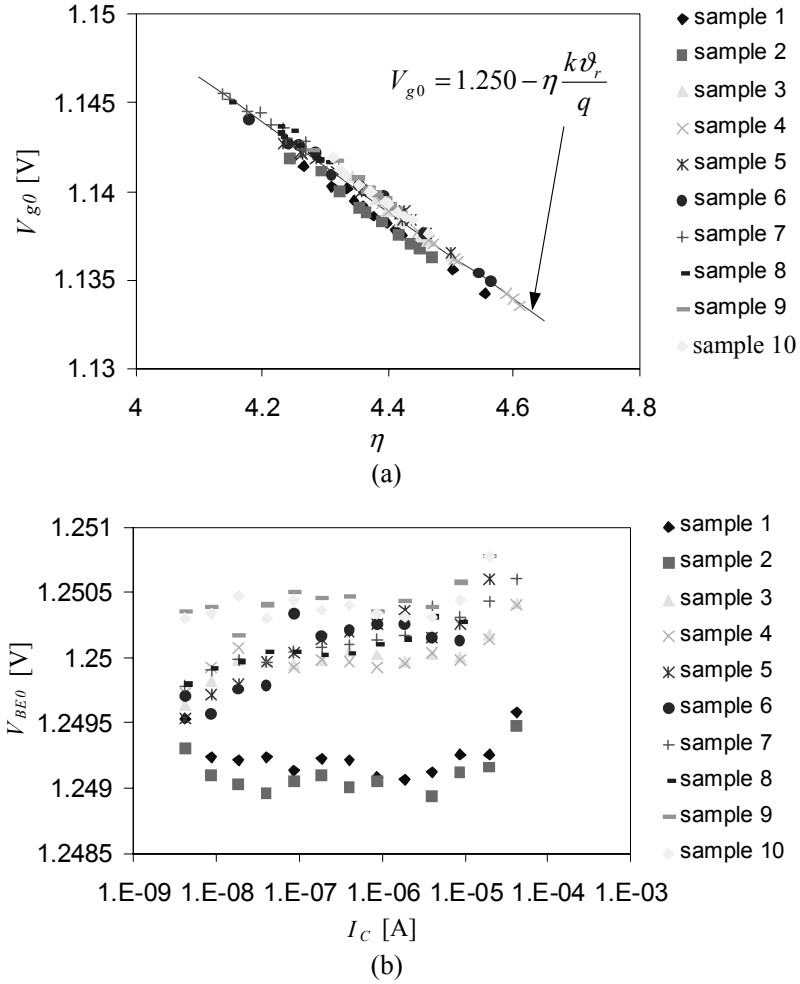


Figure 3.6 (*a*) *The calculated parameter V_{go} and η based on the measurement results for -40 ℃, 20 ℃, and 80 ℃ for 10 samples, and* (*b*) *the parameter V_{BE0} at room temperature* (*300K*) *for 0.5-μm CMOS.*

Figure 3.7 shows the difference between the measured base-emitter voltage $V_{\mathrm{BE\_meas.}}$ and the calculated base-emitter voltage $V_{\mathrm{BE\_cal}}$, based on the Gummel-Poon model, for which the extracted model parameters were used, which fits the $V_{\mathrm{BE}}(\vartheta)$ best (V_{go} = 1.147 V, η = 4.15). The inaccuracy is less than ±0.1 mV (see Figure 3.7), which corresponds to a temperature error of less than ±0.05 K for the temperature range of -20°C to 100°C. Comparing this result with those presented in [3.3] and [3.4], we can conclude that the temperature behavior of V_{BE} of CMOS bipolar substrate transistors fits the Gummel-Poon model as well as the behavior of the transistors fabricated in bipolar technology. This indicates why the curve with emitter current of 0.01 μA shows a large deviation at high temperatures. At these temperatures, the low injection effect occurs, so that the simplified exponential relation $I_{\mathrm{C}} = I_{\mathrm{S}}\exp(qV_{\mathrm{BE}}/k\vartheta)$ no longer accurately express the I_{C}-V_{BE}. For instance, the extracted saturation current at 160 °C is 3.9×10^{-10}, under the biasing current of 0.01 μA, the simplified exponential relation $I_{\mathrm{C}} = I_{\mathrm{S}}\exp(qV_{\mathrm{BE}}/k\vartheta)$ causes an error of 1.6 mV. The large deviation of the curve for the emitter current of 10 μA at high temperatures is due to the base resistance and the high injection effect.

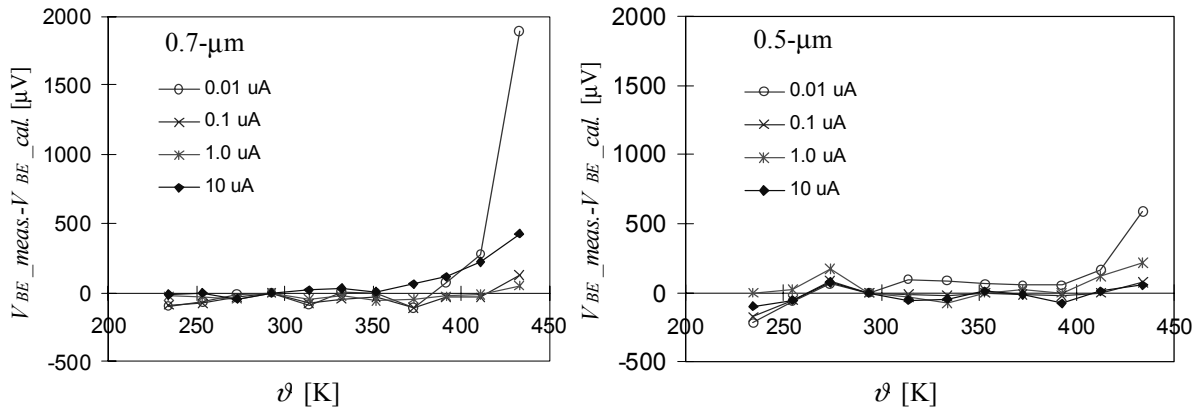


Figure 3.7 The deviation of the measured V_{BE} from the calculated value based on the Gummel-Poon model with the fitted result V_{g0} = 1.147 V, η = 4.15, for 0.7-µm CMOS and V_{g0} =1.141 V, η = 4.3, for 0.5-µm CMOS.

Table 3.3 lists the parameters derived from measurements for the current range from 0.01 µA to 10 µA. It is clear that there are only minor differences for the parameters V_{go}, η, and V_{BE0} between the devices fabricated in 0.7-µm CMOS technology and the devices fabricated in 0.5-µm CMOS technology.

	V_{go} (V)	η	V_{BE0} (V) (300K)	$V_{BE\_meas.}$- $V_{BE\_cal.}$ (µV)
0.7-µm CMOS	1.1456±0.0030	4.23 ∓ 0.10	1.255±0.001	< 100
0.5-µm CMOS	1.1390±0.0050	4.33 ∓ 0.20	1.252±0.001	< 100

Table 3.3 The parameter values for bipolar substrate transistors fabricated in 0.7-µm and 0.5-µm CMOS technology, respectively.

3.3.4 Effective Emission Coefficient *m*

The effective emission coefficient *m* is defined as [3.5]:

$$\frac{1}{m} = \frac{k\vartheta}{qI_C} \cdot \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{V_{CB}=const.} . \tag{3.9}$$

m varies from approximately unity at low collector current to approximately two at high collector currents. If we take the effective emission coefficient into account, the I_C-V_{BE} dependency is:

$$I_C = I_S \exp^{\frac{qV_{BE}}{mk\vartheta}} . \tag{3.10}$$

From the measurement results shown in Figure 3.3, the parameter *m* is derived and depicted in Figure 3.8.

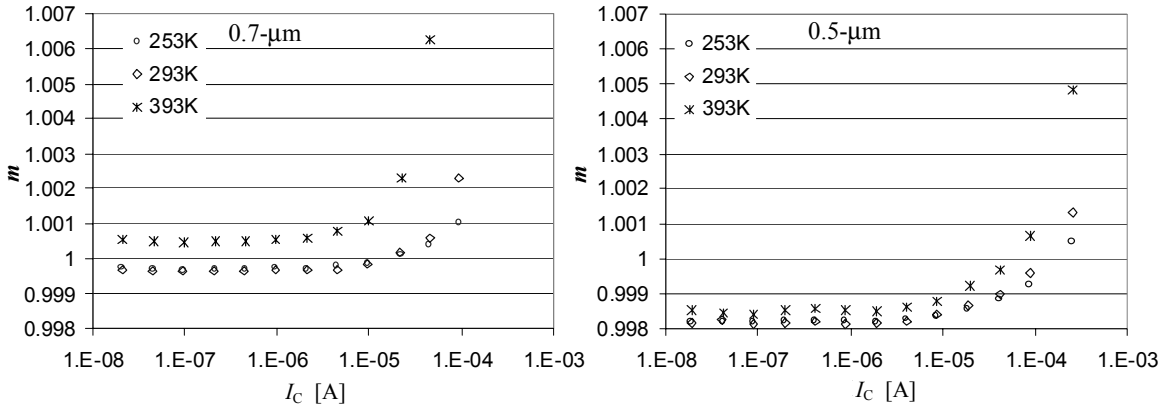


Figure 3.8 The effective emission coefficient at three temperatures.

The calculation according to equation (3.2) shows that at higher temperatures, the I_C-V_{BE} starts to deviate from the ideal exponential relation earlier, and as a result, the effective emission coefficient *m* deviates from unity earlier. Figure 3.8 supports this conclusion.

The effective emission coefficient *m* can also be derived from the $\Delta V_{BE}(I_C, \vartheta)$ measurement. In the moderate current range, the low injection effect and high injection effect can be neglected. In this current range, the effective emission coefficient *m* can be derived from:

$$m = \frac{\Delta V_{BE\_Meas.} - R_B \Delta I_B}{\Delta V_{BE\_i.}}, \tag{3.11}$$

where $\Delta V_{BE\_Meas.}$ is the measured voltage ΔV_{BE} and $\Delta V_{BE\_i.}$ is the voltage ΔV_{BE} calculated by substituting the measurement data for the current ratio and the temperature in equation (2.21). The result *m* versus temperature is shown in Figure 3.9. The drop of *m* at high temperatures and low currents is caused by the fact that the approximation of $I_C = I_S \exp^{\frac{qV_{BE}}{mk\vartheta}}$ is not valid any more. According to equation (2.1), $\Delta V_{BE\_i.}$ is calculated by:

$$\Delta V_{BE\_i} = \frac{k\vartheta}{q} \cdot \ln\left(\frac{I_{C2} + I_{S2}}{I_{C1} + I_{S1}} \cdot \frac{I_{S1}}{I_{S2}}\right), \tag{3.12}$$

which results in a lower value than when it is calculated using equation (2.21).

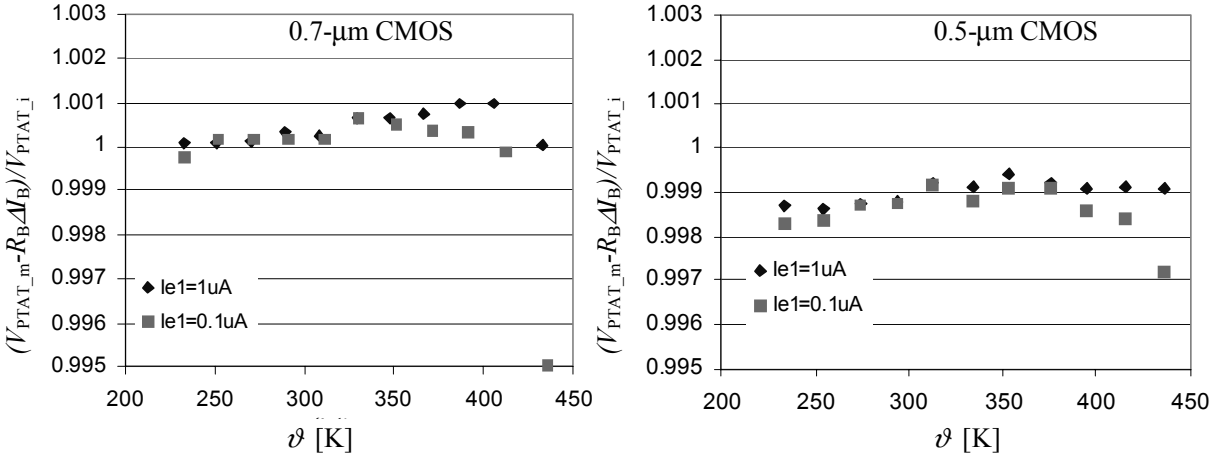


Figure 3.9 The effective emission coefficient m at I_{E1} = 0.1 µA and I_{E1} = 1 µA for the same emitter area of 10 µm × 20 µm.

The parameter *m* derived from the ΔV_{BE} measurement (Figure 3.9) is in good agreement with that derived from the V_{BE} measurement, except for the point at a temperature of 233 K.

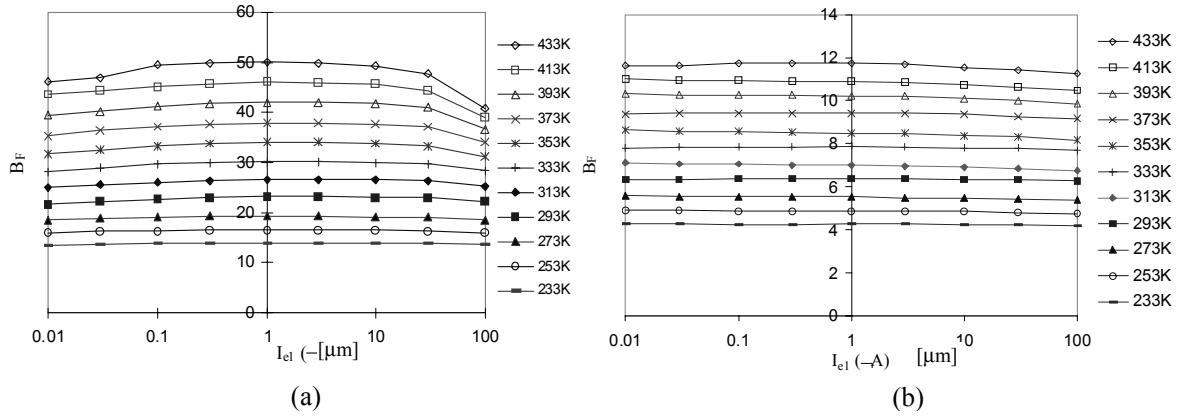
It is concluded that in the moderate current range, the effective emission coefficient in CMOS technology is very close to the ideal value of unity.

3.3.5 Forward Current Gain B_F

We determined the static forward common-emitter current gain B_F by measuring the emitter current I_E and the base current I_B, respectively.

$$B_F = \frac{I_E}{I_B} - 1 \tag{3.13}$$

The measured forward current gain B_F versus emitter current and temperature are depicted in Figure 3.10 and Figure 3.11, respectively.



(a) (b)

Figure 3.10 The current dependencies of the current gain for (a) 0.7-µm, and (b) 0.5-µm CMOS.

Figure 3.10 shows that in the intermediate current range, B_F hardly depends on the emitter current for the temperature range of –40 °C to 160 °C, for both 0.7-µm CMOS and 0.5-µm CMOS. Figure 3.10 shows that: a) the common-emitter current gain of the vertical bipolar transistors fabricated in CMOS technology is much lower than that of those fabricated in bipolar technology; b) the common-emitter current gain of the transistors fabricated in 0.5-µm CMOS technology is much lower than that of those fabricated in 0.7-µm CMOS technology.

In the moderate current range, the forward common-emitter current gain B_F is determined with the emitter efficiency γ and the transfer factor α_T, which are determined by [3.6]:

$$\gamma \approx \frac{1}{1+\frac{D_E}{D_B}\cdot\frac{n_{Eo}}{p_{no}}\cdot\frac{W_B}{L_E}} = \frac{1}{1+\frac{D_E}{D_B}\cdot\frac{n_{iE}^2}{n_{iB}^2}\cdot\frac{N_B}{N_E}\cdot\frac{W_B}{L_E}}, \tag{3.14}$$

$$\alpha_T \approx 1-\frac{W_B^2}{2L_P^2}, \tag{3.15}$$

where D_E = the diffusion coefficient at the emitter,
D_B = the diffusion coefficient at the base,
N_E = the impurity concentration at the emitter,
N_B = the impurity concentration at the base,
W_B = the base thickness,
L_E = the diffusion length at the emitter, and
L_P = the diffusion length at the base.

The forward common-emitter current gain can be approximated by the equation:

$$B_F = \frac{\alpha_T\gamma}{1-\alpha_T\gamma} \approx \frac{1-\frac{W_B^2}{2L_P^2}}{\frac{W_B^2}{2L_P^2}+\frac{D_E}{D_B}\cdot\frac{n_{iE}^2}{n_{iB}^2}\cdot\frac{N_B}{N_E}\cdot\frac{W_B}{L_E}}. \tag{3.16}$$

A possible reason to explain the low value of B_F is the big value of W_B in CMOS technology. As a parasitic device, the base thickness of a pnp vertical bipolar transistor is the space between the bottom of a p+ region and the bottom of the n-well. This space is much larger than that of bipolar transistors fabricated in bipolar technology, where the process is designed to optimize the parameters of the bipolar transistors. This fact explains why the forward common-emitter current gain B_F of the vertical bipolar transistors fabricated in CMOS technology is much lower than that of transistors in bipolar technology. This also explains why the vertical bipolar transistors fabricated in CMOS technology have much larger forward early voltages (V_{ar} = 170 V for 0.7-µm CMOS and V_{ar} = 95 V for 0.5-µm CMOS).

For smaller size of CMOS process, it requires heavier doping or implant concentrations and thus the thinner well and smaller depletion thickness. The heavier doping concentrations result in smaller diffusion lengths. The combination of all these effects results in a lower common-emitter current gain in 0.5-µm CMOS than in 0.7-µm CMOS.

As shown in Figure 3.10, the forward common-emitter current gain B_F decreases at low current levels and at high current levels. At low current levels, this is due to the generation-recombination current in the emitter-base depletion region, which is added to the base current,

resulting in the decrease of B_F. At high current levels, the decrease of B_F is caused by the high injection effect, where the injected minority-carrier density in the base tends to approach the impurity concentration N_B. In another words: the injected carriers effectively increase the base doping, which in turn cause the emitter efficiency to decrease.

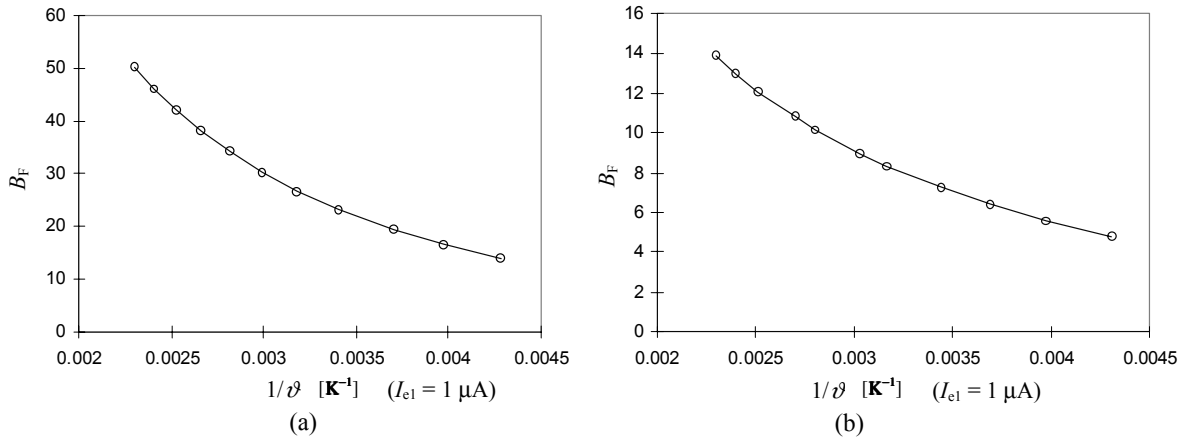


Figure 3.11 The temperature dependency of the current gain for (a) 0.7-µm CMOS, and (b) 0.5-µm CMOS.

The temperature dependence of B_F is plotted in Figure 3.11. Both items in equation (3.16) are temperature dependent. If the contribution of the term $W^2/(2L_P^2)$ is neglected, the current gain can be simplified to:

$$B_F = \frac{D_B}{D_E}\cdot\frac{n_{iB}^2}{n_{iE}^2}\cdot\frac{N_E}{N_B}\cdot\frac{L_E}{W_B} = \frac{D_B}{D_E}\cdot\frac{N_E}{N_B}\cdot\frac{L_E}{W_B}\cdot\exp^{\frac{q(V_{gE}-V_{gB})}{k\vartheta}} = \frac{D_B}{D_E}\cdot\frac{N_E}{N_B}\cdot\frac{L_E}{W_B}\cdot\exp^{\frac{q\Delta V_g}{k\vartheta}} \qquad (3.17)$$

where V_{gE} = bandgap voltage of the emitter,
V_{gB} = bandgap voltage of the base.

The bandgap narrowing of the emitter due to the heavy doping concentration has been derived from the measured temperature dependence of the forward common-emitter current gain, while the temperature dependencies of the diffusion coefficients were neglected. It was found that $\Delta V_g \cong$ -55 mV for 0.7-µm CMOS and $\Delta V_g \cong$ -45 mV for 0.5-µm CMOS.

3.3.6 Base Resistances R_B

The series base resistances and the emitter resistances also contribute to the base-emitter voltage, as seen in Figure 3. 12. Thus the base-emitter voltage becomes

$$V_{BE} = \frac{mk\vartheta}{q}\cdot\ln\frac{I_C}{I_S} + I_B R_B + I_E R_E, \qquad (3.18)$$

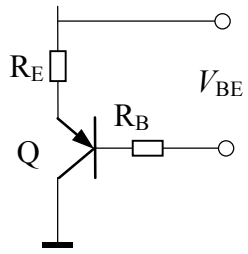


Figure 3. 12 The base and the emitter resistances contribute to the base-emitter voltage V_{BE}.

If the effects caused by the base resistance and the emitter resistance are taken into account, the voltage ΔV_{BE} becomes:

$$\Delta V_{BE} = \frac{mk\vartheta}{q} \cdot \ln r + \Delta I_B \left[R_B + (B_F + 1) R_E \right]. \tag{3.19}$$

Due to the fact that the emitter resistance is much lower than the base resistance, and to the fact that the common-emitter current gain is also low, the contribution of the emitter resistance to the voltage ΔV_{BE} can be neglected, thus:

$$\Delta V_{BE} \cong \frac{mk\vartheta}{q} \cdot \ln r + \Delta I_B \cdot R_B = \frac{k\vartheta}{q} \cdot \left[m + \frac{(r-1)}{(B_F + 1)\dfrac{k\vartheta}{q} \ln r} I_{E1} R_B \right] \ln r \,, \tag{3.20}$$

where m is the effective emission coefficient, r the emitter current ratio I_{E2}/I_{E1}, B_F the forward current gain and R_{B} the base resistance.

Figure 3.13(a) shows the normalized measured ΔV_{BE} versus I_{E1}. The slope θ of the curves is

$$\theta = \frac{r-1}{(B_F + 1)\dfrac{k\vartheta}{q} \ln r} \left[R_B + (B_F + 1) R_E \right]. \tag{3.21}$$

Neglecting the effect of emitter resistance, equation (3.21) can be rewritten as

$$R_B = \frac{\theta (B_F + 1)\dfrac{k\vartheta}{q} \ln r}{(r-1)} \,. \tag{3.22}$$

From the measurement results of ϑ, B_{F} and r, we can derive the base resistance R_{B} for different temperatures. The results are shown in Figure 3.13(b). At higher temperatures ($\vartheta >$ 373 K), for 0.7-µm CMOS, the high injection effect already occurs at relatively low currents, so that the correct base resistance cannot be extracted (see Figure 3.13(a1)).

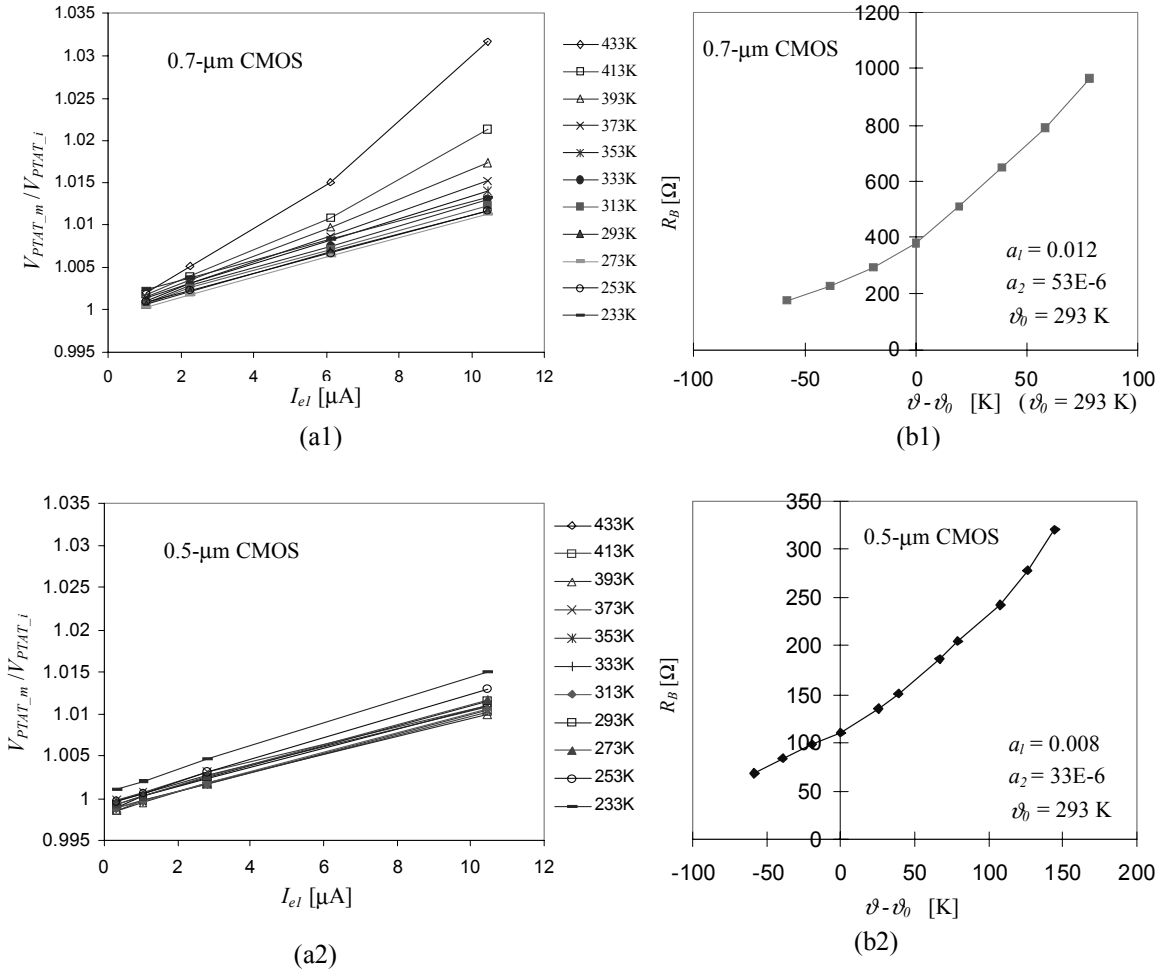


Figure 3.13 (a) the measured normalized ΔV_{BE} voltage, and (b) the extracted R_B versus temperature for devices with an emitter area of 10µm×20µm.

Above presented is a new method to measure the base resistance of a bipolar transistor. The existing methods to measure the base resistance include DC methods and AC methods [3.7]. The DC methods include δV_{BE}-$1/B_{\mathrm{F}}$ measurement and two-base contact measurement. In the δV_{BE}-$1/B_{\mathrm{F}}$ method, one measures the voltage deviation δV_{BE} from the logarithmic position under constant base current versus different current gains. From the plotted δV_{BE} versus the reciprocal current gain $1/B_{\mathrm{F}}$, the base resistance is derived in the combination with the R_{E} measurement. This method requires multiple devices in the same lot with different current gains and assumes that all devices have the same base resistance and emitter resistance. For this method the saturation current I_{S} and the emitter resistance must also be measured.

Another DC method to measure the base resistance requires a specially designed transistor with two separate base contacts, B_1 and B_2. The base current is only allowed to flow through one of the two contacts, for instance through contact B_1, while contact B_2 is left open. Both the voltage V_{B1E} and V_{B2E} are measured. The base resistance is derived from

$$R_B = \frac{V_{B1E} - V_{B2E}}{I_B}. \tag{3.23}$$

This method is simple and easy. However, it requires a specially designed layout, which deviates from the conventional design. Also the Kelvin voltage of V_{B2E} represents only the potential difference of the emitter in the closest position to the base B_2, which is not exactly the comprehensive base-emitter junction voltage.

The AC methods to measure the base resistance include the *input impedance circle method*, the *phase cancellation method* and the *frequency response method.* The *input impedance circle method* and the *frequency response method* require measurements over a wide frequency range, which are quite time consuming. The *phase cancellation method* also requires measurements at a high frequency of a few MHz, and is only suitable for transistors with $\beta > 10$.

Compared to the existing methods to measure the base resistance, the new method presented in this section is much more suitable for the specific application for temperature sensors and bandgap references, because the base resistance is derived at the similar working status.

The first-order and second-order temperature coefficients a_1 and a_2 of the base resistance are shown in Figure 3.13. These are much higher than those of the n-well resistances in 0.7-µm and 0.5-µm CMOS technology (a_1 = 0.0049/K for 0.7-µm CMOS and a_1 = 0.0043/K for 0.5-µm CMOS). This can be explained by the fact that the high injection effect already occurs in this current range. This also explains the fact that the a_1 of the base resistance in 0.7-µm CMOS is higher than that in 0.5-µm CMOS, because the high injection effect in 0.7-µm CMOS occurs earlier than that in 0.5-µm CMOS for transistors with the same emitter area size (see Table 3.2).

3.4 Effects Affecting the Accuracy of $V_{BE}(I_C, \vartheta)$ and $\Delta V_{BE}(I_C, \vartheta)$

3.4.1 The Base Resistances R_B

For two reasons, in CMOS technology the contribution of the base resistance to the base-emitter voltage is larger than that in bipolar technology, due to the larger series base resistance and the lower forward current gain in CMOS technology. When we take into account the voltage drop on base resistance, the base-emitter voltage becomes:

$$V_{BE} = V_{BE\_j} + I_B R_B = V_{BE\_j} + I_E \frac{R_B}{B_F + 1}, \tag{3.24}$$

where V_{BE_j} is the base-emitter junction voltage, which follows the ideal exponential relation. For instance, when the base current is 1 µA, according the measurement results shown in Figure 3.13(b1), the error due to the base resistance is about 1 mV at 373 K (0.7-µm CMOS device). This corresponds to a temperature error of 0.5 K.

The contribution of $I_B R_B$ to the base-emitter voltage depends on the temperature dependence of the emitter current. As shown in Figure 3.13(a1), the slope of the curves θ of the normalized ΔV_{BE} versus current I_{E1} is almost insensitive to temperature. In another word, θ is almost constant in our measurement. From equation (3.22) we can conclude that $R_B/(B_F+1)$ has a good PTAT behaviour. Consequently, the contribution of the base resistance $I_B R_B$ to base-emitter voltage approximately shows the PTAT property for a constant emitter current. The contribution of base resistance $I_B R_B$ to voltage ΔV_{BE} has a similar PTAT property. In this

case the effect of $I_B R_B$ in a bandgap reference or a temperature sensor can be corrected while performing trimming. But for an emitter current with the PTAT behaviour, which is conventional in real circuit design, the contribution of the base resistance to the base-emitter voltage depends on the square of the absolute temperature (ϑ^2), which causes a non-linearity to the base-emitter voltage.

The relative effect of the base resistance for the voltage ΔV_{BE} is stronger than for the base-emitter voltage. For instance, with ΔI_B = 1 μA and R_B = 100 Ω (Figure 3.13(b2) at room temperature), the contribution is 100 μV; suppose that ΔV_{BE} is designed to be 30 mV at room temperature, then the relative contribution is 0.3 %, corresponding to a temperature error of 1 K.

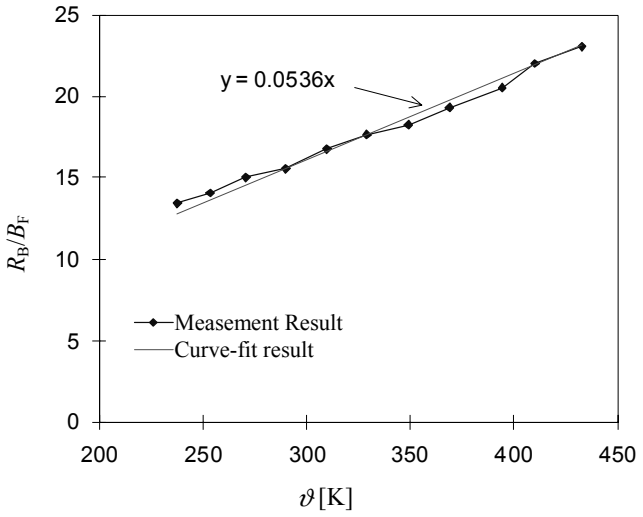


Figure 3.14 R_B/B_F versus temperature for the device fabricated in 0.5-μm CMOS technology.

The contribution of the base resistance voltage drop to the base-emitter voltage and to the voltage ΔV_{BE} can be reduced by decreasing the emitter current and/or using a multi-emitter geometry to reduce the value of the base resistance. There is a trade-off between the emitter current and a low injection effect.

3.4.2 The Forward Current Gain B_F

In section 3.3, the $V_{BE}(I_C, \vartheta)$ behaviour was analysed, where I_C was derived from the measurements of the emitter current I_E and the base current I_B.

In a practical application, it is much simpler to use the emitter current as a biasing current. However, due to the low current gain, the base current cannot be neglected. In this case, the base-emitter voltage will be expressed as:

$$V_{BE}(I_E,\vartheta) = V_{g0}\left(1-\frac{\vartheta}{\vartheta_r}\right)+\frac{\vartheta}{\vartheta_r}V_{BE}(\vartheta_r)-\eta\frac{k\vartheta}{q}\ln\frac{\vartheta}{\vartheta_r}+\frac{k\vartheta}{q}\ln\frac{I_E(\vartheta)}{I_E(\vartheta_r)}+\frac{k\vartheta}{q}\ln\left[\frac{1+\dfrac{1}{B_F(\vartheta_r)}}{1+\dfrac{1}{B_F(\vartheta)}}\right]. \quad (3.25)$$

The last term in equation (3.25) represents the contribution of the base current to the V_{BE} due to the temperature dependency of the forward common-emitter current gain. According to the measurement results shown in Figure 3.11, it is -0.5 mV ~ 1 mV for 0.7-μm CMOS, and -1 mV ~ 2 mV for 0.5-μm CMOS, respectively. For a precise bandgap reference, this term must be taken into account and compensated for in the circuit design. Figure 3.15 shows a circuit that is designed for base current compensation. The collector current of Q_1 is

$$I_{C1} = \frac{I_1 + \frac{I_1}{(B_F + 1)}}{\frac{(B_F + 1)}{B_F}} \approx I_1 . \tag{3.26}$$

In this way, the circuit reduces the contribution of the base current significantly. The main disadvantage of this circuit is that it requires a minimum supply voltage of

$$V_{DD,\min} = 2V_{BE} + V_{sat} , \tag{3.27}$$

where V_{sat} represents the saturation voltage of MOS transistors, which is about 0.3 V. Equation (3.26) gives a minimum supply voltage of about 1.7 V. This limits the low-voltage application.

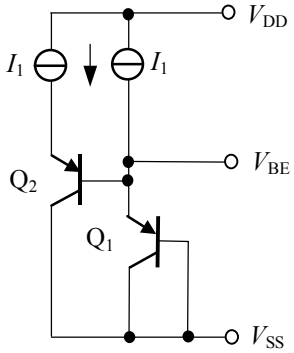


Figure 3.15 The schematic circuit used to compensate the effect of B_F.

Due to the low current gain, and the fact that emitter-current ratio is controlled, the collector current ratio differs from the emitter current ratio as follows:

$$\frac{I_{C2}}{I_{C1}} = \frac{I_{E2}}{I_{E1}} \cdot \frac{1 + \frac{1}{B_F(I_{E1})}}{1 + \frac{1}{B_F(I_{E2})}}, \tag{3.28}$$

which affects the ΔV_{BE} voltage:

$$\Delta V_{BE} = \frac{mk\vartheta}{q} \cdot \ln\frac{I_{E2}}{I_{E1}} + \frac{mk\vartheta}{q} \cdot \ln\left[\frac{1 + \frac{1}{B_F(I_{E1})}}{1 + \frac{1}{B_F(I_{E2})}}\right], \tag{3.29}$$

where the last term represents the contribution by the current dependence of the current gain. The measurement results in Figure 3.10 show that in the intermediate current range, the

current gain B_F hardly depends on the emitter current. Therefore, the second term in equation (3.29) can be neglected. An important consequence is that the collector-current ratio can be controlled quite accurately via the emitter-current ratio. Over the current range of 0.1 µA to 10 µA, the relative change in ΔV_{BE} due to the current dependence of the current gain is less than 0.05% for 0.7-µm CMOS, and less than 0.08% for 0.5-µm CMOS, respectively.

3.4.3 Effective Emission Coefficient *m*

When the effective emission coefficient m is taken into account, the base emitter voltage is

$$\begin{aligned} V'_{BE}(I_C,\vartheta) &= mV_{g0}\left(1-\frac{\vartheta}{\vartheta_r}\right)+\frac{\vartheta}{\vartheta_r}\cdot V_{BE}(\vartheta_r)-m\eta\frac{k\vartheta}{q}\cdot\ln\left(\frac{\vartheta}{\vartheta_r}\right)+\frac{mk\vartheta}{q}\cdot\ln\left[\frac{I_C(\vartheta)}{I_C(\vartheta_r)}\right] \\ &= V'_{g0}\left(1-\frac{\vartheta}{\vartheta_r}\right)+\frac{\vartheta}{\vartheta_r}\cdot V_{BE}(\vartheta_r)-\eta'\frac{k\vartheta}{q}\cdot\ln\left(\frac{\vartheta}{\vartheta_r}\right)+\frac{mk\vartheta}{q}\cdot\ln\left[\frac{I_C(\vartheta)}{I_C(\vartheta_r)}\right]. \end{aligned} \tag{3.30}$$

Equation (3.30) shows that the effective emission coefficient m does not cause a serious problem for the base-emitter voltage, because the extracted parameters, V'_{g0} and η' already included this effect. The minor error in the last term of (3.30) is negligible.
However, the effective emission coefficient m directly affects the voltage ΔV_{BE}, as in

$$\Delta V_{BE}=\frac{mk\vartheta}{q}\cdot\ln\left[\frac{I_{C2}}{I_{C1}}\frac{I_{S1}}{I_{S2}}\right]. \tag{3.31}$$

It affects the temperature-sensing signal and the bandgap-reference signal. Fortunately, this effect can be canceled in the circuit design of temperature sensors and bandgap references, where the base-emitter voltage can be calibrated. But if the circuits cannot be calibrated, their accuracy is affected. According to equations (2.19) and (2.20), the errors amount to:

$$\frac{\delta K}{K}\approx\frac{(m-1)A_1\frac{k}{q}\ln(rp)}{\lambda+A_1\frac{k}{q}\ln(rp)} \tag{3.32}$$

and

$$\frac{\delta V_{ref}}{V_{ref}}\approx\frac{(m-1)A_2\frac{k\vartheta}{q}\ln(rp)}{V_{BE}+A_2\frac{k\vartheta}{q}\ln(rp)}, \tag{3.33}$$

respectively, where K is the temperature sensitivity of the temperature-sensor signal, r the bias current ratio, and p the emitter area ratio of the ΔV_{BE} circuit, respectively.

The small deviation of m from unity, for instance 0.1%, will contribute to the error in the final signal of the temperature sensor and that in the bandgap-reference signal, which amount to 0.05%. Usually, circuits that cannot be calibrated do not require high accuracy: an error of 0.05% is acceptable.

3.4.4 High Injection Effect

The high injection effect occurs when the concentration of injected minorities in the base has the same order as the base doping concentration. In this current range, the effective emission coefficient m tends to go from one to two. In this case, both the voltages V_{BE} and ΔV_{BE} deviate from the ideal values. This results in large errors in the temperature-sensor signal and the bandgap-reference signal.

To obtain high accuracy, the designer has to minimize the high injection effect and the effect of the base resistance. This can be achieved by selecting the emitter current in the range where a good exponential relation in the $V_{BE}(I_C, \vartheta)$ characteristics is found.

3.4.5 Low Injection Effect

At low emitter currents and/or high temperatures, the low injection effect cannot be neglected. The injection effect occurs when the magnitude of the saturation current I_S is not negligible with respect to I_C. In this case, for the collector current, it holds that

$$I_C = I_S\left(e^{\frac{qV_{BE}}{mk\vartheta}}-1\right)+I_S\left(e^{\frac{-qV_{BC}}{k\vartheta}}-1\right)+\frac{I_S}{B_R}\left(e^{\frac{-qV_{BC}}{k\vartheta}}-1\right)+I_{gen}-I_{rec}, \tag{3.34}$$

where V_{BC} is the voltage across the base-collector voltage, B_R is the reverse current gain, I_{gen} and I_{rec} are the generation and recombination current in the base-collector junction respectively. When the base and the collector are connected to ground, and the small voltage caused by the base resistance can be neglected, the voltage across the base-collector junction is zero. Moreover, the generation current and the recombination current in the base-collector junction are then balanced. In this case, the equation for the base-emitter voltage can be simplified, where it holds that

$$V_{BE} = \frac{mk\vartheta}{q}\cdot\ln\left(\frac{I_C+I_S}{I_S}\right)=\frac{mk\vartheta}{q}\cdot\ln\left(\frac{I_C}{I_S}\right)+\frac{mk\vartheta}{q}\cdot\ln\left(1+\frac{I_S}{I_C}\right), \tag{3.35}$$

where the second term represents the deviation from the ideal logarithmic behavior.

Using equation (3.35), we can express the voltage ΔV_{BE} in this case as:

$$\Delta V_{BE} = \frac{mk\vartheta}{q}\cdot\ln\left(\frac{I_{C2}+I_{S2}}{I_{C1}+I_{S1}}\cdot\frac{I_{S1}}{I_{S2}}\right). \tag{3.36}$$

So the voltage $\Delta V_{BE}(\vartheta)$ deviates from the ideal PTAT behavior here.

To avoid the effect of low injection, the transistor should satisfy the condition $I_C/I_S >> 1$. A large emitter current and/or a small emitter size will make it easy to meet the requirement. The optimum emitter current level is a trade-off between the effect of the base resistance and the low injection effect.

3.4.6 The Thermal Effect

Self-Heating

Power consumption causes self-heating of the chip. For a temperature sensor, this results in an error in temperature measurement. Suppose that a thermal resistance R_{Th} exists between the chip and the ambient environment, and that the power consumption of the chip is P, then in the stationary condition the difference in temperature between the chip and the ambient $\Delta\vartheta$ is [3.8]

$$\Delta\vartheta = PR_{TH} . \tag{3.37}$$

The thermal resistance is dependent on the type of packaging and on the packaging material. For instance, suppose that the power consumption of a temperature sensor is 4 mW. In case of a plastic package, the thermal resistance to the still air would amount to 203 K/W [3.8]. Then, the temperature error due to self-heating would amount to 0.8 K, which is quite large. With a ceramic DIL package, the temperature error would be 0.5 K.

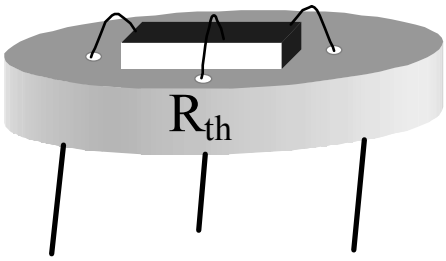


Figure 3.16 Power consumption causes self-heating.

In order to reduce the error caused by self-heating, we must reduce the power consumption of the temperature sensors, and/or reduce the thermal resistance.

Besides by designing low power temperature sensors, we can also reduce the error caused by self-heating, by having the temperature sensor operate periodically (on stand-by if not used), or to do a temperature measurement directly after start-up. In this way, the average power consumption is reduced.

Thermal Gradient

Another problem is the thermal gradient on-chip, which causes errors in the base emitter voltage and the voltage ΔV_{BE}. To calculate the thermal gradient, we used the half-sphere model in [3.8] as shown in Figure 3. 17.

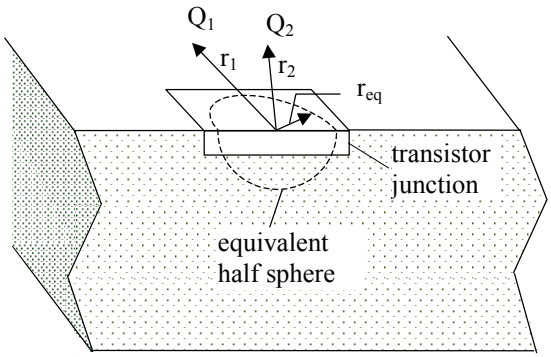


Figure 3. 17 Self-heating and thermal gradient caused by a flat transistor on the surface of a silicon chip.

Suppose that the power-consuming device is located on at the surface of a silicon chip. The thermal resistance can be calculated by

$$R_{TH} = \frac{1}{2\pi\kappa r_{eq}}, \tag{3.38}$$

where κ thermal conductance of silicon and r_{eq} is the equivalent radius of the power-consuming device, which is given by

$$r_{eq} = \sqrt{\frac{A}{2\pi}}, \tag{3.39}$$

where A is the area of the power-consuming device. Using κ = 142 W/K/m, and the assumption that the area of the power-consuming device is 1000 μm^2, equation (3.38) yields a thermal resistance of 89 K/W. So a power of 5 mW results in a self-heating of 0.4 K.

Suppose that the two transistors Q_1 and Q_2 are located at distances r_1 and r_2 away from the power-consuming device, respectively. Then the temperature difference between Q_1 and Q_2 can be calculated by

$$\vartheta_1 - \vartheta_2 = \frac{P}{2\pi\kappa} \cdot \left(\frac{1}{r_1} - \frac{1}{r_2} \right). \tag{3.40}$$

For example, r_1 = 200 μm, r_2 = 300 μm, and the power-consuming device generates a power of 5 mW; then the temperature difference of the two transistors is 0.01 K.

According to equation (2.14), a small temperature change will cause a change in the base emitter voltage:

$$\begin{aligned} \delta V_{BE}(\vartheta) &= V_{BE}(\vartheta + \Delta\vartheta) - V_{BE}(\vartheta) \\ &\approx -\lambda(\Delta\vartheta) \end{aligned}. \tag{3.41}$$

Suppose that three transistors, Q_1, Q_2 and Q_3, are used to generate the basic signals for a temperature sensor. While Q_1 is used to generate the base-emitter voltage, Q_2 and Q_3 are used to generate the voltage ΔV_{BE}. Due to the thermal gradient, the temperatures of $Q_2(\vartheta_2)$ and $Q_3(\vartheta_3)$ deviate from the temperature ϑ_1. In this case, the temperature-sensor signal amounts to

$$\begin{aligned} V'(\vartheta) &= \pm\{V_{BE}(\vartheta_1) - A_1(V_{BE3}(\vartheta_3) - V_{BE2}(\vartheta_2))\} \\ &= \pm\{V_{BE}(\vartheta_1) - A_1(V_{BE3}(\vartheta_1) - V_{BE2}(\vartheta_1)) + A_1(\lambda_3\Delta\vartheta_3 - \lambda_2\Delta\vartheta_2)\}. \\ &= \pm\{V(\vartheta_1) + \underbrace{(A_1(\lambda_3 - \lambda_2)\Delta\vartheta_3}_{\delta_1} \underbrace{- A_1\lambda_2(\vartheta_2 - \vartheta_3))}_{\delta_2}\} \end{aligned} \tag{3.42}$$

Similarly, the bandgap-reference signal becomes

$$\begin{aligned} V_{ref}'(\vartheta) &= \{V_{BE}(\vartheta_1) + A_2(V_{BE3}(\vartheta_3) - V_{BE2}(\vartheta_2))\} \\ &= \{V_{BE}(\vartheta_1) + A_2(V_{BE3}(\vartheta_1) - V_{BE2}(\vartheta_1)) + (-A_2(\lambda_3\Delta\vartheta_3 - \lambda_2\Delta\vartheta_2))\}. \\ &= \pm\{V_{ref}(\vartheta_1) + \underbrace{(-A_2(\lambda_3 - \lambda_2)}_{\delta_1}\Delta\vartheta_3 + \underbrace{A_2\lambda_2(\vartheta_2 - \vartheta_3))}_{\delta_2}\} \end{aligned} \tag{3.43}$$

It is found that the thermal gradient between the two transistors applied for generating the voltage difference ΔV_{BE} causes a significant error (δ_2). Suppose that there is a temperature difference of 0.01 K between Q_1 and Q_3, and that the same temperature difference exists between Q_2 and Q_3. Then δ_1 and δ_2 are 20 µV and 400 µV, respectively.

In order to reduce the effect of the thermal gradient, one should locate the transistors, which are used to generate voltage ΔV_{BE}, as far as possible from the power-consuming components on the chip, and to place the transistors as close to them as possible. Using the cross connection of a quad structure can also help to compensate the effect of the temperature gradient.

3.4.7 Freeze-Out Effect

As the temperature decreases, the thermal agitations may become insufficient to keep donors fully ionized. Some of the free electrons are then trapped by donors and become immobile. This phenomenon is called the freeze-out effect. Figure 3.18 shows the temperature dependency of the majority-carrier concentration for two different doping concentrations [3.9], [3.10]. Figure 3.18 shows that the higher the doping concentration, the higher the temperature at which the freeze-out takes place.

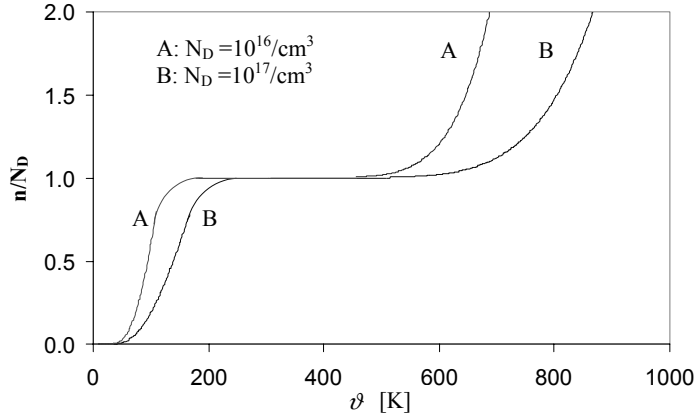


Figure 3.18 The temperature dependence of the majority-carrier concentration in a doped semiconductor (Si with a phosphorus-doped).

For the freeze-out region, the saturation current of the bipolar transistor expressed in equation (2.3) is rewritten as

$$I_S' = \frac{q^2 n_i^2 A_E D_B}{Q_B'}, \tag{3.44}$$

where

$$Q_B' = q\int_{x_E}^{x_C} N_B^+ dx, \tag{3.45}$$

N_B^+ is the concentration of the ionized dopant. The base emitter voltage at low temperatures, due to the freeze-out effect will be:

$$V_{BE}'(\vartheta) = V_{BE}(\vartheta) + \frac{k\vartheta}{q}\ln\frac{I_S}{I_S'}, \tag{3.46}$$

where the second term represents the deviation from the ideal characteristics under the assumption of full ionization. Due to $I_S' > I_S$, from equation (3.46), the freeze-out effect causes a negative deviation of the base-emitter voltage.

According to equation (2.21), the voltage ΔV_{BE} depends on the applied collector-current ratio and the saturation current ratio. Since the freeze-out effect does not affect the saturation current ratio of two bipolar transistors, the voltage ΔV_{BE} is not affected by it.

3.4.8 Piezo-Junction Effect

The differences in the Thermal Coefficient of Expansion (TCE) of the different materials of wafers and packages cause mechanical stress, which is temperature dependent and time varying. The stress-induced change in $I_C(V_{BE})$ characteristic of a bipolar transistor is the main source of long-term drift and hysteresis during thermal cycling or changes in humidity of bandgap references, [3.10], [3.11]. Although silicon has no mechanical hysteresis, many materials such as epoxy and plastic do show features of viscoelasticity, which are responsible for mechanical hysteresis in the silicon die. The geometry and material properties of the

moulding material directly affect the stress characteristics. Normally, low-cost plastic packages introduce high mechanical stress and hysteresis in a silicon die [3.11].

The stress-induced change in the $I_C(V_{BE})$ characteristic of bipolar transistors is called the piezo-junction effect. The piezo-junction effect is anisotropic and its magnitude depends on: a) the amount and orientation of the stress, b) the current direction through the base, c) the minority carrier type in the base, and d) the temperature. The silicon wafer axis is the reference for the stress orientation and current direction. Most of the industrial IC processes use the [100] wafer crystal orientation as a standard. Therefore, piezo-junction effects for transistors implemented in this wafer crystal orientation were investigated by F. Fruett and J.F. Creemer.

It was found that the piezo-junction effect in V_{BE} causes approximately 80% of the total output error induced by stress in a commercial temperature sensor SMT160-30 [3.11]. This temperature sensor was fabricated in a conventional BiCMOS process and generates the signals (V_{BE} and ΔV_{BE}) using npn transistors. Another way to generate the signals (V_{BE} and ΔV_{BE}) is to use pnp substrate transistors, which can be implemented in n-well CMOS technology. The different type of minority carriers in the base causes different stress sensitivity for pnp substrate and for npn transistors.

The stress affects the base-emitter voltage by changing the saturation current I_S in the following way:

$$\frac{\Delta I_S}{I_S} = \frac{\Delta n_i^2}{n_i^2} + \frac{\Delta \mu_B}{\mu_B} + \frac{\Delta Q_B}{Q_B}, \tag{3.47}$$

where the intrinsic carrier concentration n_i and the mobility in the base μ_B are stress dependent, and the last term, Q_B changes with the stress-induced geometry deformation. The stress dependence of the mobility varies with the type of minority in the base.

A test structure containing both types of transistors was designed. Due to the symmetrical crystal orientation of the [100]-oriented silicon wafer, the stress-induced change of the transistor characteristic lies between two limits for any stress oriented in the wafer plane. The uniaxial stress orientations [100] and [110] determine these two limits [3.12], [3.13]. The transistors have been tested for uniaxial stress in these orientations, and the results are shown in Figure 3.19.

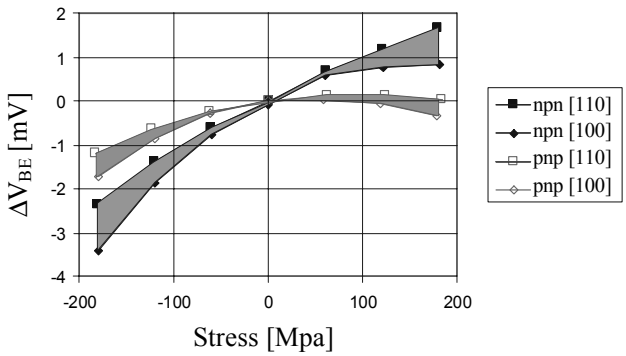


Figure 3.19 The stress-induced change in V_{BE} for the npn and pnp substrate transistors for an arbitrary stress orientation.

For an arbitrary compressive (negative) or tensile (positive) stress oriented in the wafer plane, the change in base-emitter voltage V_{BE} is in the shaded areas. Based on this result we can conclude that:

- The stress-induced change in V_{BE} of a pnp substrate transistor is smaller than that of a npn transistor;
- Both transistors are less sensitive to tensile stress than to compressive stress.

As a conclusion, we recommend using the pnp substrate transistors as these provide better performance in terms of long-term stability.

Recently, Fruett and Meijer [3.14] found that the voltage ΔV_{BE} is much less sensitive to stress than the base-emitter voltage V_{BE} itself. This can easily be explained by the fact that the voltage ΔV_{BE} only depends on the bias-current ratio and on the saturation-current ratio. The stress-induced change in the saturation current is cancelled out in the voltage ΔV_{BE}. Figure 3.20 shows the stress-induced error normalised for temperature for the signals V_{BE} and ΔV_{BE} generated using pnp substrate transistors.

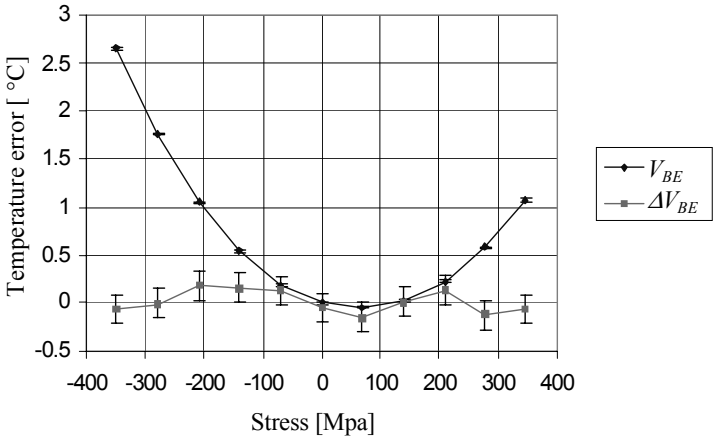


Figure 3.20 Measured temperature error due to the stress-induced change in V_{BE} and ΔV_{BE} for pnp substrate transistors.

To reduce the stress-induced error in the base-emitter voltage, one should

- Use a pnp bipolar transistor as the basic device to generate the voltage signal V_{BE};
- Package the IC in such a way that the package-induced stress is in the tensile range.

3.5 Conclusions

This chapter described the characterization of substrate bipolar transistors fabricated in CMOS technology (0.7-µm and 0.5-µm).

Using the measurements of $I_C(V_{BE}, \vartheta)$, we showed that in a moderate current range, a good exponential relation between the base-emitter voltage the collector current exists. It appears that the temperature behavior of the base-emitter voltage can be well modelled with the well-known Gummel-Poon model. The negative correlation between the extracted parameters V_{go} and η is similar to that reported earlier for bipolar technology.

The forward common-emitter current gain B_F has also been derived over a wide emitter current and temperature range. Compared to the value of B_F of bipolar transistors fabricated in bipolar technology, the value of B_F of substrate bipolar transistors fabricated in CMOS technology is much lower. This is due to the fact that the base width of substrate bipolar transistors in CMOS is much larger than that of those fabricated in bipolar technology. The larger Gummel number results in a lower forward common-emitter current gain.

The base resistance was extracted from the measured voltage ΔV_{BE}, the emitter current and the emitter current ratio I_{E2}/I_{E1}. For this we used a new method to extract the base resistance.

The effective emission coefficient m was extracted in two ways: from the measured $I_C(V_{BE})$ curve, and from the ΔV_{BE} measurements. The results showed good agreement. The results showed that the effective emission coefficient m of the devices in CMOS technology is very close to the ideal value of unity.

The following conclusions address the effects that affect the behavior of the base-emitter voltage V_{BE}.

The base resistance causes an unexpected voltage drop, which increases the external base-emitter voltage V_{BE} and the voltage ΔV_{BE}. This voltage drop can be reduced by selecting a low biasing current, or by using a multiple emitter structure. A trade-off must be made between the biasing emitter current and the low injection effect.

For those transistors that are biased via the emitter currents, the base-emitter voltage is also affected by the forward common-emitter current gain. The temperature dependence of the forward common-emitter current gain causes an error in the base-emitter voltage. Using the schematic circuit in Figure 3.15, we compensated for this effect at the cost of an increased supply voltage.

In the moderate current range, the forward common-emitter current gain is insensitive to the emitter current, and therefore the collector-current ratio can be controlled as accurately as the emitter-current ratio. This means that the voltage ΔV_{BE} can be controlled accurately by controlling the emitter current ratio.

The effect of the effective emission coefficient m was already taken into account when we extracted the parameters V_{g0} and η. However, it will directly affect the accuracy of the voltage ΔV_{BE}. Fortunately, the measurement results show that the effective emission coefficient is very close to the ideal value of unity.

We recommend biasing transistors, which are used to generate the base-emitter voltage V_{BE} and ΔV_{BE} voltage, in the appropriate current range: that where the low injection effect and the high injection effect are avoided over the whole temperature range. In the low injection range, the $I_C(V_{BE})$ characteristic deviates from the ideal exponential relationship; other minor contributions to the collector current must be taken into account. In the high injection range, on the other hand, the effective emission coefficient m tends to become 2 instead of unity.

Self-heating will introduce an error in temperature sensors. Using a package with good thermal conductance and minimizing the average power dissipation of the temperature sensors will reduce this error. It is important to reduce the thermal gradient between the transistors, which are used to generate the ΔV_{BE} voltage. The transistors used to generate ΔV_{BE} voltage should be placed as close as possible to each other in a cross quad configuration, and as far away as possible from the dissipating components.

The freeze-out effect occurs at low temperatures, when the dopant is not completely ionized. In this case, the saturation current I_S is larger than that for complete ionization, resulting in a smaller base-emitter voltage. The freeze-out effect does not affect the voltage ΔV_{BE}, because the ΔV_{BE} voltage only depends on the saturation-current ratio of two transistors and on the biasing collector-current ratio.

The package-induced stress, which is environment dependent, causes the base-emitter voltage to deviate from the value under zero stress. This piezo-junction effect causes errors, both in temperature sensors and bandgap references. The saturation current I_S of a bipolar transistor changes with applied stress because the mobility and the intrinsic carrier concentration are both stress dependent. Experimental results show that pnp vertical transistors are less stress sensitive than npn transistors. Tensile stress causes the base-emitter voltage to change less than compressive stress. Experimental results also proved that the ΔV_{BE} voltage is insensitive to mechanical stress, because this voltage is only dependent on the saturation current ratio of the transistor pair, where the stress-induced change in saturation currents are cancelled out. Thus, we recommend using the substrate pnp vertical transistor to generate the base-emitter voltage, and ensuring that the chip is packaged in such a way that the package-induced stress remains in the tensile range.

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Chapter 4 Advanced Techniques in Circuit Design

4.1 Introduction

Until now, CMOS bandgap-voltage references and the temperature sensors were much less accurate and had less long-term stability than their bipolar counterparts. The low accuracy of the CMOS voltage references and temperature sensors is due to mismatching of components, drift, temperature effects, 1/*f* noise and mechanical stress. As a result of the larger mismatching of components in CMOS technology, the applied operational amplifiers have a higher offset voltage. Moreover, CMOS transistors show larger 1/*f* noise than bipolar ones. This is due to the fact that MOS transistors are surface devices. The current flows near the surface, where the higher density of crystal imperfections results in higher flicker noise (1/*f* noise).

Recently, in [4.1] - [4.7], it was shown that a major part of the CMOS problems can be solved by applying advanced techniques in circuit design, such as auto-zeroing, auto-calibration, the chopping technique and dynamic element matching (DEM). The applicability of these techniques depends on the type of circuit to be designed.

In this chapter, two types of circuits will be distinguished:

- Circuits with a continuous-time analog output.
- Circuits with a sampled and/or modulated discrete output.

For some circuits, for instance for A/D or D/A converters, a continuous-time reference is required. An external or on-chip reference circuit must be designed with a continuous-time analog output. However, for others, such as sensor interface circuits, the way in which the output is designed is not stringent: both above-mentioned types of output are suitable. The applicability of the advanced techniques determines which type of circuit is to be chosen.

In circuits with a continuous-time analog output, auto-zeroing and chopping can be applied to reduce the offset of the OPAMP and the 1/*f* noise. For instance [4.8], in Figure 4.1, the offset of the op-amp will affect the accuracy of the bandgap reference. For the output voltage V_{ref}, it holds that

$$V_{ref} = V_{BE2} + \left(1 + \frac{R_2}{R_1}\right) \cdot \left(\Delta V_{BE} + V_{OS}\right), \tag{4.1}$$

where $\Delta V_{\mathrm{BE}}(T)$ equals

$$\Delta V_{BE} = \frac{kT}{q} \cdot \ln n. \tag{4.2}$$

For instance, with V_{OS} = 1 mV, n = 3 and R_2/R_1 = 23, the error of the output voltage due to the offset of the op-amp amounts to 23 mV. The error due to the offset of the op-amp can be reduced significantly by applying a chopping technique. But the error due to the mismatch between the transistors Q_1 and Q_2 remains.

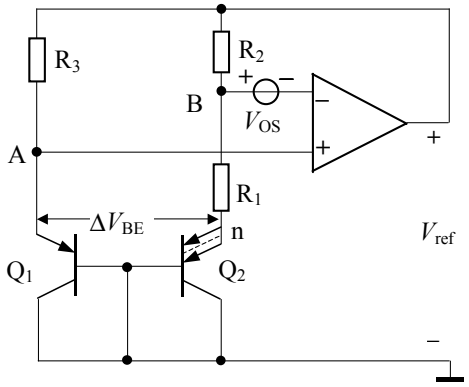

Figure 4.1 The schematics of the bandgap references in CMOS technology.

However, for circuits with a discrete output, one has a more flexible choice of advanced techniques. For instance, in a circuit as shown in Figure 4.2, the DEM technique can be applied to eliminate the mismatching error. Thus, one can obtain an accurate value for ΔV_{BE}. Furthermore, the chopping technique can be used to reduce offset. The information of the bandgap reference is obtained by further data processing performed by a microcontroller.

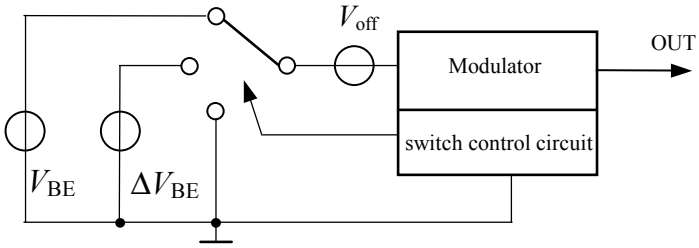

Figure 4.2 The schematics of bandgap references in CMOS technology.

The dynamic bandgap reference in Figure 4.2 is of no use unless it is combined with another measurement. For instance, an unknown voltage signal is processed by the same modulator in Figure 4.2. The voltage to be measured is derived with respect to the dynamic bandgap reference. In this case a three-signal technique is used to derive the voltage signal.

The microcontroller plays an important role in these types of systems. It measures the outputs of the modulator, stores the data in its memory, processes the data and communicates with other digital systems, like a PC.

This chapter will discuss the advanced techniques that can be applied to the circuit with a discrete output. The modulator that fits the application in combination with the microcontroller will also be discussed. The performance of the modulator will be analysed, too.

4.2 Three-Signal Technique

The three-signal technique is a technique [4.2], which can be applied to eliminate the effects of offset and an unknown gain factor in a system. The application of this technique requires, in addition to the measurement of the sensor signal E_x, the measurement of two reference signals in an identical way: E_{ref1} and E_{ref2}. The measurement of these three signals results in three output signals: F_x, F_{ref1} and F_{ref2}, respectively. When the transfer function is linear, there is a linear relation between E and F, according to the equation

$$F = a_1 E + a_0 ; \tag{4.3}$$

the final measurement result M amounts to

$$M \overset{def}{=} \frac{F_x - F_{ref1}}{F_{ref2} - F_{ref1}} = \frac{E_x - E_{ref1}}{E_{ref2} - E_{ref1}} . \tag{4.4}$$

This result does not depend on a_0 and a_1. Furthermore, it is permitted that E_{ref1} equals zero. In this case, only one reference signal E_{ref2} and an arbitrary offset are required. The effect of the drift of a_0 and a_1, due to, for instance, temperature changes or aging, can be eliminated by applying (4.4), periodically or continuously.

To obtain an accurate result, one muse use a linear transfer function, as non-linearity will cause a measurement error. Suppose that the transfer function has a minor second-order relation between E and F,

$$F = a_0 + a_1 E + a_2 E^2 , \tag{4.5}$$

then the ratio M in (4.4) becomes

$$M \approx \frac{E_x - E_{ref1}}{E_{ref2} - E_{ref1}} \left\{ 1 + \frac{a_2}{a_1} \left(E_x - E_{ref2} \right) + \left(\frac{a_2}{a_1} \right)^2 \left(E_x + E_{ref1} \right) \left(E_{ref2} + E_{ref1} \right) \right\}, \tag{4.6}$$

the second and the third term in the braces represent the measurement error due to the second-order relation in the transfer function.

Usually, the three-signal measurement is time-multiplexed, so that, one measurement cycle consists of three measurement phases. The application of the three-signal technique requires a memory to store the values of F and a calculation unit. These two key functions are usually implemented by using a microcontroller.

4.3 Modulators

The modulator in Figure 4.2 converts the voltage signals to signals that can be measured by a microcontroller or a microprocessor. In fact, the modulator and microcontroller converts the signals from analog to digital. First, the modulator converts sensor signals to time domain, and then, the microcontroller measures the time signals with its time reference and converts them to a digital signal. The reasons to use a microcontroller are:

- Low cost.

- High level of support with both hardware and software.
- Rapid prototyping.
- Memory function.
- Data processing.

Thus the selection of the modulators depends on whether or not the modulators can work with a microcontroller. The output signal of the modulator should be readable by the microcontroller. Meanwhile, in view of low cost and high performance, the modulators should fulfil the following requirements:

- Absolute accuracy: 10 bits to 16 bits,
- Conversion speed: 1 ms to 100 ms,
- Chip area: as small as possible,
- Power supply: single 3 V to 5 V supply voltage, and
- Power consumption: as low as possible.

The modulators with output signals readable for a microcontroller mainly use:

- Duty-cycle modulation (DCM). The information is stored in the duty cycle of the output signal of the modulator.
- Inverse period modulation where the information is stored in the inverse of the period (IPM).
- Period modulation where the information is stored in the period (PM).

In the next section, we will compare these forms of modulation with respect to their performance and the applicability of advanced techniques.

4.3.1 Selection of Modulator

Since IPM converts the input signals into a period in a non-linear way, one cannot apply the three-signal technique in this circuit. Therefore we will not use IPM in our design.

The choice between DCM and PM mainly depends on the quantization noise and on a fundamental non-ideality of the usually applied modulator: the delay time of the relaxation oscillator.

Quantization Noise

The time period T is measured by a microcontroller by its counting function. The process of quantization is shown in Figure 4.3. After the quantization, the duration of the time interval T is indicated by the counted number of the clock period of the microcontroller.

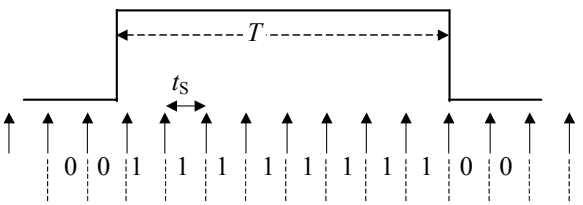

Figure 4.3 The process of quantization.

The quantization errors are created while digitising period T: one at the beginning, and one at the end of T. Every single quantization is assumed to have a mean of $t_S/2$ and a uniform distribution between 0 and t_S. Thus the variance of a single quantization amounts to [4.9]

$$\sigma^2 = \frac{1}{t_s}\int_0^{t_s}\left(t - \frac{1}{2}t_s\right)^2 \mathrm{d}t = \frac{t_s^2}{12}. \tag{4.7}$$

Since the quantization error at the beginning and that at the end of T are not correlated, the total variation is simply the sum of both and is equal to $2\sigma^2$. Since both counting's at the beginning and at the end are delayed, the mean error of a complete measurement of T is zero. The standard deviation of the relative error due to the quantization noise is given by

$$\varepsilon = \frac{\sqrt{2}\sigma}{T} = \frac{1}{\sqrt{6}} \cdot \frac{t_S}{T}. \tag{4.8}$$

Equation (4.8) shows that the resolution and the measurement time are linearly related. For example, the time T required to achieve a 16-bit resolution with a 1MHz sampling frequency is 26.7 ms. The application of three-signal technique requires at least three signals. The total measurement time will be in the order of 100 ms. This is acceptable for a sensor measurement system.

As we will see later, the modulator period is much shorter that the required 26.7 ms. To obtain the same 16-bit resolution with the same sampling frequency, we need to take into account a large period. The number of required periods, N, depends on how the data is stored in the signal.

For a DCM signal with a period of T_{mod}, as shown in Figure 4.4, the variance of the duty cycle D due to the quantization noise is

$$\sigma_D^2 = \left(1 + D^2\right)\frac{2\sigma^2}{T_{\mathrm{mod}}^2} = \left(1 + D^2\right)\frac{t_s^2}{6T_{\mathrm{mod}}^2}. \tag{4.9}$$

The standard deviation of the relative error of D is then given by

$$\varepsilon_{DCM} = \frac{\sigma_D}{D} = \sqrt{\left(1 + D^2\right)}\frac{1}{\sqrt{6}}\frac{t_s}{DT_{\mathrm{mod}}}. \tag{4.10}$$

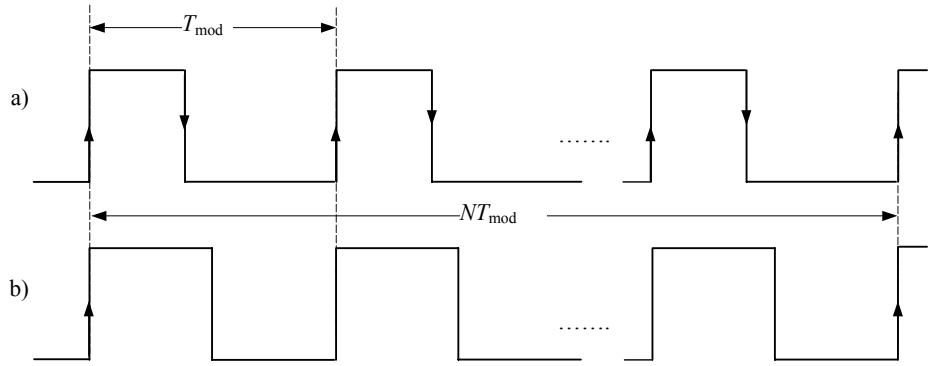

Figure 4.4 The output signal of the modulator for a) duty cycle or b) period modulation.

When N periods are measured, the quantization error is made at every edge. These errors are not correlated. The standard deviation of the relative error of D, based on N periods, is given by

$$\varepsilon_{DCM,N} = \frac{1}{\sqrt{N}} \sqrt{\left(1+D^2\right)} \frac{1}{\sqrt{6}} \frac{t_s}{DT_{\text{mod}}}. \tag{4.11}$$

For the same number N of the PM output signal, however, the quantization only takes place at the beginning and at the end of NT_{mod}, so that the standard deviation of the relative error due to quantization noise is

$$\varepsilon_{PM,N} = \frac{\sqrt{2}\sigma}{NT_{\text{mod}}} = \frac{1}{\sqrt{6}} \frac{t_s}{NT_{\text{mod}}}. \tag{4.12}$$

For example, with T_{mod} = 100 µs, D = 0.5, t_s = 1 µs, DCM requires 286×10^3 periods to obtain a 16-bit resolution, corresponding to 29 s measurement time, while PM requires only 267 periods, corresponding to 26.7 ms measurement time.

In view of the quantization noise, PM is preferred.

4.3.2 Voltage-to-Period Converter

There are several possibilities to realize voltage-to-period modulation. A first-order relaxation modulator contains only one integrator [4.10], see Figure 4.5. It converts the voltage signal (V_h-V_l) into a time duration. First, the capacitor is charged with a positive current. When the voltage level reaches the high threshold voltage V_h, the output of the upper comparator changes from high to low. The latch circuit generates a trigger signal to reverse the sign of the current source. Then the capacitor is discharged. When the voltage level reaches the low threshold voltage V_l, the output of the lower comparator changes from high to low. The latch circuit generates a trigger signal to change the sign of the current source to positive. For a complete cycle, the time duration is determined by the equation

$$T = \frac{2C\left(V_h - V_l\right)}{I}, \tag{4.13}$$

where the time duration is determined by three parameters: the capacitance, the voltage and the current. Changing any of these parameters will modulate the period.

For voltage measurement, the unknown voltage is connected at the position of V_h or V_l.

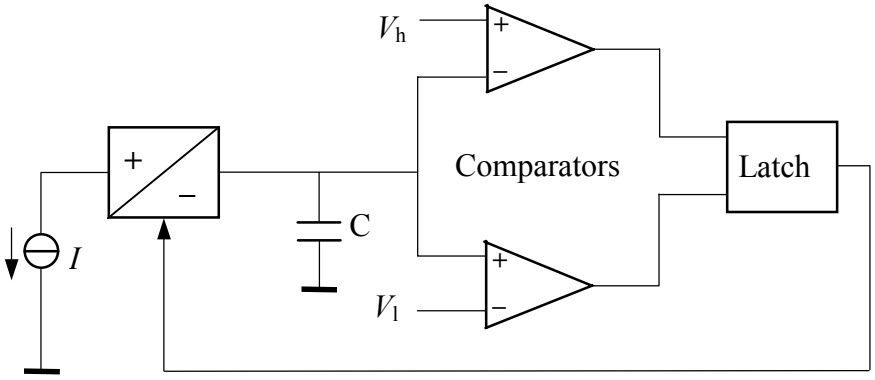

Figure 4.5 A typical first-order relaxation oscillator.

The main disadvantage of using the relaxation oscillator shown in Figure 4.5 is that it has a limited input voltage range. When the input voltage is very small or zero, the oscillation frequency is too high. In this case, it is difficult to keep the oscillator working properly. In order to prevent this problem, a so-called offset voltage is needed, which is in series connected with the input voltage. This makes the circuit complicated.

Instead of adding an offset voltage to ensure that the oscillator works properly, one can add a so-called offset capacitor. This is demonstrated in the so-called modified Martin oscillator [4.11], [4.12], shown in Figure 4.6.

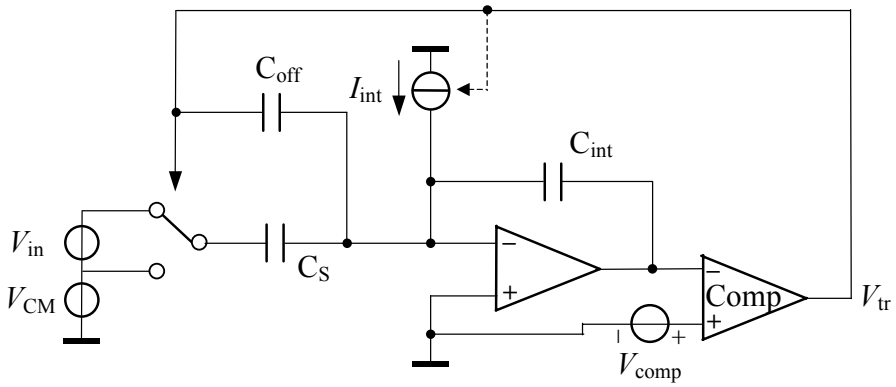

Figure 4.6 The schematic circuit of the modified Martin oscillator.

The output of the comparator V_{tr} directly controls the switch for the signal sampling and the direction of current I_{int}. When the voltage level of the comparator changes from high to low, the capacitor C_{off} injects a charge $V_{tr}C_{off}$ into the integrator capacitor. Simultaneously, the sampling capacitor injects a charge $V_{in}C_S$ into the integrator capacitor. The total amount of injected charge ($V_{tr}C_{off} + V_{in}C_S$) results in a voltage step at the output of the integrator. The current I_{int} is applied to discharge the integrator capacitor, forcing the output of the integrator back towards the voltage V_{comp}. When the integrator output voltage equals V_{comp}, the voltage level of the comparator output changes from low to high, resulting in a charge $-(V_{tr}C_{off} + V_{in}C_S)$ transferred to the integrator and in a reversal of the current I_{int}. The next time when the voltage of the integrator equals V_{comp}, the comparator output changes from high to low. This process repeats. Some signals in the circuit are shown in Figure 4.7.

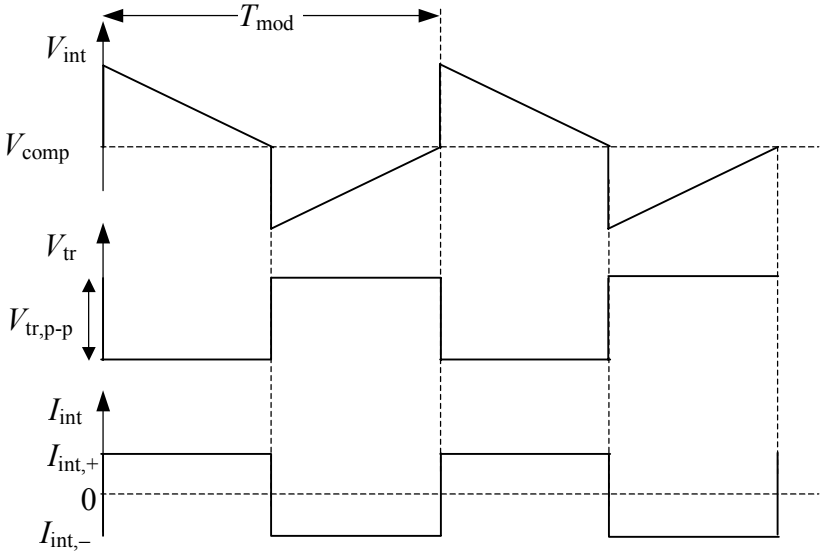

Figure 4.7 The signals in the modified Martin oscillator.

The time interval T_{mod} is:

$$T_{\mathrm{mod}} = \frac{V_{tr}C_{off} + V_{in}C_S}{I_{\mathrm{int},+}} + \frac{V_{tr}C_{off} + V_{in}C_S}{I_{\mathrm{int},-}}. \tag{4.14}$$

When $\left|I_{\mathrm{int,+}}\right| = \left|I_{\mathrm{int,-}}\right| = \left|I_{\mathrm{int}}\right|$, (4.14) becomes

$$T_{\mathrm{mod}} = \frac{2\left(V_{tr}C_{off} + V_{in}C_S\right)}{\left|I_{\mathrm{int}}\right|}. \tag{4.15}$$

The offset capacitor C_{off} ensures proper oscillation when the input voltage is zero or even negative.

The advantages of the modified Martin oscillator are high linearity, high resolution and great accuracy.

By adding some switches and a phase-selection circuit, one can easily implement the three-signal technique. One possible circuit applying the three-signal technique is shown in Figure 4.8.

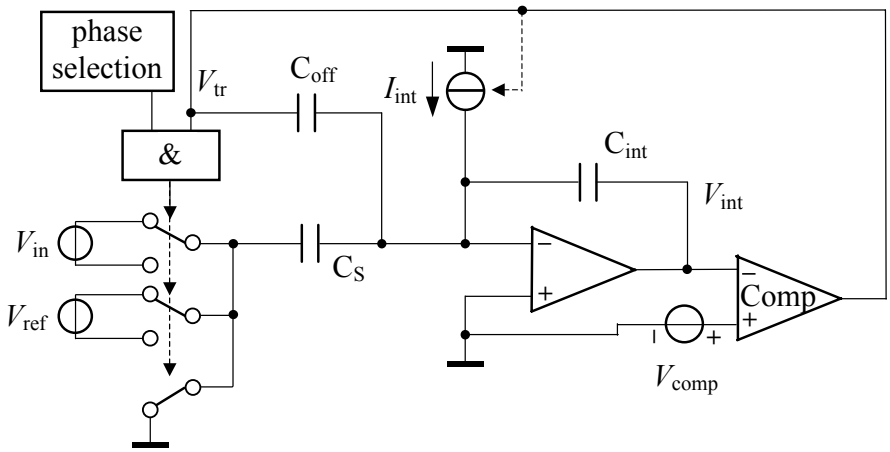

Figure 4.8 The three-signal technique is applied to the modified Martin oscillator.

Figure 4.9 shows a charge-balancing oscillator [4.13], which has the same advantage as the modified Martin oscillator.

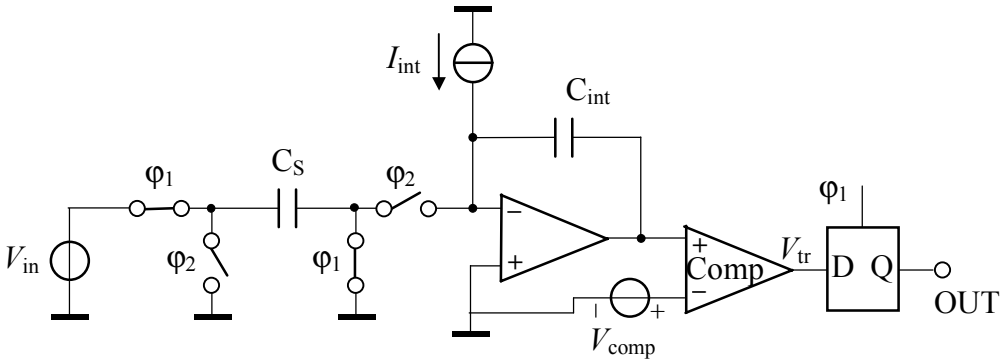

Figure 4.9 A typical charge-balancing oscillator for capacitance or voltage measurement.

When the voltage of the integrator output is higher than the threshold voltage $V_{\text{threshold}}$, the integration current is set to charge the integration capacitor, resulting in a decrease of the voltage V_{int}. In this case, φ_1 is high and φ_2 is low, so the integrator is isolated from the input-signal source V_{in}: the interference on the input-signal source cannot affect the integrator output. Once the voltage V_{int} is lower than the threshold voltage $V_{\text{threshold}}$, the voltage at the comparator output changes from high to low, which reverses φ_1 and φ_2. During this moment, the charge at the sampling capacitor $V_{\text{in}}C_S$ is transferred to the integrator capacitor, resulting in a voltage change of the integrator output. The comparator reacts and the integration current starts to discharge the integration capacitor again. The signals of the circuit in Figure 4.9 are shown in Figure 4.10. The time interval of the period depends linearly on the input voltage, according to the equation

$$T_{\text{mod}} = \frac{2V_{in}C_S}{I_{\text{int}}} + 2T_{delay}\,. \tag{4.16}$$

In a similar way as shown in Figure 4.8, the three-signal technique can easily be applied in the charge-balancing oscillator as well.

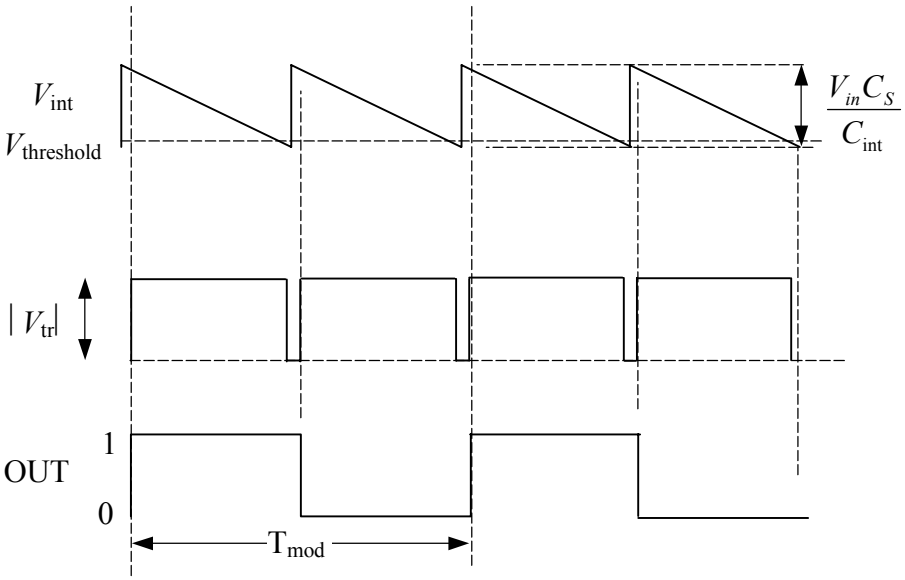

Figure 4.10 The signals in the charge-balancing oscillator.

However, the oscillator is sensitive to offset and low-frequency noise [4.14]. In order to reduce this non-ideality, we modified the circuit, as shown in Figure 4.11.

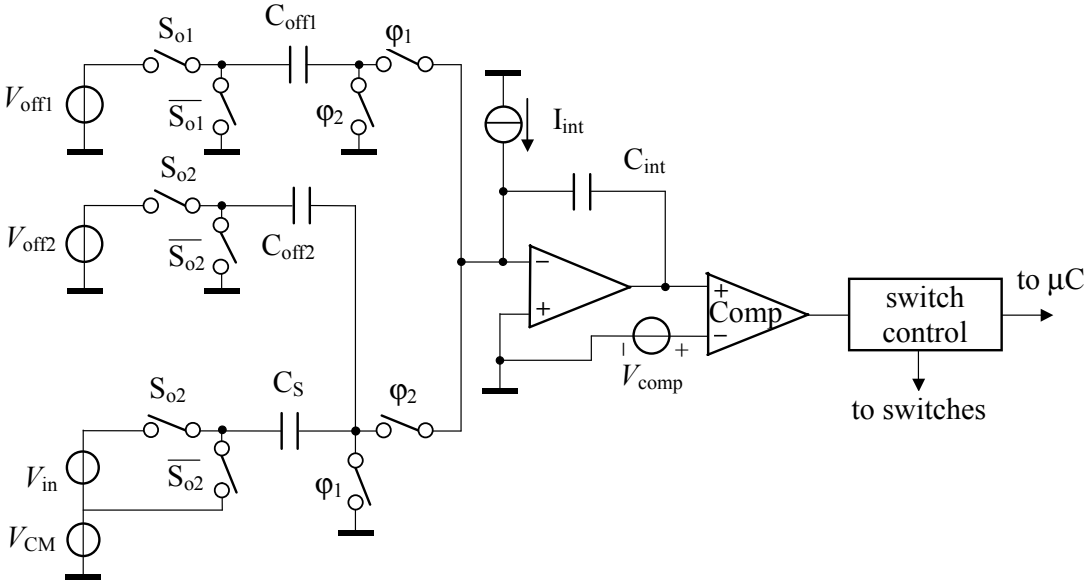

Figure 4.11 The modified charge-balancing oscillator for capacitance or voltage measurement according to [4.14].

The basic switch control signals for this circuit are shown in Figure 4.12. Charge is dumped into the integrator at the beginning of each time interval. At the beginning of $T_{1,i}(\varphi_1)$, only the capacitor C_{off1} dumps charge ($V_{off1}C_{off1}$) into the integrator, while the capacitors C_{off2} + C_S dump charge into the integrator at the beginning of $T_{2,i}(\varphi_2)$. This ensures proper oscillation, even when the input voltage is zero or negative.

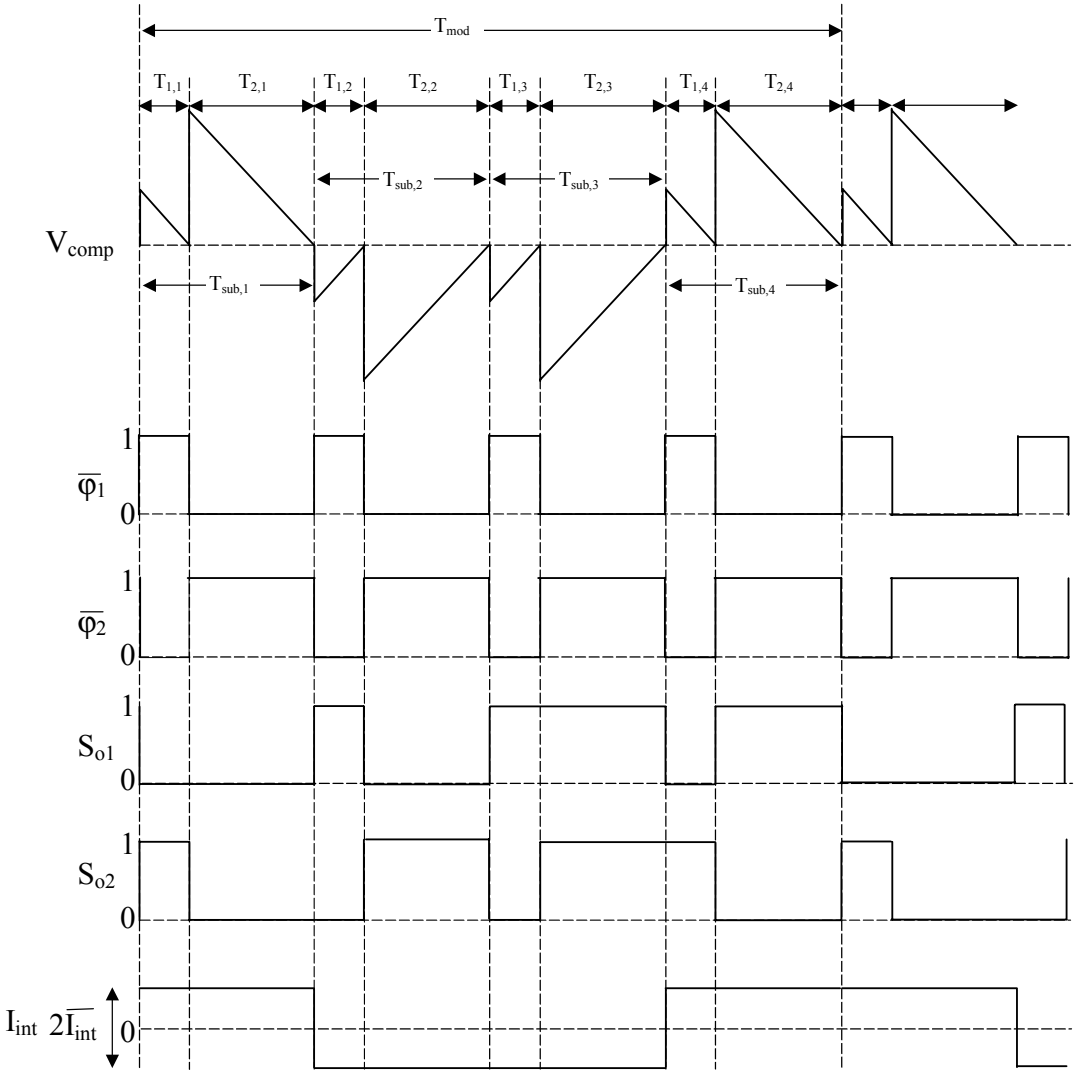

Figure 4.12 The signals in the modified charge-balancing oscillator.

The period of a complete sampling cycle, which includes four sub-sampling cycles, is

$$T_{\mathrm{mod}} = \frac{4C_{off1}V_{DD} + 4\left(V_{in}C_S + C_{off2}V_{DD}\right)}{\left|I_{\mathrm{int}}\right|}. \tag{4.17}$$

Here we still assume $\left|I_{\mathrm{int},+}\right| = \left|I_{\mathrm{int},-}\right| = \left|I_{\mathrm{int}}\right|$.

A chopping technique that will be described in section 4.4 has been applied in the modified charge-balancing oscillator. This significantly reduced the effects of offset of the integrator and the low-frequency noise and interference.

4.4 Chopping Technique

Many techniques have been developed to reduce offset and low-frequency noise (1/*f*) of an operational amplifier. For instance, the correlated double sampling (CDS) technique is applied

to reduce the offset of, for example, an op-amp [4.15]. The basic principle is that the offset and the low-frequency noise signals are stored during the first clock phase and are cancelled in the next clock phase when the signal is measured. By applying this technique properly, one cannot only reduce the offset and the low-frequency noise, but also the clock feed through noise induced by the switches. The subtraction of two samples at different time moments corresponds to filtering with a zero at zero hertz in the frequency domain. For real DC signals, all non-idealities are eliminated.

An alternative way to reduce offset and low-frequency noise is to apply the chopper-stabilization technique. The principle is to modulate the input signal, to move its spectrum from the baseband where the noise is largest, to amplify the modulated signal, and to restore it into the baseband. Figure 4.13 illustrates the basic scheme. The balanced modulator M_1 shifts the spectrum to a band around the carrier frequency, f_c, where it does not overlap with the large baseband spectrum of the $1/f$ noise. After amplification by A_1, modulator M_2 shifts the signal back into the baseband and moves the amplified $1/f$ noise to the vicinity of f_c. A low-pass filter is required to remove the modulated high-frequency offset and $1/f$ noise.

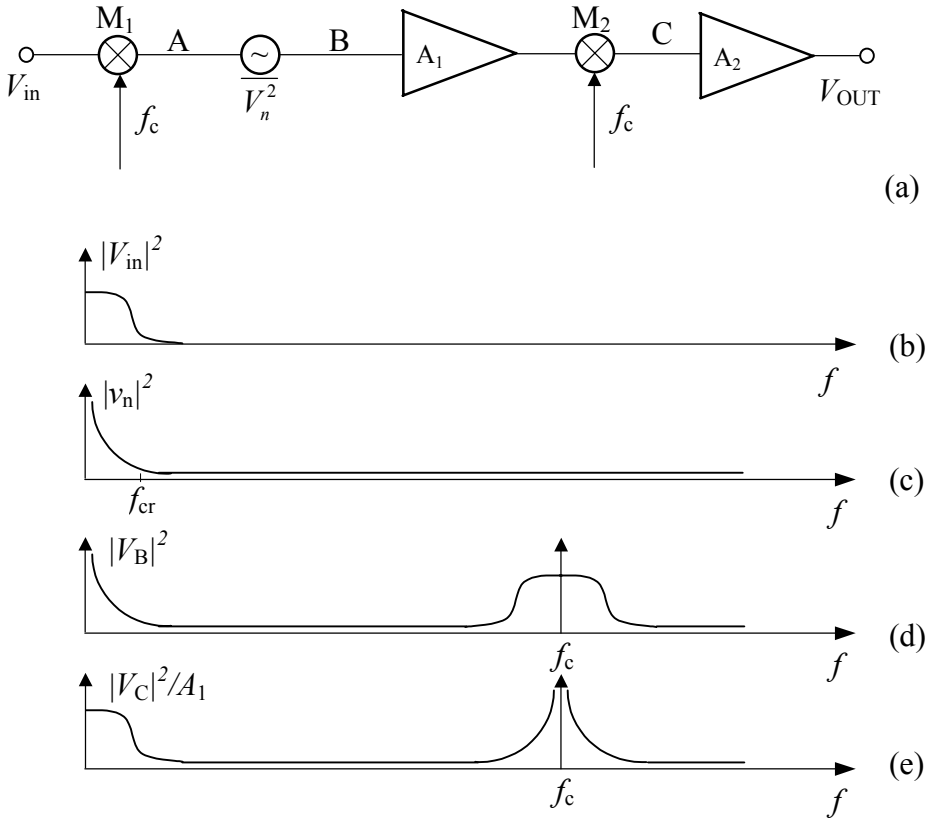

Figure 4.13 The chopper-stabilized amplifier circuit: a) a block diagram; b) the spectrum of the input signal; c) the noise spectrum; d) the spectrum at node B; e) the spectrum at node C.

Assuming that the chopper frequency is higher than the corner frequency of the $1/f$ noise, the residual noise is almost equal to the wide-band thermal noise. In [4.16] the chopping technique and the correlated double sampling (CDS) technique are compared. It is shown that with the chopper technique, the offset and low-frequency ($1/f$) noise are better suppressed than with the CDS technique.

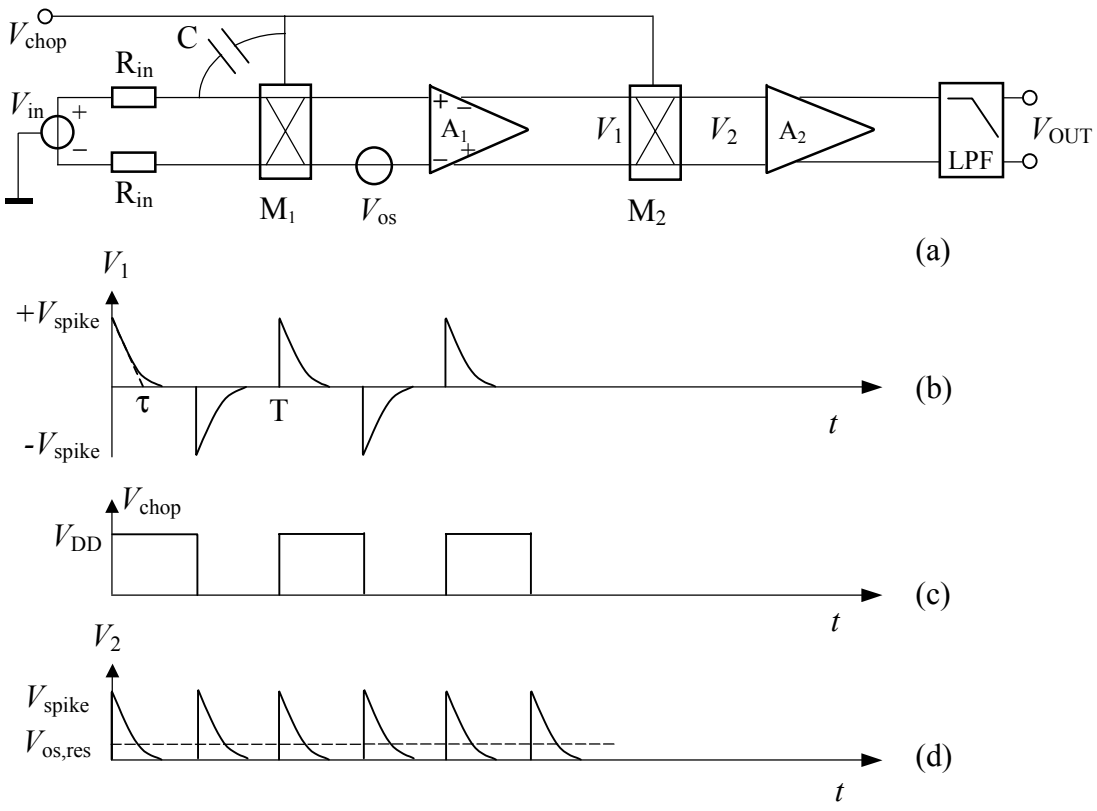

Figure 4.14 The residual offset of a chopper amplifier due to spikes a) the block diagram; b) the spike signal; d) demodulation signal; d) demodulated spikes.

The residual offset of a chopper amplifier is determined by clock-induced spikes, due to the switch-charge injection in the input chopper M_1 [4.16]. Figure 4.14 illustrates the spike signals, which are due to the time constant formed by the source impedance of the input signal R_{in} and the parasitic capacitance C. After demodulation and low-pass filtering, these spikes result in a DC voltage component $V_{os,res}$, for which it holds that

$$V_{os,res} = \frac{V_{spike}}{0.5T}\int_0^{0.5T} e^{-t/\tau}dt \approx \frac{2V_{spike}}{T}\int_0^{\infty} e^{-t/\tau}dt = \frac{2\tau}{T}V_{spike}\,. \tag{4.18}$$

In [4.17], a chopper amplifier with a band-pass filter is presented in which the residual offset is reduced. However, due to the matching limitation of the components in the circuit, the residual offset cannot be removed completely.

An alternative technique to reduce the residual offset is presented in [4.16]. The principle of this technique, called the nested-chopper technique, is shown in Figure 4.15.

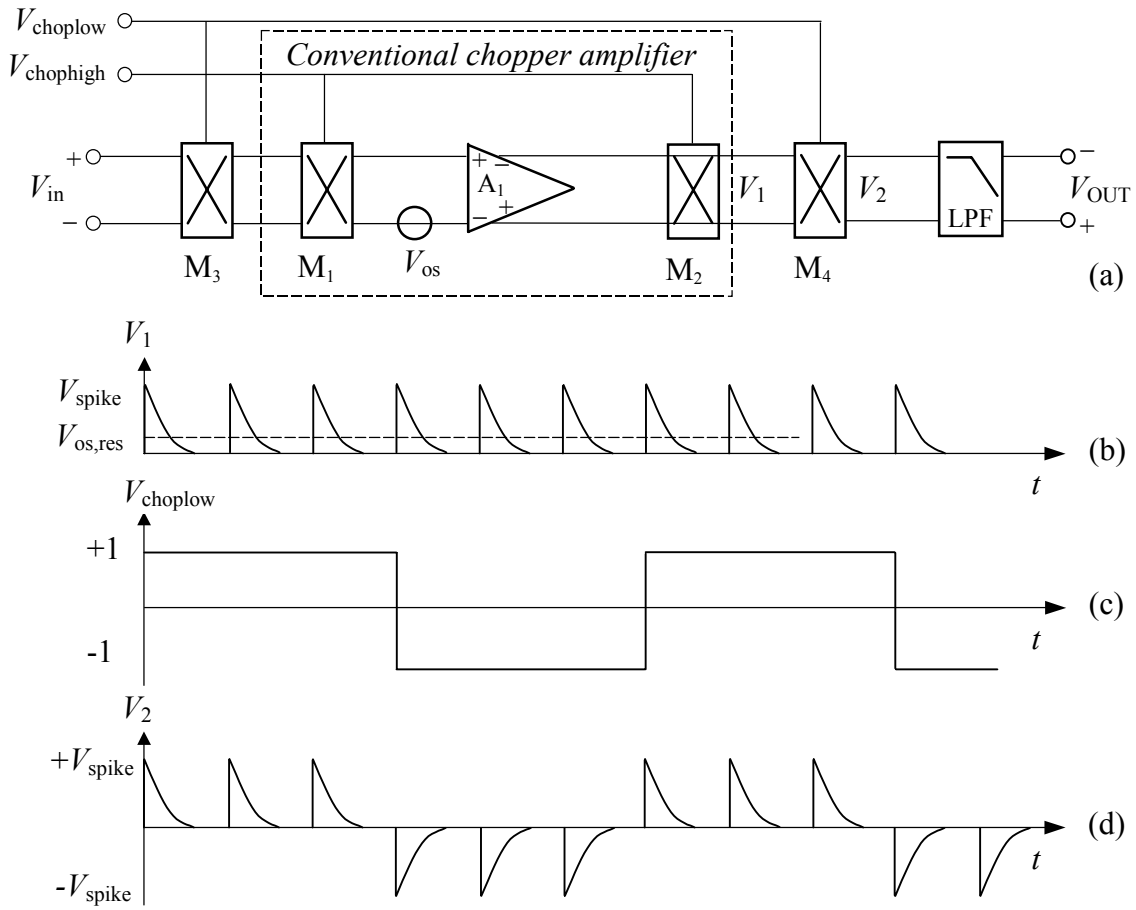

Figure 4.15 Reduction of the residual offset by the nested-chopper technique: a) the block diagram; b) the spikes after the first demodulator; c) low-frequency modulation signal; d) spikes after the second demodulator.

In the nested-chopper technique, except for the conventional chopping action, an additional outer chopping with a much lower frequency is applied. The conventional chopper amplifier reduces the offset and the 1/*f* noise, but causes a residual offset, due to the spikes. The outer chopping is applied to reduce the residual offset. The chopping frequency $f_{chophigh}$ of the inner chopper is chosen to be higher than the 1/*f* noise corner frequency, while the outer-chopping frequency $f_{choplow}$ is chosen in relation to the bandwidth of the input signal. Because the other chopper, M_2, will also suffer from clock-induced spikes, its frequency is chosen as low as possible. Usually, this frequency is chosen to be two times higher than the bandwidth of the input signal. For instance, if we look at a temperature sensor with a bandwidth of 10 Hz, the outer-chopper frequency can be as low as 20 Hz. With an inner-chopper frequency of 2 kHz, which is chosen in relation to the 1/*f* noise corner frequency, the residual offset can be reduced with a factor of 100, theoretically.

In [4.16] Bakker describes a nested-chopper amplifier, which has been designed and implemented using 1.6 µm CMOS technology. With an inner frequency of 2 kHz and an outer frequency of 16 Hz, an offset is reported of only 100 nV.

4.5 DEM Techniques

Dynamic Element Matching (DEM) is a known technique [4.3]-[4.5] to improve the overall accuracy of a system. It can be used when a number of nearly equal elements can be distinguished. By cyclically interchanging the position and the function of the elements over time, and taking the average over time, one obtains an overall relative accuracy that can be several decades better than the relative accuracy of the elements themselves.

4.5.1 DEM Amplification of Small Voltage Signals

Figure 4.16 shows a basic negative feedback configuration of a voltage amplifier. When the open-loop gain of the op-amp A_1 is ideal and infinite, the voltage amplification factor is determined by:

$$G = \frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1}. \tag{4.19}$$

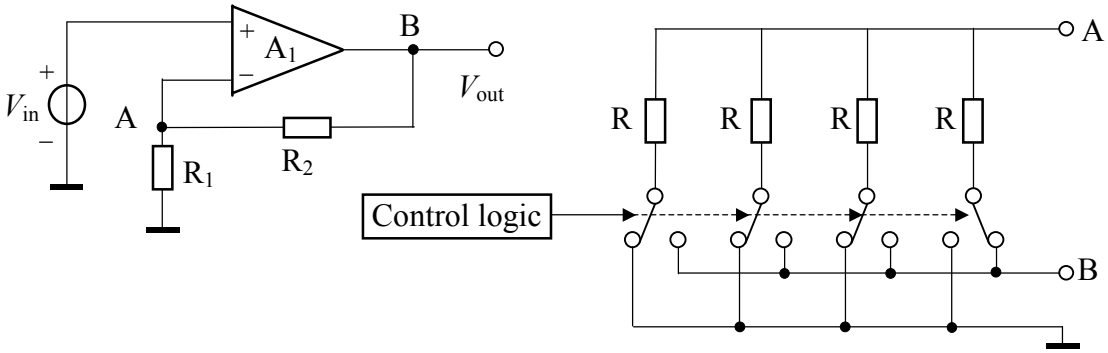

Figure 4.16 The schematic circuit of a general amplifier.

The accuracy of the amplification factor G is determined by the accuracy of the resistor ratio R_2/R_1. In order to improve the accuracy of the resistor ratio, DEM technique can be applied. In Figure 4.16, for example, an accurate resistor ratio of 3 is obtained. The DEM technique is applied by changing the position of four almost equal resistors successively; in each position state, one of the four nearly equal resistors is connected to the node B, in the position of R_2, and all other three are connected parallel to ground, in the position of R_1. After a complete cycle, which in this case includes four circuit states, the average of the resistor ratio R_2/R_1 will be closer to 3. The inaccuracy is reduced to a second-order effect of the mismatch.

The parasitic on-resistances of the switches in the feedback loop will affect the resistor ratio R_2/R_1, thus resulting in an error in the gain factor. Especially the on-resistances of the switches connecting the resistors in parallel to ground cannot be excluded from the feedback loop. In order to ensure that the on-resistances of the switches are negligible, the resistor of the feedback network must have a large resistance. However, this will be at the cost of a large chip area.

By applying force and sense wires in a different circuit configuration, one can eliminate the effect of the on-resistances of the switches. For example, in [4.5], P. C. de Jong *et al* presents

an instrumentation amplifier with DEM feedback. The principle of this amplifier is shown in Figure 4.17. The resistive feedback network consists of a chain of K matched resistors, which are hardware connected without any switch. The chain can be rotated by addressing of the appropriate force and sense switches. The feedback is realized by the u, v, and w resistors, respectively. Since the resistors are connected as a chain, a resistive load will be present which consists of z resistors. Therefore, it holds that

$$K \equiv u + v + w + z \,. \tag{4.20}$$

In this circuit configuration, the effect of the on-resistances of the switches S_1 to S_6 is completely eliminated by applying the force and sense wires. There are K states in a complete rotation of the feedback chain, so a resistor that is part of the load will become part of the feedback later. For this reason, this load resistor is essential to the functionality of the dynamic feedback. The average gain $\overline{G}$ of this amplifier over K successive states is equal to

$$A = \frac{u+v+w}{u} = 1 + \frac{v+w}{u} \,. \tag{4.21}$$

The mismatches between the resistors hardly affect the average gain, because there is an averaging effect over time when the resistors move along the chain. The resistor chain is controlled by a digital-state machine, which addresses the appropriate switches. Each successive state, the chain rotates one position. The control of the resistor chain requires that there are six switches connected to a single point between every two resistors, which results in a total of $6 \times K$ switches.

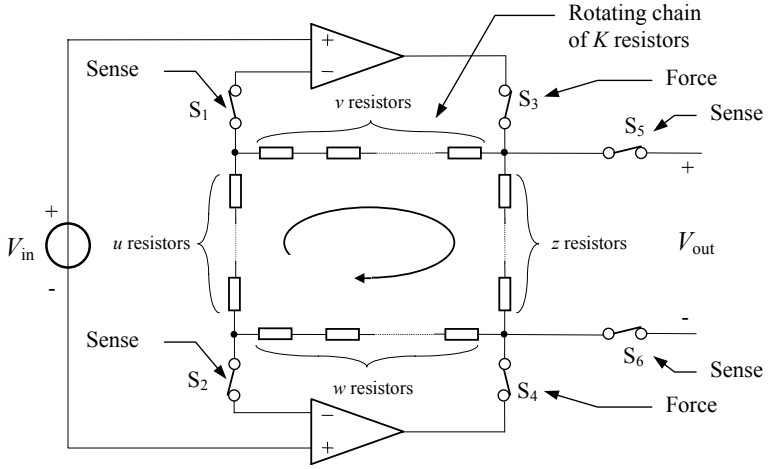

Figure 4.17 The instrumentation amplifier with dynamic feedback.

In [4.5], a DEM instrumentation amplifier is presented applying dynamic feedback, which has been fabricated in 0.7-um CMOS technology. Although the resistor mismatch is 0.1%, the relative inaccuracy is less than 5×10^{-6}. This amplifier has been applied to amplify a very small unbalance voltage of a resistive bridge transducer. The system block diagram is shown in Figure 4.18. Besides the amplifier, also a voltage divider was applied. In this way, both the voltage derived from the bridge and the small bridge-output voltage were brought within the limited linear input range of the signal processor.

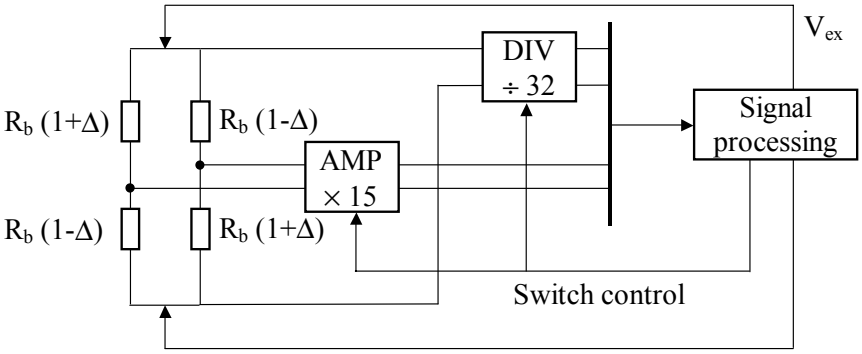

Figure 4.18 The instrumentation amplifier is applied in a bridge measurement system.

The limited common-mode (CM) input range of a DEM instrumentation amplifier limits its application. An alternative architecture for signal amplification can overcome this limitation. By applying switched capacitors in a DEM configuration [4.18] - [4.20], an accurate pre-amplifier can be realized for input voltage signals with a rail-to-rail CM level. Figure 4.19 illustrates the principle of such a switched-capacitor amplifier and the control signals for the switches.

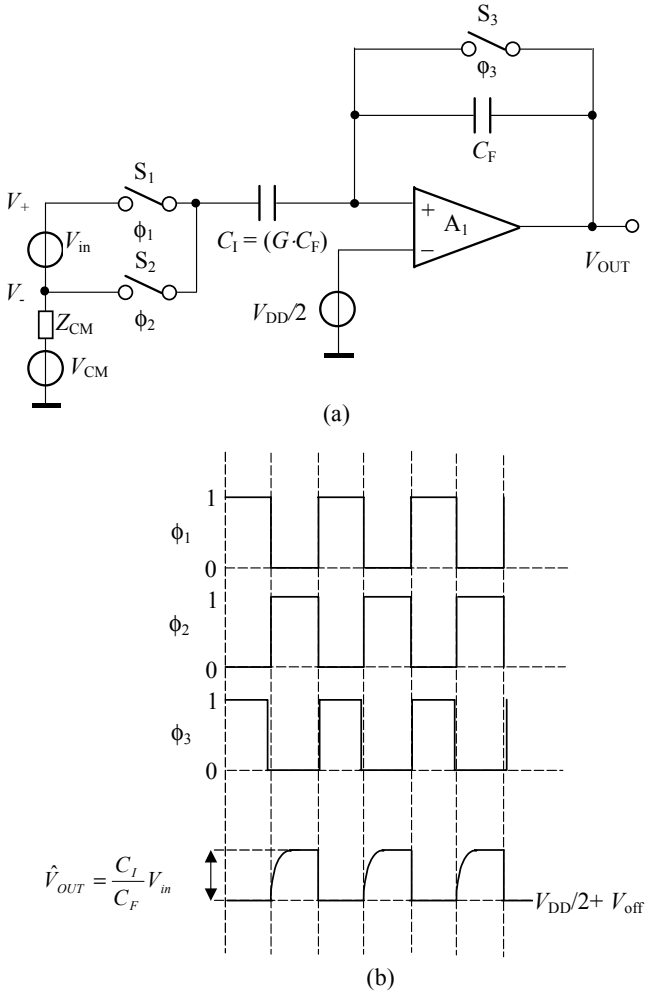

Figure 4.19. (a)The schematic circuit of switch capacitor amplifier and (b) the control signals.

The input voltage V_{in} is generated by the sensing elements, and can change slowly. The switches S_1 and S_2 control the signal sampling of the capacitor C_I; the switch S_3 is used to initialise the output. The change of the charge at the capacitor C_I will be transferred to the capacitor C_F, resulting in an output V_{OUT} with a peak-to-peak value of

$$\hat{V}_{OUT} = -\frac{C_I}{C_F} \cdot (V_+ - V_-) = G \cdot V_{in} . \tag{4.22}$$

This voltage is further processed by the signal processing circuit. The sampling switches limit the common-mode input range. The complementary switches ensure that the rail-to-rail common-mode input range can be achieved.

In this processing circuit, the signals will be sampled at the end of each clock cycle. Thus, when the time constant formed by the source resistor of the input voltage and the capacitors is much smaller than the period of the clock signal, this does not affect the accuracy of the amplification.

The gain is determined by the ratio C_I/C_F. Compared to the circuit of Figure 4.17, the advantages of this circuit are:

- A rail-to-rail CM level (0 V to V_{DD}) of the small input signal or even one that is slightly negative is allowed.
- The DC drift at the output due to the offset of the operational amplifier does not affect the measurement, as only the voltage difference at the op-amp output is further processed.

Applying the Dynamic-Element-Matching technique can reduce the inaccuracy caused by the mismatch of the two capacitors. This is demonstrated in the circuit shown in Figure 4.20.

In total, the feedback network contains $M + N$ identical capacitors, where M capacitors are applied for input-signal sampling, and N capacitors are applied for feedback. The DEM technique is realized by sequentially changing the positions of the capacitors one position each clock cycle. The average value of the amplification factor is

$$\overline{G} = \frac{M}{N} + \Delta G , \tag{4.23}$$

where ΔG represents the second-order error due to the mismatch. This residual error is very small. When, for example, $G = 7$, and the mismatch of one of the capacitors is 1%, the relative error due to mismatching is only 12×10^{-6}. This shows that the application of the DEM technique reduces the maximum error with a factor of about 800.

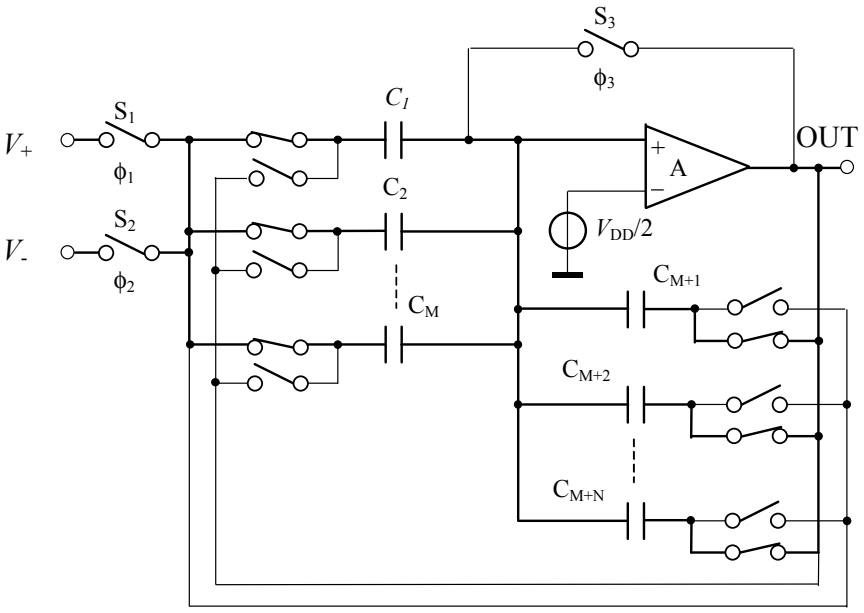

Figure 4.20. SC DEM amplification of the input voltage signal.

4.5.2 DEM Division of Large Voltage Signals

When the input voltage is very large, such as the bridge supply voltage in Figure 4.18, a voltage divider is needed to bring the signal within the dynamic input range of the signal processing circuit. The absolute accuracy of a passive voltage divider depends on the component matching. Therefore, aging effects will cause drift of the divider factor. The DEM technique can also be used for accurate voltage division.

The large voltage V_{ex} can be divided by N_d-resistors in series connection. Each time $\frac{1}{N_d}V_{ex}$ is sampled by the sampling capacitor. An alternative way is to split the sampling capacitor into N_d identical parts. Each time V_{ex} is sampled with $\frac{1}{N_d}C_S$ and other voltages are sampled with C_S. The use of DEM technique guarantees an accurate value of division factor N_d. Circuit in both cases consists of many components. By combining these two methods the divider factor N_d can be realized with many fewer components [4.14], as shown in Figure 4.21.

The circuit in Figure 4.21 consists of a resistive voltage divider combined with a capacitive voltage divider. The divider is realized with N_R resistors and N_C capacitors, resulting in an accurate division factor of $N_d = N_R N_C$. The complete division cycle consists of $N_R N_C$ sub-sampling cycles. In each sub-sampling cycle, one of the N_C sampling capacitors is charged with the voltage across one of the N_R resistors ($\sim\frac{1}{N_R}V_{ex}$); this amount of charge is transferred to the integrator and is further processed. After a complete cycle, the total charge transferred to the integrator is $V_{ex}C_{total}$. Compared to the signal without voltage division, where in each cycle, the amount of charge VC_{total} is transferred to the integrator, an equivalent division ratio of $N_R N_C$ is obtained.

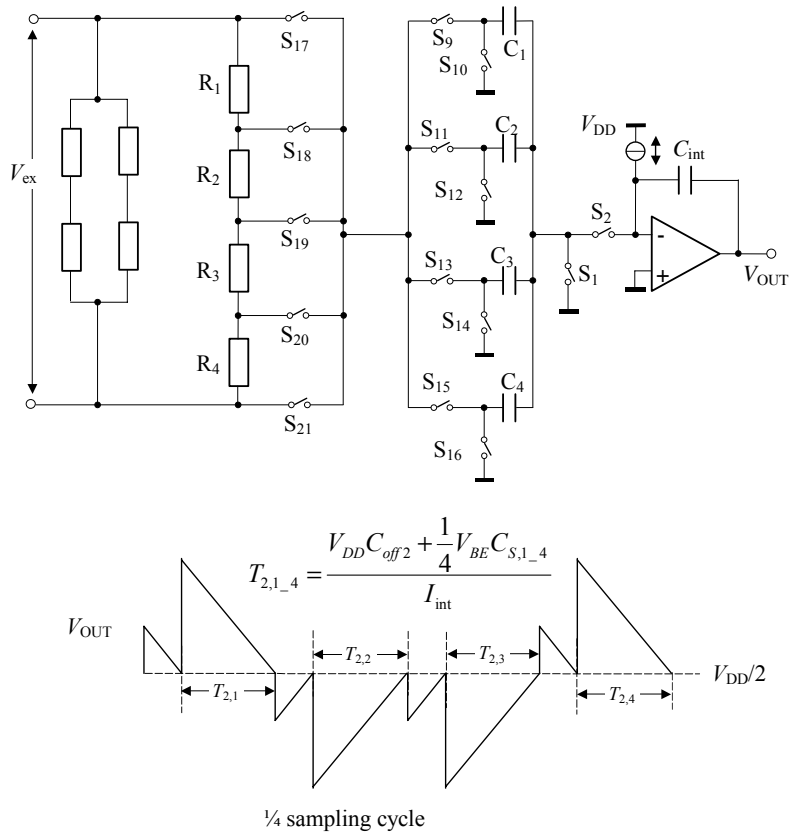

Figure 4.21 A DEM voltage divider with a factor of 16.

To implement the DEM techniques, one needs signal- and data-processing circuits, such as switch controllers, memory, and calculation circuits. These are conveniently combined in the microcontroller. Once a microcontroller is used, besides switch control it is also easy to perform data processing, in the frame of an overall system design. The data processing steps can include, for instance, averaging, non-linearity compensation, auto-calibration, self-testing and filtering.

The voltage divider in Figure 4.21 is suitable for large voltage signals from sources with very low series resistance, for instance the excitation voltage for a bridge transducer. However, when the internal resistance is not that low, there will be problems. Assume, for instance, that a base-emitter voltage is to be divided, as shown in Figure 4.22. To ensure an accuracy of 0.1%, the total resistance of the resistive part must be 1000 times larger than the equivalent differential resistance of the base-emitter diode. Assume that the transistor is biased with a current of 5 µA; then at room temperature, the equivalent differential resistance of the transistor amounts to 5.2 kΩ. Therefore the resistance of the resistive part of the divider must be larger than 5.2 MΩ, which will consume a rather large chip area. Furthermore, due to the large time constant formed by the large resistor and the capacitors, longer measurement time is required for a specific accuracy. This results in a lower measurement speed.

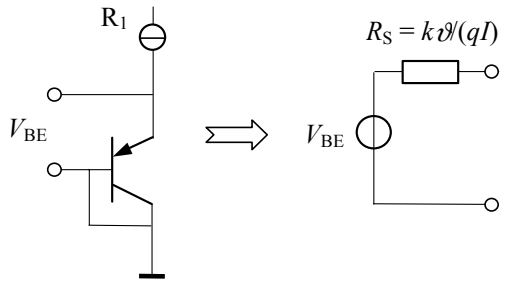

Figure 4.22. The equivalent circuit of the base emitter voltage measurement.

Applying a pure capacitive voltage divider can solve this problem. If such a capacitive divider were to be applied, for instance to realize a voltage division with the same factor of 16 as in Figure 4.21, it would require 16 identical capacitors, which involves the use of a large number of control switches. The large number of switches, the control logic circuit for the switches, and the control wires will increase the chip area.

In order to reduce the need for a large number of switches, an alternative circuit was presented in [4.20], see Figure 4.23. In this circuit, the same number of capacitors is applied as in Figure 4.21 to perform the voltage division with the same division factor. The resistive part is omitted, in order to prevent the error caused by the voltage distribution between the source resistor and the divider resistors. As a result, the charge in each sub-sampling phase, which now amounts to $V_{ex}C_i$, is 4 times larger than that in the R-C divider in Figure 4.21, where it is $¼V_{ex}C_i$. Only a factor of 4 for the voltage division is thus obtained. In order to realize the same division factor of 16, the control logic for the sampling capacitors has been changed. In this case, a complete division cycle still contains the same amount of (N_RN_C) sub-sampling cycles, but now the voltage signal is sampled only once per four (N_R) cycles. Thus the same final amount of charge $V_{ex}C_{total}$ is transferred to the integrator in one complete sampling cycle. Consequently, the same factor of the final voltage division is realized.

It might seem that there is a problem with the purely capacitive divider. During the sampling cycle, the amount of charge transferred to the integrator is N_R times larger than that in the R-C divider. In this case, overload occurs, as shown in Figure 4.23 (b). To avoid overload, smaller sampling capacitors might be applied, but this will reduce the transfer parameter, which results in a lower signal sensitivity. In principle, the overload will not cause a serious problem. Not the output voltage, but the amount of charge transferred to the integrator is of importance. If a MOSFET op-amp is applied, there is no path for charge loss in the charge-balanced integrator. And by careful design the integration current, I_{int}, is not affected by the voltage change at the non-invert input of the integrator op-amp. With these two conditions, the overload will not affect the voltage-to-period conversion in the divider application.

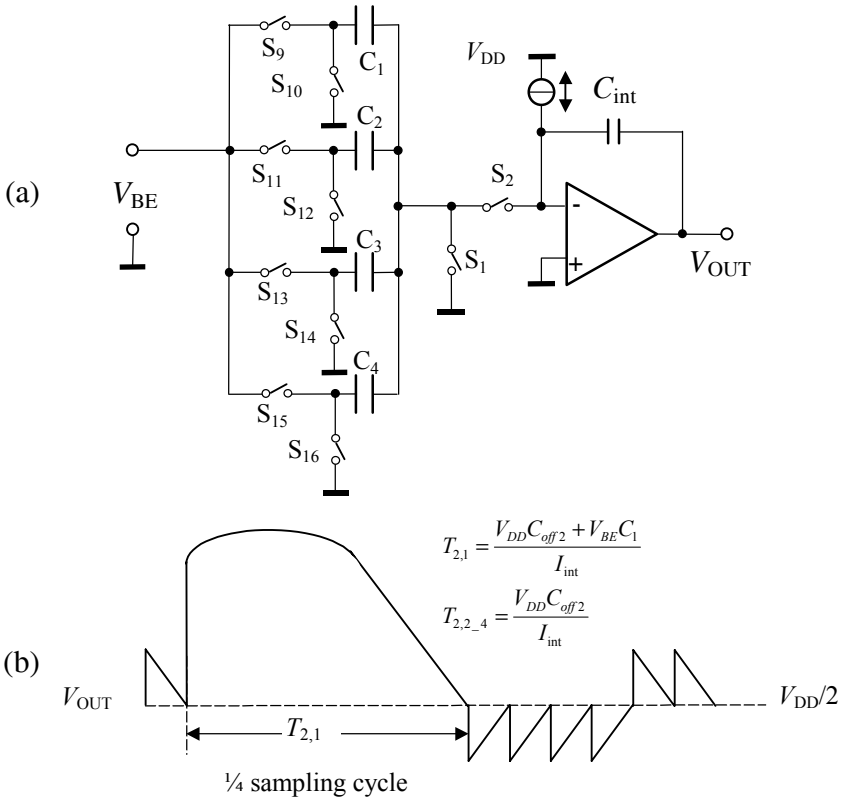

Figure 4.23. The purely capacitive DEM voltage divider, (a) The schematic circuit, (b) The output signal of the integrator.

4.5.3 DEM Biasing for a PTAT Circuit

The accuracy of a PTAT voltage is determined by that of the current-density ratios and that of the amplification factor:

$$V_{PTAT} = A \cdot \Delta V_{BE} = A\frac{kT}{q} \cdot \ln\left(\frac{I_{C2}}{I_{C1}} \cdot \frac{I_{S1}}{I_{S2}}\right). \tag{4.24}$$

By applying a DEM amplifier, one can realize an accurate amplification factor for the small-voltage ΔV_{BE}. In that case, the accuracy of the PTAT voltage is still limited by

- the mismatch of the bipolar transistor pair;
- the mismatch of the MOSFET transistors of the current mirror circuit.

The mismatch of the transistor pair can be minimized by a careful layout design: by applying a quad structure for a transistor pair with identical emitters. The residual mismatch can be reduced by interchanging the position of Q_1 and Q_2, as shown in Figure 4.24, and taking the average of the two results [4.7]. This can easily be realized in the time domain.

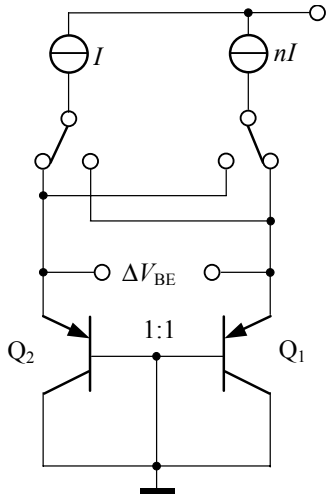

Figure 4.24. The effect of the transistor mismatching can be reduced by dynamically interchanging the position of Q_1 and Q_2.

Similarly, by applying the DEM technique, one can also obtain an accurate current ratio [4.21]. The mismatch error in the current-mirror circuit can be reduced significantly by the application of the DEM technique, as shown in Figure 4.25. The switches control the current flowing to the transistors. For example, in the first step, the current $I(1+\delta_1)$ is switched to the emitter of Q_1 and all the other currents are switched to transistor Q_2; in the second step, current $I(1+\delta_2)$ is switched to the emitter of Q_1 and all the other currents are switched to transistor Q_2, and so on. After a complete cycle, the average $\overline{\Delta V_{\mathrm{BE}}}$ of the PTAT voltage is given by

$$\overline{\Delta V_{BE}} = \frac{1}{n+1}\sum_{i=1}^{i=n+1}\frac{kT}{q}\ln\frac{(n+1)-(1+\delta_i)}{1+\delta_i} \approx \frac{kT}{q}\left(\ln n + \frac{1}{2}\frac{n+1}{n^2}\sum_{i=1}^{n+1}\delta_i^2\right), \tag{4.25}$$

where it is assumed that $\delta_i << 1$. The residual error is of the second order. Example: for a current ratio of 3, with $\delta_1 = -\delta_2 = 1\%$, and $\delta_3 = -\delta_4 = 0$, the relative inaccuracy after applying DEM is only 18×10^{-6}. Without DEM, the relative inaccuracy can be up to $\pm3300\times10^{-6}$.

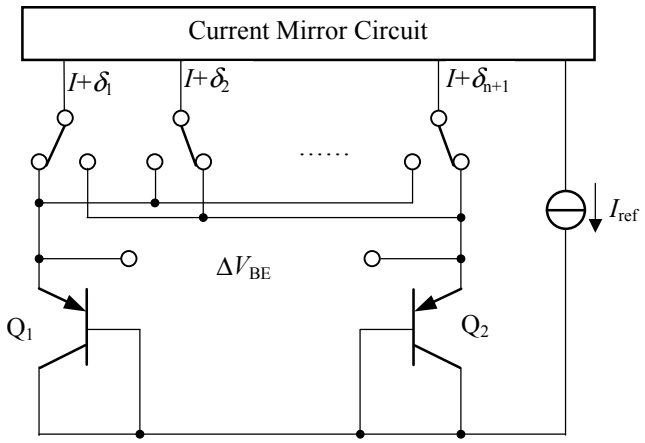

Figure 4.25. DEM current ratio for ΔV_{BE}.

4.6 Remaining Non-Idealities

Since advanced techniques are applied in the circuit design, the effect of the first-order non-idealities has been minimized. The non-linearity and the noise are the remaining limitations for the accuracy of the signal measurement. In [4.14], the linearity and the noise performance of a signal-to-time converter have been carefully analysed. In this section, the analyses for these two non-idealities will be briefly summarized, based on the circuit of the voltage-to-time converter shown in Figure 4.11.

4.6.1 Non-Linearity

A non-linearity might be introduced by several circuit non-idealities:

- The finite DC gain of the amplifier in the integrator,
- The time-constant at the integrator input,
- The low- and high-frequency poles of the integrator,
- The switch-charge injection,
- The voltage dependence of the sampling capacitors,
- The non-linear effects of the comparator, and
- The mismatch of the integration current.

The Finite DC Gain of the Amplifier in the Integrator

The finite DC gain limits the charge that is completely transferred to the integrator capacitor at the transient moment. But while the charge of the integrator is discharging, the integrator voltage is falling back to the initial value. During this time period, the residual charge due to the finite DC gain is totally transferred to the integrator capacitor. Thus the finite DC gain does not affect the charge-to-period conversion.

The Time Constant at the Integrator Input

The time constant formed by the series resistance R_S of the input voltage and the sampling capacitance C_S will affect the linearity. Figure 4.26 shows the voltage at the sampling capacitor, together with the integrator output voltage and the control signal φ_1.

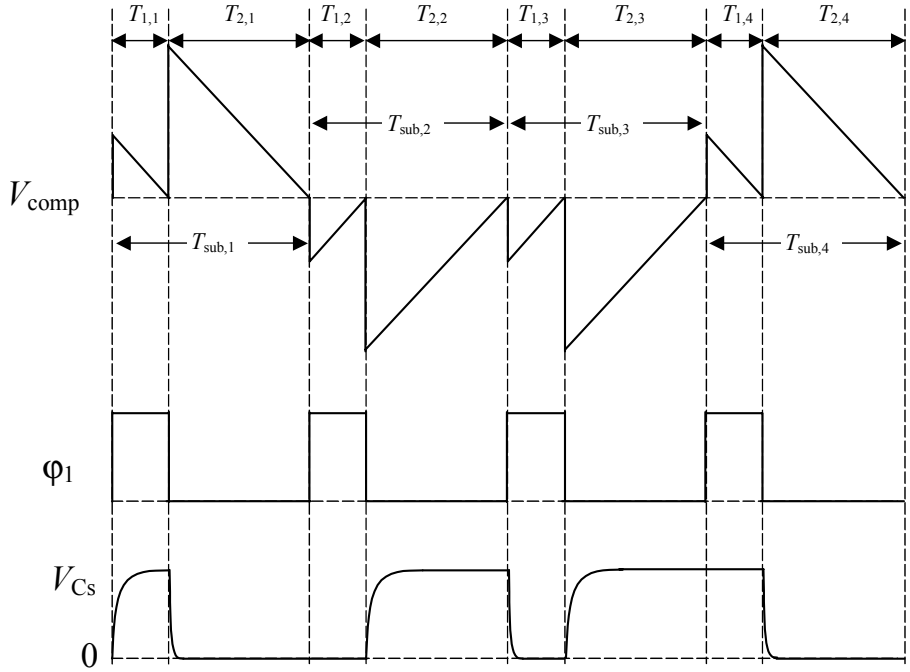

Figure 4.26 The modified charge-balancing oscillator for capacitance or voltage measurement.

The charge at the sampling capacitor at the transient moment is

$$Q = V_{in} C_S \left(1 - e^{-\frac{T_{1,1}}{R_S C_S}} \right). \tag{4.26}$$

So, a finite linear gain error due to the series resistance is determined by

$$\varepsilon_{R_S C_S} = e^{-\frac{T_{1,1}}{R_S C_S}}. \tag{4.27}$$

This error can be eliminated by the three-signal method, but only when the three signals have the same series resistances. For input signals with a different series resistance, this error cannot be completely cancelled using the three-signal method. The residual error is determined by the dominant one. To keep the error under a certain level, the following requirement must be fulfilled

$$T_{1,1} \geq R_S C_S \left| \ln \varepsilon_{R_S C_S} \right|. \tag{4.28}$$

Example: in order to keep the non-linearity smaller than 10×10^{-6}, $T_{1,1}$ must be 11.5 times larger than the time constant.

The Low- and High-Frequency Poles of the Integrator

Figure 4.27 can be used to calculate the low-frequency pole. The time constant of the low-frequency pole is given by

$$\tau_{LF,\mathrm{int}} = R_i\left[C_S + C_{pb} + (1 + A_{\mathrm{int}})C_{\mathrm{int}}\right] \approx A_{\mathrm{int}} R_i C_{\mathrm{int}}, \tag{4.29}$$

where A_{int} represents the DC gain of the integrator amplifier, R_{i} the input resistance of the amplifier, and C_{int} the integrator capacitance.

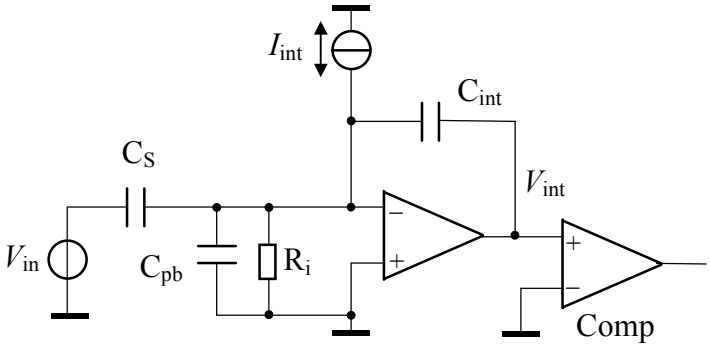

Figure 4.27 The circuit used to calculate the low-frequency pole.

The effect of the low-frequency pole is a charge leakage (via R_{i} in Figure 4.27), and has been described in [4.14]. As a result of this effect, the output in the time domain deviates from the ideal value,

$$T_{2,LF} = T_2\left(1 - \frac{T_2}{\tau_{LF,\mathrm{int}}}\right), \tag{4.30}$$

where T_2 denotes the ideal value of the converted time interval when no LF pole exists, and $T_{2,\mathrm{LF}}$ the converted time interval when the LF effect is taken into account. The non-linearity caused by the low-frequency pole is thus determined by

$$\varepsilon_{LF,\mathrm{int}} = \frac{T_{2,LF,x1}}{T_{2,LF,x2}} \cdot \frac{T_{2,x2}}{T_{2,x1}} - 1 \cong \frac{T_{2,x2} - T_{2,x1}}{\tau_{LF,\mathrm{int}}}, \tag{4.31}$$

where $T_{2,\mathrm{x1}}$ and $T_{2,\mathrm{x2}}$ are the converted time intervals for the case without LF pole where two signals are to be measured, while $T_{2,\mathrm{LF,x1}}$ and $T_{2,\mathrm{LF,x2}}$ are the converted time intervals when the LF effect is taken into account, respectively. In other words, in order to keep the non-linearity due to the low-frequency pole low enough, the following requirement must be fulfilled, namely

$$\left|T_{2,x2} - T_{2,x1}\right|_{\max} \le \tau_{LF,\mathrm{int}} \left|\varepsilon_{LF,\mathrm{int}}\right|. \tag{4.32}$$

Example: with $\tau_{\mathrm{LF,int}} = 2$ s, to keep the non-linearity less than 10×10^{-6}, $\left| T_{2,\mathrm{x2}} - T_{2,\mathrm{x1}} \right|_{\max}$ should be less than 20 μs.

On the other hand, the high-frequency pole of the integrator due to the limited bandwidth of the integrator amplifier introduces an incomplete charge transfer. The corresponding effective time constant is given by

$$\tau_{2,HF} = \tau_{\mathrm{int}} \cdot \frac{C_S + C_{pb} + C_{\mathrm{int}}}{C_S + C_{pb} + C_{\mathrm{int}} + A_{\mathrm{int}} C_{\mathrm{int}}}, \tag{4.33}$$

where τ_{int} is the -3dB time constant of the integrator amplifier, and A_{int} is the DC gain of the integrator. Due to the HF pole, the charge transferred to C_{int} during $T_{2,x}$ for the measurement of V_x, called $Q_x(T_{2,x})$ is given by:

$$Q_x(T_{2,x}) = Q_x\left(1-\exp(-\frac{T_{2,x}}{\tau_{HF}})\right), \tag{4.34}$$

where Q_x is the steady-state value. Since the charge is not completely transferred, the converted time interval $T_{2,x}$ is smaller than its ideal value. The non-linearity for two measurements V_{x1} and V_{x2} can be calculated by

$$\varepsilon_{HF} = \frac{Q_{x2}(T_{2,x2})}{Q_{x1}(T_{2,x1})}\cdot\frac{Q_{x1}}{Q_{x2}} - 1 \cong \exp\left(-\frac{T_{2,x1}}{\tau_{HF}}\right) - \exp\left(-\frac{T_{2,x2}}{\tau_{HF}}\right), \tag{4.35}$$

where it is assumed that $\exp(-T_{2,x}/\tau_{HF}) << 1$. For example, with $T_{2,x}$ = 10 µs, τ_{HF} = 0.5 µs, the non-linearity amounts to 0.2×10^{-6}, which is negligible compared to other non-linear contributions.

The Switch-Charge Injection

Figure 4.28 illustrates the two basic switch states for the signal sampling. In Figure 4.28(a), where switches S_1 and S_3 are closed, the sampling capacitor is charged with a voltage V_{in}; in Figure 4.28(b), where switches S_2 and S_4 are closed, the amount of charge $C_S V_{in}$ is transferred to the integrator capacitor C_{int}. In order to prevent charge loss at the inverting node of the integrator, S_1 and S_2 are operated in a break-before-make mode.

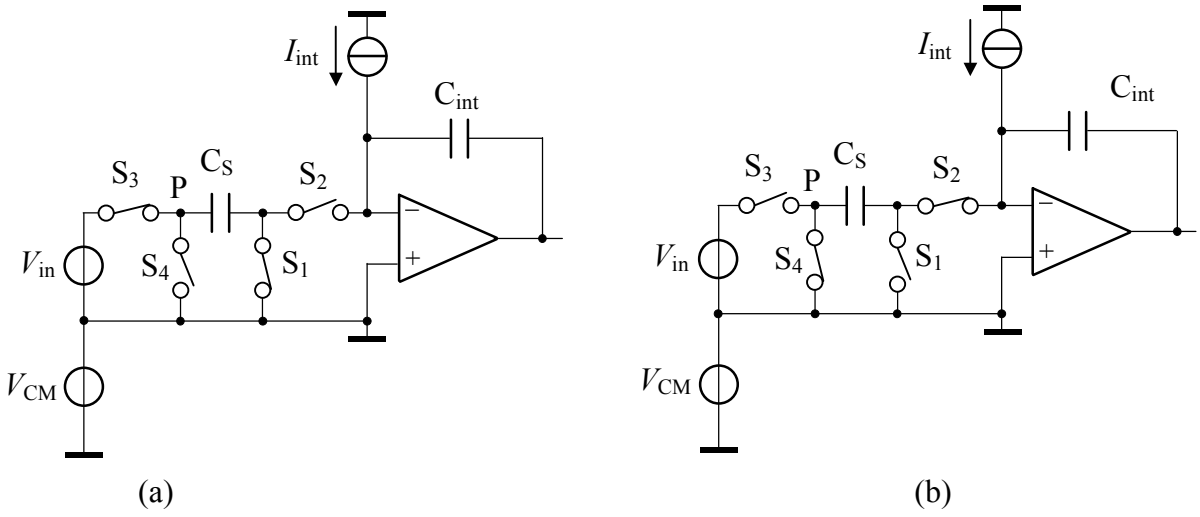

Figure 4.28 Two basic states of the switched-capacitor circuit for signal sampling.

When switch S_1 changes from close to open (state a to state b of Figure 4.28), due to charge injection, it contributes an amount of charge to the sampling capacitor C_S. This amount of charge will be transferred to the integrator capacitor C_{int} together with the sampling charge $C_S V_{in}$. When the switch S_2 changes from close to open (state b to state a of Figure 4.28), due to charge injection, it contributes an amount of charge to the sampling capacitor C_S and the

integrator capacitor C_{int} respectively. Since the voltage conditions are constant when S_1 and S_2 are changed between (a) and (b), these amounts of charge are constant. In another word, the switches S_1 and S_2 contribute a constant switch charge Q_{const} to the integrator capacitor. This charge will not affect the accuracy of measurement, since applying the three-signal technique will eliminate it.

Now we study the effect of charge injection of switch S_3 and S_4. The effect of charge injection is shown in Figure 4.29, where S_3 is assumed to be a single NMOS transistor.

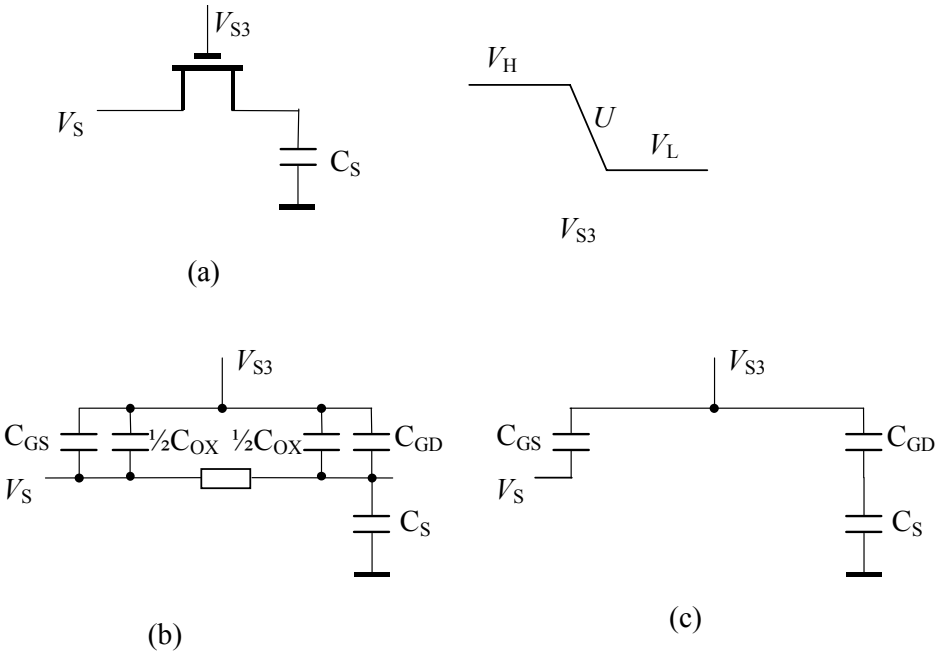

Figure 4.29 (a) The schematic of S_3, (b) the equivalent lumped model while S_3 is conducting, (c) the equivalent lumped model while S_3 is cut off.

Due to the parasitic capacitors, each time the switch signal changes from high to low, an amount of charge is injected to the sampling capacitor C_S. Suppose that the voltage dependence of the parasitic capacitance of the switch transistor is neglected. When the switch S_3 is changed from closed to open, the charge injected to the sampling capacitor is [4.22]

$$q_{S3} = \begin{cases} -(C_{GD} + \frac{C_{OX}}{2})\sqrt{\frac{\pi U C_S}{2\beta}} - C_{GD}(V_S + V_T + V_L) & \text{if } \frac{\beta V_{HT}^2}{2C_S} >> U \\ -(C_{GD} + \frac{C_{OX}}{2})(V_{HT} - \frac{\beta V_{HT}^3}{6UC_S}) + C_{GD}(V_S + V_T + V_L) & \text{if } \frac{\beta V_{HT}^2}{2C_S} << U \end{cases}, \tag{4.36}$$

where

$\beta = \mu C_{OX0} \frac{W}{L}$,

$V_{HT} = V_H - V_S - V_T$,

μ the channel mobility,

C_{OX0} the gate capacitance per unit area,

C_{OX} the gate capacitance of S_3,

W	the channel width of S_3,
L	the channel length of S_3,
C_{GD}	the gate-drain overlap capacitance of S_3,
C_{GS}	the gate-source overlap capacitance of S_3,
V_T	the threshold voltage of S_3, and
U	the falling rate of the voltage V_{S3}.

For example, in practical design, C_S = 80 pF, W = 10 µm, L = 0.7 µm, $C_{OX0} = 2\times10^{-3}$ F/m^2, μC_{OX0} = 2900 µA/V^2, $C_{GD0} = 3.1\times10^{-10}$ F/m, V_T = 0.75 V, V_H = 5 V, V_L = 0 and the delay time from high to low of S_3 is 0.3 ns. We have C_{OX} = 0.014 pF, C_{GD} = 0.003 pF, $\beta = 4\times10^4$ µA/V^2 and $U = 1.67\times10^{10}$ V/s. For V_S = 0 V, 2.5 V and 5 V, $\frac{\beta V_{HT}^2}{2C_S} = 4.5\times10^9$ V/s, 7.6×10^8 V/s and 1.4×10^8 V/s, respectively. The case of $\frac{\beta V_{HT}^2}{2C_S} << U$ is can be applied for all input levels.

Equation (4.36) is also valid for switch S_4.

At period $T_{2,1}$ and $T_{2,4}$, switch S_3 contributes an extra charge q_{S3} to the sampled charge $V_{in}C_S$; at period $T_{2,2}$ and $T_{2,3}$, switch S_4 contributes an extra charge q_{S4} to the sampled charge $-V_{in}C_S$. The total extra charge due to the switch-charge injection for a complete sampling period T_{mod} (see Figure 4.12) amounts to $2(q_{S3} - q_{S4})$. It can be seen that applying chopping can eliminate the constant part of the effect of the switch-charge injection.

Application of the three-signal technique will eliminate the effects of the constant term and the linear term of the channel-charge injection described in equation (4.36). However, the effects of the non-linear parts remain and cause a measurement error. To minimize it, a small switch sizes can be used. However, this will have the drawback of a large on-resistance value. But when three-signal technique is not possible to be applied, for instance the SC amplifier discussed in section 4.5.1, the effect of the switch-charge injection can be significant.

Since in CMOS technology, a pair of complementary MOS transistors is applied for a single switch, the amount of charge injected into the sampling capacitor is, in some cases, partly diminished by compensation. But the amount of compensation depends on the input voltage V_S and the control signals for NMOS and PMOS of the switch. For instance, when V_S is close to ground, the switch-charge injected by NMOS transistor is dominant. In this case PMOS transistor is not conducting; only the parasitic capacitor C_{GD} of PMOS transistor injects an amount of charge to the sampling capacitor C_S, which is in opposite sign of that injected by NMOS transistor. When V_S is close to V_{DD}, the switch-charge injected by PMOS transistor is dominant. In this case NMOS transistor is not conducting; only the parasitic capacitor C_{GD} of NMOS transistor injects an amount of charge to the sampling capacitor C_S, which compensates part of switch-charge injected by NMOS transistor. When V_S is in the range where both NMOS and PMOS transistors are conducting, the total injected switch-charge depends on the control signals for NMOS and PMOS transistors, as shown in Figure 4.30.

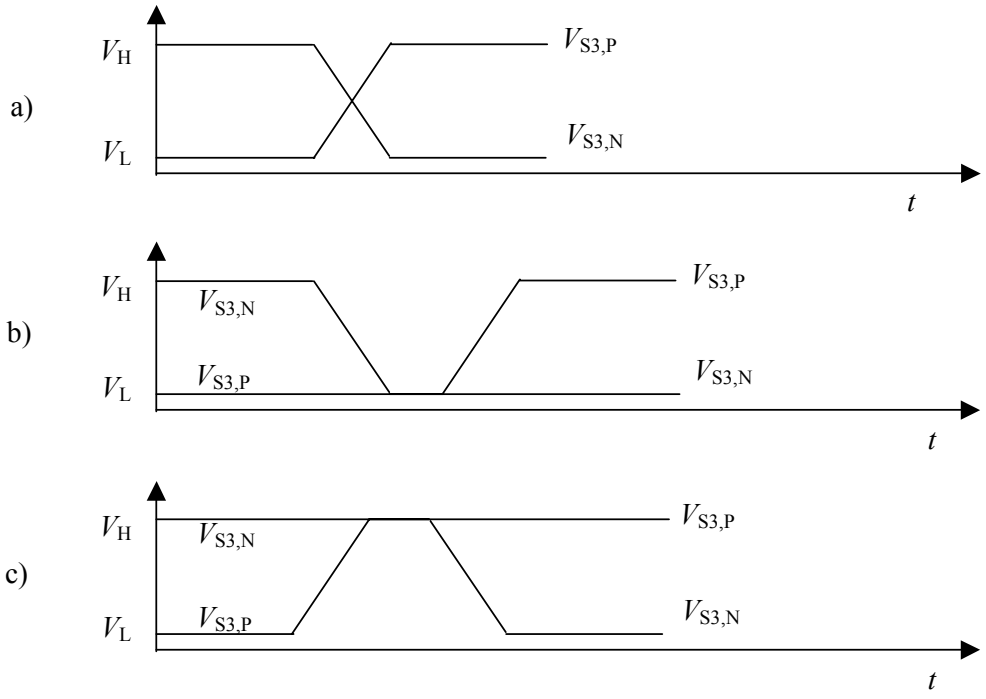

Figure 4.30 The control signals of S_3 for NMOS and PMOS, (a) NMOS and PMOS cut-off simultaneously (b) NMOS cut-off first, (c) PMOS cut-off first.

In case (a), NMOS and PMOS are cut-off simultaneously, the injected switch-charges minimised by the compensation of NMOS and PMOS. In case (b), NMOS transistor is cut-off first, then PMOS transistor is cut-off. The charge injected by NMOS transistor decreases via the path of PMOS transistor, the charge left will partly compensate the charge injected by PMOS transistor. How much is compensated depends on delay between PMOS and NMOS. The case is reversed for case (c).

According to above discussion, for signals with different common-mode voltages, applying three-signal technique can only partly reduce the effect of the switch-charge injection.

The Voltage Dependence of the Sampling Capacitors

The voltage dependency of the sampling capacitor C_S can contribute substantially to the non-linearity in voltage measurement. The voltage dependency of the capacitor C_S can be modelled by

$$C(V) = C_0\left(1 + a_1 V + a_2 V^2 + a_3 V^3\right), \tag{4.37}$$

where V is the voltage across the capacitor, and C_0 is the capacitance at zero voltage. By connecting two equal capacitors in anti-parallel, one can easily remove the odd-order component a_1 and a_3. Only a_2 remains, which results in a non-linearity. For two voltage signals V_{x1} and V_{x2}, with common-mode voltage V_{CM1} and V_{CM2}, respectively, the sampled charge at sampling capacitor C_S is

$$\begin{aligned} Q_{x1} &= (V_- - V_{x1} - V_{CM1})C_{S0}\left[1 + a_2(V_- - V_{x1} - V_{CM1})^2\right] \\ &\quad -(V_- - V_{CM1})C_{S0}\left[1 + a_2(V_- - V_{CM1})^2\right] \\ Q_{x2} &= (V_- - V_{x2} - V_{CM2})C_{S0}\left[1 + a_2(V_- - V_{x2} - V_{CM2})^2\right] \\ &\quad -(V_- - V_{CM2})C_{S0}\left[1 + a_2(V_- - V_{CM2})^2\right] \end{aligned}, \tag{4.38}$$

respectively. The parameter V_- represents the potential of the other electrode of the sampling capacitor, as shown in Figure 4.31.

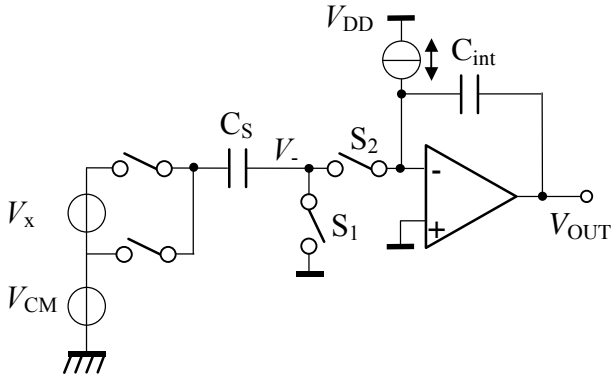

Figure 4.31. A simplified circuit to calculate the charge transferred to the integrator capacitor.

The non-linearity due to the voltage dependence of the sampling capacitor is defined as

$$\varepsilon_{C\_V} = \frac{Q_{x2}}{Q_{x1}}\frac{V_{x1}}{V_{x2}} - 1. \tag{4.39}$$

Example: in our case, n-well/oxide/poly capacitors in 0.7-µm CMOS technology have been applied in the circuit design. The specifications show that the second-order voltage dependence c_2 of this capacitor amounts to $5\times10^{-6}/V^2$. In the case where a thermocouple voltage and an on-chip base-emitter voltage are to be measured, we have, for example, $V_{x1} = 0.05$ V, $V_{x2} = 0.7$ V, $V_{CM1} = V_{CM2} = 0$ V (the thermocouple is grounded), $V_- = 2.5$ V (for a supply voltage of 5 V). Substituting equation (4.38) into (4.39) shows that the non-linearity due to the second-order voltage dependence of the sampling capacitor amounts to 22×10^{-6}.

The value of the non-linearity ε_{C_V} depends on the common-mode voltage of the input. The non-linearity as a function of the common-mode voltage V_{CM1} is shown in Figure 4.32 (the other parameters and voltages are the same as those given in the example). The figure shows that for the sampling capacitor with two equal capacitors in anti-parallel connection, the common-mode voltage should be close to the ground potential or close to the supply voltage in order to minimize the non-linearity.

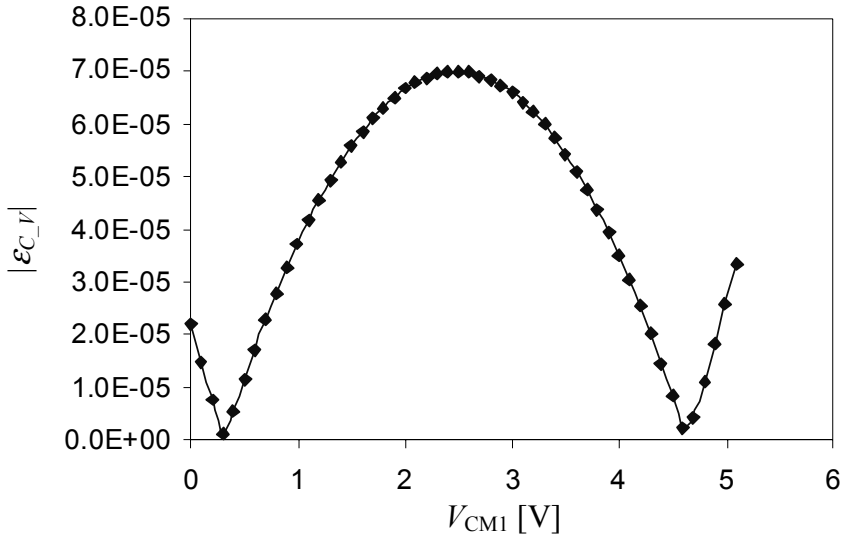

Figure 4.32. The non-linearity caused by the second-order voltage dependence of the sampling capacitor as a function of the common-mode voltage at the input.

The voltage dependence of the integrator capacitor C_{int} will not cause non-linearity, since the converted time period only depends on the charge transferred to this capacitor.

The Non-Linear Effects of the Comparator

The propagation delay of a comparator varies as a function of the amplitude of the input, and the larger the amplitude of the input transient signal, the smaller the propagation delay [4.22]. For a voltage signal V_x, the delay time is

$$t_d = b_0 + b_1 V_x + b_2 V_x^2 . \tag{4.40}$$

The non-linearity due to the non-linear comparator delay is thus

$$\varepsilon_d = \frac{T_{x2} - T_{off}}{T_{x1} - T_{off}} \cdot \frac{T_{x1\_0} - T_{off\_0}}{T_{x2\_0} - T_{off\_0}} - 1 \approx \frac{t_{d2} - t_{doff}}{T_{x2\_0} - T_{off\_0}} - \frac{t_{d1} - t_{doff}}{T_{x1\_0} - T_{off\_0}} , \tag{4.41}$$

where $T_{x1\text{-}0}$ and $T_{x2\text{-}0}$ are the time intervals without comparator delay, t_{d1} and t_{d2} are the delay times under the condition of the input signals V_{x1} and V_{x2}, respectively. The three-signal technique eliminates the effects of the zero- and first-order terms. Second-order and higher-order terms will cause non-linearity.

The Mismatch of the Integration Current.

If the positive and the negative integration current are not identical, the time interval of the modulated period is

$$T_{\mathrm{mod}} = \frac{2\left(C_{\mathrm{off1}}V_{\mathrm{DD}} + C_{\mathrm{off2}}V_{\mathrm{DD}} + V_{\mathrm{in}}C_{\mathrm{S}}\right)}{I_{\mathrm{int},+}} + \frac{2\left(C_{\mathrm{off1}}V_{\mathrm{DD}} + C_{\mathrm{off2}}V_{\mathrm{DD}} + V_{\mathrm{in}}C_{\mathrm{S}}\right)}{I_{\mathrm{int},-}}. \tag{4.42}$$

The factors '2' are due to two times charge and discharge in one complete conversion period, see Figure 4.12. Thus a mismatch between the positive and the negative integration current results in a multiplicative error. This error can be eliminated by the three-signal technique.

4.6.2 Noise and Resolution

All the noise sources, such as thermal noise, shot noise, and 1/*f* noise, contribute to the jitter of the modulator period. This jitter determines the resolution that can be achieved with the modulator.

Noise Sources and Noise Model

Figure 4.33 depicts the circuit of the charge-balancing modulator with noise sources.

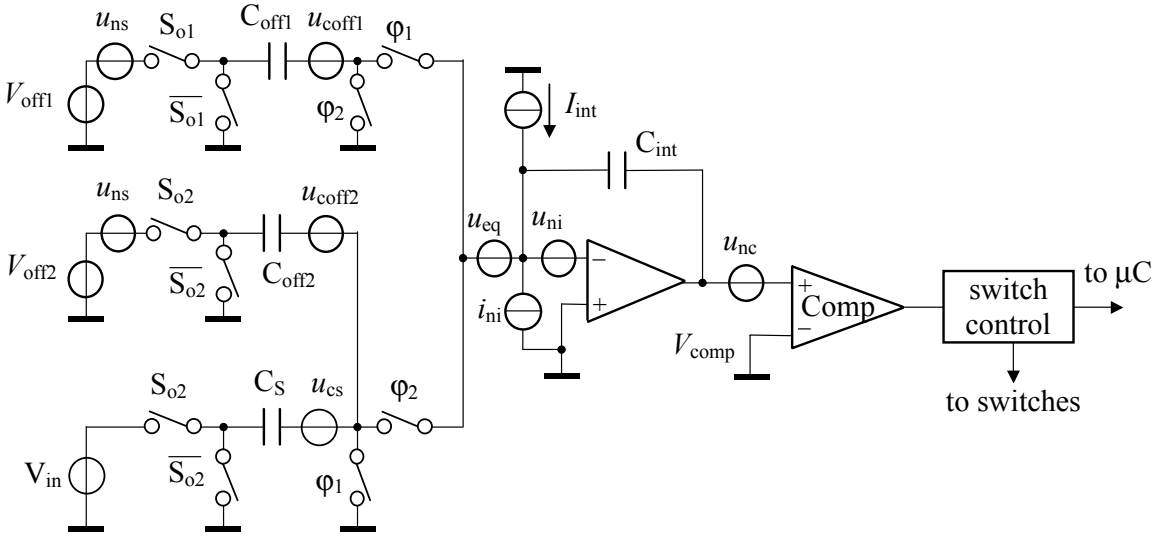

Figure 4.33 The noise of the modified charge-balancing oscillator.

The noise sources considered here include:

- noise voltage u_{ni} of the amplifier in the integrator,
- noise current i_{ni} at the input of the integrator,
- noise voltage u_{ns} of the input source,
- noise voltage u_{nc} of the comparator, and
- thermal noise of the ON resistance of the switches, resulting in kT/C noise.

The noise calculations are based on the Bennet model [4.9]. Bennet showed that white noise can be described as an infinite sum of discrete sinusoidal components. These components have different frequency, equal amplitude and a random phase, which is uniformly distributed in the interval [-π, π]. The sum of the power of the individual components equals the total power of the modelled noise source. By using this model, the effect of the noise on the

resolution can be calculated in a simple way. We determine the influence of one Bennet component on N modulator periods and calculate the variance due to only one component. We then use all Bennet components to find the total variance, where we need the relation between the amplitude of the Bennet components and the Power Spectral Density (PSD). To handle 1/*f* noise, we assumed that the amplitude of the Bennet components depends on the frequency.

The Noise Voltage of the Integrator Amplifier

According to the analysis in [4.14], the variance on the time value NT_{mod} of the modulator due to the noise voltage of the integrator amplifier is given by

$$\sigma_{\mathrm{ni}}^2 = \left(\frac{C_{\mathrm{total}}}{I_{\mathrm{int}}}\right)^2 4NB_{\mathrm{int}}S_{u_{ni}}\left(1+\frac{4f_{\mathrm{c,ni}}}{B_{\mathrm{int}}}\right), \tag{4.43}$$

where $C_{\mathrm{total}} = C_{\mathrm{S}}+C_{01}+C_{02}+C_{\mathrm{pb}}+C_{\mathrm{int}}$ is the total capacitance at the inverting input of the integrator amplifier, I_{int} is the amplitude of the integration current I_{int}, $S_{u_{ni}}$ is the power spectral density of the voltage noise, $f_{\mathrm{c},ni}$ is the corner frequency of the 1/*f* contribution to the voltage noise, and B_{int} is the closed-loop bandwidth of the integrator.

The relative jitter due to the voltage noise of the integrator amplifier is then

$$\varepsilon_{\mathrm{ni}}^2 = \frac{\sigma_{\mathrm{ni}}^2}{(NT_{\mathrm{mod}})^2} = \left(\frac{C_{\mathrm{total}}}{\hat{V}_{\mathrm{O}}(C_{01}+C_{02})+\hat{V}_{\mathrm{x}}C_{\mathrm{S}}}\right)^2 \frac{B_{\mathrm{int}}S_{u_{ni}}}{4N}\left(1+\frac{4f_{\mathrm{c,ni}}}{B_{\mathrm{int}}}\right), \tag{4.44}$$

for example, with $N = 256$, $C_{\mathrm{S}} = 80$ pF, $C_{01} = C_{02} = 1$ pF, $C_{\mathrm{pb}} = 10$ pF, $C_{\mathrm{int}} = 10$ pF ($C_{\mathrm{total}} = 102$ pF), $B_{\mathrm{int}} = 500$ kHz, $S_{u_{ni}} = 6\times10^{-16}$ V^2/Hz (25 nV/√Hz), $f_{\mathrm{c,ni}} = 0$ (the 1/*f* noise is neglected), $\hat{V}_o = 5$ V, $\hat{V}_x = 0.03$ V, the relative jitter amounts to 4.5×10^{-6}.

In the three-signal technique, the ratio *M* is obtained based on three measurement phases: T_{x}, T_{ref} and T_{off}, as in

$$M = \frac{T_{\mathrm{x}}-T_{\mathrm{off}}}{T_{\mathrm{ref}}-T_{\mathrm{off}}} = \frac{V_{\mathrm{x}}}{V_{\mathrm{ref}}} \quad . \tag{4.45}$$

The variance in *M* due to the voltage noise of the integrator amplifier is given by

$$\sigma_{\mathrm{M,ni}}^2 = \sigma_{\mathrm{ni}}^2\left[\left(\frac{\partial M}{\partial T_{\mathrm{x}}}\right)^2+\left(\frac{\partial M}{\partial T_{\mathrm{ref}}}\right)^2+\left(\frac{\partial M}{\partial T_{\mathrm{off}}}\right)^2\right] = \sigma_{\mathrm{ni}}^2\frac{K}{(T_{\mathrm{ref}}-T_{\mathrm{off}})^2}, \tag{4.46}$$

where

$$K = 2\frac{T_{\mathrm{ref}}^2+T_{\mathrm{x}}^2+T_{\mathrm{off}}^2-T_{\mathrm{x}}T_{\mathrm{ref}}-T_{\mathrm{ref}}T_{\mathrm{off}}-T_{\mathrm{x}}T_{\mathrm{off}}}{(T_{\mathrm{ref}}-T_{\mathrm{off}})^2}, \tag{4.47}$$

lies to between 1.5 and 2, depending on T_{x}.

The resolution $\Delta\upsilon_{\mathrm{ni}}$ in V_{x} due to u_{ni} is determined by $\partial M/\partial V_{\mathrm{x}}$ and the standard deviation $\sigma_{\mathrm{M,ni}}$:

$$\Delta \upsilon_{\mathrm{ni}} \cdot \left(\frac{\partial M}{\partial V_{\mathrm{x}}} \right) = \sigma_{\mathrm{M,ni}} \,. \tag{4. 48}$$

With the help of (4.43), (4.45), (4.46) and (4.47), the voltage resolution $\Delta\upsilon_{\mathrm{ni}}$ is calculated by

$$\Delta \upsilon_{ni}^2 = K\sigma_{ni}^2 \left(\frac{\hat{I}_{\mathrm{int}}}{4NC_S} \right)^2 = \left(\frac{C_{total}}{C_S} \right)^2 \frac{KB_{\mathrm{int}} S_{u_{ni}}}{4N} \left(1 + \frac{f_{c,ni}}{B_{\mathrm{int}}} \right), \tag{4. 49}$$

with the same values as before and $K = 2$, the resolution $\Delta\upsilon_{\mathrm{ni}}$ amounts to 1 µV.

Other Noise Sources and Their Contributions to the Voltage Resolution

The contribution of the other noise sources can be determined in the same way. Table 4.1 lists all noise sources and their contributions to the voltage resolution.

Noise source	Dithering in time domain	Voltage resolution
Noise voltage of the integrator amplifier u_{ni}	$\sigma_{ni}^2 = \left(\frac{C_{total}}{I_{\mathrm{int}}} \right)^2 4NB_{\mathrm{int}} S_{u_{ni}} \left(1 + \frac{4f_{c,ni}}{B_{\mathrm{int}}} \right)$	$\Delta \upsilon_{ni}^2 = \left(\frac{C_{total}}{C_S} \right)^2 \frac{KB_{\mathrm{int}} S_{u_{ni}}}{4N} \left(1 + \frac{f_{c,ni}}{B_{\mathrm{int}}} \right)$
Noise current at the input of the integrator i_n	$\sigma_{i_n}^2 = \frac{NT_{msm} S_{i_n}}{2\hat{I}_{\mathrm{int}}^2}$	$\Delta \upsilon_{i_n}^2 = \frac{KT_{msm} S_{i_n}}{32NC_S^2}$
Noise voltage of the input source u_{ns}	$\sigma_{ni}^2 = \left(\frac{C_S}{I_{\mathrm{int}}} \right)^2 4NB_{\mathrm{int}} S_{u_{ns}} \left(1 + \frac{4f_{c,ni}}{B_{\mathrm{int}}} \right)$	$\Delta \upsilon_{u_{ns}}^2 = \frac{KB_{\mathrm{int}} S_{u_{ns}}}{4N} \left(1 + \frac{f_{c,ni}}{B_{\mathrm{int}}} \right)$
Noise voltage of the comparator, u_{nc}	$\sigma_{nc}^2 = \left(\frac{C_{\mathrm{int}}}{I_{\mathrm{int}}} \right)^2 4NB_{comp} S_{u_{nc}}$	$\Delta \upsilon_{u_{nc}}^2 = \left(\frac{C_{\mathrm{int}}}{C_S} \right)^2 \frac{KB_{\mathrm{int}} S_{u_{nc}}}{4N}$
$k\vartheta/C$	$\sigma_{SC}^2 = \frac{8Nk\vartheta C_{total}}{I_{\mathrm{int}}^2}$	$\Delta \upsilon_{SC}^2 = \left(\frac{C_{total}}{C_S} \right) \frac{k\vartheta K}{2NC_S}$
Quantization noise	$\sigma_{clk}^2 = \frac{t_{clk}^2}{6}$	$\Delta \upsilon_q^2 = \frac{K}{6} \left(\frac{t_S \hat{I}_{\mathrm{int}}}{4NC_S} \right)^2$

Table 4.1 The summary of the noise sources and their contributions to the signal processing circuit.

Here, S_{i_n}, $S_{u_{ns}}$ and $S_{u_{nc}}$ represent the PSD of i_{n}, u_{ns} and u_{nc}, respectively; B_{comp} represents the bandwidth of the comparator, and t_{s} the sampling period of the microcontroller. Table 4.1 shows that by increasing the duration of the sampling period N, one can reduce the voltage noise, and thus improve the voltage resolution. However, this reduces the measurement speed: there is a trade-off between the voltage resolution and the measurement speed. To reduce the quantization noise, use a microcontroller with a higher clock frequency.

It is important to determine the dominant noise source and to reduce the noise. By applying a MOSFET operation amplifier, the contribution of the current source i_{n} can be kept smaller than that of u_{ni}. The contribution of the $k\vartheta/C$ can easily be kept small if one chooses a sufficiently large value of C_{S}. When the noise voltages u_{ni} and u_{nc} have an equal spectral density, the contribution of u_{nc} can be neglected, since $C_{\mathrm{int}} >> C_{\mathrm{S}}$. Thus we can conclude that the most important noise source is the voltage noise u_{ni} of the integrator op-amp.

4.7 Conclusions

Based on considerations with respect to the accuracy, the resolution and the conversion speed, the indirect A/D converters (modulators) are found to be very suited for use in low-cost smart sensor systems. These modulators will be applied in combination with a microcontroller, which will digitize the output signals of the modulators. Three types of modulators were described in this chapter: the frequency modulator, the period modulator, and the duty-cycle modulator. The period modulator was shown to be the most suitable one for our sensor-measurement system.

It was shown that the charge-balance period modulator is preferred for sensor interfaces dealing with voltage signals.

A chopping technique can be applied to reduce the low-frequency interference and the $1/f$ noise. Applying the nested-chopper technique can further reduce the residual offset due to the clock feed-through.

The Dynamic-Element-Matching (DEM) technique plays an important role in the circuit as they can eliminate the systematic errors caused by mismatching. This technique can easily be applied in a charge-balance period modulator. With the application of DEM, small voltage signals can be amplified and large voltage signals can be attenuated accurately. An accurate voltage signal ΔV_{BE}, which is required in the design of temperature sensors and bandgap references, can also be generated using the DEM technique.

When the three-signal method is applied, non-linearity will limit the systematic measurement accuracy of the circuit. The non-linearity is mainly caused by the low- and high-frequency poles of the integrator, the voltage dependence of the sampling capacitors, and by the non-linear delay time of the comparator. By careful design of the circuit, the effects due to the low- and high-frequency poles of the integrator can be minimized. The effect of the switch-charge injection depends not only on the cut-off speed, but also on the common-mode level of the input signal. For signals with different common-mode levels, applying three-signal technique can only partly eliminate this effect. When two identical sampling capacitors are connected in anti-parallel, only the effect of a second-order voltage dependence of the sampling capacitor will remain. Common-mode levels of the voltage signals affect the measurement accuracy due to the voltage dependence of the sampling capacitors. In order to minimize this effect, use voltage signals that have the same common-mode levels.

Noise determines the measurement resolution. The voltage resolution can be improved by increasing the number of sampling periods. However, this reduces the measurement speed, as there is a trade-off between the voltage resolution and the measurement speed. To reduce the quantization noise, we used a microcontroller with a higher clock frequency.

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Chapter 5 Considerations for the Architecture of a Thermocouple Measurement System

5.1 Introduction

Here, a thermocouple interface will be designed using the characterization of bipolar transistors in CMOS presented in Chapter 3 and the research in circuit design presented in Chapter 4. Before we start, we discuss the design considerations for the thermocouple measurement system. Some of the considerations will determine the requirements for the interface circuit.

In designing the thermocouple measurement system, the thermal design is important. Any parasitic thermal-electrical effects, which can cause measurement errors, must be minimized by careful thermal design.

Measurement requirements will be discussed. These requirements will determine the performance of the interface circuit. Considerations in circuit design of the interface will also be discussed. These include the considerations for input circuits, output circuits and the circuits to generate the basic signals V_{BE} and ΔV_{BE}.

5.2 Thermal Design Considerations

Figure 5.1 shows the block diagram of a set-up for temperature measurement where a thermocouple is used as a temperature sensor. The thermocouple is applied to measure the temperature (ϑ_M) of an object. The terminals of the wires (which consist of metal A and B) are connected to the input of an interface circuit, via metal C wires. The wires inside the interface IC are made of metal D.

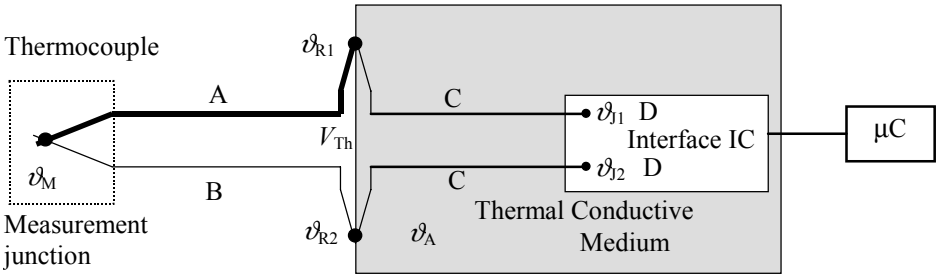

Figure 5.1 The measurement system for thermocouples.

The interface circuit measures the voltage V_{m}, which equals

$$V_{\mathrm{m}} = e_{\mathrm{DC}}(\vartheta_{\mathrm{J1}}) + e_{\mathrm{CA}}(\vartheta_{\mathrm{R1}}) + e_{\mathrm{AB}}(\vartheta_{\mathrm{M}}) + e_{\mathrm{BC}}(\vartheta_{\mathrm{R2}}) + e_{\mathrm{CD}}(\vartheta_{\mathrm{J2}}), \tag{5.1}$$

where $e_{\mathrm{AB}}(\vartheta_{\mathrm{M}})$ represents the *thermal electromotive force* (*emf*) of the AB junction at the temperature ϑ_{M}. The other parameters, $e_{\mathrm{CA}}(\vartheta_{\mathrm{R1}})$, $e_{\mathrm{DC}}(\vartheta_{\mathrm{J1}})$, $e_{\mathrm{CD}}(\vartheta_{\mathrm{J2}})$, $e_{\mathrm{BC}}(\vartheta_{\mathrm{R2}})$ represent the *emf* of junctions CA, DC, CD, and BC at temperatures ϑ_{R1}, ϑ_{J1}, ϑ_{J2}, and ϑ_{R2}, respectively. The voltage V_{m} depends not only on the type of thermocouple and the temperatures ϑ_{M}, ϑ_{R1} and ϑ_{R2}, but also on the types of metal C and D, and on the temperatures ϑ_{J1} and ϑ_{J2}. When certain thermal precautions are taken, the measurement of ϑ_{M} can be simplified. Under the conditions

$$\begin{aligned} \vartheta_{\mathrm{R1}} &= \vartheta_{\mathrm{R2}} = \vartheta_{\mathrm{R}} \\ \vartheta_{\mathrm{J1}} &= \vartheta_{\mathrm{J2}} = \vartheta_{\mathrm{J}} \end{aligned}, \tag{5.2}$$

the law of the third metal [5.1] gives

$$\begin{aligned} e_{\mathrm{BC}}(\vartheta_{R2}) + e_{\mathrm{CA}}(\vartheta_{\mathrm{R1}}) &= e_{\mathrm{BC}}(\vartheta_{\mathrm{R}}) + e_{\mathrm{CA}}(\vartheta_{\mathrm{R}}) = e_{\mathrm{BA}}(\vartheta_{\mathrm{R}}) = -e_{\mathrm{AB}}(\vartheta_{\mathrm{R}}) \\ e_{\mathrm{DC}}(\vartheta_{\mathrm{J1}}) + e_{\mathrm{CD}}(\vartheta_{\mathrm{J2}}) &= e_{\mathrm{DC}}(\vartheta_{\mathrm{J}}) + e_{\mathrm{CD}}(\vartheta_{\mathrm{J}}) = 0 \end{aligned}. \tag{5.3}$$

In this case, equation (5.1) becomes

$$V_{\mathrm{m}} = e_{\mathrm{AB}}(\vartheta_{\mathrm{M}}) - e_{\mathrm{AB}}(\vartheta_{\mathrm{R}}) = V_{\mathrm{Th}}. \tag{5.4}$$

Here, the voltage V_{m} depends only on the type of thermocouple applied to measure temperature, and on the temperatures at the measurement junction and the reference junctions.

To derive the temperature ϑ_{M}, one needs to know the reference-junction temperature ϑ_{R} as well. There are mainly two ways to determine the reference-junction temperature: Firstly, to control the reference-junction temperature at certain value, such as the triple point of water, Secondly, to add another temperature sensor to measure the reference-junction temperature.

Most industrial thermocouple measurement systems measure, instead of control, the reference-junction temperature.

In order to realize a low-cost thermocouple measurement system, we integrated a temperature sensor into the interface IC. Since the interface circuit can only measure its own temperature, ϑ_{J}, any difference between ϑ_{R} and ϑ_{J} contributes to the error of the temperature measurement. Therefore, the thermal conductive medium must be well designed in order to minimize (ϑ_{R} - ϑ_{J}). Thus, for the temperature-measurement system of Figure 5.1, the following thermal requirements have to be met to minimize the measurement error:

1. The temperatures of the reference-junctions should be equal: $\vartheta_{\mathrm{R1}} = \vartheta_{\mathrm{R2}} = \vartheta_{\mathrm{R}}$;
2. The temperatures of the two inputs to the interface circuit should be equal: $\vartheta_{\mathrm{J1}} = \vartheta_{\mathrm{J2}} = \vartheta_{\mathrm{J}}$;
3. The two temperatures ϑ_{R} and ϑ_{J} should be equal: $\vartheta_{\mathrm{J}} = \vartheta_{\mathrm{R}}$.

The first requirement can be achieved by designing the thermal-conductive medium carefully. The second requirement can be realized by

1. Designing the two inputs of the interface physically close to each other, thus reducing the effect of the thermal gradients;
2. Locating the two inputs as far as possible from any power-consuming part;

3. Designing the circuit in such a way that they are symmetric with respect to the power-consuming part.

In fact, there are more junctions between the conducting wires D and the input transistors, such as Al-Si junction. Due to the large Seebeck coefficient [5.2] (200 μV/K to 1000 μV/K, depending on the type of doping and the doping concentration), even small temperature differences can contribute error to the measurement. For instance, suppose that the two input transistors are located at distances of 200 μm and 300 μm respectively from a power-consuming part with a dissipation of 5 mW. Equation (3.40) shows that in this case, the temperature difference between the two transistors is 0.01 K. With a Seebeck coefficient of 1000 μV/K, this can result in an input error of 10 μV, which corresponds to an error of 0.25 K for a T-type thermocouple. Therefore, not only the input of the interface IC, but also the two input transistors should be located far from and symmetric with respect to any power-consuming part. Fortunately, due to the excellent thermal conductivity of silicon, this type of error can be reduced to an insignificant level by using a proper chip layout.

The third requirement can be met by designing the interface circuit for low power consumption and assembling the interface IC in good thermal contact with a heat sink, thus reducing the effect of self-heating.

5.3 Considerations for the Electrical System Design

The interface chip has two functions:

- To measure the on-chip temperature, ϑ_J, and
- To measure the thermocouple voltage, V_{Th}.

In order to measure the thermocouple voltage with a high accuracy, three-signal auto-calibration technique can be applied [5.3]. Thus, some additive and multiplicative uncertainties can be eliminated. To perform auto-calibration, two extra voltages, one voltage and one offset voltage should be measured in exactly the same linear way as the thermocouple voltage.

For the reference voltage, we can apply an external reference voltage or an on-chip reference voltage. An on-chip reference voltage is preferred, because it makes the measurement system simpler and reduces the cost. In our experiments we applied a bandgap-reference voltage.

Bipolar transistors were used to generate the temperature-sensor voltage and the bandgap-reference voltage. The bandgap-reference voltage was generated as the sum of a base emitter V_{BE} voltage and an amplified PTAT voltage ΔV_{BE}. The negative temperature coefficient of the base-emitter voltage was compensated by the positive temperature coefficient of the PTAT voltage. As discussed in section 4.1.1, a major disadvantage of a conventional bandgap-reference voltage, which is implemented in CMOS technology, is related to the operational amplifier used to generate the PTAT voltage. The offset voltage of the operational amplifier will cause an error in the bandgap-reference voltage. To reduce the offset voltage, one needs not only use large geometries and a quad transistor configuration for the input stage, but one should also optimize the current densities [5.3]. But even then, the achieved accuracy is far less than that for bipolar implementations. So we have to find another solution.

The solution can be found by applying auto-calibration (section 4.2) [5.4]. In the system with auto-calibration, the interface circuit processes signals successively, and the data are read and stored in the memory of a microcontroller. The unknown signal is derived from the ratio between the unknown signal and the reference signal. In this case we do not have to apply a reference signal with a continuous analog voltage output [5.5] - [5.6]. The voltages V_{BE} and ΔV_{BE} can be sequentially processed by the interface circuit, and a virtual bandgap-reference voltage can be derived by data processing of the microcontroller. Although there is also an offset in the interface circuit, the effect of the offset can be eliminated by data processing. The temperature-sensing signal can be derived in such a way as well. To implement this idea, one needs a circuit that converts the voltages to microcontroller-readable signals. For this purpose we used a voltage-to-period converter.

The block diagram of the measurement system described above is shown in Figure 5.2(a). The voltage-to-period (V-P) converter successively converts four voltage signals, V_{Th}, V_{BE}, ΔV_{BE} and V_{off} into time intervals. The switch-control circuit selects the measured voltage signal. The output signal of the voltage-to-period converter is shown in Figure 5.2(b). In this figure, T_{off}, T_{BE}, $T_{\Delta VBE}$ and T_{Th} represent the time intervals of the output signals, which correspond to the measurements of V_{off}, V_{BE}, ΔV_{BE} and V_{Th}, respectively.

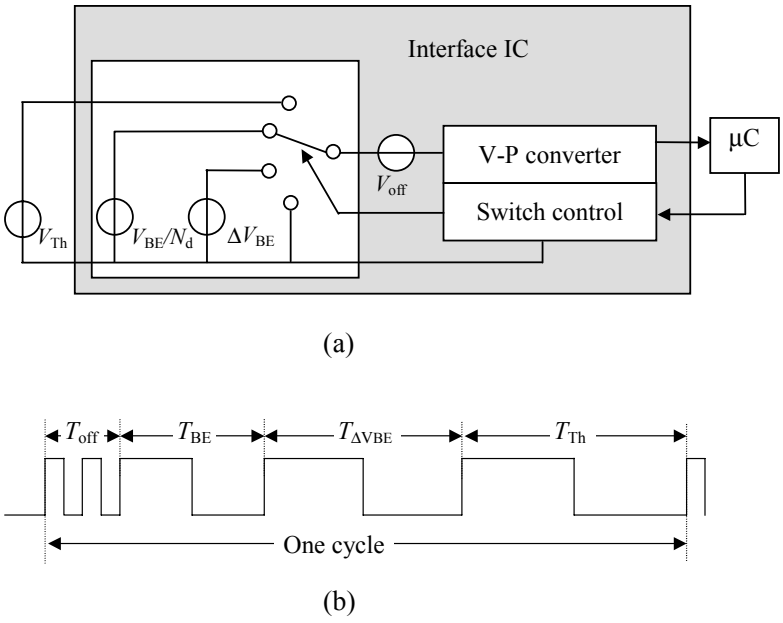

Figure 5.2 a) The basic system diagram for the dynamic thermocouple voltage measurement; b) the interface output signal.

The values of V_{off}, V_{Th} and ΔV_{BE} are 50 mV or less, while the voltage V_{BE} is about 0.7 V. It is difficult to design a precision voltage-to-period converter with high linearity for such a wide dynamic input range. In order to keep all the voltage signals to be measured in a similar range of magnitude, the voltage V_{BE} should be divided by a factor N_d before it is sampled by the V-P converter, or the small voltage signals V_{off}, V_{Th} and ΔV_{BE} should be pre-amplified by a factor G. Since the divider and the pre-amplifier are not included in the three-signal auto-calibration configuration, the accuracy should be very high. For this reason, the DEM technique presented in Chapter 4 could be used for these circuits.

In our design, we used a voltage divider for the following reasons:

- The use of an accurate amplifier, using the DEM technique, will cause a lot of power dissipation, which will increase self-heating,
- A DEM voltage divider requires less circuitry than a DEM amplifier;
- The chip area for a DEM divider is less than that for a DEM amplifier.

The disadvantage of applying a voltage divider is that it reduces the signal-to-noise ratio. But this is acceptable when the signal-to-noise ratio can meet the measurement requirement.

The block diagram of the interface circuit for thermocouples is shown in Figure 5.3. The interface circuit is mainly composed of a voltage-to-period (V-P) converter, the V_{BE} and ΔV_{BE} generating circuit, the voltage-division circuit, the frequency divider, and the switch-control circuit. The switch-control circuit controls the V-P converter to successively measure these four basic voltage signals. The frequency divider divides the output signals of the V-P converter into a proper period time length, which can be read by the microcontroller with acceptable low quantization noise.

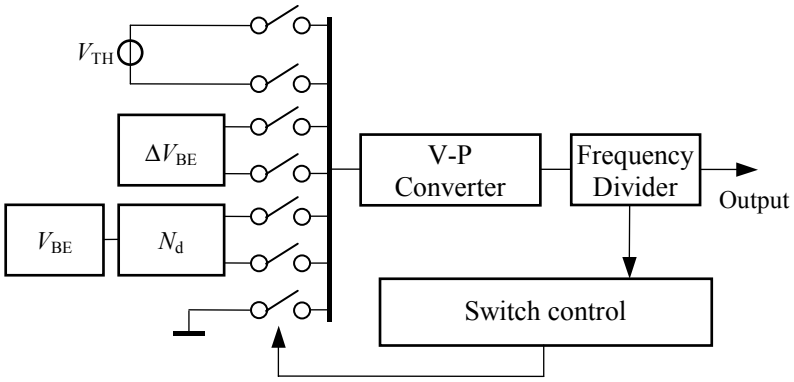

Figure 5.3 The block diagram of the thermocouple interface circuit.

The main reasons to divide the output of the V-P converter to a lower frequency are:

- It allows the longer time constant required for external wiring, as shown in Figure 5.4.
- There is less energy loss. Each up-going transient of the output signal consumes $\frac{1}{2}C_{par.}U^2$ of energy, where C_{par} represents the total parasitic capacitance and U is the voltage swing of the interface output.

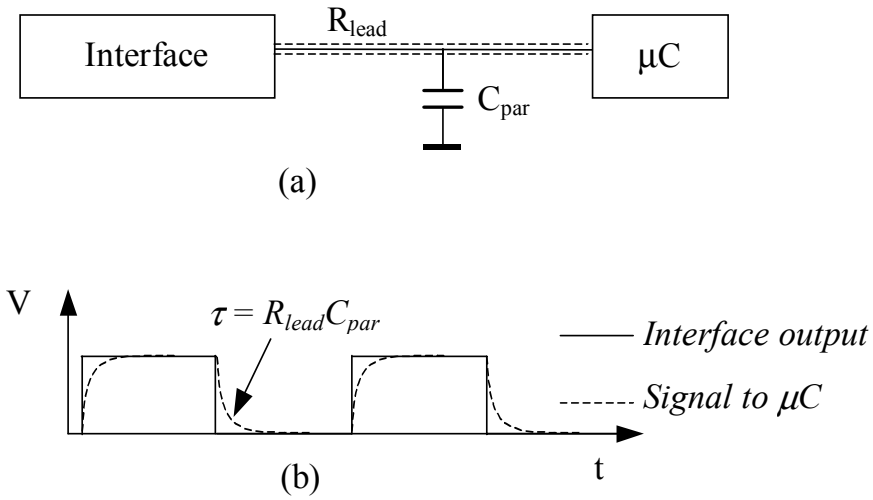

Figure 5.4 The time constant of the external wiring changes the waveform of the interface output signal.

5.4 Measurement Requirements

The precision of the interface system depends on:

1. The accuracy of the bandgap-reference voltage,
2. The accuracy of the measurement of reference-junction temperature, and
3. The linearity and the noise of the V-P converter.

In general we want a total error of the sensor interface that to be less than that of the thermocouple itself. For a typical T-type thermocouple, the relative tolerance is 0.4% over the temperature range of -40 °C to 350 °C [5.1]. This tolerance corresponds to an absolute error of 1.4 K. We can split the tolerance into two error budgets for the interface circuit: 0.2% for the measurement of the thermocouple voltage, and 0.2% for the measurement of the reference-junction temperature.

5.4.1 Accuracy of Bandgap-Reference Voltage

The main error in the voltage measurement is due to the inaccuracy of the bandgap-reference voltage, since the thermocouple-voltage is derived from the ratio V_{Th}/V_{ref}. The characterization results presented in Chapter 3 show that by carefully selecting the bias currents and using multi-emitter bipolar transistors, one can obtain the voltage ΔV_{BE} with an inaccuracy of less than 0.1%. The base-emitter voltage can be trimmed with an inaccuracy of less than 0.1%. As a consequence, it is easy to achieve a total inaccuracy of less than 0.1% in the bandgap-reference voltage at the ambient temperature.

5.4.2 Accuracy of the Measurement of the Reference-Junction Temperature

The inaccuracy of 0.1 % in the voltages ΔV_{BE} and V_{BE} results in an inaccuracy of 0.1% in the on-chip temperature measurement. This inaccuracy corresponds to a temperature error of 0.3 K at room temperature (300 K). By selecting a package with a low thermal-resistance and design a chip with a power consumption of less than 2 mW, the self-heating can be kept below 0.3 K. This yields a total error in the reference-junction temperature measurement of 0.6 K (0.2%). The error due to the voltage measurement should be less than 0.2%, which corresponds to half the error budget.

5.4.3 Linearity and the Noise of the V-P Converter

The error due to the non-linearity of the V-P converter, which was discussed in Chapter 4, can be rather low, even when a low-cost and low-power V-P converter is applied; a non-linearity of less than 100×10^{-6} can easily be realized. With an error budget of 0.2%, such a non-linearity is negligible.

The resolution in the temperature of the thermocouple-measurement system is mainly limited by the noise performance of the interface circuit. For instance, a T-type thermocouple has a sensitivity of 35 μV/K to 62 μV/K over a temperature range of -40 °C to 200 °C. When this type of thermocouple is applied in the measurement system, and a temperature resolution of better than 0.3 K is required, the standard deviation of the equivalent input noise-voltage should be less than 10 μV.

A summary of the requirements for the interface circuit is listed in Table 5.1.

Inaccuracy of the on-chip temperature sensor	< 0.4 K
Inaccuracy of the bandgap-reference voltage	< 0.1%
Non-linearity of the V-P converter	< 0.01%
Equivalent input noise voltage	< 10 μV
Power consumption of the interface	< 2 mW
Thermal resistance of the package	< 150 K/W

Table 5. 1 The requirements for the thermocouple interface.

5.5 The Input Configuration

The typical structures of the assembled thermocouples are shown in Figure 5.5 (a) and (b) [5.1]. They consist of two conductors, insulation material (mostly ceramic), and a metal well. The insulation provides electrical separation for the conductors. The metal well has several functions in the thermocouple system:

- It compacts the insulation.
- It shields the insulation and the conductors from the environment.
- It adds/provides mechanical strength to the assembly.

The metal well can be isolated from the thermocouple junction (Figure 5.5(a)) or be connected to it (Figure 5.5(b)). Since the metal well is generally connected to the whole measurement system, which is normally connected to the safety ground, as a result, the two structures of Figure 5.5 have different common-mode voltages. The structure in Figure 5.5(a) corresponds to an output voltage source with a floating common-mode voltage V_{CM}, while the structure in Figure 5.5(b) corresponds to an output voltage source with a grounded common-mode voltage. The equivalent circuits are shown in Figure 5.5(c) and Figure 5.5(d), respectively.

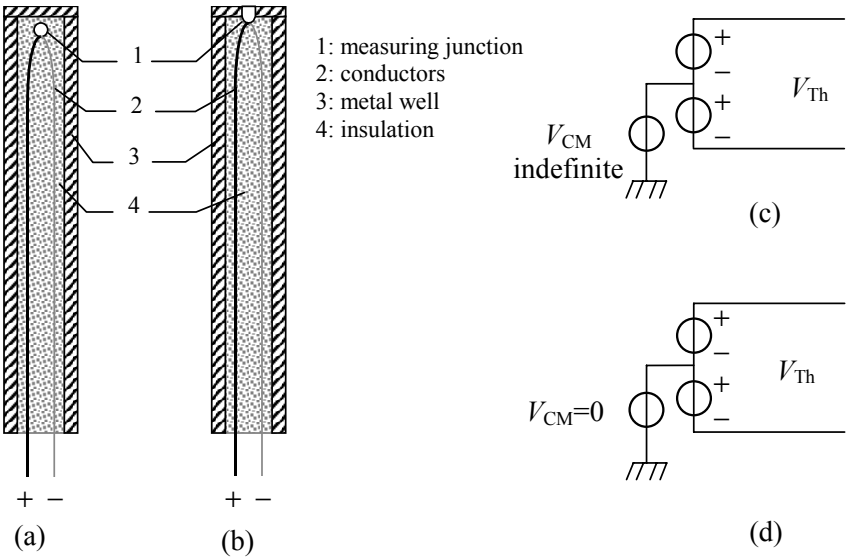

Figure 5.5 The (*a, b*) *typical structures of two thermocouple sensors and* (*c, d*) *their equivalent circuits.*

For the input stage of the low-cost thermocouple interface with a single supply voltage, we posed the following requirements:

- A high common-mode voltage rejection should be realized;
- The input voltage range should cover both the conditions shown in Figure 5.5(c) and Figure 5.5(d);
- A high input-impedance should be realized to reduce the effect of lead resistances.

These requirements can be met by applying a switched-capacitor circuit (see section 4.3.1) at the input of the interface (Figure 5.6) for amplifying the thermocouple voltage. The main advantage of the switched-capacitor amplifier is that the DC common-mode voltage is isolated by the sampling capacitor. Only the differential thermocouple voltage is sampled and amplified. Even with a single supply voltage, the switched-capacitor amplifier can process the small voltages with a grounded common-mode voltage. Even a small negative voltage can be processed. However, it should be taken into account that a negative voltage will forward bias the source-bulk junctions of the switches. So only a small negative voltage is allowed.

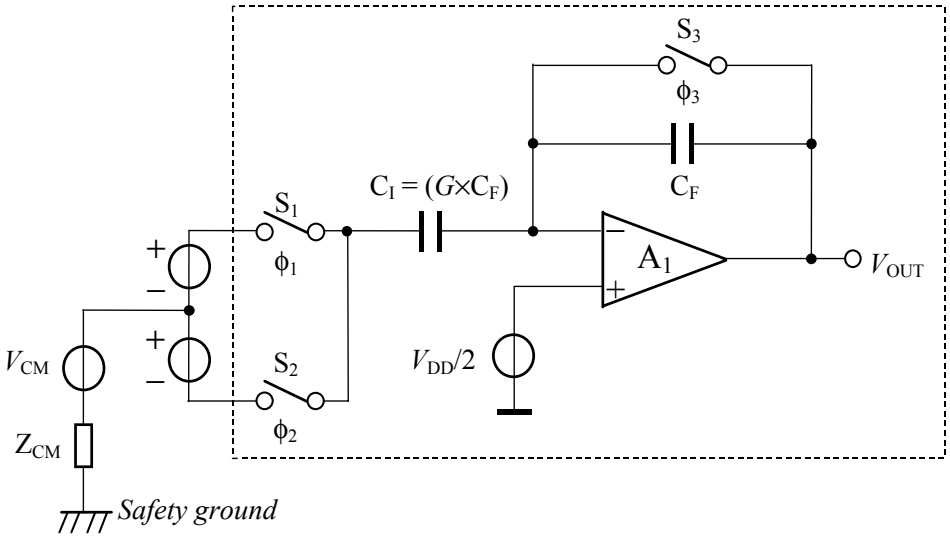

Figure 5.6 The switched-capacitor amplifier can isolate the common-mode voltage.

Figure 5.7 shows how the switched-capacitor amplifier can be integrated in the voltage-to-period converter.

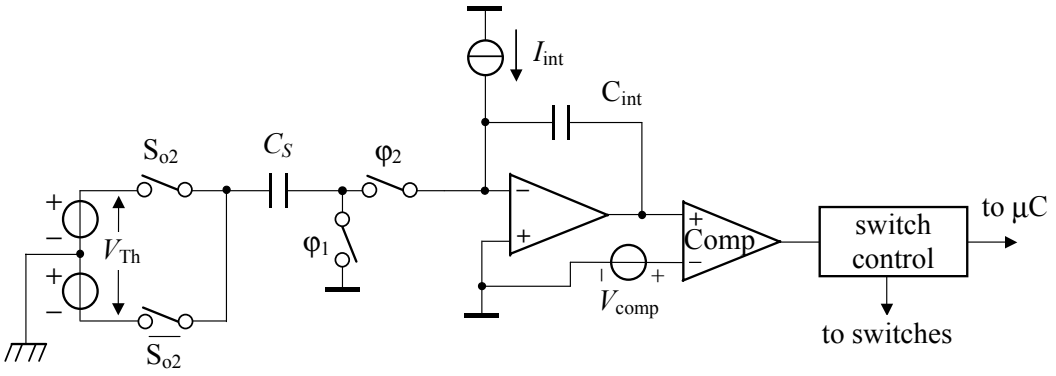

Figure 5.7 The switched-capacitor input in the voltage-to-period converter.

The time constant caused by the lead resistance R_S of a thermocouple and the sampling capacitor C_S of the voltage-to-period converter could result in some error. This error is due to the fact that sampling capacitor cannot sample the thermocouple voltage completely. Suppose that the time interval used to charge the sampling capacitor is T_1, and then at the end of T_1, the capacitor is charged to a voltage (see (4.26))

$$V_{\text{chg}} = V_{\text{Th}}\left(1 - e^{\frac{-T_1}{R_S C_S}}\right). \tag{5.5}$$

The relative inaccuracy due to the incomplete charging is $e^{\frac{-T_1}{R_S C_S}}$. For instance, a relative inaccuracy of less than 10^{-3} requires that

$$\frac{T_1}{R_S C_S} > 7 .$$

When, for instance, T_1 =10 µs, this yields for the time constant that $R_S C_S$ < 1.45 µs. In the case where the capacitance of the sampling capacitor is for example 80 pF, the lead resistance should be less than 18 kΩ.

If the measuring junction is located far from the measurement system, the lead resistance of the long cable can be rather high. In order to reduce the error caused by the large lead resistance, the interface circuit can be put close to the measuring junction, and the converted signal can be sent to measurement system. In this case, at least three wires are needed, or a special modulator is needed for two-wire current-loop transmission. This is also useful to reduce the effects of the leakage currents and of interference.

5.6 Configurations for Considering the Circuits with Bipolar Transistors

The on-chip temperature sensor and the on-chip bandgap reference can be realized with a multiple transistor configuration or a single transistor configuration. In this section we will describe these configurations for the CMOS temperature sensor and bandgap reference. Their performance will be compared in terms of accuracy, resolution and circuit complexity.

5.6.1 Configuration Using Multiple Bipolar Transistors

A processing circuit that uses multiple transistors can directly handle the voltage signals V_{BE} and ΔV_{BE}, as shown in Figure 5.8. A good reason to use a separate transistor Q_3 for base-emitter voltage generation is that the base-emitter voltage needs to be trimmed to the nominal value at a certain ambient temperature. This requires some special precautions, which we do not want to use for ΔV_{BE} generation. The voltage-to-period converter converts the voltage signals to periods. The output signal is shown in Figure 5.9.

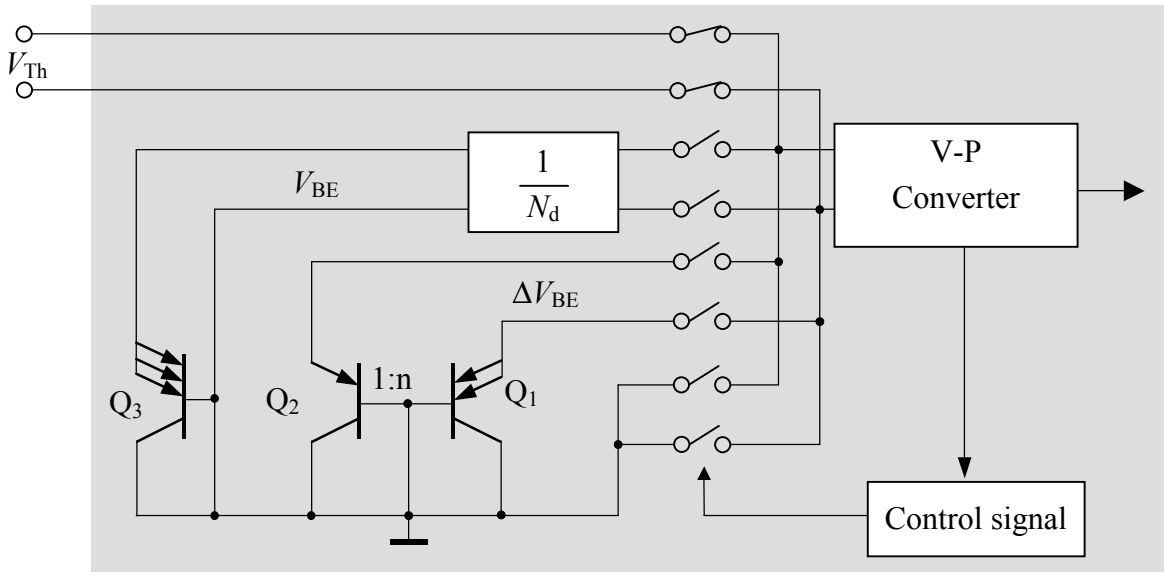

Figure 5.8 The schematic circuit of the thermocouple interface using multiple transistors for V_{BE} and ΔV_{BE}.

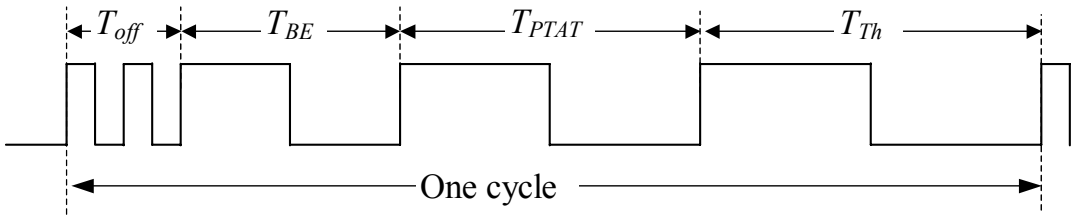

Figure 5.9 The output signal of the interface.

The four time intervals are determined by the four voltage signals, V_{off}, V_{BE}, ΔV_{BE} and V_{T}, according to the equations:

$$\begin{aligned} T_{\text{off}} &= KV_{\text{off}} + a_0 = a_0 \\ T_{\text{BE}} &= K\left(V_{\text{BE}} / N_{\text{d}}\right) + a_0 \\ T_{\Delta\text{VBE}} &= K\Delta V_{\text{BE}} + a_0 \\ T_{\text{Th}} &= KV_{\text{Th}} + a_0 \end{aligned} \tag{5.6}$$

where N_{d} is the division factor of the divider for the base emitter voltage and K and a_0 are the transfer parameters of the voltage-to-period converter. These time intervals can be measured using the counter of the microcontroller. The counted numbers N_{off}, N_{BE}, $N_{\Delta\text{VBE}}$ and N_{Th} correspond to the time intervals T_{off}, T_{BE}, $T_{\Delta\text{VBE}}$ and T_{Th}, respectively.

The thermocouple voltage V_{Th} and the temperature signal V_{ϑ} can be calculated by

$$\begin{aligned} M_1 &= \frac{N_{\text{Th}} - N_{\text{off}}}{N_{\text{d}}N_{\text{BE}} + c_1 N_{\Delta\text{VBE}} - (N_{\text{d}} + c_1)N_{\text{off}}} = \frac{V_{\text{Th}}}{V_{\text{ref}}} \\ M_2 &= \frac{c_2 N_{\Delta\text{VBE}} - N_d N_{\text{BE}} - (c_2 - N_{\text{d}})N_{\text{off}}}{N_{\text{d}}N_{\text{BE}} + c_1 N_{\Delta\text{VBE}} - (N_{\text{d}} + c_1)N_{\text{off}}} = \frac{V_{\vartheta}}{V_{\text{ref}}} \end{aligned}, \tag{5.7}$$

where c_1 and c_2 are design parameters, as described in Chapter 2, V_{ref} is the bandgap-reference voltage, and V_{ϑ} is the temperature-sensing voltage. Knowing the value of the bandgap-reference voltage and the ratios M_1 and M_2, one can derive the thermocouple voltage and the chip temperature.

5.6.2 Configuration Using a Single Bipolar Transistor

The bandgap-reference signal and the temperature sensor signal can also be obtained by using just one single bipolar transistor. The voltage ΔV_{BE} is obtained by subtracting the base-emitter voltages, which are successively measured for two different bias currents. The single transistor is biased in such a way that

$$\Delta V_{\text{BE}} = V_{\text{BE}}(I_2) - V_{\text{BE}}(I_1) = V_{\text{BE2}} - V_{\text{BE1}}, \tag{5.8}$$

which value equals that for the circuit of Figure 5.8. This voltage difference can also be sampled by the V-P converter and converted to a period, as shown in Figure 5.10. In this case the output signal is equal to that in Figure 5.9. The equations (5.6) and (5.7) are also valid for the circuit in Figure 5.10. The single transistor Q also needs to be trimmed. This does not affect the generation of the voltage ΔV_{BE}.

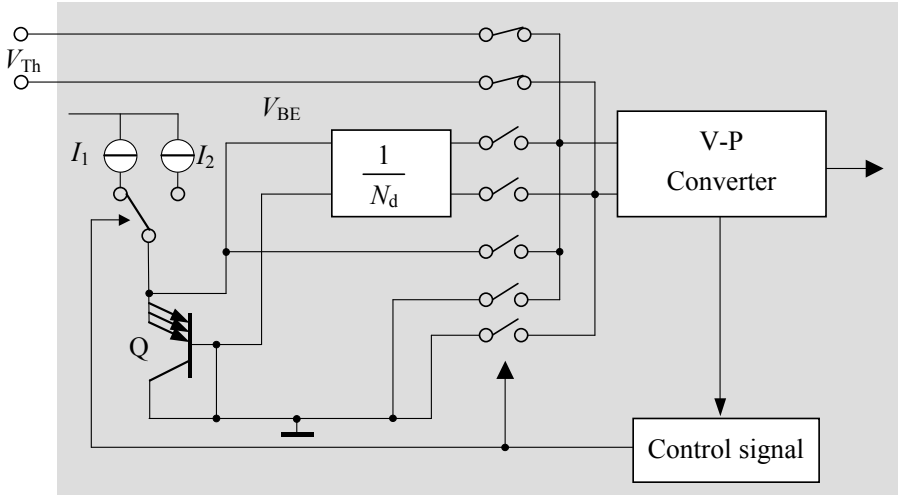

Figure 5.10 The schematic circuit of the thermocouple interface using a single transistor for V_{BE} and ΔV_{BE}.

5.6.3 Comparison of the Two Configurations

Comparing the circuit in Figure 5.8 and that in Figure 5.10, one can see that the circuit with a single bipolar transistor is simpler than that with multiple bipolar transistors. Some advantages of using a single transistor are:

- It saves some chip area, and
- It is not necessary to use the DEM technique to eliminate the effect of a mismatch between the bipolar transistors. However we still need to apply the DEM technique to generate an accurate ratio of the biasing currents.

Provided that the same voltage-to-period converter is applied, there is no difference between the performances of both kinds of circuits, such as the linearity and the noise. Overall, there is no strong reason to prefer one of the two configurations. We choose to apply the multiple-transistor configuration.

5.7 Conclusions

For the thermocouple measurement systems two variables must be measured: the thermocouple voltage and the reference-junction temperature. The object temperature can be derived from these two measurements. Inaccuracy of either measurement will affect the accuracy of the object-temperature measurement.

In order to measure the thermocouple voltage accurately, the measurement system must avoid thermal errors, and hence the measurement system:

- The temperatures of the two reference junctions of the thermocouple should be equal, and
- The temperatures of any other pair of connection junctions should also be equal.

These requirements can be realised by:

- Applying a high thermal-conductive medium for the material between the pairs of connection junctions;
- Locating the two reference junctions as close to each other as possible;
- Locating the two inputs to the interface as close to each other as possible;
- Locating the two inputs of the interface symmetrically with respect to any power-consuming points.

In order to reduce the cost and to simplify the measurement system, we choose an on-chip temperature sensor. Therefore, the interface circuit was designed such that it measures both the thermocouple voltage and its own temperature. Therefore, the chip temperature should be equal to the reference-junction temperature. But in fact, due to self-heating, there is a difference between these two temperatures, which results in a measurement error. By minimizing the power consumption of the interface and by making sure that the interface circuit is in good thermal contact with a heat sink, we minimized the measurement error due to self-heating.

In order to measure the thermocouple voltage accurately, we applied the three-signal technique to eliminate the additive and multiplicative uncertainties and errors of the interface circuit. This technique consists of measuring two extra signals: one reference signal and one offset signal in exactly the same linear way as the thermocouple voltage. For this reason, a reference voltage is required. An on-chip bandgap reference is preferred instead of an external one.

The total measurement error of the interface circuit is mainly due to the inaccuracy of the on-chip temperature sensor and the on-chip bandgap-reference voltage. The inaccuracy caused by the non-linearity of the voltage-to-period converter is negligible. The voltage resolution is limited by the noise-performance of the interface circuit.

The typical structures of thermocouples assembled in a metal well result in a thermocouple voltage with a floating or a grounded common-mode voltage. The switched-capacitor input configuration is very suitable to handle these voltages with a low-cost single-power-supply measurement system.

Bipolar transistors are used to generate the basic signals for the on-chip temperature sensor and the on-chip bandgap-reference. Both a single-transistor configuration and a multiple-transistor configuration can be applied. There is no significant difference in the circuit performances of these two configurations.

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Chapter 6 Design and Realization of a Smart Thermocouple Interface

6.1 Introduction

In this chapter we discuss the design and realization of an interface IC for thermocouples. The discussion includes the basic signal generation, the processing circuit and the voltage divider. Also the non-linearity and the resolution of the circuit are analysed. The circuit has been realised using CMOS technology. The experimental results are discussed.

6.2 Circuit Design

The design considerations and the basic requirements for the thermocouple measurement system have been discussed in Chapter 5. The interface circuit for thermocouples (see Figure 5.3) mainly consists of:

- A basic-signal generator, which generates the basic voltage signals V_{BE} and ΔV_{BE}. These signals are required for the on-chip temperature sensor and bandgap-reference voltage.
- A voltage-to-period converter, which converts the voltage signals to time signals.
- A logic-control circuit, which generates the control signals for the switches.
- A frequency divider, which divides the basic frequency of the voltage-to-period converter by N ($N = 2^n$).
- Biasing circuits, which bias the bipolar transistors, the active circuits of the voltage-to-period converter, etc.

In this section the design of these circuits is discussed.

6.2.1 The Generation of the Basic Signals

For an integrated bandgap reference and temperature sensor, two basic signals are required: a base-emitter voltage V_{BE} and the difference between two base-emitter voltages ΔV_{BE}.

The Voltage ΔV_{BE}

According to equation (2.21), the voltage difference ΔV_{BE} generated by two identical bipolar transistors ($I_{S2}/I_{S1} = 1$) biased at different current is

$$\Delta V_{BE}(\vartheta_R) = \frac{k\vartheta_R}{q} \ln \frac{I_{C2}}{I_{C1}}. \tag{6.1}$$

In our circuit, the current ratio I_{C2}/I_{C1} is designed to be 3.

Component mismatching causes errors in the current ratio I_{C2}/I_{C1} and the saturation-current ratio I_{S2}/I_{S1}. Applying the DEM technique, we can reduce errors due to mismatches to the second order, using for instance the circuit of Figure 6.1.

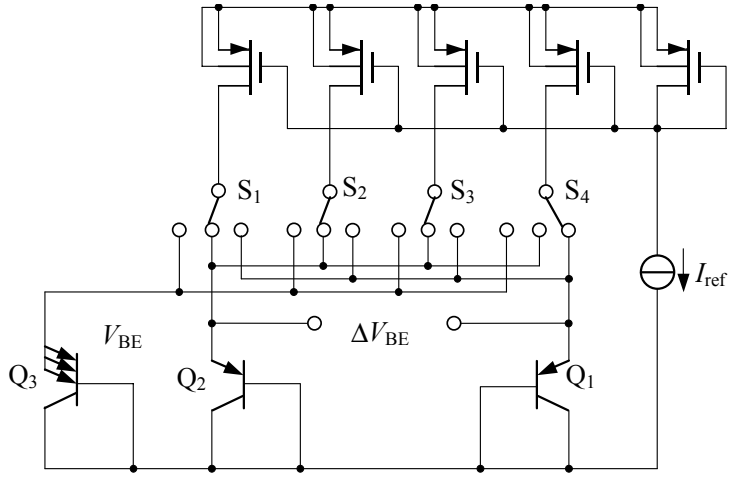

Figure 6.1 The schematic circuit for generating V_{BE} and ΔV_{BE}.

Four switches, S_1, S_2, S_3 and S_4, are controlled to bias the transistors Q_1 and Q_2. Table 6.1 illustrates the logic of the switches. A complete DEM cycle includes eight clock cycles. In the first four clock cycles (Phase A), the bias current for Q_1 is three times larger than that for Q_2; the voltage ΔV_{BE} corresponds to (V_{BE1} - V_{BE2}). Cycling of the current sources takes place in these four clock cycles. The effect of a mismatch between the current sources is reduced by taking the average of (V_{BE1} - V_{BE2}) in these four clock cycles. In the second four clock cycles (Phase B), the bias current for Q_2 is three times larger than that for Q_1; the voltage ΔV_{BE} corresponds to (V_{BE2} - V_{BE1}). By taking the average of the results in phase A and in phase B, we reduce the error induced by the mismatch between the two bipolar transistors. The sequence of the switches for controlling the biasing-current sources is given in Table 6.1.

	Phase A		Phase B	
	Q_1 biased via	Q_2 biased via	Q_1 biased via	Q_2 biased via
Phase 1	S_1, S_2, S_3	S_4	S_1	S_2, S_3, S_4
Phase 2	S_4, S_1, S_2	S_3	S_2	S_4, S_1, S_3
Phase 3	S_2, S_3, S_4	S_1	S_4	S_1, S_2, S_3
Phase 4	S_1, S_3, S_4	S_2	S_3	S_1, S_2, S_4

Table 6.1 The logic status of the switches for ΔV_{BE} generation applying DEM technique.

In order to prevent a voltage spike in bipolar transistors when the switches are changed from one stage to another, the switches should be arranged in a make-before-break design. In this

case, the base-emitter voltage does not drop to zero during switching. But special care has to be taken to ensure that the switches are operated in a make-before-break mode. This complicates the switch control. Therefore, we prefer an alternative solution in which the transistors are always continuously biased at least with a part of the current and the switches control only the additive amount of the current. In this way the base-emitter voltage cannot drop to 0V. We can achieve this by rearranging the above proposed switching sequence to Phase 1A, Phase 1B, Phase 2A, Phase 2B, Phase 3A, Phase 3B, Phase 4A, Phase 4B, (Table 6.1). Besides that there is no special requirement for the control logic design, and yet it is guaranteed that no zero biasing occurs throughout the complete measurement cycle.

The Base-Emitter Voltage V_{BE}

To generate the base-emitter voltage V_{BE}, we used a separate transistor Q_3. This transistor is equipped with a trimming network, which allows us to trim the base-emitter voltage at the ambient temperature towards to its nominal value, as shown in Figure 6.2.

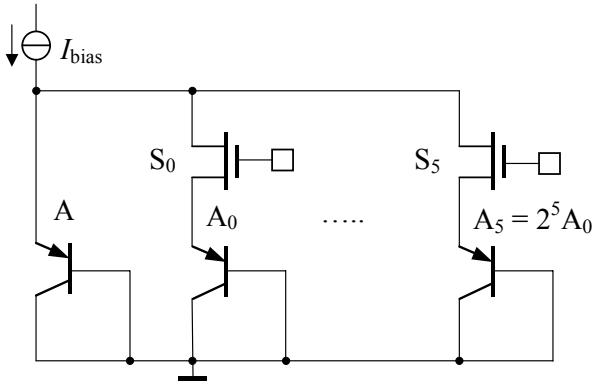

Figure 6.2 The trimming network for Q_3.

The base-emitter voltage was trimmed by adjusting the emitter area of transistor Q_3. According to the technology note of 0.7-µm CMOS technology, the spreading of the base-emitter voltage at room temperature is ±10 mV. We wanted to trim the base-emitter voltage with an accuracy of 0.5 mV. According to the design description of section 2.2.5, we designed a 6-bit trimming network.

Since the on-resistances can cause an error in the base-emitter voltage, low on-resistance analog switches were required. For the transistors through which a relatively large current can pass, wide-channel switches were applied to reduce the on-resistance.

Because the voltage signals are processed successively, the current sources used to generate ΔV_{BE} can also be used to bias the bipolar transistor Q_3, which generates the base-emitter voltage. When the base-emitter voltage has to be processed, the drains of the MOS transistors M_1 to M_4 are all connected to the transistor Q_3.

6.2.2 Bias Current for the Bipolar Transistors

As mentioned in Chapter 4 (equation (4.26)), the time constant $R_S C_S$, which is formed by the output resistor R_S of the voltage source and the sampling capacitor C_S, prevents that the

capacitor C_S is fully charged in the available time. According to equation (4.27), this will cause a relative error that is equal to

$$\varepsilon_{R_S C_S} = e^{-\frac{T_{1,1}}{R_S C_S}}, \tag{6.2}$$

where $T_{1,1}$ is the time used for charging the sampling capacitor. With $T_{1,1}$ = 10 µs, and for example, $\varepsilon_{R_S C_S} < 10^{-5}$, the time constant $R_S C_S$ should be less than 0.87 µs. With $C_S = \sum_{i=1}^{4} C_{Si}$ = 80 pF, the series resistance of R_S should be less than 11 kΩ.

The voltage source in our case is formed by a bipolar transistor, which is connected as a diode. It shows a small-signal resistance $(k\vartheta_T)/(qI_C)$. To ensure that the small-signal differential resistance of this bipolar transistor with short-circuited b-c terminals is less than 11 kΩ over the whole temperature range (from -40 °C to 160 °C), its bias current should be larger than 3.5 µA. In our design, we use a minimum bias-emitter current of 5 µA (room temperature).

6.2.3 Voltage-to-Period Converter

The modified charge-balancing oscillator has been designed to convert voltage signals into periods. The schematic circuit is shown in Figure 6.3.

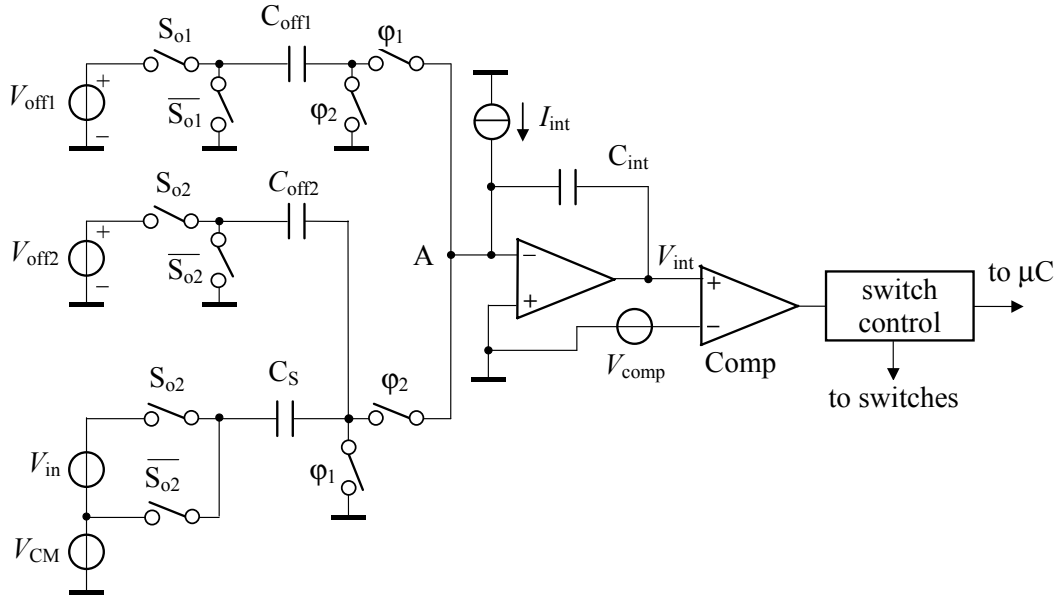

Figure 6.3 The modified charge-balancing oscillator.

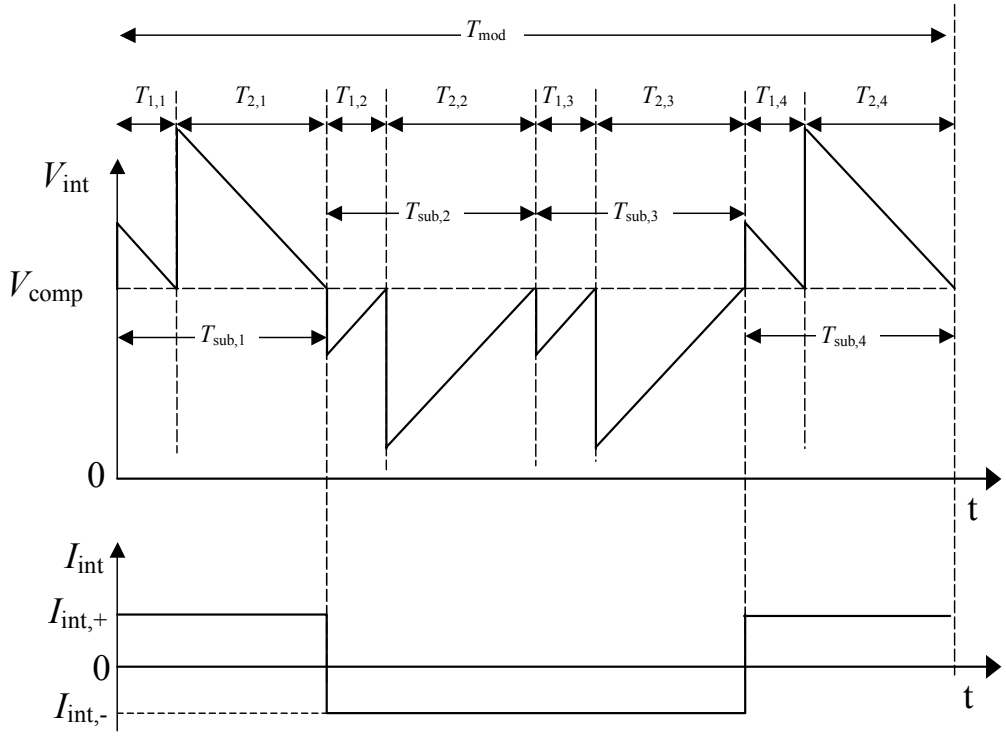

Figure 6.4 The waveforms of the integrator output voltage and the integration current I_{int}.

The capacitor C_{off1} is used to ensure that the input voltage V_{in} is properly sampled by the sampling capacitor C_S during period time T_1. And C_{off2} is applied to ensure that the oscillator is working properly when the input signal is zero or negative (see chapter 4.3 and [6.4]). During $T_{1,1}$, $T_{1,2}$, $T_{1,3}$ and $T_{1,4}$, the voltage V_{off1} is sampled (by C_{off1}) and converted into time interval. The time intervals are

$$\begin{aligned} T_{1,1} = T_{1,4} &= \frac{C_{off1} V_{off1}}{\left| I_{int,+} \right|} \\ T_{1,2} = T_{1,3} &= \frac{C_{off1} V_{off1}}{\left| I_{int,-} \right|} \end{aligned}, \tag{6.3}$$

where $I_{int,+}$ and $I_{int,-}$ represent the values of I_{int} in the corresponding time intervals. During $T_{2,1}$, $T_{2,2}$, $T_{2,3}$ and $T_{2,4}$, the voltage V_{off2} and the input voltage V_{in} are sampled by C_{off2} and C_S, respectively. The time intervals are

$$\begin{aligned} T_{2,1} = T_{2,4} &= \frac{C_{off2} V_{off2} + C_S V_{in}}{\left| I_{int,+} \right|} \\ T_{2,2} = T_{2,3} &= \frac{C_{off2} V_{off2} + C_S V_{in}}{\left| I_{int,-} \right|} \end{aligned}. \tag{6.4}$$

Since there is no strict requirement for the voltage signals V_{off1} and V_{off2}, the supply voltage V_{DD} is used to generate V_{off1} and V_{off2}.

When second-order chopping + - - + is performed (see Figure 6.4), a complete chopping cycle consists of four sub-sampling cycles. The time interval of T_{mod}, which includes a complete chopping cycle, depends on the input voltage according to the equation

$$T_{\mathrm{mod}} = \sum_{i=1}^{4}(T_{1,i} + T_{2,i}) = \frac{2C_{off1}V_{DD} + 2\left(V_{in}C_S + C_{off2}V_{DD}\right)}{\left|I_{\mathrm{int},+}\right|} + \frac{2C_{off1}V_{DD} + 2\left(V_{in}C_S + C_{off2}V_{DD}\right)}{\left|I_{\mathrm{int},-}\right|}. \quad (6.5)$$

To completely suppress the disturbing low-frequency signals caused by interference, offset, and $1/f$ noise, the values of $I_{\mathrm{int},+}$ and $I_{\mathrm{int},-}$ must be opposite with equal amplitude. With $\left|I_{\mathrm{int},+}\right| = \left|I_{\mathrm{int},-}\right| = \left|I_{\mathrm{int}}\right|$, equation (6.5) becomes

$$T_{\mathrm{mod}} = \frac{4\left(C_{off1}V_{DD} + C_{off2}V_{DD}\right) + 4V_{in}C_S}{\left|I_{\mathrm{int}}\right|}. \quad (6.6)$$

The output signal V_{int} of the integrator in Figure 6.3 has a frequency of about 50 kHz for the specified component values. For the reasons discussed in Chapter 5.3, we applied an n-bit digital divider to divide the high-frequency output of the integrator into a lower frequency. Thus, for each voltage (V_x) measurement, in the time interval T_x of the output signal of the interface as shown in Figure 5.9, the voltage signal was sampled $4N$ ($N = 2^n$) times. In our design $N = 256$.

The values of the capacitors C_{off1}, C_{off2}, C_S and C_{int} have been chosen according to the following considerations:

- The operation frequency should be higher than the corner frequency of the $1/f$ noise.
- The corresponding time intervals should meet the requirements of equations (4.28) and (4.32).

For instance, if we have $\tau_{HF} = 0.5$ µs, $\tau_{LF} = 2$ s, $\varepsilon_{HF} = \varepsilon_{LF} = 10^{-5}$, and $(T_{2,x} - T_{2,off})|_{max} = 2T_{1,1}$, then $T_{1,1} = 10$ µs will meet the requirements in equations (4.28) and (4.32).

When for V_{off1} and V_{off2}, a supply voltage of 5 V is applied, and when the integration current is 0.5 µA, with $T_{1,1} = 10$ µs, it is found that $C_{off1} = 1$ pF. With these component values, for zero input ($V_{in} = 0$), T_{mod} is 80 µs.

A large value of the sampling capacitor C_S results in a high measurement sensitivity. However, such a C_S also consumes a large chip area. For that reason the size of C_S is a trade-off between the measurement sensitivity and the chip area. In our design, the sampling capacitor C_S was chosen to be 80 pF, and it consumed a chip area of 1.2×10^5 µm^2 fabricated in the 0.7-µm CMOS technology of Alcatel Microelectronics. Usually, the maximum amplitude of the output of a thermocouple does not exceed 100 mV, so that $(T_{2,x} - T_{2,off})|_{max} <$ 16 µs. Under the above-mentioned conditions, the time interval of the oscillator output will meet the requirements in equations (4.28) and (4.32).

When we determined the value for C_{off2}, we assumed that $T_{2,x}$ should be positive even when the input voltage is negative. Usually, the maximum amplitude of a negative output voltage of a thermocouple does not exceed 10 mV. Therefore, a C_{off2} with a value larger than 0.16 pF can meet this requirement. In our design, C_{off2} was chosen to be equal to C_{off1}.

The value of the integrator capacitor C_{int} does not affect the voltage-to-period conversion; since only the charge transferred from the sampling capacitors to the integrator capacitor

together with the integration current determine the voltage-to-period conversion. But the value of the integrator capacitor determines the amplitude of the integrator output voltage, and thus it determines the relative effect of the voltage jitter of the comparator. In order to reduce the effect of the voltage jitter of the comparator, one should choose the integrator output voltage within the linear output range that is as large as possible. For this reason, we chose an integrator capacitor of 10 pF.

6.2.4 Design of the Integrator Op-amp

For the integrator op-amp we chose an Operational Transconductance Amplifier (OTA), because of its large output voltage swing and the simplicity of obtaining HF stability. Since the nonlinearity is not affected by the DC gain, as discussed in section 4.6, we used a single-stage topology. The schematic circuit of the applied OTA has been plotted in Figure 6.5. Because the transconductance of an NMOS transistor is larger than that of a PMOS transistor with the same size, NMOS transistors have been applied for the input stage. Since the effect of 1/*f* noise can be significantly reduced by applying the chopping technique, the relatively larger flicker noise of the NMOS transistor is not a problem [6.3].

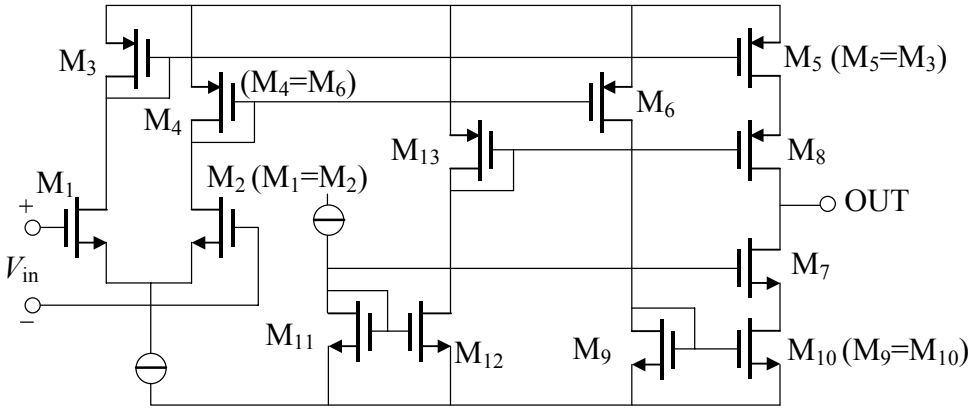

Figure 6.5 The schematic circuit of the OTA for integrator.

The minimum required bias current for the input stage depends on the desired high-frequency time constant τ_{HF} of the integrator and the noise requirements. In [6.4], F. van der Goes analyses the high-frequency time constant, which is given by

$$\tau_{HF} = \frac{C_{input}}{g_{m,\mathrm{int}}}\left(1 + \frac{C_{load,\mathrm{int}}}{C_{\mathrm{int}}}\right) + \frac{C_{load,\mathrm{int}}}{g_{m,\mathrm{int}}}, \tag{6.7}$$

where C_{input} represents the total capacitance at the input of the integrator, for which it holds that

$$C_{input} = C_{off1} + C_P \qquad \text{at } T_{1,\mathrm{i}}, \text{ and}$$

$$C_{input} = C_{off2} + C_P + C_S \qquad \text{at } T_{2,\mathrm{i}}.$$

Furthermore,

C_{p} = the parasitic capacitance at node A of Figure 6.3,

$g_{m,int}$ = the transconductance of the transistors M_1 and M_2,
$C_{load,int}$ = the load capacitance at the output of the OTA.

When C_{off2} = 1 pF, C_S = 80 pF, C_p = 5 pF, thus C_{input} = 86 pF, and with C_{int} =10 pF, $C_{load,int}$ = 2 pF, then in order to achieve that τ_{HF} = 500 ns, we should use an OTA with transconductance of at least 210 μA/V.

Let us assume that the bias current of the output stage equals that of the input stage. In that case, no extra transconductance is contributed by the output stage. Furthermore, when we assume that the transistors are operated in the strong inversion region, it holds that [6.3]

$$g_m = \sqrt{2K'(W/L)|I_D|}\ , \tag{6.8}$$

where K' = the transconductance parameter in the saturation region,
W/L = the width/length ratio of the MOS transistors M_1 and M_2,
I_D = the drain current of M_1 and M_2.

For the transistors fabricated in 0.7-μm CMOS technology of Alcatel Microelectronics ($K' \cong$ 90 μA/V^2) and the designed W/L (64.8 μm/2.4 μm), the required bias current is 9 μA for each transistor. In our case, we used a bias current of 25 μA.

6.2.5 Integration Current Source

In the voltage-to-period converter, the integration current I_{int} is very important. Its value, and the values of the sampling capacitors, determine the transfer gain of the circuit. According to the discussions in section 4.3, 4.5 and 6.2.3, some important requirements for the integration current are:

- The positive and the negative value of the current should be equal. A mismatch between these currents will not affect the linearity of the circuit, but it will deteriorate the suppression of the low-frequency interference.
- The output-impedance of the current sources should be large enough. Low output impedance will cause non-linearity of the voltage-to-period conversion.

A simple current source formed by a voltage source and a resistor R, as applied in the modified Martin oscillator (see Figure 6.6(a)), could also be applied in the voltage-to-period converter of Figure 6.6(b). However, this circuit has a main drawback: it has a relatively low output-impedance (R). For a current of 0.5 μA with a supply voltage of 5 V, the value of the resistor R should be 5 MΩ. With such a low output-impedance, any fluctuation in the inverting point of the op-amp will affect the value of the integration current I_{int}. Furthermore, such a low out-impedance cannot meet the second requirement either. Another drawback is that the inaccuracy of $V_{DD}/2$ and the offset voltage of the integrator op-amp will cause $|I_{int,+}| \neq |I_{int,-}|$.

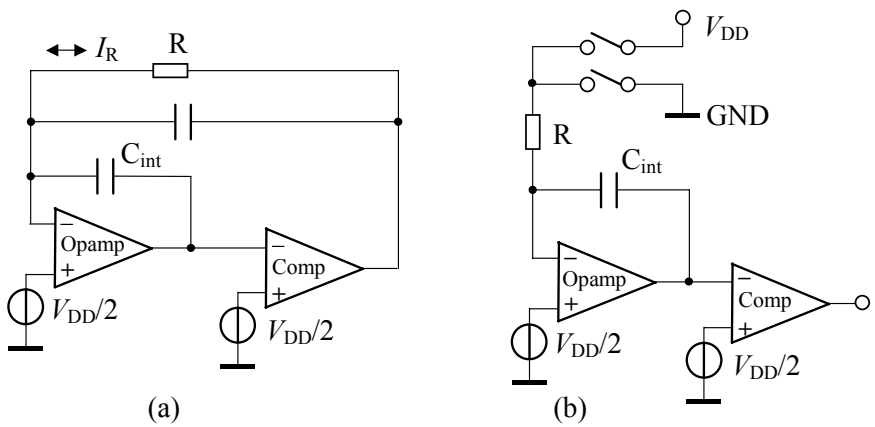

Figure 6.6 The integration current source for (a) the Martin oscillator and (b) the integrator of the voltage-to-period converter.

These problems can be solved with the circuit of Figure 6.7. This figure shows an alternative design of the integration current source that includes a current mirror.

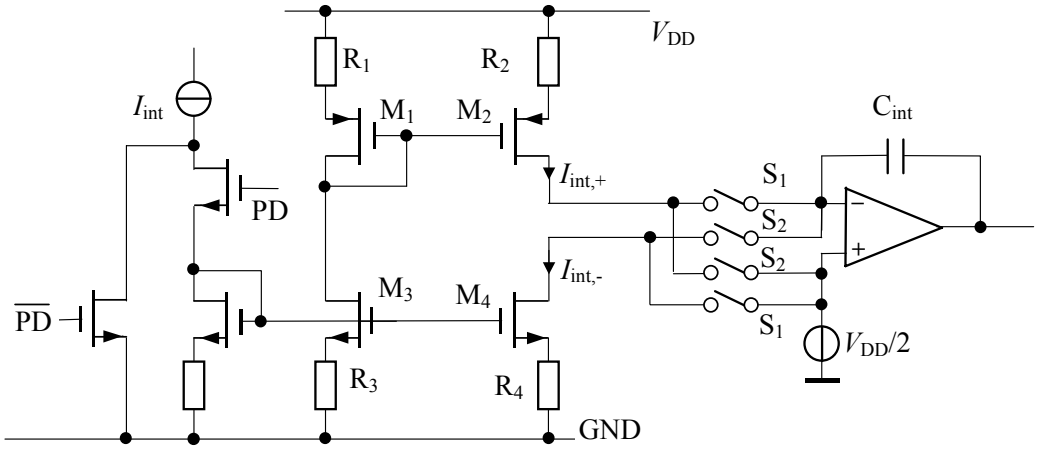

Figure 6.7 The integration current source using a current mirror.

For the output resistances $r_{out,+}$ and $r_{out,-}$ of the current mirror, it holds that:

$$\begin{aligned} r_{out,+} &= r_{ds2}(1+g_{m2}R_2) \\ r_{out,-} &= r_{ds4}(1+g_{m4}R_4) \end{aligned}, \tag{6.9}$$

where

$$\begin{aligned} g_m &= \frac{\partial I_{DS}}{\partial V_{GS}} = \sqrt{(2K'W/L)|I_D|(1+\lambda V_{DS})} \approx \sqrt{(2K'W/L)|I_D|} \\ r_{ds} &= \frac{\partial V_{ds}}{\partial I_{ds}} = \frac{1+\lambda V_{DS}}{\lambda I_D} \approx \frac{1}{\lambda I_D} \end{aligned}. \tag{6.10}$$

I_D is the drain current of the MOS transistor, which equals $I_{int,+}$ and $I_{int,-}$ for M_2 and M_4, respectively. The other parameters are: μ the mobility of the channel carriers, C_{ox} the oxide capacitance per unit area, and W/L the width/length ratio of the MOS transistor.

The current mismatch of the current mirror depends on the drain/collector current of transistors. The typical characteristic of the current mismatch of the current mirror versus the drain/collector current is illustrated in Figure 6.8 [6.1]. To minimize the current mismatch, the transistor pairs (M_1, M_2) and (M_3, M_4) should be operated in strong inversion. The mismatch can be reduced further by using large-sized MOS transistors with a large WL product. An additional advantage of using such transistors with a long channel is that the corresponding low value of λ results in a higher output resistance r_{ds}. For example, with the practical values $|I_{int,+}| = |I_{int,-}| = 0.5\,\mu A$, g_m = 5 µA/V, $R_2 = R_4$ = 1 MΩ, $\lambda = 7.3\times10^{-4}$ V^{-1} for NMOS and 8.7×10^{-4} V^{-1} for PMOS [6.2] with a channel length of 2.4 µm, the output resistance equals 16 GΩ and 14 GΩ for current sources $I_{int,+}$ and $I_{int,-}$, respectively.

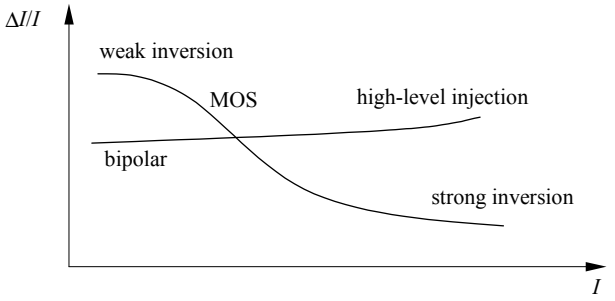

Figure 6.8 The current mismatch of the current mirror versus the drain/collector current for bipolar and CMOS transistors.

6.2.6 Division of Base-Emitter Voltage

As explained in Section 4.5, the resistive-capacitive voltage divider is not suitable for dividing the base-emitter voltage. Therefore, we applied a pure capacitive voltage divider. In order to realize the pure capacitive voltage divider, we split the sampling capacitor C_S in Figure 6.3 into four small capacitors, corresponding to C_{S1} to C_{S4} (Figure 6.9), where each small capacitor was controlled by two switches for the base-emitter voltage sampling. The voltage division was realized by controlling the sampling switches, as explained in Section 4.5.

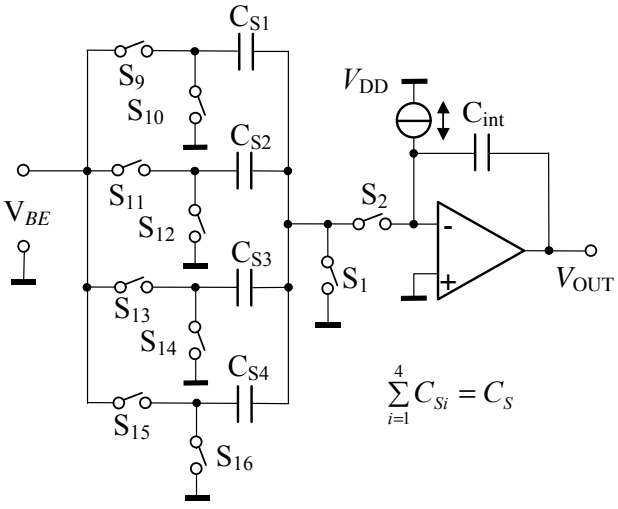

Figure 6.9 The circuit for base-emitter voltage division.

For small voltage signals, which do not have to be divided, the switches were controlled in such a way that the four small capacitors were functioning in parallel, just like a single capacitor C_S. The control logic is changed when the base-emitter voltage is processed. Each time, only one of the four small capacitors C_{Si} (i∈ 1,4) samples the voltage signal. The charge in the small capacitor $V_{BE}C_{Si}$ is transferred to the integrator capacitor C_{int} only one time in a complete sampling cycle T_{mod}. Figure 6.10 shows the integrator-output waveforms for both small and large input voltages.

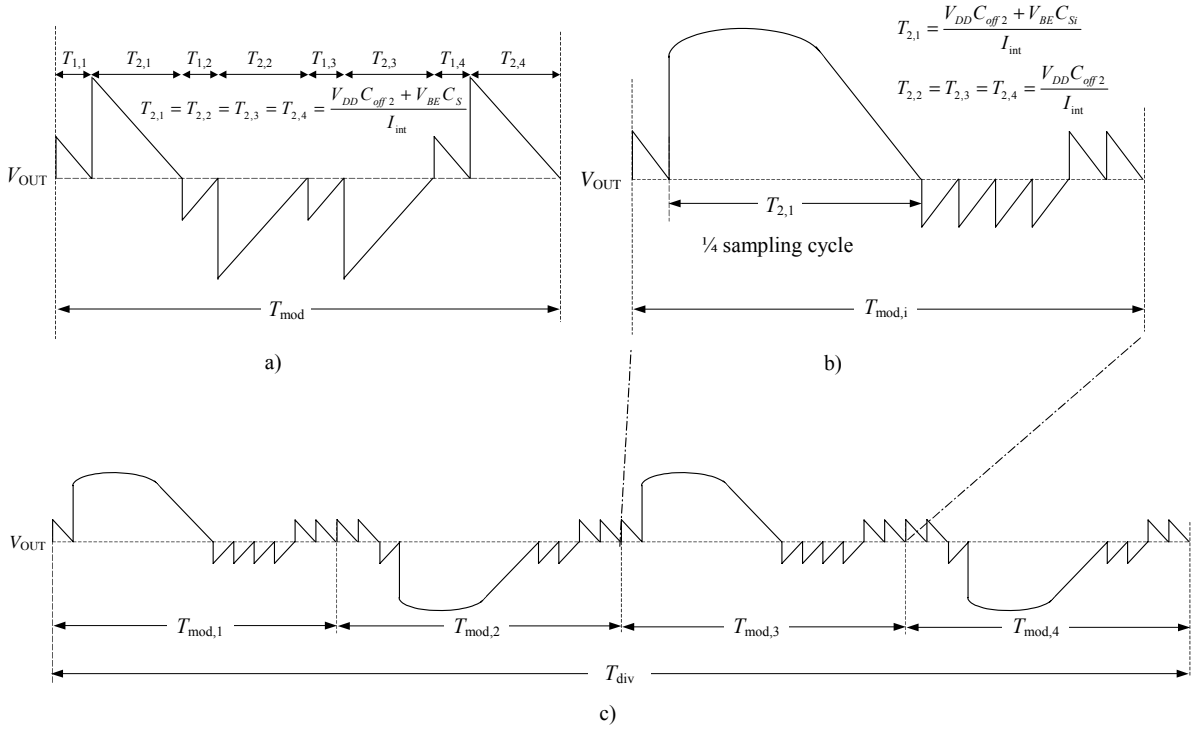

Figure 6.10 The integrator output a) for small-voltage conversion b) for large-voltage conversion and c) for a complete division cycle for large voltages.

For large input voltages, a complete division cycle includes a complete rotation of the small sampling capacitors during the four sampling cycles $T_{mod,i}$ (i = 1 ~ 4) . The total time interval for a complete rotation cycle is

$$T_{div} = \sum_{i=1}^{4} T_{\mathrm{mod},i} = \sum_{i=1}^{4} \left\{ \frac{4\left(C_{off1}V_{DD} + C_{off\,2}V_{DD}\right)}{\left|I_{\mathrm{int}}\right|} + \frac{C_{Si}V_{BE}}{\left|I_{\mathrm{int}}\right|} \right\} = 4\frac{4\left(C_{off1}V_{DD} + C_{off\,2}V_{DD}\right)}{\left|I_{\mathrm{int}}\right|} + \frac{V_{BE}C_S}{\left|I_{\mathrm{int}}\right|} \quad (6.11)$$

Compared to the time conversion of the small voltage signal as formulated in equation (6.6), the large voltage signal (base-emitter voltage) is divided with an equivalent factor of 16. It is also possible to design other voltage division factors. But for design simplicity, a division factor of 2^n is to be preferred. Since a complete voltage division takes four sampling cycles, the minimum factor of the frequency divider (N) should be also four.

6.2.7 The Complete Circuit

The complete circuit of the thermocouple interface is shown in Figure 6.11. The $V_{DD}/2$ voltage source, which is used for the non-inverting node of the integrator and the comparator, was implemented with a resistive voltage divider followed by a buffer. A frequency divider divides the modulated signals to lower frequencies for the reasons discussed in Section 5.3. The switch-control block generates the control signals for all the switches.

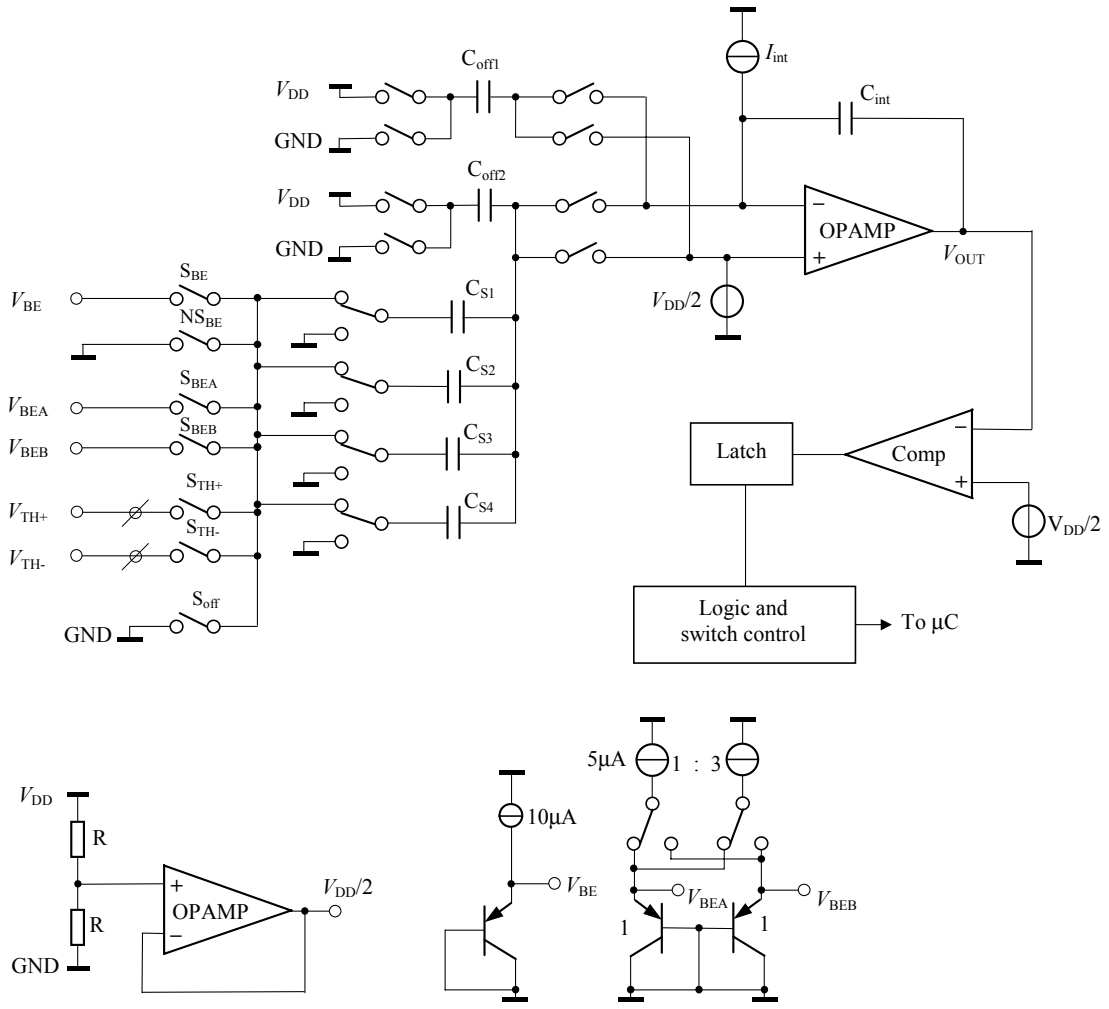

Figure 6.11 The complete interface circuit.

6.3 Non-Linearity

The sources of non-linearity were discussed in Chapter 4. As concluded in Chapter 4, possible causes of the non-linearity of the interface circuit are the low- and high-frequency poles of the integrator, and the voltage dependence of the sampling capacitor. These effects will be considered here. For our specific design of the op-amp, we have a DC gain of 100 dB ($A_{int} = 10^5$) and $C_{int} = 10$ pF. The input resistance is very high (> a few GΩ). According to (4.29), this yields a time constant of the low-frequency pole of 1×10^3 s. In this case, according to (4.31), the non-linearity due to the low-frequency pole is negligible. According to (4.33)

and with $A_{int} = 1\times10^5$, $\tau_{int} = 0.02$ s, $C_S = 80$ pF, $C_{pb} = 10$ pF and $C_{int} = 10$ pF, the time constant of the high-frequency pole is 200 ns. When, for example, $T_{2,x1} = 6$ µs (when the input signal is negative), according to (4.35), the non-linearity due to the high-frequency pole is 9.3×10^{-14}. This is also negligible.

As discussed in Chapter 4, the voltage dependency of the sampling capacitor C_S induces a non-linearity. The examples given in section 4.6.1 to analyze the non-linearity caused by the voltage dependence of the sampling capacitor represent our practical design. This shows a non-linearity of 22×10^{-6}.

Based on the above analysis, we concluded that the voltage dependence of the sampling capacitor C_S is the dominant source of non-linearity.

6.4 Noise Analysis

The noise sources of the voltage-to-period converter and the noise of the basic-signal voltages V_{BE} and ΔV_{BE} determine the input-voltage resolution. The noise sources of the voltage-to-period converter have been analysed in Chapter 4, and will be briefly reviewed in this section. The noise at the basic voltage signals V_{BE} and ΔV_{BE} will also be analysed, since these noise voltages will affect the thermocouple voltage measurement via the three-signal calculation.

6.4.1 Noise of the Voltage-to-Period Converter

The noise sources of the time-to-period converter and their effects on the variances in the time domain have been analyzed in detail by Frank v. d. Goes [6.4] and are reviewed in Chapter 4. Table 4.1 lists the variances in the time domain for the interface output signal due to the various noise sources. From the expression for these variances, it can be seen that these variances are not sensitive to the 1/*f* noise. This is due to the applied chopping technique.

The quantization noise depends on the counting frequency of the microcontroller. By choosing a microcontroller with high clock frequency and thus a high counting frequency, one can reduce the quantization noise such that it is non-dominant.

In the interface circuit for thermocouples, we applied an on-chip bandgap-reference voltage. This bandgap-reference voltage was obtained after data processing of the signals V_{BE} and $V_{\Delta VBE}$. The ratio between the unknown input V_x and the bandgap-reference V_{ref} is determined by

$$M = \frac{T_x - T_{off}}{N_d (T_{BE} - T_{off}) + C_2 (T_{\Delta V_{BE}} - T_{off})} = \frac{V_x}{V_{ref}}, \tag{6.12}$$

where T_x, T_{BE}, $T_{\Delta VBE}$ and T_{off} correspond to the output period for the voltages V_x, V_{BE}, ΔV_{BE} and V_{off}, respectively, N_d is the factor of the voltage divider for the base-emitter voltage, and C_2 is a design constant for the bandgap-reference voltage (see section 2.2.4).

The equations for the variances in the time domain, listed in Table 4.1 for the different noise sources, are valid for all the four measurement phases, T_x, T_{BE}, $T_{\Delta VBE}$ and T_{off}. The total ratio variance σ_M can be expressed as

$$\sigma_M^2 \cong \left(\frac{\partial M}{\partial T_x}\right)^2 \sigma_x^2 + \left(\frac{\partial M}{\partial T_{BE}}\right)^2 \sigma_{BE}^2 + \left(\frac{\partial M}{\partial T_{\Delta V_{BE}}}\right)^2 \sigma_{\Delta BE}^2 + \left(\frac{\partial M}{\partial T_{off}}\right)^2 \sigma_{off}^2 . \quad (6.13)$$

According to the equations listed in Table 4.1, for most of the noise sources, the corresponding time variances do not depend on the phases, except for the noise current at the input of the integrator. However, the current noise in the MOSFET op-amp is very low and therefore its influence can be neglected. In this case, for all the time variances in each phase, it holds that

$$\sigma_x^2 = \sigma_{BE}^2 = \sigma_{\Delta BE}^2 = \sigma_{off}^2 = \sigma^2 , \quad (6.14)$$

where σ represents the total time variance caused by the noise sources listed in Table 4.1, which equals

$$\sigma^2 = \sigma_{ni}^2 + \sigma_{nc}^2 + \sigma_{ns}^2 + \sigma_{SC}^2 + \sigma_{clk}^2 . \quad (6.15)$$

Thus, equation (6.13) becomes

$$\sigma_M^2 \cong \left[\left(\frac{\partial M}{\partial T_x}\right)^2 + \left(\frac{\partial M}{\partial T_{BE}}\right)^2 + \left(\frac{\partial M}{\partial T_{\Delta V_{BE}}}\right)^2 + \left(\frac{\partial M}{\partial T_{off}}\right)^2\right]\sigma^2 . \quad (6.16)$$

After substitution of equation (6.10) in equation (6.14), it is found that

$$\sigma_M^2 = \sigma^2 \frac{K'}{\left[N_d\left(T_{BE} - T_{off}\right) + C_2\left(T_{\Delta V_{BE}} - T_{off}\right)\right]^2} , \quad (6.17)$$

where for the constant K' it is found that

$$K' = 2 + 2M^2\left(N_d^2 + C_2^2 + N_d C_2\right) - 2M\left(N_d + C_2\right). \quad (6.18)$$

Example: with N_d =16, C_2 =25 and V_{ref} = 1.255 V, for the input voltage from -20 mV to 100 mV, K' ranges from 1.3 to 12.

According to (4.46), the voltage resolution is obtained from

$$\Delta v_x = \frac{\sigma_M}{\frac{\partial M}{\partial V_x}} = V_{ref}\sigma_M . \quad (6.19)$$

Example: with the practical parameters C_S = 80 pF, $C_{off1} = C_{off2}$ = 1 pF, C_{int} = 10 pF, C_p = 10 pF (C_{total} = 102 pF), N = 256, the simulation result of the integrator op-amp shows that B_{int} = 500 kHz and S_{uni} = 6×10^{-16} V^2/Hz, S_{unc} = 6×10^{-16} V^2/Hz, B_{comp} = 5 MHz and t_s = 0.3 µs. Assuming the input voltage is noise free (S_{uns} = 0), then the noise-induced time variances are:

σ_{ni}^2 = 1.28×10^{-14} s^2,

σ_{nc}^2 = 1.2×10^{-15} s^2,

$\sigma_{ns}^2 = 0$,
$\sigma_{SC}^2 = 3.5\times10^{-15}$ s^2 and
$\sigma_{clk}^2 = 1.5\times10^{-14}$ s^2.

Then the total time variance is $\sigma^2 = 3.25\times10^{-14}$ s^2.

At room temperature, we have: $V_{BE} = 0.6$ V, $\Delta V_{BE} = 28.5$ mV, $N_d = 16$ and $C_2 = 25$, so that

$$T_{off} = \frac{4(C_{off1} + C_{off2})V_o}{I_{int}} N = 2.04\times10^{-2} \text{ s}$$

$$T_{BE} = T_{off} + \frac{4NC_S V_{BE}}{I_{int}} \frac{1}{N_d} = 2.64\times10^{-2} \text{ s}$$

$$T_{\Delta VBE} = T_{off} + \frac{4NC_S \Delta V_{BE}}{I_{int}} = 2.51\times10^{-2} \text{ s}$$

$$N_d(T_{BE} - T_{off}) + C_2(T_{\Delta V_{BE}} - T_{off}) = 0.213 \text{ s}.$$

As the input voltage V_x affects the value of K', the value of σ_M^2 depends on the input voltage. For the worst-case scenario, which is V_x =100 mV, K' amounts to 12. Under this condition, we have that $\sigma_M^2 = 8.6\times10^{-12}$. Equation (6.19) gives the voltage resolution, which is 3.7 μV.

6.4.2 Noise of the Bipolar Transistors

The power spectral density of the voltage noise of a bipolar transistor connected as a diode can be expressed as

$$\frac{v^2}{\Delta f} = 4k\vartheta\left(r_b + \frac{1}{2g_m}\right), \tag{6.20}$$

where r_b is the base resistance and g_m is the transconductance of the transistor. Since the base-emitter voltage is sampled N times for a complete conversion period, the effective noise voltage is

$$v_{BE} = \sqrt{\frac{4k\vartheta\left(r_b + \frac{1}{2g_m}\right)B_{int}}{N}}, \tag{6.21}$$

where B_{int} represents the bandwidth of the integrator. The input voltage noise due to the voltage noise of the base-emitter voltage is determined by

$$v_{in\_BE} = M\left(\frac{\partial V_{ref}}{\partial V_{BE}}\right)v_{BE} = Mv_{BE}. \tag{6.22}$$

Example: in our design, the bipolar transistor is biased at 10 µA at room temperature, r_b = 300 Ω, B_{int} = 500 kHz and N = 256, which yields v_{BE} = 0.23 µV. For an input of 50 mV, M is 0.04 (V_{ref} = 1.25 V), so the equivalent input voltage noise is 9 nV. Compared to the contribution of the noise sources of the integrator, the noise of the base-emitter voltage is negligible.

Similarly, the voltage noise of the ΔV_{BE} generator is

$$\frac{v^2}{\Delta f} = 4k\vartheta\left(r_{b1} + \frac{1}{2g_{m1}}\right) + 4k\vartheta\left(r_{b2} + \frac{1}{2g_{m2}}\right), \tag{6.23}$$

where r_{b1}, r_{b2}, are the base resistances of the two bipolar transistors, which are applied to generate the voltage ΔV_{BE}, respectively, and g_{m1}, g_{m2} represent the transconductance of the two transistors respectively. Because the voltage ΔV_{BE} is sampled 4N times in a complete conversion period, the equivalent voltage noise is

$$v_{\Delta V_{BE}} = \sqrt{\frac{\left[4k\vartheta\left(r_{b1} + \frac{1}{2g_{m1}}\right) + 4k\vartheta\left(r_{b2} + \frac{1}{2g_{m2}}\right)\right]B_{int}}{4N}}. \tag{6.24}$$

The equivalent input noise voltage due to the voltage noise of the base-emitter voltage amounts to

$$v_{in\_\Delta V_{BE}} = M\frac{\partial V_{ref}}{\partial(\Delta V_{BE})}\upsilon_{\Delta V_{BE}} = (MC_2)v_{\Delta V_{BE}}. \tag{6.25}$$

Example: in our design, two transistors are biased at 5 µA and 15 µA, respectively, where r_{b1} = r_{b2} = 300 Ω, B_{int} = 500 kHz and N = 256, the voltage noise is 0.18 µV. With C_2 = 25, for an input of 50 mV, M is 0.04 (V_{ref} = 1.25 V); substitution of these values in (6.25) shows that the equivalent input noise is 0.18 µV.

These examples show that the noise of the bipolar transistors is very small compared to the contribution of the noise from the voltage-to-time converter (3.7 µV).

6.5 Measurement Results

The thermocouple interface was fabricated using 0.7-µm CMOS technology of Alcatel Microelectronics. A small amount of chips were packaged and tested. In this section, we present and discuss the test results, including the measurement accuracy and the voltage resolution.

6.5.1 The Whole Chip Design

A microphotograph of the interface circuit is shown in Figure 6. 12. The die size is 3.23 mm^2 (1.9 mm × 1.7 mm). For test purposes, the chip was packaged in a 16-pin ceramic DIL package.

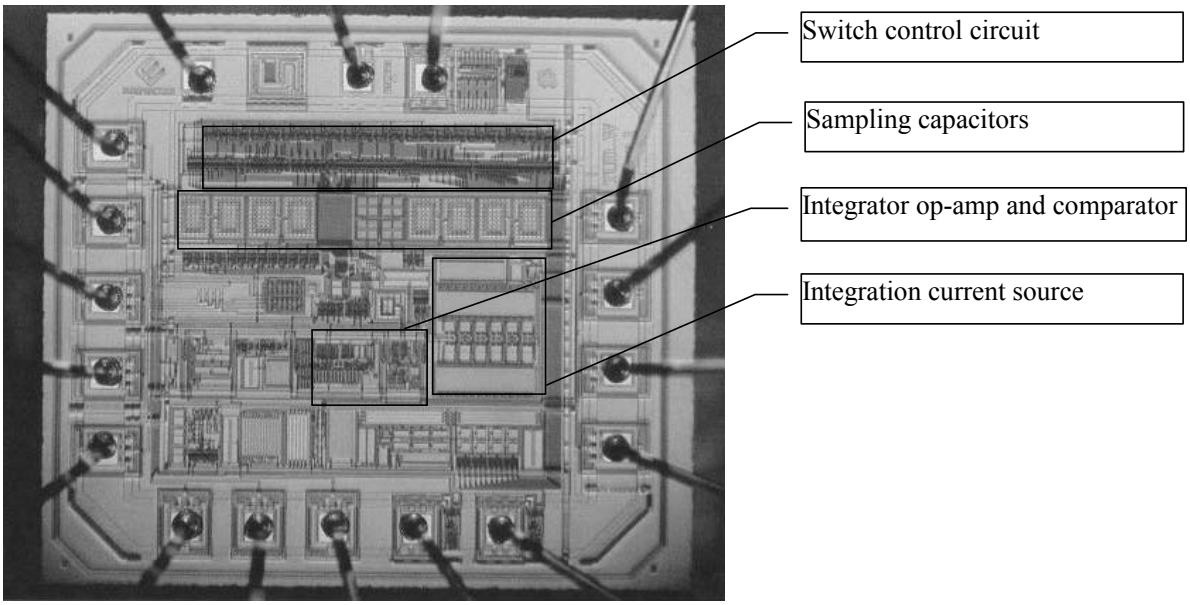

Figure 6. 12 Photograph of the thermocouple interface. The chip measures 1.9 mm×1.7mm and was packaged in a 16-pin ceramic DIL package.

Bipolar transistors, which are applied to sense the chip temperature, have been placed as far as possible from the power-consuming circuit blocks, such as the op-amps. To minimize the piezo-junction effect, we placed the bipolar transistors, especially the base-emitter-voltage-generating transistor, around the centre of the chip, where the stress is believed to be relatively constant and well predictable.

The tests were performed with a supply voltage of 5 V, over a temperature range from -40 °C to 140 °C.

6.5.2 Accuracy of the Voltage Divider

In order to test the performance of the voltage divider, instead of the on-chip base-emitter voltage, we applied an external voltage V_L to the input of V_{BE}. Another voltage source $V_{Th,test}$ was applied at the thermocouple input.

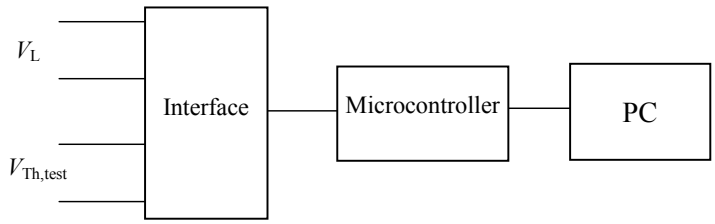

Figure 6.13 The test set-up for the voltage divider evaluation.

The periods T_{off}, T_L, $T_{\Delta VBE}$ and T_{Th} of the output signal correspond to the input V_{off}, V_L, $V_{\Delta VBE}$ and V_{Th}, according to the equations

$$\begin{aligned} T_{off} &= K \cdot V_{off} + a_0 \\ T_L &= K \cdot (V_L / N_d) + a_0 \\ T_{\Delta V_{BE}} &= K \cdot \Delta V_{BE} + a_0 \\ T_{Th} &= K \cdot V_{Th,test} + a_0 \end{aligned}, \tag{6.26}$$

respectively. These periods are measured by a microcontroller using its internal counter. The counted numbers N_{off}, N_{L}, $N_{\Delta\text{VBE}}$ and N_{Th} correspond to T_{off}, T_{L}, $T_{\Delta\text{BE}}$ and T_{Th}, respectively. The factor N_{d} of the divider equals

$$N_d = \frac{V_L}{V_{Th,test}} \cdot \frac{N_{Th} - N_{off}}{N_L - N_{off}}, \tag{6.27}$$

For the purpose of chip testing, we measured the voltage V_{L} and V_{Th} using an accurate multimeter. The extracted divider factor is shown in Figure 6.14.

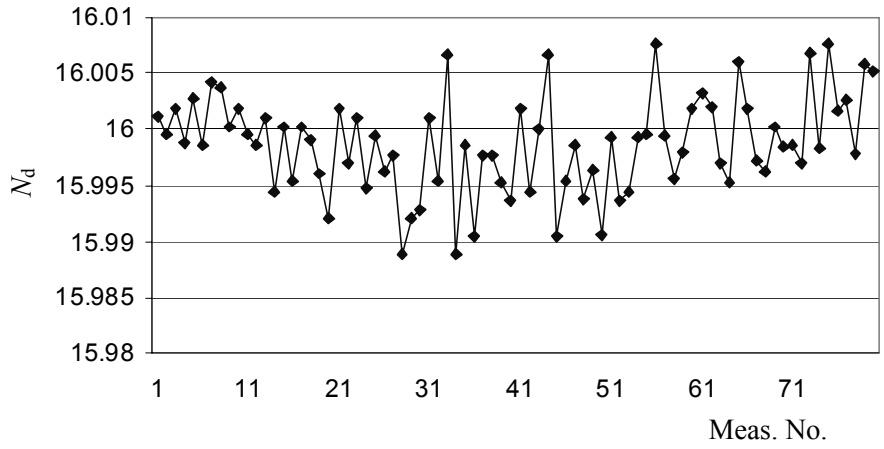

Figure 6.14 The extracted factor of the voltage divider, designed for N_D = 16.

The average and the standard deviation of the measured divider factor were N_{D} = 15.998 and σ = 0.004, respectively. Every single measurement took less than 100 ms. For this reason we concluded that the dynamic divider has a rather good performance.

6.5.3 Base-Emitter Voltage and ΔV_{BE}

Using the external input voltage $V_{\text{Th,test}}$ as a reference signal, we calculated the on-chip voltage signals V_{BE} and ΔV_{BE} using the equations

$$V_{BE,meas.} = \frac{N_d \left(N_{BE} - N_{off}\right)}{N_{Th} - N_{off}} V_{Th,test}, \tag{6.28}$$

and

$$\Delta V_{BE,meas.} = \frac{N_{\Delta V_{BE}} - N_{off}}{N_{Th} - N_{off}} V_{Th,test}\,, \tag{6.29}$$

where N_{off}, N_{BE}, $N_{\Delta\mathrm{VBE}}$ and N_{Th} correspond to T_{off}, T_{BE}, $T_{\Delta\mathrm{VBE}}$ and T_{Th}, respectively. The calculated voltages V_{BE} and ΔV_{BE} are plotted in Figure 6.15 versus the temperature.

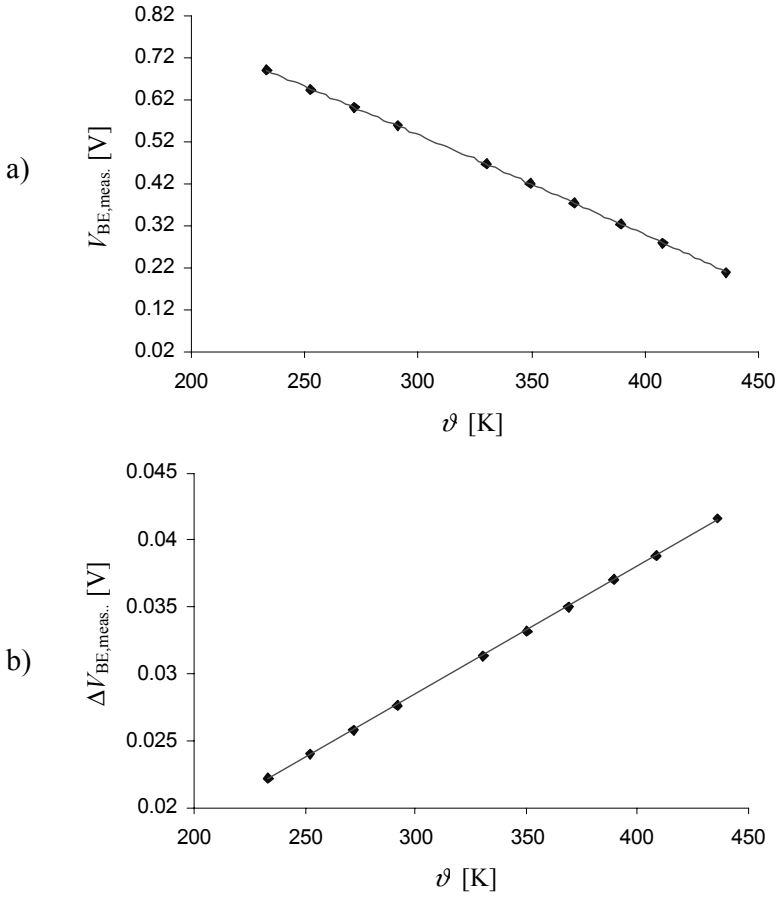

Figure 6.15 The measured base-emitter voltage and the voltage ΔV_{BE}.

As a reference, we measured the temperature with an accurate Platinum resistor. The measured voltage ΔV_{BE} depicted in Figure 6.15(b) was slightly larger than the one calculated with the simple equation (2.21). As discussed in Chapter 3, this is mainly due to the effects of the base resistance of the bipolar transistor and non-unit of the effective emission coefficient m. Both effects can be taken into account by replacing the parameter m by m', according to equation

$$\Delta V_{BE} = \frac{m' k \vartheta}{q} \ln n\,. \tag{6.30}$$

According to the characterization results presented in section 3.3, m' is 1.003. The measurement results show that this precisely models both effects. Therefore, during data

processing for the bandgap reference and the on-chip temperature, we applied a correction factor of m' (m' = 1.003).

6.5.4 On-Chip Bandgap-Reference Voltage

In the designed interface circuit, no bandgap-reference voltage with a time-continuous output is available. The value of the bandgap-reference voltage should be derived from data processing performed by the microcontroller. Now the calculation based on the experimental results will be compared with the designed nominal value.

According to the characterization results of the pnp vertical bipolar transistors fabricated in 0.7-um CMOS technology, presented in Chapter 3, we have the parameters V_{g0} = 1.146 V and η = 4.23. The bandgap-reference voltage has been designed for a reference temperature (ϑ_r) of 320 K. With n = 0 (constant bias current for bipolar transistors), equation (2.22) gives the value of the bandgap-reference voltage:

$$V_{ref,nom} = V_{go} + (\eta - n)\frac{k\vartheta_r}{q} = 1.263 \text{ V}. \tag{6.31}$$

The base-emitter voltage $V_{BE}(\vartheta_r)$ has been chosen to be 0.55 V at the reference temperature. According to (2.15), the temperature coefficient of the base-emitter voltage is

$$\lambda = \frac{V_{ref,design} - V_{BE}(\vartheta_r)}{\vartheta_r} = 0.002355 \ \ V/K. \tag{6.32}$$

This value determines the required amplification factor C_2 for the voltage ΔV_{BE}

$$C_2 = \frac{\lambda}{\frac{k\vartheta_r}{q}\ln n} = 24.87. \tag{6.33}$$

Taking into account the correction factor m' for the voltage ΔV_{BE}, we define a corresponding corrected parameter C'_2 according to the equation

$$C_2' = \frac{C_2}{m'}. \tag{6.34}$$

Substituting these design parameters together with the measurement results of the interface output signals N_{off}, N_{BE}, $N_{\Delta VBE}$ and N_{Th}, in equations (6.28) and (6.29), and according to (2.20), we calculated the value of the virtual bandgap-reference voltage from the equation

$$\begin{aligned} V_{ref,meas.} &= V_{BE,meas.} + C_2'\Delta V_{BE,meas.} \\ &= \frac{N_d\left(N_{BE} - N_{off}\right) + C_2'\left(N_{\Delta V_{BE}} - N_{off}\right)}{N_{Th} - N_{off}} V_{Th,test} \end{aligned}. \tag{6.35}$$

Note that this reference voltage is not available in real time. This reference voltage versus the temperature has been plotted in Figure 6.16. The parameter C_2 has been adjusted according to

the measured base-emitter voltage at 320 K. trimming has not been performed in out measurement.

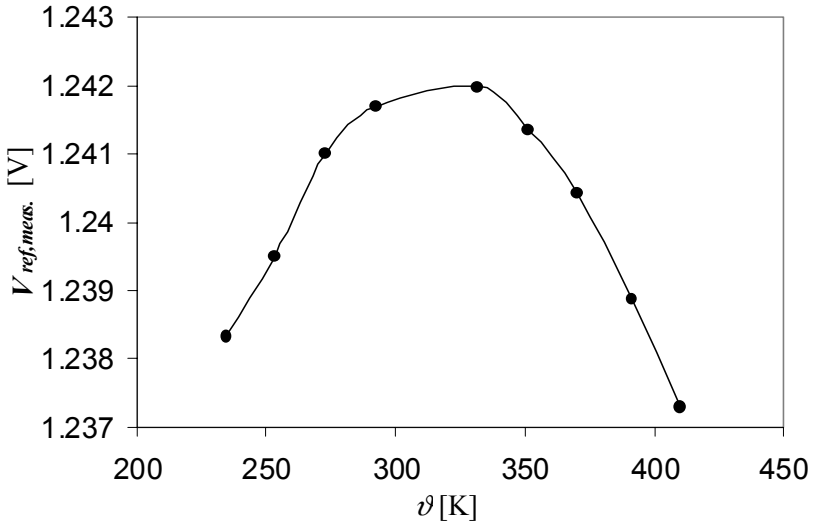

Figure 6.16 The extracted on-chip bandgap-reference voltage, which was found by substituting the measurement results in equation (6.35).

The extracted value of the bandgap reference $V_{\text{ref,meas.}}$ deviates from the design value of 1.263 V. This is partly due to the temperature dependence of the biasing current of bipolar transistors. This can be explained in the following experimental way: the temperature dependence of the output T_{off} includes the temperature dependence of the integration current I_{int}, which is derived from the same current source as the bias current for the bipolar transistors. In this indirect way, we have extracted the temperature dependence of the bias current, which has been plotted in Figure 6.17. It appears that the bias current depends on the temperature with approximately a power of about 0.34 (n = 0.34).

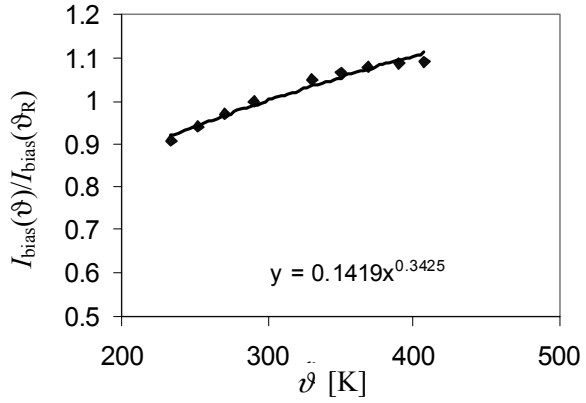

Figure 6.17 The extracted temperature dependence of the bias current for the bipolar transistors.

Taking into account this temperature dependence of the bias current with equation (6.31), it is found that $V_{\text{ref,nom}}$ = 1.253 V. So, the temperature dependence of the bias current does not

completely explain the observed difference between the extracted value of the bandgap-reference voltage and the designed value. Some unknown effects still have to be found.

6.5.5 High-Order Correction for the Bandgap-Reference Voltage

In equation (6.35), only the first-order temperature compensation of the base-emitter voltage is considered. As shown in Figure 6.16, the higher-order non-linearity of the base-emitter voltage causes a parabolic temperature dependence of the bandgap-reference voltage. In the temperature range of -40 °C to 120 °C, this dependence is 5 mV. This will directly affect the accuracy of the thermocouple voltage measurement.

A higher-order temperature compensation of the base-emitter voltage can be achieved by processing the data in a different way. According to (2.16), the higher-order term of the temperature dependence of the base-emitter voltage can be approximated with a Taylor expansion around the ambient temperature ϑ_r, according to the equation

$$V_{BE}(\vartheta) = V_{BE0} - \lambda\vartheta - \frac{1}{2}(\eta - n)\frac{k\vartheta_r}{q}\cdot\frac{(\Delta\vartheta)^2}{\vartheta_r^2}. \tag{6.36}$$

The temperature-dependent bandgap-reference voltage $V_{ref}(\vartheta)$ is thus expressed as

$$\begin{aligned} V_{ref}(\vartheta) &= V_{ref,meas}(\vartheta_r) - \frac{1}{2}(\eta - n)\frac{k\vartheta_r}{q}\cdot\frac{(\Delta\vartheta)^2}{\vartheta_r^2} \\ &= V_{ref,meas}(\vartheta_r) - \alpha(\vartheta - \vartheta_r)^2 \end{aligned}. \tag{6.37}$$

When we use the experimentally derived value of $n = 0.34$ (Figure 6.17), for the value of α it is found that

$$\alpha = \frac{1}{2}(\eta - n)\frac{k}{q\vartheta_r} \approx 5.24\times10^{-7}\ \mathrm{V/K^2}. \tag{6.38}$$

The calculation results from the equations (6.35) and (6.37) is plotted in Figure 6.18. The figure shows that up to the second order, the approximation of the base-emitter voltage by the Taylor expansion will show a good fit with the higher-order temperature dependence of the bandgap-reference voltage.

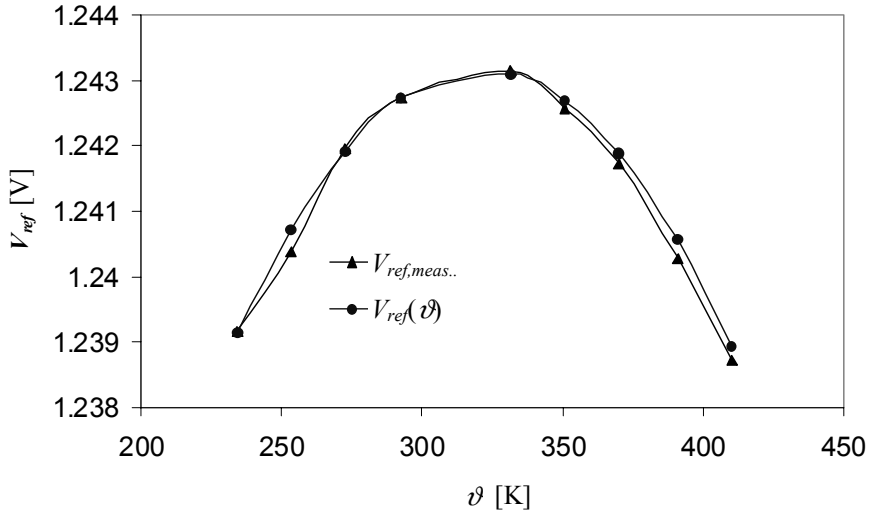

Figure 6.18 Measured result together with the second-order approximation according to (*6.37*) *for the bandgap-reference voltage.*

More samples were tested in order to investigate the spread of the bandgap-reference voltage. Figure 6.19 shows the extracted bandgap-reference voltage of five samples. Since the samples are from the same wafer, the spread is very small.

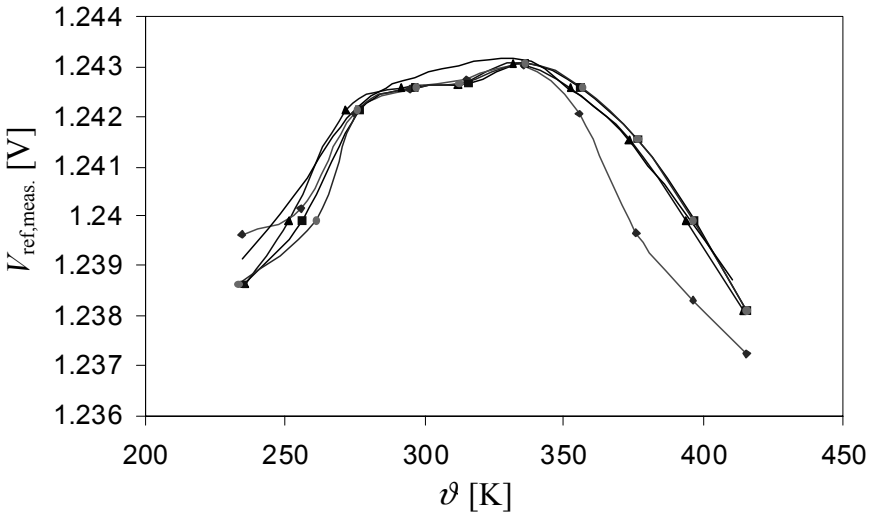

Figure 6.19 Experimental results for the bandgap-reference voltage for five chips.

6.5.6 The Complete System

When an unknown input voltage V_{Th} is to be measured, the measurement result is derived from

$$V_{Th,meas.} = \frac{N_{Th} - N_{off}}{16\left(N_{BE} - N_{off}\right) + C_2\left(N_{\Delta V_{BE}} - N_{off}\right)} \cdot V_{ref}\,, \tag{6.39}$$

where V_{ref} is the bandgap-reference voltage. Both the results of $V_{ref,meas.}(\vartheta_r)$ (ϑ_r = 320 K) in equation (6.35) and $V_{ref}(\vartheta)$ in equation (6.37) have been applied in this equation. We compared the input voltage $V_{Th,meas}$ calculated by (6.39) with the value of the input voltage source $V_{Th,test}$, which was measured using accurate equipment. The difference between the two voltages has been plotted in Figure 6.20. It can be seen that using the temperature-dependent bandgap-reference voltage $V_{ref}(\vartheta)$ improves the accuracy significantly.

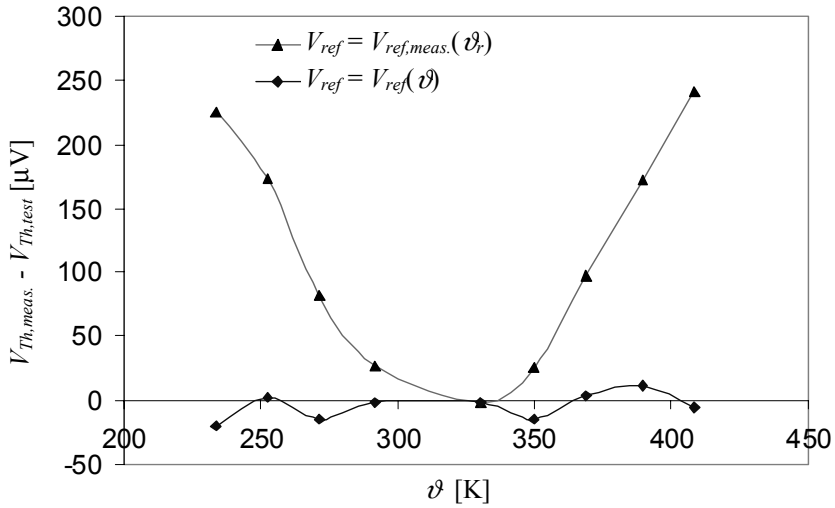

Figure 6.20 The measurement inaccuracy (with V_x=50 mV) with and without taking into account the curvature of V_{ref}.

6.5.7 On-Chip Temperature Sensor

The voltage ΔV_{BE} was found from the measurement results using the equation

$$\Delta V_{BE} = \frac{N_{\Delta V_{BE}} - N_{off}}{16\left(N_{BE} - N_{off}\right) + C_2\left(N_{\Delta V_{BE}} - N_{off}\right)} \cdot V_{ref}\,, \tag{6.40}$$

where V_{ref} is the bandgap-reference voltage. Both the results of $V_{ref,meas.}(\vartheta_r)$ (ϑ_r = 320 K) in equation (6.35) and $V_{ref}(\vartheta)$ in equation (6.37) have been applied in this equation.

The chip temperature can be calculated from equation (6.30). In our design, the current ratio n = 3, so that

$$\vartheta = \frac{\Delta V_{BE}}{\frac{m' k}{q} \ln 3}\,. \tag{6.41}$$

The temperature ϑ, which was calculated using (6.41), was compared with the temperature ϑ_A, which was obtained by measuring the resistance of a platinum resistor Pt100. The difference has been plotted in Figure 6.21.

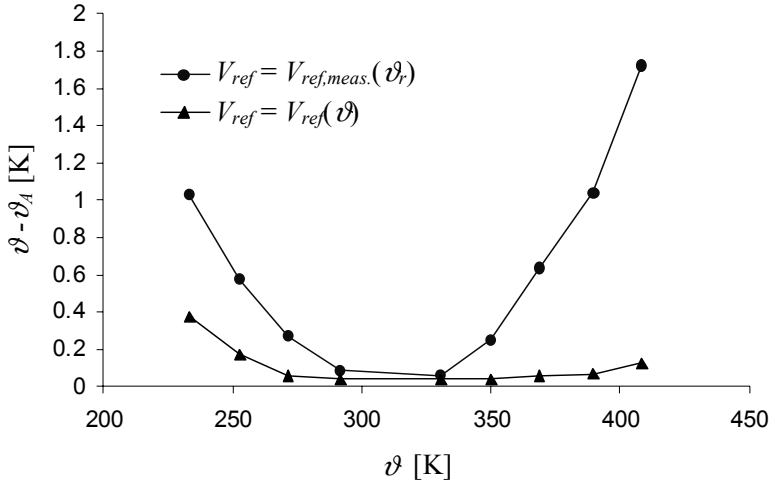

Figure 6.21 The temperature error with and without taking into account the curvature of V_{ref}.

It can be concluded that the temperature difference over the whole temperature range is less than 0.4 K. This is less than the error budget of 0.7 K discussed in section 5.4. The difference (ϑ - ϑ_A) is larger at low temperatures; this is probably due to the simple model *m'* used to describe the effects of the base resistance. As discussed in section 3.4.1, when the transistors are biased with constant currents, the effect of the base resistance is PTAT-like, so it can be modelled by replacing the parameter *m* with *m´*. However, since the real bias current is temperature dependent, see Figure 6.17, the approximation of *m´* deviates from the real one.

6.5.8 The Noise Performance

The calculated values of the input voltage according to (6.39) have been plotted in Figure 6.22 for 100 measurements. The measurements were performed under stable conditions: ϑ = 20°C and with V_x = 0 V. The reason to choose the condition V_x = 0 V is that in this case the input is short-circuited, so the voltage source does not contribute any noise to the total measurement noise. Under these conditions, each measurement takes about 70 ms.

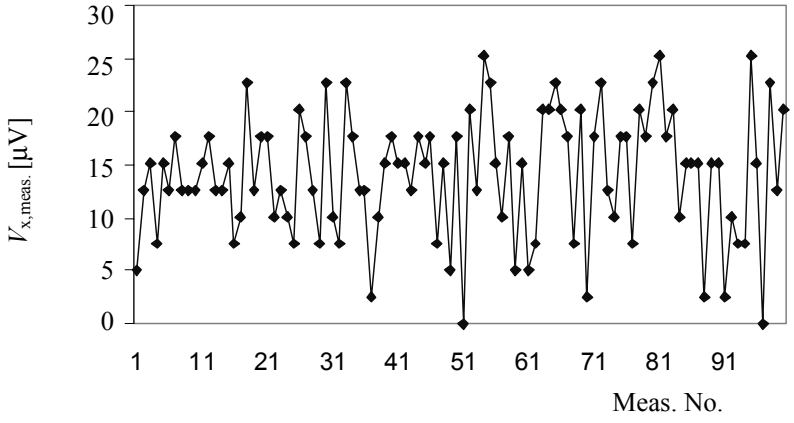

Figure 6.22 The calculated input voltage for 100 measurements.

The measurement noise includes the interface noise and interference, and is represented by the standard deviation σ_v. The experimentally found standard deviation σ_v = 5.9 μV is worse than that calculated in section 6.4, being 3.7 μV. This is probably due to the environmental interference. For a T-type thermocouple (40 μV/K), σ_v = 5.9 μV corresponds to a temperature resolution of 0.15 K.

The fluctuation in the calculated temperature for 100 measurements has been plotted in Figure 6.23. The standard deviation σ_ϑ is 0.02 K. Compared to the effect of the voltage noise, σ_v, the noise in the temperature measurement is much smaller.

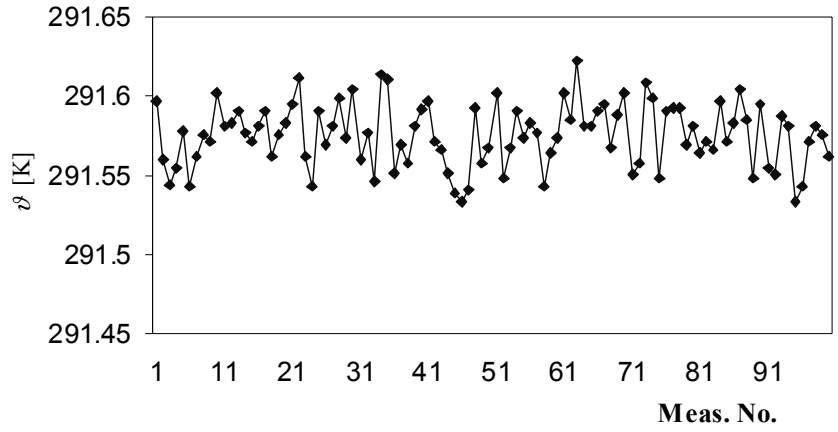

Figure 6.23 The calculated temperature for 100 measurement cycles.

The measurement noise was tested over the temperature range of -20 °C to 140 °C. The results have been listed in Table 6.2.

6.5.9 The Residual Offset

The measurement results of Figure 6.22 also show that there is residual offset, which amounts to about 14 μV. Due to this offset, the calculated output is not equal to zero at zero input. This error cannot be eliminated by applying the three-signal auto-calibration technique.

The reasons causing the residual offset are not yet understood. One of the possible reasons could be that different analog switches were applied to control the signal sampling. The switch-charge injection is different in different measurement phases due to the mismatch in the threshold voltage and the parasitic gate-to-drain capacitance. Another reason could be thermal-electrical effects. Because of the parasitic thermocouples (section 5.2), the temperature gradients will cause an offset voltage at the input.

The measurement offset caused by the residual offset can be reduced by carrying out the voltage measurement in two steps. In the first step, the input is externally short-circuited and the residual offset is stored in the microcontroller memory; in the second step, the voltage is measured, and the unknown input voltage is obtained by subtracting the residual offset from the calculated result. In Figure 6.20 the residual offset has been removed.

6.5.10 Summery of the Performances of the Interface

Table 6.2 shows a list of the main properties and experimental results for the thermocouple interface. A supply voltage of 5 V has been applied for the circuit. The measurement time varied from 70 ms to 100 ms over the temperature range from -40 °C to 140 °C for an input voltage from 0 mV to 100 mV. The reason why at low temperatures the noise is higher is the large external interference when the thermostat is cooling.

Parameters	Value			
Supply voltage	5 V			
Current consumption	300 µA			
Measurement time	70 ms ~ 100 ms			
	-20 °C	20 °C	60 °C	140 °C
Noise (Standard deviation) in voltage measurement σ_v	9.8 µV	5.9 µV	7.6 µV	8.01µV
Voltage inaccuracy ($V_{Th,meas}$ - $V_{Th,test}$) (0 mV ~ 70 mV input)	22 µV	24 µV	24 µV	36 µV
Temperature inaccuracy (ϑ - ϑ_A)	0.37 K	0.04 K	0.04 K	0.13 K

Table 6.2 The interface performances

As a reference the characteristics of the integrated thermocouple interface MAX6675 [6.5] have been listed in Table 6.3 together with some major experimental results of the thermocouple interface presented in this thesis. Both the circuits are referred to K-type thermocouple application.

Parameter	Prototype	MAX6675
Current consumption (V_{DD} = 5 V)	350 µA	700 µA
Temperature error (0 °C to +700 °C)	±1 K	±9 K
Reference-junction compensation error	0.4 K (-20 °C to +140 °C)	±3 K (-20 °C to +85 °C)
Resolution	0.5 K (3σ)	0.25 K
Measurement time	70 ms ~ 100 ms	170 ms

Table 6.3 The interface performances

Considering the accuracy in temperature measurement, the thermocouple interface presented in this chapter performs much better than MAX6675.

6.6 Conclusions

In this chapter we designed an interface circuit for thermocouples. In this design, advanced signal-processing techniques, such as chopping, DEM and three-signal auto calibration are applied. The interface circuit was fabricated in 0.7-µm CMOS technology. The chip size measures 1.9 mm × 1.7 mm. The chip is packaged in a standard 16-pin ceramic DIL package. The interface was tested over the temperature range from -40 °C to 140 °C.

The voltage divider of the interface was analyzed and tested. The relative inaccuracy was found to be less than 85×10^{-6}, which easily meets our requirements. The performance of the on-chip bandgap reference and the on-chip temperature sensor was also analyzed and tested. Taking into account the effects of the base resistance and the effective emission coefficient, we applied a correction factor m' to the voltage ΔV_{BE}. The experimentally found value of m' corresponds to the value derived from the characteristics of the bipolar transistors. The experimentally found bandgap-reference voltage is lower than the nominal one. When the effect of the temperature dependence of the bias current is taken into account, a difference of 10 mV still remains.

The high-order temperature dependency of the measured on-chip bandgap reference is in agreement with that found from the $V_{BE}(\vartheta)$ characteristics described in section 3.3.3. A residual offset of 14 µV in the voltage measurement was found. This error can be removed through data processing. However, this requires external hardware. The inaccuracy in the voltage measurement amounts to 36 µV over the temperature range from -40 °C to 140 °C. The inaccuracy in reference-junction temperature measurement amounts to 0.37 K over the temperature range from -40 °C to 140 °C. The measured standard deviation of the input voltage is 6 µV ~ 8 µV at room temperature but larger at lower temperatures.

Compared to the integrated K-thermocouple interface MAX6675, our circuit performs much better in temperature measurement accuracy.

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Chapter 7 Switched-Capacitor Instrumentation Amplifier with Dynamic-Element-Matching Feedback

7.1 Introduction

In Chapter 4, we presented the principle of a switched-capacitor (SC) instrumentation amplifier with Dynamic-Element-Matching (DEM) feedback [7.1] - [7.3]. This amplifier can be applied in combination with the thermocouple interface to accurately pre-amplify the extremely small thermocouple voltage before this signal is converted into the time domain.

In this chapter, non-idealities such as the systematic inaccuracy and noise will be analysed. The amplifier has been implemented as an integrated circuit. The test results of a prototype will be presented.

7.2 Circuit Design

7.2.1 The DEM SC Instrumentation Amplifier

The schematic diagram of a DEM SC instrumentation amplifier is shown in Figure 7.1. The amplification factor is designed to be 7. For that reason there are eight identical capacitors in this circuit. In each phase of the rotating cycle, one of the eight capacitors is connected to the output as the feedback capacitor. The other seven capacitors are connected in parallel to the input, together forming the sampling capacitor. A complete rotating cycle consists of eight rotating phases. After a complete rotating cycle, each capacitor is connected to the output as a feedback capacitor one time. The average of the amplification factors equals

$$\overline{G} = \frac{1}{8}\sum_{j=1}^{8}\frac{\sum_{i=1}^{8} C_i - C_j}{C_j} \cong 7 + \frac{1}{8}\sum_{j=1}^{8}\delta_j^2 , \tag{7.1}$$

where δ_j is the relative mismatch between the capacitors with respect to the average value $\overline{C}$

$$\delta_j = \frac{C_j - \overline{C}}{\overline{C}}, \tag{7.2}$$

and

$$\overline{C} = \frac{1}{8}\sum_{i=1}^{8} C_i \,. \tag{7.3}$$

The switches S_1 and S_2 control the signal sampling of the input capacitor. The switch S_3 is applied to initialize the output voltage. This is done each time before the charge is transferred to the feedback capacitor. The output voltage is further processed by the voltage-to-period converter, which has been described in Chapter 4 and Chapter 6.

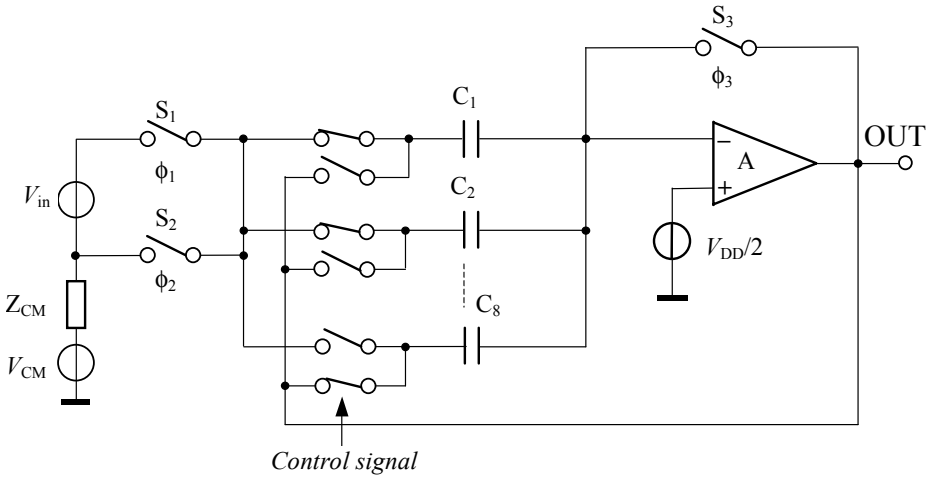

Figure 7.1 The schematic circuit of the DEM SC instrumentation amplifier.

The complementary analog switches can work properly over the whole range of the supply voltage. Thus a rail-to-rail input range of the common-mode voltage can be achieved.

7.2.2 The Complete Circuit

To evaluate the performance of the DEM SC instrumentation amplifier, an interface circuit including the DEM SC instrumentation amplifier has been designed, and its block diagram is shown in Figure 7.2. In this circuit, the input voltage V_{x1} is pre-amplified by the DEM SC instrumentation amplifier. The pre-amplified voltage and the voltages V_{x2}, V_{BE}, ΔV_{BE} and V_{off} are linearly converted to time periods.

The time intervals of the output signal are T_{off}, T_{x1}, T_{off1}, T_{x2}, T_{BE}, and $T_{\Delta VBE}$, and correspond to the input signals V_{off}, V_{x1}, V_{off1}, V_{x2}, V_{BE} and ΔV_{BE} respectively, according to

$$\begin{aligned}
T_{off} &= K \cdot V_{off} + a_0 \\
T_{x1} &= K \cdot G \cdot (V_{x1} + V_{OS}) + a_0 \\
T_{off1} &= K \cdot G \cdot V_{OS} + a_0 \\
T_{x2} &= K \cdot V_{x2} + a_0 \\
T_{BE} &= K \cdot V_{BE} / N_d + a_0 \\
T_{\Delta VBE} &= K \cdot \Delta V_{BE} + a_0
\end{aligned} \,. \tag{7.4}$$

where K represents the transfer parameter of the voltage-to-period converter, a_0 represents the offset of the voltage-to-period converter and V_{OS} the offset of the DEM SC amplifier.

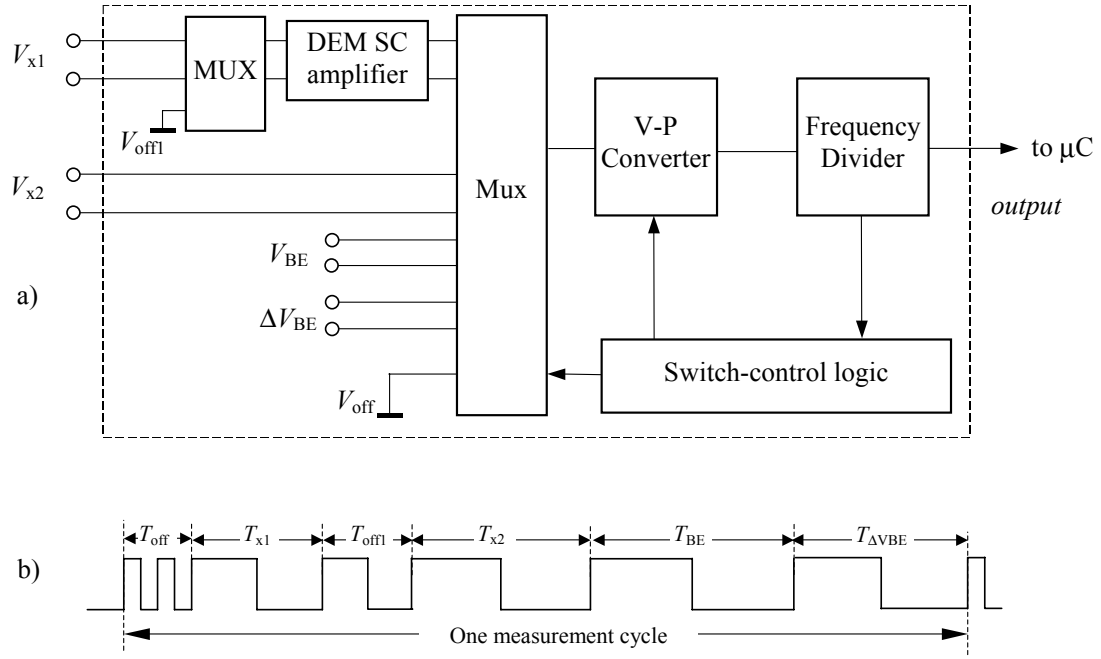

Figure 7.2 a) The block diagram of an interface system in which the DEM SC amplifier with gain G has been applied and b) the output signal.

7.3 Non-Idealities of the DEM SC Amplifier

The non-idealities of the DEM SC instrumentation amplifier are mainly due to

- *finite open-loop gain,*
- *leakage current at the input of op-amp at high temperatures,*
- *switch-charge injection,*
- *noise.*

7.3.1 Finite Open-Loop Gain

The limited DC open-loop gain of the op-amp causes inaccuracy of the instrumentation amplifier. The relative error δ due to the limited open-loop gain is given by

$$\delta \approx \frac{G}{A_0}, \tag{7.5}$$

where A_0 is the DC open-loop gain of the op-amp and G is the amplification factor of the DEM SC amplifier. For example, with $G = 7$ and $A_0 = 100$ dB, the inaccuracy is 7×10^{-5}.

This error cannot be cancelled by the three-signal method, because the instrumentation amplifier is not applied during all measurement phases. Therefore, in order to keep this inaccuracy low, an op-amp with a high open-loop gain must be used.

7.3.2 Leakage Current at the Inverting Input of the Op-amp

The leakage current I_k at the inverting input of the op-amp will cause charge loss, which will result in a voltage error at the output, as shown in Figure 7.3(b). The amount of charge loss depends on the leakage current and the time interval T. The voltage error at the end of T is

$$\delta V = \frac{\Delta Q}{C_2} = \frac{I_k T}{C_2}. \tag{7.6}$$

The leakage current is mainly due to the junction leakage of the switch S_3 and the parasitic diode at this node. In order to reduce the voltage dependency of the capacitance, we used two identical capacitors for each of the sampling capacitors C_i connected in anti-parallel. In this case, for a poly/oxide/n-well capacitor, a parasitic diode exists at each side of the capacitor. When the temperature rises, the leakage current increases. At a certain high temperature, the error due to the leakage current cannot be neglected anymore. Fortunately, by applying chopping we can reduce this error. The chopping technique can be realized by arranging the control signals for the switches S_1, S_2 and S_3, as shown in Figure 7.4(a), (b) and (c). The output signal of the instrumentation amplifier V_{out} and the corresponding output V_{o_int} of the integrator in the voltage-to-period converter are shown in Figure 7.4(d) and (e). When the leakage current is constant, the effect of the leakage current for a negative output signal is opposite to that for a positive output signal. Therefore, the total time interval of a complete chopping cycle will not depend on the leakage current.

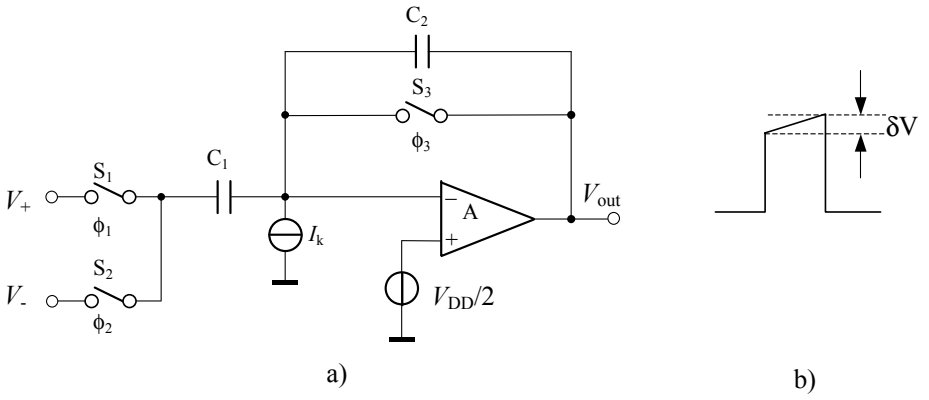

Figure 7.3 The effect of an input leakage current I_K: a) circuit diagram, b) output voltage V_{out} versus time.

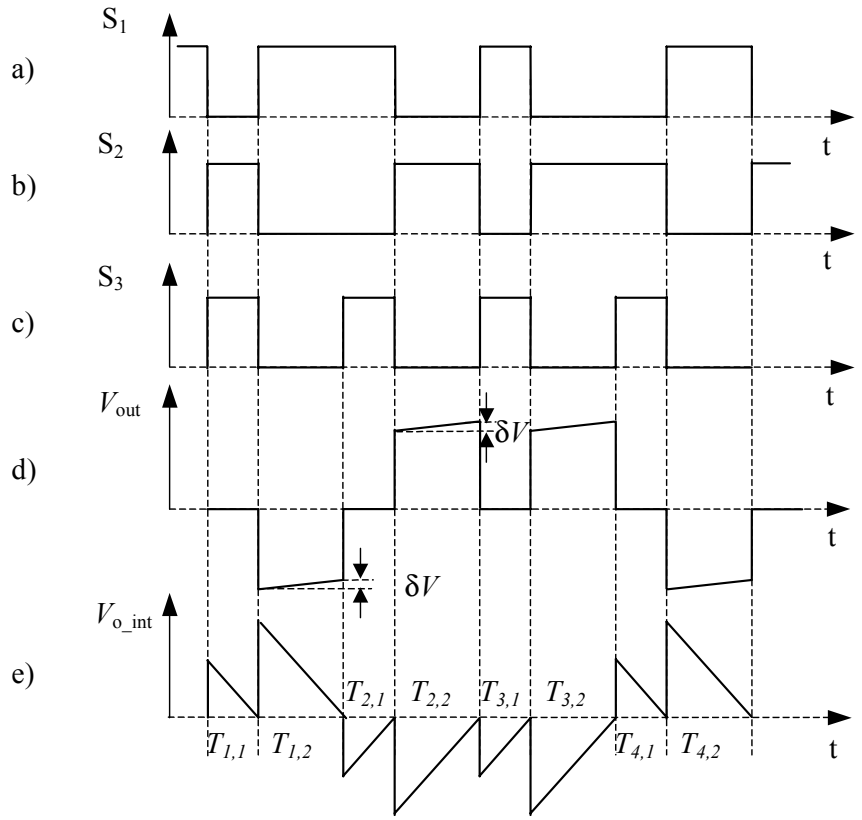

Figure 7.4 The control and output signals of the SC instrumentation amplifier, and the output of the integrator in the voltage-to-period converter.

When the chopping frequency f_{chop} is selected high enough, also low-frequency interference and 1/*f* noise will be reduced significantly. In our design, we have chosen f_{chop} = 12.5 kHz.

7.3.3 Switch-Charge Injection

The effect of switch-charge injection can be explained using Figure 7.5.

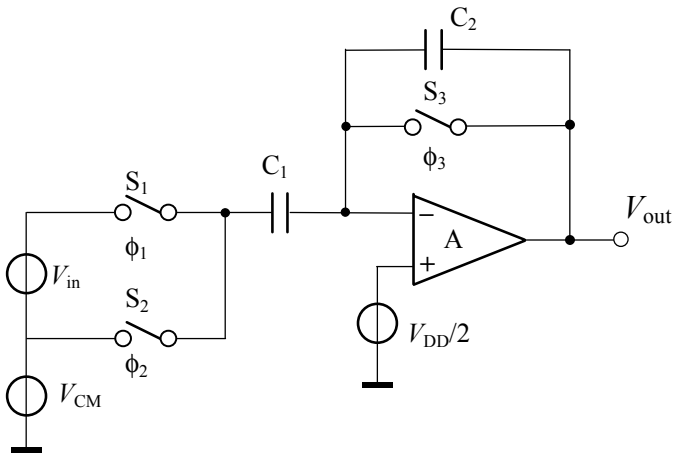

Figure 7.5 The switch-charge injection of S_1 and S_2 will cause an error.

Because the chopping technique has been applied in this circuit, the situations of switches S_1 and S_2 are arranged as following: Firstly, switch S_1 is switched off from the ON state and then S_2 is switched on from the OFF state; an amount of charge C_1V_{in} is transferred to the feedback capacitor C_2. Secondly, switch S_2 is switched off from the ON state and then S_1 is switched on from the OFF state, and an amount of charge $-C_1V_{in}$ is transferred to the feedback capacitor C_2. In the first situation, due to switch-charge injection, an extra amount of charge q_{S1} (see equation 4.36) is added to C_1V_{in}. Similarly, in the second situation, an extra amount of charge q_{S2} is added to $-C_1V_{in}$. The total equivalent input error due to switch-charge injection is

$$\delta V_{SCI} = \frac{q_{S1} - q_{S2}}{2C_1}. \tag{7.7}$$

For example, C_1 = 14 pF, W =10 µm, L = 0.7 µm, $C_{OX0} = 2\times10^{-3}$ F/m^2, μC_{OX0} = 2900 µA/V^2, $C_{GD0} = 3.1\times10^{-10}$ F/m, V_T = 0.75 V, V_H = 5 V, V_L = 0 and the delay time from high to low of S_3 is 0.3 ns, we have C_{OX} = 0.014 pF, C_{GD} = 0.003 pF, $\beta = 4\times10^4$ µA/V^2 and $U = 1.67\times10^{10}$ V/s. For V_{CM} = 0 V, 2.5 V and 5 V, $\frac{\beta V_{HT}^2}{2C_S}$ amounts to 2.6×10^{10} V/s, 4.3×10^9 V/s and 8.0×10^8 V/s, respectively. Thus, $\frac{\beta V_{HT}^2}{2C_S} >> U$ for V_{CM} = 0 and $\frac{\beta V_{HT}^2}{2C_S} << U$ for V_{CM} = 2.5 V and 5 V. According to (4.36), for V_{CM} = 0 V it holds

$$\delta V_{SCI} = -\frac{C_{GD}}{2C_1}V_{in}, \tag{7.8}$$

while for V_{CM} = 2.5 V and 5 V

$$\delta V_{SCI} \approx \frac{C_{OX}V_{HT}^2V_{in}}{12UC_1^2}. \tag{7.9}$$

for V_{CM} = 2.5 V and 5 V.

The relative error due to switch charge injection amounts to:

1.1×10^{-4} for V_{CM} = 0,
1.1×10^{-3} for V_{CM} = 2.5 V and
2.0×10^{-4} for V_{CM} = 5 V.

Thus, it is suggested that, when possible, the floating input is connected to ground.

From equations (7.8) and (7.9), we can conclude that in order to reduce the error caused by switch-charge injection, we should choose the switch size as small as possible. However, this will cause a large on-resistance. Therefore, there is a trade-off between these two effects. As mentioned in section 4.6.1, we can reduce the error by using a complementary pair of CMOS switches.

7.3.4 Noise of the DEM SC Amplifier

The main noise sources are the noise voltage of the op-amp and the thermal noise kT/C. We will discuss the effects of these two noise sources.

The Noise Voltage of the Op-amp

A noise model of the DEM SC amplifier is shown in Figure 7.6(a); it is equivalent to that of Figure 7.6(b).

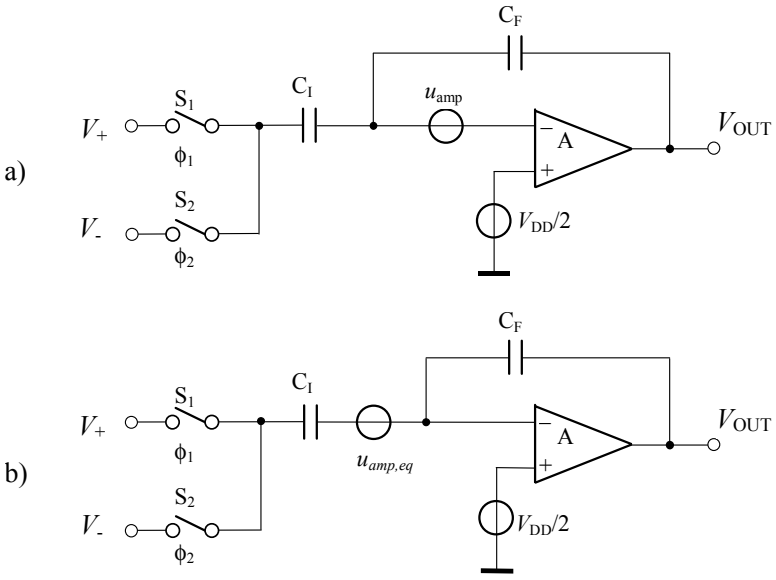

Figure 7.6 (a) The noise voltage of the amplifier and (b) equivalent circuit.

For the equivalent circuit in Figure 7.6(b), it holds that

$$u_{amp,eq} \approx u_{amp}\left(1+\frac{C_F}{C_I}\right). \tag{7.10}$$

When we only consider the white noise, for a noise source with a power spectral density S_{u_amp}, the noise voltage amounts to

$$u_{amp}^2 \approx \int_0^{B_{amp}} S_{u\_amp}(f)\mathrm{d}f = S_{u\_amp}B_{amp}, \tag{7.11}$$

where B_{amp} is the bandwidth of the op-amp. Since the chopping technique has been applied, the effect of the $1/f$ noise can be neglected. The equivalent input noise voltage is then

$$u_{amp,eq}^2 \approx 2\left(1+\frac{C_F}{C_I}\right)^2 S_{u\_amp}B_{amp}. \tag{7.12}$$

The factor of 2 is due to the fact that the noise voltage is sampled twice each time the input voltage is sampled. After 4N times averaging in the frequency divider, the equivalent input noise voltage due to the noise voltage of the amplifier is

$$u_{amp,eq,4N} = \sqrt{\frac{u_{amp,eq}^2}{4N}} = \left(1+\frac{C_F}{C_I}\right)\sqrt{\frac{S_{u\_amp}B_{amp}}{2N}}. \tag{7.13}$$

For example, in our practical design with: C_I = 14 pF, C_F = 2 pF, B_{amp} = 25 MHz, S_{u_amp} = 1.4×10^{-16} V^2/Hz (12 nV/√Hz) and N = 256, the equivalent input noise voltage due to the noise of the op-amp is 3.0 μV.

The Thermal Noise of $k\vartheta/C$

The thermal noise of the ON-resistance of the switch results in $k\vartheta/C$ noise. In order to simplify the calculation, we assumed that the eight capacitors C_1 … C_8 (Figure 7.1) have an equal value C_i. Each sampling step, the noise charge in one sampling step is given by

$$q_n^2 = 2k\vartheta(7C_i)\,. \tag{7.14}$$

The equivalent noise voltage is

$$v_{SC} = \frac{q_n}{7C_i} = \sqrt{\frac{2k\vartheta}{7C_i}}\,. \tag{7.15}$$

For the 4N-time average, the equivalent noise voltage is

$$v_{SC,eq} = \sqrt{\frac{2k\vartheta}{7C_i(4N)}}\,. \tag{7.16}$$

For example, in our practical design, with C_i = 2 pF and N = 256, with equation (7.16), we find that the noise voltage $v_{sc,eq}$ = 0.76 μV. Taking into account all the noise sources, we obtain a total equivalent input noise voltage of 3.1 μV.

7.4 Experimental Results

A prototype of the interface circuit including the DEM SC instrumentation amplifier was fabricated in 0.7-μm CMOS technology of Alcatel Microelectronics. The photograph of the chip is shown in Figure 7.7. The chip was packaged and tested.

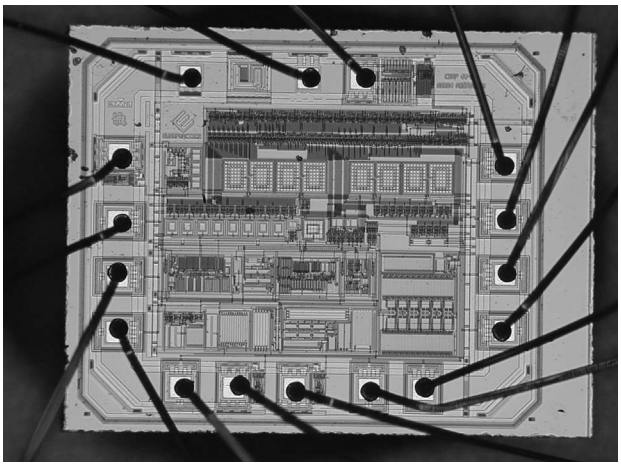

Figure 7.7 The chip photograph of the DEM amplifier.

For the amplifier, an OTA was applied with the following specifications (Table 7.1).

Supply current	530 μA
g_m	1.3mA/V
White noise	12 nV/√Hz
Bandwidth	25 MHz

Table 7. 1 The specifications of the OTA used in the DEM SC instrumentation amplifier.

In order to test the accuracy of the DEM SC instrumentation amplifier, we applied an external voltage source V_x to both the inputs V_{x1} and V_{x2}, as shown in Figure 7.8.

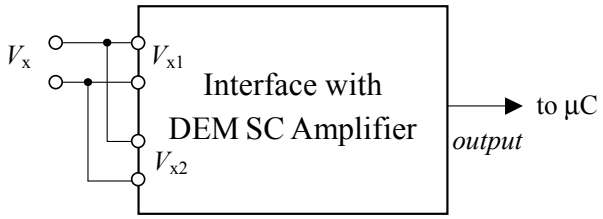

Figure 7.8 The test set-up for DEM SC instrumentation amplifier.

According to equation (7.4), the amplification factor G can be derived by

$$G = \frac{T_{x1} - T_{off1}}{T_{x2} - T_{off}}. \tag{7.17}$$

The measurements were performed at room temperature with supply voltage of 5 V. The derived amplification factor for 100 measurements is plotted in Figure 7.9, where each measurement takes 68 ms. The corresponding input voltage $V_{x,meas.}$ is also shown in this figure. With a series of such experiments it has been found that the fluctuations shown in Figure 7.9 are due to random additive noise.

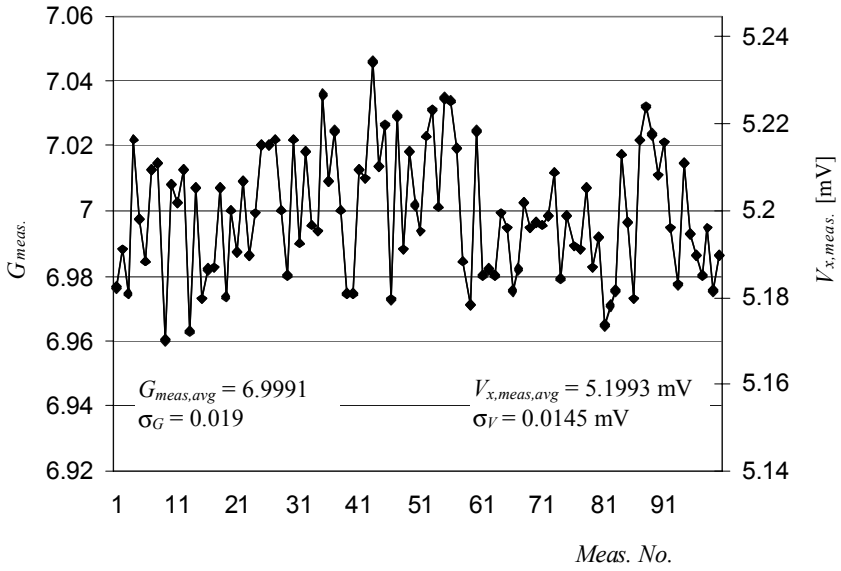

Figure 7.9 The derived amplification factor G at room temperature (V_x = 5.2 mV).

The fluctuations, on the other hand, are quite large. The standard deviation σ_v of the derived input voltage amounts to 14.5 μV, which is about 5 times larger than calculated results in section 7.3. For T-type of thermocouple this noise corresponds to an error of 0.4 K. This error can easily be reduced by enlarging the measurement time.

The average of the amplification factor (G = 6.9991) is rather accurate. The relative inaccuracy amounts to 1.3×10^{-4}. With an error budget of 0.2% (see section 5.4), this easily meets the requirement of the thermocouple voltage measurement.

Table 7.2 lists the time intervals and their standard deviations of the time periods T_{x1}, T_{off1}, T_{x2} and T_{off}. It is shown that the standard deviations of T_{x1} and T_{off1} are much larger than those of T_{x2} and T_{off}. This means that the noises in the amplifier are dominant.

Parameters	Values (ms)	σ (s)
T_{x1}	19	3.0×10^{-6}
T_{off1}	16	2.9×10^{-6}
T_{x2}	17	4.9×10^{-7}
T_{off}	16	4.9×10^{-7}

Table 7.2 The standard deviation of the output signal.

We did not find the reason for this large noise.

7.5 Conclusion

A switched-capacitor instrumentation amplifier with dynamic element matching for the feedback network was designed and fabricated in CMOS technology. By rotating the capacitors in the feedback position successively, the average gain error due to the element mismatching was reduced to the second order.

Limited open-loop gain of op-amp causes error of amplification factor; using high-gain op-amp can reduce this error. Another error source is the switch-charge injection. In order to reduce this error, it is suggested that, if possible, the floating input is connected to ground. Furthermore, using a complementary pair of CMOS switches can also partly reduce this error.

The DEM SC instrumentation amplifier was then tested at room temperature. The extracted amplification factor proved quite accurate. However, the measured equivalent input noise voltage is 5 times larger than the calculated one. The reason for this large noise could not be determined.

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Chapter 8 Conclusions

In integrated bandgap references and temperature sensors, the $I_C(V_{BE},\vartheta)$ characteristics of bipolar transistors are used to generate the basic signals with high accuracy. To investigate the possibilities to fabricate high-precision bandgap references and temperature sensors in low-cost CMOS technology, the electrical characteristics of substrate bipolar pnp transistors have been investigated over a wide temperature range.

Characteristics: The measurement results of the $I_C(V_{BE},\vartheta)$ characteristics show that at a moderate current range, a good exponential relation between the base-emitter voltage and the collector current exists. Moreover, the temperature behavior of the base-emitter voltage can be well modelled with the well-known Gummel-Poon model. Even the negative correlation between the extracted parameters V_{go} and η is similar to that earlier reported for bipolar technology.

Compared to bipolar transistors fabricated in bipolar technology, bipolar transistors fabricated in CMOS technology show a much lower forward common-emitter current gain (B_F). This is mainly due to the fact that the base thickness of a pnp vertical bipolar transistor, which is the distance between the bottom of a p+ region and the bottom of the n-well, is much larger than that of bipolar transistors fabricated in bipolar technology. This also explains why vertical bipolar transistors fabricated in CMOS technology have a much larger forward early voltage. For instance, the pnp substrate transistors fabricated in 0.7-µm CMOS technology of ALCATEL Microelectronics have an early voltage of 370 V. The experimental results show that, at a moderate current range, B_F is almost current independent.

Because of the low doping of the n-well ($4\times10^{16}/cm^3$), the base resistance R_B of the bipolar transistors fabricated in CMOS technology is higher than that of bipolar transistors fabricated in bipolar technology. The effort to extract the value of the base resistance from the measurement results provided to a new method for measuring the base resistance. Compared to the existing methods for measuring the base resistance, the new method is much more suitable to be used for temperature sensors and bandgap references.

The measurement results show that the effective emission coefficient m at moderate current levels is quite close to the ideal value of unity. At high current levels, the value of effective emission coefficient m deviates from 1 to 2, which is due to the high-level-injection effect.

At high current levels, the voltage drop I_BR_B significantly affects the voltage ΔV_{BE}. In order to reduce this effect, a low bias current and a multi-emitter structure should be applied. However, when the bias current is minimized, the low-level injection effect has to be taken into account, because for very low bias currents, ΔV_{BE} deviates from the simple logarithmic expression.

Since the collectors of the substrate vertical bipolar transistors are all connected to ground, they can only be biased via the emitter currents. Therefore, the voltages V_{BE} and ΔV_{BE} are affected by the low value of the forward common-emitter current gain (B_F). The temperature dependence of the forward common-emitter current gain could cause errors. By circuit design, this effect on V_{BE} can be compensated at the cost of an increased supply voltage. Fortunately, at a moderate current range, B_F is almost current independent. Therefore, the emitter-current ratio equals the collector-current ratio. Thus the voltage ΔV_{BE} can be controlled accurately by controlling the emitter-current ratio, which is much easier than controlling the collector-current ratio.

In the temperature sensors, self-heating will cause an additional error. Using a package with good thermal conductance and minimizing the average power dissipation will reduce this error. It is important to minimize the temperature differences between the transistors used to generate the ΔV_{BE} voltage. This can be achieved by placing these transistors as close as possible to each other in a cross-quad configuration, and far away from the power-dissipating components.

The accuracy of temperature sensors and bandgap references is also affected by mechanical stress. This is due to the so-called piezo-junction effect, where, as an effect of mechanical stress, the base-emitter voltage deviates from the ideal value under zero stress. Compared to npn transistors, pnp transistors are less stress-sensitive. Due to the favorable crystal orientation, the vertical pnp substrate transistors in {001} wafers show only a very low piezo-junction effect. Tensile stress changes the base-emitter voltage less than compressive stress. Our experimental results showed that the ΔV_{BE} voltage is immune to mechanical stress. To minimize stress-induced effects in bandgap references and temperature sensors we used a substrate pnp vertical transistor to generate the base-emitter voltage and a packaging technique that only causes stress in the tensile range.

Circuits: In order to design high-performance temperature sensors or bandgap references in CMOS technology, in addition to exploiting the best characteristics of the bipolar transistors, we needed to apply advanced circuit techniques. In this thesis, special advanced circuit techniques for application in low-speed sensor systems have been described. The application of these techniques requires a memory function and a counting function, implemented in, for instance, a microcontroller or microprocessor. Firstly, the basic voltages are processed. Next, the temperature-sensing signal and the bandgap-reference signal are derived from the data processed by the microcontroller. Compared to the traditional CMOS analog circuits and systems, the “embedded” analog/digital systems have the advantage that they can eliminate most systematic errors and most low-frequency noise. For accurate measurements, the three-signal auto-calibration technique can be applied to eliminate the additive and multiplicative uncertainties and errors of the interface circuit. To realize the three-signal technique, two extra signals: a reference signal and an offset signal have to be measured in exactly the same linear way as the signal to be measured. This technique can easily be implemented in a microcontroller-based measurement system.

In the described sensor systems, indirect A/D converters (modulators) have been applied, because of their simplicity, high accuracy and high resolution. The features of different modulators, frequency modulators, period modulators and duty-cycle modulators were compared. A period modulator is very suitable for use in low-speed sensor systems. The linearity of its voltage-to-period conversion makes it easy to apply the three-signal auto calibration technique. However, since its simplicity, accuracy and the easy way in which the

advanced circuit can be applied, the charge-balance period modulator was found most suitable for the described sensor interfaces.

To reduce the effects of low-frequency interference and 1/*f* noise, a chopping technique was applied. Due to clock feedthrough, there is some residual offset. By applying the so-called auto-calibration or nested-chopper technique, this residual offset was reduced significantly. There exists only a limited range over which modulators, such as voltage-to-period converters can process voltage signals with sufficient linearity. To increase this range, it is necessary to pre-amplify the small voltage signals and/or to divide the large voltage signals before these signals are processed. Since the required amplifiers and dividers are out of the three-signal auto-calibration chain, their absolute accuracy should be very high. Such amplifiers and dividers can be obtained using the DEM technique. In this way the errors due to component mismatching can be significantly reduced.

A novel capacitive voltage divider with DEM has been presented. Compared to R-C (resistive-capacitive) dividers, this capacitive divider has the advantage that the effect of the resistance of the input voltage source is much less. In case of the capacitive divider, the sampling capacitor C_S is split up into smaller ones, which only slightly increases the chip area. Compared to an R-C divider, the required chip area is much smaller. However, a possible problem could occur due to overload of the integrator amplifier at the moment that charge is transferred from the sampling capacitor to the integrator capacitor. Fortunately, when a MOSFET op-amp is applied, there is no path for charge loss. Thus, overload will not cause an error in the voltage-to-period conversion.

Also a novel switched-capacitor instrumentation amplifier with DEM feedback that accurately pre-amplifies the small voltage signals has been presented. By applying dynamic element matching, the inaccuracy due to component mismatching was reduced to second order. A major advantage of the switched-capacitor configuration is that a rail-to-rail input range for the common-mode voltage can be allowed.

Remaining non-linearity and noise: Non-linearity limits the accuracy of a V-P modulator applying the three-signal auto-calibration technique. This non-linearity is mainly caused by the low- and high-frequency poles of the integrator, the voltage dependence of the sampling capacitors, and the non-linear delay time of the comparator. By careful circuit design, the effects of the low- and high-frequency poles of the integrator can be minimized. When two identical sampling capacitors are anti-parallel connected, only second-order voltage dependence of the sampling capacitor contributes to the non-linearity. Even so, the main cause of non-linearity is the voltage dependence of the sampling capacitor.

Noise limits the measurement resolution. Increasing the number of sampling periods will improve the voltage resolution. However, this also reduces the measurement speed: there is a trade-off between the voltage resolution and the measurement speed. In case of fast measurement, quantization noise will predominate the system noise. To reduce the quantization noise, microcontrollers or counters with a higher clock frequency have to be applied.

A thermocouple measurement system: As a case study, an integrated interface circuit for thermocouples was designed. In this design, bipolar transistors in CMOS technology as well as advanced circuit techniques were applied. In order to get an accurate measurement system, not only the electronic problems also the thermal problem was taken into account.

In order to measure the object temperature, the thermocouple voltage and the reference-junction temperature should be measured.

Regarding to the thermal design aspects, it is recommended to take care that: (1) the temperatures of the two reference junctions of the thermocouple mounted to the system are equal, and (2) that the temperatures of the two inputs of the interface chip are equal.

In order to reduce the cost and to simplify the measurement system, an on-chip temperature sensor was used. Therefore, the interface circuit had been designed such that it measures both the thermocouple voltage and its own temperature. Therefore, the chip temperature should be equal to the reference-junction temperature. Due to self-heating, there is a difference between these two temperatures, which results in a measurement error. By minimizing the power consumption of the interface and assembling the interface circuit in good thermal contact with the thermal conductive medium, the measurement error due to self-heating can be minimized.

A circuit design for the thermocouple interface has been presented. A switch-capacitor input circuit has been applied which allows the thermocouple voltage to have a rail-to-rail common-mode voltage. Furthermore, advanced circuit techniques such as three-signal auto-calibration, DEM and chopping have been applied too.

Realization: The interface circuit has been designed and implemented in 0.7-µm CMOS technology. The chip measures 3.23 mm^2 and is assembled in a standard 10-pin TO-5 package. The interface has been tested over the temperature range from -40 °C to 140 °C. Experimental results show that the internal voltage divider of the interface has a relative inaccuracy of less than 85×10^{-6}. The total inaccuracy in the voltage measurement was 36 µV over the temperature range from -40 °C to 140 °C for an input range from 0 to 70 mV. This is mainly due to the inaccuracy of the on-chip bandgap-reference voltage. The inaccuracy in the internal temperature measurement is 0.4 °C over the temperature range from -40 °C to 140 °C. This is mainly due to the inaccuracy of the on-chip bandgap-reference voltage and the inaccuracy of the on-chip temperature sensor. At room temperature, the voltage resolution is 7.6 µV. This value increases slightly with temperature. For a T-type thermocouple, this values correspond to a total inaccuracy from 1.0 K to 1.4 K over the temperature range from -40 °C to 350 °C, and a temperature resolution of 0.2 K.

DEM SC instrumentation amplifier: To improve the resolution of the measurement of the thermocouple voltages, it would be a good idea to pre-amplify the small thermocouple voltage. The SC DEM instrumentation amplifier is very suitable for this purpose, especially because it can handle large common-mode signals, which allows the user to choice between using grounded or floating thermocouples.

A DEM SC instrumentation amplifier has been described and implemented in 0.7-µm CMOS technology. It has been tested at room temperature. The extracted relative inaccuracy is less than 1.3×10^{-4}, which is suitable for the described application. However, the noise performance is not as predicted. The measured input noise voltage is almost 5 times worse than that calculated and amounts to 14.5 µV, which corresponds to an error of 0.4 K for a T-type thermocouple. The reason for this large noise was not found. For this reason, this amplifier was not used for the thermocouple interface circuit.

Summary

Chapter 1:

This chapter is an introduction. Firstly, it explains why it is necessary to investigate the characteristics of bipolar transistors fabricated in CMOS technology. Secondly, it presents the problems in designing an integrated temperature sensor or a bandgap reference, together with some possible solutions. Thirdly an outline of the research work is presented.

Chapter 2:

In this chapter the temperature characteristics of bipolar transistors are reviewed. Based on the knowledge about these temperature characteristics, a temperature sensor and bandgap reference can be designed. Also two possible structures, lateral and vertical bipolar transistors in CMOS technology, are presented in this chapter. A comparison of these two structures shows that the vertical parasitic substrate bipolar transistors are to be preferred for designing high-performance temperature sensors and bandgap references.

Chapter 3:

In this chapter the DC characterization of substrate bipolar transistors fabricated in CMOS are presented together with the experimental results. For testing purposes, such bipolar transistors were fabricated and packaged. For the device characterization, set-ups were designed and implemented. Measurements of the voltages V_{BE} and ΔV_{BE} versus the temperature and the bias current have been performed.

From the measurement results of $I_C(V_{BE}, \vartheta)$, it is concluded that at moderate current range, a good exponential relation between the base-emitter voltage and the collector current exists. It appears that the temperature behavior of the base-emitter voltage can be well modelled with the well-known Gummel-Poon model. The negative correlation between the extracted parameters V_{go} and η is similar to that reported earlier for bipolar technology.

The forward common-emitter current gain B_F is also derived over a wide range of bias currents and temperatures. Compared to the value of B_F of transistors fabricated in bipolar technology, the value of B_F of substrate bipolar transistors in CMOS technology is much lower. Due to the large base width, the larger Gummel number results in a lower forward common-emitter current gain.

A new method to extract the base-resistance is presented. The base resistance is extracted from the measurements of the voltage ΔV_{BE}, the emitter current and the emitter current ratio

I_{e2}/I_{e1}. Compared to the existing methods for measuring the base resistance, the new method is much more suitable for application of temperature sensors and bandgap references, because the base resistance is derived at the working status. The measurement results show that the value of the base resistance can exceed 1000 Ω at high temperatures. Also it is shown that for the same emitter size, the transistor fabricated in 0.5-μm CMOS has lower base resistance than that fabricated in 0.7-μm CMOS. This is mainly due to the heavier doping in 0.5-μm CMOS. The base resistance causes an undesired voltage drop, which increases the external base-emitter voltage V_{BE} and ΔV_{BE} voltage. This voltage drop can be reduced by selecting a low biasing current, or by using a multi-emitter structure. There is a trade-off between the biasing emitter current and the low injection effect.

The effective emission coefficient m is extracted in two ways: from the measured $I_C(V_{BE})$ curve, and from the measurements on ΔV_{BE}. The results showed good agreement. The results show that the effective emission coefficient m of the devices in CMOS technology is very close to the ideal value of unity. For high-precision applications, even a small deviation from unity has to be taken into account.

It is found that at a moderate current range, the forward common-emitter current gain is insensitive to the biasing-current level. For circuit design this means that the collector-current ratio can be controlled as accurately as the emitter-current ratio. So the voltage ΔV_{BE} can be generated accurately by controlling the emitter current ratio.

The package-induced stress, which is environment dependent, causes the base-emitter voltage to deviate from the value under zero stress. This piezo-junction effect causes errors both in temperature sensors and bandgap references. Experimental results show that the pnp vertical transistors are less stress sensitive than npn transistors. For pnp vertical transistors, tensile stress changes the base-emitter voltages less than compressive stress. Experimental results also show that the ΔV_{BE} voltage is insensitive to mechanical stress. Therefore, we use the substrate pnp vertical transistor to generate the base-emitter voltage, and to make sure that the packaging is done in such a way that the package-induced stress is in the tensile range only.

Chapter 4

In this chapter, advanced circuits that are to be applied in smart temperature sensors and dynamic bandgap references are presented. In smart sensor systems, high precision can be obtained by applying the three-signal auto-calibration method. The application of this method eliminates the effects of the uncertainties in the additive and multiplicative parameters of the measurement circuit. Usually in such a smart sensor system, a microcontroller is applied to read and process the data from the signal-processing circuit. Therefore, it is required that the signal-processing circuit generates output readable by a microcontroller. Based on considerations with respect to the accuracy, the resolution and the conversion speed, the indirect A/D converters are found to be very suitable.

The main part of indirect A/D converters consists of a modulator, which converts voltage signals into the time domain. The microcontroller digitises the modulated signals. The types of modulators described in this chapter are the frequency modulator, the period modulator and the duty-cycle modulator. Of these modulators, the period modulator is most suitable for a smart sensor system. Of the period modulators, the modified Martin oscillator is found to be

very suitable for voltage-to-period conversion due to its simplicity, accuracy and the easy way in which advanced circuit techniques can be applied.

To reduce the effects of low-frequency interference, offset and $1/f$ noise of the CMOS amplifiers, the chopping technique was applied. Due to the effect of clock feedthrough, a residual offset exists. This residual offset can either be reduced by applying the nested-chopper technique or by auto-calibration. However, the auto-calibration is applied anyway to eliminate the effects of the additive uncertainty and multiplicative parameters: so it is not necessary to apply the nested-chopper technique in our circuits.

Dynamic-Element-Matching (DEM) technique plays an important role in our circuit design to eliminate the systematic errors caused by mismatching. This technique is very suitable for applications in pre-amplifiers and dividers that cannot be auto-calibrated. With the application of DEM, accurate amplification of the small voltage signals and attenuation of the large voltage signals can be realised. Also an accurate voltage signal ΔV_{BE}, which is required in designing the temperature sensors and the bandgap references, can be generated using the DEM technique.

When a system is linear, three-signal auto-calibration can eliminate the effects of most of the systematic errors. However, non-linearity will limit the systematic measurement accuracy. The non-linearity can be caused by, for instance, the low- and high-frequency poles of the integrator, the voltage dependence of the sampling capacitors, and the non-linear delay time of the comparator. By careful design of the circuit, the effects due to the low- and high-frequency poles of the integrator can be minimized. When two identical sampling capacitors are anti-parallel connected, only the effect of the second-order voltage dependence of the sampling capacitor will remain. For further improvement, it is recommended to take care that the input-voltage signals have the same common-mode levels.

Noise and interference determine the measurement resolution. The measurement resolution can be improved by increasing the number of sampling periods. However, this reduces the measurement speed, as there is a trade-off between the voltage resolution and the measurement speed. To reduce the quantization noise, a microcontroller with a higher clock frequency should be used.

Chapter 5:

As a case study for the research work presented in chapter 3 and chapter 4, a thermocouple interface system was designed. In this chapter, the architecture considerations for this system are presented. These considerations concern both the thermal domain and the electrical domain.

In the thermocouple system, two signals have to be measured: the thermocouple voltage and the reference-junction temperature. From these two measurements, the object temperature can be derived. For an accurate measurement of the thermocouple voltage, parasitic thermocouple effects should be minimized. This requires firstly that the temperatures of the two reference junctions of the thermocouple mounted to the system should be equal, and secondly that the temperatures of the two input junctions to the interface should be equal. The thermal arrangements to be made to meet these requirements are discussed.

Costs can be reduced and the measurement system can be simplified by on-chip temperature sensing and by taking care that this temperature equals that of the reference juntions. For this

reason, the interface circuit was designed such that it measures both the thermocouple voltage and its own temperature. Due to self-heating, there exists a difference between the chip temperature and the reference-junction temperatures, which results in a system error. By minimizing the power consumption of the interface and arranging a good thermal contact of the interface chip with the reference junctions, the measurement error due to self-heating can be minimized.

In order to measure the thermocouple voltage accurately, we applied the three-signal technique. For this purpose at least one reference voltage is needed. Therefore, an on-chip bandgap reference is used for reference voltage.

Analysis showed that the measurement error of the interface system is mainly due to the inaccuracy of the on-chip temperature sensor and the on-chip bandgap-reference voltage. The inaccuracy caused by the non-linearity of the voltage-to-period converter is negligible. The voltage resolution is limited by the noise of the interface circuit.

The thermocouples are assembled in a thermo-well which can be grounded or floating with respect to the thermocouple. In both cases, the applied switched-capacitor input configuration is very suitable to handle these voltages, even when a single power-supply voltage is used.

Chapter 6:

This chapter presents the design aspects and test results of the thermocouple interface fabricated in 0.7-μm CMOS technology, according to the architecture discussed in Chapter 5. The characterization results of bipolar transistors in CMOS are applied to design the on-chip temperature sensor and the on-chip bandgap-reference. In the signal-processing circuit, the advanced signal-processing techniques discussed in Chapter 4, such as three-signal auto-calibration, chopping and DEM are applied.

The designed chip measures 1.7 mm × 1.9 mm. The chip is packaged in a standard 10-pin TO-5 package. The interface chip is tested over the temperature range from -40 °C to 140 °C. The voltage divider of the interface is also tested and evaluated. The relative inaccuracy appears to be less than 85×10^{-6}, which easily meets our requirements.

The performance of the on-chip bandgap reference and the on-chip temperature sensor is also evaluated. To take into account the effects of the base resistance and the effective emission coefficient, a correction factor m' is applied to the voltage ΔV_{BE}. The emperical value of m' corresponds to the value derived from the characteristics of the bipolar transistors. The experimentally found bandgap-reference voltage is lower than the nominal one. When the effect of the temperature dependence of the bias current is taken into account, still a difference of 10 mV remains. The higher-order temperature dependency of the measured on-chip bandgap reference is in agreement with that found from the $V_{BE}(\vartheta)$ characteristics described in Chapter 3. In the voltage-measurement circuit, a residual offset of 14 μV is found, and this value can change over time. It is suggested to remove this error with some additional hardware.

The total inaccuracy in the voltage measurement is 36 μV over the temperature range from -40 °C to 140 °C. The total inaccuracy in the temperature measurement is 0.37 K over the temperature range from -40 °C to 140 °C. The standard deviation of the measured input voltage amounts to 6 μV ~ 8 μV at room temperature and increases slightly at lower

temperatures. The standard deviation of the measured on-chip temperature is 0.02 K. Compared to the voltage noise; the noise in the temperature measurement can be neglected.

Chapter 7:

In this chapter, a switched-capacitor instrumentation amplifier is presented. This amplifier can be applied to pre-amplify the very small voltage of the thermocouple outputs. In this amplifier, the advanced circuit technique with dynamic-element matching of the switched capacitors is applied. Because of switched-capacitor configuration, a rail-to-rail common-mode level of the input voltage is allowed.

The DEM SC instrumentation amplifier is tested at room temperature. The extracted amplification factor is quite accurate. However, the noise performance is not as predicted: The measured input noise voltage was 5 times larger than that calculated. The reason for this large noise could not be determined.

Chapter 8 summarises the main conclusions of the research work presented in this thesis.

Samenvatting

Hoofdstuk 1:

Dit hoofdstuk vormt een introductie tot het onderwerp. Allereerst wordt het belang uiteengezet om bipolaire transistoren vervaardigd in CMOS technologie te karakteriseren. Vervolgens worden de problemen die zich voordoen bij het ontwerpen van geïntegreerde temperatuursensoren en bandgap-spanningsreferenties besproken. Tot slot wordt een overzicht van het onderzoeksprogramma gepresenteerd.

Hoofdstuk 2:

In dit hoofdstuk wordt een overzicht gegeven van de temperatuurkarakteristieken van bipolaire transitoren. Op basis van deze kennis is het mogelijk om temperatuursensoren en bandgap-spanningsreferenties te ontwerpen. Twee mogelijke structuren voor bipolaire transistoren vervaardigd in CMOS technologie worden besproken. Het betreft verticale substraat transistoren en laterale transistoren. Een vergelijking van de eigenschappen van beide typen transistoren laat zien dat, voor de vervaardiging van hoogkwalitatieve temperatuursensoren en bandgap-spanningsreferenties, verticale substraat transistoren de voorkeur verdienen.

Hoofdstuk 3:

In dit hoofdstuk worden de karakteristieke eigenschappen van bipolaire transistoren vervaardigd in CMOS technologie gepresenteerd in samenhang met de resultaten van het experimentele onderzoek. Voor testdoeleinden zijn dergelijke transistoren ontworpen, vervaardigd en ingehuisd. Testopstellingen voor karakterisatiedoeleinden zijn ontwikkeld in gebouwd. Vervolgens zijn metingen uitgevoerd om de afhankelijkheid van de spanningen V_{BE} en ΔV_{BE} van respectievelijk de temperatuur ϑ en de collectorstroom I_C te bepalen.

Uit de meetresultaten voor $I_C(V_{BE},\vartheta)$ kan worden geconcludeerd, dat in het middelbare stroombereik, het verband tussen de collectorstroom en de basis-emitterspanning een mooi exponentieel gedrag vertoont. Verder blijkt, dat het temperatuurgedrag van de basis-emitterspanning goed kan worden gemodelleerd met het bekende Gummel-Poon model. Ook de eerder gevonden negatieve correlatie tussen de geëxtraheerde parameters V_{go} and η komt overeen met die voor transistoren vervaardigd in bipolaire technologie.

De voorwaartse gemeenschappelijke-emitter stroomversterkingsfactor B_F is experimenteel onderzocht voor een groot stroom- en temparatuurbereik. Vergeleken met de B_F waarden van

transistoren vervaardigd in bipolaire technologie zijn de B_F waarden van substraattransistoren vervaardigd in CMOS technologie veel lager. Dit is een gevolg van het hoge Gummelgetal dat voortvloeit uit de grote basisbreedte.

Er is een nieuwe methode voor het extraheren van de basisweerstand gevonden. Deze methode maakt gebruik van gemeten waarden van de spanning ΔV_{BE}, de emitterstroom en de emitterstroomverhouding I_{e2}/I_{e1}. Doordat deze basisweerstandmeetmethode beter aansluit bij onze toepassing ervan, levert deze methode betere resultaten bij het voorspellen van gerelateerde niet-idealiteiten in temperatuursensoren en bandgap-spanningsreferenties. De meetresultaten laten zien dat bij hoge temperaturen de waarden van de basisweerstanden gemakkelijk de 1000 Ω kunnen overschrijden. Verder blijkt dat de basisweerstand van transistoren vervaardigd in 0.5-µm CMOS technologie lager is dan die van overeenkomstige transistoren in 0.7-µm technologie. Dit is een gevolg van de zwaardere doping in het eerstgenoemde proces. De basisweerstand veroorzaakt een ongewenste spanningsval die tot een ongewenste verhoging van de externe basis-emitterspanning leidt. Deze spanningsval kan worden gereduceerd door een lage stroominstelling te kiezen en door het effectieve emitteroppervlak te vergroten door een multi-emitter geometrie te kiezen. Er is echter een trade-off tussen de stroomdichtheid en het lage-stroomeffect.

De effectieve emissiecoëfficiënt m kan op twee manieren worden geëxtraheerd: uit de gemeten $I_C(V_{BE})$ curve, en uit de gemeten waarden van ΔV_{BE}. De resultaten van beide methoden komen goed overeen. Deze resultaten tonen dat de effectieve emissiecoëfficiënt m slechts weinig afwijkt van de ideale waarde van één. Bij precisietoepassingen dient deze afwijking echter in rekening te worden gebracht.

Mechanische spanning, die voornamelijk ontstaat bij het inhuizen, veroorzaakt een verandering van de basis-emitterspanning. Dit effect is temperatuurafhankelijk en vertoont drift en instabiliteit, hetgeen afwijkingen kan veroorzaken in temperatuursensoren en bandgap-spanningsreferenties. Experimentele waarnemingen hebben onlangs aangetoond dat pnp verticale transistoren minder last hebben van dit effect dan npn transistoren. Bij pnp transitoren blijkt het effect bij samendrukken minder groot te zijn dan bij uitrekken. Verder is aangetoond dat de ΔV_{BE} relatief minder gevoelig is voor mechanische spanning dan de basis-emitterspanning zelf. Als gevolg hiervan is het te verwachten dat bij het gebruik van pnp substraat transistoren de effecten van inhuizing op de drifteigenschappen van temperatuursensoren en bandgap-spanningsreferenties minder is dan in overeenkomstige devices die gebruik maken van npn transistoren. Verder is het aan te bevelen om een verpakkingstechniek uit te kiezen die uitsluitend mechanische rekspanningen opleverd.

Hoofdstuk 4:

In dit hoofdstuk worden geavanceerde circuits besproken die kunnen worden toegepast in dynamische temperatuursensoren en bandgap-spanningsreferenties. In pientere sensorsystemen wordt een hoge nauwkeurigheid bereikt door toepassing van onder andere autocalibratietechnieken. Mits aan bepaalde voorwaarden is voldoen wordt door toepassing van deze technieken een zeer hoge nauwkeurigheid verkregen, doordat de effecten van additieve en multiplicatieve parameters van de meetcircuits worden geëlimineerd. Gewoonlijk wordt er in pientere sensorsystemen gebruik gemaakt van microcontrollers om de uitgangssignalen van de elektronische circuits uit te lezen en te bewerken. Het is daarom nodig dat deze uitgangssignalen geschikt zijn om door microcontrollers te worden uitgelezen.

Afwegingen met betrekking tot de nauwkeurigheid, de resolutie en de omzettingsnelheid leiden tot een keuze voor het gebruik van lading-tijd convertoren in combinatie met de toepassing van conversieprincipes van indirecte A/D conversie. Het belangrijkste onderdeel van deze A/D convertor bestaat uit een modulator die gelijksspanningsignalen converteert naar het tijdsdomein. De microcontroller digitaliseert deze signalen. In dit hoofdstuk worden verschillende typen modulatoren besproken, die de signalen naar respectievelijk frequentie of tijd omzetten. Het meest geschikt voor onze toepassing zijn de modulatoren die een duty-cycle- of periodeduur-gemoduleerd uitgangssignaal opleveren. Met het oog op eenvoud, nauwkeurigheid, en gebruiksgemak, hebben we voor onze toepassing de voorkeur gegeven aan de "Modified Martin" periodeduuroscillator.

Teneinde de invloed van laagfrequent storingen, offset en 1/*f* ruis te reduceren wordt een chopping techniek toegepast. Een nadeel hiervan is dat door het optreden van klokdoorspraak een nieuwe offset component ontstaat. Deze offset kan worden gereduceerd door het toepassen van de "nested-chopper techniek" of door autocalibratie. Omdat autocalibratie toch al wordt toegepast om de effecten van additieve en multiplicatieve parameters te elimineren, is toepassing van de nested-chopper techniek in ons geval overbodig.

In onze schakelingen speelt de "Dynamic-Element-Matching (DEM)" techniek een belangrijke rol bij het elimineren van systematische fouten die door componentongelijkheid worden veroorzaakt. Deze techniek is zeer geschikt voortoepassing in voorversterkers en delers waarbij autocalibratie niet mogelijk is. Door toepassing van DEM kunnen nauwkeurige versterking van kleine signalen en deling van grote signalen worden gerealiseerd. Ook is het mogelijk om met behulp van DEM techniek het signaal $\Delta V_{\mathrm{BE},}$ dat nodig is in temperatuursensoren en bandgap-spanningsreferenties, nauwkeurig op te wekken.

Als het systeem lineair is dan kan de 3-signaal autocalibratiemethode de effecten van de meeste systematische fouten elimineren. Nietlineariteit zal in dit geval de systematische meetnauwkeurigheid beperken. Nietlineariteit kan een gevolg zijn van bijvoorbeeld de laag- en hoogfrequent polen van de integrator, de spanningafhankelijkheid van de bemonsteringscapaciteit en de nietlineariteit van tijdsvertraging van de comparator. Met een zorgvuldig circuitontwerp kan het effect van de laag- en hoogfrequent polen worden geminimaliseerd. Door twee identieke bemonsteringscondensatoren parallel te schakelen wordt het effect van de spanningsafhankelijkheid ervan teruggebracht tot de tweede orde. Verder verbetering kan worden bereikt door ervoor te zorgen dat de common-mode niveau's van alle ingangsspanningen aan elkaar gelijk zijn.

De meetresolutie wordt bepaald door ruis en storing. De resolutie kan worden verbeterd door een groter aantal bemonsteringsperioden te nemen. Dit zal echter de meetsnelheid doen afnemen, zodat er een trade-off is tussen resolutie en meetsnelheid. Kwantisatieruis kan worden verminderd door een hoger klokfrequentie van de microcontroller te kiezen.

Hoofdstuk 5:

Als case study voor de onderzoeksresultaten die in hoofdstuk 3 en 4 zijn gepresenteerd is een thermokoppel-interfacesysteem ontworpen.

In dit hoofdstuk zullen overwegingen betreffende de architectuur van dit systeem worden behandeld. Deze overwegingen betreffen zowel het thermische als het elektrische domein.

In het thermokoppelsysteem worden twee signalen gemeten: de thermokoppelspanning en de temperatuur van de referentiejunctie. Uit deze twee metingen kan de temperatuur van het te meten object worden afgeleid. Voor een nauwkeurige meting van de thermokoppelspanning moet het effect van parasitaire thermokoppeleffecten worden geminimaliseerd. Dit vereist dat de temperatuur van de twee referentiejuncties, die ontstaan als het thermokoppel aan het systeem wordt bevestigd, aan elkaar gelijk zijn. De thermisch maatregelen die getroffen zijn om dit te bewerkstelligen worden besproken.

Kosten kunnen worden bespaard en het meetsysteem kan worden vereenvoudigd door de chiptemperatuur op te meten. Daarom is het interface systeem zodanig ontworpen dat zowel de thermokoppelspanning als de chiptemperatuur worden gemeten. Als gevolg van zelfopwarming zal er een temperatuurverschil ontstaan tussen de chiptemperatuur en de temperatuur van de referentiejuncties, hetgeen in een systeemfout resulteert. Deze fout kan worden geminimaliseerd door de vermogensdissipatie van de interface chip te beperken en door deze chip in goed thermisch contact te brengen met de referentiejuncties

Teneinde de thermokoppelspanning nauwkeurig te kunnen meten wordt de 3-signaal autocalibratiemethode toegepast. Voor dit doel is tenminste één referentiespanning vereist. Deze wordt opgewekt met een bandgap-spanningsreferentie die op de chip wordt geïmplementeerd.

Een analyse van de meetresultaten toont aan dat de belangrijkste fout van het interfacesysteem wordt veroorzaakt door onnauwkeurigheid van de chiptemperatuursensor en de bandgap-spanningsreferentie. Anderzijds blijkt dat de onnauwkeurigheid welke wordt veroorzaakt door nietlineariteit van de spanning-periode omzetter verwaarloosbaar is. De spanningsresolutie wordt begrensd door de ruis van het interface circuit.

Thermokoppels worden gemonteerd in een “thermowell” die kan worden geaard of zwevend kan worden gebruikt.

Hoofdstuk 6:

Dit hoofdstuk behandeld de ontwerpaspecten en de testresultaten van de thermokoppel-interfacechip, die is vervaardigd in 0.7-μm CMOS technologie, volgens de architectuur die is besproken in hoofdstuk 5.

De karakteristieke resultaten van transistoren die in CMOS technologie kunnen worden vervaardigd zijn toegepast voor het ontwerp van de temperatuursensor en de bandgap-spanningsreferentie. In het signaalbewerkingscircuit zijn de geavanceerde signaalbewerkingstechnieken die zijn besproken in hoofdstuk 4, zoals autocalibratie, chopping en DEM, toegepast.

De ontworpen chip heeft de afmetingen van 1,7 mm × 1,9mm en is verpakt in een standaard 10-pin TO-5 behuizing. De interfacechip is getest over het temperatuurbereik van -40 °C tot 140 °C. De dynamische spanningsdeler is apart getest en geanalyseerd. De relatieve onnauwkeurigheid blijkt minder te zijn dan 85×10^{-6}, hetgeen ruimschoots aan onze eisen voldoet.

De eigenschappen van de “on-chip” temperatuursensor en bandgap-spanningsreferentie zijn eveneens geëvalueerd. Teneinde het effect van de basisweerstand en de effectieve emissiecoëfficiënt in aanmerking te nemen is bij het berekenen van ΔV_{BE} een correctiefactor

m', met een emperische waarde, toegepast. De experimenteel gevonden waarde van de bandgap-referentiespanning is lager dan de nominale spanning. Na compensatie van de effecten van de temperatuurafhankelijke instelstroom blijft er nog een verschil over van 10 mV. De hogere-orde temperatuurafhankelijkheid van de gemeten bandgap-referentiespanning is in overeenstemming met hetgeen is gevonden voor de $V_{BE}(\vartheta)$ karakteristiek die is gepresenteerd in hoofdstuk 3. Voor het spanningsmeetcircuit is een resterende offsetspanning gevonden van 14 µV. Deze waarde vertoont enige drift. Er wordt een methode gesuggereerd om deze offset te verminderen met aanvullende hardware.

De totale onnauwkeurigheid van de spanningsmeting bedraagt 36 µV over het temperatuurbereik van -40 °C tot 140 °C. De totale onnauwkeurigheid van de temperatuurmeting is 0,37 K over het temperatuurbereik van -40 °C tot 140 °C. De standaarddeviatie van de gemeten ingangsspanning bedraagt 6 µV ~ 8 µV bij kamertemperatuur en loopt enigszins op bij lagere temperaturen. De standaarddeviatie van de on-chip temperatuurmeting bedraagt 0,02 K. Vergeleken met de ruis in de spanningsmeting kan is de ruis in de temperatuurmeting verwaarloosbaar klein.

Hoofdstuk 7:

In dit hoofdstuk wordt een switched-capacitor (SC) instrumentatieversterker gepresenteerd. Deze versterker kan worden gebruikt als voorversterker van de zeer kleine thermokoppelspanningen. In deze versterker wordt een geavanceerde circuittechniek toegepast, die gebruik maakt van geschakelde capaciteiten en dynamic element matching (DEM). Dank zij de switched-capacitor configuratie kan een rail-to-rail common-mode niveau van de ingangsspanning worden toegestaan.

The DEM SC instrumentatieversterker is getest bij kamertemperatuur. De geëxtraheerde versterkingsfactor blijkt zeer nauwkeurig te zijn. De ruiseigenschappen blijken echter niet over te komen met de verwachtingen: De gemeten equivalente ingangsspanningsruis blijkt ongeveer een factor 5 groter te zijn dan verwacht. De reden hiervan kon nog niet worden vastgesteld.

Acknowledgements

This thesis would not have been possible without the support of many people. Therefore, I would like to thank all of them, including those whose names are not mentioned below. First, I would like to express my deep gratitude to Prof. Gerard Meijer. Without his continuous support for my work, and his great help in improving the clarity, this thesis would not have been finished. Secondly, I would like to thank Prof. Arthur van Roermond for reading the earlier versions of this thesis and giving comments to improve its structure.

Further, I would like to thank:

My colleague and roommate Fabiano Fruett for his help during the past four and half years. Harry Kerkvliet, Loek van Schie, Wil Straven and Antoon Frehe for all technical supports for repairing and updating my PC, for updating the software from time to time, and for managing the UNIX systems, etc.

Yvonne van der Broek, Olfien Lefebre, Nicollet Dingeldein and Marion de Vlieger for their kind help in administration.

Herman Casier of Alcatel Micorelectronics for his advice on and support in fabricating the test devices in different CMOS technologies.

Danny Lambricht, Greta Milczanowska and Marc van Eylen of IMEC for doing DRC and ERC checks of chip layouts.

Mirjam Nieman for the English review of the whole thesis.

Especially, I would like to thank the Technology Foundation STW; their financial support under contract DEL 3532 was of crucial importance to this research.

And last, but far from least, I would like to thank Xiujun Li, my husband and colleague, for his continuous support.

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Biography

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