DC Cable Short Circuit Fault Protection in VSC-MTDC

By Shining Lu (4299841)

in partial fulfillment of the requirements for the degree of

MSc Electrical Engineering at Delft University of Technology (TU Delft)

& MSc Technology – Wind Energy at Norwegian University of Science and Technology (NTNU)

To be defended

on Monday, July 6th, 2015

at EWI/EEMCS faculty, TU Delft

Supervisors:	Prof. Marjan Popov (TU Delft)
	Prof. Hans Kristian Høidalen (NTNU)
Thesis Committee:	Prof. Marjan Popov (TU Delft)
	Prof. Jose Rueda Torres (TU Delft)
	Prof. Armando Rodrigo Mor (TU Delft)

TUDelft
Delft University of Technology

EWEM

NTNU – Trondheim
Norwegian University of Science and Technology

Abstract

With the development of offshore wind farms, Voltage Source Converter based High Voltage Direct Current or Multi-terminal High Voltage Direct Current Technology (VSC-HVDC/MTDC) is becoming promising in the field of large-capacity and long-distance power transmission. However, its extreme vulnerability to DC contingencies remains a challenge in both research and practice. DC cable short circuit faults, or cable pole-to-pole faults, though less common than DC cable ground faults, can cause the most severe damage to the VSC as well as the whole system. In this thesis work, firstly a simple 3-terminal MTDC system is built and validated in PSCAD/EMTDC. Afterwards, based on the self-built MTDC system, DC cable short circuit faults with different locations are studied and analyzed in both theory and numerical simulation. Finally, a comprehensive protection scheme is proposed against such DC cable short circuit faults in the target MTDC system, combining the sub-schemes in fault detecting/locating principles, fault isolating tools and fault current limiting technologies. The coordination among the three parts is also taken into consideration. The scheme is later proven to be fast, selective, reliable, sensitive and robust in general. Moreover, the specific design procedure is further extended into a general design philosophy for DC cable short circuit fault protection in VSC-MTDC systems.

Keywords

Preface

This is the report for the master thesis 'DC Cable Short Circuit Fault Protection in VSC-MTDC' for European Wind Energy Master Program (EWEM), Electric Power System track. This project lasted from October 2014 to June 2015, with the work done partly in Norwegian University of Science and Technology (NTNU), Trondheim, Norway and partly in Delft University of Technology (TU Delft), Delft, the Netherlands.

Along with the emerging offshore wind farms, HVDC technology is becoming more and more attractive in high-capacity and long-distance transmission. On the other hand, the integration of wind farms is also widely acknowledged to be one of the most imminent applications in HVDC. Indeed, HVDC technology and wind energy interconnect and interact with each other. This is largely the reason why I chose this thesis topic to complete the two-year master study in EWEM. Although the report mainly falls into the electrical engineering field, the whole project roots in the context of a larger integration of wind energy and other sustainable resources in the future. The author also believes that the coming breakthroughs in HVDC as well as in other fields of electric power systems would contribute to further development in the wind energy industry.

Promising as the VSC-MTDC technology might be, it is also extremely vulnerable to DC contingencies, especially the pole-to-pole faults. During such faults, the diodes are usually considered to be the most critical component and that the fault current flowing through them cannot exceed 2 p.u.. In this thesis, a three-terminal VSC-MTDC system is built in PSCAD/EMTDC and a DC cable short circuit protection scheme is proposed for it. In the protection scheme, faults are detected by differential protection and/or wavelet-based fault detection, with overcurrent protection as the backup plan. Based on the data, the exact location of the fault can be further estimated by the travelling wave based fault locating principle. For fault isolation, three types of DC circuit breakers are introduced and the selection is made based on the coordination of the clearance time and the critical time limit with different diode sizing strategies. Above all, fault current limiters of both protective inductors on the DC side and the LCL circuit on the AC side are also implemented in the protection scheme to limit the overcurrent magnitude as well as to postpone the critical moment. Coordination among the three aspects of fault detecting/locating, fault isolating and fault current limiting are briefly discussed in the report as well, followed by a preliminary evaluation proving the proposed scheme to be fast, selective, reliable, sensitive and robust. Yet, the report also presents some suggestions in optimization and follow-up studies.

Throughout the thesis work, both model development, fault study and protection scheme design are illustrated with both theory and PSCAD simulation. Although the proposed scheme is based on a simple self-built three-terminal MTDC system, the general principle in protection system design should be similar for other grid topology. Nevertheless, particular issues might arise with the increase of terminal numbers and network complexity, or a change in VSC and cable configuration.

This work could not have been done without the help and support from many people, to whom I would like to extend my sincere gratitude here. Firstly, to my two supervisors, Professor Dr. Marjan Popov at TU Delft and Professor Dr. Hans Kristian Høidalen at NTNU, for providing the opportunity to study this interesting topic, as well as the valuable feedback throughout the work. The appreciation also goes to Lian Liu for his enthusiasm, patience and timely help in simulations; to Dr. Olimpo Anaya Lara and Dr. Raymundo Torres as well, for the guidance and assistance during my stay in NTNU. In addition, I also appreciate the valuable time and effort from the thesis committee, Dr. Marjan Popov (TU Delft supervisor), Dr. Jose Rueda Torres and Dr. Armando Rodrigo Mor. Last but not the least, thanks to the hugs and brownies; they will always be the warmest and sweetest memories of Europe.

Shining Lu

16/06/2015

Contents

List of Figures

List of Tables

Abbreviation

ANN	Artificial Neural Network
AOA	Angle Of Attack
CSC	Current Source Converter
CWT	Continuous Wavelet Transform
DB4	4th order Daubenchies Wavelet
DCCB	Direct Current Circuit Breaker
DWT	Discrete Wavelet Transform
FCL	Fault Current Limiter
GPS	Global Positioning System
HVAC	High Voltage Alternative Current
HVDC	High Voltage Direct Current
ICC	Inner Current Controller
IGBT	Insulated-Gate Bipolar Transistor
KCL	Krichhoff's Current Law
KVL	Krichhoff's Voltage Law
LCC	Line Commutated Converter
MMC	Modular Multilevel Converter
MTDC	Multi-Terminal High Voltage Direct Current
OWF	Offshore Wind Farm
PLL	Phase-Locked Loop
PTC	Positive Temperature Coefficient
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
SWT	Stationary Wavelet Transform
TSR	Tip Speed Ratio
VS	Vacuum Switch
VSC	Voltage Source Converter
XLPE	Cross Linked Polyethylene

Chapter 1 Introduction

1.1 Background and Motivation

Nowadays, due to the concerns about the depleting fossil resources and the global warming effects, the idea of sustainable energy is getting an increasing amount of interest and attention. One possible approach to satisfying the ever growing need in renewable energy is to construct more Offshore Wind Farms (OWF). Compared to its onshore counterpart, an OWF is able to capture stronger and steadier wind, thus generating greater and smoother electricity. Moreover, it also causes fewer public objections concerning audio and visual 'pollutions', land occupation, etc.

Along with the emerging OWFs and their demand in high-capacity and long-distance transmission, High-Voltage Direct Current (HVDC) technology is becoming more attractive than the conventional High-Voltage Alternative Current (HVAC) in the technical, economic and environmental aspects [1]. On the other hand, it is also believed that the most imminent application in HVDC is probably the integration of wind farms [2]. Therefore, it is of interest and significance to look into the interactions between them, and see how HVDC facilitates OWF power transmission and how the OWF production profile affects the HVDC transmission system.

Speaking of the history of HVDC technology, it was first commercially adopted to connect Gotland Island to the mainland Sweden in 1954. Ever since, HVDC technology has undergone rapid developments, one of the most noteworthy breakthrough among which is the introduction of HVDC based on Voltage Source Converters (VSC). Compared to the classic Current Source Converters (CSC), also known as Line Commutated Converters (LCC), VSC is superior in aspects such as better controllability, smaller filter size and less demand in AC network support. More importantly, since there is no DC voltage reversal associated with power reversal (as CSC-HVDC will require), VSC-HVDC technology has furthermore brought the Multi-Terminal HVDC (MTDC) topologies and the vision of Supergrid closer to reality.

However, VSC's destructive vulnerability to DC contingencies turns out to be an obstacle in the way of further developments and wider applications. On one hand, the lack of change in current polarity makes DC fault clearance much more challenging than that in AC systems. On the other hand, the low impedance in HVDC cable systems will result in high fault current magnitude which can damage the entire grid [3]. Moreover, unlike a CSC-HVDC system, even when all the IGBTs are blocked, it is still impossible to prevent the AC grid from feeding the fault via the freewheeling diodes path [4]. Indeed, DC fault handling and protection is usually reckoned to be the most important and most difficult remaining technical challenge in VSC-MTDC [5].

Among all DC side faults, DC cable short circuit faults, or pole-to-pole cable faults, can cause the most severe danger to the system. During the fault, the current rises considerably in a short time and can not only damage the freewheeling diodes and DC cables nearby, but also put the whole converter station or the entire MTDC system at risk. Therefore, it is necessary and important to study DC cable short circuit protection in a VSC-MTDC system.

1.2 Problem Description

Unlike conventional HVDC technology where the DC fault current can be successfully suppressed by the converters and the smoothing reactors, VSCs are highly vulnerable to DC faults, especially DC cable short circuit faults. While the Insulator-gate bipolar transistors (IGBTs) could be blocked for self-protection, the fault current can still find its path through freewheeling diodes until the corresponding circuit breakers trip and isolate the fault. In fact, it is the anti-parallel diodes that are the most vulnerable components during the DC fault [3]. This has been one of the main challenges VSC-MTDC technology encounters.

In theory, literature [3] defines three stages in the fault response, and concludes that the switchgear should operate before the *critical time* to protect the system from the devastating *overcurrent*. This indicates that the DC fault has to be cleared in the system within a few milliseconds [5]. However, such requirements cannot yet be fully satisfied by the existing technology [4, 6].

Above all, a protection system aims to be selective, sensitive, fast, reliable and robust [5]. More specifically, it is designed to reliably isolate the faulty part from the system in a short time when and only when there is a fault, while maintaining the remaining part in secure operational state. As mentioned earlier, when a DC cable short circuit occurs, the current quickly rises to a large magnitude, usually within a few milliseconds. Therefore, speed is reckoned to be the most stringing requirement for the DC protection system. In order to isolate the fault before the current exceeds the maximum current that a system can sustain, numerous research and experiments have been done in recent years. Generally speaking, they can be divided into two main categories. One focuses on <u>shortening the fault clearance time</u> by faster fault detecting algorithm and fault isolating devices. The other approach is <u>limiting the fault current</u> directly by introducing various kinds of fault current limiters, so that the fault can be cleared before the system gets damaged. Both ways have been explored extensively; however, not much work has gone into combining them.

In this thesis project, all of the three aspects in fault detection principles, fault isolation devices and fault current limiting technologies are considered, and a comprehensive protection scheme is proposed afterwards. The interaction and coordination of different aspects are also studied and discussed. Last but not the least, although the proposed scheme is designed for the specific VSC-MTDC system discussed in this project, the general principle should be similar and the methodology can be applied to other MTDC systems as well.

1.3 Objective and Scope

The goal of this master thesis is to propose a feasible and comprehensive DC cable short circuit protection scheme for a three-terminal VSC-MTDC model built in PSCAD/EMTDC, with the three aspects of 1) fault detection & location, 2) fault isolation, and 3) fault current limiters taken into consideration.

This topic can furthermore be divided into several sub-topics:

- Network modeling and control philosophy
- Fault response of the DC cable short circuit and how the fault location affects it
- Fault detecting and locating algorithms
- DC Circuit Breaker (DCCB) Technology
- Fault current limiters and the effects
- Proposing a protection scheme based on the previous study

The scope of the master thesis is set as follows:

- Target System – a simple 3-terminal MTDC system in radical topology is modeled and studied in PSCAD/EMTDC. The model is in symmetrical monopole configuration, with two-level VSC technology and HVDC submarine cable systems.
- Fault Configuration – only bolt (zero fault impedance) and permanent pole-to-pole faults are studied in this project. The fault will be implemented at different locations along one of the two cables (due to the symmetry of the system topology).
- Testing Method – all the tests are performed in PSCAD/EMTDC and the conclusions drawn from the simulation results. No practical tests are involved.
- Exclusions – the following aspects are not considered in the project:
  - Distinguishing DC cable short circuit faults from AC faults or pole-to-ground DC faults

- o Subsequent faults after the pole-to-pole fault
- o Control strategy on the reboot/recovery of the healthy part in the system after the faults
- o The impact of relays, sensors, DCCBs and other added devices except for the fault current limiters in the proposed protection system
- o The details in the onshore and offshore AC systems modeling (instead, they are modeled as ideal AC voltage sources)
- o The detailed modeling of DCCBs as well as the current interruption process (instead, a DCCB is modeled as an ideal switches that always successfully opens with a delay of clearance time)
- o Noise, measurement errors and communication errors.

1.4 PSCAD/EMTDC and Simulation

As mentioned in the previous section, the general methodology used in this master thesis project is numerical simulation in PSACD/EMTDC.

PSCAD, or "Power System Computer Aided Design", is a widely used power transient simulation software especially in Europe. Above all, PSCAD also has a reputation in its advanced cable model. Therefore, PSCAD is an appealing tool in HVDC modeling and fault transient simulation for this project.

In the project, extensive simulations are conducted, the purpose of which is concluded as follows:

- To validate the model performance in operational states
- To study and analyze the system fault response and then comparing it with the theory
- To verify and evaluate different detecting/locating methods
- To test and size the fault current limiters
- To propose a protection scheme
- To evaluate the proposed scheme

1.5 Report Layout

This thesis report contains eight chapters in total. Firstly, Chapter 1 introduces the project background and illustrates the motivation, the objective and the numerical simulation method of the project. Next, Chapter 2 focuses on developing the VSC-MTDC model and later validates it with simulation results. In Chapter 3, DC short circuit fault is studied in both theory and simulation, ending by suggesting three intuitive ideas in fault protection: efficient fault detecting & locating principles, fast fault isolating devices, and effective fault current limiting technologies. Each of them is further elaborated in Chapter 4 to Chapter 6 respectively. Based on the simulation results and the preliminary conclusions obtained from those chapters, Chapter 7 proposes a comprehensive protection scheme, followed by a preliminary evaluation and some possible optimization advices. Finally, Chapter 8 concludes the whole report by summarizing the main findings and contributions of this thesis work and suggesting some interesting topics for future work.

Chapter 2 Developing the VSC-MTDC Model

In this chapter, the dynamic model of a simple VSC-MTDC system is built in PSCAD/EMTDC. The target system is a simplified version of sub-system DCS1 of *CIGRE B4 DC Grid Test* benchmark with some necessary modifications. More specifically, it is a three-terminal, two-level VSC-MTDC system connected with two submarine HVDC cables in radical topology and symmetrical monopole configuration. As for the control part, the decoupled vector control mechanism with inner loop current controllers and outer loop controllers is adopted. Sizing of the components and tuning of the controllers have been dealt with, as well as the cable configuration. Finally, a testing simulation is run to test and verify the model performance. The VSC-MTDC system provides a base platform for further studies in this project.

2.1 System Description

In 2013, a DC grid test system is proposed by CIGRE B4 [6], shown as in Figure 2.1. This system is relatively comprehensive, consisting of two onshore AC systems, four offshore AC systems and two DC nodes connected by three VSC-DC sub-systems as well as some HVAC connections. In addition, it also considers both DC Monopole (symmetrical) and DC Bipole in HVDC configurations, both overhead lines and cables in transmission line types, as well as two DC-DC converters.
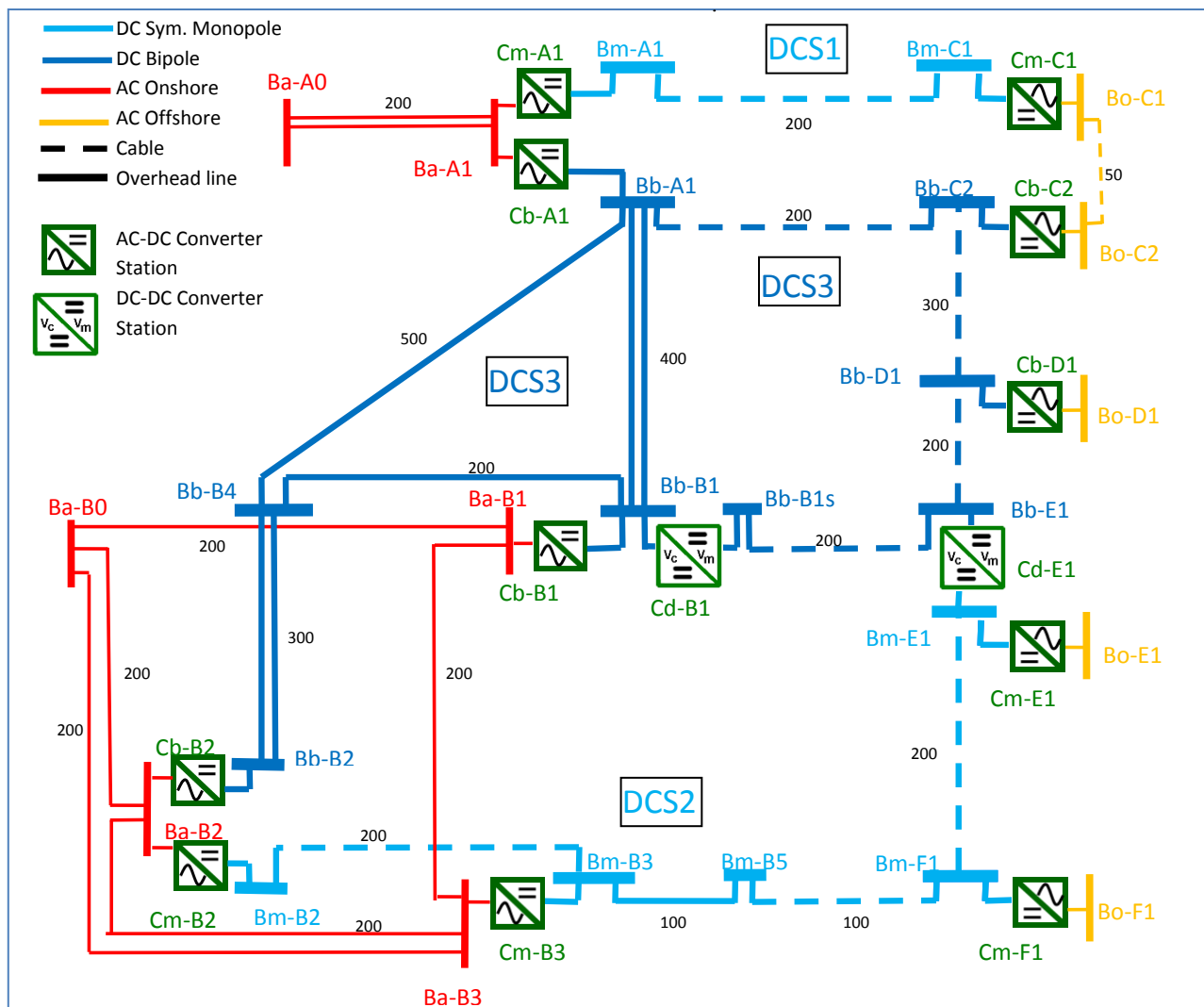
Figure 2.1 CIGRE B4 DC Grid Test System (taken from [6])

Interesting as such comprehensive system might be, the thesis only focuses on protecting the system from DC fault in MTDC grids. Therefore, due to the limited time and effort, the scope of the thesis narrows down to a three-terminal sub-system DSC1 comprised of Node A1 (onshore), C1 and C2 (offshore). For further simplification, the bipolar HVDC configuration between A1 and C2 is also modified into symmetrical monopole in this stage (same as between A1 and C1), while the DC capacitors are divided into two with the mid-points grounded. What is more, since the main focus is on the HVDC grids instead of the HVAC network, the AC connection between C1 and C2 is <u>not</u> considered at this moment. The modified system topology is shown in Figure 2.2 or Figure 2.3 in PSCAD/EMTDC environment.

As can be seen from Figure 2.2 and Figure 2.3, the built system is in radical topology. Compared to ring topology and meshed topology, this topology lacks in redundancy and reliability, but is much simpler and cheaper than its counterparts [7].

The general system data is given in Table 2.1-2.3 as specified in [6]. For electrical components sizing and control system tuning, per unit (p.u.) values will be referred, given the base values set as in Table 2.4.
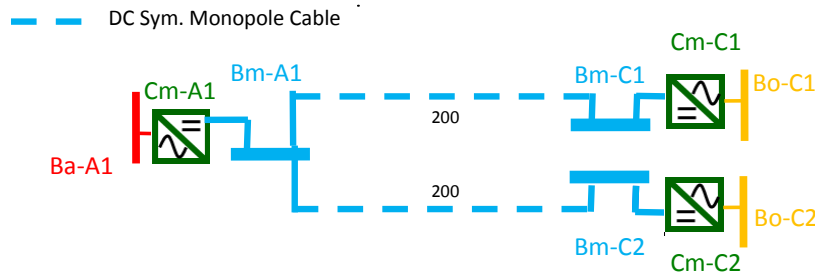
Figure 2.2 Modified Three-terminal VSC-HVDC System Connected with DC Symmetrical Monopole Cable
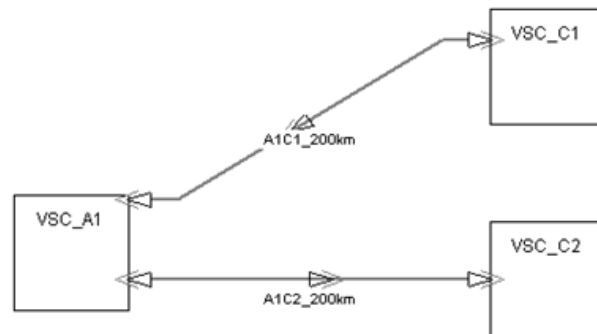
Figure 2.3 System Layout in PSCAD/EMTDC Environment

Table 2.1 AC Bus Data

AC Bus	Nominal Voltage [kV]	Generation [MW]	Load [MW]
Ba-A1	380	Slack Bus	
Bo-C1	145	500	0
Bo-C2	145	500	0

5

Table 2.2 AC-DC Converter Station Data

AC-DC Converter Station	Power Rating [MVA]	DC Side Voltage [kV]	Operation Mode Setpoints	
Cm-A1	800	+/-200	Q = 0	V_{DC} = 1pu
Cm-C1	800	+/-200	P = 500MW	Q = 0
Cm-C2	800	+/-200	P = 500MW	Q = 0

Table 2.3 Line Data

Line	Length [km]	Power Rating [MVA]	Max. current [A]	Type
A1C1	200	800	1962	Submarine Cable
A1C2	200	800	1962	Submarine Cable

Table 2.4 Base Value for Per Unit

	Base
S	1000 MW
V_{AC} (onshore)	220 kV
V_{AC} (offshore)	145 kV
V_{DC}	400 kV

2.2 Electrical Components

This section describes the intensive work on electrical components modeling. According to the VSC-HVDC technology theory, the converter stations at each end of the HVDC transmission link share the same topology. Therefore, the electrical circuit parts of sub-system VSC_A1, VSC_C1 and VSC_C2 are modeled as identical (except for the necessary difference in parameters), as shown in Figure 2.4.
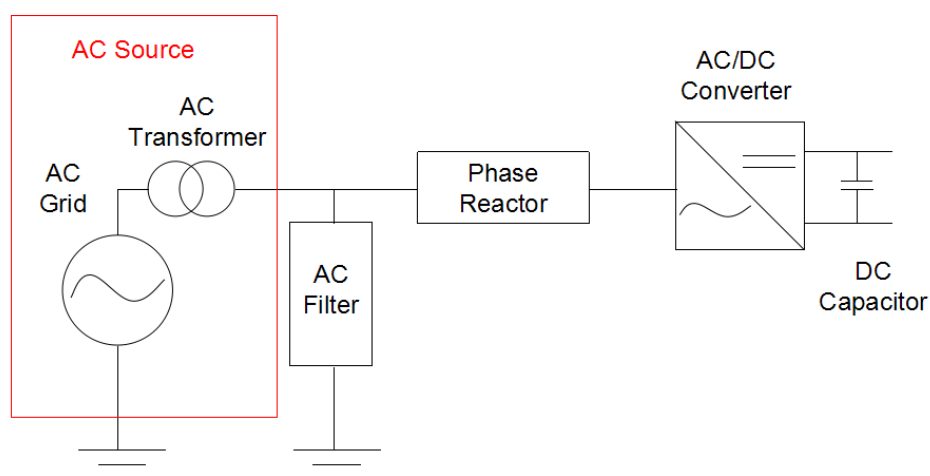
Figure 2.4 Electrical Circuit Model Overview

As can be seen from Figure 2.4, each model is comprised of five units listed as below.

- AC source unit (including the AC grid and the transformer)

6

- AC filter unit
- Phase reactor unit
- AC/DC converter unit
- DC capacitor unit

A more detailed modeling procedure as well as the sizing parameter calculation will be illustrated in the remainder of this section.

2.2.1 AC Source Unit

Since the main focus is on the HVDC grids, the AC Source unit is considerably simplified in the model. Firstly, the AC grid is represented by an ideal voltage source. It neglects the harmonic disturbance and the thevenin impedance, which indicates that the AC grid is perfectly stiff. This assumption, however, is not realistic in practice especially for offshore wind farm plants (C1 & C2). Actually, numerous control strategies have been put forward to deal with the weak offshore grid. Yet, such topics are not within the scope of the thesis. Secondly, the AC transformer component is not modelled. Actually, it is treated as a part included in the ideal voltage source model. This avoids the consideration of phase shift, ratio selection, tap setting, transformer losses, saturation problems, etc. However, a step-down ratio of 380/220 in voltage (as the wye/delta transformer usually adopted in practice) is taken into consideration from the onshore side, turning the voltage level to 220kV.

As a summary, the voltage seen after the transformer point, or the AC source unit as indicated in Figure 2.4, is modeled as an ideal voltage source (R=0) of the nominal voltage, as shown in Figure 2.5 and Table 2.5.
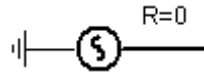
Figure 2.5 AC Source Block Model

Table 2.5 AC Source Parameters

AC System	Voltage (kV)
A1	220
C1	145
C2	145

2.2.2 AC Filter Unit

Due to the Pulse Width Modulation (PWM) technology adopted by the converter, high frequency harmonics are generated in the circuit. As a result, AC filters are necessary to remove such harmonics. In literature [8], an RLC filter, as shown in Figure 2.6, is designed to realize this function given the tuned resonant frequency ω_0, quality factor q, and shunt reactive power Q_{shunt} injected at the power frequency. The RLC values in the filter can be calculated with Equation (2.1) – (2.3).

$$C = \frac{Q_{shunt}}{2\pi f V_n^2}$$ Eq. (2.1)

$$R = \frac{q}{\omega_0 C}$$ Eq. (2.2)

$$L = \frac{1}{C\omega_0^2}$$ Eq. (2.3)

7

In the model, switching frequency (f_{sw}) is set as 1800Hz (36th harmonic of 50 Hz), so that the resonant frequency is calculated as in Equation (2.4). Furthermore, assume quality factor q=25, shunt reactive factor Q_{shunt}=0.06 p.u. (as in [3]), the calculated RLC in per unit (p.u.) values are listed in Table 2.6.

$$\omega_0 = 2\pi f_{sw} = 2\pi \times 1800 = 11310 \text{ rad/s} \qquad \text{Eq. (2.4)}$$
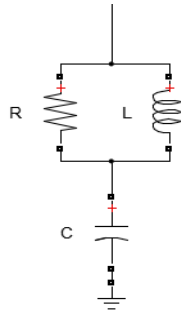
Figure 2.6 AC Filter Block Model

Table 2.6 AC Filter Parameters

Component	Value (p.u.)
R	11.56
L	0.013
C	0.06

2.2.3 Phase Reactor Unit

Phase reactors provide the attenuation of current ripples - the larger the phase reactor, the smaller the peak-to-peak ripple. On the downside, a larger phase reactor also slows down the dynamics of the converter. Therefore, there is a tradeoff in the phase reactor sizing. In the model, the phase reactor model is designed as a resistor and inductor in series, as shown in Figure 2.7. The parameters are selected as L_pr=0.15 p.u., R_pr=1% L_pr = 0.0015 p.u., as listed in Table 2.7.

L_pr   R_pr
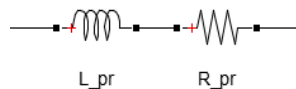
Figure 2.7 Phase Reactor Block Model

Table 2.7 Phase Reactor Parameters

Component	Value (p.u.)
L	0.15
R	0.0015

2.2.4 AC/DC Converter Unit

Unlike CSC-HVDC, VSC-HVDC usually uses GTOs or IGBTs which can be fully controlled, usually by PWM techniques. There are several possible configurations for a three-phase VSC, the simplest among which is the two-level topology. The two-level topology is comprised of six switch arms, each anti-paralleled by a free-wheeling diode. Compared to other topologies such as multi-level or Modular Multilevel Converter (MMC), it can only provide with two different voltage levels and therefore has more severe problems in harmonics.

In the model, the two-level IGBT based VSC is selected for the system, as shown in Figure 2.8. Moreover, a three-phase sinusoidal pulse width modulation (SPWM), Ua, Ub and Uc, with triangle carrier (tri) switching at 1800Hz (36th harmonics) is selected to provide with the gate signal, as in Figure 2.9. According to the PWM theory, the system will see relatively high 35th and 37th harmonic, which should be attenuated by the AC filter designed in 2.2.2. The signal '*dblk*' controls the operation/blocking mode of the PWM; it helps to block the IGBT for protection during start-up, fault contingency and so on. As for the control strategy, vector control is selected, the details of which will be further discussed in Section 2.3.
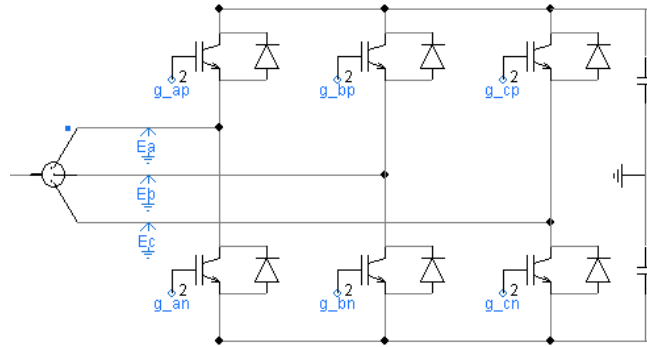
Figure 2.8 Two-level IGBT-VSC
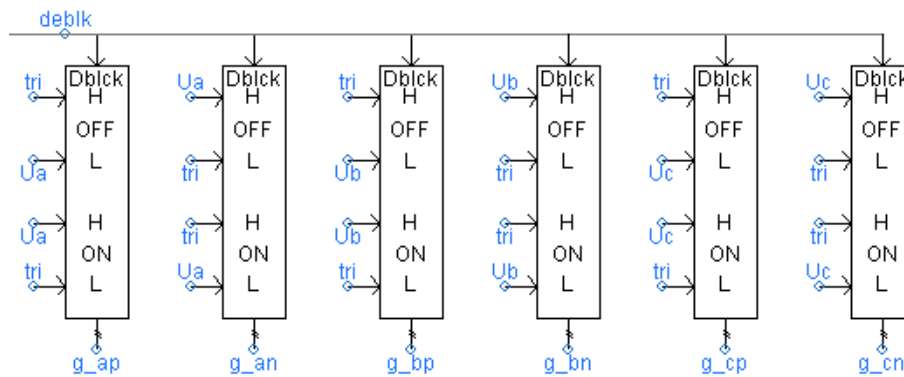
Figure 2.9 PWM Modulation

2.2.5 DC Capacitor Unit

The capacitors on the DC side aim to maintain the DC voltage for VSC operation, as well as to filter the ripples of the DC side. The sizing is a trade-off between ripple tolerance, control stiffness and capacitor lifetime, as well as cost and space restrictions [4]. In practice, the size of DC capacitors are mainly determined by the desired transient behavior, usually characterized by time constant τ, as illustrated in Equation (2.5). It is defined as the time needed to fully charge the capacitor at nominal power rating and rated voltage level. In the model, each capacitor in Figure 2.8 is designed as $625\ \mu F$ so that the so-called critical time (as will be introduced in Chapter 3) is extended to millisecond scale.

$$C_{dc} = \frac{2 \times \tau \times P_n}{V_{dc}{}^2}$$
Eq. (2.5)

More often than not, DC capacitors are included in the VSC-HVDC converter enclosure, as shown in Figure 2.8. Also from the figure, it can be noticed that the DC capacitor unit is divided into two capacitors connected to the ground-clamped neutral point of the converter in the model, in accordance to the adopted symmetrical monopole topology.
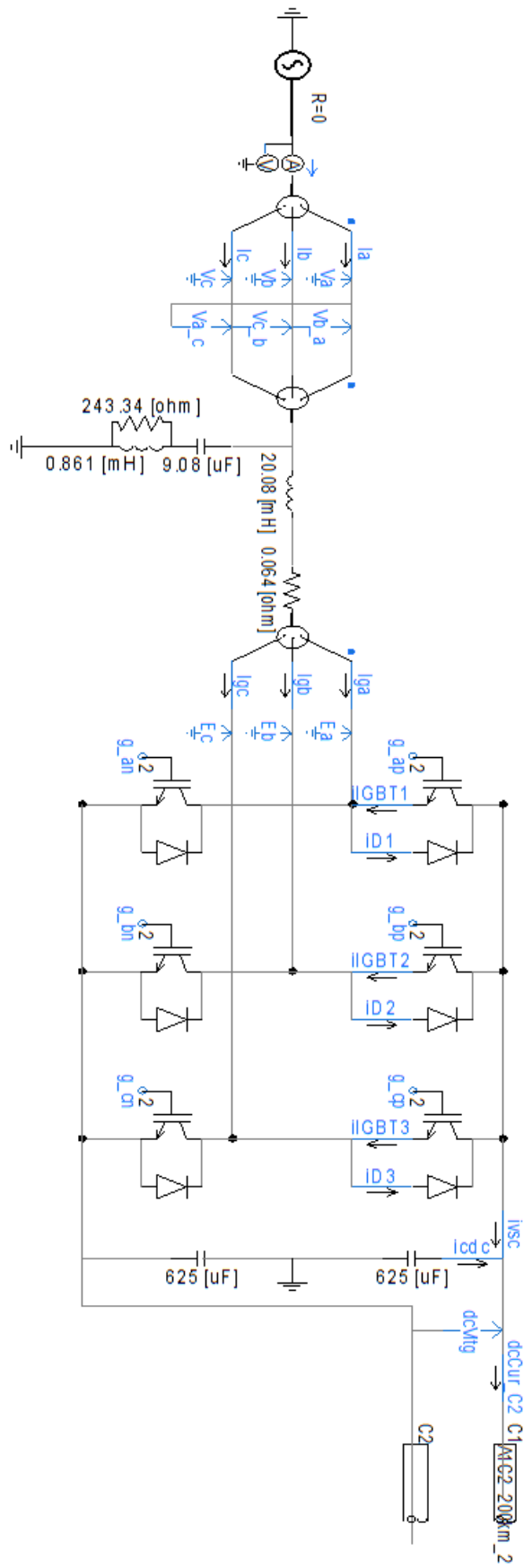
Figure 2.10 VSC Station Electrical Subsystem (VSC_C2 as an example)

2.2.6 Electrical Subsystem Overview

In summary, the electrical part of a VSC station block is given in Figure 2.10. The figure also defines the positive directions for the measurements in the remainder of the report.

2.3 Control Strategy

One of the most distinguished advantages of VSC-HVDC over CSC-HVDC is its full controllability. There are mainly two control mechanisms, namely

- Load angle control
- Vector control

Compared to the load-angle control mechanism, vector control outperforms in dynamics. Since the project focuses on transient behavior, the latter is adopted in the model. An overview of VSC controllers with vector control is given in Figure 2.11.

According to the figure, the whole control system can be divided into three parts:

- Phase-Locked Loop (PLL) Controller
- Inner Loop (Current) Controller
- Outer Loop Controller
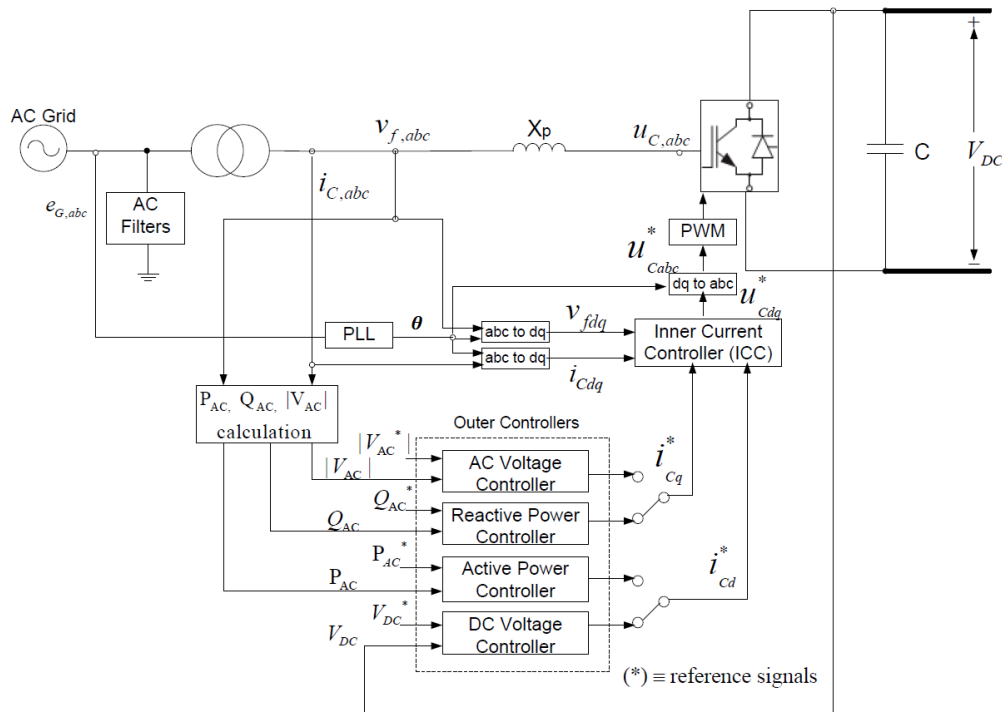
Figure 2.11 VSC Controller Overview (modified from [4])

2.3.1 PLL Controller and Park Transformation

In vector control, all the three-phase electrical quantities in abc-system, i.e., I_{abc} and U_{abc} are transformed through Park Transformation into those in direct- and quadrature-components in dq0-system. The park transformation block is provided by PSCAD/EMTDC library, the details in transform matrix of which can be found in *Appendix A*. Thereafter, the dq-components can further be controlled through two decoupled PI controllers respectively, which will be described soon in Section 2.3.2. Then an inverse Park transformation block transforms the components in dq0-system back to abc-system for the PWM control.

11

Apart from the abc-components, Park/Inverse-Park transformation also needs one more input – transformation angle θ, which is generated as the output of the PLL block. Note here that in order to align the voltage with d-axis (so that V_q=0), an offset of $\pi/2$ is necessary in the PLL block setting in this case.

2.3.2 Inner Current Controller

The Inner Current Controller (ICC) roots from Kirchhoff's Voltage Law (KVL) stating that the voltage drop across the phase reactor equals the potential difference between the AC source unit and the AC/DC converter unit, as expressed in Equation (2.6), or Equation (2.7) & (2.8) when transformed into dq-system.

$$V_{abc} = Ri_{abc} + L\frac{di_{abc}}{dt} + V_{conv,abc} \qquad \text{Eq. (2.6)}$$

$$L\frac{di_d}{dt} + Ri_d = V_d + \omega Li_q - V_{conv,d} \qquad \text{Eq. (2.7)}$$

$$L\frac{di_q}{dt} + Ri_q = V_q - \omega Li_d - V_{conv,q} \qquad \text{Eq. (2.8)}$$

According to the control theory, the ICC can be modeled as in Figure 2.12. As can be seen in Figure 2.12, a pair of decoupled PI controllers is utilized in ICC. When it comes to PI tuning, literature [9] recommends the *modulus optimum* method in inner loop control for its fast response. According to the theory, modulus optimum is achieved by canceling the largest time constant [10], as shown in Equation (2.9) and (2.10) in this case. Therefore, $T_i = \tau_{pu} = 0.318$ s . Furthermore, K_p can be calculated in Equation (2.11).

$$T_a = \frac{T_{sw}}{2} = \frac{1/1800}{2} = 0.0003 \text{ s} \qquad \text{Eq. (2.9)}$$

$$\tau_{pu} = \frac{L_{pr,pu}/\omega_b}{R'_{pr,pu}} = \frac{0.15/100\pi}{0.0015} = 0.318 \text{ s} \qquad \text{Eq. (2.10)}$$

$$K_p = \frac{\tau_{pu} \times R'_{pr,pu}}{2T_a} = \frac{\tau_{pu} \times R'_{pr,pu}}{T_{sw}} = \frac{0.318 \times 0.0015}{1/1800} = 0.859 \qquad \text{Eq. (2.11)}$$
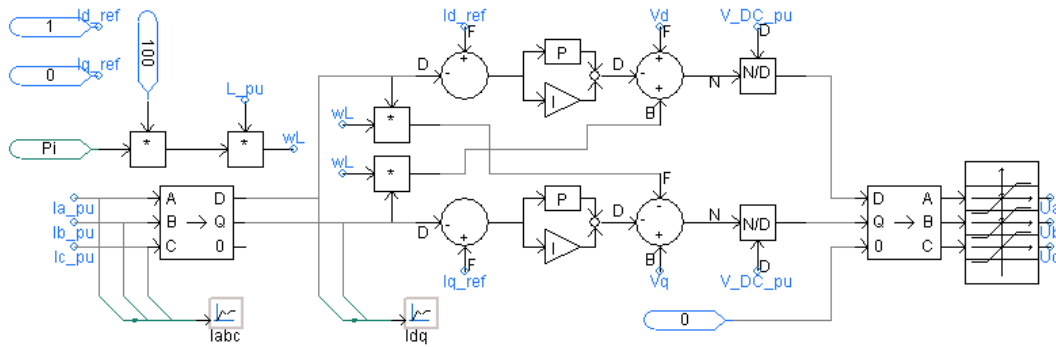
Figure 2.12 Inner Current Controller Models in PSCAD/EMTDC

2.3.3 Outer Controllers

As indicated in Figure 2.11, the outer controller system is comprised of two groups of controllers providing with the reference signals of d-component and q-component respectively for ICC. Each group contains two options: id* can be controlled by either Active Power (P) or DC Voltage (V_{DC}), while iq* by either Reactive Power (Q) or AC Voltage Magnitude ($|V_{AC}|$). In weak AC grid conditions, real power will be controlled by AC frequency. Neglecting the AC frequency controlling for now, there are four possible combinations of control strategy which could be arbitrarily selected for each converter:

- Controlling P and Q
- Controlling V_{DC} and Q
- Controlling P and $|V_{AC}|$

- Controlling V_{DC} and $|V_{AC}|$

In a HVDC or MTDC system, however, at least one controller should be responsible for DC Voltage control to maintain the power balance [11]. Actually, it is crucial to maintain the stable DC voltage, similar to the importance of maintaining a stable frequency in AC system [5]. In the three-terminal system described in Figure 2.3, the following control strategy given in Table 2.8 is selected.

Table 2.8 Control Strategy in Outer Controllers

AC-DC Converter Station	Control Strategy	
Cm-A1	V_{DC} = 400 kV = 1 p.u.	Q = 0
Cm-C1	P = 500 MW = 0.5 p.u.	Q = 0
Cm-C2	P = 500 MW = 0.5 p.u.	Q = 0

Note here that what has been given in Table 2.8 only shows a base case in the operation, based on which the fault simulation is run in the following chapters. However, since the VSC_C1 & C2 are offshore wind farm, their production is not constant as nominal power all the time. Instead, they may vary within the range from 0 to the rated power according to the wind speed, which is further illustrated in _Appendix B_. Therefore, load variation study has also included in both model validation (Section 2.5) and proposed scheme evaluation (Section 7.4). Since the AC grid is only modelled as an ideal voltage source, the load variation is implemented by changing in active power reference value in VSC_C2 station.

DC Voltage Controller

A simple PI controller is implemented in the DC Voltage Controller, as shown in Figure 2.13 (a). According to [9], a feed-forward component of $(\frac{v_{dc,pu}}{v_{d,pu}} I_{L,pu})$ can be imposed to improve the speed of dynamic response, as shown in Figure 2.13 (b).
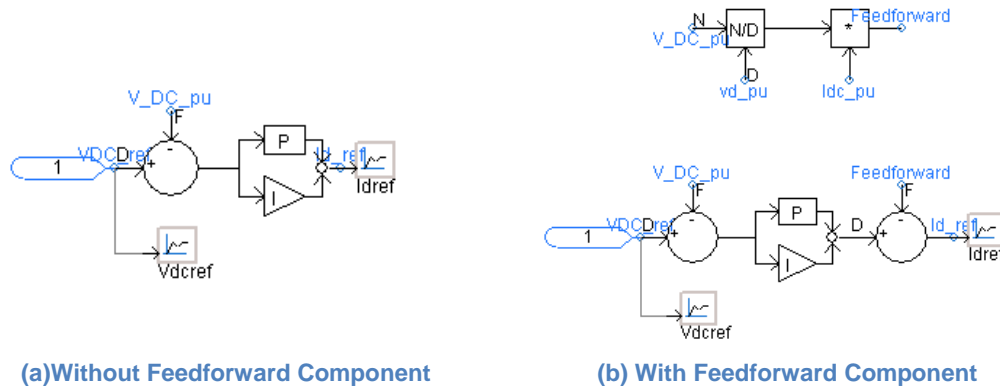
(a)Without Feedforward Component   (b) With Feedforward Component
Figure 2.13 DC Voltage Controller (Outer Loop)

PI parameters for the controllers are tuned according to "symmetrical optimum" method with linearization around the operating point for this nonlinear system [8]. The symmetrical optimum method ensures the maximum phase margin, so that it excels in robustness in systems with disturbance [11], such as the feed-forward component in this case.

Assume $\frac{T_{eq}}{T_a} = 2$, $a = \frac{T_{iv}}{T_{eq}} = 3$ as selected in literature [9], the results can be calculated as in Equation (2.12) and (2.13).

$$T_{iv} = a^2 T_{eq} = 9 \times \frac{1}{1800} = 0.005 \text{ s} \qquad\qquad \text{Eq. (2.12)}$$

$$K_{pv} = \frac{CZ_{base\,DC}}{\frac{v_{d,pu}}{v_{dc,pu}}\sqrt{T_{iv}T_{eq}}} = \frac{\frac{625}{2}\times10^{-6}\times\frac{400^2}{1000}}{1\times3\times\frac{1}{1800}} = 30 \qquad\qquad \text{Eq. (2.13)}$$

Furthermore, a saturation block is implemented in PI regulator to limit the current to +/-1.5 p.u..

Active and Reactive Power Controllers

Since v_q=0, in p.u. system active and reactive power can be expressed as in Equation (2.14) and (2.15). As a result, a set of decoupled PI regulators are implemented to feed the current reference value in dq-system (i_d* and i_q*) for ICC, as shown in Figure 2.14. For PI tuning, literature [4] suggests that the same pair of parameters used for DC Voltage controller could be applied for active and reactive power controllers too, which is adopted in the case.

$$P = v_d i_d + v_q i_q = v_d i_d \qquad\qquad \text{Eq. (2.14)}$$
$$Q = v_q i_d - v_d i_q = -v_d i_q \qquad\qquad \text{Eq. (2.15)}$$
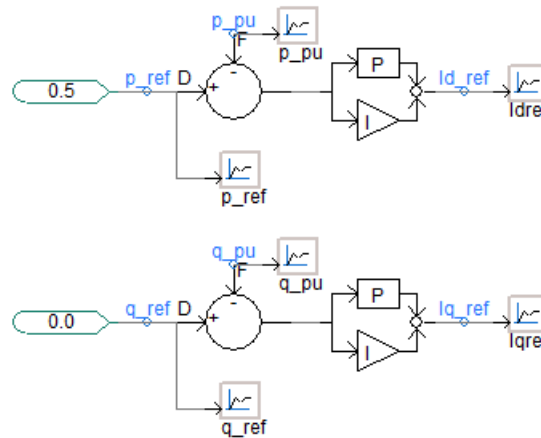
Figure 2.14 Active and Reactive Power Controllers (Outer Loop)

2.4 Cable Configuration

One of the distinguished strength of PSCAD/EMTDC over other simulation software is its advanced and accurate cable modeling, especially in transients. This section describes in detail the cable configuration in PSCAD/EMTDC environment for the system.

As mentioned before, only symmetrical monopole topology with grounded midpoint is adopted in the model, as shown in Figure 2.15. Due to the symmetry of the system, the two cable systems connecting A1&C1 and A1&C2 are designed as identical. *Frequency Dependent (Phase)* model option is selected, which is acknowledged as the most advanced time domain model available so far, and is proved in [12] to be in better agreement with experimental data compared with *Frequency Dependent (Mode)* model.
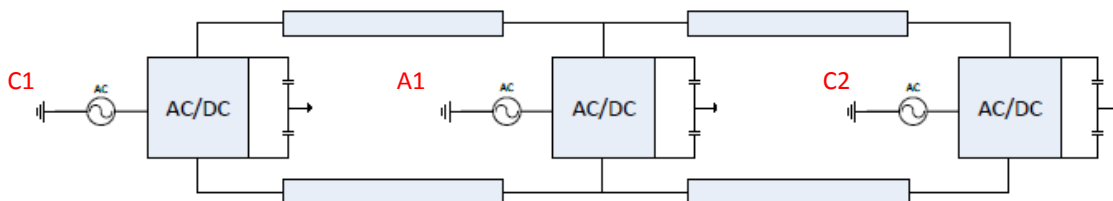
Figure 2.15 Symmetrical Monopole with Grounded Midpoint in 3-terminal MTDC System (taken from [16])

According to CIGRE B4 DC Test benchmark, Cable A1C1 is a 200km, +/-200kV submarine cable, with the max current of 1962A [6]. According to the datasheet given in [13], the ABB submarine cables with 1400mm^2 copper conductor in spaced laying in moderate climate could be selected in this case. Moreover, the diameter is set as 130mm considering the voltage level it should withstand, and the burial depth is set as 1m (as in [13]). Further technical data of such cables can be looked up in [14], which results in 24.0mm in cross linked polyethylene (XLPE) insulation (layer 1) thickness, 3.1mm in Lead sheath thickness and 5mm in Copper armor thickness. The relevant snapshots of the ABB datasheet and assumptions are presented in _Appendix C_. The semiconducting layers between insulation and core as well as between insulation and sheath, however, are not implemented in the model. To compensate for this, permittivity of the insulation has been slightly modified [15]. Two other insulator layers of XLPE and PP also exist between sheath & armor and outside armor layer [15]. Assume that these two insulator layers have the same thickness, which can be calculated as in Equation (2.16) and (2.17). In summary, the cable cross section is shown as in Figure 2.16 with the parameters set as in Table 2.9.

$$r_{conductor} = \sqrt{\frac{1400}{\pi}} = 21.2 \text{ mm} \qquad\qquad \text{Eq. (2.16)}$$

$$d_{insulator2} = d_{insulator3} = \frac{\frac{130}{2} - 21.2 - 24 - 3.1 - 5}{2} = 5.85 \text{ mm} \qquad \text{Eq. (2.17)}$$

Table 2.9 Cable Cross Section Parameters

Layer	Material	Thickness/Radius [mm]	Outer Radius [mm]	Resistivity [Ω*m]	Relative Permittivity	Relative Permeability
Conductor	Copper	21.2	21.2	1.72e-8	1	1
Insulator 1	XLPE	24.0	45.2	--	2.3	1
Sheath	Lead	3.1	48.3	2.2e-7	1	1
Insulator 2	XLPE	5.85	54.15	--	2.3	1
Armour	Copper	5.0	59.15	1.72e-8	1	1
Insulator 3	PP	5.85	65	--	2.1	1
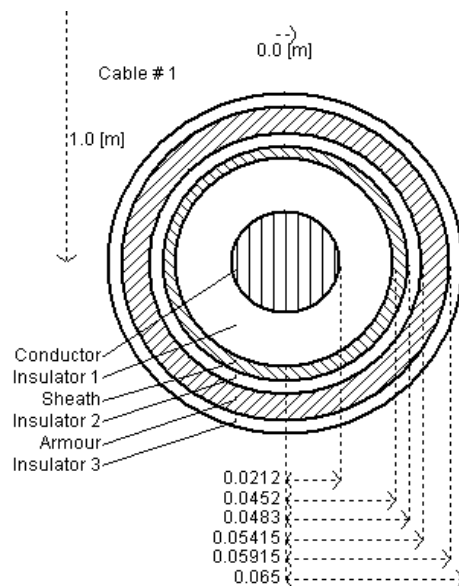
Figure 2.16 Cable Configuration

15

2.5 Simulation and Model Validation

Now that the electrical part and control part for each terminal are established, as well as the submarine HVDC cables configured, a testing simulation is conducted to validate the model performance. The simulation scenario is set as follows:

- Firstly, the reference of active power for all three VSC stations ramps up to nominal value of each terminal as indicated in literature [6], while that of reactive power remains zero.
- After it enters the steady state in operation point, the reference settings pair of VSC_C2 varies to several different values as shown in Table 2.10. Here the active power reference changes linearly while the reactive power reference changes in step function. All the other reference values in the two other VSC stations keep unchanged throughout the simulation.

Table 2.10 Reference Value Configuration for VSC_C2 in Load Change Study

Time [s]	Pref [p.u.]	Qref [p.u.]
0 - 0.1	0->0.5	0
0.1-0.3	0.5	0
0.3-0.5	0.5	0.1
0.5-0.7	0.5	-0.1
0.7-0.8	0.5->0.3	-0.1
0.8-0.9	0.3	0
0.9-1.0	0.3->0.6	0
1.0-1.1	0.6	0
1.1-1.2	0.6->0.1	0
1.2-1.3	0.1	0
1.3-1.4	0.1->0	0
1.4-1.5	0	0

Note here although the rated power of VSC_C2 is 500MW (0.5 p.u.), the case of Pref=600MW is also conducted to set some safety margins in case of control failure. When Pref = 100MW or 300MW, the system is operating at a degraded setpoint. The reactive power reference is usually set as 0 to reduce the current, and thus the loss. Under some circumstances, the OWF might also need to either generate or absorb reactive power from the system. The simulation results of both control and electrical variables in each VSC station are presented in Figure 2.17 and *Appendix D*. In these figures, the positive direction for active/reactive power is assumed to be from AC grid to VSCs and from VSCs to DC cables, as in Figure 2.10. Based on the result, some conclusions are listed as below:

- The simulation results successfully validate the model and verify the control strategy in nominal operation point and load/production varying scenarios. This is the prerequisite of fault analysis to be introduced in the following chapters.
- During the steady state, the DC current flowing in DC cable is around 1.3kA, which is consistent to the calculated value in Equation (2.18).

$$I_{DC} = 500MW/400kA = 1.25kA \qquad \text{Eq. (2.18)}$$

- Since A1 is not controlling the active power, it is responsible for compensating the transmission loss in the system, similar to the slack bus in power flow analysis. According to the measured active power detected at A1, the efficiency of the system at the nominal operational point is around 97%.

- For the described start-up setting, the MTDC system enters steady operational point before 0.3s. Therefore, it is acceptable to simulate the first variation in load at t=0.3s. In the following chapters, the load is assumed constant, but similarly the short circuit fault needs to be implemented after the system enters the stable steady state.
- The active power and reactive power follows the reference value well.
- As VSC_A1 is controlling DC voltage (which usually remains constant), the DC voltage remains almost constant of the nominal value of 400kV throughout the power variation.
- As the DC voltage remains almost constant, DC current will change with the active power. Therefore, it might be tricky for the relays relying on current-signal to distinguish faults from a change in load.
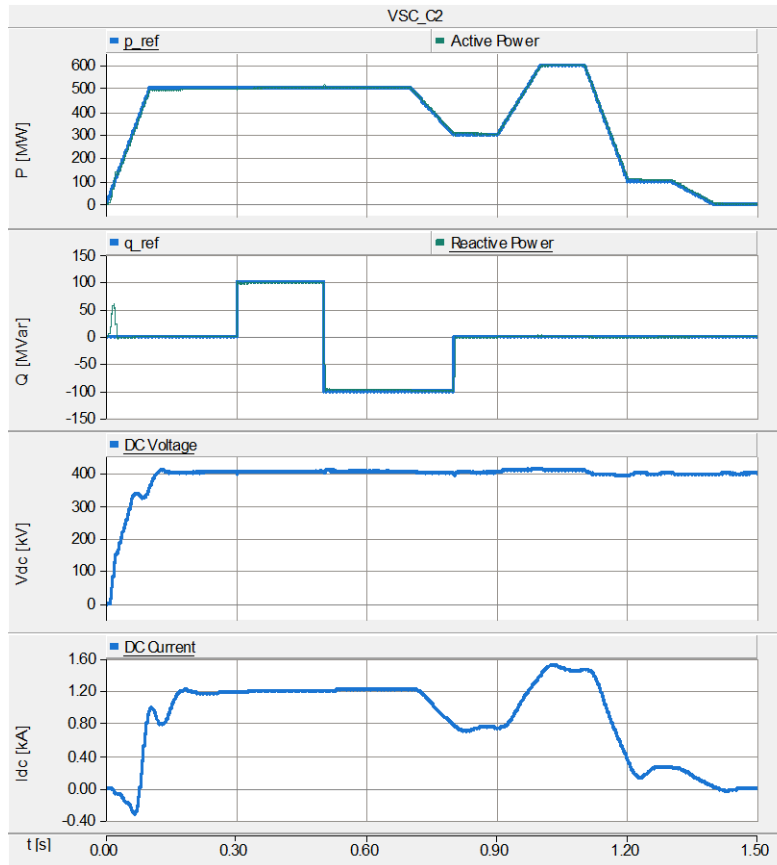
Figure 2.17 Simulation Results of VSC_C2

2.6 Summary and Discussions

This chapter focuses on the modeling of the target VSC-MTDC system in PSCAD. It begins with the system description, specifying the assumptions and simplifications. Then the electrical part of each terminal is introduced component-wise with more details about the sizing, followed by the controlling principle and PI tuning for each controller. Cable configurations are defined by looking up the manufacturer datasheet as well as the data from the literature. To verify the model, a simulation was conducted based on which a series of conclusions are obtained and listed. The model presented in this chapter works as the basis for the remainder of this project in which cable short circuit faults, fault detecting, current limiters and the proposed protection scheme will be implemented.

Chapter 3 DC Cable Short Circuit Study

As mentioned earlier in Chapter 1, VSC-HVDC is very vulnerable to DC faults and requires corresponding protective measures. To better identify fault consequences and protection requirements, the system transient during cable short circuit is studied in this chapter. Literature [3] specifies and defines three stages during the DC cable fault response based on the π-equivalent cable model. Taking the distributed parameters and the frequency dependent (phase) cable model into consideration, the travelling wave theory is also introduced in this chapter. After the theoretical analysis, a set of fault scenarios are conducted in PSCAD simulation, based on which some conclusions are drawn. Finally, the chapter ends with summary and discussions.

3.1 Introduction

Unlike conventional HVDC technology where the DC fault current can be successfully suppressed by converters and smoothing reactors, VSCs are highly vulnerable to DC faults, such as DC link short circuits, DC cable short circuits, DC cable ground faults, etc. Among them, cable fault usually occurs more often than in other parts of the system, mainly caused by insulation deterioration or breakdown, electrical stresses, environmental conditions, aging and physical damage [3].

There are three types of cable faults from DC side in a symmetrical monopole cable system:

- Positive line to ground fault
- Negative line to ground fault
- Positive line to negative line fault

Since the system is symmetrical, the first two types can be combined into the same category called *DC cable ground fault,* or pole-to-ground fault, while the third called *DC cable short circuit* or pole-to-pole fault.

DC cable short circuit, though less common than the other type, can cause the most serious problems to VSC. While the IGBT could be blocked for self-protection, the fault current can still flow through the freewheeling diodes, acting as an uncontrolled bridge rectifier [4]. This will be a threat to the diodes, the DC cables as well as the whole MTDC system.

3.2 Fault Response based on Lumped Cable Models

In literature [3], a solid DC cable short circuit fault (R_f=0) in VSC-HVDC system is analyzed in detail where the cables are simply modeled as the π-model equivalent resistance (R) and inductance (L) in series while the grounding capacitors are omitted, as depicted in Figure 3.1 (a). Throughout the response after a pole-to-pole fault occurs, three stages are defined in [3], the equivalent circuit of which are expressed in Figure 3.1 (b):

- Stage 1: capacitor discharge stage, where the DC capacitor get discharged through the fault
- Stage 2: diode freewheel stage, where IGBTs are blocked for self-protection and the freewheeling diodes work as uncontrolled bridge rectifier
- Stage 3: grid current feeding stage, where AC grid feeds the fault via diodes path

Literature [3] further presents the complete fault response divided into the corresponding three stages in Figure 3.2, where the voltage of the capacitor (VC), the current flowing through the DC cable (I_cable), the capacitor (I_C), the VSC station (I_VSI), the diodes (I_D1, I_D2 and I_D3) and the AC grid side (Iga, Igb and Igc) are given. Based on the figure, it is eventually put forward that the second stage is the most challenging stage in protections when the freewheeling diodes are forced to flow an abrupt and devastating overcurrent with high initial value.

Literature [3] also points out that the dc cable short circuit fault response can be featured by two factors:

- Critical time limit (t_c), which is the time duration for the DC voltage drops to zero, as t_1 in Figure 3.2.
- Total freewheel overcurrent value (i_{cable}), which is the cable current at the critical time.

Literature [3] further gives the mathematical expressions for the critical time as well as the fault overcurrent throughout the entire process, as presented in *Appendix E*. With these two factors determined, the action time demand in protection scheme can be determined too. In addition, they can also be used to indicate the fault distance, as shown in Figure 3.3. Therefore, such information could be utilized in relay settings as well.

(a)

Stage 1 : Capacitor Discharge Stage

Stage 2: Diode Freewheel Stage

Stage 3: Grid Current Feeding Stage

(b)
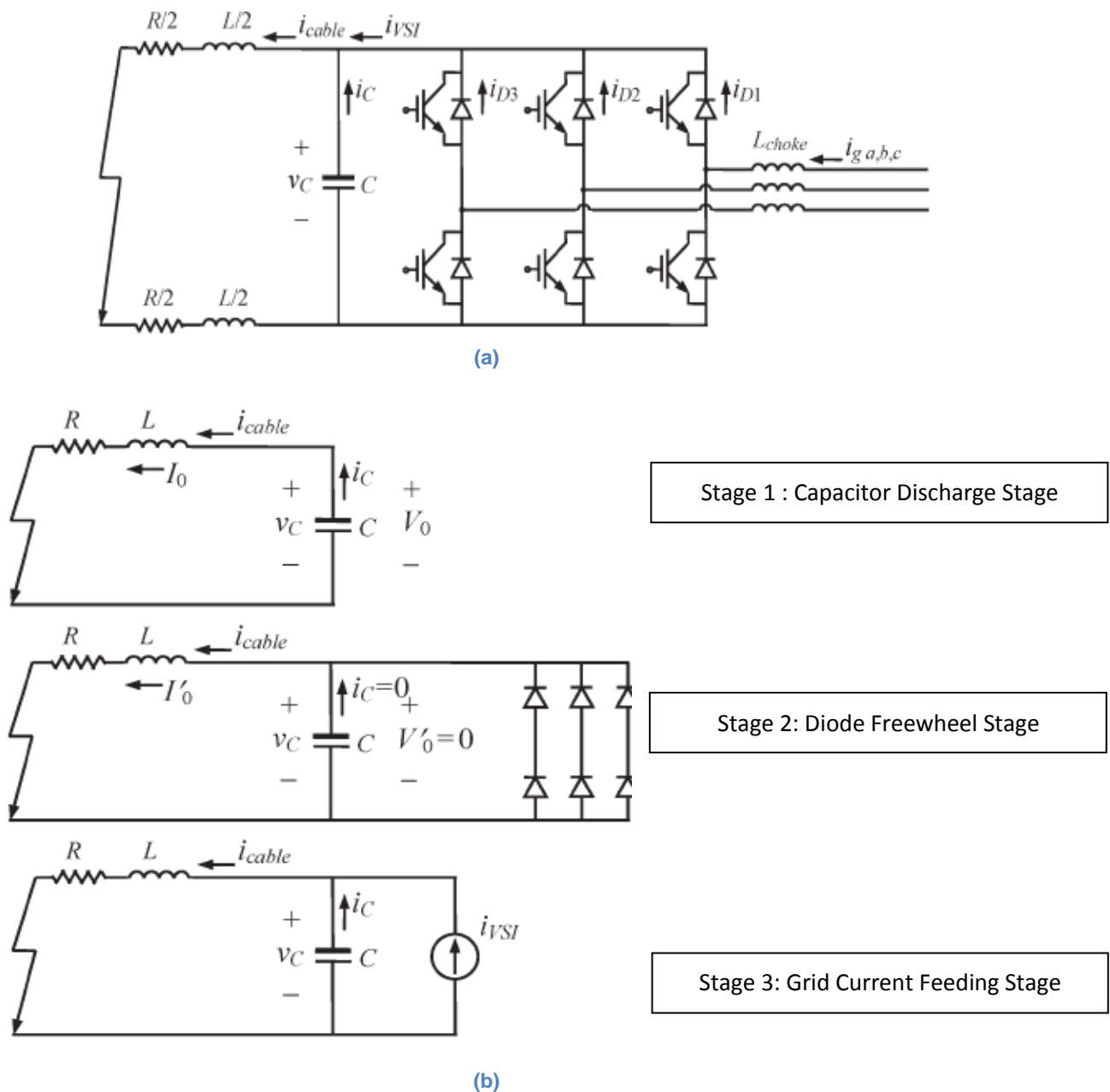
Figure 3.1 Cable Short Circuit Fault Equivalent Circuits for
(a) the whole model; (b) each of the three stages (taken from [3])

19
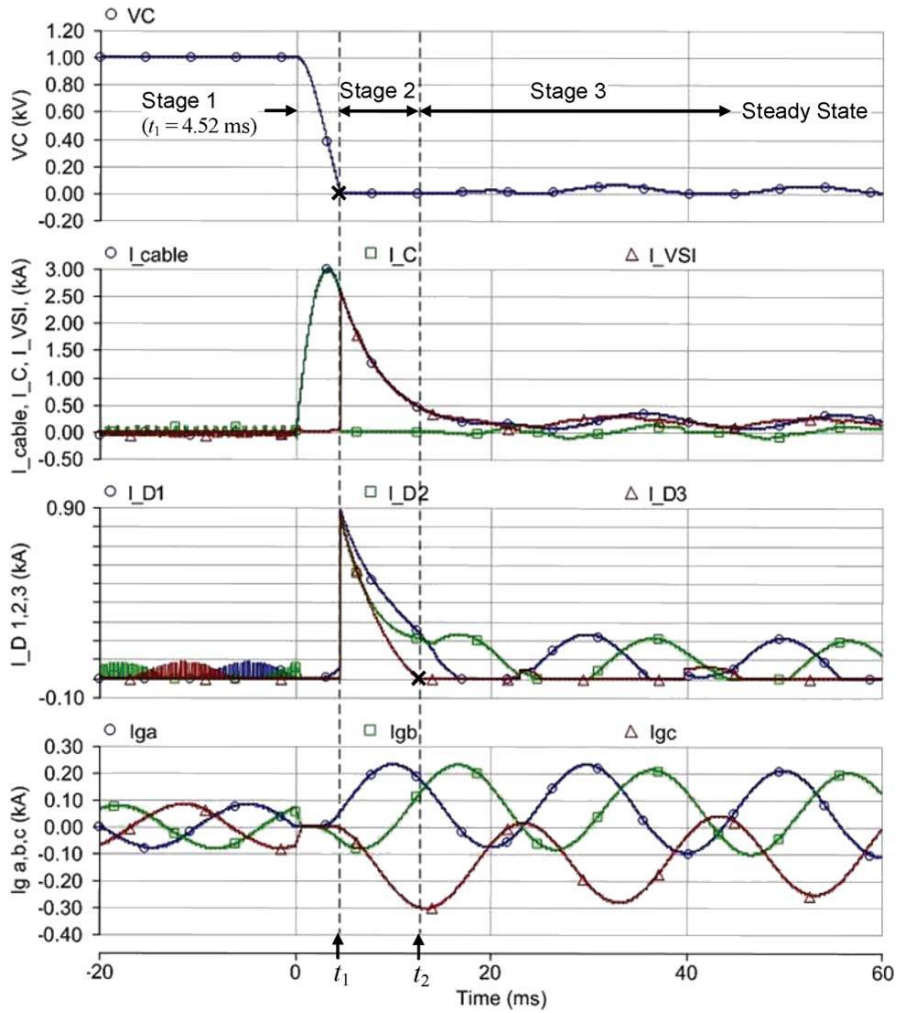
Figure 3.2 Fault Response in VSC DC Cable Short Circuit (taken from [3])
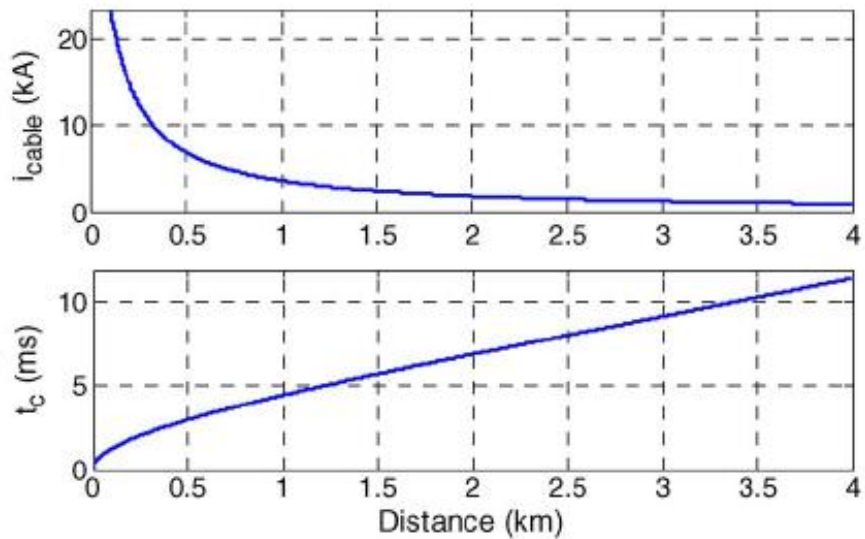
Figure 3.3 Total Freewheel Overcurrent and Critical Time with Different Fault Location (taken from [3])

3.3 Travelling Wave Effect

In the previous section, the cable is modeled in lumped parameters as R and L. However, for long submarine cables, it is usually more appropriate to consider the distributed parameters. Therefore, the travelling wave effect needs to be considered, which will be described in this section.

According to the travelling wave theory, the occurrence of a fault triggers a wave to travel along the cable in both directions away from the fault. Once the wave reaches the converter stations at the end of the cable, it will be reflected and refracted according to the reflection and refraction coefficients. Such coefficients are ultimately determined together by the character impedance of the cable and the equivalent impedance of the converter station. For example, if a wave is travelling from the cable (character impedance Z_1) to a VSC station (equivalent impedance Z_2), the reflected and refracted voltage and current are given in Equation (3.1) – (3.4). Thereafter, the reflected wave at the converter station travels back to the faulty point, and once again the similar phenomena of reflection and refraction phenomena occur there.

$$v_{reflected} = \frac{Z_2 - Z_1}{Z_2 + Z_1} v_{incident} \qquad \text{Eq. (3.1)}$$

$$i_{reflected} = \frac{Z_1 - Z_2}{Z_2 + Z_1} i_{incident} \qquad \text{Eq. (3.2)}$$

$$v_{refracted} = \frac{2Z_2}{Z_2 + Z_1} v_{incident} \qquad \text{Eq. (3.3)}$$

$$i_{refracted} = \frac{2Z_1}{Z_2 + Z_1} i_{incident} \qquad \text{Eq. (3.4)}$$

Figure 3.4 is a lattice diagram indicating the general idea of voltage wave reflection and refraction in a lossless case with open terminals at each end, where reverse and forward wave denoted as r and f and the reflection coefficients at each converter station as k_A and k_B [16]. Similarly, the current caused by the DC fault also travels along the cable with reflections and refractions, so that the step-wise increase will be detected in fault current development. With losses taken into consideration, literature [16] also shows the development of fault current measured at the converter station as in Figure 3.5, where τ represents the time for the wave to travel from fault to the converter station and k_n (n=1,2,…) the damping variable accounting for the attenuation. Such information will be useful in fault locating which will be introduced in more details in Chapter 4.
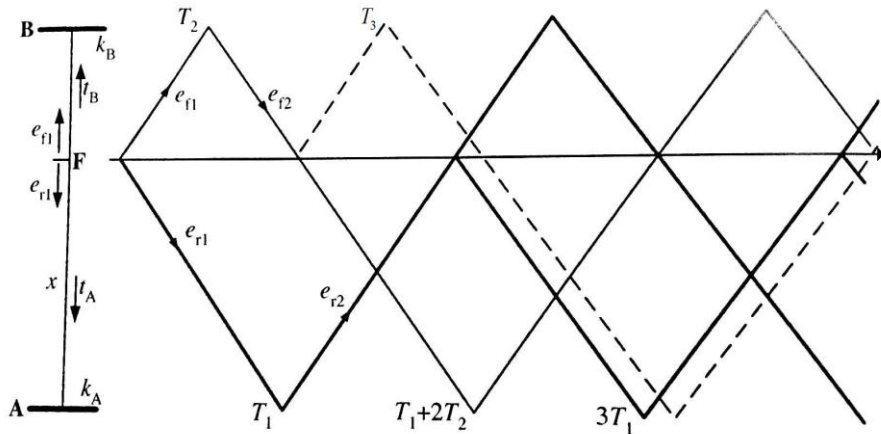
Figure 3.4 Lattice Diagram within Two Converter Stations and Fault Point (taken from [16])
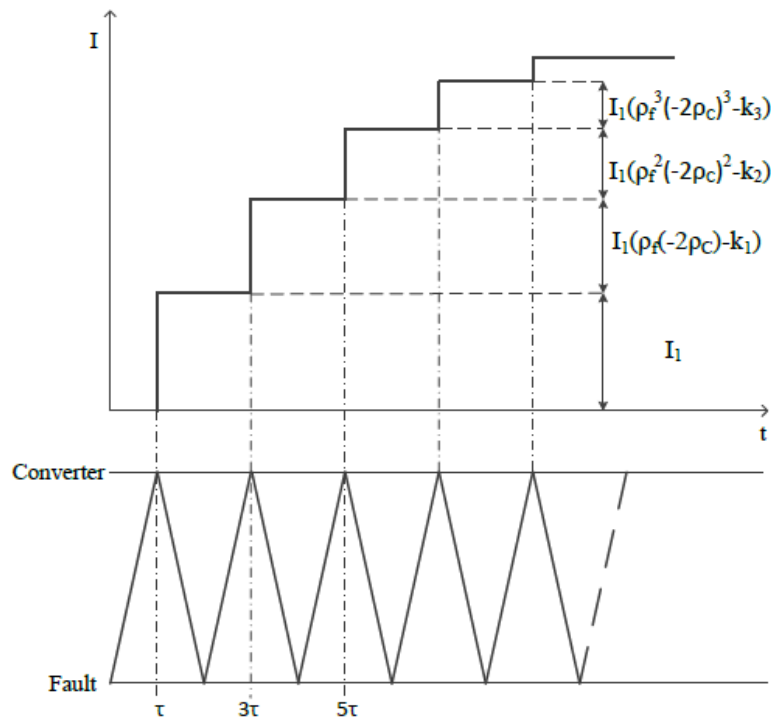
Figure 3.5 Fault Current Development at the Converter Station (taken from [16])

3.4 Fault Simulation

Due to the symmetry of the model, the short circuit fault is only simulated in Cable A1C2. To implement the faults with various locations in a handy way, Cable A1C2 is modeled as two segments of d and (200km-d) in length that connected in series, with an extra 'Fault' block set in between, as shown in Figure 3.6. The fault is configured as a permanent, solid (Rf=0) pole-to-pole fault occurring at t=1.0s, when the start-up transient has been faded away long before. Moreover, IGBTs will be blocked for self-protection when the cable current exceeds 13kA as indicated in [4].
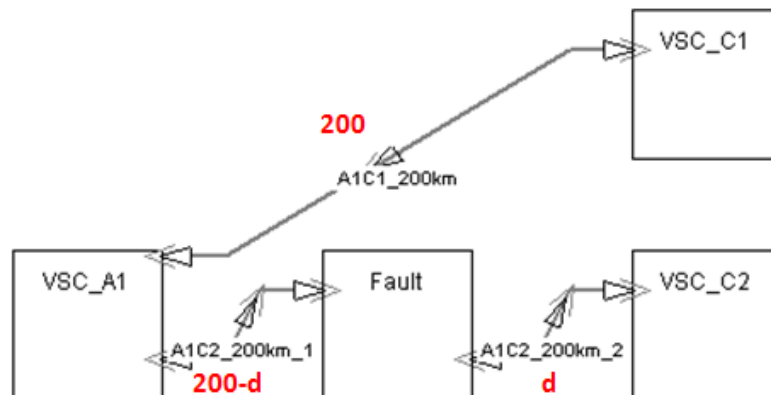
Figure 3.6 System Overview after Fault Implementation

Extensive simulation work has been conducted, which produces a great amount of plots. Only the results of short circuit analysis at VSC_C2 during a fault which is 1km away from VSC_C2 (d=1km) is shwon here as in Figure 3.7. Compared to what is presented in Figure 3.2, the shapes for the measurements look alike. Plus,

22

the currents flowing through the IGBTs (iIGBT1, iIGBT2 and iIGBT3) are also shown to illustrate the blocking of IGBTs during fault situations.

As can be observed from the figures, the insant when the capacitors are fully discharged (v_{DC}=0, at the start of 2nd stage), an abrupt overcurrent occurs in diodes, putting them at stake. In this specific case, the _critical time limit_ is 0.8ms and _peak fault overcurrent_ is around 222kA. This justifies the necessity for DC protection. An instictive idea will be either to isolate the fault within the _critical time limit_ or to reduce the _peak fault overcurrent_ with fault current limiters. This validates the theory described in section 3.2 as put forward in [3, 17].
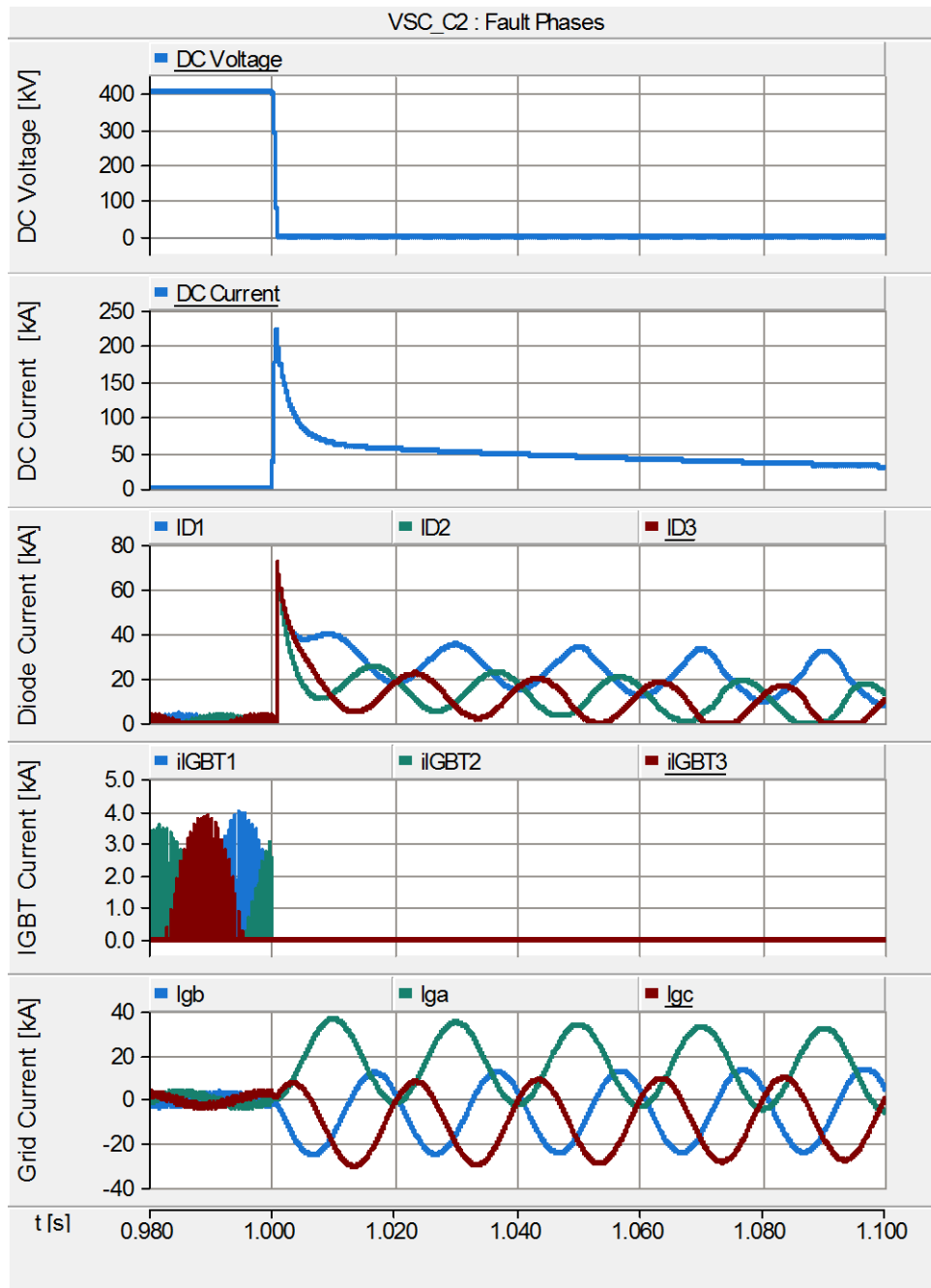
Figure 3.7 DC Cable Short Circuit Study of VSC_C2 (d=1km)

Afterward, DC cable short circuit faults with different distances to VSC_C2 (d) as 1km, 10km, 100km, 190km, 199km are simulated in Cable A1C2 (l= 200km) at t=1s. The results of DC voltage and DC current

23

detected at VSC_C2 in different sceniros are grouped in Matlab plots, as presented in Figure 3.8. It can be concluded that the closer the fault is to VSC_C2 station, the shorter the critical time and the larger the overcurrent magnitude, thus the more vulnerable the station and the cable connected to it will be. Besides, except for d=1 km or 10km, the DC voltage at VSC_C2 will not drop to 0. In this way, the most severe fault current overshoot is somewhat avoided. Actually, it can be further found out that no distinughishable 'stages' can be recognized from the complete fault response in these cases. On the other hand, the critical times for d=1km and 10km are 0.8ms and 2.2ms respectively. Also, when zooming in the fault current upon the fault moment, the travelling wave effect in DC current flowing out of VSC_C2 when d=1km and 10km can also be clearly observed in Figure 3.9, as the current is rising in a stepwise way.

(a)

(b)
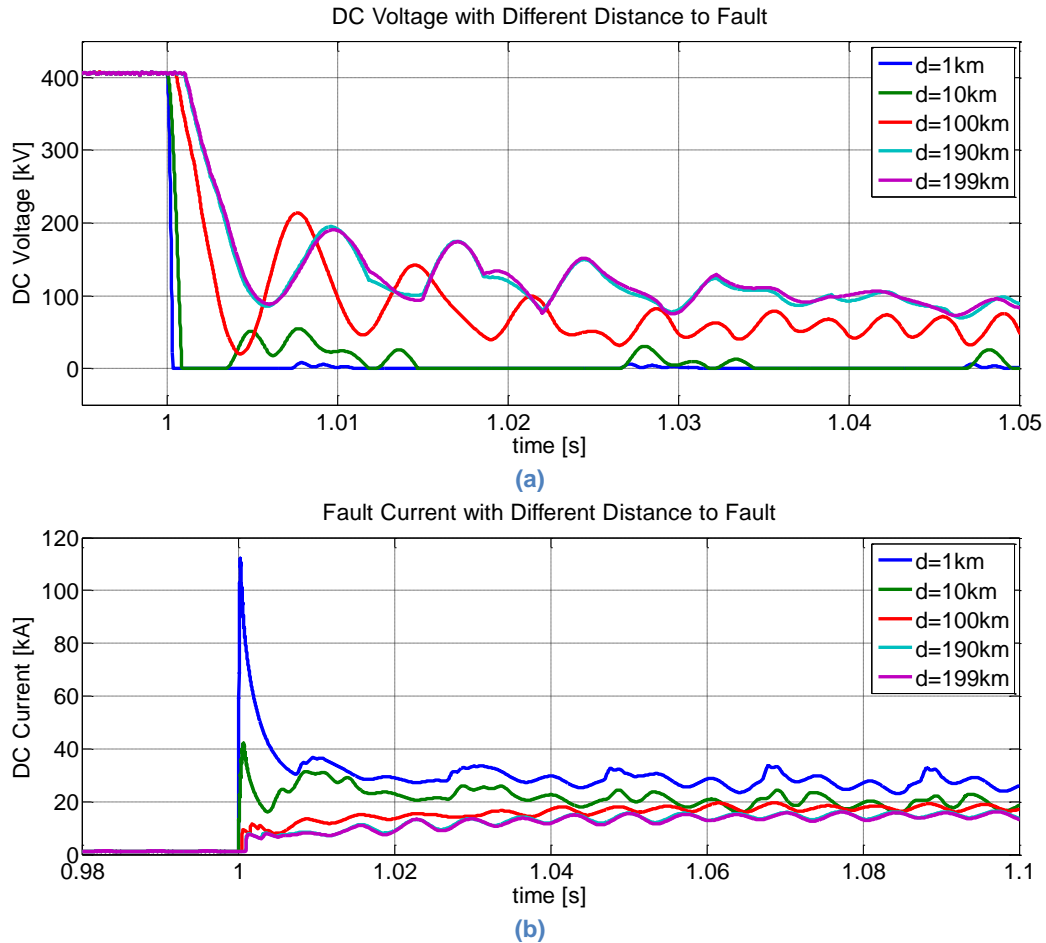
Figure 3.8 (a) DC Voltage and (b) DC Current at VSC_C2 during Faults with Different Locations
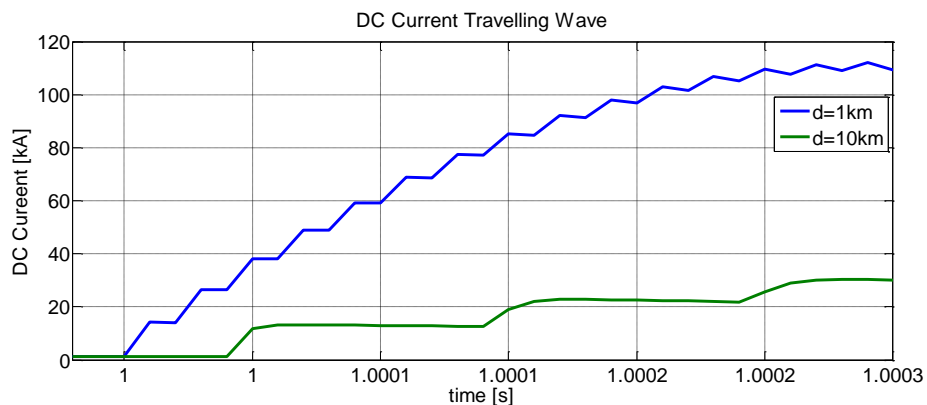
Figure 3.9 Travelling Wave Effect in DC Current Detected in VSC_C2

24

Apart from different fault locations, the impacts of various DC capacitance and fault impedance are also studied. Only the conclusion will be provided here: smaller DC capacitance or smaller fault impedance results in shorter critical time and larger overcurrent magnitude, which indicates a more severe situation.

3.5 Summary and Discussions

In this chapter, the DC cable short circuit fault study is illustrated in both theory and simulation. The conclusion indicates that the fault should be cleared before the *critical time* to protect the system from the *overcurrent.* In other words, the key in DC cable short circuit fault protection is to isolate the fault before the current exceeds the maximum current the components (such as the diodes) can sustain. This means that the DC faults have to be cleared within a few milliseconds, with fault detection, fault localization and fault isolation included [18]. However, such requirements cannot yet fully be satisfied by the existing technology [4, 16]. Therefore, more efficient and reliable fault detecting/locating methods have to be proposed, and fast fault isolation tools need to be designed and tested. Another possible solution is to limit either the magnitude or the derivative of the fault current to a reasonable range by introducing fault current limiters. As a result, the time constraint for the protection system becomes less strict. Each of the possibility will be explored in more details in the chapters to follow.

Chapter 4 Fault Detecting & Locating Principles

As mentioned at the end of the previous chapter, in an attempt to protect the system from overcurrent during a DC cable short circuit fault, three possible directions are put forward:

- Efficient fault detecting and locating principles
- Fast fault isolation devices – DC breakers
- Effective fault current limiting technologies

In this chapter, the first aspect will be discussed while the other two in Chapter 5 and 6 respectively. The chapter introduces both the conventional protecting relays as employed in HVAC as well as more innovative techniques based on the wave transients. Among the large amount of plots generated in the simulations, only the ones in the case when d=10km are selected to represent the principle of each detecting and locating method. Besides, the measured/processed data in different fault scenarios are also summarized in tables for each detecting/locating method.

The simulation time is set as 1.1s while the fault occurs at t=1.0s. The time length is determined based on the assumption that the AC breakers will clear the faults within 100ms even when there is no effective protection from the DC side.

4.1 Introduction

Rapid fault detecting strategy is a prerequisite for the DC protection scheme. It aims to detect if there is a fault, discriminate which is the faulty part, determine which breakers to trip and send them such signals. This is realized by the protection relays.

Fault locating is to estimate the exact fault location in the faulty line. Although this is not compulsory in the protecting scheme, fault locating is still significant and essential in DC cable short circuit since these faults are almost always permanent and require repairs later on. In this circumstances, it is usually assumed that the faulty line has already been determined and isolated from the system. As a result, speed is no longer the highest priority in this condition, and that the data is usually processed offline. However, it is always desirable that the fault location can be estimated only with the data which have already been obtained during the fault.

When it comes to the signal selection, usually both DC current and DC voltage signals can be used. However, in the system studied in this project, the voltage is controlled by VSC_A1. Therefore, the voltage signals cannot distinguish the faulty line from the healthy line when the fault occurs close to VSC_A1, as shown in Figure 4.1 when d=199km. Also, for fault locating, DC voltage signals are not competent either. The DC voltage of VSC_C2 and the DC current flowing out of VSC_C2 during the fault when d= 1km, 10km and 100km are given in Figure 4.2. The figure shows that while the travelling wave effect can be represented in the stepwise increase in the DC current, the DC voltages do not have the similar indications. This can also be verified according to the theory. Since the impedance of the VSC station is assumed to be much less than that of the cable (almost an ideal voltage source), the voltage reflection coefficient is nearly -1. Therefore, the surge will not be clearly visible in the DC voltage at the converter station terminal [19]. Plus, current travelling waves can be extracted by a cost effective design based on a conventional current transformer [20]. As a summary, only the DC current will be the object signals fault detecting and locating in HVDC DC cable short circuit. More specifically, the five currents listed below will be measured; the measurements as well as their positive directions are indicated in Figure 4.3.

- Current flowing out of VSC stations A1 denoted as data A1
- Current flowing out of VSC stations C1 denoted as data C1
- Current flowing out of VSC stations C2 denoted as data C2

- Current flowing out of VSC_A1 into cable A1C1 denoted as data A11
- Current flowing out of VSC_A1 into cable A1C2 denoted as data A12

Moreover, some detecting and locating methods also require communications, so a fiber optic channel is added along with each cable where the signal travels at 200km/ms as suggested in [21].
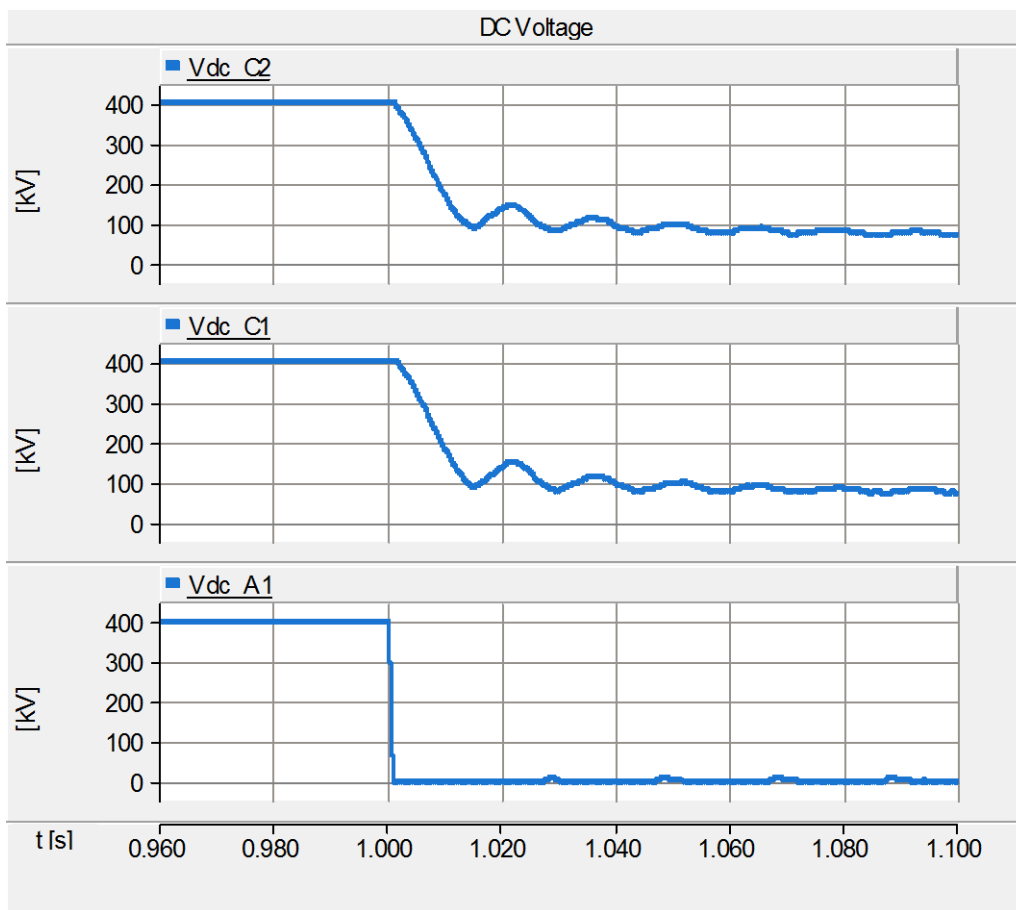
Figure 4.1 DC Voltage at Different VSC Stations (d=199km)
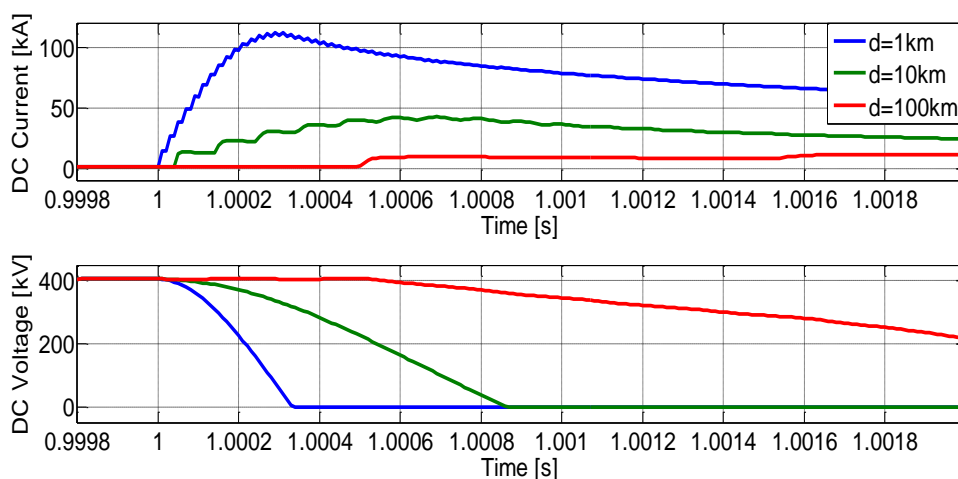
Figure 4.2 DC Current and DC Voltage at VSC_C2 with Different Fault Locations

27
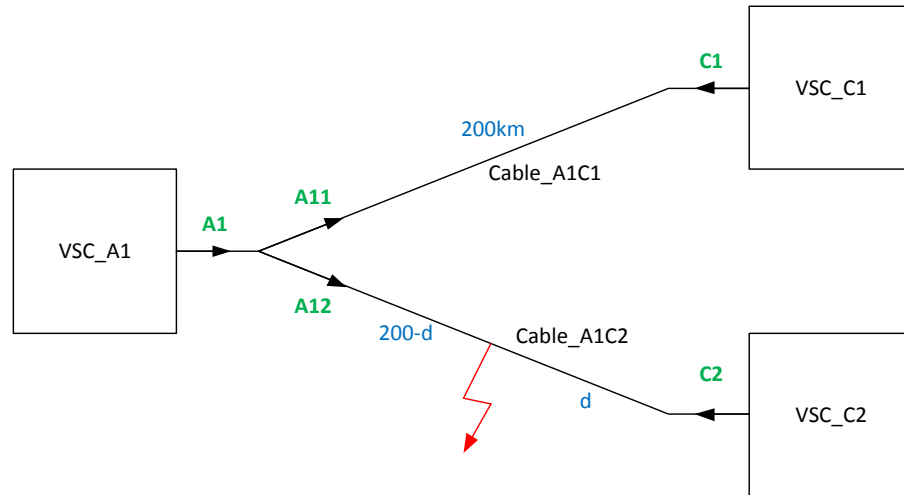
Figure 4.3 System Overview and Current Measurements (in green)

4.2 Fault Detection with Conventional Protecting Relays

There are a number of techniques used in HVAC protection, such as overcurrent protection, differential protection, distance protection, etc. Since the calculated 'complex impedance' in HVDC system does not have the same indication as in HVAC system, distance protection cannot be directly used under this circumstance. However, both overcurrent protection and differential protection can be implemented in the situation without significant change. The details will be introduced in the remainder of this section.

4.2.1 Overcurrent Protection

Overcurrent protection is a mature technology and is widely in use in system protection. The working principle is very straightforward: the overcurrent relays measures the corresponding current and compares it to a given threshold. If the magnitude of the input exceeds the threshold, a fault signal is generated and will be transmitted to the corresponding circuit breaker(s) to isolate the fault.

As illustrated before in Chapter 3, the current rises to a huge magnitude during faults. For example, Figure 4.4 presents the five measured DC currents when d=10km. In order to set the threshold, it is necessary to know the peak current occurring to both the healthy and faulty lines during the fault. From the plot, one can read that the maximum current magnitude detected at C2, C1, A12, A11, and A1 during the simulation period is 75.37kA, 7.59kA, 26.34kA, 7.59kA and 19.09kA respectively. In addition, Chapter 3 also reveals that different fault locations do affect such current magnitudes: the closer the fault is to the measuring point, the higher the magnitude gets. The maximum DC current magnitudes measured at different spots in different fault scenarios throughout the 1.1s of simulation are summarized and presented in Table 4.1, based on which he following comments are made:

- When the fault occurs very close to VSC, the DC current is extremely high (highlighted in the table). Under such circumstances, fuses or instantaneous overcurrent relays can be used to clear the fault current quickly.
- For the fault occurring close to VSC_A1, the maximum current magnitude detected from VSC_C1 and VSC_C2 are close (marked in red), which indicates a lack of selectivity for such faults.
- Moreover, as described at the end of Chapter 2, the fault current is dependent on the power production generated from C1 and C2. Since the power production from offshore wind farm varies over the time, it

28

cannot be guaranteed that the lowest fault current is always higher than the highest operational current. Therefore, the protection system is sensitive to production/load variation and has low selectivity.

In summary, overcurrent protection is simple yet not selective, but might be used as secondary or final backup scheme, which is also suggested in [3, 16].
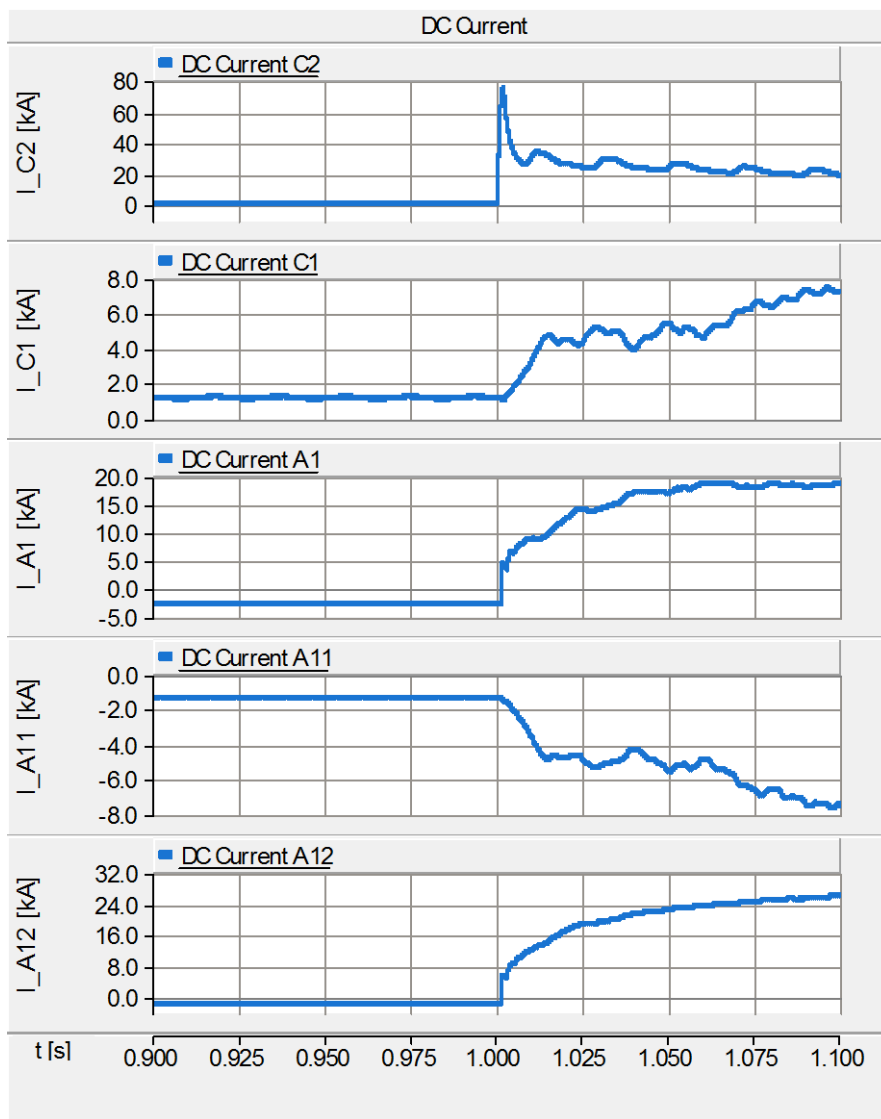
Figure 4.4 Fault Currents in Simulation (d=10km)

Table 4.1 Overcurrent Protection Study

		Maximum Fault Currents [kA]				
Distance from C2[km]		1	10	100	190	199
A1	A12	25.71	26.34	32.37	74.09	219.15
	A11	7.15	7.59	10.55	14.99	15.44
	A1	18.93	19.09	22.14	69.87	213.64
C2		222.11	75.37	18.71	15.70	15.45
C1		7.1	7.53	10.48	14.94	15.38

4.2.2 Differential Protection

Differential protection is yet another technology that is in wide use for long. It measures the current flowing into or out of the cable from each side and adds them together to obtain the algebraic sum. According to the Kirchhoff's current law (KCL), during normal operation the sum of currents should be zero. In practice, various factors such as the communication delay, wave attenuation in long distance cables and measurement errors contribute to an offset in the algebraic sum other than zero. Therefore, an appropriate threshold needs to be set for selectivity.

From the description above, differential protection is highly selective in detecting and seems very promising. However, in cases with long transmission lines, the differential protection causes a significant time delay in communication. While the time constraint is extraordinary strict in DC fault protection, this drawback of differential protection is often deemed as unacceptable or even fatal, especially in long distance transmission lines.

Fortunately, the cable in the target system is not extremely long (200km), and later in this section it will be proved that the communication delay in this case is still acceptable. Actually, literature [22] proposes that 200km is the limiting length for the cable length for today's communication technology, i.e. power lines, an independent Ethernet infrastructure, etc. [23]. Yet, this limit in length could be extended in the future [22]. In the target system, it is assumed that the data is transmitted through a fiber optic at 200km/ms as indicated in literature [21, 22]. As a result, it takes 1ms for the signal of one side to be received at the other side 200km away. To make the detection time as short as possible, it would not be desirable to leave out the precious newly updated transient data. Therefore, the i_sum should be the sum of the real-time local measurement and a history data of remote measurement. For example, the current sum detected at VSC_C2 (i_sum_C2) at the time of t_0 is the sum of the current flowing out of C2 (i_C2) detected at the time of t_0 and the current flowing out of A1 and into cable A1C2 (i_A12) detected 1ms before t_0, as in Equation 4.1. Similar definitions apply to the current sums i_sum_C1, i_sum_A11 and i_sum_A12 measured at C1, A11 and A12 respectively.

$$\text{i\_sum\_C2}(t_0) = \text{i\_C2}(t_0) + \text{i\_A12}(t_0 - 1\text{ms}) \qquad\qquad \text{Eq. (4.1)}$$

As an example, Figure 4.5 presents the DC current algebraic sum measured at A11, C1, A12 and C2 when taking the communication delay of 1ms into consideration. Due to the time delay, the sum from one side of the cable is not identical to that from the other side. More specifically, the maximum magnitude of current sum detected at A12, A11, C2 and C1 during the entire simulation period is 80.83kA, (-)0.698kA, 74.11kA and 0.48kA respectively. Moreover, the simulation results of maximum magnitude of DC current sum at different spots during the 1.1s of simulation with different fault distances are summarized and presented in Table 4.2. Some comments are made based on the results:

- Differential Protection provides an intrinsic selectivity [3]. The threshold can be set to distinguish the faulty line from the healthy line, for example 10 in this case.
- As can be seen from Figure 4.5, the maximum value in current sum reaches 10kA (threshold) at 0.6ms and 1.06ms after the fault occurs at C2 and A12 respectively. Both are shorter than 2.2ms, which is the critical time for d=10km. As for fault scenarios with larger d, the voltage does not drop to zero so the most vulnerable stage has been avoided [3]. However, when d=1km, the critical time is 0.8ms which is shorter than the communication delay. Yet, this can be further solved by using overcurrent protection as backup protection as introduced before.
- The maximum magnitude of sum detected at A11 are the same in cases of d=1km and 10km. This happens to C1 as well. This is due to the fact that when the fault is very far away from the detecting points, the transient during the fault is less significant than that during the start-up process. Actually, as

verified in the simulation data later, these two values of -0.698 and 0.48 are reached before the fault (t<1.0s).

- In reality, apart from the signal transmitting time, the time delay can also be caused by measuring, digitalizing and other data processing. This makes the time delay even longer.
- Except for the delay in time, communication will also result in less reliability caused by potential communication errors. To improve the reliability of the detecting system, protection based on other methods should be considered and included in fault detecting scheme.

In summary, differential protection provides a high selectivity, though this will be reduced to some extent in the long distance transmission due to communication delay and wave attenuation [16]. Besides, the dependence on communication also lowers the speed and reliability of the fault detection [16, 24]. Literature [5] also proposes a more robust cable directional protection where only current directions are recorded and transmitted, but it has the similar communication problems.
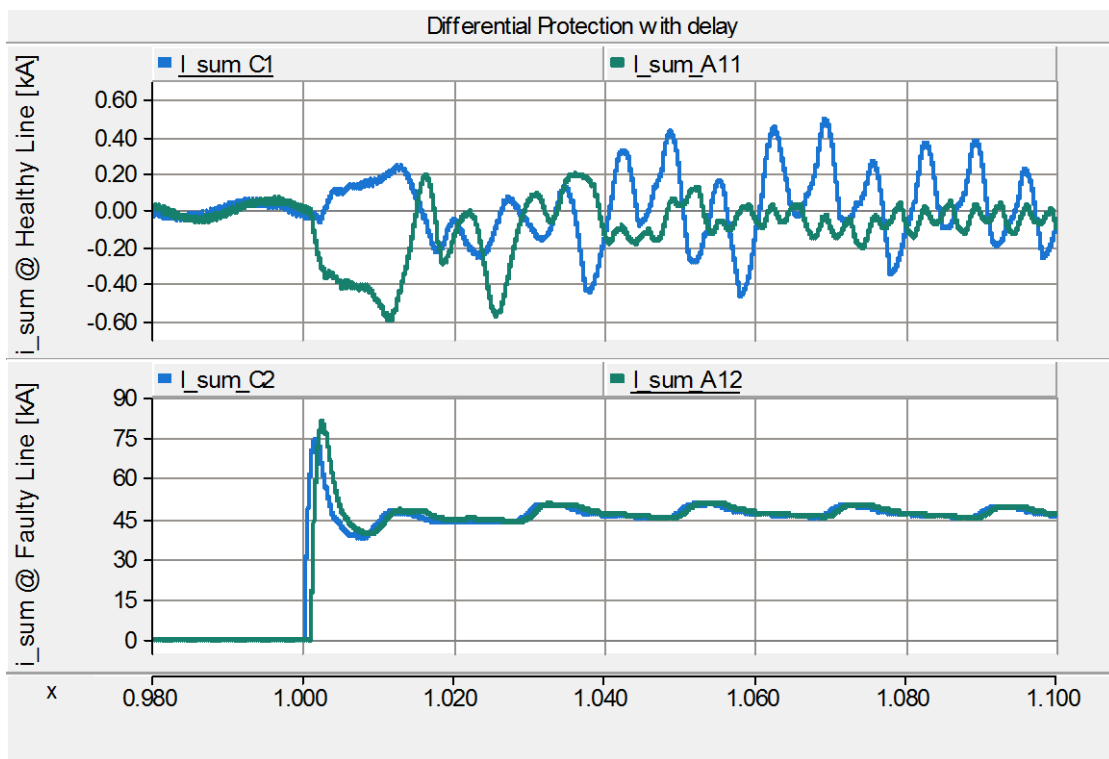
Figure 4.5 Current Differential Protection Study with Communication Delay (d=10km)

Table 4.2 Differential Protection Study

	Maximum I_sum Detected at Converter with Time Delay				
Distance from C2	1	10	100	190	199
A12(faulty)	227.90	80.83	49.67	76.09	220.43
A11 (healthy)	-0.698	-0.698	-0.91	-4.50	-5.40
C2(faulty)	220.86	74.11	49.64	81.87	227.36
C1 (healthy)	0.48	0.48	0.43	2.09	2.47

4.3 Fault Detection with To-be-developed Devices

To improve the performance of the protection system, a more selective and non-communication-dependent fault detecting method is necessary. Literature [5] suggests that the new, to-be-developed devices could possibly make use of the signal processing technique such as derivative or Fourier/Wavelet transformation. In this section, the following two types of new detecting methods will be introduced:

- Derivative-based fault detection
- Wavelet-based fault detection

4.3.1 Derivative-based Fault Detection

Fault detection based on current or voltage derivatives is useful in point to point HVDC protection [5]. It compares the weighted sum of the current derivative and voltage derivative to a given threshold and is able to detect the fault very fast [16]. The drawback of this method is that the setting of the weight and threshold is quite tricky. In the remainder of this section, only current derivatives are discusses, i.e. the weight of current derivative and voltage derivatives are set as 1 and 0 respectively.

During a fault, the current derivative of the faulty line is higher than that of the other part of the system. The derivative of the corresponding DC current can thus be compared with a given threshold for fault detection for discrimination. If the magnitude of the derivative exceeds the threshold, a trip signal will be generated and sent to the corresponding circuit breaker.

As an example, Figure 4.6 presents the DC current derivatives measured from both sides of the two cables (namely C1, A11, C2 and A12) in the simulation when d=10km. As can be obtained from the figure, the maximum current derivative magnitude detected at C2, C1, A12, A11 throughout the 1.1s of simulation period is 1046.4kA/s, 0.79kA/s, 123.64kA/s and (-)0.61kA/s respectively. The simulation results of maximum magnitude of DC current derivatives measured at different spots in other fault scenarios are furthermore summarized and presented in Table 4.3. Some comments are made based on the simulation results:

- In general, derivative protection is effective and fast for fault detection. However, it is very sensitive to noise and other scenarios, which impedes the reliability.
- The closer a fault is to the detecting point, the higher the derivative magnitude reaches and the sooner the derivative exceeds the threshold. This also complies with the requirements in the protection system: the closer the fault is to the station, the more vulnerable that station is and the shorter the reaction time should be.
- For selectivity, the threshold can be set as 15 for the system, or lower if coordinated with fuses or instantaneous overcurrent relays or other backup protection.
- Moreover, the polarity of derivative could indicate the direction of fault for VSC_A1, which helps with identifying the faulty line.
- The maximum magnitude of derivatives detected at A11 are the same in cases of d=1km and 10km. This happens to C1 as well. This is due to that when the fault is very far away from the detecting points, the transient during the fault is less significant than that during the start-up process. Actually, these two values of -0.61 and 0.79 are reached before the fault (t<1.0s).

In summary, derivative protection is a fast and mature technology, but is also sensitive to noise. Yet, it is capable of indicating fault directions which helps to improve the selectivity of the entire protection scheme.
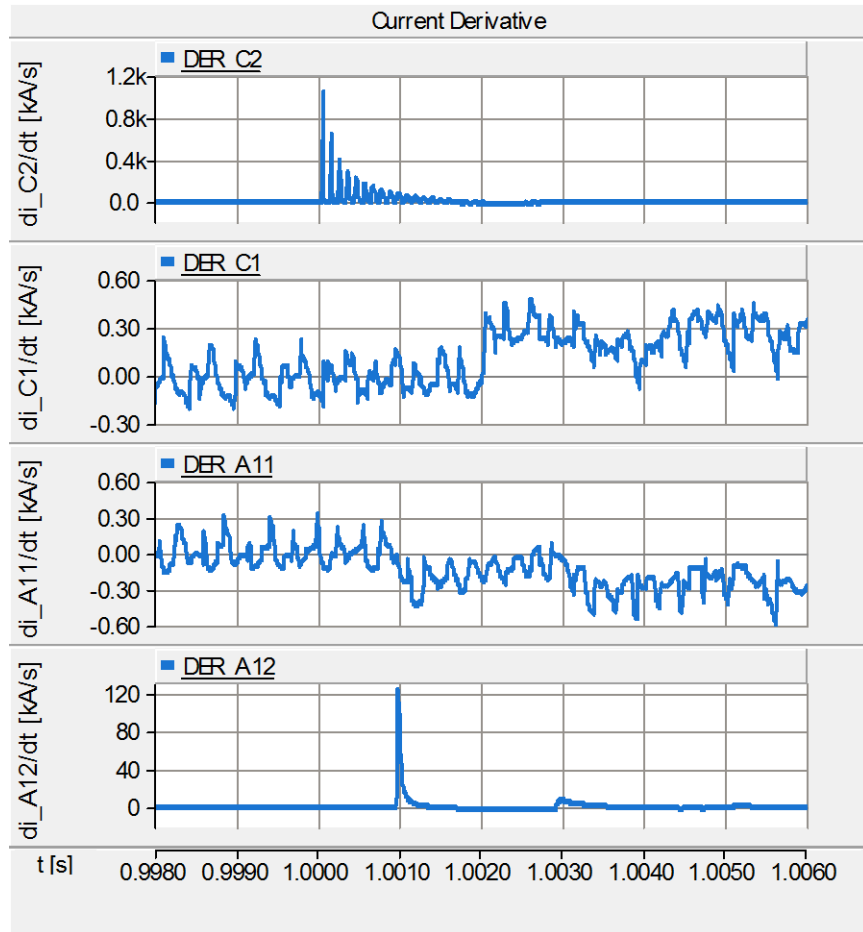
Figure 4.6 Snapshot of Fault Current Derivative around Fault Instant (d=10km)

Table 4.3 Maximum Current Derivative in Different Cases

		dI_DC/dt Maximum Magnitude				
D from C2		1	10	100	190	199
A1	A12	115.77	123.64	251.30	1031.31	1283.04
	A11	(-)0.61	(-)0.61	(-)0.77	(-)2.62	(-)8.87
C2		1302.2	1046.4	251.21	121.12	113.75
C1		0.79	0.79	0.83	3.93	11.51

4.3.2 Wavelet-based Fault Detection

As introduced earlier in Section 3.3, the transient waves caused by the fault will travel in both directions through the cable and be reflected at the VSC stations as well as the fault point till they attenuate to zero [16]. This can be detected and verified by the stepwise rise in current measurements. In other words, current transient signals contain information indicating the fault characteristics. Therefore, a fault can be determined by detecting the arrival of the fault-generated surge.

The detection of the wavefront caused by the fault can be performed with the help of the wavelet transformation. Actually, literature [25] describes wavelet analysis as 'a power signal processing method well suited to detect abrupt, local changes in a signal', such as faults. It further gives an introduction of the principle of wavelet analysis. The wavelet analysis uses a time-scale region rather than time-frequency one, in which the input signal is decomposed into different levels of output (wavelet coefficient) by a designated 'mother wavelet

φ'. These outputs or wavelet coefficients represent the correlation between the (scaled) wavelet and the signal [25].

In general, there are three types of wavelet transforms, with more details provided in *Appendix G*.

- Continuous Wavelet Transform (CWT), defined as the convolution of the signal and the scaled and shifted mother wavelet [25].
- Discrete Wavelet Transform (DWT), the discrete form of CWT.
- Stationary Wavelet Transform (SWT), also known as the time-invariant wavelet transform.

Each type has its own strengths and weaknesses and is adopted in different cases. Even in fault data processing, different preferences exist among different individuals. Generally speaking, CWT is both time- and memory-space-consuming, and is deemed not suitable in fault detection. However, literature [26] also points out that in off-line fault location (which will be introduced in the next section) CWT is more accurate and effective. DWT is, indicated by its name, in the discrete from. In this type, the wavelet transform is digitalized, making it more practical in fault detecting. Contrary to DWT, the translation parameter in SWT is a constant so that the transform obtained from different lines in SWT are compared without shift in time. As a result, the resulting wavelet and coefficients become time invariant [25]. Furthermore, SWT has inherent redundancy; it has wide applications in cases which require de-noising [27].

In this report, the focus is on the application of the wavelet transform. Therefore, the theory will not be given in more details. To implement the wavelet-based fault detection method in the built system, DWT is selected in this case and more specifically the model "Discrete Wavelet Transform (DWT)" provided by the PSCAD master library (as shown in Figure 4.7) will be added in the target system model.
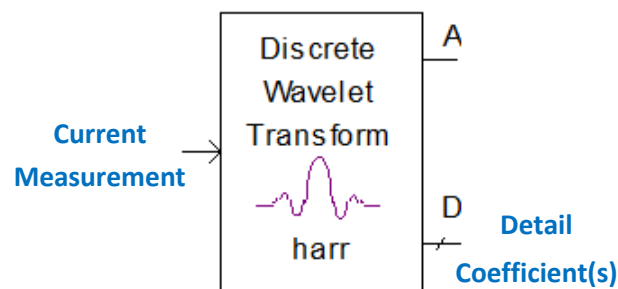
Figure 4.7 Discrete Wavelet Transform (DWT) Model in PSCAD

Here, the input of this block is the signal of current measured at the five different spots, namely C1, C2, A11, A12 and A1. Besides, there are three settings that need to be configured for the block,

- Sampling frequency: the frequency for digitalization. In this project, it is set as 100kHz, in consistency to the solution time step of 10µs.
- Mother Wavelet: a function which has zero average in a short duration of time and that decays fast at the edge [28]. Two types of widely used mother wavelet include:
  - Haar wavelet, shown in Figure 4.8, often recognized as the first known wavelet basis and has been used in many fields.
  - Fourth order Daubenchies (db4) wavelet, shown in Figure 4.9, which is deemed as a better alternative suggested in [29].

  Yet, in [32], a more scientific method of mother wavelet selection is introduced that is based on the minimum norm of the error between the original and reconstructed signal. However, this will not be considered in this project.

34
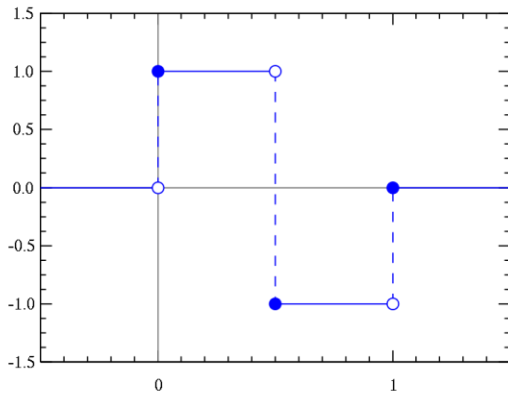
Figure 4.8 Haar Wavelet (taken from [30])
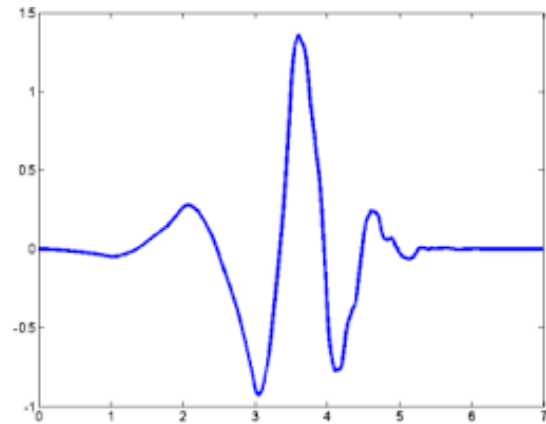
Figure 4.9 Db-4 Wavelet (taken from [31])

- Level: the level of detail to compute. In PSCAD, the level number can be set as up to 6, and '6 level' is selected in this project. In [20], the optimal level of the wavelet transformation is determined as the one with the highest energy content at different resolution level. However this will not be considered for the time being. More details about the meaning of levels will be given below soon.

Apart from the inputs and configurations, there are two output channels of this block: the approximation coefficients (A) and the detail coefficient (D). The mechanism is like this: the DWT of a signal (x) is calculated by passing it through a series of low-pass filters (g) and high-pass filters (h), the outputs (y) of which give the approximation coefficients and detail coefficients respectively, as indicated in Equation 4.2-4.3.

$$y_{low}[n] = \sum_{-\infty}^{\infty} x[k]g[2n - k] \qquad \text{Eq. (4.2)}$$
$$y_{high}[n] = \sum_{-\infty}^{\infty} x[k]h[2n - k] \qquad \text{Eq. (4.3)}$$

Afterwards, the sampling frequency is reduced to half of the original since half the signals have been removed. As a result, the resolution time will be doubled, and each output will expect a doubled frequency resolution [28]. Figure 4.10 illustrates how this works. Usually, the output from the low pass filter can be further transformed into a second layer of approximation coefficients and detail coefficients. In fact, DWT includes successive *levels* of such high- and low-pass filters, so the decomposition is repeated to further increase the frequency resolution [16, 33]. For each level, the frequency of higher spectrum is covered, where the latter layers covering the lower frequency [31]. A binary tree called 'filter bank' is presented in Figure 4.11.
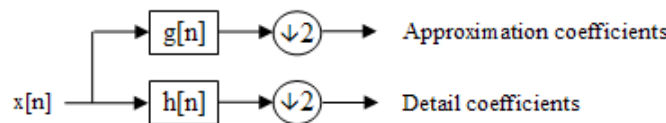
Figure 4.10 Block Diagram of Filter Analysis (taken from [33])
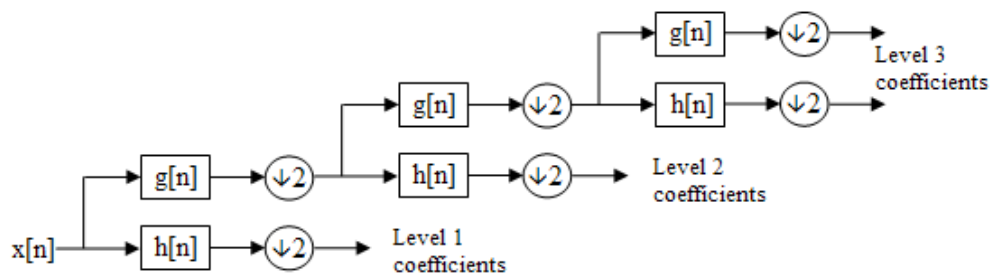
Figure 4.11 Block Diagram of Filter Bank (taken from [33])

35

Regardless the complexity in theory, the general principle in wavelet protection is quite simple - when the magnitude of the wavelet coefficients (detailed coefficients of a certain level) exceeds a specified threshold, a fault is identified. In the simulation, DWT with mother wavelet of both <u>Haar</u> and <u>Db4</u> of <u>6 levels</u> is tested out for different fault locations. Figure 4.12 shows the output detail coefficients of all 6 levels detected at C2, C1, A1, A11 and A12 for both mother wavelets.

(a)   **(b)**
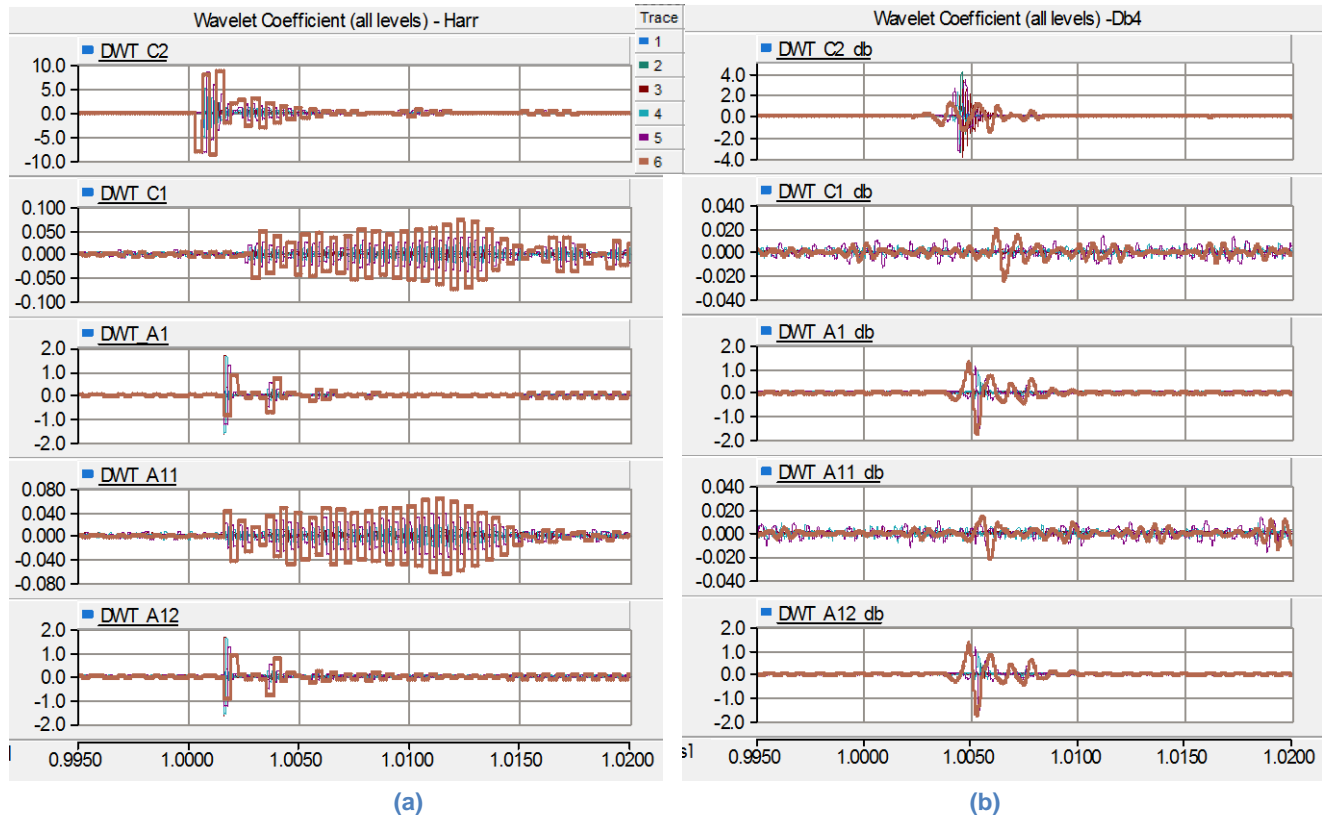
Figure 4.12 Wavelet Transform Detail Coefficients (d=10km) with the Mother Wavelet as (a) Haar; (b) Db-4

As can be seen from the figures, 6th level coefficient (in orange) is for most of the time of the largest magnitude and therefore less sensitive to noise. Therefore, the scope further narrows down to considering only the 6th level detail coefficients detected at C2, C1, A12 and A11 for fault discrimination, as in Figure 4.13. As can be read from Figure 4.13, the maximum magnitude of level-6 detail coefficients detected at A12, A11, C2 and C1 during the entire simulation period is 1.91, 0.07, 8.64 and 0.11 respectively for Haar mother wavelet, and 1.75, 0.03, 4.45 and 0.03 for Db4 mother wavelet. Similarly, results in other fault scenarios are summarized and presented in Table 4.4.

Table 4.4 6th level Detail Wavelet Coefficients Magnitude

Magnitude		Haar (6 level)					Db4 (6 level)				
D from C2 [km]		1	10	100	190	199	1	10	100	190	199
A1	A12 (faulty)	1.37	1.91	2.9	8.71	40.3	1.48	1.75	3.46	7.45	8.14
	A11(healthy)	0.07	0.07	0.1	0.41	1.22	0.03	0.03	0.03	0.17	1.04
C2 (faulty)		40.76	8.64	2.9	1.89	1.87	7.77	4.45	3.46	2.37	2.31
C1 (healthy)		0.11	0.11	0.11	0.60	0.88	0.02	0.03	0.02	0.15	0.47
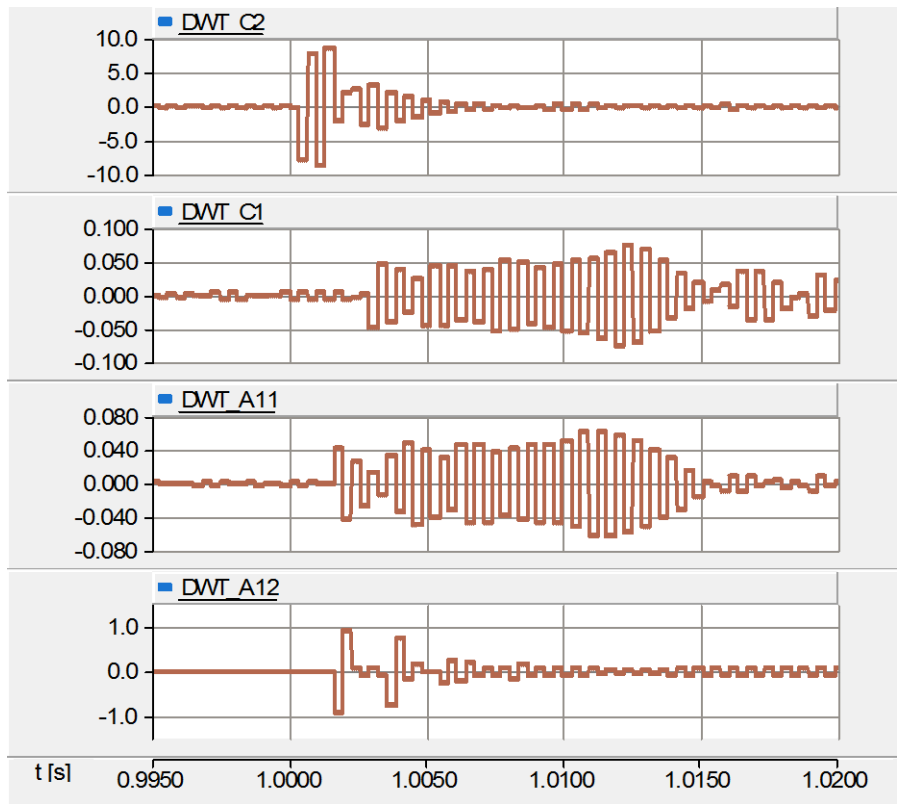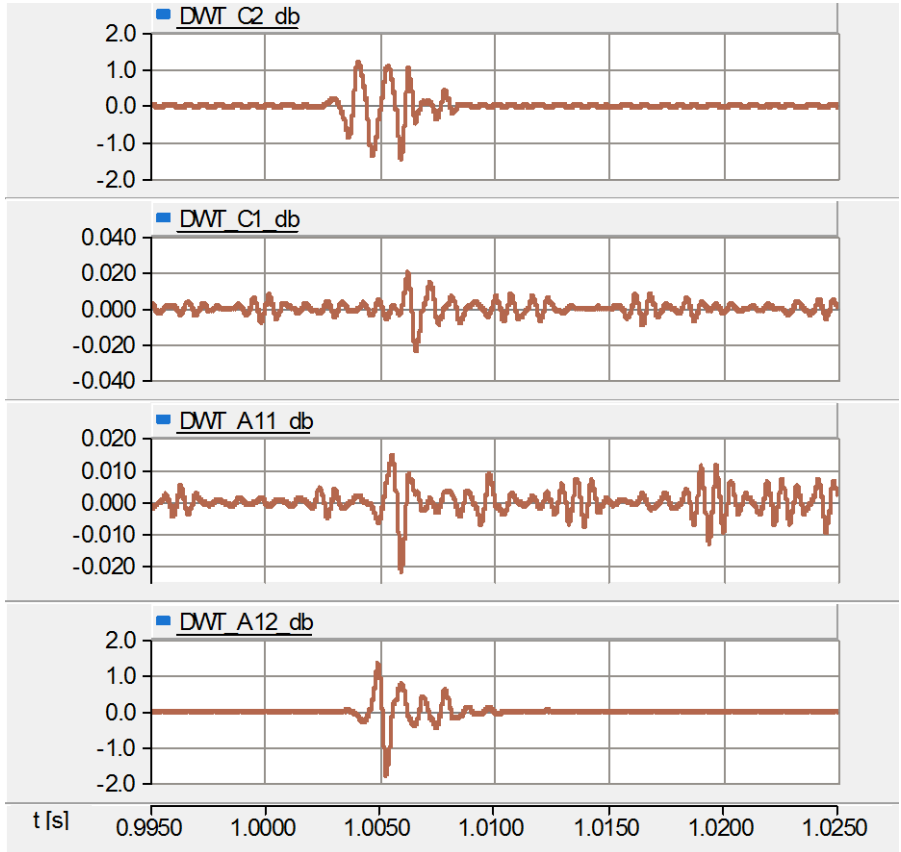
Figure 4.13 Wavelet Transform 6-level Detail Coefficients (d=10km) with the Mother Wavelet as (a) Haar; (b) Db-4

Some comments are made based on the results:

- By setting an appropriate threshold, wavelet based fault detection with both mother wavelets are effective in discrimination. However, since the maximum of recorded data at A11 is 1.22 for Haar (or 1.04 for Db-4) when d=199km while the minimum of recorded data at A12 is 1.37 for Haar (or 1.48 for Db-4) when d=1km, the threshold is a bit tricky to set in practice where noise, measurement error, etc. exist. However, several solutions can be proposed here for VSC_A1:
  - Use fuses or instantaneous overcurrent relays as backup protection to clear extreme currents in very close faults as discussed in Section 4.2.
  - Use current derivative as auxiliary unit, which can tell the direction of fault based on the polarity of the derivatives as discussed in Section 4.3.
- As for the selection of mother wavelet, although Db4 is believed to outperform Haar as suggested in literature [25], it requires large processing time and seems not satisfactory for fault detecting in this case. This can be validated in Figure 4.12 (b), as the first peak appears with a delay with 2.5-4 ms, which is larger than the critical time in this case as 2.2ms. In fact, even if the threshold is set as exactly 0.15 (equals the value taken when d=190km), it still takes 2.85ms for C2 to report a fault, which still cannot meet the requirement.
- As for the levels of transform, since the time delay is mainly caused by the filters needed in wavelet transform, a lower level can help reduce it. In [20], the optimal level of the wavelet transformation is determined as the one with the highest energy content at different resolution level. As 6th level Haar wavelet transformation works desirable and effective, lower level wavelet transform will not be tested for the time being.

In summary, wavelet transform technique are effective in detecting the wave front under faults in a relatively short time [16, 22], and thus distinguishing the faulty line and the healthy line. Other sub-protection units such as overcurrent relay, derivative will enhance the performance. However, it also requires massive and complicated calculation which makes the implementation difficult. Furthermore, it also causes the time delay. Between the two sets tested in the project, Db-4 mother wavelet causes more delay in processing time than Haar mother wavelet although the former is usually believed as a better and more effective alternative [29]. Indeed, if Db-4 is used as the mother wavelet, 6th level wavelet transform will not be possible to detect the fault in time in the case. Yet, wavelet transform of lower levels might be the possible solution here. Nevertheless, the detail coefficient of lower level is usually smaller in magnitude and is more sensitive to noise.

4.4 Travelling Wave Based Fault Location

Once the faulty line has been determined and isolated from the system, exact fault locating is essential for permanent faults to facilitate the repairing work afterwards. Although speed is no longer of the top priorities in the fault locating algorithm, it is still preferred to locate the fault with the data obtained from fault detection within the fault clearance period. In this project, travelling wave based fault location techniques will be adopted.

4.4.1 Classifications

There are mainly three different types of travelling wave based fault location method.

- Type A, or single-ended mode relying on fault generated transients

  In Type A, the fault location can be determined by Equation (4.4)

$$d = (T2 - T1) \times v/2 \qquad\qquad Eq. (4.4)$$

where d is the distance from the fault to a terminal, and T1, T2 the arrival times of the first two waves to reach that terminal.

In this project, VSCs act almost as ideal voltage sources and that only bolt faults are considered. In other words, the voltage reflection coefficient is around -1 at both fault and terminals. However, large impedance of the equivalent VSC station and the fault may result in failure of the method, such as after installing the fault-current-limiting protective inductors at the station terminals which will be introduced in Chapter 7. Moreover, it will also be affected by the fault arc duration [35].

- Type D, or double-ended mode relying on fault generated transients

In this type, the fault location can be determined by Equation (4.5)

$$d = L - (Ta - Tb) \times v/2 \qquad\qquad\qquad \text{Eq. (4.5)}$$

where d is the distance from the fault to a terminal b, (Ta-Tb) the difference in arrival times at station a and station b, and L the line length between the two stations.

Compared to Type A, Type D has less restrictions in fault impedance. However, Global Positioning System (GPS) is in need for obtaining time stamps. Moreover, the communication is required as well.

- Type E, or single-ended mode relying on breaker and generated transients

In this type, the signal is generated by the circuit breaker. However, this type is of less interest to this project and no more details will be given here.

4.4.2 Method Description

It is pointed out in literature [36] that the fault occurred on a VSC-HVDC line will cause a steep wavefront on the DC current. It further recommends that the arrival time of the travelling wave can be detected based on the measured DC current.

It can be further concluded from Section 4.4.1 that given the information of the faulty line, the estimation of the fault location is determined by two factors, namely:

- Wave velocity
- Arrival Time(s)

Wave Velocity

The wave velocity (v) is dependent on the line property and is constant for a specific cable, calculated either with Equation (4.6) or (4.7).

$$v = \frac{c}{\sqrt{\text{Relative Permittivity}}} \qquad\qquad\qquad \text{Eq. (4.6)}$$

$$v = \frac{1}{\sqrt{LC}} \qquad\qquad\qquad \text{Eq. (4.7)}$$

Similar to what has been done in literature [16], the speed of the travelling wave in this study case can be calculated by Equation 4.6:

$$v = \frac{3 \times 10^5 [\text{km/s}]}{\sqrt{2.3}} = 198\ [\text{km/ms}]$$

Arrival Time(s)

As described before, it is preferred to locate the fault with the transient data obtained from the fault detection. Therefore, in this section, the two methods as introduced in Section 4.3 will be tested out.

1. Arrival time detection based on <u>Current Derivative</u> [16]

It is intuitive to use the current derivative to detect the arrival time. More specifically, the arrival time of each wave can be roughly estimated as the moment when the current derivative exceeds a pre-set threshold, in this case 0.5. Given the resolution time for simulation as 10 microseconds and the wave velocity as 198km/ms, the uncertainty range of travelling wave based fault locating with arrival time detected by current derivatives is $\pm$1.98km. However, the threshold of 0.5 may further expand the error margin a little larger, especially for faults farther away with smaller current derivatives.

Once again, taken the case d=10km as an example, the arrival times defined as above are listed in Table 4.5. According to Equation 4.4 and 4.5, the distance between VSC_C2 and the fault d is estimated as <u>9.9km</u> and <u>9.91km</u> by Type A and Type D respectively. The minimum requirement of the time window of information is <u>0.15ms</u> for Type A and <u>0.96ms</u> for Type D, both below the critical time of 2.2 ms when d=10km. This indicates the data from fault detection will be sufficient in fault locating in this case. Therefore, both estimation results are considered as well-performed in effectiveness and accuracy when d=10km. Results for other fault scenarios are summarized and presented in Table 4.6.

Yet, like derivative based fault detection method, such time domain techniques are sensitive to noises, load fluctuations, etc.

Table 4.5 Arrival Times based on Current Derivatives (d=10km)

	Value
T1	0.05ms
T2	0.15ms
Ta	0.05ms
Tb	0.96ms

Table 4.6 Travelling Wave based Fault Locating based on Current Derivatives

		Performance based on current derivative				
D		1	10	100	190	199
Type A	Time [ms]	0.03	0.25	1.51	2.91	3.06
	Estimated Distance [km]	1.98	9.9	99.99	193.05	203.94
	Absolute Error [km]	0.98	0.1	0.01	3.05	4.94
Type D	Time [ms]	1	0.96	0.5	0.96	1
	Estimated Distance [km]	1.99	9.91	100	190.09	198.01
	Absolute Error [km]	0.99	0.09	0	0.09	0.99

2. Arrival time detection based on <u>Wavelet Transformation</u> [20, 37]

An alternative option is to detect the arrival time with the detail wavelet coefficient(s) of the appropriate level(s) resulting from the wavelet transformation. Upon an arrival of the wavefront, the square of the wavelet coefficient rises significantly, which can be read from the corresponding plots, for example Figure 4.14 in the case when d=10km.

It has been discussed in Section 4.3.2 that the Haar wave outperforms Db-4 as the mother wavelet in this specific case since it requires shorter processing time. Besides, it also points out that the higher level coefficients do not contain high frequency signals thus having less time resolution. This can be further proved in

Figure 4.14, which presents the square of 1st to 3rd detail wavelet coefficient of the 6-level wavelet transformation with Haar mother wavelet for VSC_C2 when d=10km. While the 1st and 2nd detail wavelet coefficients gives similar results in wavefront detection, the 3rd level fails so after the first wavefront. Yet, the loss in high-frequency information causes less problem in faults further away from the detecting point, as shown in Figure 4.15 where the similar results are given with data A12. In this case, the fault is 190km away from the detecting point A12, and that all of the 6 levels detailed wavelet coefficient gives the identical arrival time within the acceptable error. However, another problem can be noticed here that the lower level coefficients are small in magnitude and thus susceptible to noise. Literature [20] proposes a scheme to select the proper details level based on the highest energy content at different resolution levels. This could be taken into consideration in the future for protection scheme optimization. In this project, however, for simplification noise is not be considered and that only the 1st detailed wavelet coefficient will be used for wavefront arrival time detection. Since the time resolution of 1st detail wavelet coefficient is twice of the signal sampling time resolution, the uncertainty in this case is also doubled to $\pm$3.96km, which is twice as much as in that with current derivatives.
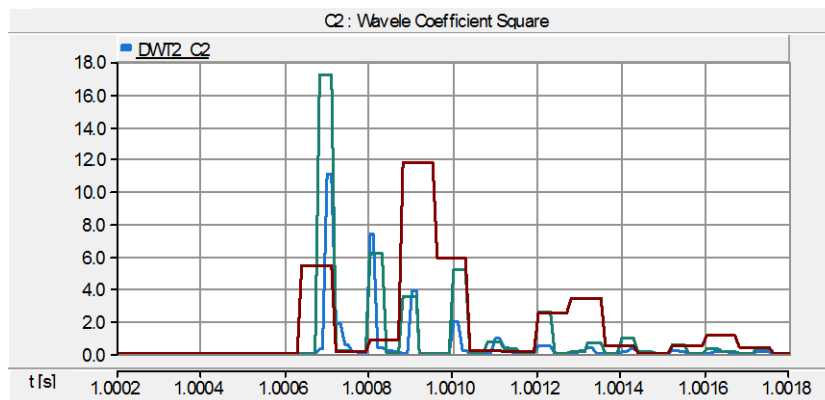
Figure 4.14 1st - 3rd Detailed Wavelet Coefficient Square of 6-level Wavelet Transform (Haar) of C2 (d=10km)
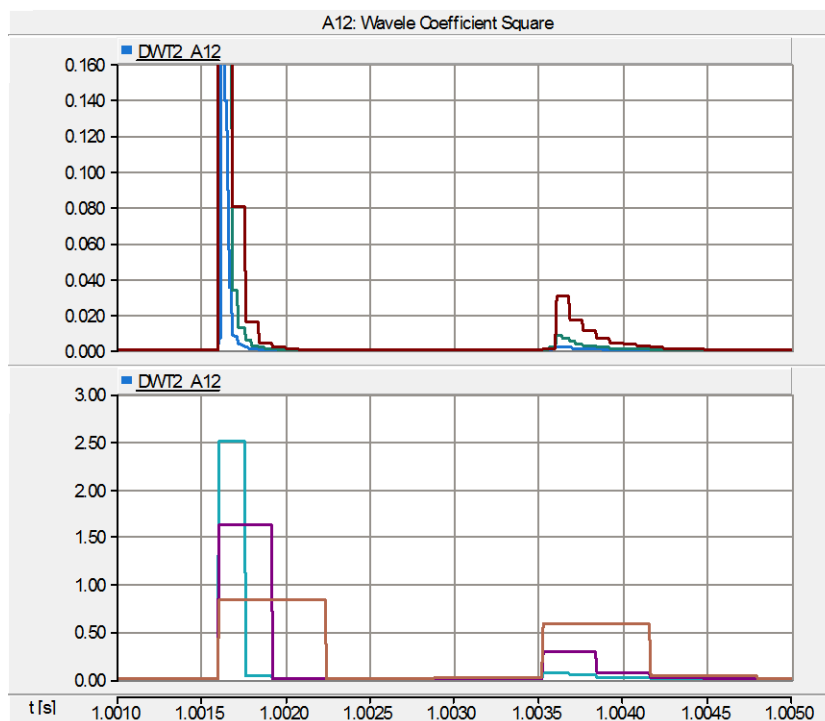
Figure 4.15 Detailed Wavelet Coefficient Square of 6-level Wavelet Transform (Haar) of A12 (d=10km)
(up: 1st -3rd down: 4th – 6th)

41

Table 4.7 Arrival Times based on 1st Wavelet Coefficient (d=10km)

	Value
T1	0.68ms
T2	0.8ms
Ta	0.68ms
Tb	1.6ms

Table 4.8 Travelling Wave based Fault Locating based on 1st Wavelet Coefficient

		Performance based on 1st wavelet coefficient				
	d	1	10	100	190	199
Type A	Time [ms]	0.7	0.8	2.16	3.56	3.72
	Estimated Distance [km]	3.96	11.88	100.98	194.04	205.92
	Absolute Error [km]	2.96	1.88	0.98	4.04	6.92
Type D	Time [ms]	1.64	1.6	1.14	1.6	1.64
	Estimated Distance [km]	2.98	8.92	100	191.08	197.02
	Absolute Error [km]	1.98	1.08	0	1.08	1.98

In the case when d=10km, the wavefront arrival times detected are listed in Table 4.7. According to Equation 4.4 and 4.5, the distance between VSC_C2 and the fault (d) is estimated as <u>11.88km</u> and <u>8.92km</u> by Type A and Type D respectively. The minimum requirement of the time length of information is <u>0.8ms</u> for Type A and <u>1.6ms</u> for Type D, both below the critical time of 2.2 ms when d=10km. This indicates the data from fault detection will be sufficient in fault locating in this case. Therefore, both estimation results are considered well-performed in effectiveness and accuracy when d=10km. Results for other fault scenarios are summarized and presented in Table 4.8.

Some comments are made based on the results:

- For both Type A and Type D, the sample rate should be high enough to detect and identify the wavefront. In the simulation, the resolution time is set as 10 microseconds. On the down side, this requires a great amount of data storage and processing.

- Accurate travelling speed can also be obtained and calibrated during a series of tests performed after cable installation and before operation.

- Comparing the two methods for arrival time detection, the simulation results show that the one based on the current derivatives is more accurate and needs fewer amounts of data. However, the simulation only considers ideal condition without noise or load fluctuation. Actually, current derivative is very sensitive to noise or other changes and is very likely to give the incorrect result. This, however, could be fixed by setting a time window of successive samples or a sufficiently selective threshold. The wavelet coefficient is in general less susceptible, but both the mother wavelet type and the level of the detail coefficient need to be selected with care taking both noise and time resolution into consideration. In practice, both methods can be used to calculate the location.

- Type D seems more accurate in location estimation than Type A. For Type A, the accuracy in cases when d=190km and 199km (also d=1km with 1st detail wavelet coefficient) is not good enough (>uncertainty). For d=199km, the prediction of Type A even reports that the fault is not within the cable. Moreover, the required data for fault farther away is also considerably large and long in post-fault time duration. However, this problem could be compensated by adopting the data from A12.

In summary, travelling wave protection of both Type A and Type D can fulfill the task of fault location with a certain degree of accuracy. The wave velocity can be either calculated from the cable property or measured in the tests prior to the system operation. On the other hand, the arrival time can be detected with either current derivative or wavelet coefficient, with the data obtained and stored before the fault clearance. However, both methods are somehow constrained by the possible noise. The heavy load on data storage and processing due to the high sampling frequency required is yet another drawback of this method. Type D is generally considered to be more accurate than Type A [35], but it requires more equipment installations such GPS and therefore is more expensive.

4.5 Summary and Discussions

In this chapter, different detecting methods have been introduced and tested in the target system. Some preliminary conclusions are obtained as follows:

- Overcurrent protection is straightforward and mature. Although it lacks selectivity, it is still a powerful backup protection scheme.
- Differential protection has intrinsic selectivity but is not desirable for extra-long distance transmission. Although the time delay in communication proves acceptable in this project when coordinated with backup overcurrent protection, the potential communication failure is still a threat to its reliability.
- Fault detecting based on current derivative is fast and effective. However, it is sensitive to noise and incorrect data samples. Nevertheless, its capability in indicating fault direction helps diagnoses in other detection method, such as wavelet-based fault detection.
- Fault detecting based on wavelet transform with 6-level Haar mother wavelet can effectively detect the fault. In contrary, wavelet transform with 6-level Db-4 mother wavelet needs too much processing time to detect the fault within the time limit. Besides, other sub-protection units such as overcurrent relay and derivative calculating unit could enhance the performance of this method. On the downside, it requires massive and complicated calculation which makes the implementation difficult.
- Travelling wave based fault location of both Type A and Type D shows relatively accurate estimation in locating with either current derivative or wavelet coefficients. Such data usually requires high sampling frequency, resulting in a challenge in big data storage and processing. Also, such methods might not work in noisy situations. While Type D is believed to be more accurate than Type A, it require communication and GPS installation.
- Other methods include those based on frequency dependent parameters [2, 38, 39, 40], Artificial Neural Network (ANN) [41, 42], self-adaptive filters [43, 44] and fuzzy logic [45]. All are promising but need further study before implementation. Therefore, they are not discussed in detail in this report.

Based on the statements concluded above, a feasible detecting and locating scheme can be proposed as below:

- Fast and non-communicate-dependent wavelet-based fault detecting method is advised as the main detecting scheme, preferably aided by the derivative-based fault detecting method for both direction indication and detection double-check. For better performance, the mother wavelet and transform level need to be selected with care as well.

- Differential protection is also proposed as a main protection for the scheme. Although the communication time delay is to some degree acceptable in this case, the reliability might still be impeded by its dependence on the communication system.

- The overcurrent protection is designed as the backup protection. It deals with the situation when the faults are extremely close to the station, or when both of the wavelet-based fault detecting method and differential protection fail.

- The exact location of the fault in the faulty line is further estimated based on the travelling wave. The wave velocity can either be calculated in theory or measured in practice, while the arrival time of wavefront is determined with the data of current derivative or/and wavelet coefficient obtained from fault detecting.

- A communication line is required in the system for differential protection and Type D travelling wave based fault location.

Chapter 5 Fault Isolating Devices

The second approach of improving DC protection scheme is designing and manufacturing fast fault isolating devices, i.e. DC circuit breakers (DCCB). This will be further discussed in this chapter. DC breakers are often believed as one of the key elements in the development of the future DC grids, especially in topologies where fault currents cannot be cleared or limited intrinsically [22]. This chapter serves as an introduction to these technologies; yet, the modeling or simulation of such devices is out of scope in this project.

5.1 Introduction

Circuit breakers (CB) are responsible for interrupting fault currents and isolating the faults from the system under the short circuit circumstances. In normal operation, they should cause as little loss as possible. In general, the requirements for circuit breakers are listed as below [4, 46]:

- In normal operation, CBs should have low voltage drop and low conducting losses.
- During fault, CBs are to interrupt short circuit current or overload current quickly without abnormal voltage transients.
- When CBs are open, they act as excellent insulators and should be able to withstand the transient voltages.
- CBs are also required to withstand the rated current as well as the short circuit current both mechanically and thermally.

Accordingly, the performance of a CB is characterized by several parameters, including on-state losses, interruption time, and maximum withstanding current and voltage. Such parameters are to be tested and compared to decide the appropriate portfolios for a specific case. However, in this report, only the interruption time will be considered. Furthermore, no details will be given regarding the transients caused by the CB interruption. In fact, CBs are modeled as ideal switches which open with a time delay that equals the sum of detecting time and interrupting time after the fault occurrence. This simplification is based on the following (ideal) assumptions:

- The on-state loss is 0.
- CBs are able to interrupt any current of whichever magnitude or polarity.
- CBs in off state act as perfect insulators no matter what voltage they carry.
- CBs can withstand currents of whatever magnitude or polarity both mechanically and thermally
- Since no complicated models or interrupting procedures are of concern here, it can be further assumed that inserting CBs do not influence the PI parameters in control system.

5.2 AC Circuit Breakers and DC Circuit Breakers

In theory, it is possible to clear DC faults by tripping ACCBs. A handshaking method proposed in [47] which, as described by the author, is tested as reliable in fault locating and isolating. However, since the interrupting time for ACCBs is normally within 50-100ms [6], with the best as two cycles (i.e. 40ms in 50Hz system) [48], they are obviously not acceptable in DC fault protections where faults are required to be cleared within a few milliseconds. Moreover, the basic "cut-and-try" method is not desirable in MTDC [38, 49]. On the contrary, DCCBs can apply mechanisms other than the mechanical one, and thus providing possibilities for shorter clearance time. Moreover, its ability in sectionalizing lines also enhances the performance of MTDC systems [48]. Therefore, DCCB is indispensable in protecting the HVDC grids from DC faults [49]. Usually, each DC cable is equipped with two DCCBs at both ends. Besides, ACCBs are also installed for backup protection.

Although DCCB is believed to be the solution in fast fault isolation, it still turns out challenging to design and manufacture the competent DCCBs which can interrupt extremely high currents within extremely short time (within millisecond range) [50], especially for extra-long transmission cables where longer time is required in fault propagation and communication [19]. Indeed, it is also reckoned as one of the key issues that prohibits the extensive application of DC systems [23]. Nevertheless, research and development has taken place in this field and several DC breaker prototypes have been introduced and tested in simulation or laboratory environment in recent years. In general, they are classified into three categories:

- Mechanical Breakers
- Semiconductor-based Breaker, also known as Solid State Breakers
- Hybrid DC Breakers

Each will be introduced in more details in the remainder of this chapter.

5.3 Mechanical DC Breakers

The first generation of high voltage DCCBs is the mechanical DC breakers based on the technology of AC gas breakers of both air-blast and the SF_6 ACCBs [51]. However, since DC current does not have zero crossing, it needs to be generated by the resonance circuit [3]. The basic topology of an air-blast ACCB is presented in Figure 5.1, also known as the BBC prototype [4, 51]. As can be shown in the figure, a mechanical DCCB has three branches, consisting of a switching equipment (path A) in parallel with an LC resonant circuit (path B) and a surge arrestor (path C) [51]. The principle works as follows [3, 23, 52-55]:

- During the normal operation, the switch is closed and path B and C are short-circuited.
- However, whenever a fault is detected, the switch opens and the separation of CB contacts creates the high voltage arc.
- Such arc can initiate the oscillating current in C-L-CB loop (path A & B) at the natural frequency of the loop.
- Due to the negative voltage-current characteristic of the arc, it keeps increasing resulting from the positive feedback till the maximum current hits the set value of current interruption.
- When the oscillating current crosses 0, the switch is capable of interrupting the current by parting the switch contacts completely from each other.
- Once CB is open, the capacitor is charged by the commutated current rapidly till the voltage reaches the threshold of the arrestor in path C.
- Then surge arrestor works to dissipate the energy in the system, limiting the commutation current/ voltage across the capacitor.
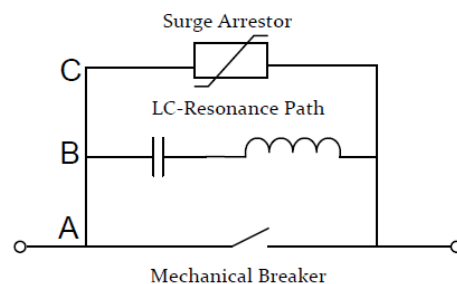
Figure 5.1 Air-blast DCCB Basic Topology (taken from [4])

There is yet another 'Westinghouse prototype' based on the SF_6 AC breaker technology [51]. The main principle is similar, while the resonant circuit in Westinghouse prototype does not contain any inductor but an independent vacuum switch (VS) is added to produce an optimal gas flow condition when the interrupter reaches the desired gap [23]. The principle of SF_6 breaker prototype is shown in Figure 5.2 [51].
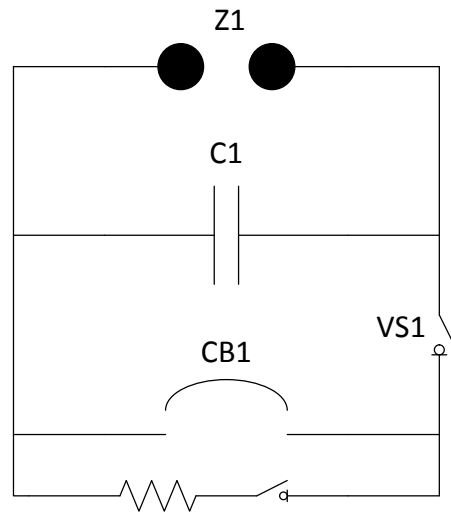
Figure 5.2 SF_6 DCCB Westinghouse Prototype

The two prototypes introduced above are innovative breakthrough in the field of HVDC breakers. Moreover, they have low on-state losses as well as low cost. However, due to the intrinsic drawbacks of mechanical breakers, the clearance time goes as long as tens to a hundred milliseconds [2, 5, 23]. The idea of active resonance circuit, which includes the capacitor charger to actively charge the capacitor, has made a little improvement in the clearance time, as indicated in Figure 5.3 (b) [23]. However, the mechanical DCCB is in general slower than other breakers, and it cannot meet the requirements for DC protection without the application of current limiters [52]. More details about fault current limiters will be described in Chapter 6.

(a)   (b)
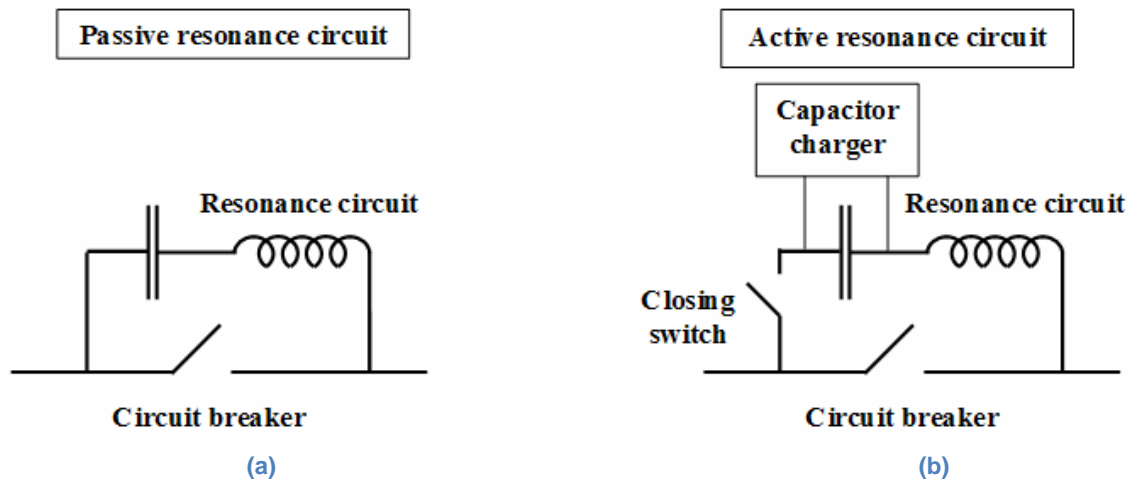
Figure 5.3 Principle of Passive and Active Resonant Circuit (taken from [23])

5.4 Semiconductor-based DC Breakers

Semiconductor-based DCCB, also known as solid state breakers, have been proposed in literature such as [52, 56, 57]. Such type of breakers can easily overcome the limitations in operation speed, contributing to a

clearance time <u>within 1ms</u> [4, 52]. However, on the downside it generates large transfer losses. The switches in this category are usually based on IGBT and gate turn-off thyristors such as GCTs (gate commutated turn-off thyristors) and GTOs.

5.4.1 IGBT-based DC breakers

The inherent capability in limiting the fault current has made the IGBT breaker a good candidate in DCCB. For a single IGBT breaker module, a diode is anti-paralleled to each IGBT. The working principle is illustrated in literature [48]: when a fault is detected in a line, the corresponding IGBT breaker will receive a blocking signal; once the fault current is extinguished, the faulty line will be isolated from the system by fast acting DC switches.

Since the IGBT breaker is unidirectional, it needs two main paths to accommodate the bidirectional power flow, each with another diode in series to prevent the current flowing through the freewheeling diodes [4]. Besides, IGBT breaker models are connected in series to increase the withstand capacity of the breaker. Surge arrestors, aiming to limit the fault level, are also connected in series. This causes high state-on losses in this type of DCCBs [56].

The topology of an IGBT breaker is presented in Figure 5.4. As can be seen from Figure 5.4, there are three branches in Semiconductor-based DCCBs. As mentioned before, two of them are main paths to enable the bi-directional flow, with the other for surge arrestors to dissipate the energy in the system.
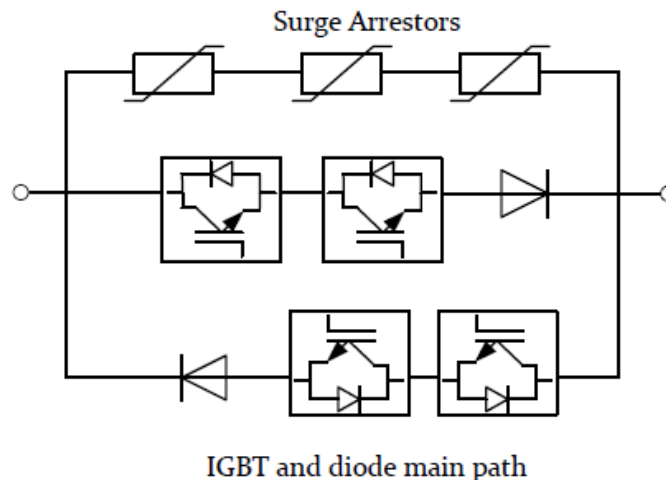
Figure 5.4 IGBT Breaker Topology (taken from [3])

5.4.2 Thyristor-based DC breakers

As mentioned earlier, although IGBT breakers have the inherent capability to limit the fault current, it has significant on-state losses on the downside. Literature [57] concludes that the losses caused by IGBT breakers are three times higher than that of the thyristor-based breakers in normal operation. Therefore, the latter option seems more desirable [4].

However, by its nature thyristors can only interrupt zero currents. As a result, thyristor-based DC breakers need to incorporate a zero-current imposing circuit in the design [23]. Literature [58] elaborates four topologies of such kind based on the parallel capacitor current commutation principle, as presented in Figure 5.5. In all these four circuit topologies, thyristor T_1 works as the main thyristor which carries the load current when DCCB is closed. Figure 5.5(a) presents a basic thyristor DCCB topology that interrupts fault current by turning on thyristor T_2. When a fault is detected, the pre-charged capacitor C discharges into the cathode of thyristor T_1, forcing a current zero to block T_1. Afterwards, the thyristor T_2 also blocks at current zero caused by the resonant

circuit comprised of C-L-T_2. Thus the fault is interrupted successfully. A drawback of this topology is the long dead-time caused by the high series resistor in the charging circuit R_c, which is compulsory due to the use of diode D_c. To shorten the time between an interruption and the following closing, the topology in Figure 5.5 (b) replaces the diode D_c with another thyristor T_3. However, like the topology in Figure 5.5 (a), this topology is dependent on the external power supply for pre-charging the capacitor C. A solution to this is to charge the capacitors from the DC rail through C-L-R_c, as suggested in Figure 5.5 (c) and (d). In Figure 5.5 (c), the resonant circuit is comprised of C-T_1-T_2/D_2-L which produces resonant current of the same polarity as the fault current. As a result, the thyristor T_1 becomes more thermally vulnerable. This threat is somehow alleviated by making the positive resonant current flow in the C-T_3-L loop while the negative resonant current flow in C-L-D_2/T_2 forcing a zero fault current in T_2 [23, 58].
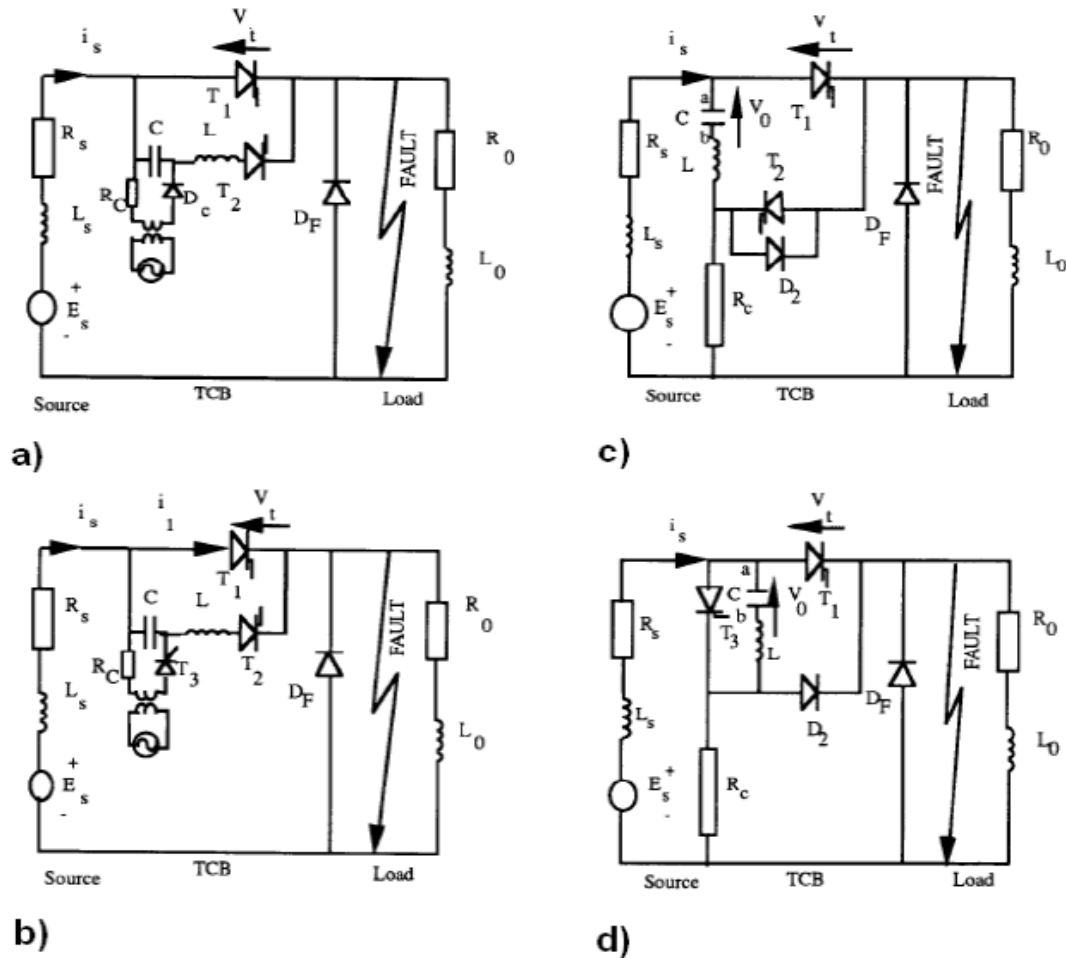
Figure 5.5 Thyristor-based Breakers Topology (taken from [58])

5.5 Hybrid DC Breakers

As described earlier, the mechanical DCCBs have low state-on losses but a significant time delay in fault clearance; on the contrary, the semiconductor-based DCCBs have short clearance time but are not efficient enough regarding the losses. Therefore, a 'proactive hybrid HVDC breaker' is proposed and has become commercially available by ABB in literature [59] which combines the advantages of the mechanical and semiconductor design and offers both fast operation and negligible transfer losses. The principle of this HVDC breaker is presented in Figure 5.6 [59].
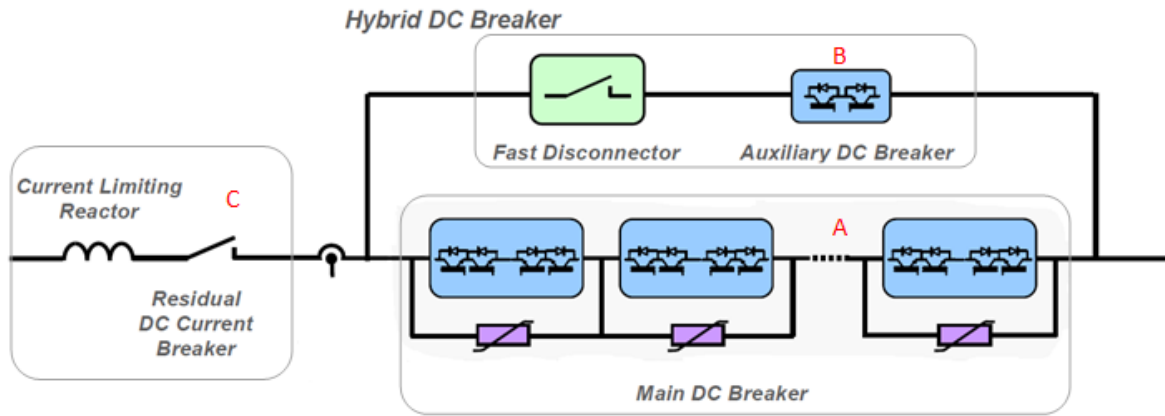
Figure 5.6 Proactive Hybrid HVDC Breaker - ABB (taken from [59])

As can be observed from the figure, the design can be divided into three sections [4, 16, 59]:

- Section A is a fully-rated main DC breaker, consisting of several groups of IGBTs connected in series, each group paralleled with a surge arrestor to limit the fault voltage.
- Section B is a bypass path, where the fast mechanical disconnector works together with a series of IGBTs as the auxiliary DCCB to interrupt the current quickly.
- Section C is comprised of a mechanical current limiting reactor connected to a mechanical isolator as the residual DCCB.

Section A and Section B are in parallel, with Section C in series with them. As indicated by its name, the proposed solution is capable of proactive operations. During the fault, the auxiliary breaker in Section B opens quickly, commutating the current to the main breaker path in Section A and enters into the standby status [4, 59]. Afterwards, if the main breaker receives the trip signal, current will be interrupted within a few microseconds [16, 59].

According to the descriptions above, the clearance time for the proactive hybrid HVDC breaker is a bit higher than the semiconductor-based DCCB due to the time needed for the mechanical disconnector. However, a clearance time as short as 2ms is still achievable [59]. When it comes to the losses, since the auxiliary are rated for lower voltage and current, the forward voltage as well as the on-state losses will also be lowered during normal operation. In summary, it combines the strengths of mechanical DCCBs and semiconductor-based DCCBs. However, they cannot withstand very high fault current, and the operating time is extended when protecting long transmission systems [2].

One more comment is that the proactive hybrid DCCB prototype introduced above is sometimes also referred to as Hybrid I. There is yet another Hybrid II type which combines the mechanical DCCBs or semiconductor-based DCCBs and current limiters together. Upon the fault detection, the switches in the main path will switch off and the current commutates to the second path through the current limiter. As a result, the current is dramatically constrained to a relatively low value. This indicates that the clearance time is no longer highly strict so that a mechanical DCCB might also be competent in fault isolation. Of course, fast semiconductor-based breakers can still be utilized here, but in desire to reduce the on-state losses, an auxiliary branch similar to what has been introduced in Hybrid I prototype needs to be incorporated as well [3, 60, 61]. More details on fault current limiters will be discussed in Chapter 6.

5.6 Summary and Discussions

Since AC breakers lack in both speed, selectivity and robustness in DC fault protection, it is necessary to design and manufacture competent DCCBs. While the zero-crossing can be artificially created by resonant circuit, DCCBs still remain challenging due to the stringent requirements in response time and maximum current. Three types of DCCBs have been discussed in this chapter, with some of the conclusions listed as below:

- Mechanical breakers are slow, with the clearance time as <u>tens to a hundred of milliseconds</u>. As a result, this type can only be used in combination with current limiters.
- Semiconductor-based breakers have fast operation, the clearance time of which can be reduced to within <u>1ms</u>. However, this type has significant on-state losses.
- Hybrid I breakers combines the strengths of the two types of breakers above, and a clearance time of <u>2ms</u> is achievable.
- Hybrid II breakers combines DCCB with current limiters, so that the requirement in clearance time will become less stringent.

Literature [4] also compares these DCCBs and summarizes the results as shown in Figure 5.7. It further concludes that none of the existing DCCB technology fulfills all of the requirements for DC fault protection, and that more research is in urgent need.

	Solid State Breakers	Hybrid Solid State Breakers with Mech. Disconnector	Hybrid Fault-Current Limiting Breaker	Active or Passive Resonance CB
Commutation time [ms]	0.1 switch	<0.2 switch ~0.25 disconnector	~0.1 switch <20 breaker 1-5 UFS	<20 breaker ~30 passive res. ~2 active res.
Energy absorption time [ms]	~1	~1	-	-
Total interruption time [ms]	<1	<2	<5-30	<60
Max rated voltage U_n [kV]	≤800	120 tested (up to 320 feasible)	AC-CB >500 UFS<12	≤550 available
Max breaking DC current [kA]	<5	9 tested (up to 16 expected)	~6-12 (estimated)	4 tested in operation (8 with active res.)
Expected power losses compared to a VSC station [%]	GCT ~30% GTO ~40%	<1% (few series switches)	negligible; only due to metallic contacts	negligible; only due to metallic contacts

Figure 5.7 DC Breaker Comparison (taken from [4])

In this project, only the clearance time is of focus in DCCB study. More specifically, DCCBs are modeled as ideal switches with the corresponding time delay that equals the sum of detecting time and interrupting time in the simulation. This indicates that losses, maximum withstanding current, maximum withstanding voltage, etc. will not be considered. Note here that some technology such as Hybrid I breakers is at the time being unable to deal with high voltages. However, since the maximum withstanding voltage is not discussed for the time being, all DCCB types introduced in this chapter will be considered as candidates in the DC protection scheme to be proposed in Chapter 7.

Apart from the DCCBs mentioned above, it is also possible to interrupt DC faults with DC/DC converters

as designed in [62] with acceptable dealing time. Moreover, it also has added values as a DC transformer, a current limiter and a power regulator. Nevertheless, the drawbacks lie in higher losses and cost [62]. More information of 'half bridge DC/DC chopper' and 'full bridge DC/DC chopper' can be found in [63] and [64] respectively. Actually, in [65], four fault isolating tools: a) Series hybrid DC breaker; b) Half bridge DC/DC chopper; c) Full bridge DC/DC chopper; d) LCL thyristor converter (Hybrid II) are compared and evaluated based on the performances, costs, losses, etc. in a 1.2 GW DC testing system. It concludes that so far there is no satisfactory DC breaker for HVDC. Therefore, this field needs more research and testing in the future [65].

Chapter 6 Current Limiting Technologies

While the fast fault detection and isolation can shorten the clearance time to avoid the huge fault current, another possible and more direct approach for DC cable short circuit protection is to limit the current itself to avoid the damage to the converters. By introducing various fault current limiters (FCLs) from either AC or DC side, the magnitude and/or derivative of the fault current will be effectively reduced. In this way, it allows the fault detecting and fault isolation to have longer reaction time. This chapter focuses on this aspect.

6.1 Introduction

Literature [66] introduces numerous state of the art FCLs of both passive and active types, such as saturable core FCL and the resonance type solid-state FCL. It also includes some more novel approaches utilizing superconducting materials, positive temperature coefficient (PTC) resistors, liquid metals, etc. Inductor-capacitor-inductor VSC, also known as LCL-VSC, is usually deemed as an innovative fault tolerant VSC topology. However, as can be noticed in Figure 6.1, it does not necessarily require re-design of the converter. Its basic idea is to inherently limit the fault current to a level that the system can sustain [67]. Thus the extra 'LCL' part of this design is also reckoned as a type of FCL in this report, and the related study will be included in this chapter too.
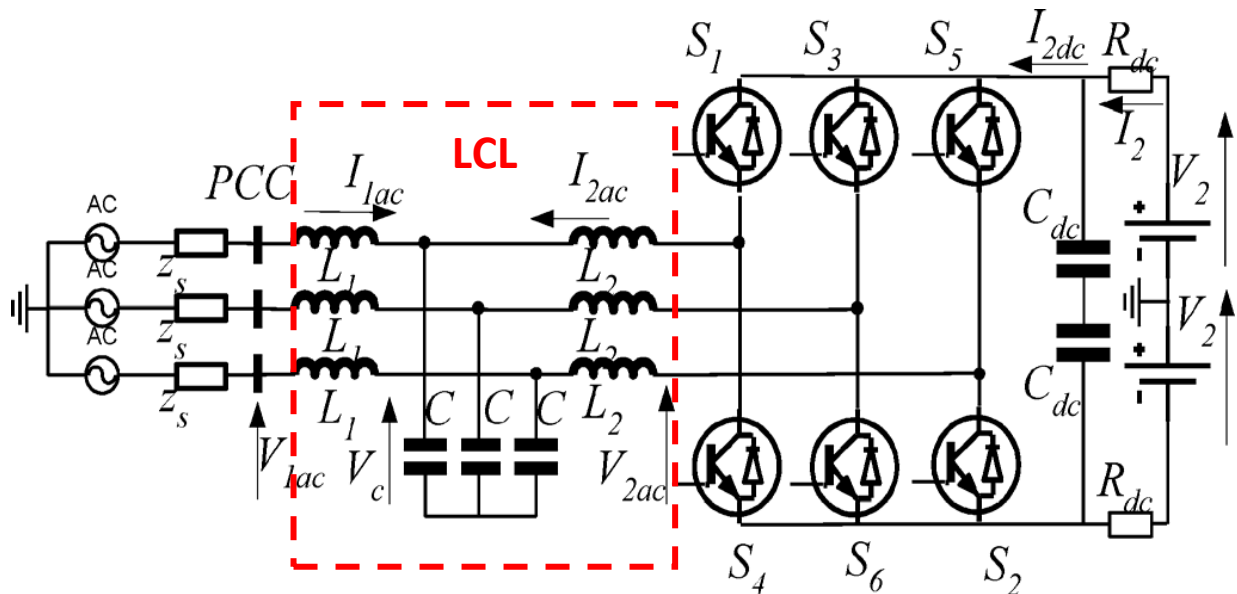
Figure 6.1 LCL-VSC Topology (taken from [2])

As analyzed earlier, in the three-stage fault response, the AC part only plays a role in the third stage (the grid feeding stage) [3]. Therefore, to avoid the overshoot in the second stage (the diode freewheel stage, also considered as the most challenging stage), FCLs need to be installed on the DC side. However, later in this chapter the simulation results also indicate that FCLs on the AC side are necessary in the target system too.

In the following sections, the fault current limiting schemes listed below will be discussed:

- Protective inductors installed on the DC side
- An LCL circuit installed on the AC side
- Nonlinear resistors, such as superconducting FCLs, PTC-resistor FCLs and liquid metal FCLs, installed on either DC or AC side

Similar to what have been displayed before in Chapter 4, only the cases when d=10km will be discussed in this chapter. Also, only the fault simulation results of VSC_C2 will be given. It is further assumed that faults

occur closer than 10km to the VSC station (d<10km or d>190km) will be taken care of by the backup overcurrent protection.

Moreover, throughout all the simulations in this chapter except for the last set, only station VSC_C2 implements the current limiting strategy while the other two VSC stations remain unchanged. These simulations provides with a qualitative view of how the current limiters affect the fault current. In the final simulation set presented in Section 6.5, however, all the three VSC stations apply the proposed current limiting scheme, so that its performance can be quantitatively verified and evaluated.

6.2 Protective Inductors

According to the three-stage theory which has been introduced in Section 3.2, DC side protective inductors can effectively limit the rate of rise in current during the first and second stages of the fault response, as well as limiting the current amplitude during the third stage. Literature [68] studies the system transient under faults and proves with simulation that inserting soothing inductors of suitable size between the cables and VSC stations (Figure 6.2) can effectively limit the capacitor discharge current, cable current and diode current and thus protecting the system. Moreover, since the inductors are inserted in the DC side, its impedance is relatively low that the system efficiency is not affected too much during the normal operations. However, the extra inserted inductors will impede the dynamic response of the whole system. Besides, a larger inductor brings up the total cost as well. Actually, sizing the protective inductors should be a trade-off between the current limiting effect, dynamic slow-down effect and the total cost of the project.
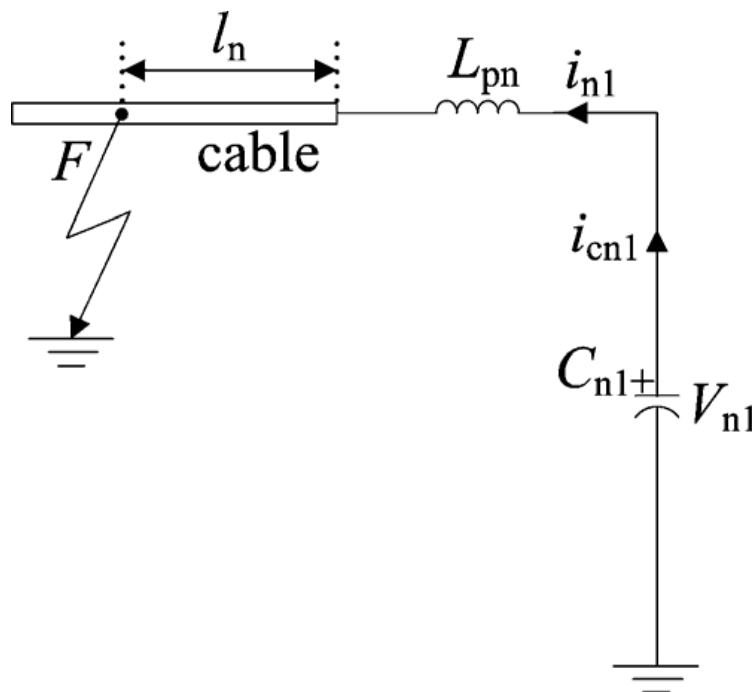
Figure 6.2 Insertion of Protective Inductors (taken from [68])

In the simulations, a pair of protective inductors, named 'L_protective', is inserted between the DC side of the VSC and the DC cables, as shown in Figure 6.3. To determine the appropriate size of such inductors, various inductance values are given to 'L_protective' and the maximum current in the upper-arm diodes (ID1, ID2 & ID3) and that in the DC cable are recorded in each corresponding simulation. This is realized by 'Multiple Run' (Figure 6.4) provided by PSCAD.
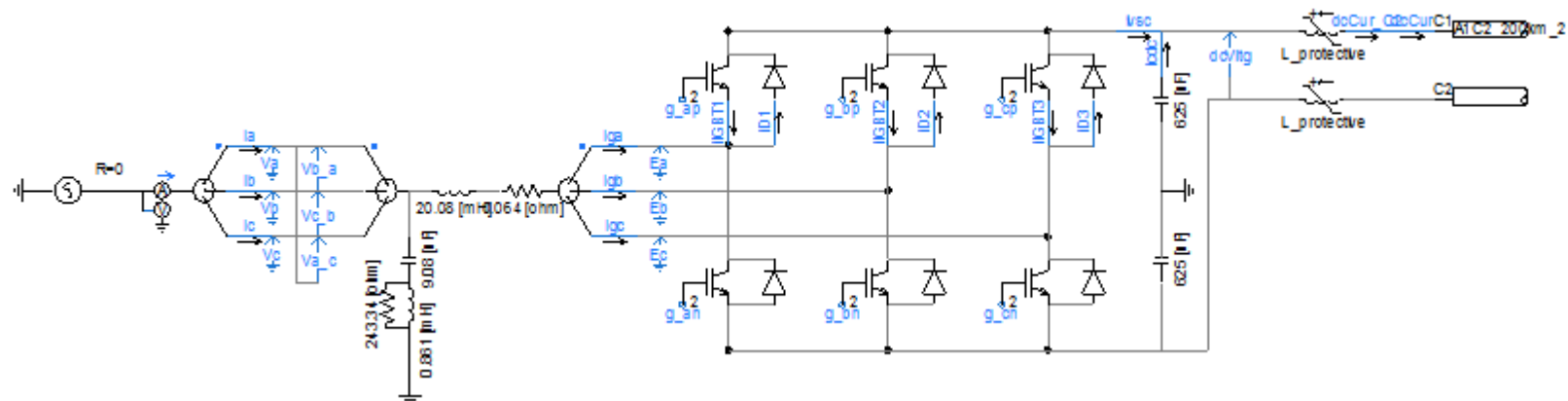
Figure 6.3 Protective Inductor and VSC System (VSC_C2 as an example)
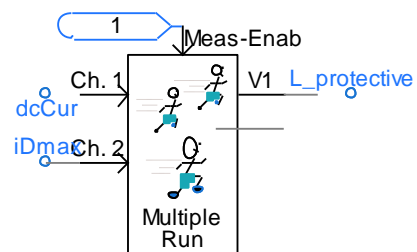
Figure 6.4 Protective Inductor Sizing and Multiple Run Setting

Table 6.1 Protective Inductor Sizing and Multiple Run Result (d=10km)

Run #	L_protective [mH]	I_D_max [kA]	I_cable_max [kA]
1	2	32.73874	61.02238
2	4	30.81017	52.87779
3	6	28.88168	47.44213
4	8	27.69929	43.60108
5	10	26.43872	40.50005
6	12	28.16779	38.04762
7	14	28.95929	36.03068
8	16	29.46447	34.35922
9	18	29.87272	32.84929
10	20	30.30227	31.54351
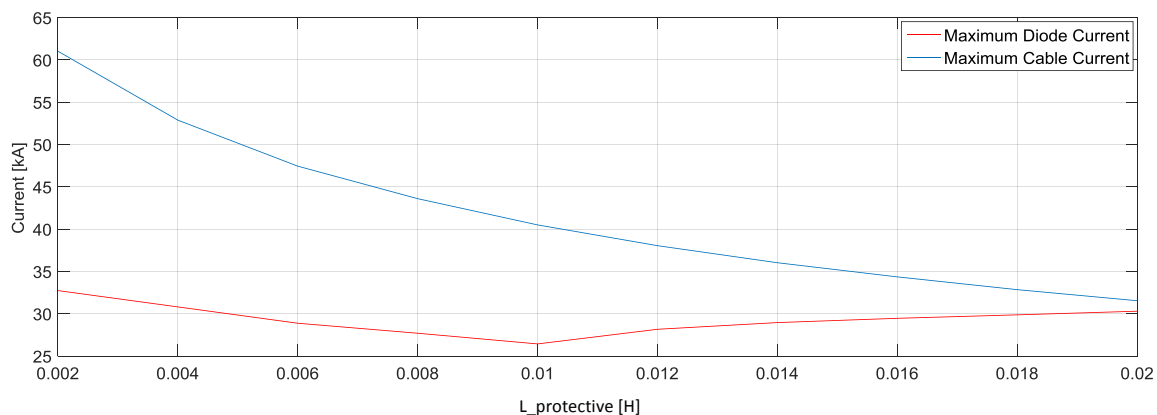
Figure 6.5 Protective Inductor Sizing and Fault Current Result (d=10km)

The *Multiple Run* simulation results of case d=10km are summarized and plotted in Matlab, presented in Table 6.1 and Figure 6.5. As can be seen from the results, with an increase in the inductance value of the protective inductors, the magnitude of the maximum fault current flowing through the DC cable is effectively decreased. However, the current limiting effect flowing through diodes is not very obvious. In fact, the maximum diode current increases a little bit with an increase of the protective inductor after 10mH. This is not desirable at all since diodes are usually deemed as the most vulnerable components [3]. Actually, in this specific case, the maximum diode current is no longer the overshoot which occurs by the end of the capacitor discharging process as discussed in literature [3]. Instead, 3rd stage (the grid feeding stage) can give rise to an even higher diode current, as shown in Figure 6.6 (without protective inductors) and Figure 6.7 (with L_protective =8mH). In fact, the decrease in maximum DC cable current is mainly caused by the increase of the total impedance in 3rd stage with the increase of the protective inductors' size. Of course, if the protective inductors keep increasing in sizes to a very large value, the diode current will eventually drop with the decrease in the total cable current. However, this is not economically desirable. It would be preferred to apply AC side devices, such as the LCL circuit, which will be discussed in more details in the next section. Nevertheless, by comparing the overshoot current at the beginning of 2nd stage (the diode freewheel stage), it is obvious that the protective inductors do limit the current at that specific moment, from around 25kA to around 17kA after the installation of a pair of protective inductors of 8mH.
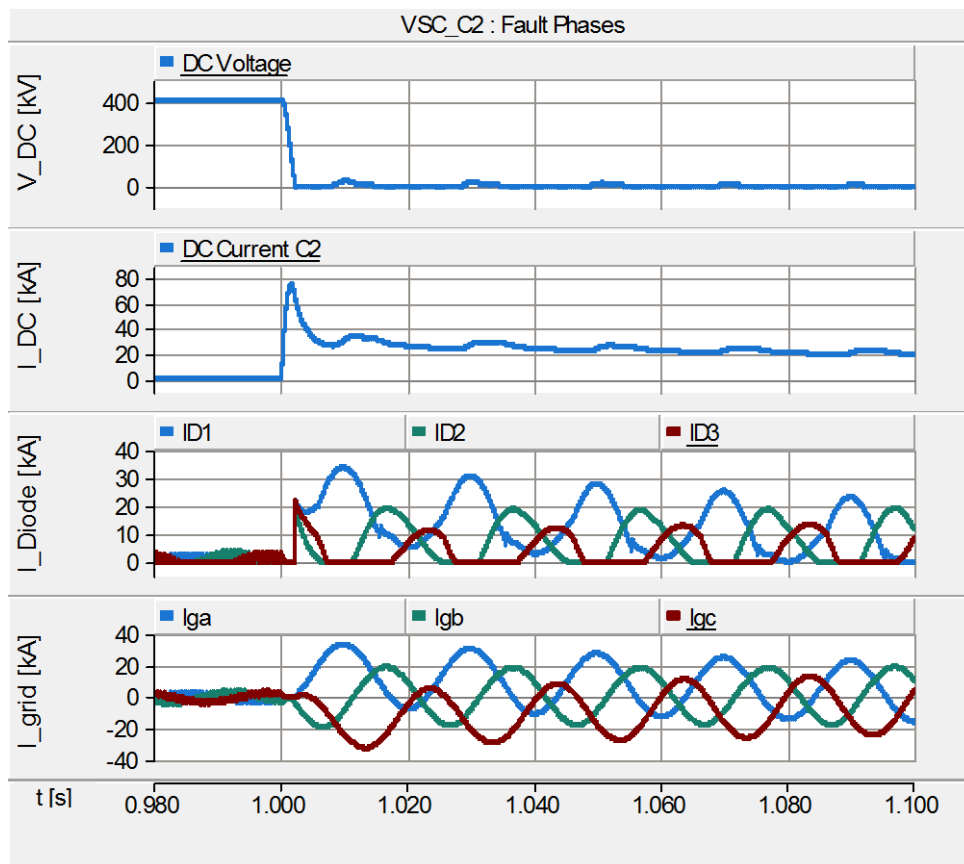
Figure 6.6 Fault Simulation Results without Fault Current Limiters (d=10km)
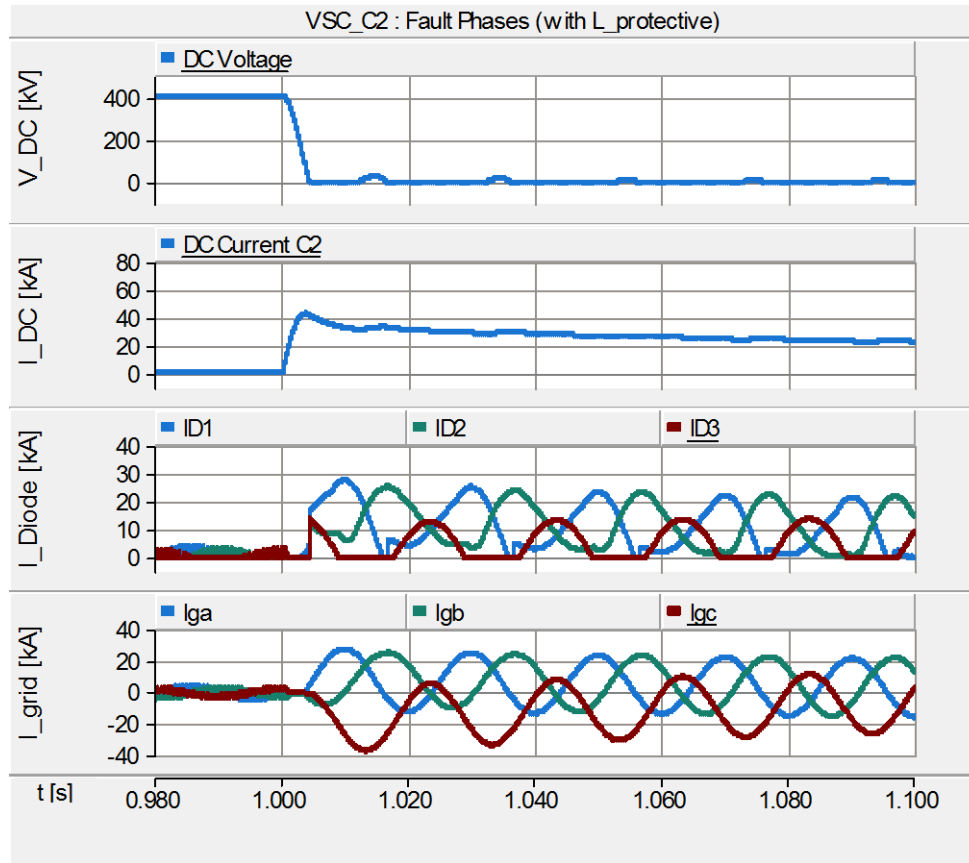
Figure 6.7 Fault Simulation Results with Protective Inductors of 8mH (d=10km)

6.3 Inductor-capacitor-inductor VSC

LCL-VSC, as shown before in Figure 6.1, is usually categorized as a fault tolerant VSC, but it does not necessarily need actual re-design of the converter and is extremely economic among other fault tolerant VSCs. In this section, however, this VSC topology is treated as a normal VSC station in combination with a LCL circuit on the AC side. The procedure of sizing a satisfactory LCL circuit has been introduced in depth in literature [2] and [69]. Moreover, due to the change in electrical topology, the logics in control system needs to be altered as well, as shown in Figure 6.8 which has also been discussed in literature [2]. More details can be found in literature [2] and [69] accordingly, and will not be further introduced in this report.

Referring to literature [2] and [69], the LCL circuit could be sized given the values of:

- Rated operational data
  - a. the rated power (P_{1r})
  - b. the rated AC voltage (V_{1AC})
  - c. the rated DC voltage (V_{DC}),
- Design parameters
  - d. the rated PWM modulation (M_r)
  - e. fault current ratio (r), defined as the ratio between the current flowing out of the VSC station(I_2) during fault and that in rated operation

57
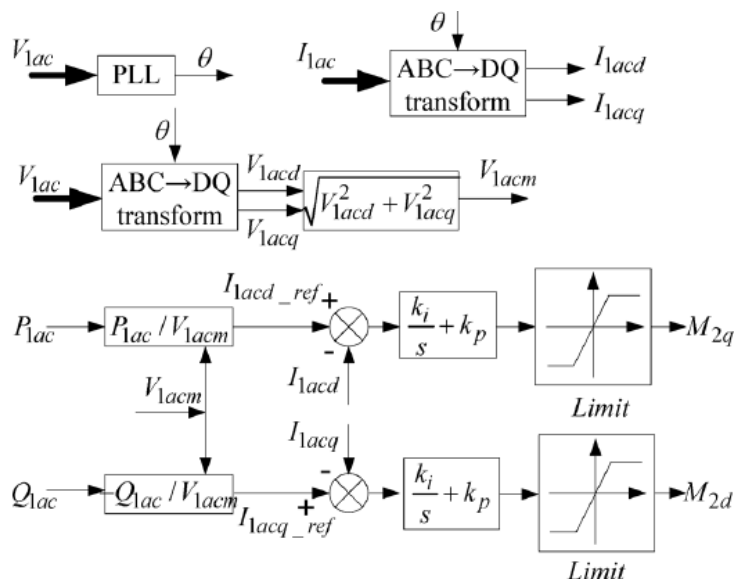
Figure 6.8 Control Scheme for LCL-VSC (taken from [2])

The corresponding Matlab code for sizing the LCL parameters for VSC_C2/C1 is given in *Appendix H*, while the parameters for VSC_A1 is calculated with a minor change in the inputs of P_{1r} and V_{1AC}. For the designing parameters, M_r is set as 0.95 and r as 1.02 at this moment. The results are shown in Table 6.2. The new ICC is also redesigned as shown in Figure 6.9 according to literature [2], with PI parameters determined based on trial-and-error.

Table 6.2 LCL Circuit Parameters

Component	VSC_A1	VSC_C1	VSC_C2
L1	135.2 mH	192.2 mH	192.2 mH
L2	131.6 mH	149.8 mH	149.8 mH
C	60.958 µF	46.244 µF	46.244 µF
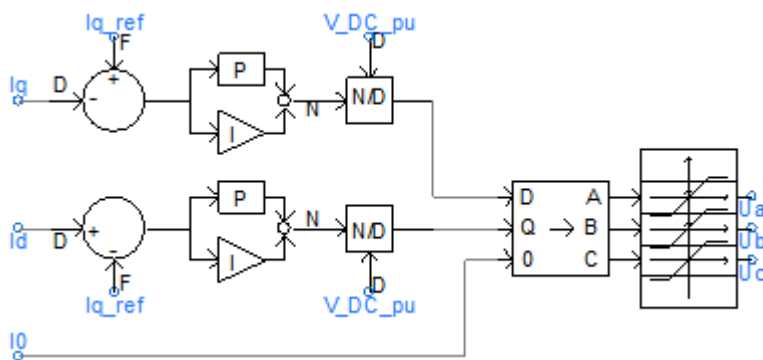
Figure 6.9 ICC for LCL-VSC

The fault simulation (d=10km) results with the designed LCL-VSC are given in Figure 6.10. Although it is claimed in literature [19] that the LCL-VSC topology works well with low speed mechanical DCCB due to its inherent capability in fault current limiting, the simulation result challenges such statement. In fact, the overshoot current at the beginning of 2nd stage still exists, threatening both the diodes and the DC cables, as shown in Figure 6.10. Indeed, as emphasized before, since the LCL circuit is installed on the AC side and that the AC part only plays a role in 3rd stage, the overshoot fault current cannot be avoided by AC side FCLs only.

Therefore, FCLs on the DC side, such as protective inductors introduced in the previous section, are indispensable in the protection scheme. Nevertheless, the effect of the LCL circuit in limiting the fault current in the grid feeding stage is considerable, as can be proved in Figure 6.10. With the LCL circuit, the amplitude of the grid feeding current is restrained from more than 30kA to less than 5kA. Moreover, for diode currents, the magnitude in 3rd stage is not as significant as the overshoot fault current any more.
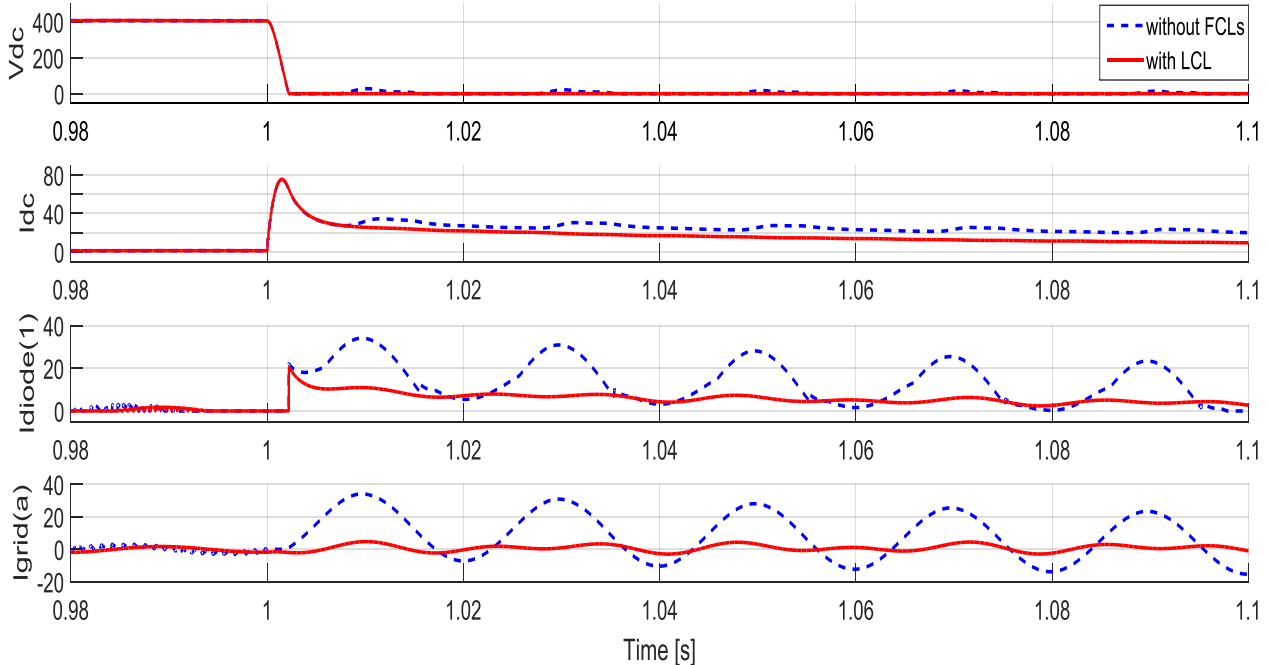
Figure 6.10 Fault Simulation Results with and without the Designed LCL-VSC (d=10km)

6.4 Nonlinear Resistors

Needless to say, the fault current limiting of DC and/or AC side could also be realized by installing nonlinear resistors, such as superconducting FCLs [70], PTC-resistor FCLs [71], liquid metal FCLs [72], etc. Although each has a different physical mechanism, all three type shares the similar principle of the 'desirable' characteristics of the nonlinear resistors – the low resistance during normal operations will rise sharp after the fault due to the increased temperature resulting from the fault current [66]; once the fault is cleared and the temperature of such devices cool down, they become low in resistivity again. Since the device is merely resistive, it does not affect the system dynamics as protective inductors do.

Figure 6.11 and 6.12 presents the fault simulation results of such nonlinear resistors installed on the DC and AC side respectively. In the simulation configuration, it is ideally assumed that the resistance of such component is zero during operational state and jumps to 15Ω (arbitrary chosen) in a step function at the instant of fault (t=1s) and remains constant afterwards. As can be concluded from these two figures, once again when the current limiting devices is installed on the AC side, it cannot prevent the threatening overshoot fault current in 2nd stage. However, when installed on the DC side, the nonlinear resistors seem to effectively limit the current in all three stages in the fault response. Moreover, since the resistance is relatively large, the DC voltage during fault does not drop to 0, but stays around 200kV in this case.
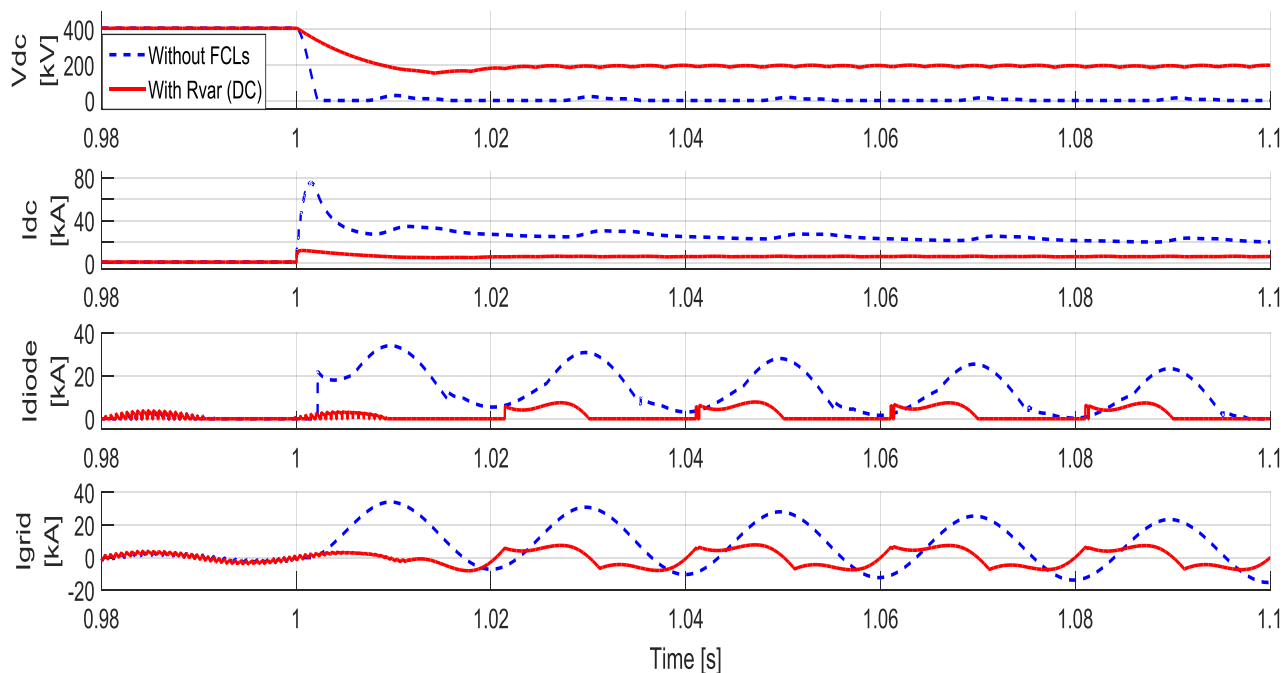
Figure 6.11 Fault Simulation Results with the Ideal Nonlinear Resistor on the DC Side (d=10km)
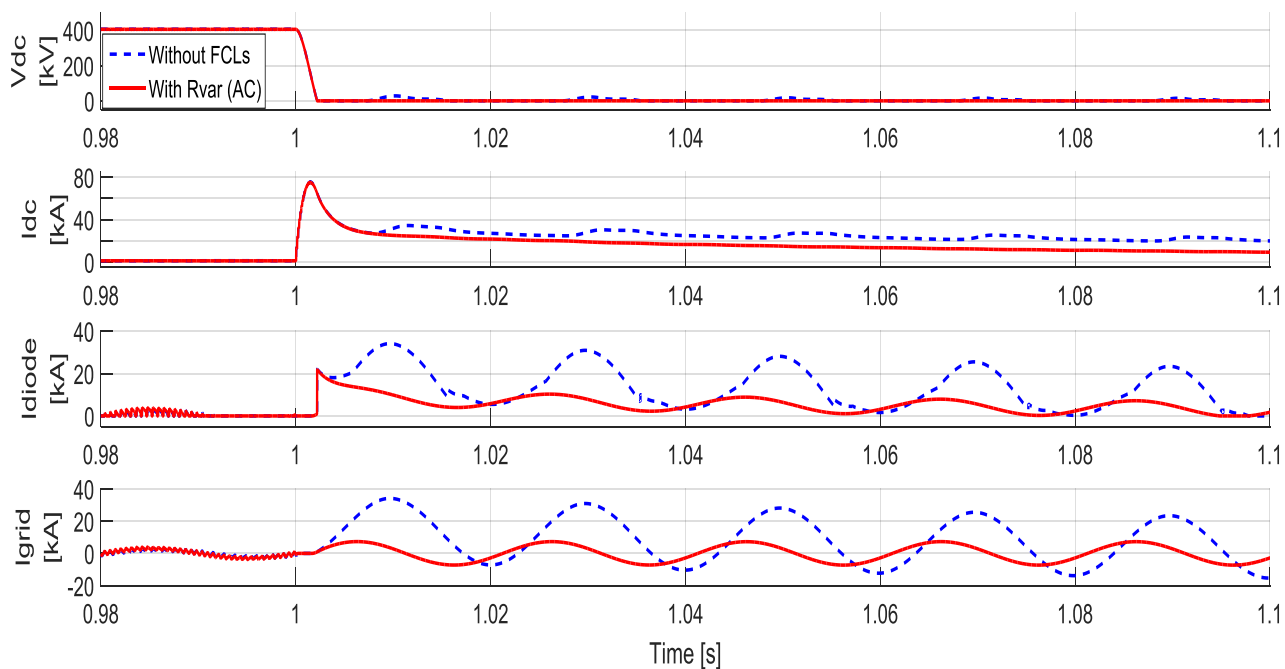
Figure 6.12 Fault Simulation Results with the Ideal Nonlinear Resistor on the AC Side (d=10km)

6.5 Proposed Current Limiting Scheme

As illustrated in sections above, current limiters can be installed on either DC or AC side, and the simulations show that none of the protective inductors on the DC side, LCL circuit on the AC side or nonlinear resistors on the AC side alone can effectively protect the system from the DC cable short circuit. Nonlinear resistors on the DC side in the simulation can somehow limit the fault current throughout all of the three fault development stages. However, this is based on the assumption of the ideal characteristics of the applied non-

linear resistors. In reality, there should be a delay for the temperature to rise and for the resistance to increase, and that both the temperature and resistance should go up as a continuous function instead of a step function. Moreover, the exact values of the resistance during the fault are difficult to determine regardless of the careful design. Besides the uncertainty in the design of the nonlinear resistors, the drawbacks of such components also includes that they are still under development and usually very expensive. All these factors have made nonlinear resistors not as desirable as the other options. Therefore, they will not be considered in the protection scheme to be proposed. In other words, the fault current limiting would be realized by the combination of the protective inductors installed on the DC side and the LCL circuit installed on the AC side.

To propose the current limiting scheme for the project, another Multiple Run procedure is simulated with various values for the protective inductors, this time together with the LCL circuits on the AC side designed as described in Section 6.3. Given the results shown in Table 6.3 and Figure 6.13, the protective inductors are temporarily select as L_protective=16mH so that the maximum fault current through diodes throughout the entire simulation period is less than 13kA (which equals the blocking threshold for IGBTs). This selection of the value is made also referring to literature [68] where the protective inductors are sized so that the fault current is limited to 12.2kA. Yet, if it turns out unsatisfactory in the later analysis of the protecting scheme, both LCL circuits or the protective inductors could be re-sized then. An optimization of the size is also determined by the trade-off between the security and economy of the project.

So for now, the current limiting scheme has been (temporarily) determined as follows:

- AC Side: LCL-VSC, with M_r=0.95 and r=1.02 for all three VSC stations
- DC Side: Protective Inductors, with L_protective =16mH for each side of every DC cable

The fault simulation results (d=10km) of each of the three VSC station based on such scheme are presented in Figure 6.14. Figure 6.15 further compares the measurements at the VSC_C2 side with and without the proposed schemes.

Table 6.3 Protective Inductor Sizing and Multiple Run Result with LCL-VSCs (d=10km)

	L_protective [mH]	I_D_max [kA]	I_cable_max [kA]
1	1	21.64	67.64
2	2	20.45	61.59
3	4	18.56	53.47
4	8	15.87	44.16
5	10	14.95	41.14
7	12	14.38	38.72
8	14	13.68	36.68
9	15	13.24	35.76
10	16	12.96	34.95
11	18	12.56	33.47
12	20	12.28	32.17
14	25	11.72	29.55
15	30	11.21	27.55
16	35	10.75	25.94
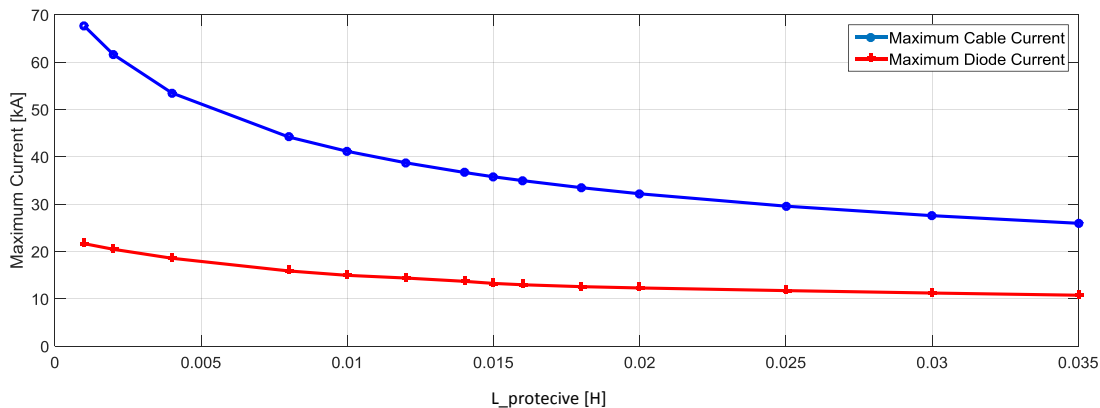
Figure 6.13 Protective Inductor Sizing and Fault Current Result with LCL-VSCs (d=10km)
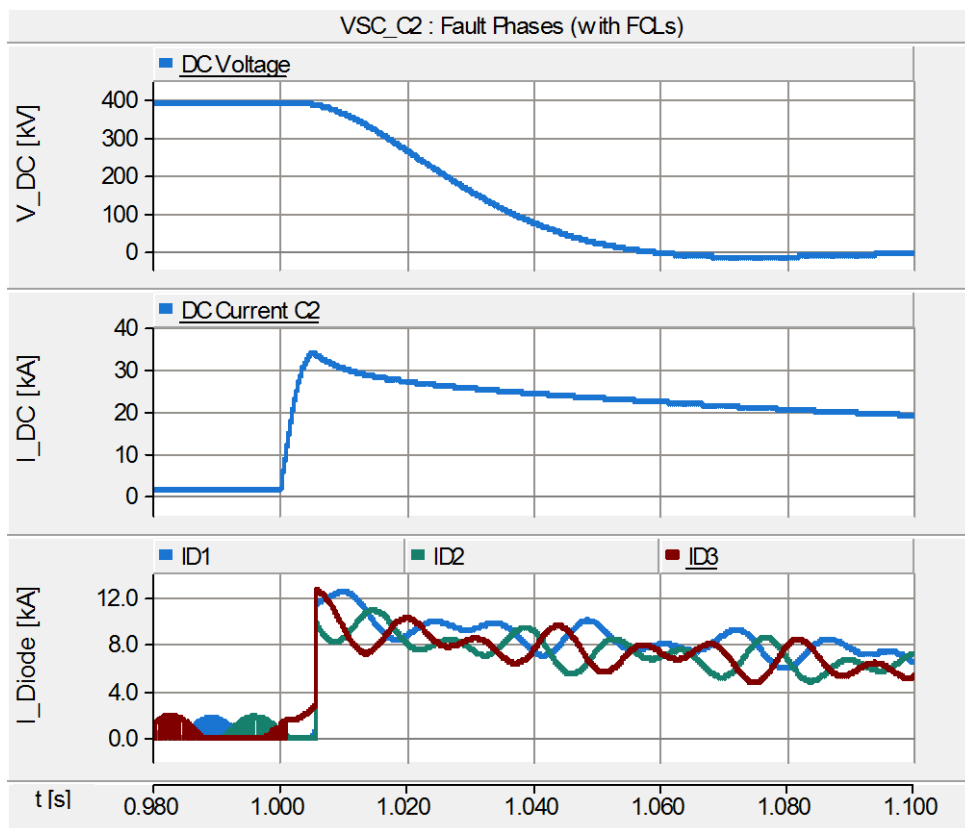
(a)
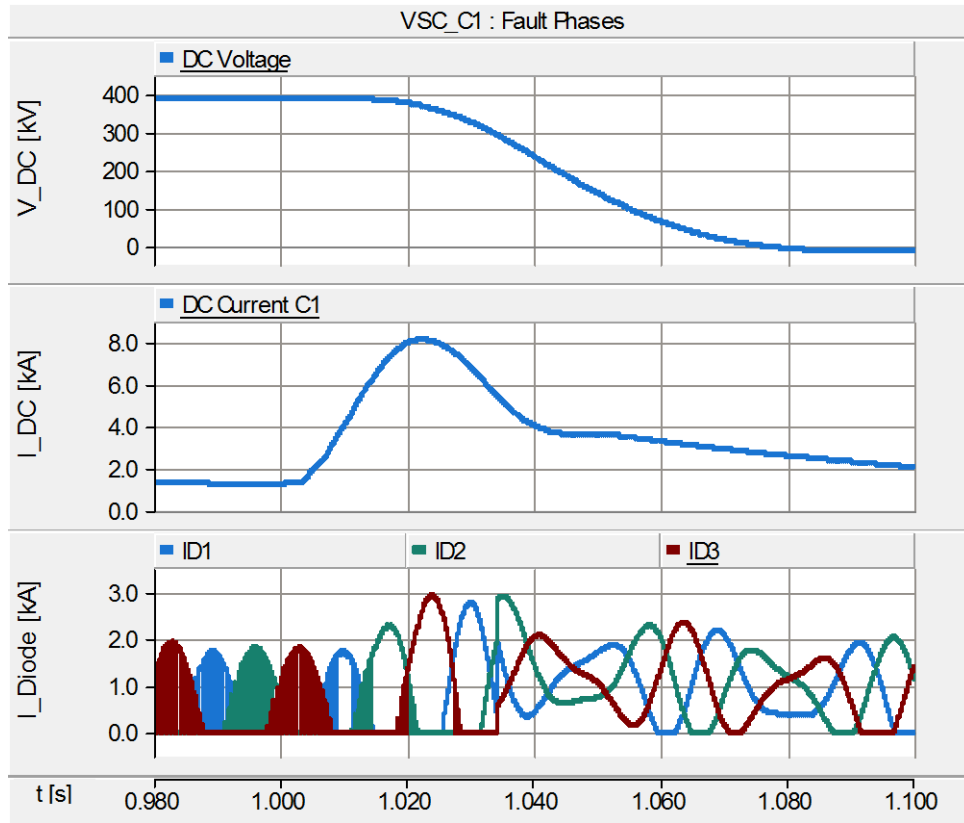
(b)
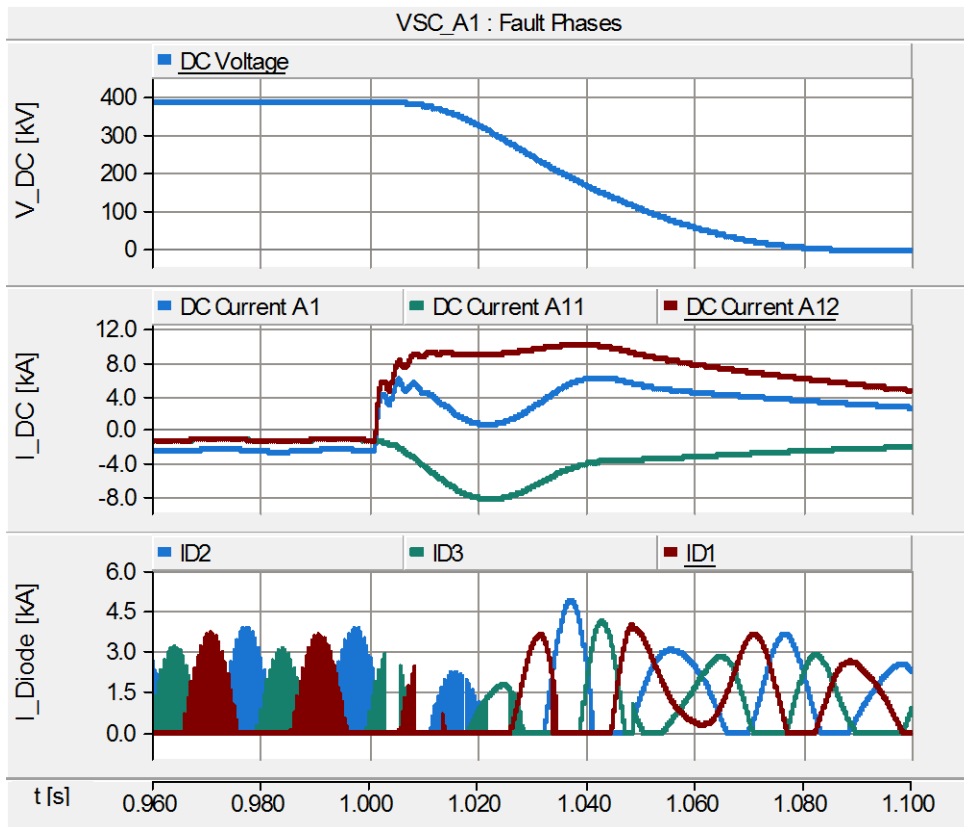
(c)

**Figure 6.14 Fault Simulation Results with the Proposed Current Limiting Scheme (d=10km) of
(a) VSC_C2; (b) VSC_C1; (c) VSC_A1**
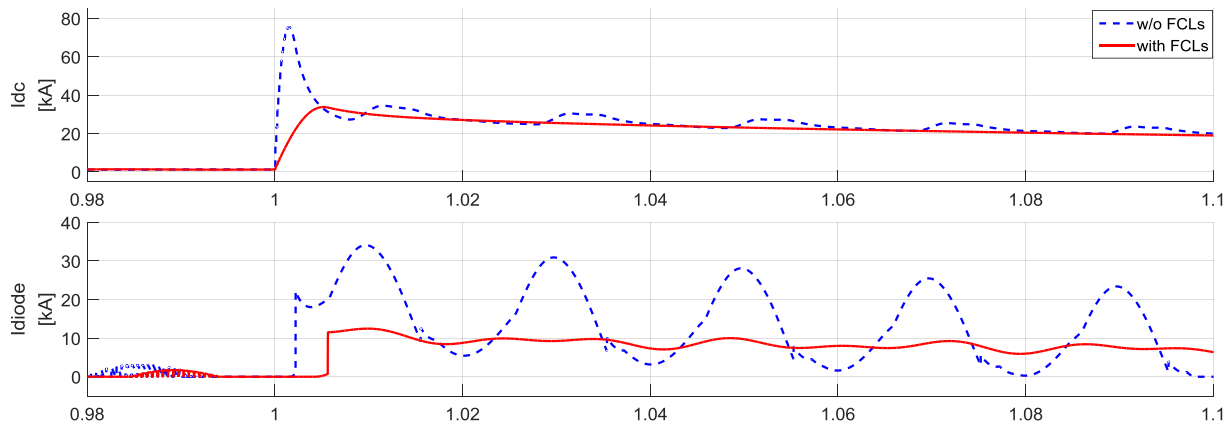
Figure 6.15 Comparison of DC Cable Current and Diode Current with and witout FCLs

Compared to those without FCLs, the DC voltage drops to 0 at a much slower speed. More specifically, it takes around 60ms (which is of the order of the action time of mechanical DCCBs) instead of around 1ms for the DC voltage to drop to 0 for VSC_C2, and even longer for VSC_C1 and VSC_A1. As for the fault currents flowing through the diodes, they are substantially limited to a smaller value within 13kA for every VSC stations when d=10km. For faults closer to the station, an overcurrent backup protection might be necessary to isolate the fault to prevent the impeding damage. Moreover, since the value of the detected DC currents differ from what have been discussed before in Chapter 4, the fault detecting and locating methods introduced before might either completely fail or require threshold resetting. Furthermore, as mentioned before, the designing parameters can be changed in the procedures for coordination or optimization issues. Another thing worthy noting is that the implementation of such FCLs also leads to a poorer dynamic performance, which is not desirable in starting up and load change. These respects will be further discussed in Chapter 7.

6.6 Summary and Discussions

In this chapter, different fault current limiting technologies have been introduced and tested in the target system, including:

- Protective inductors installed on the DC side
- An LCL circuit installed on the AC side
- Nonlinear resistors, such as superconducting FCLs, PTC-resistor FCLs and liquid metal FCLs, installed on either DC or AC side

Some conclusions obtained in this chapter can be summarized as follows:

- Current limiters can be installed on either DC or AC side, and usually the DC side FLC is responsible for limiting the current in 1st stage (the capacitor discharging stage) and 2nd stage (the diode freewheeling stage) while the AC side FCL for that in 3rd stage (the grid feeding stage).
- The simulations show that neither the protective inductors on the DC side nor the LCL circuit on the AC side alone can effectively protect the system from the DC cable short circuit.
- Nonlinear resistors based on superconducting materials, PTCs or liquid metals is effective in limiting fault current in theory, preferably installed on the DC side so that it can avoid the overcurrent of 2nd stage too. However, such devices are immature and usually expensive, and might not be very desirable in practice.

Based on the study, a fault current limiting scheme for the target system is proposed as below:

- AC Side: LCL-VSC, with M_r=0.95 and r=1.02 for all three VSC stations
- DC Side: Protective Inductors, with L_protective=16mH for each side of every DC cable

Simulation results show that the proposed scheme can effectively slows down the transient of the DC voltage drop and limit the DC current magnitude flowing through both diodes and DC cables during the fault. At the same time, the control system needs to be re-designed to comply with the new topology. Moreover, the fault detecting scheme may need some modification too. After installing the FCLs, some detecting methods will not be effective anymore; for others, the threshold needs to be reset. Another drawback of FCLs installations is that they will slow down the dynamics of the system. Last but not the least, the parameters adopted in the current limiting (M_r, r in LCL as well as L_protective in protective inductors) can be further optimized if necessary. These aspects will be addressed in more details in Chapter 7.

Chapter 7 Proposed Protection Scheme

Now that all the three aspects of fault detecting/locating, fault isolating and fault current limiting have been introduced, in this chapter, a comprehensive scheme to protect the target system from the DC cable short circuit faults will be proposed, tested and evaluated, taking all of the three aspects into consideration.

7.1 Introduction

When it comes to a protection system, there are several general requirements it has to meet; some are listed in literature [73]:

- Speed – the protection system interrupts the fault fast enough before further damage;
- Selectivity – the (main) protection algorithm only acts during the fault and only in the faulty part;
- Reliability – the protection system is reliable and should have backup plans;
- Sensitivity – the protection system is capable of detecting any fault in any operational point;
- Robustness – the protection system is able to discriminate faults from other disturbances;
- Seamlessness – the protection system keeps the healthy part in secure operations after the fault.

As mentioned before, when a DC cable short circuit occurs the current rises quickly to a large magnitude, making the protection requirements very demanding [74]. For one thing, the constraint in action time is extremely critical for the protection system, usually within a few milliseconds; actually, speed is often reckoned as the most stringing requirement for the DC protection system. For another, an incorrect tripping of the healthy lines would also significantly disturb the entire HVDC system and might lead to a total collapse of the grid [74].

The protection scheme aims to protect every component of the system from being damaged by the large fault current, the weakest among which are the anti-parallels diode of the converters [3, 22]. This is considered as the main constraint in the protection system. Literature [22] further suggests that <u>these diodes can only withstand a maximal current of 2 p.u.</u>, indicating that all of the fault detection, fault identification and fault isolation need to be completed within a few milliseconds.

In Section 7.2, a general description of the protection scheme for the target system will be given, combining the three aspects discussed before – fault detecting/locating algorithms, fault isolating tools as well as fault current limiting technologies. More design details such as threshold setting and relay coordination will be introduced in Section 7.3, while the evaluation of the scheme presented in Section 7.4.

7.2 General Description

In overall, each end of every cable as well as every busbar should be equipped with a protection relay, which is furthermore associated with the corresponding DCCBs, current sensors and relays [5, 22]. Since the fault clearance time is extremely demanding, speed is considered as the main concern throughout the process of (sensitively) detecting faults, (selectively) sending the trip signals to the corresponding DCCBs, and (reliably) isolating the fault from the healthy part of the system. During such procedure, time delay can be caused by fault propagation delay (from fault to the detecting point), fault detection delay (for reaching the threshold and necessary communication), fault interruption delay (from CB action to fault totally isolated). etc.. To extend the time constraint, appropriate current limiters are installed to gain more reaction time. Therefore, the selections of fault detecting/locating algorithms, DCCBs and FCLs need careful coordination, which will be discussed in more details in Section 7.3. Yet, this section summarizes the preliminary conclusions from the previous chapters to offer an overview of the protection scheme.

7.2.1 Fault Detecting/Locating

In Chapter 3, a feasible detecting and locating scheme has been proposed, briefly reiterated as below:

- Main fault detecting algorithm: <u>wavelet-based fault detection and differential protection</u>, the first based on local measurements while the second on fast communication media such as the optic fiber.
- Backup plan: <u>overcurrent protection</u>, though lacking in selectivity, it is a good candidate for backup plan upon extremely close-up faults, or a failure of (both) main fault detecting algorithms.
- Fault locating method: <u>travelling wave based fault locating</u>, with the wavefront arrival time determined by off-line data processing of current derivative and/or current wavelet coefficients.
- Auxiliary units: <u>A communication line</u> is required in the system for differential protection and Type D travelling wave based fault location, as well as the possibility to send trip signal to remote DCCBs. Apart from the communication lines, <u>derivative calculating units</u> may also help with detection selectivity and speed.

7.2.2 Fault Isolating

In Chapter 4, it is concluded that since AC breakers lack in both speed and selectivity in DC fault protection, competent DCCBs need to be designed and manufactured. In this project, only the clearance time of the DCCB is considered. Three types of DCCBs with their corresponding clearance time are concluded here:

- Mechanical breakers: <u>< 60ms</u>, usually in combination with FCLs.
- Semiconductor-based breakers: within <u>1 ms</u>.
- Hybrid breaker (I) : <u>2ms</u> achievable.

The selection will be made based on the critical time limit identified from fault analysis as well as the diode sizing. More details will be further discussed in the Section 7.3.

7.2.3 Fault Current Limiting

In Chapter 5, a current limiting scheme on both AC and DC side has been proposed, as shown in Figure 7.1.

- AC side: an LCL circuit, with design parameters as M_r=0.95 and r=1.02
- DC side: a pair of protective inductors installed on the DC side at each VSC stations, with design parameter as L_protective = 16 mH.

The possible optimization and final determination of the parameters adopted in the current limiting scheme will be discussed in more detail in Section 7.3.
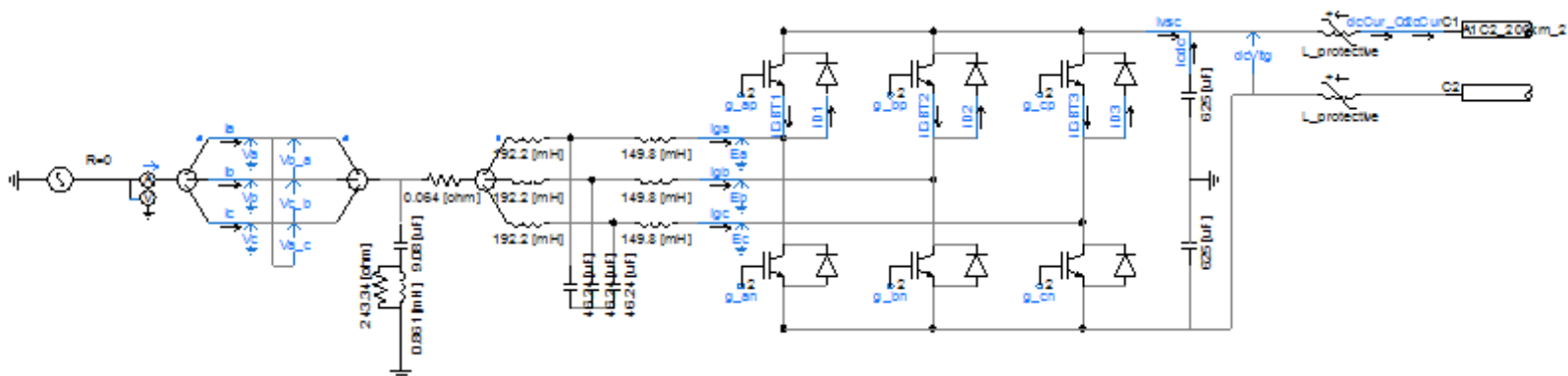
Figure 7.1 Current Limiting Scheme with temporary parameters (VSC_C2 as an example)

7.3 Detailed Design

Now that the general idea of the protection scheme has been described in the previous section, this section will focus on more details of each aspect, as well as the philosophy of coordination between these three aspects. Moreover, the procedure of possible optimization is also discussed in brief.

7.3.1 Fault Simulation with FCLs

To begin with the protection scheme design, fault simulations with different fault locations (d=1km, 10km, 100km, 190km & 199km) are once again conducted, this time with the designed FCLs, i.e. the LCL circuit (M$_r$=0.95, r=1.02) and protective inductors (L_protective=16mH). Note here that although it can be concluded from the earlier study that the extreme cases always occur when d=1 and/or d=199km, all fault scenarios are simulated in this section since the main detecting method are not necessarily to cover the entire length of the cable. Actually, as illustrated before, faults close up to the station can be protected by the backup overcurrent protection algorithm. The simulation results with FCLs under the five pre-set fault scenarios are also presented in _Appendix F_, in comparison of the ones without FCLs. Among the large amount of data obtained, three groups are of special interest here, namely:

- Maximum current flowing through DC cables; the results are summarized in Table 7.1.
- Maximum current flowing through diodes; the results are summarized in Table 7.2.
- Critical time limit, which equals the time spent from the fault occurrence till the any diode current exceeds 2 p.u.; however, this is also related to the diode sizing and will be discussed below.

Table 7.1 Maximum Operational and Fault Current (within 100ms) in DC Cables

Maximum DC Current [kA]						
	Normal Operation	Fault Scenario (d=1km)	Fault Scenario (d=10km)	Fault Scenario (d=100km)	Fault Scenario (d=190km)	Fault Scenario (d=199km)
I_DC @ C2 (Faulty)	1.4	39.1	33.8	15.9	11.3	11.02
I_DC @ C1 (Healthy)	1.4	8.1	8.2	9.9	10.6	10.58
I_DC @ A12 (Faulty)	-1.4	10.0	10.1	14.1	33.3	38.5
I_DC @ A11 (Healthy)	-1.4	-8.3	-8.4	-10.4	-10.7	-10.7

Table 7.2 Maximum Operational and Fault Current (within 100ms) in Diodes

Maximum Diode Current [kA]						
	Normal Operation	Fault Scenario (d=1km)	Fault Scenario (d=10km)	Fault Scenario (d=100km)	Fault Scenario (d=190km)	Fault Scenario (d=199km)
I_D_max @ C2 (Faulty)	2.0	15.2	12.7	6.3	5.1	4.9
I_D_max@ C1 (Healthy)	2.0	2.9	3.0	3.8	4.8	4.8
I_D_max @ A1 (Voltage Support)	3.9	4.9	4.9	5.5	9.5	14.1

Here are a couple of more comments on the last point:

- Although the large fault current can damage the DC cables as well, it is usually acknowledged that they are more robust due to their thermal mass [3]. In other words, during the DC short circuit faults, it is the diodes that determine the time constraint for the protection system.
- Nevertheless, it is also possible to oversize the diodes to take some burden off the protection scheme so that slower and cheaper devices such as mechanical DCCBs can be competent, as will be discussed later in Case 2 in Section 7.3.3. Under such circumstances, it is likely that the cables become the more vulnerable component and will determine the critical time limit.
- Of course, like diodes the cables can be oversized as well, but this should take into account the technical and economic aspect, i.e.: if the scheme with mechanical DCCB and oversized components is better-performed and/or cheaper than the solid-state or hybrid DCCB with rated-sized components.
- However, in the proposed protection scheme, the diodes are invariably assumed to be the most vulnerable component, no matter if any of the diodes and cables is oversized or not. Yet, since the backup overcurrent protection is also included in the protection scheme, the relay threshold can always be coordinated to the maximum cable current capacity in practice for cable protection.

7.3.2 Threshold Setting and Relay Coordination

In Chapter 4, some fault detecting and locating methods have been introduced and simulated, each with a temporarily proposed threshold. Based on the results, the fault detecting scheme is designed as such that the wavelet-based detecting method and differential protection act as main protection algorithms while overcurrent protection as backup plans. Fault locating is performed based on the offline data processing. However, the installation of FCLs will affect the current transient and challenges the validity of these detecting method. In this part, the previous proposed methods will be tested and calibrated based on the FCL-MTDC system.

Wavelet-based Fault Detection

The wavelet-based fault detection detects the fault by comparing the corresponding wavelet coefficient to a pre-set threshold. This algorithm is fast and reliable since it is based on the local measurements and does not need communication. On the downside, it requires high sampling rate and large data storage and processing.

The maximum magnitude of 6th detail wavelet coefficients of 6-level Haar wavelet transform in normal operation and different fault scenarios of each VSC with the designed FCLs are summarized in Table 7.3. As can be seen from the recorded data, the following conclusions can be drawn:

- When a fault occurs, the magnitude in every detecting point rises distinctively, which can be used as an indication of safe/fault mode.
- During a fault, the difference between the magnitude of the faulty part and healthy part can be distinguished easily, guaranteeing the selectivity of the method.
- Based on the data listed in Table 7.3, the threshold can be temporarily set as 0.5. This could later on be optimized to achieve better performance (such as in sensitivity, selectivity, reliability, etc.) of the detecting scheme. More details will be referred to in Section 7.3.4.
- With the threshold of 0.5, the detection time in each case can be determined; they are listed in Table 7.4.

Table 7.3 6th Level Detail Wavelet Coefficients Maximum Magnitude (with FCLs)

	Wavelet Coefficient Maximum Magnitude [kA]					
	Normal Operation	Fault Scenario (d=1km)	Fault Scenario (d=10km)	Fault Scenario (d=100km)	Fault Scenario (d=190km)	Fault Scenario (d=199km)
I_DC @ C2 (Faulty)	0.005	1.87	1.61	1.62	1.39	1.34
I_DC @ C1 (Healthy)	0.005	0.09	0.09	0.13	0.27	0.29
I_DC @ A12 (Faulty)	0.004	1.36	1.40	1.62	1.59	1.83
I_DC @ A11 (Healthy)	0.004	0.09	0.09	0.12	0.23	0.24

Table 7.4 Wavelet-based Fault Detection Method Detecting Time (with FCLs)

	Fault Detecting Time (threshold=0.5) [ms]				
	Fault Scenario (d=1km)	Fault Scenario (d=10km)	Fault Scenario (d=100km)	Fault Scenario (d=190km)	Fault Scenario (d=199km)
I_DC @ C2	0.64	0.64	1.28	1.92	1.92
I_DC @ A12	1.92	1.92	1.28	0.64	0.64

Table 7.5 6th Level Detail Wavelet Coefficients Maximum Magnitude (without FCLs)

	Wavelet Coefficient Maximum Magnitude [kA]				
	Fault Scenario (d=1km)	Fault Scenario (d=10km)	Fault Scenario (d=100km)	Fault Scenario (d=190km)	Fault Scenario (d=199km)
I_DC @ C2 (Faulty)	40.76	8.64	2.9	1.89	1.87
I_DC @ C1 (Healthy)	0.11	0.11	0.11	0.60	0.88
I_DC @ A12 (Faulty)	1.37	1.91	2.9	8.71	40.3
I_DC @ A11 (Healthy)	0.07	0.07	0.1	0.41	1.22

Compared to the case without FCLs as listed in Table 4.4 (also relisted here as Table 7.5), the following results can be made:

- The installation of FCLs slows down the transient response, resulting in lower magnitudes in almost all the wavelet coefficients. However, the selectivity in distinguishing the faulty and the healthy line is still guaranteed.

- Actually, the selectivity even increases given the measurements are accurate enough. For example, when without FCLs, the data for A12, d=1km and for A11, d=199km are 1.37 and 1.22 respectively, making the threshold setting a bit tricky. However, after installing the FCLs, the magnitude for them become 1.36 and 0.24, with the former as large as 5.7 times of the latter.

Differential Protection

Differential protection detects a fault by comparing the current sum to a pre-set threshold. This detecting method requires telecommunication which will causes time delay. Therefore, literature [22] puts forward that only the fast communication link of optic fiber (200km/ms) could be used, and that the length of

DC cables should be within 200km. In this project, both cables are 200km in length and each accompanied with an optic fiber communication line. Therefore, the communication delay is 1ms. Similar to what have been discussed earlier, the current sum is calculated by adding the real-time data from the local measurement to the 1ms-old history data received from the remote measurement. The simulation result after the installation of FCLs are summarized in Table 7.6.

Table 7.6 Differential Protection Study (with FCLs)

	Magnitude of Current Sum [kA]					
	Normal Operation	Fault Scenario (d=1km)	Fault Scenario (d=10km)	Fault Scenario (d=100km)	Fault Scenario (d=190km)	Fault Scenario (d=199km)
I_sum@C2 (Faulty)	0.04	47.1	41.0	29.6	43.4	49.2
I_sum@C1 (Healthy)	0.04	0.46	0.46	0.57	1.22	1.33
I_sum@A12 (Faulty)	0.03	47.4	41.5	29.8	43.4	48.9
I_sum@A11 (Healthy)	0.03	0.79	0.81	1.32	2.26	2.42

Table 7.7 Differential Protection Detecting Time (with FCLs)

	Fault Detecting Time (threshold=1.5 for C1 &C2; 2.5 for A11 &A12) [ms]				
	Fault Scenario (d=1km)	Fault Scenario (d=10km)	Fault Scenario (d=100km)	Fault Scenario (d=190km)	Fault Scenario (d=199km)
I_DC @ C2	0.13	0.13	0.64	1.09	1.1
I_DC @ A12	1.15	1.12	0.71	0.27	0.22

Based on the recorded data, the following conclusions can be drawn:

- When a fault occurs, the current sum in every detecting point rises distinctively, which can be used as an indication of safe/fault mode.
- During a fault, the difference between the magnitude of the faulty part and healthy part is easy to distinguish, guaranteeing the selectivity of the method.
- Based on the data listed in Table 7.6, the threshold can be temporarily set as 1.5 for C1&C2, and 2.5 for A11&A12. This could be further optimized to achieve better performance (such as in sensitivity, selectivity, reliability, etc.) of the detecting scheme. More details will be discussed in Section 7.3.4.
- With the threshold set as mentioned above, the detection time in each case can be determined; they are listed in Table 7.7.

Compared to the case without FCLs as listed in Table 7.8, the following results can be made:

- The installation of FCLs limits the current magnitude, therefore most of the magnitude of the current sums become smaller after the installation of FCLs.
- However, it is still easy to distinguish the faulty line from the healthy line by the updated threshold.

Table 7.8 Differential Protection Study (without FCLs)

	Magnitude of Current Sum [kA]				
	Fault Scenario (d=1km)	Fault Scenario (d=10km)	Fault Scenario (d=100km)	Fault Scenario (d=190km)	Fault Scenario (d=199km)
I_sum@C2 (Faulty)	220.86	74.11	49.64	81.87	227.36
I_sum@C1 (Healthy)	0.48	0.48	0.43	2.09	2.47
I_sum@A12 (Faulty)	227.90	80.83	49.67	76.09	220.43
I_sum@A11 (Healthy)	0.698	0.698	0.91	4.50	5.40

Comparing the detecting time of wavelet-based fault detecting method (Table 7.4) and that of differential protection (Table 7.8), one can notice that in spite of the communication delay, differential protection is even faster than the wavelet-based fault detection in this specific case. Yet, the reliability and synchronization of the telecommunication link poses as major concern [22]. To reduce the false alarm caused by communication error, a time window can be set. For example, a fault will be detected only if the current sum exceeds the threshold for 3 consecutive samples (the length of time window is determined empirically from the simulation results) [22]. In case of long-period or permanent communication failure, it is always possible to rely on the wavelet-based protection scheme, which is slightly slower but still within 2 milliseconds in this case. Moreover, for better performance, a blocking time can also be set when the current sum exceeds a negative threshold.

Overcurrent Protection

Overcurrent protection detects a fault by comparing the current measurement to a pre-set threshold. Though lacking in selectivity, overcurrent is a good candidate to deal with the situation when:

- The faults are extremely close to the station;
- Both of the wavelet-based fault detecting method and differential protection fail.;
- Since the diodes are oversized, the cables might become the more vulnerable component, and the overcurrent protection can help with this too;
- In case of DCCB failures, overcurrent protection relay at busbars can disconnect the VSC station.

In practice, a series of time-delayed and instantaneous overcurrent protection can be coordinated and installed to cover all the necessities in back-up scheme. In this project, it is simplified into an instantaneous overcurrent relay with a set threshold. Based on the data in Table 7.1, the threshold is temporarily set as 10kA. Once again, this could be adjusted and optimized to achieve better performance (such as in sensitivity, selectivity, reliability, etc.) of the detecting scheme. More details will be referred to in Section 7.3.4.

Travelling Wave Based Fault Locating

As described earlier, the fault location is determined based on the travelling wave, the wavefront of which detected by the offline data of current derivative and/or wavelet coefficient. After the installation of FCLs, the travelling wave transient is somewhat changed mainly due to the inserted protective inductor. As a result, Type A can no longer work in this case. Figure 7.2 shows the difference in current transient behavior with and without FCLs. It further proves that the inserted inductors impede the transient response after fault, resulting in a failure in the Type A locating principle. However, Type D estimates the fault location by the time difference of the wavefront arrival time in two sides, and since both sides of the cable are assumed to be equipped with the identical protective inductor, Type D travelling wave fault locating method seems not to be affected too much

by the installation of FCLs. Nevertheless, as pointed out before, Type D requires communication and GPS installation, which will make it more expensive than Type A.
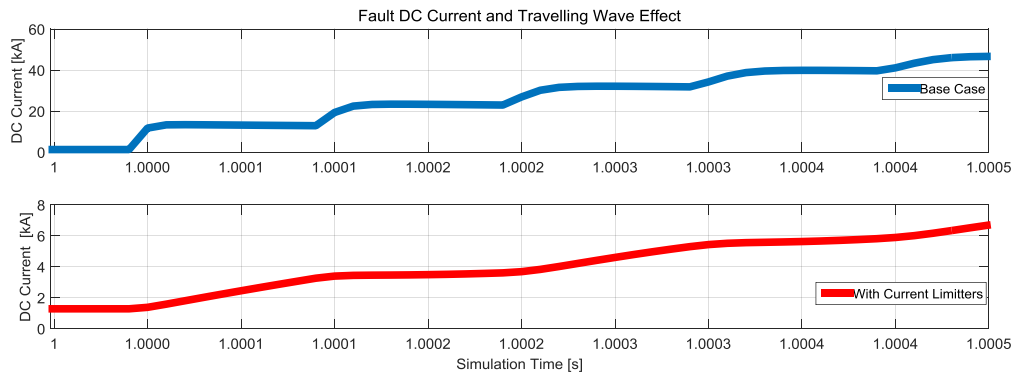

Figure 7.2 Post-fault DC Current Transient without and with protective inductors (d=10km)

Like wavelet coefficient, since the installed FCLs soothes the transient, the magnitude of the current derivatives is reduced in general; yet it does not affect the detection of wavefront arrival. Similar to what have been introduced in Section 4.4, the recorded data can be plotted and the arrival time can be read from the plots. The results of the fault distance estimation based on Type D travelling wave fault location method as well as the minimum time window of the data collection of each estimation are summarized in Table 7.9. Once again, the fault locating based on current derivatives outperforms that based on wavelet coefficient in both accuracy and (data) space efficiency when noise is not considered.

Table 7.9 Travelling Wave Protection Study (with FCLs)

		Performance				
D		1	10	100	190	199
Current Derivative	Minimum Time Window [ms]	1.02	0.97	0.5	0.97	1.02
	Estimated Distance [km]	0.01	8.92	100	191.08	199.99
	Absolute Error [km]	0.99	1.08	0	1.08	0.99
Wavelet Coefficient	Minimum Time Window [ms]	1.66	1.62	1.14	1.62	1.66
	Estimated Distance [km]	-0.98	6.94	100	193.06	200.98
	Absolute Error [km]	1.98	3.06	0	3.06	1.98

One may notice that in the case when d=1km and 199km, the locating indicates that the fault is out of the faulty line. However, since the fault location is conducted <u>after</u> the fault detection and identification so that selectivity is not of concern here anymore. As a result, the results of estimation of either -0.98km or 200.98km simply indicates that the fault is extremely close to VSC_C2 or VSC_A1.

Another thing worth noting is that since the cable is only 200km in length and the travelling speed is calculated as 198km/ms in theory, the travelling wavefront can always be detected within 1.01ms after the fault for the faulty line. On the other side, even the fastest DCCBs (solid state breakers) need 1ms for fault isolation, and that the fault detection will also takes time. Therefore, the recorded data is almost always large enough for travelling wave based fault locating.

7.3.3 Diode Sizing and DCCB Selection

In this report, only the clearance time of the DCCB is considered in selection. In other words, DCCB is configured based on the speed requirement identified by the critical time limit under fault conditions [3]. The critical time limit is further determined by the time constraint related to the most vulnerable component, diodes. In this section, the DCCB type will be determined for two cases with different diode sizing strategies.

Case 1: With Rated-sized Diodes

According to the simulation results, the maximum diode current in normal operation is 2kA for VSC_C1 and VSC_C2, and 3.9kA for VSC_A1. When the diodes are sized with such rated values, the latest time that a fault has to be isolated is the instant when the current flowing through diodes exceeds 2 p.u., namely 4kA for VSC_C1 and VSC_C2 and 7.8kA for VSC_A1. Such results are summarized in Table 7.10, where '-' indicates that the diode current has not exceeded 2p.u. throughout the 100ms of the post-fault simulation period.

Table 7.10 Critical Time Limit for Fault Isolation

	Diode Sizing (1 p.u.) [kA]	Instant when Diode Current Exceeds 2 p.u. [ms]				
		Fault Scenario (d=1km)	Fault Scenario (d=10km)	Fault Scenario (d=100km)	Fault Scenario (d=190km)	Fault Scenario (d=199km)
VSC_ C2 (Faulty)	2.0	5.1	5.7	11.8	17.6	18.1
VSC_C1 (Healthy)	2.0	-	-	-	22.9	22.5
VSC_ A1 (Voltage Support)	3.9	-	-	-	6.2	5.5

The conclusion is that if the protection scheme can selectively clear the fault within 5.1ms, in theory the system can be effectively protected. Needless to say, mechanical DCCBs with its clearance time as long as 60ms cannot be used in this case. As described in Section 7.3.2, the clearance time for the two main protections scheme, differential protection (Diff) and wavelet based fault detection (WT) are relisted in Table 7.11.

Table 7.11 Detection Time for Main Fault Detecting Methods (with FCLs)

Fault Detecting Time [ms]										
d	1km		10km		100km		190km		199km	
Type	Diff	WT	Diff	WT	Diff	WT	Diff	WT	Diff	WT
I_DC @ C2	0.13	0.64	0.13	0.64	0.64	1.28	1.09	1.92	1.1	1.92
I_DC @ A12	1.15	1.92	1.12	1.92	0.71	1.28	0.27	0.64	0.22	0.64

As can be read from the table, a possible 'worst case' happens when the fault is 1km from either VSC station and that the communication for differential protection fails, leading to the detecting time as 1.92ms. Given the assumption that a Hybrid I DCCB is able to clear the fault within 2ms after trip signal regardless of the current magnitude and so on, it seems satisfactory to use Hybrid I DCCB in this case (1.92+2=3.92ms <5.1ms). Moreover, the overcurrent protection is designed as backup plan, which should also be coordinated with the two main fault detecting algorithms as well as the time constraint of 5.1ms.

Case 2: With Oversized Diodes

As mentioned before, if one desires to use the cheaper mechanical DCCBs, apart from installing FCLs of appropriate parameters, it is also useful to oversize the diodes to withstand the large fault current. Since the FCL parameters are determined to constrain the fault current in diodes within 13kA when d=10km, in this part, a simple example is given when all of the diodes are sized as 6.5kA, so that they can always withstand faults when d = 10 ~ 190 km.

For the closer up faults, overcurrent protection will act as the backup plan. Moreover, since the diodes are oversized, it is likely that the DC cables become more vulnerable than the diodes. This can be solved either by including it in overcurrent relay setting or oversizing the DC cables too. Above all, all of the sizing and threshold setting should be a result from the trade-off study and will not be discussed further here in this report.

7.3.4 Coordination and Optimization Principles

So far, several aspects in the detailed design of the protection scheme such as FCL installation, relay setting and DCCB selection have been discussed. For a more structured delivery, these three aspects are introduced separately in the previous sections from 7.3.1 to 7.3.3. However, in real cases, they are always interacting with one another, and the coordination among them is of critical importance in the entire design procedure.

With a bit of sheer luck, the previously proposed sizing of FCLs and the suggested threshold for relay setting seem to go well with the selected DCCB type in both Case 1 and Case 2. If this were not true at the first trial, either the size of the FCLs need to be re-designed or the threshold of the detecting relays needs to be reset.

A general idea of design and coordination is described as below:

1) Firstly, based on the fault response of fault simulation (without FCLs), arbitrary determine a set of parameters for designing FCLs.

2) Secondly, based on the simulation with the designed FCLs, determine the threshold for fault detecting scheme which should be selective and fast enough. If this is not possible, keep going back to step 1) and try another combination of FCLs configurations.

3) Thirdly, based on the critical time limit and detecting time for the main detecting algorithms, select the DCCB type. If no DCCB type is satisfactory, go back to step 2) to reset the threshold. If threshold reset is not possible to solve the problem, go back to step 1) to redesign the FCLs. Sometimes oversizing the diode or DC cables can be a solution as well. Besides, resizing the DC capacitors is yet another possibility.

4) Afterwards, based on the already determined part of the protection scheme as well as the cable property, set the scheme for backup overcurrent protection(s).

5) After finding a feasible solution such as the one proposed above, the scheme could be further optimized by once again going through step 1) to step 4) while constantly comparing the technical feasibility, economic cost and other aspects among the proposed schemes.

Another possible yet simple optimization is related to reducing the fault detecting time by auxiliary unit as mentioned earlier. When it comes to auxiliary unit in fault detecting, first of all, a communication line is required in the system for differential protection and Type D travelling wave based fault location, as well as the possibility to send trip signal to remote DCCBs. Apart from the communication lines, derivative calculating unit may also help with detection selectivity and speed. The fault detecting time of the system in the relative extreme case of d=1km and 199km under the following three conditions are summarized in three sets in Table 7.12:

- Set A: no auxiliary unit, only with trip signals from the local relay.

    In this set, the detection time of the system is the larger detecting time of VSC_C2 and that of VSC_A1 (refer to Table 7.11).

- Set B: with communication unit, so that the CB can receive trip signal from the remote relay.

    In this set, for each VSC station the detection time is the minimum value between:

    o   1) the remote relay detection time adding 1ms communication delay

    o   2) the local relay detection time.

    And once again, the detecting time of the system is the larger detecting time between VSC_C2 and VSC_A1.

- Set C: with polarity of the derivative to help distinguish the faulty and healthy line by Data A11 and Data A12; communication is also included in this set.

    In this set, the detection time of the system is still the larger one between A1 and C2, while the detection time for A1 is the smallest among the detection time:

    o   1) based on derivative polarity

    o   2) based on the local trip signal

    o   3) based on the remote trip signal adding 1ms communication delay

    And the detection time for C2 is the smallest among the detection time:

    o   1) based on derivative polarity adding 1ms communication delay

    o   2) based on the local trip signal

    o   3) based on the remote trip signal adding 1ms communication delay

Table 7.12 Detection Time w/o and with Auxiliary Unit (with FCLs)

Detection Time [ms]				
		Set A	Set B	Set C
d=1km	Diff	1.15	1.13 (1)	1.01 (1)
	WT	1.92	1.64 (1)	1.01 (1)
d=199km	Diff	1.10	1.10 (2)	1.01 (1)
	WT	1.92	1.64 (1)	1.01 (1)

Based on the results, it is concluded that the detecting time for the 'worst case' of 1.92ms can be reduced to 1.01ms with the related auxiliary components of communication line and derivative unit.

7.4 Evaluation

In this section, the proposed protection scheme will be evaluated according to the requirements introduced in Section 7.1.

7.4.1 Speed

According to the simulation results discussed in Section 7.3, the proposed protection scheme can effectively isolate the fault within the critical time limit (assuming overcurrent backup protection is well designed), so that no diodes or other components in the system will be damaged. Therefore, the protection scheme is deemed as fast.

7.4.2 Selectivity

The selectivity is guaranteed by the threshold setting, as described in Section 7.3.2. Therefore, the requirement of selectivity is also met. Yet, another issue in selectivity might arise when coordinating the overcurrent backup protection with the main protections. An appropriate time lag needs to be implemented in the former to provide a deal of selectivity. Nevertheless, in cases of extreme fault current, selectivity can be sacrificed to a certain degree and that fast fuses or instantaneous overcurrent protection is necessary in the scheme as well.

7.4.3 Reliability

The reliability of the protection scheme is guaranteed by the two main protection algorithm as well as the overcurrent backup protection. Even if all forms of protection from the DC side fail, the CB from the AC side can still trip and disconnect the fault.

7.4.4 Sensitivity

The sensibility of the protection system includes two aspects. First, it should be capable of detecting any fault; second, such faults can be detected at any operational point too.

For the first aspect, in the simulation DC cable short circuit faults of various fault distances have proved the effectiveness of the protection scheme regardless of the fault location. However, since only bolt, permanent and pole-to-pole DC cable faults are considered in this project, the sensitivity in different fault types such as faults with impedance, pole-to-ground faults, AC faults, etc. needs to be further studied in the future.

For the second aspect, fault simulations under degraded production (100MW) and (slight) over-producing (600MW) scenarios are studied as well. The results manifest that both differential protection and wavelet-based fault detection are still effective and almost as fast and selective as in rated operation with the thresholds set previously.

7.4.5 Robustness

The robustness of the protection system means that it should be able to discriminate faults from other disturbances, such as setpoint changes, noises, etc.

A simulation of load change test on VSC_C2 is conducted on the target system with the proposed protection scheme, similar to the one conducted before in Chapter 2 for model verification; the results of the system behaviors of the system are shown in Figure 7.3. Compared to Figure 7.4 (without FCLs), it can be seen that the installation of FCLs significantly slows down the dynamics of the system. Therefore, a trade-off should be carefully considered before making the final decision in the real practice. Yet, the system still follows the control after around 20ms.

According to the simulation results of all of the fault detecting methods of overcurrent protection, differential protection derivative-based fault detection, wavelet transform-based fault detection (as presented in *Appendix I*), the proposed scheme will not at all be disturbed by the start-up or load changes. In other words, the protection system can be regarded as robust.
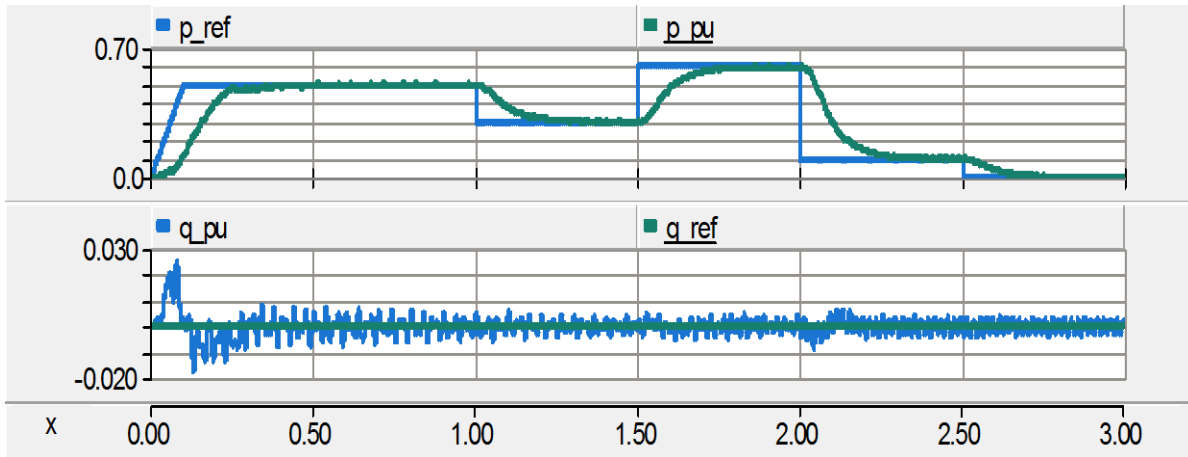
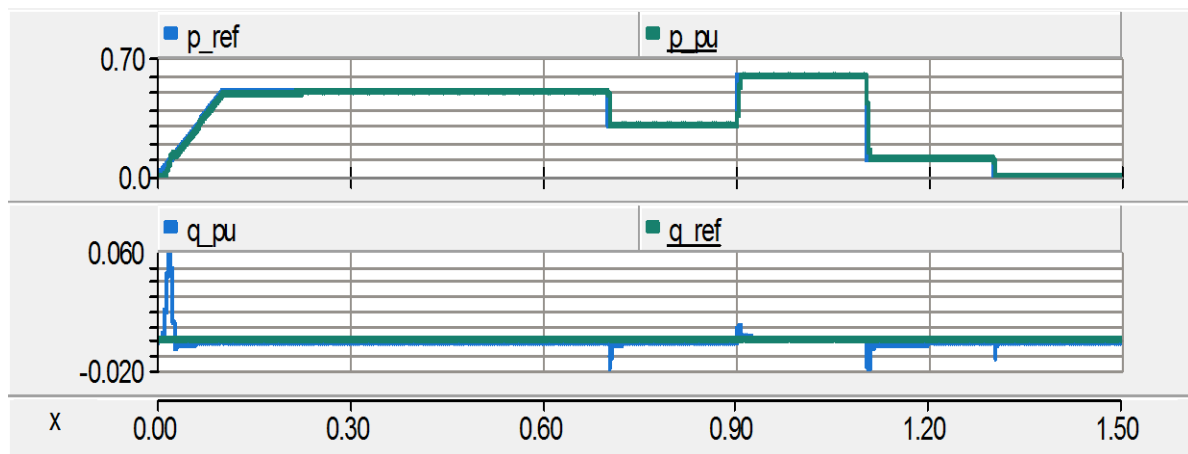**Figure 7.3 Load Change Test with FCLs (values in p.u.)**

Figure 7.4 Load Change Test without FCLs (values in p.u.)

7.4.6 Seamlessness

A protection scheme is seamless if the remaining part of the system could still operate in safe state after the fault clearance. This, however, is reckoned as a drawback of the proposed scheme. The simulation shows that even after the corresponding DCCBs are open after the time delay of 3.92ms, the remaining system which is comprised of VSC_A1 and VSC_C1 still fails to go back to the normal operational state automatically. This might result from the failure in DC voltage restore. To tackle with this problem, more studies in control strategy in DC voltage control or post-fault reboot need to be carried out in the future, such as the 'parallel controller' proposed by literature [48].

7.5 Summary and Discussions

In this chapter, a protection scheme has been proposed for the target system based on the preliminary conclusions drawn from the previous studies. The chapter starts with the definition for some general requirements of a protection system (speed, selectivity, reliability, sensitivity, robustness and seamlessness). It also defines the main constraints in the scheme designing, i.e. the diodes cannot withstand a current above 2 p.u.. Afterwards, the general principle and a more detailed illustration of the protection scheme are presented in Section 7.2 and 7.3 respectively.

In summary, the protection scheme is designed as below:

- Fault Current Limiting Sub-scheme
  - AC Side: an LCL circuit (M_r=0.95, r=1.02) for each VSC station
  - DC Side: a protective inductor of 16mH installed on each end of every DC cable
- Fault Detecting/Locating Sub-scheme:
  - Detecting:
    - Main Algorithm 1: differential protection
      Threshold: VSC_A1: 2.5kA; VSC_C1/C2: 1.5kA.
    - Main Algorithm 2: wavelet-based fault detecting method
      Sampling rate: 10µs; Threshold: 0.5.
    - Backup plan: overcurrent protection, threshold to be determined depending on the cable and CB properties and other issues in reality
    - Auxiliary Components: an optic fiber communication line for each cable;
      current derivative calculating units (optional)
  - Locating:
    - Type D travelling wave based fault location method
    - Wavefront arrival time detected by the off-line data processing from the data recorded during the fault, such as wavelet coefficients and current derivatives
    - Requires high sampling and synchronized communication
- Fault Isolating Sub-scheme:
  - The Hybrid I type DCCB with clearance time within 2ms can be adopted in the case when the diodes for VSC_C1/C2 are sized for 2kA and VSC_A1 for 4kA
  - If all the diodes are oversized to withstand current as high as 13kA, the mechanical DCCBs might also be feasible when the backup overcurrent protection is properly coordinated and that the DC cables are strong enough.

Nevertheless, the proposed scheme is only *an* example among all the feasible ones, but not *the* one; some general ideas in optimization are also briefly described in Section 7.3. Finally, Section 7.4 focuses on the evaluation of the proposed scheme based on the requirements introduced in Section 7.1.

In overall, the proposed scheme is generally considered to be fast, selective, reliable, sensitive and robust. Yet, more follow-up projects and future improvements need to be performed regarding the selectivity to other fault types, post-fault seamlessness, dynamic behavior of the system, etc.

Furthermore, in the project the DCCBs are to a large extent simplified into an ideal time-delayed switch. Issues such as breaking capability, the interruption procedure of CBs, and above all, the designing of a more practical type of DCCB still worth more attention and research in the future.

Last but not the least, although the proposed scheme is based on the target system, the general principle in protection system design should be similar for other grid topology. Nevertheless, particular issues might arise with the increase of terminal numbers and the complexity of the network, or a change in VSC and cable configuration. How to generalize the protection scheme proposed in this project to a larger extent is yet another interesting direction for future research.

Chapter 8 Conclusions

8.1 Summary

Along with the development of the offshore wind farms, VSC-HVDC/MTDC technology is getting an increasing amount of interest and attention in the long-distance and large-capacity transmission. However, the extreme vulnerability to DC contingencies of VSCs remains a challenge in both research and practice. DC cable short circuit faults, though less common than DC cable ground faults, can cause the most severe damage to the VSC as well as the whole system. The final goal of this thesis project is to propose a comprehensive protection scheme to protect the self-built MTDC system from the DC cable short circuit faults, taking into consideration all the three aspects in fault detecting/locating, fault isolating and fault current limiting.

For this purpose, in Chapter 2 a dynamic model of a three-terminal VSC-MTDC system connected with two submarine HVDC cables is built and verified in PSCAD. Based on the model, DC cable short circuit faults are studied in Chapter 3, and the results are analyzed and compared with both the three-stage fault response theory and the travelling wave effect. The conclusion indicates that a switchgear should operate before the *critical time* to protect the system from the *overcurrent.* Therefore, efficient and reliable fault detecting/locating principles have to be researched and studied, and fast fault isolation devices need to be designed and tested. Moreover, introducing effective fault current limiters to postpone the damaging moment is yet another possible solution; it will allow the fault dealing procedure more time to take actions. These aspects of the fault detecting/locating, fault isolating and fault current limiting are discussed in Chapter 4-6 respectively.

Based on the simulation results and preliminary conclusions, in Chapter 7 a comprehensive protection scheme is proposed as below:

- Fault Current Limiting Sub-scheme
  - AC Side: an LCL circuit (M_r=0.95, r=1.02) for each VSC station
  - DC Side: a protective inductor of 16mH installed on each end of every DC cable
- Fault Detecting/Locating Sub-scheme:
  - Detecting:
    - Main Algorithm 1: differential protection
      Threshold: VSC_A1: 2.5kA; VSC_C1/C2: 1.5kA.
    - Main Algorithm 2: wavelet-based fault detecting method
      Sampling rate: 10μs; Threshold: 0.5.
    - Backup plan: overcurrent protection, threshold to be determined depending on the cable and CB properties and other issues in practice
    - Auxiliary Components: an optic fiber communication line for each cable;
      current derivative calculating units (optional)
  - Locating:
    - Type D travelling wave based fault location method
    - Wavefront arrival time detected by the off-line data processing from the data recorded during the fault, such as wavelet coefficients and current derivatives
    - Requires high sampling and synchronized communication
- Fault Isolating Sub-scheme:
  - The Hybrid I type DCCB with clearance time within 2ms can be adopted in the case when the diodes for VSC_C1/C2 are sized for 2kA and VSC_A1 for 4kA

- o If all the diodes are oversized to withstand current as high as 13kA, the mechanical DCCBs might also be feasible when the backup overcurrent protection is properly coordinated and that the DC cables are strong enough.

Afterwards, the scheme is tested and evaluated with more simulations. In overall, the proposed scheme is proven to be fast, selective, reliable, sensitive and robust in general. Yet, the chapter also describes the possible optimization and follow-up studies.

Although the proposed scheme is based on the target system, the general principle in protection system design should be similar for other grid topology. Nevertheless, particular issues might arise with the increase of terminal numbers and complexity of the network, or a change in VSC and cable configuration. Yet, a general design philosophy is proposed and briefly described below:

1, Run the simulation and obtain the fault response without any protection;

2, Based on the fault analysis and design goals, temporarily determine the parameters for LCL circuits;

3, Run a Multirun simulation with LCL-VSC to temporarily determine the size of protective inductors;

4, Run simulation with the designed FCLs, set the relay threshold based on the simulation results;

5, Based on the critical time limit and the detecting time, coordinate the diode size and DCCB type;

6, Optimize the design, compare different schemes and determine the final scheme.

8.2 Thesis Contribution

The major contribution of this thesis is combining the three aspects of fault detection/location, fault isolation and fault current limiters into a comprehensive protection scheme, which has not been much explored in existing literature. While the first and third aspects are studied with numerical simulation in depth, the second aspect of DCCBs are discussed briefly in this report. Yet, the related work determines the requirement in clearance time for the DCCBs, as well as describing how this can be affected by the diode sizing. These conclusions can help in DCCB selection and system configuration in the future.

As for the FCL design, it combines the LCL circuit on the AC side and the protective inductors on the DC side, so that the fault current can effectively be limited throughout all the stages in the fault response. This has been proven in both theory and simulation results. Another innovation in the thesis work is that the effects of the FCLs installation on system dynamics, relay settings, etc. are also discussed in the report.

8.3 Limitation and Future Work

The thesis work is meant to take a comprehensive view on the topic of DC cable short circuit fault protection in VSC-MTDC; yet due to limited time and effort, the scope is narrowed down to:

- System Topology: three-terminal MTDC system connected with two HVDC cables in radical topology
- VSC Configuration: two-level VSC technology
- Cable Configuration: symmetrical monopole configuration
- Fault Configuration: bolt, permanent, pole-to-pole DC faults in different locations along Cable A1C2
- Study Method: numerical simulation in PSCAD/EMTDC
- Other simplifications:
  - o Each AC grid is modelled as an ideal voltage source.
  - o DCCB is modeled as an ideal switch opening with a time delay.
  - o The impact of installations of sensors, relays, DCCBs, etc. are ignored.
  - o Noise, measurement errors and communication errors are ignored.

- o Subsequent issues such as recovery scheme of the healthy part, protection scheme of the subsequent faults caused by DCCB interruptions or other component malfunction are not considered.

Therefore, the suggestions for the future work include:

- Working on a more complicated MTDC system, such as adding the HVAC connection between VSC_C1 and VSC_C2 as indicated in the subsystem DSC1 in the *CIGRE B4 DC Grid Test* benchmark in literature [6].
- Adapting the system to multi-level or MMC configuration for better system performance in harmonics. Moreover, it is also claimed that the configuration of full-bridge MMC [75], clamp double half-bridge MMC [76], and alternative arm MMC [77] can contribute to an intrinsically fault-tolerant VSC station. This too is of great interest to future study.
- Studying other cable configurations such as bipolar configuration of cable A1C2 as indicated in [6].
- Studying on more fault types such as pole-to-ground faults, AC faults, etc. Coordinate the relays so that the protection is selective, sensitive and robust in a nire general context.
- Improving the models in AC grid, DCCBs, relays, sensors, communication lines, environmental noise etc. in the simulation.
- Conducting tests in laboratory mock-ups or even in testing projects besides the software simulation.
- Studying the subsequent issues after the fault, such as the CB interruption procedure, subsequent faults, recovery scheme, etc.
- Studying the role of DC/DC converters in fault protection
- In addition, optimizing the proposed scheme is also an interesting topic; for example, improving in detecting/locating methods, fault isolation tools, fault current limiting devices (component-wise or topol11y-wise), as well as in the philosophy in sizing the freewheeling diodes and DC capacitors.

APPENDIX

A. Park and Inverse-Park Transform Matrix in PSCAD (as in PSCAD Help file)

A.1 abc to dq0:

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

A.2 dq0 to abc:

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \cdot \begin{bmatrix} d \\ q \\ 0 \end{bmatrix}$$

B. Wind Turbine Generator/Wind Farm Power Curve

According to the theory of aerodynamics, the power output of a wind turbine generator is proportional to the cube of wind speed. More specifically, the equation is defined as below:

$$P = \frac{1}{2} \rho v^3 \frac{\pi d^2}{4} C_p \tag{Eq. B.1}$$

where P is the power output, ρ the air density, v the wind speed, d the diameter of the blade, and finally C_p the power coefficient.

C_p has a theoretical limit of 16/27 (around 60%), which is also called 'the Betz limit'. Furthermore, when given the blade number, C_p is a function of angle of attack (AOA) α and tip speed ratio (TSR) λ. The former is defined as the angle between the incoming wind direction and the chord line of the blades (Figure B.1) while the latter as the ratio between the wind turbine rotational speed over the wind speed.
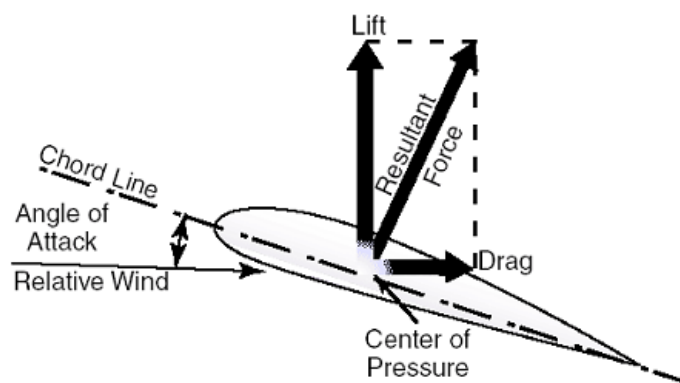
Figure B.1 Angle of Attack
(source: https://www.advanced-flight-systems.com/Products/AOA/132.png)

Given the turbine shape and a certain wind speed, it can be further seen that AOA is determined by the pitch angle θ_p (Figure B.2), while the TSR determined by the rotational speed ω.
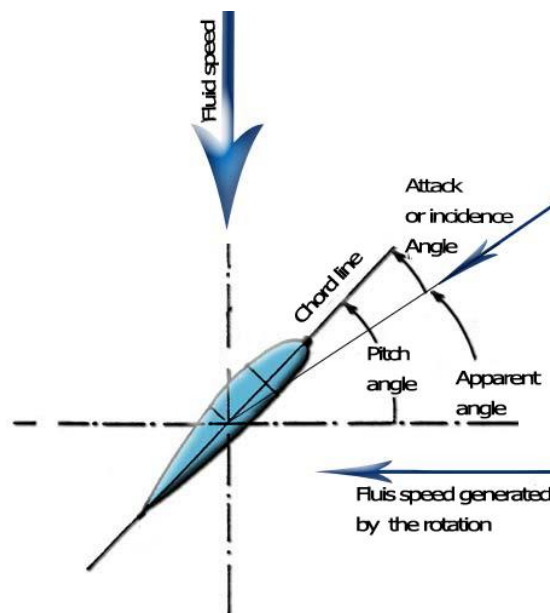
Figure B.2 Pitch Angle
(source: http://www.heliciel.com/en/images/geometrie-incidence.jpg)

The power curve of a wind turbine generator depicts the energy a wind turbine can utilize under the certain wind speed, shown in Figure B.3. As can be seen from the figure, the power curve is divided into several sections according to the different control scheme adopted by each. A general control scheme of a pitch-regulated wind turbine is shown as in Table B.1.
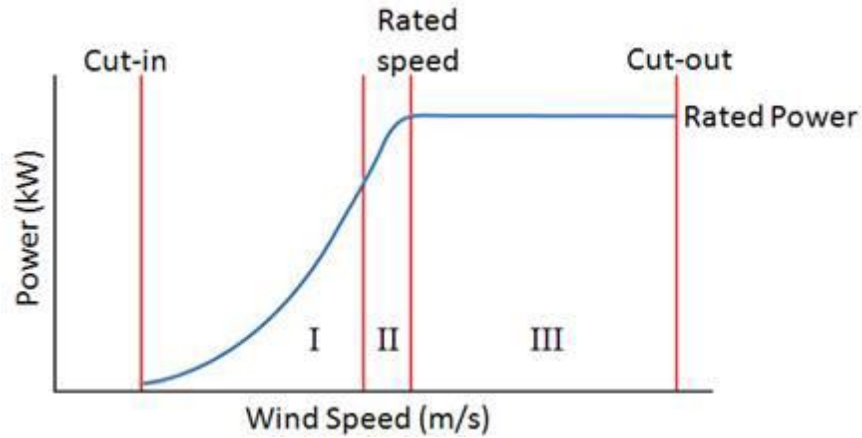

Figure B.3 Wind Turbine Generator Power Curve

(source: http://www.ni.com/white-paper/8189/en/)

Table B.1 Pitch Regulated Wind Turbine Generator Control Scheme

Power Curve Section	Wind Speed	Power	Rotational Speed	Pitch Angle	Note
I	$V_{wind} < V_{cut-in}$	0	0	N/A	Available energy below minimum threshold.
II	$V_{cut-in} < V_{wind} < V_{star}$	$\frac{1}{2}\,\rho\,v^3\,\frac{\pi d^2}{4}\,C_p$	Optimal TSR	Optimal pitch angle	Extract the most power with optimal setting of rotational speed and pitch angle
III	$V_{star} < V_{wind} < V_{rated}$	$\frac{1}{2}\,\rho\,v^3\,\frac{\pi d^2}{4}\,C_p$	ω_{max}	Optimal pitch angle	Rotational speed limited by noise restriction.
IV	$V_{rated} < V_{wind} < V_{cut-out}$	P_{rated}	ω_{max}	Pitch regulated	Limit output by pitch regulation. Other regulation scheme can also work.
V	$V_{wind} < V_{cut-out}$	0	0	N/A	Use break to protect the rotor from being damaged.

Generally speaking, the output of the wind farm is the sum of the individual output of each wind turbine generator in the wind farm. More often than not, a smoother variation in production change is expected.

C. Snapshots of ABB Datasheet

C.1 From 'HVDC Light Technology' [13]

Moderate climate, submarine cables with copper conductor

Area	Ampacity		±80 kV bipole				±150 kV bipole				±320 kV bipole			
Con-ductor	Close laying	Spaced laying	Close laying	Spaced laying	Weight per cable	Diam. over cable	Close laying	Spaced laying	Weight per cable	Diam. over cable	Close laying	Spaced laying	Weight per cable	Diam. over cable
mm²	Amps	Amps	MW	MW	kg/m	mm	MW	MW	kg/m	mm	MW	MW	kg/m	mm
95	343	404	55	65	4,7	42	103	121	8,5	60	220	259	15	90
120	392	463	63	74	5,5	44	118	139	9,4	61	251	296	16	91
150	441	523	71	84	6,7	47	132	157	10	63	282	335	17	93
185	500	596	80	95	7,4	49	150	179	11	64	320	381	18	95
240	583	697	93	112	8,4	52	175	209	12	67	373	446	20	99
300	662	797	106	128	9,4	56	199	239	13	69	424	510	22	102
400	765	922	122	148	11	61	230	277	16	75	490	590	24	105
500	883	1072	141	172	13	66	265	322	18	78	565	686	26	108
630	1023	1246	164	199	15	71	307	374	21	83	655	797	30	114
800	1175	1438	188	230	17	76	353	431	24	88	752	920	33	118
1000	1335	1644	214	263	21	81	401	493	26	96	854	1052	37	122
1200	1458	1791	233	287	24	85	437	537	29	100	933	1146	40	126
1400	1594	1962	255	314	27	89	478	589	32	103	1020	1256	43	130
1600	1720	2123	275	340	30	92	516	637	35	107	1101	1359	47	133
1800	1830	2265	293	362	32	96	549	680	38	110	1171	1450	50	137
2000	1953	2407	312	385	35	99	586	722	41	113	1250	1540	53	140
2200	2062	2540	330	406	40	103	619	762	45	118	1320	1626	58	145
2400	2170	2678	347	428	42	106	651	803	48	121	1389	1714	61	148

Sea soil: Temperature 15 degrees C, burial 1.0 meter, thermal resistivity 1.0 K × W /m
Cable: Copper conductor, HVDC polymer insulation, steel wire armor

* The original datasheet is about bipole cables. Here it is assumed that the current capacity of a monopole cable is approximately the same as a bipole one. Nevertheless, in real case, exact and detailed data can be further acquired from the manufacturer.

C.2 From 'Submarine Cable Systems' [14]

Single-core cables with lead sheath

Cross-section of con-ductor	Diameter of con-ductor	Insulation thickness	Diameter over insulation	Lead sheath thickness	Outer diameter of cable	Cable weight (Aluminium)	Cable weight (Copper)	Capaci-tance	Charging current per phase at 50 Hz	Inductance ●●●
mm²	mm	mm	mm	mm	mm	kg/m	kg/m	µF/km	A/km	mH/km

Table 38

Single-core cables, nominal voltage 275 kV (Um = 300 kV)										
500	26.2	26.0	81.6	3.0	115.2	20.5	31.1	0.14	6.8	1.42
630	29.8	24.0	81.2	3.0	114.8	20.6	31.8	0.16	7.7	1.40
800	33.7	24.0	85.1	3.1	119.5	22.5	35.2	0.17	8.3	1.37
1000	37.9	24.0	89.3	3.1	123.9	24.1	38.4	0.18	9.0	1.35
1200	41.2	24.0	92.6	3.1	127.4	25.5	41.6	0.19	9.5	1.33
1400	44.4	24.0	95.8	3.1	130.6	26.8	44.4	0.20	10.0	1.32
1600	47.4	24.0	98.8	3.1	133.8	28.1	47.2	0.21	10.4	1.31

* The original datasheet is about HVAC cables. Here it is assumed that the insulation level of an HVDC cable is approximately the same as an HVAC one. Nevertheless, in real case, exact and detailed data can be further acquired from the manufacturer.

D. Simulation on Model Validation

D.1 Simulation Scenario

Table D.2 Reference Value Setting for VSC Stations

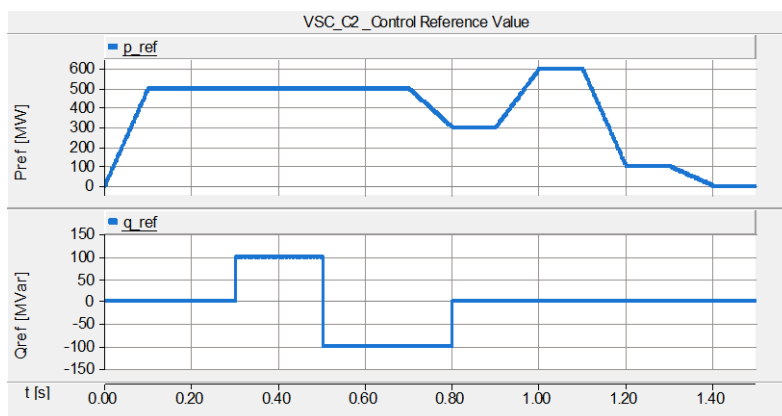| AC-DC Converter Station	Control Strategy	
Cm-A1	VDC = 400 kV = 1 p.u.	Q = 0
Cm-C1	P = 500 MW = 0.5 p.u.	Q = 0
Cm-C2	See Figure D.1	

Figure D.1 Reference Value Setting for VSC_C2 in Load Change Study
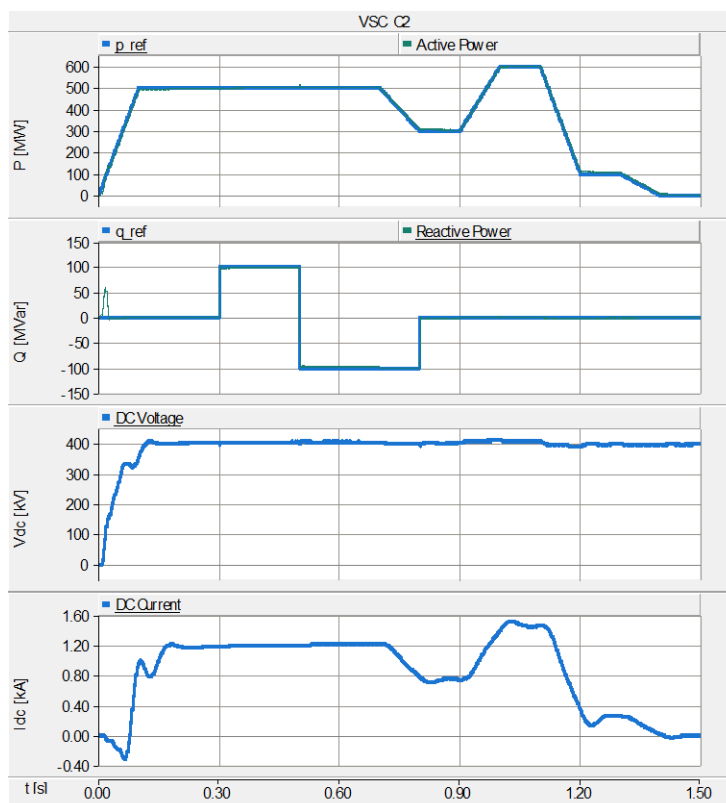
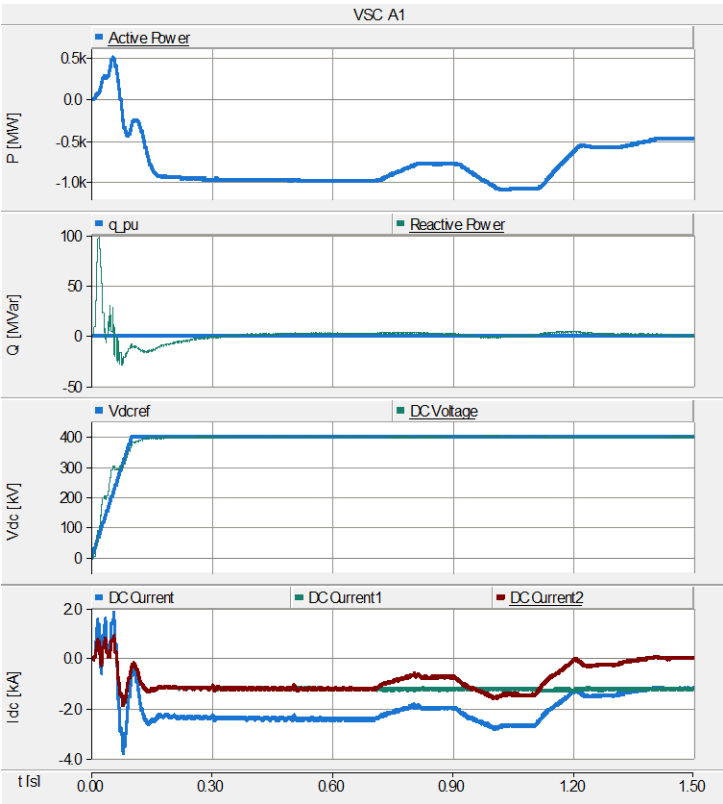### D.2 Simulation Results

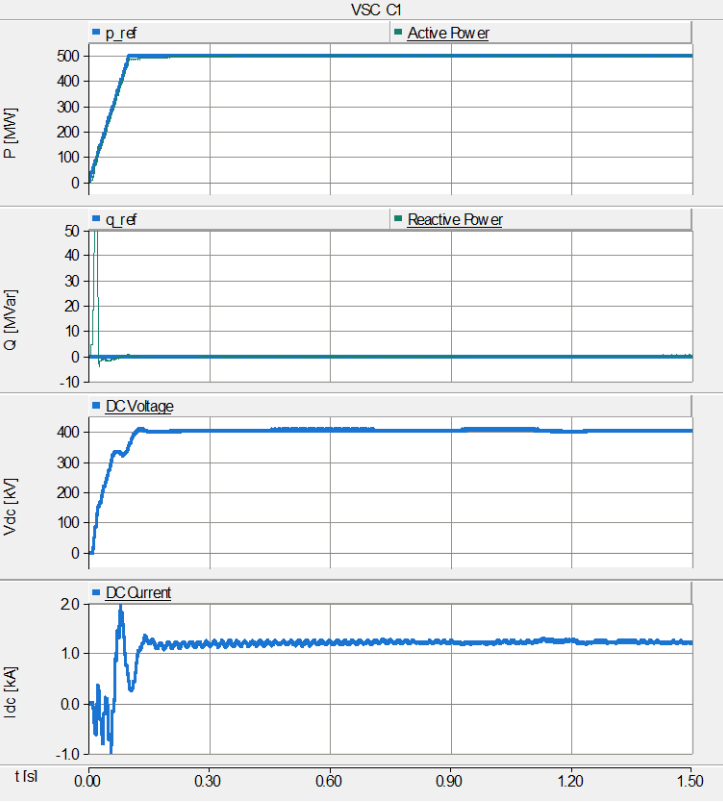
Figure D.2 Simulation Results VSC_C2

87

Figure D.3 Simulation Results VSC_A1

Figure D.4 Simulation Results VSC_C1

E. Theory on Fault response of DC Cable Short Circuit Fault (from [2])

E.1 Critical Time

$$t_c = (\pi - \gamma)/\omega \qquad \text{Eq. (E.1)}$$

E.2 Fault Current

$$I_{cable} = \begin{cases} -\dfrac{I_0\omega_0}{\omega}e^{-\delta t}\sin\omega t & \text{Stage 1} \\ I_0'e^{-\lambda t} & \text{Stage 2} \\ A\sin(\omega_s + \alpha - \varphi - \theta) + Be^{-t/\tau} + \dfrac{[C_1 e^{-\delta t}\sin(\omega t+\beta)]}{\omega} + \dfrac{C_2 e^{-\delta t}\sin\omega t}{\omega} & \text{Stage 3} \end{cases} \qquad \text{Eq. (E.2)}$$

where $\omega_0 = 1/LC$

$$\delta = \frac{R}{2L}$$

$$\omega^2 = \omega_0^2 - \delta^2$$

$$\beta = \text{arttan}\left(\frac{\omega}{\delta}\right)$$

$$\gamma = \text{arttan}(\frac{V_0\omega_0 C\sin\beta}{V_0\omega_0 C\cos\beta - I_0})$$

$$\lambda = \frac{R}{L}$$

$$I_0' = I_{cable}(t_c)$$

$$A = I_g\sqrt{[(1 - \omega_s^2 LC)^2 + (RC\omega_s)^2]}$$

$$\varphi = \text{arttan}\left(\frac{\omega_s(L_{choke}+L)}{R}\right)$$

$$\theta = \text{arttan}\left(\frac{RC\omega_s}{1 - \omega_s^2 LC}\right)$$

$$\tau = \frac{(L_{choke} + L)}{R}$$

$$B = I_g\frac{\tau^2}{\tau^2 - RC\tau + LC}$$

$$C_1 = -A\sin(\alpha - \varphi - \theta) - B$$

$$C_2 = \frac{B}{\tau} - \omega_s A\cos\gamma$$

89

F. Fault Analysis Simulation Results (Left: without FCLs; Right: with FCLs)

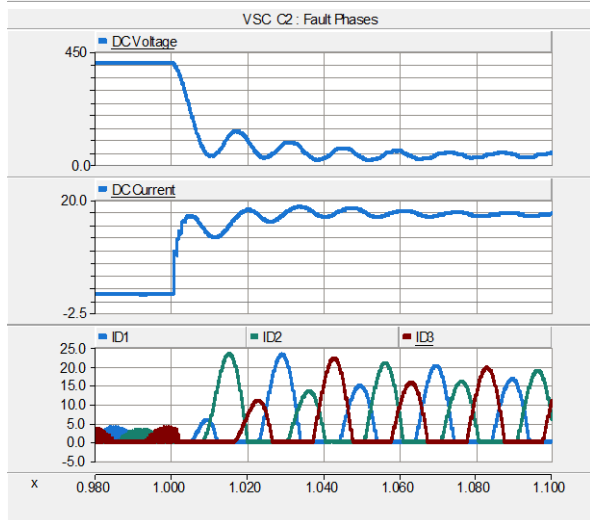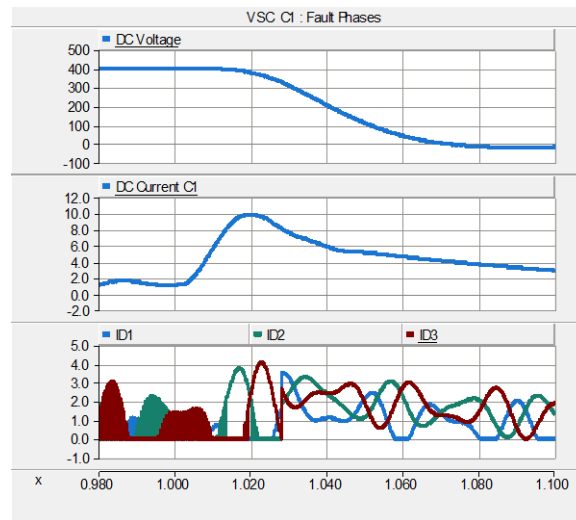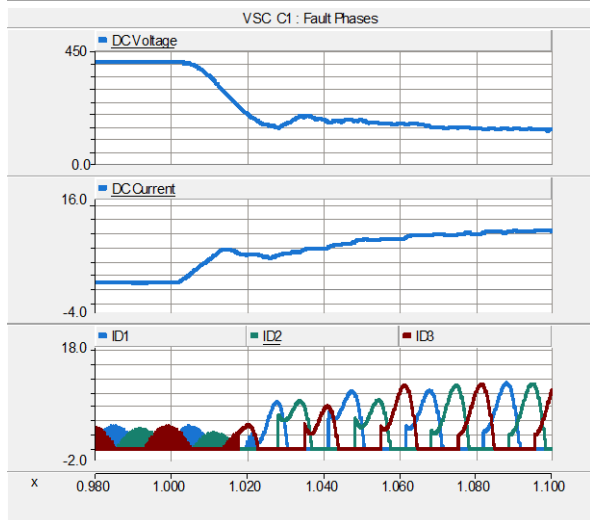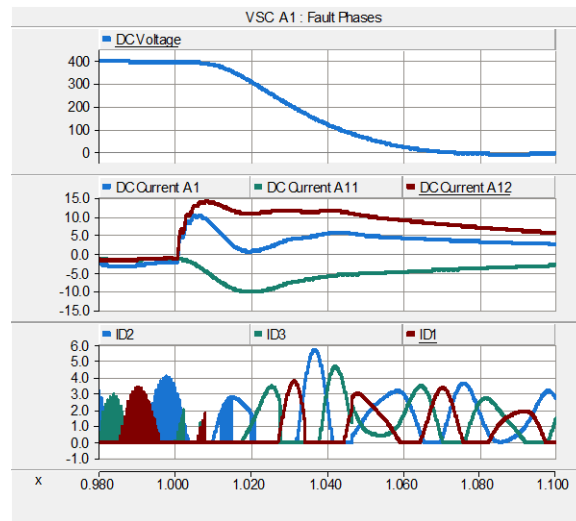D= 1km, without FCLs
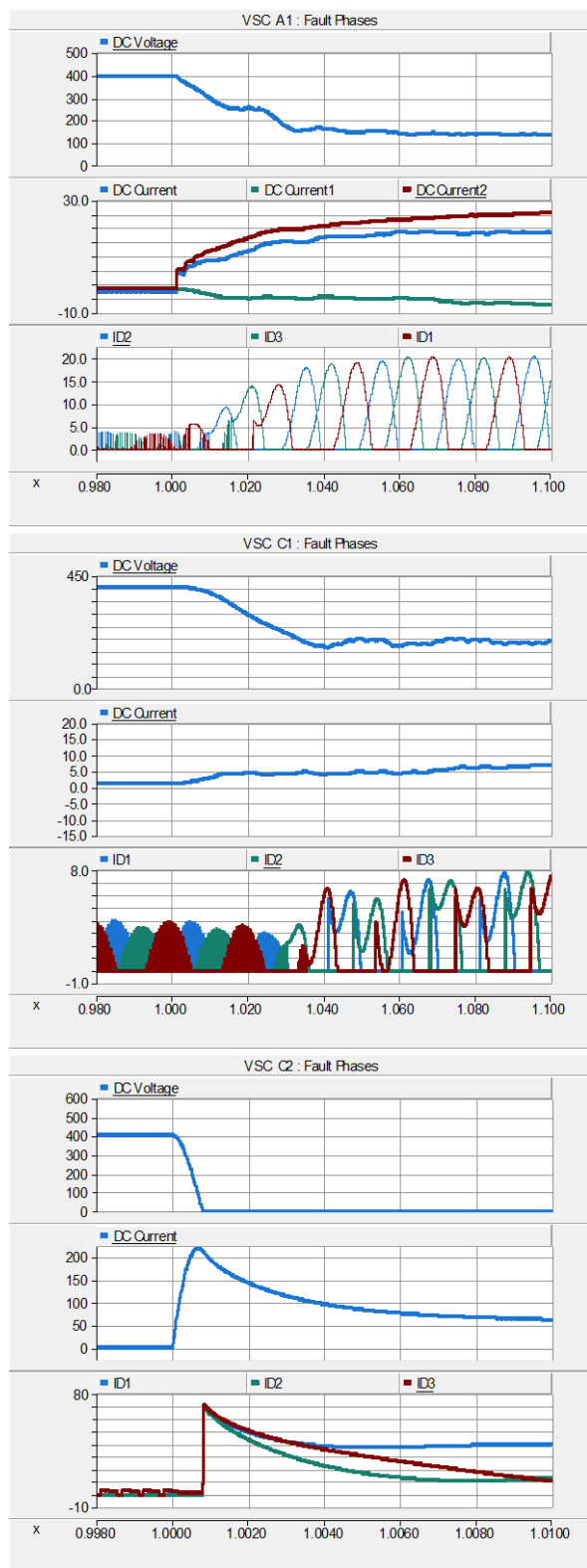
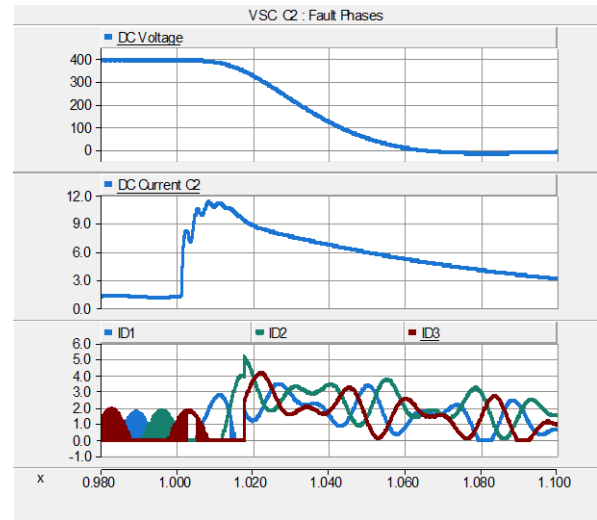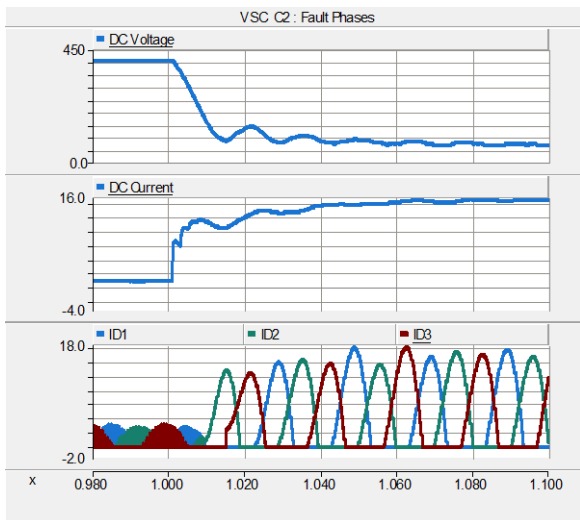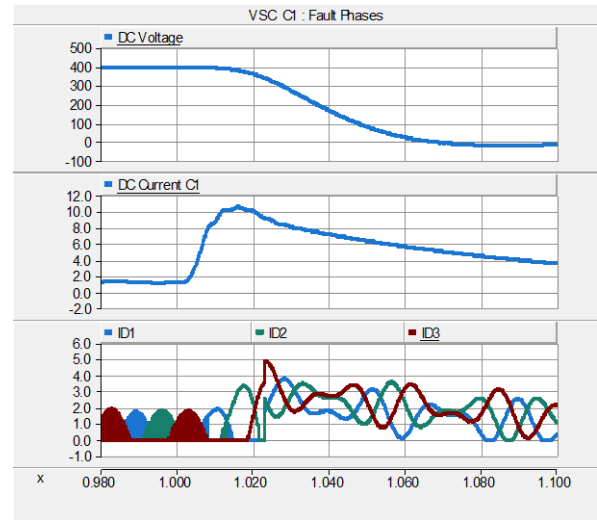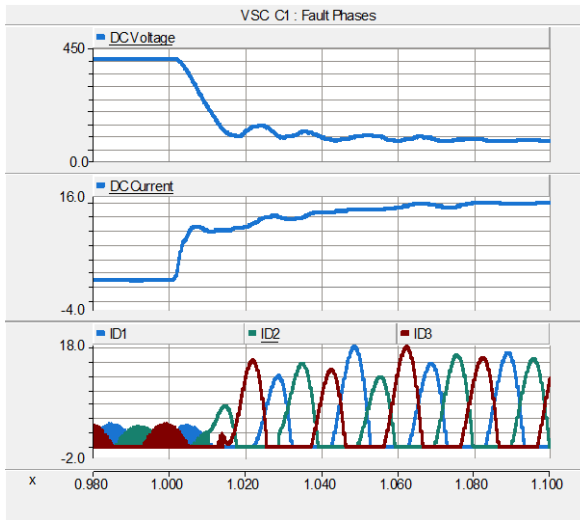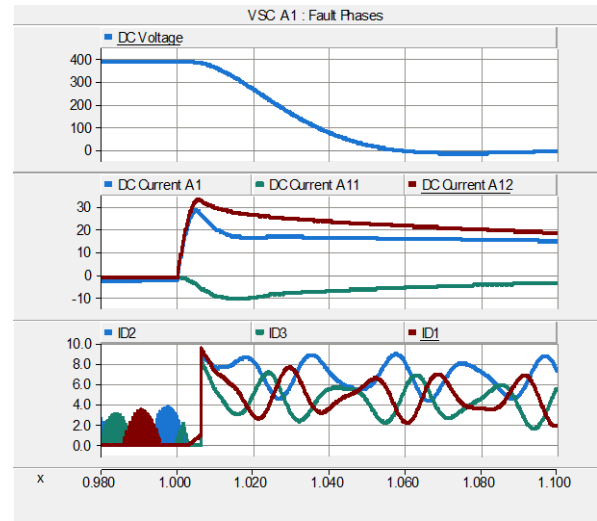D= 1km, with FCLs
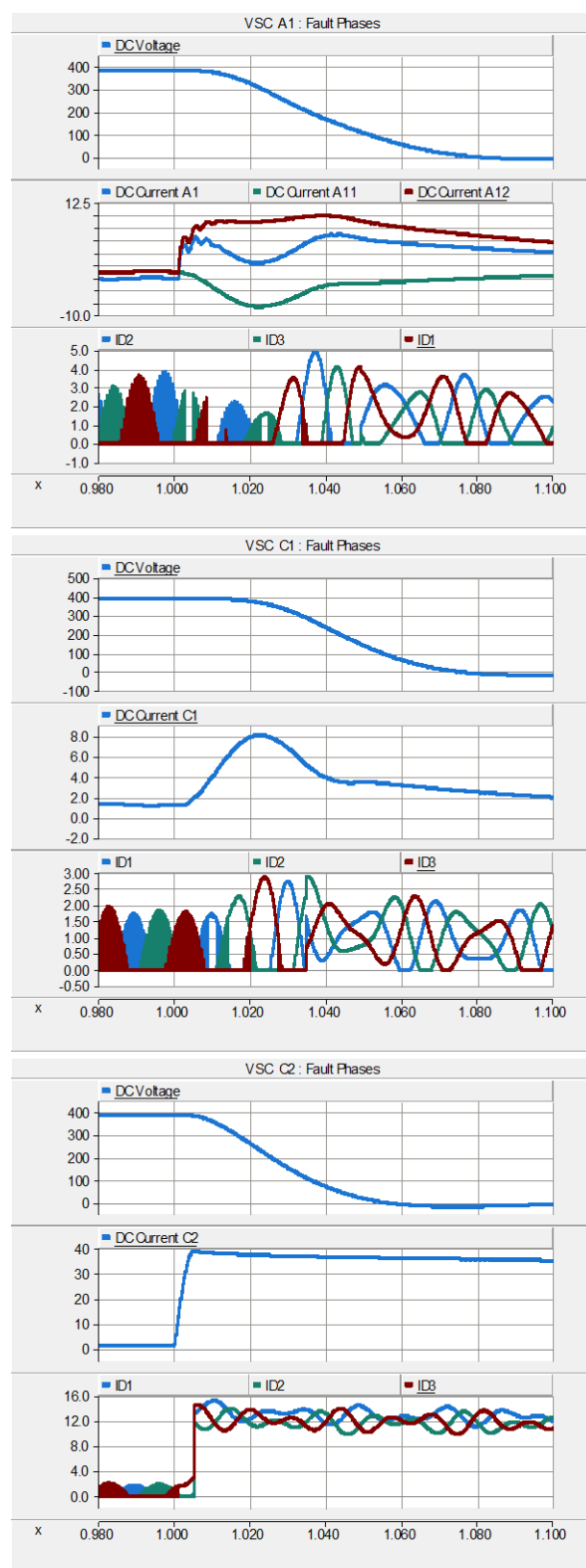
D= 10km, without FCLs
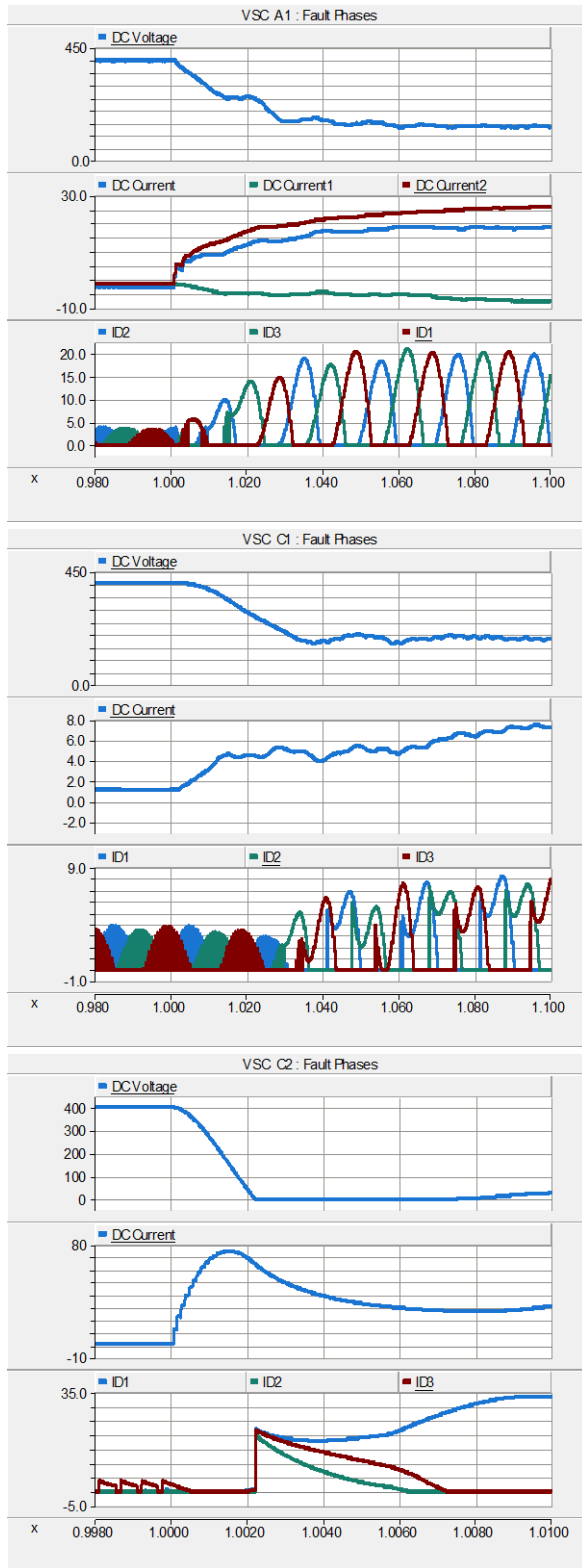
D= 10km, with FCLs
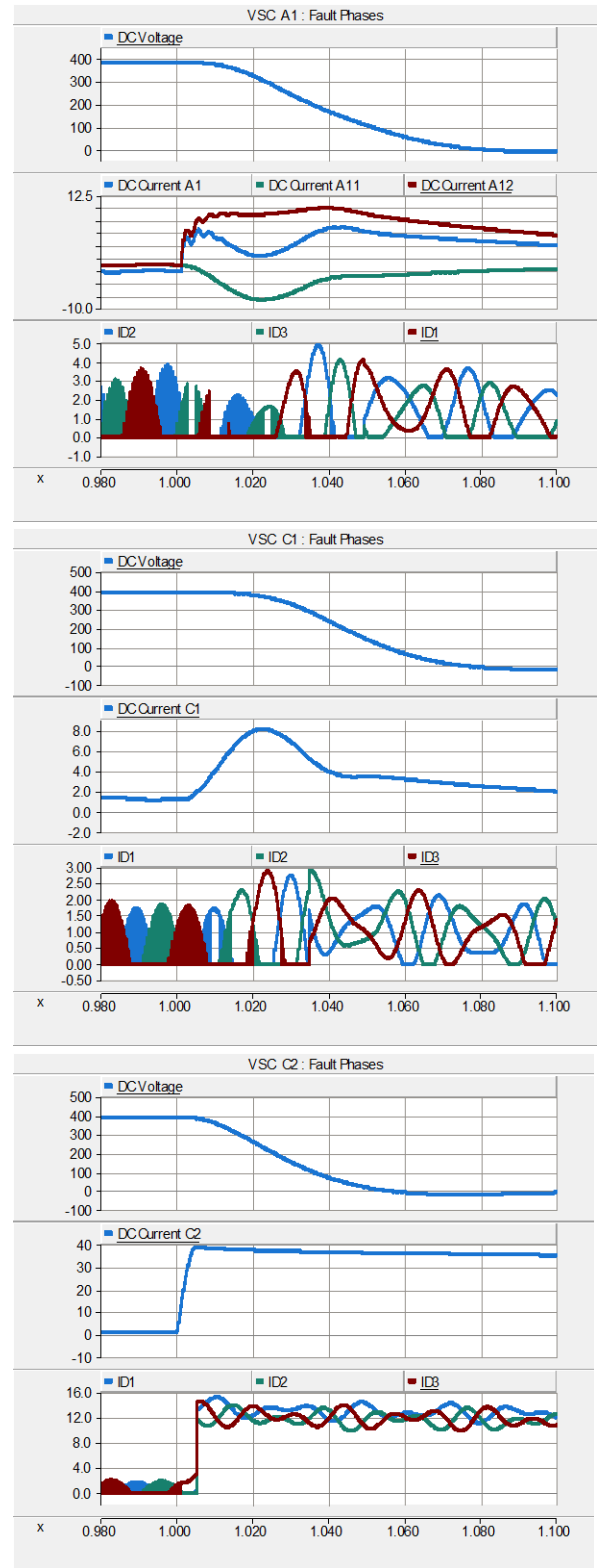
D=100km, without FCLs

D=100km, with FCLs

92
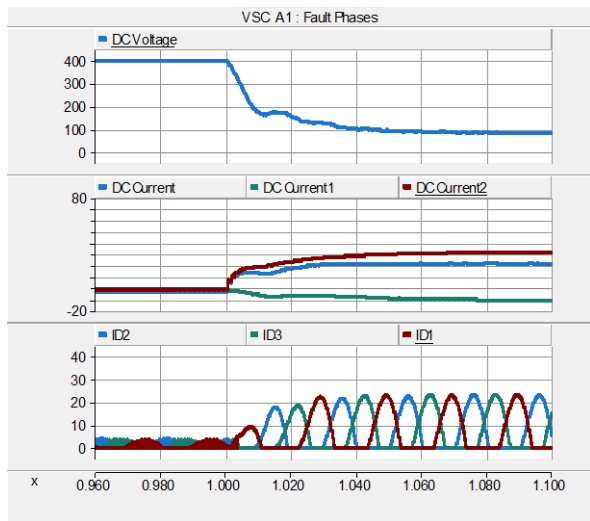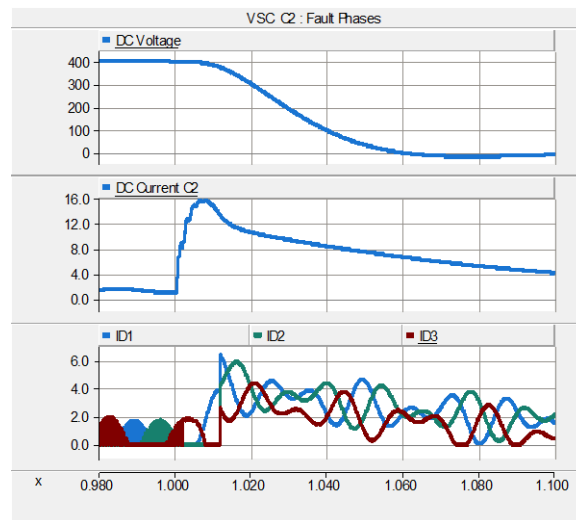
D=190km, without FCLs
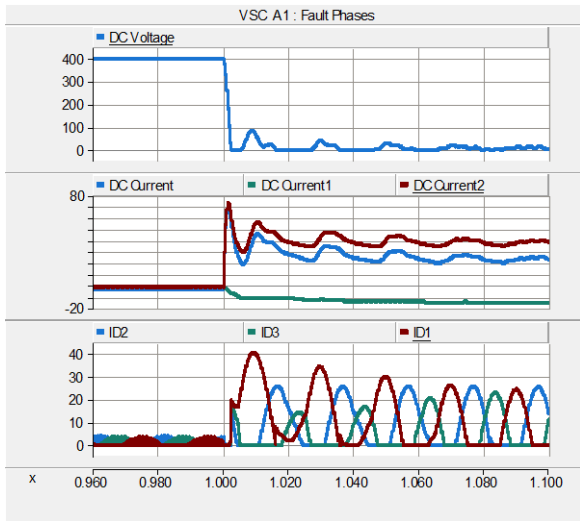
D=190km, with FCLs

D=199km, without FCLs
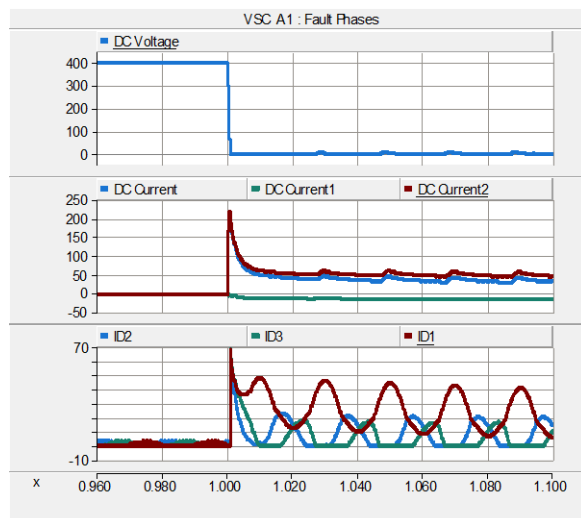
D=199km, with FCLs
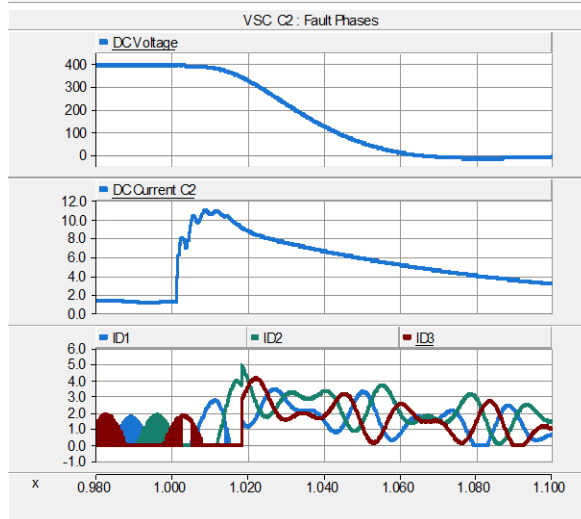
G. Wavelet Transformation Theory

There are three types of wavelet transforms in general:

- Continuous Wavelet Transform (CWT)
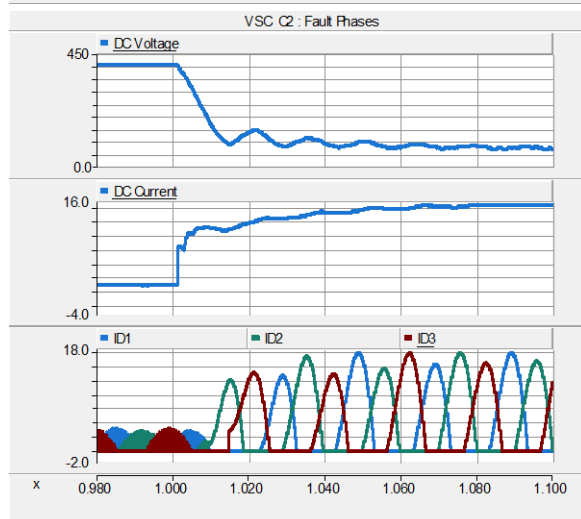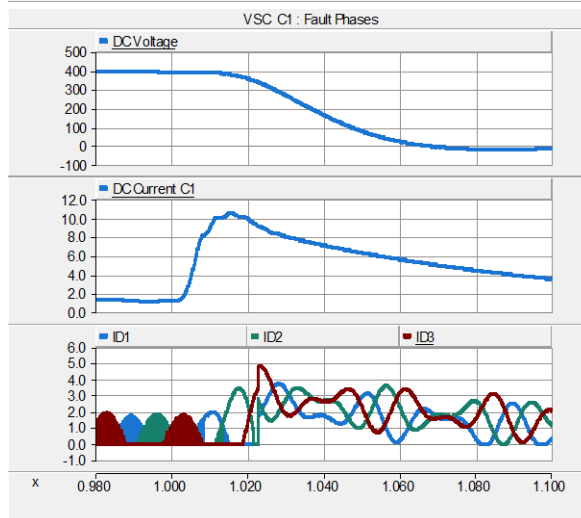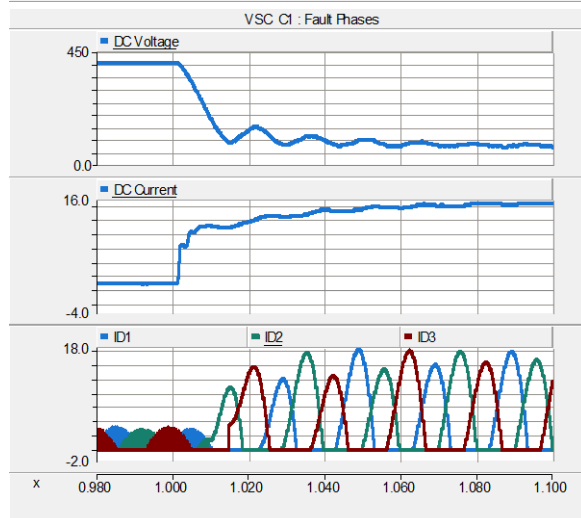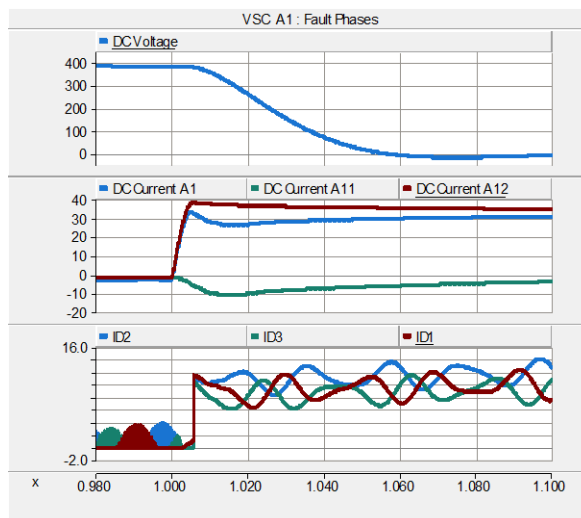
  CWT is defined as in Equation (G.1):

  $$W(s, u) = \frac{1}{\sqrt{s}} \int_{-\infty}^{\infty} x(t) \varphi^* \left(\frac{t-u}{s}\right) dt \qquad \text{Eq. (G.1)}$$

  where $\varphi^* \left(\frac{t-u}{s}\right)$ is the conjugate of the mother wavelet, s is the dilation parameter which determines the window of the wavelet transform, and u as the translation parameter which determines the time shift from the center point of each window [25].

- Discrete Wavelet Transform (DWT)

  DWT is defined as in Equation (G.2):

  $$DW(m, k) = \frac{1}{\sqrt{p_0^m}} \sum_n x(n) \varphi^* \left(\frac{k - np_0^m}{p_0^m}\right) \qquad \text{Eq. (G.2)}$$

  where $\varphi^* \left(\frac{k - np_0^m}{p_0^m}\right)$ the conjugate of the mother wavelet, integer m is known as the scale parameter which determines the window of the wavelet transform, and integer k as the shift parameter which determines the time shift from the center point of each window [28].

  This is the discrete form of Equation (G.1). In this way, the wavelet transformation is digitalized to become practical for fault detecting. In practice, the DWT of a signal x is calculated by passing it through a series of low-pass filters (g) and high-pass filters (h), the outputs of which give the approximation coefficients and detailed coefficients respectively, as indicated in Equation G.3 - G.4. Of course, the two filters requires coordination so that to shape a 'quadrature mirror filter'.

  $$y_{low}[n] = \sum_{-\infty}^{\infty} x[k] g[2n - k] \qquad \text{Eq. (G.3)}$$
  $$y_{high}[n] = \sum_{-\infty}^{\infty} x[k] h[2n - k] \qquad \text{Eq. (G.4)}$$

  Afterwards, the sampling frequency is reduced to half of the original since half the signals have been removed. As a result, the resolution time will be halved, and each output will expect a doubled frequency resolution [28]. Figure G.1 illustrates how this works.

  Usually, the output from the low pass filter, which contains information of detail coefficients, can be furthermore transformed into a second layer of approximation coefficients and detail coefficients. In fact, DWT includes successive levels of such high- and low-pass filters, as the decomposition is repeated to further increase the frequency resolution [16, 28]. For each level, the frequency of another spectrum is covered, where the latter layers covering the lower frequency [29]. A binary tree called 'filter bank' is presented in Figure G.2. In such circumstances, the p_0 in Equation (G.2) equals 2. In other words, the mother wavelet is scaled and shifted by the power of two [28].
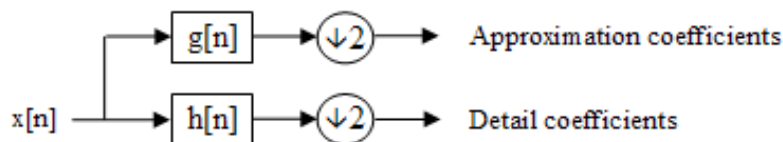
Figure G.1 Block Diagram of Filter Analysis (taken from [28])
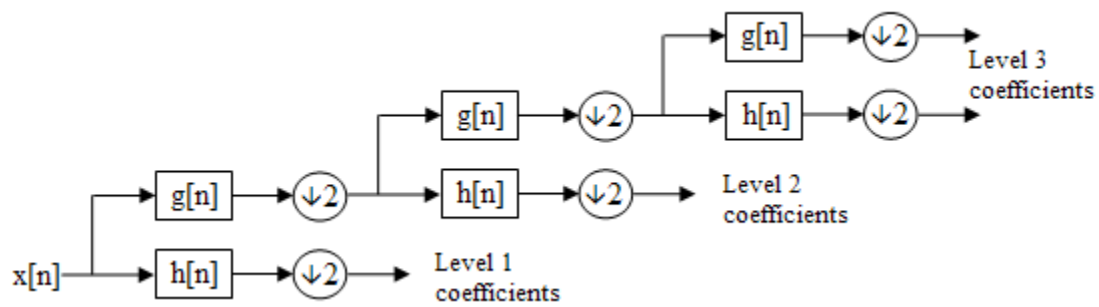
Figure G.2 Block Diagram of Filter Bank (taken from [28])

- Stationary Wavelet Transform (SWT)

  Contrary to DWT, the translation parameter in SWT is a constant so that the transforms obtained from different lines in SWT are compared without shift in time. As a result, the resulting wavelet and coefficients become time invariant [25]. Furthermore, SWT has inherent redundancy; it has wide applications in cases which require de-noising [33].

H. Matlab Code for LCL Sizing

```
clc
clear all

P1r=1000; %[MW]
Vdc=200; %+/-200kV
V1ac=220; %line to line, rms, [kV]
Mr=0.95;
w=2*pi*50;

r=1.02; %select 1<r<2 according to i_D
V1r=V1ac/sqrt(3);
V2r=Mr*Vdc/sqrt(2);
s=V1r/V2r

k1r=sqrt(1-1/r^2)/s;
k2r=sqrt(1-1/r^2)*s;

Mdr=k1r*s*Mr;
Mqr=-sqrt(Mr^2-Mdr^2);
k3r=-3*s*(V2r)^2*Mqr/(P1r*w*Mr);

syms x y z
[x,y,z]=solve('k1r=1-w^2*y*z','k2r=1-w^2*x*z','k3r=x+y-w^2*x*y*z','x,y,z');
L1=subs(x)
L2=subs(y)
C=subs(z)
```

I. Robustness Study - Distinguish Faults from Disturbances of Load Change

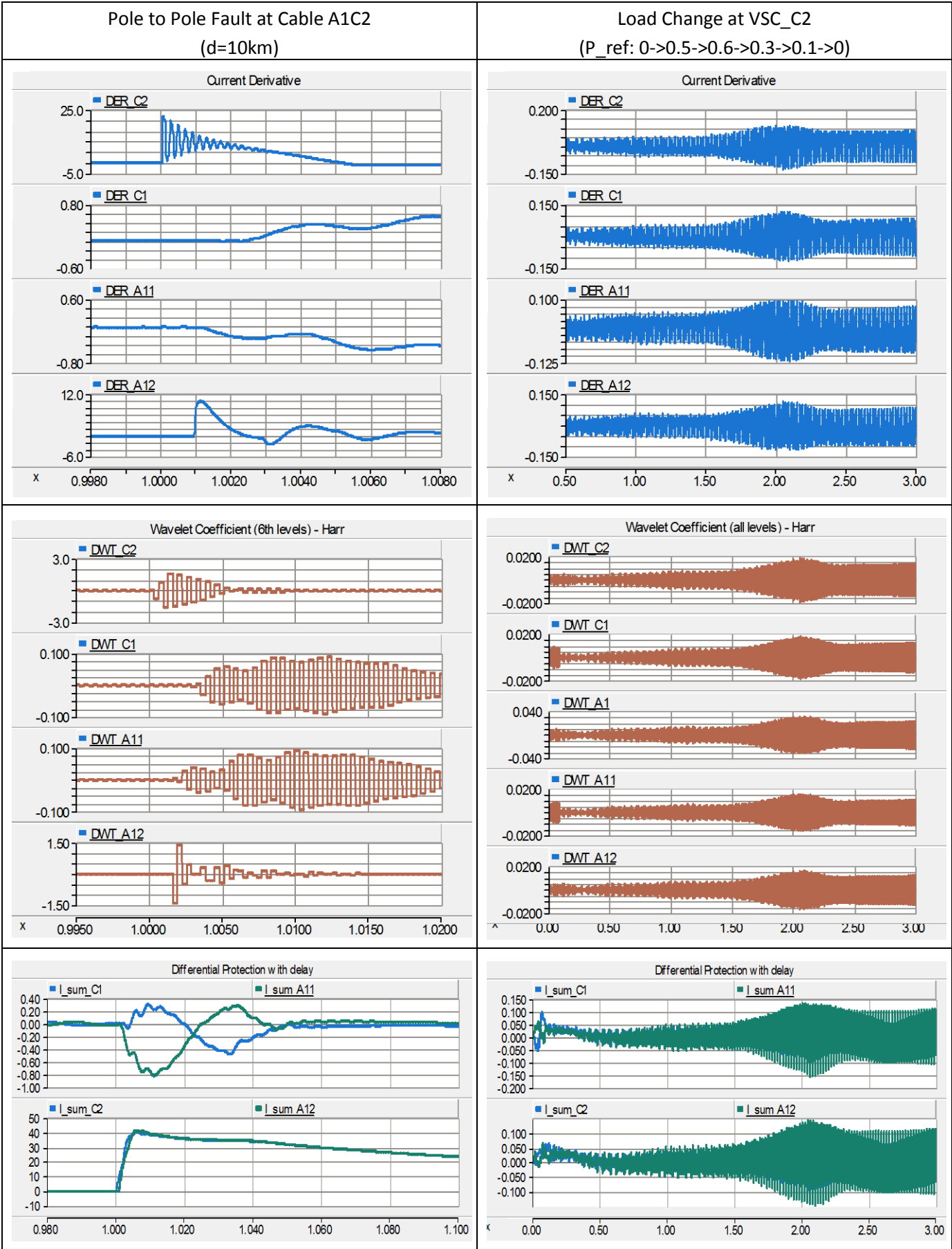| Pole to Pole Fault at Cable A1C2 (d=10km)	Load Change at VSC_C2 (P_ref: 0->0.5->0.6->0.3->0.1->0)

Bibliography

[1] Rudervall R, Charpentier J P, Sharma R. High voltage direct current (HVDC) transmission systems technology review paper[J]. Energy week, 2000, 2000.

[2] Jovcic D, Zhang L, Hajian M. Lcl vsc converter for high-power applications[J]. Power Delivery, IEEE Transactions on, 2013, 28(1): 137-144.

[3] Yang J, Fletcher J E, O'Reilly J. Short-circuit and ground fault analyses and location in VSC-based DC network cables[J]. Industrial Electronics, IEEE Transactions on, 2012, 59(10): 3827-3837.

[4] Kontos E. Control and Protection of VSC-based Multi-terminal DC Networks[D]. Delft University of Technology, 2013.

[5] Jovcic D, Van Hertem D, Linden K, et al. Feasibility of DC transmission networks[C]//Innovative Smart Grid Technologies (ISGT Europe), 2011 2nd IEEE PES International Conference and Exhibition on. IEEE, 2011: 1-8.

[6] Vrana T K, Yang Y, Jovcic D, et al. The CIGRE B4 DC Grid Test System[J]. System, 2013, 500: D1.

[7] Pfeiffer M D, Bucher M K, Franck C M. The effect of grid topology on transient fault currents in multi-terminal vsc-hvdc offshore networks[C]//Proc. International Conference on Power Systems Transients (IPST), Vancouver, Canada. 2013.

[8] Chaudhary S K. Control and Protection of Wind Power Plants with VSC-HVDC Connection[D]. Aalborg University, 2011.

[9] Bajracharya C, Molinas M, Suul J A, et al. Understanding of tuning techniques of converter controllers for VSC-HVDC[C]//Nordic Workshop on Power and Industrial Electronics (NORPIE/2008), June 9-11, 2008, Espoo, Finland. Helsinki University of Technology, 2008.

[10] Rezek A J J, Coelho C A D, Vicente J M E, et al. The modulus optimum (MO) method applied to voltage regulation systems: modeling, tuning and implementation[C]//Proc. International Conference on Power System Transients, IPST. 2001, 1: 24-28.

[11] Aydin O, Akdag A, Stefanutti P, et al, Optimum controller design for a multilevel AC-DC converter system[C]//Applied Power Electronics Conference and Exposition, APEC 2005, 6-10 March 2005, Vol. 3, pp. 1660 -1666.

[12] Daud M Z, Ciufo P, Perera S. Investigation on the suitability of PSCAD/EMTDC models to study energisation transients of 132 kV underground cables[C]//Power Engineering Conference, 2008. AUPEC'08. Australasian Universities. IEEE, 2008: 1-6.

[13] Soderstrom J. It's time to connect-Technical description of HVDC Light technology[R]. Ludvika, Sweden: ABB AB Grid Systems-HVDC, 2005.

[14] ABB X. Submarine Cable Systems: Attachment to XLPE Land Cable Systems-Users Guide[J]. 2011.

[15] Mura F, Meyer C, De Doncker R W. Stability analysis of high-power dc grids[J]. Industry Applications, IEEE Transactions on, 2010, 46(2): 584-592.

[16] Martinsen E. Evaluation of Methods for Detecting and Locating Faults in HVDC Grids[D]. Norwegian University of Science and Technology, 2014.

[17] Bucher M K, Franck C M. Analysis of transient fault currents in multi-terminal hvdc networks during pole-to-ground faults[C]//Proc. International Conference on Power Systems Transients (IPST), Vancouver, Canada. 2013.

[18] Descloux J, Raison B, Curis J B. Protection strategy for undersea MTDC grids[C]//PowerTech (POWERTECH), 2013 IEEE Grenoble. IEEE, 2013: 1-6.

[19] Pathirana, K. P. A. N., et al. "Detecting fault generated surges in DC line of VSC HVDC schemes for travelling wave based fault location." 2012 CIGRÉ Canada conference, Canada. 2012.

[20] Elhaffar, Abdelsalam, and Matti Lehtonen. "Multi-end traveling wave fault location based on current traveling waves." Proceedings of 16 th PSCC (2008).

[21] Hajian, M., L. Zhang, and D. Jovcic. "DC Transmission Grid with Low Speed Protection using Mechanical DC Circuit Breakers."

[22] Twentie Project: Description of a Protection Plan for DC Networks – Preliminary Results towards the real-time experimentation of a small-scale model of a DC network and the 120 kV DC breaker prototype tasks Status report for European Commission Deliverable: D11.2 (http://www.twenties-project.eu/system/files/2012-10-09-Twenties_D11.2-extended_2012-12-07.pdf)

[23] Haj-Maharsi, Mohamed Yassine. "Novel DC Ring Topology and Protection System–a Comprehensive Solution for mega city power grids." (2010).

[24] Naidoo D, Ijumba N M. HVDC line protection for the proposed future HVDC systems[C]//Power System Technology, 2004. PowerCon 2004. 2004 International Conference on IEEE, 2004, 2: 1327-1332.

[25] Haj-Maharsi M Y. Novel DC Ring Topology and Protection System–a Comprehensive Solution for mega city power grids[D]. North Carolina State University. 2010.

[26] Azizi, Sadegh, et al. "A Traveling-Wave-Based Methodology for Wide-Area Fault Location in Multiterminal DC Systems." (2014).

[27] Fowler J E. The redundant discrete wavelet transform and additive noise[J]. Signal Processing Letters, IEEE, 2005, 12(9): 629-632.

[28] Robertson D C, Camps O I, Mayer J S, et al. Wavelets and electromagnetic power system transients[J]. Power Delivery, IEEE Transactions on, 1996, 11(2): 1050-1058.

[29] Gargoom A, Ertugrul N, Soong W. Comparative study of using dfferent mother wavelets on power quality monitoring[C]//Australasian Universities Power Engineering Conference (14th: 2004: Brisbane, Australia). 2004.

[30] Figure: Haar Wavelet: http://en.wikipedia.org/wiki/Haar_wavelet#/media/File:Haar_wavelet.svg

[31] Figure: Fourth Order Daubenchies Wavelet: http://ej.iop.org/images/0964-1726/21/10/105026/Full/sms420176f13_online.jpg

[32] Gaouda, A. M., et al. "Application of multiresolution signal decomposition for monitoring short-duration variations in distribution systems." Power Delivery, IEEE Transactions on 15.2 (2000): 478-485.

[33] Wikipedia:Discrete Wavelet Transform: http://en.wikipedia.org/wiki/Discrete_wavelet_transform

[34] Magnago F H, Abur A. Fault location using wavelets[J]. Power Delivery, IEEE Transactions on, 1998, 13(4): 1475-1480.

[35] Krzysztof G, Kowalik R, Rasolomampionona D. Regular paper TRAVELING WAVE FAULT LOCATION IN POWER TRANSMISSION SYSTEMS: AN OVERVIEW[J]. Electrical Systems, 2011, 7(3): 287-296.

[36] Nanayakkara, OMK Kasun, Athula D. Rajapakse, and Randy Wachal. "Traveling-wave-based line fault location in star-connected multiterminal HVDC systems." Power Delivery, IEEE Transactions on 27.4 (2012): 2286-2294.

[37] Galijasevic, Zijad, and Ali Abur. "Fault area estimation via intelligent processing of fault-induced transients." Power Systems, IEEE Transactions on 18.4 (2003): 1241-1247.

[38] Yang J, Fletcher J E, O'Reilly J. Multiterminal DC wind farm collection grid internal fault analysis and protection design[J]. Power Delivery, IEEE Transactions on, 2010, 25(4): 2308-2318.

[39] Guobing S, XinLei C, ShuPing G, et al. Natural frequency based protection and fault location for VSC-HVDC transmission lines [C]//Advanced Power System Automation and Protection (APAP), 2011, International Conference on. IEEE, 2011, 1: 177-182.

[40] Suonan J, Gao S, Song G, et al. A novel fault-location method for HVDC transmission lines[J]. Power Delivery, IEEE Transactions on, 2010, 25(2): 1203-1209.

[41] Ramesh M, Laxmi A J. Fault identification in HVDC using artificial intelligence—Recent trends and perspective[C]//Power, Signals, Controls and Computation (EPSCICON), 2012 International Conference on. IEEE, 2012: 1-6.

[42] Xiaoyun S, Xiangqian T, Jun Y. Fault diagnosis for VSC-HVDC using wavelet transform[C]//Power and Energy Engineering Conference (APPEEC), 2012 Asia-Pacific. IEEE, 2012: 1-4.

[43] ZhiQing Y, Ximei L. Application of intelligent fault diagnosis technology in HVDC system[C]//Advanced Power System Automation and Protection (APAP), 2011 International Conference on. IEEE, 2011, 3: 2114-2122.

[44] Liu X M, Wei W Y, Wei K T, et al. Fault diagnosis of High Voltage Direct Current system based on H∞ filter[C]//Robotics and Biomimetics, 2007. ROBIO 2007. IEEE International Conference on. IEEE, 2007: 162-166.

[45] Santhosh S. ANFIS based HVDC control and fault identification of HVDC converter[C]//Emerging Trends in Electrical Engineering and Energy Management (ICETEEEM), 2012 International Conference on. IEEE, 2012: 186-190.

[46] Nakanishi K. Switching phenomena in high-voltage circuit breakers[J]. 1991.

[47] Tang L, Ooi B T. Locating and isolating DC faults in multi-terminal DC systems[J]. Power Delivery, IEEE Transactions on, 2007, 22(3): 1877-1884.

[48] Candelaria J, Park J D. VSC-HVDC system protection: A review of current methods[C]//Power Systems Conference and Exposition (PSCE), 2011 IEEE/PES. IEEE, 2011: 1-7.

[49] Candelaria J, Park J D. VSC-HVDC system protection: A review of current methods[C]//Power Systems Conference and Exposition (PSCE), 2011 IEEE/PES. IEEE, 2011: 1-7.

[50] Van Hertem D, Ghandhari M, Curis J B, et al. Protection requirements for a multi-terminal meshed DC grid[C]//Cigrè International Symposium THE ELECTRIC POWER SYSTEM OF THE FUTURE Integrating supergrids and microgrids location. 2011.

[51] Vithayathil J J, Courts A L, Peterson W G, et al. HVDC circuit breaker development and field tests[J]. Power Apparatus and Systems, IEEE Transactions on, 1985 (10): 2692-2705.

[52] Bucher M K, Walter M M, Pfeiffer M, et al. Options for ground fault clearance in HVDC offshore networks[C]//Energy Conversion Congress and Exposition (ECCE), 2012 IEEE. IEEE, 2012: 2880-2887.

[53] Franck C M. HVDC circuit breakers: A review identifying future research needs[J]. Power Delivery, IEEE Transactions on, 2011, 26(2): 998-1007.

[54] Pauli B, Mauthe G, Ruoss E, et al. Development of a high current HVDC circuit breaker with fast fault clearing capability[J]. Power Delivery, IEEE Transactions on, 1988, 3(4): 2072-2080.

[55] Andersson D, Henriksson A. Passive and active DC breakers in the three Gorges-Changzhou HVDC project[C]//Proceedings of the International Conference on Power Systems. Wuhan, China: CIGRE. 2001: 391-395.

[56] Meyer C, Schroder S, De Doncker R W. Solid-state circuit breakers and current limiters for medium-voltage systems having distributed power systems[J]. Power Electronics, IEEE Transactions on, 2004, 19(5): 1333-1340.

[57] Sano K, Takasaki M. A surge-less solid-state dc circuit breaker for voltage source converter based HVDC transmission systems[C]//Energy Conversion Congress and Exposition (ECCE), 2012 IEEE. IEEE, 2012: 4426-4431.

[58] Tennakoon S B, McEwan P M. Short-circuit interruption performance of thyristor circuit breakers[C]//Applied Power Electronics Conference and Exposition, 1994. APEC'94. Conference Proceedings 1994., Ninth Annual. IEEE, 1994: 832-838.

[59] Hofner J, Jacobson B. Proactive Hybrid HVDC Breakers-A key innovation for reliable HVDC grids[J]. Proc. of Cigré Bologna, Paper, 2011, 264.

[60] Holaus, Walter, and K. Frohlich. "Ultra-fast switches-a new element for medium voltage fault current limiting switchgear." Power Engineering Society Winter Meeting, 2002. IEEE. Vol. 1. IEEE, 2002.

[61] Steurer, Michael, et al. "A novel hybrid current-limiting circuit breaker for medium voltage: principle and test results." Power Delivery, IEEE Transactions on 18.2 (2003): 460-467.

[62] Jovcic D, Ooi B T. Theoretical aspects of fault isolation on high-power direct current lines using resonant direct current/direct current converters[J]. IET generation, transmission & distribution, 2011, 5(2): 153-160.

[63] Barker C D, Davidson C C, Trainer D R, et al. Requirements of DC-DC Converters to facilitate large DC Grids[J]. Cigre Session 2012, 2012.

[64] Zhan C, Smith C, Crane A, et al. DC transmission and distribution system for a large offshore wind farm[C]//AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on. IET, 2010: 1-5.

[65] Hajian M, Jovcic D, Wu B. Evaluation of semiconductor based methods for fault isolation on high voltage DC grids[J]. Smart Grid, IEEE Transactions on, 2013, 4(2): 1171-1179.

[66] Barker C D, Davidson C C, Trainer D R, et al. Requirements of DC-DC Converters to facilitate large DC Grids[J]. Cigre Session 2012, 2012.

[67] Zhan C, Smith C, Crane A, et al. DC transmission and distribution system for a large offshore wind farm[C]//AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on. IET, 2010: 1-5.

[68] Deng, Fujin, and Zhe Chen. "Design of protective inductors for HVDC transmission line within DC grid offshore wind farms." Power Delivery, IEEE Transactions on 28.1 (2013): 75-83.

[69] Lin, Weixing, and Dragan Jovcic. "LCL and L-VSC Converters With DC Fault Current-Limiting Property and Minimal Power Losses." (2014): 1-1.

[70] Manohar, Premila, and Wajid Ahmed. "Superconducting fault current limiter to mitigate the effect of DC line fault in VSC-HVDC system." Power, Signals, Controls and Computation (EPSCICON), 2012 International Conference on. IEEE, 2012.

[71] Strumpler, R., et al. "Novel medium voltage fault current limiter based on polymer PTC resistors." Power Delivery, IEEE Transactions on 14.2 (1999): 425-430.

[72] Wu, Huaren, et al. "Analysis of a liquid metal current limiter." Components and Packaging Technologies, IEEE Transactions on 32.3 (2009): 572-577.

[73] Adibi, Mahmod M., ed. Power system restoration: methodologies & implementation strategies. Wiley-IEEE press, 2000.

[74] Asplund, Gunnar, et al. "HVDC grid feasibility study." Electra 267 (2013): 50-59.

[75] Grain, A. D. A. M., et al. "H-bridge modular multilevel converter (M2C) for high-voltage applications." 21st International Conference on Electricity Distribution. Frankfurt, Germany: CIRED. 2011.

[76] Ding, Guanjun, et al. "New technologies of voltage source converter (VSC) for HVDC transmission system based on VSC." Power and Energy Society General Meeting-Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE. IEEE, 2008.

[77] Merlin, M. M. C., et al. "A new hybrid multi-level voltage-source converter with DC fault blocking capability." AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on. IET, 2010.