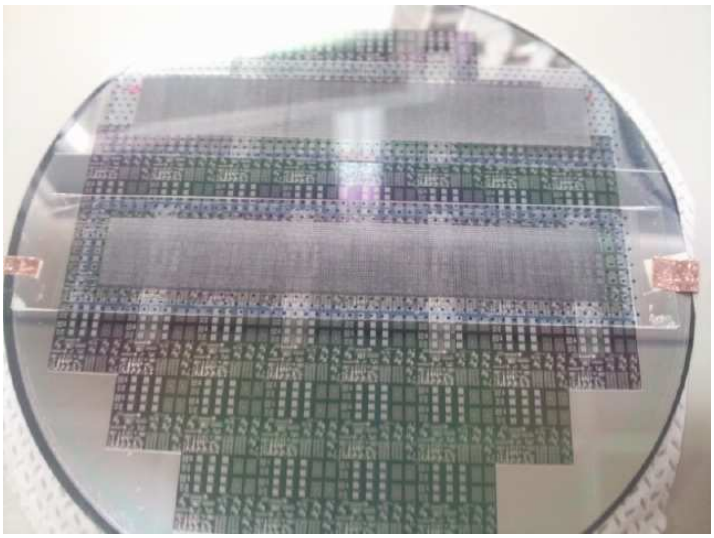
The Optimum Driving Method of Super E-paper

The technical research complementing R:eFlex's businessplan



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Bachelor of Science Thesis

In

Electrical Engineering

Delft 2010

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Photo on the cover by M. Trifunovic

Preface

This thesis is written with regards to the bachelor graduation project on the optimization of the Super E-paper, conducted in the 3rd and final year of Bachelor in Electrical Engineering at Delft University of Technology. During the research the optimum characteristics for the Super E-paper had to be found, by testing the Super E-paper under various conditions. To achieve this, various steps have been taken from study in theory to designing the supplying voltage circuit for the measurements.

For our research we made a schedule of requirements that are reflected on in every chapter. During our research, some difficulty has occurred which will be described in this thesis. Most of them are avoided, some were inevitable.

With the continuous environmental awareness rising globally, researchers from all over the world are looking for alternatives in order to do one's bit to contribute to a better environment. As result of this, researchers from the TU Delft are currently developing a technology that can replace all ordinary papers by one single device: Super E-paper.

Those who are interested in reading about the market analysis of our product are advised to read the first part of this report (chapters 2 and 3). The ones interested in the technology behind the Super E-paper and technical research conducted on this Super E-paper, are advised to start reading from part 2 onwards (chapters 4 to 9).

We would like convey our special gratitude to the following persons for their useful contributions.

- Dr. R. Ishihara (TU Delft), for his overall support and guidance throughout the project
- J. Derakhshandeh Kheljani (TU Delft), for his support and guidance with respect to all the measurements conducted in DIMES
- Wei Man Chim (Master graduate from TU Delft), for his master thesis on flexible E-paper and his support
- P. J. F. Swart (Electronic components, technology and materials), for the tutorial of how to use the different measurement machines.
- N. Saputra, (TU Delft), for his support with regards to the level shifter
- A. Baiano, (TU Delft), for his PhD thesis on Single Grain TFTs
- D. Tajari Mofrad (TU Delft), for his explanation of the Excimer Laser process and support
- J. Hoekstra, T. Slats, M. Schumacher for their support by providing the equipment and materials for the circuits we've built.

Amit Gupta & Miki Trifunovic
Delft, 28 May 2010

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Abbreviations

a-Si	= Amorphous Silicon
AC	= Alternating Current
c-Si	= Single-Crystalline Silicon
DC	= Direct Current
dId/dVgs	= Derivative of the Id function to the gate-source voltage
E-paper	= Electronic paper
Fa	= Attraction Force
Fe	= Electric field Force
Fq	= Coulomb Force
Fv	= Van der Waals Force
GND	= Ground voltage or zero volts
HV	= High Voltage
HV SG-TFT	= High Voltage Single Grain Thin-Film Transistor
Ids or Id	= Drain-Source Current
IDVD	= Drain Current versus Drain Voltage
IDVG	= Drain Current versus Gate Voltage
ITO	= Indium-Tin-Oxide
LV	= Low Voltage
MOSFET	= Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	= N-type Metal-Oxide-Semiconductor Field-Effect Transistor
p-Si	= Poly-crystalline Silicon
p-TFT	= Poly-crystalline Silicon Thin-Film Transistor
PMOS	= P-type Metal-Oxide-Semiconductor Field-Effect Transistor
QR-LPD	= Quick-Response Liquid-Powder Display
SG-TFT	= Single-Grain Thin-Film Transistor
SMU	= Source Monitoring Unit
SOI	= Silicon-On-Insulator
TFT	= Thin-Film Transistor
TU Delft	= Delft University of Technology
U	= Voltage
Vcommon	= Voltage supplied to the common electrode
Vds or Vd	= Drain-source Voltage
Vgs or Vg	= Gate-source Voltage
Vstep	= Voltage step size
VSU	= Voltage Source Unit
Vth	= Threshold Voltage

Summary

Introduction
With the so many available sorts of E-paper, the optimal performing and consumer friendly E-paper needs to be found in order to win the E-paper market. As result of this, researchers from the TU Delft are currently developing a technology that can replace all ordinary papers by one single device, which has outperforming characteristics compared to the current E-papers: Super E-paper. In order to launch this superior product, a research needs to be conducted with regards to the optimum driving method of the Super E-paper. This thesis shall not only investigate what the optimum driving method of the Super E-paper is, by applying different types of power to the product. But also describe our steps towards this measurement by sharing background knowledge, linking theory to practice, designing the source that will be used for our Super E-paper measurements. For the measurements, several variables are analysed:

- Voltage amplitude
- Frequency of the source (number of electric pulses sent to the Super E-paper)
- Duty cycle of the source (the percentage of high voltage within a period of an electric pulse)

Core
Through our market analysis a schedule of requirements of our product has been developed. These requirements are met through our technical research in every chapter. The most important requirements prove to be the flexibility of the Super E-paper and the wirelessly refreshable feature.

The Super E-paper is made up of two main technologies. The first technology is the Single Grain Thin-Film Transistor (SG-TFT) that is used for the back plane of our product. This transistor compared to other types of transistors is manufactured at low temperatures so that flexible plastics can be used to build the transistors on. This makes flexible electronics possible. The technology also makes it possible to stack transistors so that in the final product all electronics are integrated behind the display, for wireless interaction and an edgeless product.

The second technology is the Quick-Response Liquid-Powder Display (QR-LPD) technology that uses oppositely charged and coloured particles that are attracted and repulsed through appliance of voltage on the screen. This second technology is also flexible and faster than other front plane technologies and is therefore beneficial for the full flexibility of our final product and displaying motion pictures.

SG-TFT proved to be better than poly crystalline TFT's which has worse electrical properties due to the type of silicon used. The Silicon-on-insulator (SOI) transistors that we measured had worse characteristics than the SG-TFT transistors we measured, however theoretically the range of the SOI transistor's mobility should be higher than those of SG-TFT's. The performance of the SG-TFT and the low temperature process of manufacturing such a transistor make it ideal for the flexible Super E-paper.

The prototype Super E-paper requires to be driven by a voltage of at least 35V. We made a level shifter that can send pulses of 70V for a better result. Three level shifters have been designed: the first and basic design had an overloading issue, so that in the second design we have placed a resistor to avoid this problem. This second design has been used for short periods of time for our measurements with the prototype when another error has been discovered. The third design avoids the problem of breakdown voltage on the PMOS transistors, and outputs gradual increasing pulses of higher than the threshold voltage.

Active Matrix addressing of our Super E-paper prototype proved to be difficult due to the bad visibility of the under laying design behind the pixels. Data lines that were available on the back plane

that were running under the pixels were used to activate the pixels which showed more movement within the pixels compared to previous research by A. Baiano and W. M. Chim. A remarkable condition has been discovered when applying voltages to both electrodes for the movement of the pixels, the pixels changed when both voltages were switched off.

During our Passive Matrix research, we used a flexible plastic substrate with metal shapes, made by electron beam evaporation, on which the QR-LPD has been pasted to model a flexible display. Effects of various types of voltages applied through the metallic shape have been analyzed.

Conclusion

The 70V pulse proved to have a better effect on the Super E-paper Display than the 70Vdc voltage. We also discovered the issue when applying a pulse to one electrode, and high voltage at the other. When switching off both voltages, the screen shows change because of the slight delay of shutting down of the pulse voltage.

It was clear that higher amplitude caused a bigger electric field which caused more movement in particles. Also when duty cycle was equal to 100% we may assume the source to be supplying a DC voltage and so we could say that the pulse voltage compared to the DC voltage had more effect on the particles in the pixels. We faced however some difficulties during our research so that a specific optimum frequency, amplitude, and duty cycle were hard to define. A list of difficulties in the order of importance follows:

1. lack of change in pixels when voltage applied;
2. no common reference point to be able to compare different situations;
3. no visibility of the colour of the grains under the microscope;
4. circuitry underneath the pixels was invisible and of incorrect size;
5. no plastic layer keeping the Liquid Powder at its place.

Recommendations

For future research we have a number of recommendations:

1. Use a new front plane that makes the underlying circuitry visible so that active matrix addressing can be checked accordingly.
2. This new front plane should have equal active matrix addressing cell size as pixel size.
3. Ask from Bridgestone a separate piece of E-paper front plane that can be used for passive matrix addressing.
4. Use a magnifying glass in stead of a microscope to see the movement of different coloured particles.

1. Introduction

Electronic paper or E-paper is a display technology that mimics the appearance of ordinary ink on paper. While a conventional flat panel display, like LCD displays for example, uses a backlight to display its pixels, E-paper reflects light like any ordinary paper. The reading comfort of such E-paper therefore is exactly the same as ordinary paper making it possible for one to enjoy hours of reading on such a device without getting their eyes strained, like when looking at a conventional flat panel device. One single device can replace all the papers needed for books, newspapers, flyers etc. Besides a better space utilization and lighter transportation, the biggest advantage of this device is the fact that it contributes significantly to a better environment. Due to the utilised technology, the power consumption of the E-paper is also very low. With the rapidly advancing technology, researchers from the TU Delft now have managed to make a new type of E-paper also known as the Super E-paper. The Super E-paper has compared to the current E-paper: Full flexibility, a higher refresh rate so that animations can be played, full colour, and integrated drivers within the display that minimizes the edges around the display.

Super E-paper however, needs to be further developed before it can enter the display market. One of the researches required on the product is the optimum driving method. At this point the exact specifications on the best functioning conditions of the device are still unknown.

Research on these conditions is absolutely essential for the development of the product. Not only is this necessary for bringing the product to the market, but when further experiments and research need to be done with the product, one can greatly benefit from the information on the optimum driving methods.

The goal of our project is to investigate what the optimum driving method of the Super E-paper is by applying different types of power to the product.

We followed the following steps for our research on the Super E-paper. We have analyzed TU Delft's driving backplane, combined with the E-paper front plane from Bridgestone; together they form the Super E-paper. We will design a level shifter for supplying the product. In order to discover the optimum driving method, several conditions are analyzed:

- Voltage amplitude
- Frequency of the source (number of electric pulses sent to the Super E-paper)
- Duty cycle of the source (the percentage of high voltage within a period of an electric pulse)

Naturally, each phase of our research had some restrictions and requirements, these requirements will be first analysed and later met in every chapter. Changes in pixels are analyzed under the microscope and for a better analysis, these changes are filmed. The pixels are monitored carefully while triggering the pixels on the Super E-paper with different variables. However, noted changes are subjectively measured, since individual particle changes are impossible to be quantified. The rates at which pixels change rely therefore on the individual analyzing.

This report is divided into two parts. The first part provides intrinsic information about the market analysis and the second part gives the outcomes of our technical research. The market analysis starts in chapter 2. This chapter describes all the market participants for the applications of our product. The other chapter in this section (chapter 3), will provide a schedule of requirements.

Chapters 4-9 give outcomes of our technical research. Chapter 4 reveals in-depth information about the various technologies used in the Super E-paper based on our literature research. In the 5th chapter the results from the measurements on SG-TFT's are analysed. Chapter 6 provides information about the level shifter, which is designed to supply the E-paper with high voltage pulses. Bridgestone's E-paper measurements can be found in the 7th and 8th chapter, starting with Active Matrix addressing and afterwards Passive Matrix addressing. The conclusions and recommendations about the technical research can be found in the last chapter, chapter 9.

PART I
Market Research

2. Market analysis

The product that we are researching is new and is not yet introduced to the market. Expectations of how well the Super E-paper will do in the market can be analysed through its external environment [1]. This analysis gives an overview of all the players in the market in which the product is active. Through this analysis we can obtain the requirements and restrictions of our product. Our research however is searching for the optimum way to drive the product. In the next chapter we will give a schedule of the requirements of our technical research.

This chapter is divided into three sections, each explaining a different type of player in the market. Section 2.1 gives an overview of the customers and their requirements. Section 2.2 explains who the suppliers for the Super E-paper will be. Finally, the third section will give an overview of the competition in the Super E-paper market

2.1 Customer requirements

The following section shall elaborate on the requirements of the main customers of our E-paper technology. These customers can be divided in three sectors; advertisement, newspaper and others. Subsection 2.1.1 shall be devoted for the advertisement branch. Subsection 2.1.2 shall provide information regarding the newspaper branch.

2.1.1 Customer 1: Advertisement

In the Netherlands there are two main companies active with regards to advertising. The biggest of them is JCDecaux and the second largest is CBS Outdoor. Both of them are interviewed, to get a feeling on their view of the application of E-paper in this market sector. Here follows a brief summary about the requirements of the Super E-paper for these two players.

JCDecaux

From the interview with JCDecaux it became clear that replacing all the $2m^2$ (bus stop size) spaces won't be cost effective, as the cost of paper posters is significantly lower than the costs of E-paper. However about 1,500 of the $2m^2$ posters and all the larger posters of 8 m^2, use a rotating system that allows JCDecaux to display multiple posters at an interval without manually having to change them. These systems are relatively expensive and replacing these with the E-paper can be a very lucrative investment. More detailed information about the interview can be read in the [2]

CBS Outdoor

CBS Outdoor (previously called Viacom Outdoor) a sub-division of the CBS Corporation is also one of the leading outdoor media companies globally. From the interview with CBS Outdoor, it became quite clear that CBS Outdoor sees the implementation of the E-paper in their advertisement business as an opportunity to set a stronger hold in this market section. The reason why CBS believes so is E-paper's ability to refresh advertisements using wireless transmission. This way the advertisements don't need to be manually changed, which in its way contributes to CBS Outdoors cost saving procedures. Therefore, they would like Super E-paper to have a lifecycle of at least 4 years after calculating the possible price of the product. The full interview can be read in [3]

2.1.2 Customer 2: Newspaper

In the Netherlands, about 3.5 million people have a subscribed to a newspaper[1]. With such a large number of subscribers, successfully penetrating this market shall definitely give a boost to us. During the interviews with relatively large market players in this field, HDC Media and Het Financieel Dagblad, their interest in an e-newspaper as a substitute for the conventional paper version became clear. Here follows a brief summary about the requirements from the newspaper branch.

HDC Media

HDC Media was certainly interested in the Super E-paper, however was waiting for it to develop further. HDC Media is looking for a version of E-paper which has a price from approximately 150 euro's, flexibility of the display for the newspaper feeling, and they were looking for the possibility of displaying multiple pictures. Once the technology is this advanced, HDC Media hopes to deliver the news quickly and efficiently per region (city or neighbourhood). An option of bonus editions or updates, in case the customer pays extra, should also be integrated. They also hope that the option of viewing high resolute videos on the Super E-paper, should also be possible in the next version. The biggest advantage HDC Media sees from this product, apart from the cost cutting factors, is quickly updating its customers. They therefore hope to attract customers as they shall be providing a service keeping all its customers fully updated at all times and therefore making the midnight deadline obsolete. More detailed information about this all can be read in the [4]

Het Financieel Dagblad

Het Financieel Dagblad (FD) is a Dutch newspaper. As the internet is rapidly taking over the news-supplying-market, FD is having troubles keeping up with this digital world. In order to safeguard itself, the company therefore wants an innovative tool/idea to attract new customers. They said that they would like the Super E-paper to have a function of being a personalized product, which could adjust the news to the taste of the subscriber. By implementing this new technology, the company hopes to save costs, provide better service to the customers and hopes to attract new customers. The price of our product should range from 100 to 200 euro's. According to FD the two most important requirements for this product are: remaining up-to-date and adjusting to personal interests/requirements. The full interview can be read in [5]

2.2 Suppliers

Super E-paper uses two main technologies that are supplied by Bridgestone and JSR. These technologies make it possible for the product to be flexible, however certain conditions naturally have to be met. Bridgestone supplies us with the Quick-Response Liquid Powder Display (QR-LPD) that can only be driven with at least 35 volts. JSR supplies us with liquid silicon that forms the basis of the driving circuit for Bridgestone's display. More information on the suppliers of our product can be found in [1]

2.3 Competitors

Products competing with Super E-paper have an influence on product requirements, if our product would be much more expensive than the products of our competitors, the Super E-paper would be pushed out of the market. Besides the type of competitor that produces a similar product as ours, a different type would be is the substitute. Products such as plain paper, non E-paper displays or E-readers can be used for the same purpose as the Super E-paper. The extra features that we offer such as flexibility, motion on display, full colour, energy efficiency, should outperform the competing products. More information on the competitors of our product can be found in. [1]

3. Schedule of requirements

Product requirements can be derived from our market research, however in our technical research we will be focussing on the optimization of driving the product. Our product is relatively new and specific customer orientated requirement implementation is still difficult. Our thesis will however meet some of these requirements and at the end of chapter an evaluation, of the requirement that has been met through the corresponding research, shall be provided

Super E-paper features

Super E-paper has a number of features that it aims to achieve:

1. fully flexible display;
2. all drivers and electronics integrated in the display so that the final product will have minimum edges, together with feature 1, this would mean that the electronics are flexible as well;
3. full colour and animations possible;
4. wireless communication possible;
5. energy efficient.

These features make the product besides a useful replacement for current billboards and newspapers, possible to replace current price tags, E-readers, make clothing with animated pictures possible, and even flexible medical sensors are some of the many potential applications of the Super E-paper.

Requirements based on market research

The market stakeholders have a couple of requirements regarding what the product needs to be. These requirements are ordered, starting with the most important requirement first.

[1.1] Super E-paper needs to be able to display multiple images with minimum effort (all customers indicated in section 2.1).

[1.2] The product needs to be fully flexible since no other non E-paper displays or current E-readers have this ability (suppliers and competitors from chapter 2).

[1.3] The same product should be wirelessly refreshable (all customers indicated in section 2.1).

[1.4] Super E-paper must be cheaper than current LCD screens (advertising companies).

[1.5] The newspaper variant of Super E-paper needs to be flexible to maintain a similar feeling to the current paper newspaper (newspaper customers from section 2.1).

[1.6] The newspaper variant of the product needs to have a price of approximately 150 euro's (HDC Media and Het Financieel Dagblad).

[1.7] The billboard variant of the product should have a lifecycle of at least 4 years (CBS Outdoor).

Requirements concerning the ecological and social situation

Here follows a list of requirements seen from the environmental, safety and social perspectives.

[2.1] Product should meet internationally set product safety standards with regards to EM-radiation.

[2.2] Product should meet internationally set product safety standards with regards to the health and safety of consumers using our product.

[2.3] Product should meet internationally set product safety standards with regards to the hazardous materials that may spread when the product is damaged.

Requirements concerning the design of the product

Here follows a list of requirements with regards to the design of the product. This is categorized in three subsections: User interface requirements, Production requirements and Usage requirements and Recycling requirements.

User interface requirements

[3.1.1] The Super E-paper should be easy to use through its interface.

[3.1.2] The Super E-paper should be able to adapt to the user's personal preferences (text size, etc).

Production and usage requirements

[3.2.1] With regards to the production of the Super E-paper, both the technologies μ-Czochralski and QR-LPD shall be applied.

[3.2.2] The production process of the Super E-paper shall be led by certified members only.

[3.2.3] The production process should produce minimum harm to the environment

[3.2.4] The display resolution should have a similar appearance as print on paper.

[3.2.5] The product should be able to play animations.

Recycling requirements

[3.3.1] Product should meet internationally set product recycling standards with regards to the materials used, which could be harmful for the environment once disposing or recycling.

[3.3.2] Upon breaking the display, it should be able to be replaced by a new screen

Schedule of product requirements based on our technical research

For our research we analysed a prototype Super E-paper under the microscope and applied different types of voltages to drive the pixels. By varying a single parameter from the 70V pulse, for example, the frequency, the duty cycle or the amplitude, we can see at which values of these parameters the change in pixel colour is the greatest. Therefore our primary requirement is:

The pixel has to change more heavily for a value of the variable closer to the optimum parameter setting.

Related sub requirements would be:

- The difference in change of pixel between two different valued parameters should be great enough to be able to assign the change of pixel to the change of value in the corresponding parameter.
- A common reference situation should be realized to compare the change in value of the parameters under equal conditions.

When these requirements are met, the optimum driving method can be derived. Once the optimum driving method is concluded, research for meeting the other requirements in this chapter can be focussed on.

In this thesis we have divided our approach of testing the prototype into several sections that meet the requirements announced in this chapter. The requirements that need to be met are briefly explained in the introduction of every chapter, and evaluated at the end of every chapter.

Chapter 4: Technological background of Super E-paper
Requirement: The capabilities of the technologies used

Chapter 5: Measurements on the Single Grain Thin-Film Transistor
Requirement: The choice of SG-TFT over other transistors

Chapter 6: Level shifter: supply for the Super E-paper
Requirement: The required supply for driving the E-paper front plane

Chapter 7: Active Matrix Measurements on Bridgestone's E-paper
Requirement: Identifying the optimum parameters through the Active Matrix approach

Chapter 8: Passive Matrix Measurements on Bridgestone's E-paper
Requirement: Identifying the optimum parameters through the Passive Matrix approach

PART II
Technical Research

4. Technological background of Super E-paper

The Super E-paper uses two main technologies [6]. The first one is the Single Grain Thin-Film Transistor (SG-TFT) which is developed by TU Delft. The other one is the Quick Response Liquid Powder Display technology (QR-LPD) that is developed by the company Bridgestone. The two technologies are needed for the construction of Super E-paper: the SG-TFT is used for the integrated circuit backplane of the device and the QR-LPD is required for the E-paper front plane of the device.

In this chapter these technologies are explained. Section 4.1 describes the different types of transistors, the manufacturing process of a SG-TFT, and finally the resulting product. Section 4.2 explains the physics behind QR-LPD, and the structure that is used in the front plane of the Super E-paper. Section 4.3 is a summary of the discussed technologies with reflection on the schedule of requirements

4.1 The Single Grain Thin-Film Transistor

This section will start with a brief background explanation of different materials used for transistors, and how this is important for the SG-TFT. The process and technique of manufacturing such a transistor is explained afterwards, and finally the advantages of such a transistor are discussed. The theory can be found in [6][7][8].

4.1.1 Types of Transistors

Transistors are made of different types of semi-conductor material. Amorphous silicon (a-Si), polycrystalline silicon (p-Si) and single crystalline silicon (c-Si) are some of the different types of silicon used to make a transistor. The types are characterized by the size of an ordered region within the material. Ordered regions in this sense are spatial volumes in which atoms or molecules have regular geometric periodicity. These ordered regions are also known as grains and are separated by grain boundaries when more grains are present in the material. A-Si has almost no order or ordered regions, p-Si does have ordered regions, but these vary in size and orientation with respect to each other, and c-Si has a high degree of order or regular geometric periodicity throughout the entire volume of the material as shown in Figure 4.1. Ordered materials have superior electrical characteristics to non-ordered materials and are therefore preferred [7].

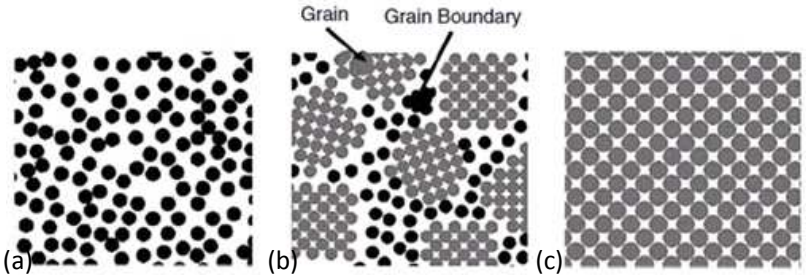


Figure 4.1: Different types of solids: amorphous silicon (a), polycrystalline silicon (b), and single crystalline silicon(c). [9]

Thin-Film Transistors (TFT) are special types of MOS transistors, where a thin film of semiconducting material is deposited on a substrate like glass for example. However, since the silicon must be deposited, only a-Si or p-Si materials can be used, which ultimately results in a lower electrical performance than single crystalline versions of MOS transistors. The c-Si transistors are made from c-Si wafers that are grown from a single seed so that the wafer as a whole consists of a single grain.

There is however a way to greatly improve an a-Si TFT so that the electrical properties will become comparable to the c-Si transistor. This process is also known as the µ-Czochralski process and uses a special way to fabricate high performance TFT's at a relatively low temperature of 100°C [10]

4.1.2 The Manufacturing Process of a SG-TFT

The µ-Czochralski process is used to locate single grains from amorphous silicon and let it grow as a seed to single grain islands so that TFT's can be built within this single grain island. This greatly improves the electrical performance TFT since there are no grain boundaries within the TFT that degrades its performance. The process of making one single grain is illustrated in Figure 4.2. and explained in the following steps:

Step 1: A substrate is chosen, since the µ-Czochralski process works with relatively low temperatures (350°C compared to over a thousand degrees Celsius for a regular transistor), we can use plastic as a substrate as well. (Figure 4.2(a))

Step 2: A layer of the insulating material silicon dioxide (SiO_2) is deposited on top of the substrate. (Figure 4.2(b))

Step 3: Holes are made in the SiO_2 by using a grain filter. This grain filter patterns a grid of cavities over the whole layer of SiO_2. (Figure 4.2(c))

Step 4: A layer of a-Si is deposited on top. This layer covers the whole area and fills up all the holes made by the grain filter. (Figure 4.2(d))

Step 5: Excimer Laser is used to melt the top part of the a-Si layer, leaving a non-molten a-Si crystal at the bottom of the hole. This crystal will serve as the seed that grows into a single grain island on top of the SiO_2 layer. Excimer Laser is used because this laser type can remove very thin layers of surface material with almost no effect to the rest of the material. (Figure 4.2(e))

Step 6: Within every grain phosphorus or boron is implanted to form NMOS SG-TFT and PMOS SG-TFT respectively. (Figure 4.2(f))

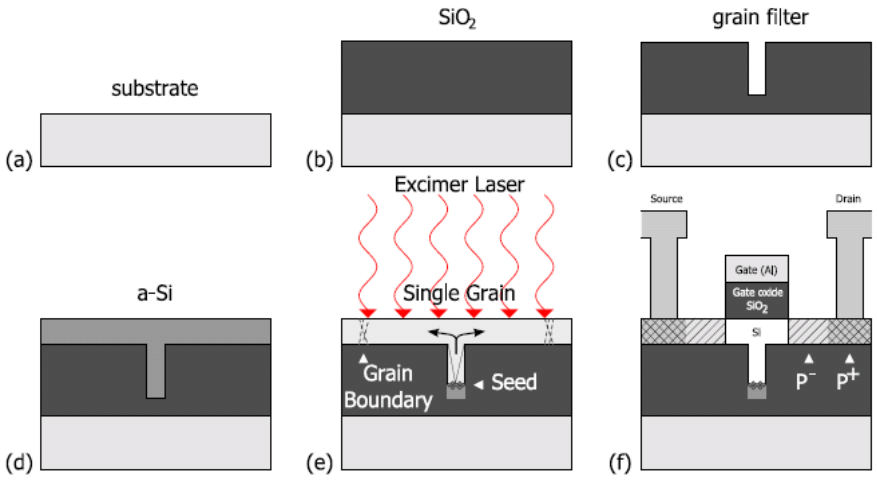


Figure 4.2: µ-Czochralski process for the manufacturing of a single SG-TFT: starting with a substrate (a), with a layer of SiO_2 deposited on top (b). Then by using a grain filter, a hole in the SiO_2 is made(c) which gets filled by the deposition of a-Si (d). Excimer Laser melts the top layer leaving a seed at the bottom of the hole (e). Finally we have a transistor (f). [6]

Since TFT's are made within a single grain island, the grain boundary limitations are not an issue anymore and the electrical properties are greatly improved. However, the TFT's do have minor planar defects as shown in Figure 4.3. These planar defects have a far less negative effect on the electrical properties compared to the effects of grain boundaries.

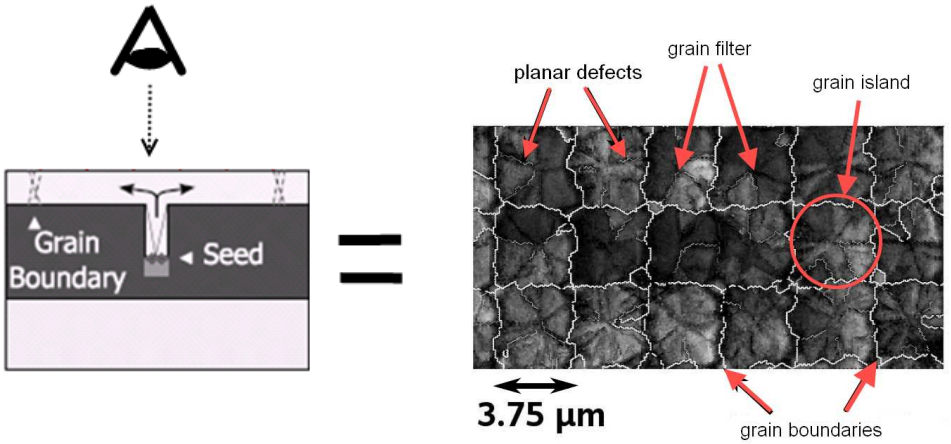


Figure 4.3: Microscopic view of the grid of grains, showing the planar defects, grain filter holes, grain islands and grain boundaries. [8]

As we will discuss in section 5.2, Bridgestone's E-paper front plane requires a supply voltage of 70V. An SG-TFT that we described in the previous section would break down at these voltages; breakdown voltage is about 6V. Therefore, an extra processing step is needed. A thicker gate oxide and a change in doping profile are needed. This High Voltage SG-TFT (HV SG-TFT) can handle the 70V supply voltage but is slower in return. A combination of both the fast but fragile SG-TFT and the strong but slow HV SG-TFT is needed for driving at high speeds and low voltages, and change pixels on the screen respectively.

4.1.3 The SG-TFT features

The SG-TFT technology offers the possibility of 3D-integrated circuits and flexible electronics[11]. 3D-Integration of integrated circuits (IC's) is now possible because the transistors can be stacked. The stacking is made possible by the use of Excimer Laser technology, which doesn't penetrate through multiple layers of transistors, but only a very thin layer as shown in Figure 4.2(e). This stacking of electronics would mean for the Super E-paper that all of its electronics can be integrated behind the display. In Figure 4.4 this feature is used with an inverter.

The development of flexible electronics is also a positive feature for the Super E-paper. This flexibility is made possible due to the relatively low temperature manufacturing process (100°C). Due to this low temperature, every type of flexible plastic can be used as a substrate for flexible electronics.

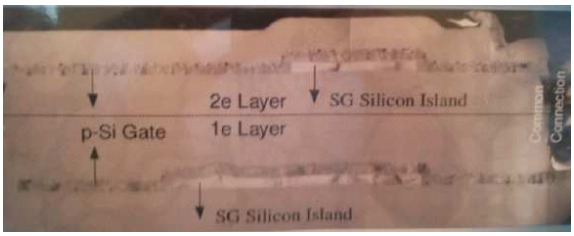


Figure 4.4: 3D inverter made from SG-TFT's, picture from transmission electrode microscope (TEM) [12]

4.2 The Quick-Response Liquid Powder Display

Figure 4.5: QR-LPD developed by Bridgestone [13]

While Bridgestone's core business is tire production, they have managed to be the first to develop a new Electronic Liquid Powder suitable for making E-paper Displays. They managed to achieve this by using the high-level materials design and processing technology cultivated through their tire business. The E-paper Displays using this highly advanced technology are also known as QR-LPD (Quick-Response Liquid Powder Display).

A paper like appearance, low power consumption, high resolution, an excellent image stability, quick response, and clear threshold characteristics are the ideal characteristics which make the QR-LPD the ideal technology for the E-paper displays. The theory discussed in this section can be found in [6] [11]

Subsection 4.2.1 will describe the properties of Bridgestone's newly made Liquid-Powder and shall also describe the forces which are acted on the particles and in subsection 4.2.2 the structure of the QR-LPD is explained. Finally, in section 4.2.3 other types of E-paper are discussed briefly.

4.2.1 Properties of the QR-LPD

E-paper is a type of display technology that has similar characteristics to paper. It doesn't require backlight since it simply reflects light as plain paper does. It is also very thin, light and doesn't consume energy while displaying a static image. Through electronics the display can be updated.

The Electric Liquid Powder developed by Bridgestone for the QR-LPD, is an electrical sensitive powder which combines the properties of a liquid and powder. Because of this combination, the material despite having a powder form, still behaves like a liquid; making the material highly fluid and easily suspended, where every single particle reacts to the electric field.

Bridgestone has developed two types of powders: a negatively charged white coloured powder and a positively charged blacked coloured powder that are placed between two electrodes. One of the electrodes is made of Indium-Tin-Oxide (ITO) which is both conductive as well as optically transparent. Once a negative voltage is applied over an electrode, the black particles get attracted to this electrode and once a positive voltage is applied the white particles will. More detailed explanation can be found in section 4.2.2. Observing this, we can conclude that the Liquid-Powder moves when subjected to an electric field. Figure 4.5 shows the forces implied on the powder particles.

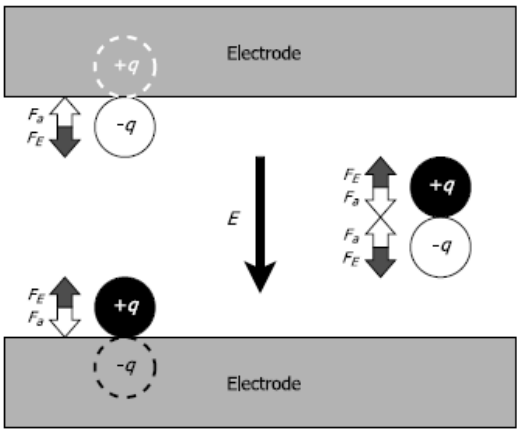


Figure 4.6: The electric field causing movement in the Liquid-Powder particles [6]

Forces applied in the QR-LPD

The particles in the figure are given two sorts of colours; the positively charged black particle and the negatively charged white particle. As the charges of the particles are intrinsic to themselves, external frictions to obtain those charges are not required. Basically, there are three forces applied on the particles; the attraction force Fa, the image charge force and the electric field force Fe. The attraction force Fa is the force which attracts the positive and negative particles to each other. This attractive force consists of two forces; the Coulomb force Fq and the Van der Waals force Fv. Everywhere in the cell this attractive force is of the same magnitude, but only at the surface of the electrode an additional force acts upon the particles. This force is called the image charge force and arises due to the polarization of the electrode by the charged particles. Due to this polarization the charged particle is kept at its position on the electrode even when the electric field is removed. In other words, these attractive and repulsive forces between the particles and the electrodes make it possible to retain an image on the display without any power consumption; a black image when the electric field is removed after applying negative voltage to the electrode, and a white image when the electric field is removed after positive voltage. This feature makes the QR-LPD bistable.

Once voltage is applied on the electrodes, the electric field that arises acts as a repulsive force to the pair of oppositely charged particles. This electrical field shall therefore separate the oppositely charged particles from each other, once the electric field force Fe is larger than the attractive force Fa. If so, the particles move to the electrode of the opposite charge with respect to their own charge. A similar principle holds for separating the particles from the electrode.

Gradual change of colours

While the particles travel from one electrode to the other, the particles reach high speeds. It has been reported that the particle transfer speed was over 11.11m/sec (about 40 km/hour), the pixel response time will result in 0.2ms from black to white and the other way around which gives the display the capability of showing animations [8][11].

Below in Figure 4.7 the hysteresis plot can be found. This hysteresis plot explains the reflectivity of the particles when different voltages are applied. As can be seen from the plot, once the pixel has a colour, for example black, when a voltage higher than the threshold voltage Vth is applied, the electrode will gradually turn white as more and more white particles are attracted, and black particles are repulsed. Once polarization of the electrode occurs, the pixel will remain in that colour even when the electric field is switched off so the applied voltage is 0V. The pixel will change to the opposite colour again once the negative threshold is reached (-Vth). The QR-LPD requires relatively high driving voltage of 70V and the voltage required to overcome the attractive force is the threshold voltage which is about 35V. The voltage potentials between 35V and 70V are interesting for grey-scale levels. The higher the voltage above the threshold, the more the particles get attracted by the electrode. This causes different grey scale levels for different voltages between 35V and 70V.

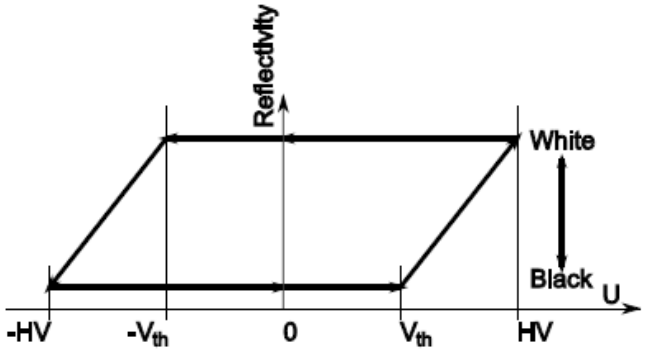


Figure 4.7: Hysteresis plot, reflectivity (pixel colour) versus applied voltage on the electrode. (HV stands for High Voltage and Vth for the Threshold Voltage)[6]

4.2.2 Structure of a QR-LPD

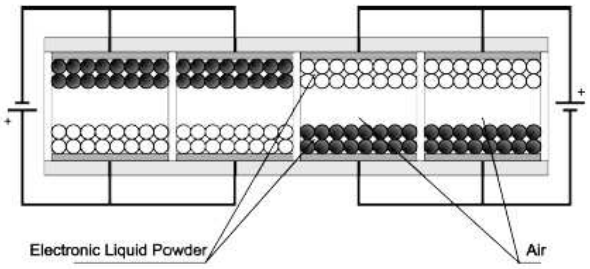


Figure 4.8: Display structure of the QR-LPD [6]

In Figure 4.8 the structure of the QR-LPD is shown. This figure shows four cells only. As we have stated before: each cell contains two types of powder; a white coloured negatively charged powder and a black coloured positively charged powder. As both powders are of opposite charge, the two are attracted to each other forming a grey mass. As soon as the top electrode has a different voltage with respect to the bottom electrode, the particles will arrange at the oppositely charged electrode. When looking at the top electrode, the arrangement of a single particle type is visible, while the other type of particles is attracted by the other electrode and therefore can not be seen. However these particles attracted by the lower electrode, can be seen again once the opposite voltage is applied.

In the cell, the remaining space is filled by plain air, which is also the transport medium and free space for the moving powder particles. The speed of the particles through the air is high enough to give a response time of 0.2ms.[6]

4.2.3 Other types of E-paper

Besides Bridgestone's E-paper that uses charged particles and cells filled with air and driven by electrodes, there are various other technologies that are also recognized as E-paper. Since they also have a paper like appearance, we will discuss two important types briefly.

E-ink

E-Ink is a spin-off from the American MIT Media Lab. The technology uses microcapsules with charged particles and a transparent fluid in them [15]. These particles are attracted and repulsed by applying a voltage between two electrodes that keep the microcapsules in between them. In this sense, this technology is similar to the one that Bridgestone uses, however, Bridgestone uses air in stead of the liquid that make the movement of the particles faster, and also uses cells in stead of capsules, so that no space in between the capsules is wasted.

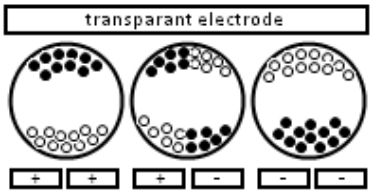


Figure 4.9: E-ink technology displaying 3 pixels as capsules

Electrowetting

Electrowetting is a technology that uses dark oil and water. By applying a voltage, the oil becomes increasingly hydrophilic rather than hydrophobic. Figure 4.10 shows two images of an applied voltage on oil, on a surface of water. When the oil covers a larger surface area, the screen turns black. When otherwise, the light gets reflected through the oil-less area, and white can be observed. The display will consist of cells with water and oil trapped within each cell. An electrode is used to shape the oil so that either the screen absorbs light or reflects light, causing the black and white colours.

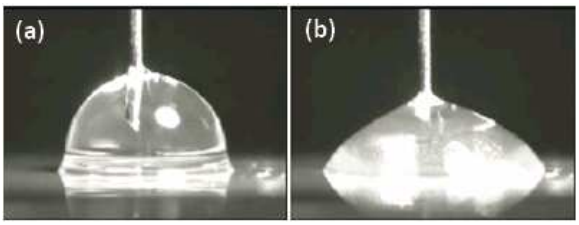


Figure 4.10: A drop of oil positioned on the surface of water, in (a) no voltage is applied in the oil through the electrode, in (b) voltage is applied an oil becomes gradually hydrophilic. [16]

4.3 Summary

In this section, the two main technologies used for making the Super E-paper are analysed. The first technology forms the driving back plane of the Super E-paper which is Single Grain Thin-Film Transistor (SG-TFT) technology. The second technology discussed, forms the Super E-paper front plane that is produced by Bridgestone: the Quick-Response Liquid-Powder Display (QR-LPD) technology.

SG-TFT

There are three basic types of silicon used for making a transistor: Amorphous Silicon (a-Si), Polycrystalline Silicon (p-Si), and Single Crystalline Silicon (c-Si). The types are ordered in size of regular geometric periodicity within the material, where a-Si has least geometric periodicity throughout the material, and c-Si the most. The more geometric periodicity, the less the material has grain boundaries which results in better the electric performance.

Thin-Film Transistors (TFT) are made from a-Si, p-Si and c-Si. The c-Si transistors are manufactured at high temperatures, therefore a-Si or p-Si transistors have to be used. However the μ-Czochralski process makes it possible to make high quality TFT's at low temperatures (<100°C), which makes it suitable to use plastic substrates, from a-Si or p-Si transistors. The process builds TFT's onto single grain islands that are grown, which avoids the grain boundary influence and results in a TFT quality close to c-Si. The SG-TFT's can be used for flexible electronics, and stacking of the electronics.

QR-LPD

The QR-LPD developed by Bridgestone essentially uses two types of particles: white negatively charged particles and black positively charged particles. These particles are placed between two electrodes which attract or repulse the types of particles. One of the electrodes is made of Indium-Tin-Oxide (ITO) that is both conductive and optically transparent. Within the QR-LPD, various forces are applied. The particles attract each other through Coulomb force and Van der Waals force. Once an electric field is applied between the electrodes, the particles will be pulled apart. As soon as the particle touches the electrode, the electrode gets polarized and keeps attracting the particle even after switching off the electric field. This results in no energy consumption when holding a certain image on the display. The screen therefore has a hysteresis effect that changes the colour of the image after crossing opposing threshold voltages. The particles are contained in cells with air as a medium that can individually be addressed as pixels.

Besides QR-LPD, there are two other commonly used E-paper front plane techniques. The first technique is E-ink, which uses microcapsules that contain the same charged particles with a fluid medium; the idea is similar to the QR-LPD. The second technique is Electrowetting which uses the hydrophilic and hydrophobic characteristics of oil when voltage is applied to an electrode. The oil absorbs the light and changes shape within a cell to let light reflect from the other electrode.

Schedule of requirements

Both technologies give an answer to some of the product requirements. SG-TFT makes it possible to use a flexible substrate for achieving flexible electronics. It also has the feature of the possibility of stacking transistors, which is beneficial for the requirement of having an edgeless final product, since all electronics can be integrated behind the display of the Super E-paper.

The QR-LPD is also flexible, so the combination of this technology with SG-TFT makes a fully flexible product possible. The technology also serves the requirement of minimum energy consumption since it doesn't use power when holding a certain image on the display. QR-LPD uses air as a medium in stead of a fluid in E-ink, which results in higher speeds and therefore higher refresh rates. This property of reaching higher speeds, makes animations on the display possible.

5. Measurements on the Single Grain Thin-Film Transistor

In chapter 4 we have discussed about using the Single Grain TFT technology in Super E-paper. In this chapter we will analyze the quality of this type of transistor by measuring the I_D-V_{GS} curve. This curve can provide information of the transistors such as the sub threshold voltage swing, the leak current, the on-current, the threshold voltage, the mobility of the transistor, and the current and voltage characteristics of the transistor when different gate voltages are applied. Ultimately we want to compare the SG-TFT with different transistors to obtain a better knowledge of the quality of such a transistor.

In section 5.1 we will define the different parameters that we will analyze by means of a sample NMOS curve and explain their meaning. Following this section, first the SG-TFT parameters are identified in section 5.2, after which it is compared to the p-TFT. These transistors being both TFT's, can prove to us the higher quality of the SG-TFT. Section 5.3 and 5.4 will compare the SG-TFT characteristics to silicon-on-insulator (SOI). Finally, in section 5.5, a conclusion will be given on the quality of the SG-TFT.

5.1 Measurement parameter descriptions

Comparing transistors is done by analyzing the I_D-V_{GS} curve. From this curve important parameters can be obtained which can be used to compare different transistors. The examples in the following descriptions are used with regards to NMOS transistors. PMOS transistors have a similar but mirrored image in the y-axis. Formula's and ways of finding the various parameters were provided by J. Derakhshandeh and [17]

Mobility

The mobility of a transistor, describes the average drift velocity of a carrier due to an electric field, which is expressed as cm²/Vs and has the symbol μ. When one transistor has a higher mobility than the other, this transistor will usually be of higher quality since the mobility determines the speed of the transistor. This parameter can be calculated from the formula for the drain current, when the transistor is in the linear region. We will use for every measurement minimum V_{ds} which is low enough for the transistor to be in the linear region.

$$I_d = \mu \cdot C_{OX} \cdot \frac{W}{L}\left(V_{GS} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds} \qquad (5.1)$$

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} \qquad (5.2)$$

Where I_d is the drain current, C_{OX} is the oxide capacitance which is inversely proportional to the thickness of the gate oxide t_{OX}. The oxide permittivity (ε_{OX}) is equal to 3.5e-11 F/m [17]. W and L are the width and length of the depletion region of the transistor respectively. V_{GS} is the gate voltage with respect to the source, and V_{th} is the threshold voltage. Finally, V_{ds} is the drain voltage with respect to the source. We take the differential of I_d with respect to V_{GS} to obtain the function:

$$\frac{dI_d}{dV_{GS}} = \mu \cdot C_{OX} \cdot \frac{W}{L} \cdot V_{ds} \qquad (5.3)$$

This function shows that from the I_D-V_{GS}, graph, we need to differentiate it to V_{GS}, and obtain its maximum to get the maximum mobility of the transistor. Figure 5.1 shows the differential graph of I_D-V_{GS} of a sample NMOS transistor.

Figure 5.1: Computing mobility from the dI_D-dV_{GS} graph of an NMOS transistor.

By using formula 5.3, the mobility can be computed by filling in the maximum value obtained from the derivative graph: dId/dVgs. The mobility can then be obtained by:

$$\mu = \frac{dI_d}{dV_{GS}} \cdot \frac{1}{C_{OX} \cdot V_{ds}} \cdot \frac{L}{W} \qquad (5.4)$$

Subthreshold voltage swing

Figure 5.2 shows an example of deriving the subthreshold voltage swing S from the I_D-V_{GS} curve. When a transistor is switched on, a voltage at the gate is applied crossing the threshold voltage. The speed at which it turns on when crossing this threshold voltage is important to the quality of a transistor. A low subthreshold swing accounts for a fast transition from the off-current to the on-current. Optimally the transistor is off when voltage is applied at the gate that is under the threshold voltage, and on when the voltage goes above the threshold voltage. Notice that we use the logarithmic y-axis for easier computation. From the I_D-V_{GS} curve we can easily compute the S in terms of mV/dec. So the voltage needed to increase the current by a factor 10. An ideal transistor has a swing of 60mV/dec [6].

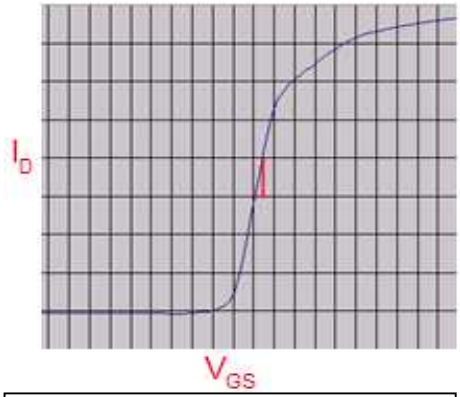


Figure 5.2: Sample NMOS IDVG curve for subthreshold voltage swing computation, Id is logarithmically scaled

Off-Current

It is important to know how much current is "leaking" when the gate-source voltage is under the threshold voltage. A transistor is better if it has a low leak current/off-current. This current is defined as the minimum current in the I_D-V_{GS} curve, as you can see in Figure 5.3. Again the y-axis is logarithmically scaled.

On-Current

How much current is running through the transistor when it is switched on? There has to be a significant difference between on-current and off-current. This ratio would also describe in a lesser sense the speed of the transistor. To obtain this current we take the current level of the transistor that is switched on and saturated when taking the logarithmically scaled y-axis. In Figure 5.3 we also show the on-current of the sample transistor.

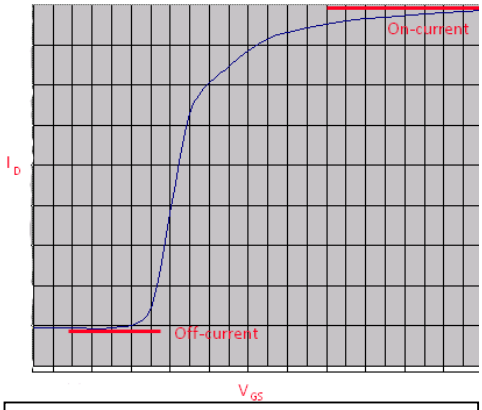


Figure 5.3: Sample NMOS transistor IDVG curve for off- and on-current computation, ID is logarithmically scaled

Threshold Voltage

This parameter defines at what gate voltage the transistor is switched on and off. Preferably this voltage would be between 0V and 1V for an NMOS and between -1V and 0V for a PMOS, so that low gate to source voltages can drive the transistor. To compute this parameter, we need again the I_D-V_{GS} curve, but this time the I_D-axis needs to be in a linear scale. We use the extension of the increasing line through the x-axis to compute the threshold voltage, as shown in Figure 5.4 for a sample NMOS transistor.

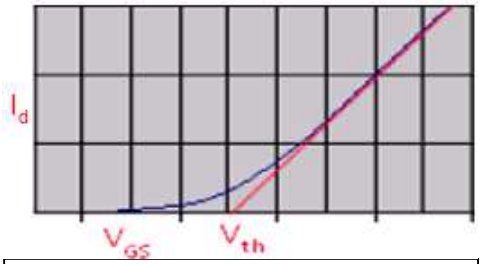


Figure 5.4: Sample IDVG curve for NMOS threshold voltage computation, both ID and VG are linearly scaled

I_D-V_{DS} Curves

Different gate voltages cause different I_D-V_{DS} characteristics. It is important to know how the I_D-V_{DS} curve changes for different gate voltages. Increased gate voltages usually cause an increased saturation linear region. One would have to take care which formula to use for the drain current for a particular gate voltage. Figure 5.5 shows an example of such a curve for an NMOS transistor. For PMOS transistors the curves are in the fourth quadrant with similar shapes but mirrored in the vertical and horizontal axis. For our measurements regarding the IDVG curve, we take a Vds of 0.02V to stay in the linear region of the transistor for every Vgs.

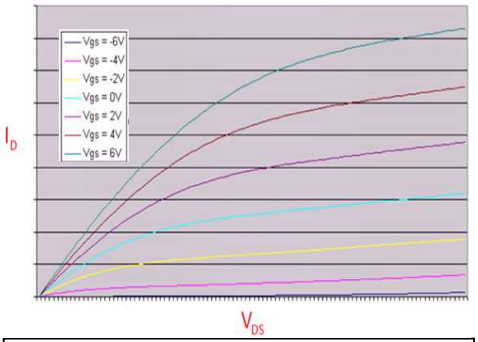


Figure 5.5: sample NMOS I_D-V_{DS} curve with different gate-source voltages

These curves have been appended for every type of transistor for our measurements. The curves are obtained from transistors with short channel lengths which explains why they don't saturate to a constant Id value for high Vds [17].

5.2 Measurement 1: SG-TFT characteristics

In this section we will take a close look at the results of our SG-TFT measurements. The measurements we did with other transistors will come in sections 5.3 and 5.4, since we first need to know what to take as a reference. The SG-TFT is also used in Super E-paper and it is therefore very important to gain a better knowledge of the product. We used a Vds of 0.02V

The particular group of SG-TFT's that we used for our measurements has the following characteristics:

- a gate oxide thickness (t_{OX}) of 27nm,
- made with tetra-ethyl-ortho-silicate (TEOS);
- has 250 nm of silicon thickness.
- channel width is 4µm, and length is 2µm.

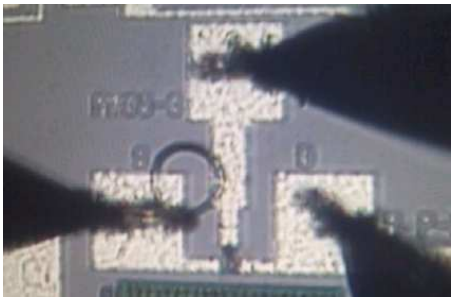
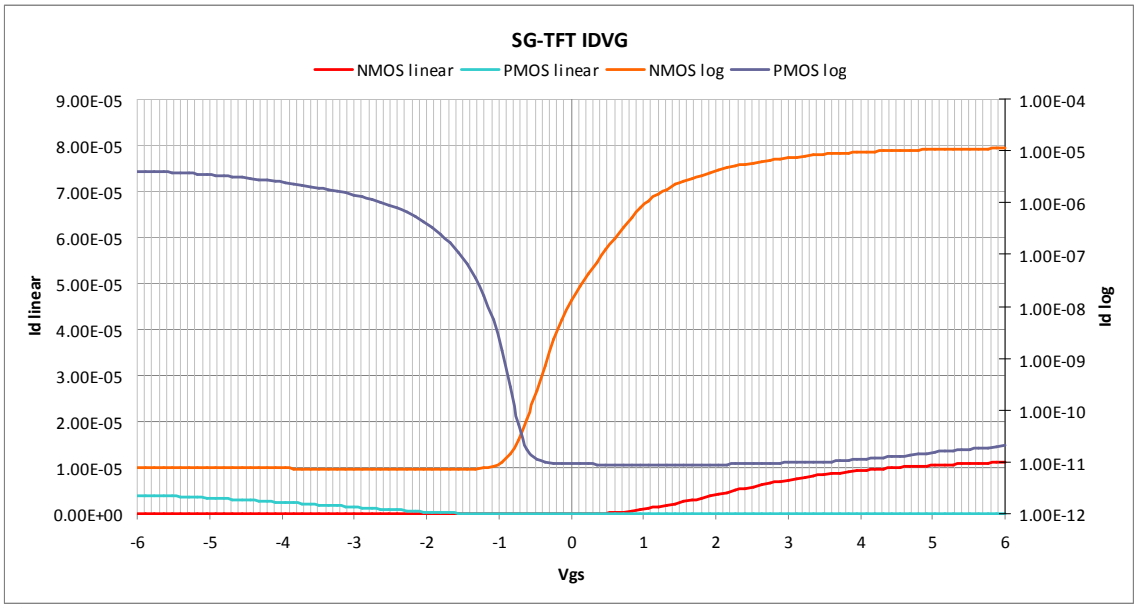
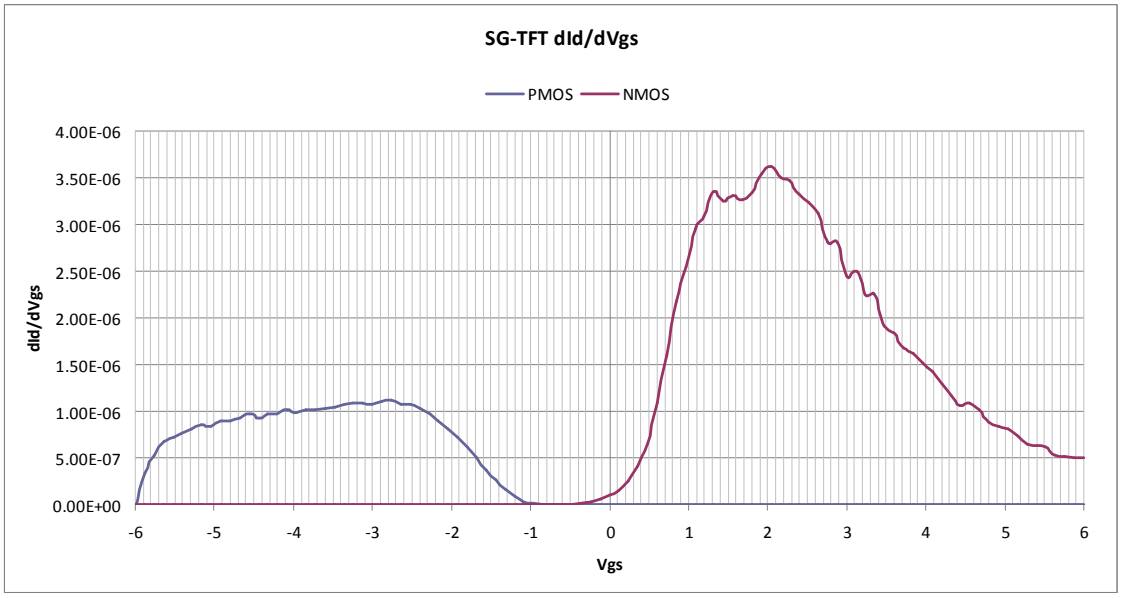


Figure 5.6: layout of the PMOS SG-TFT on the wafer under the microscope

For our measurements we used CAS34 with an 8-slot precision measurement mainframe. These machines can be viewed in Appendix 7. The layout of the transistor under the microscope is observed in Figure 5.6. The source and drains are symmetrical and can be used one way or the other during our measurements. The black areas in the figure are the Source Monitoring Unit (SMU) pins, which are used for measurement purposes. The top pin touches the gate of the transistor, whereas the other two are touching the source and drain. We expect the mobility of this transistor to be around 600 cm²/Vs [10]



(a)



(b)

Figure 5.7: Linear and logarithmic scaled IDVG graphs for both NMOS and PMOS SG-TFT's in (a). SG-TFT dId/dVgs curves for PMOS and NMOS in (b).

Table 5.1: SG-TFT NMOS and PMOS characteristics.

Transistor type	Mobility (μ)	Subtheshold Swing (S)	Off-current	On-current	Threshold Voltage
NMOS	694 cm²/Vs	360 mV/dec	7.3e-12 A	1.1e-05 A	0.8V
PMOS	216 cm²/Vs	480 mV/dec	9.0e-12 A	4.0e-6 A	-1.7V

Id-Vgs

Figure 5.7(a) shows the results of our Id-Vgs measurements on the SG-TFT's. We introduced a Vds of 0.02V to measure the transistor in the linear region. 101 Voltage steps have been taken between -6V and 6V equally separated by 0.12V each. The red and orange lines from Figure 5.7(a) are both the results of the NMOS Id-Vgs measurement. The orange line is scaled logarithmically on the y axis positioned on the right side of the graph. The red line is scaled linearly on the y-axis positioned on the left side of the graph. The dark blue line and light blue line are both the measurement results of the PMOS Id-Vgs measurement and are logarithmically and linearly scaled respectively. From this graph the subthreshold voltage swing, the off- and on-current and threshold voltage can be derived in the ways described in section 5.1. The results are shown in table 5.1.

dId/dVgs

For the mobility, a separate graph has to be made. As function 5.4 describes, the derivative function of the Id-Vgs graph with respect to Vgs has to be made. This derivative graph is shown in Figure 5.7(b). From this graph the maximum values of dId/dVgs for the NMOS SG-TFT (3.6e-6) and PMOS SG-TFT (1.12e-6) can be obtained. These maximums are used in function 5.4 to finally obtain the mobility of the SG-TFT transistors.

Discussion on the obtained parameters

Remarkably the PMOS threshold voltage is less than -1V, which means that this particular SG-TFT needed more doping to shift this level to between -1V and 0V. Also, it is clear that the NMOS transistor is of a higher quality than the PMOS transistor. This can be seen from the much higher mobility, and the higher ratio of on- versus off-current.

During our Id-Vg measurements, Id-Vd measurements have been done as well, and these can be seen in Appendices 1 to 3. For the parameters that we are focusing on, these graphs aren't very important. Both Id-Vd curves however, show in the higher Vds voltages a non linear behaviour; as can be seen in Figure 5.8 for the lower Vgs voltages. This behaviour is due to the thickness of the silicon layer which is 250nm.

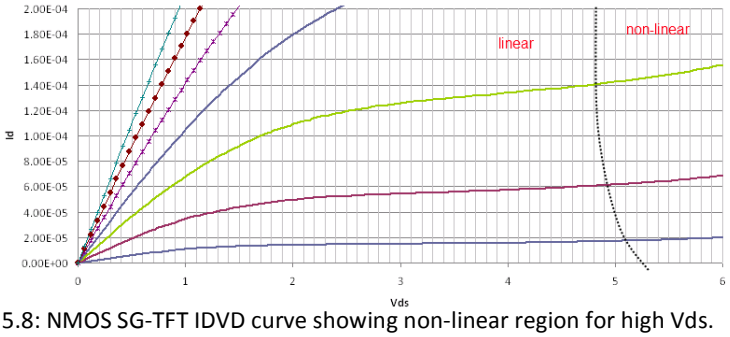
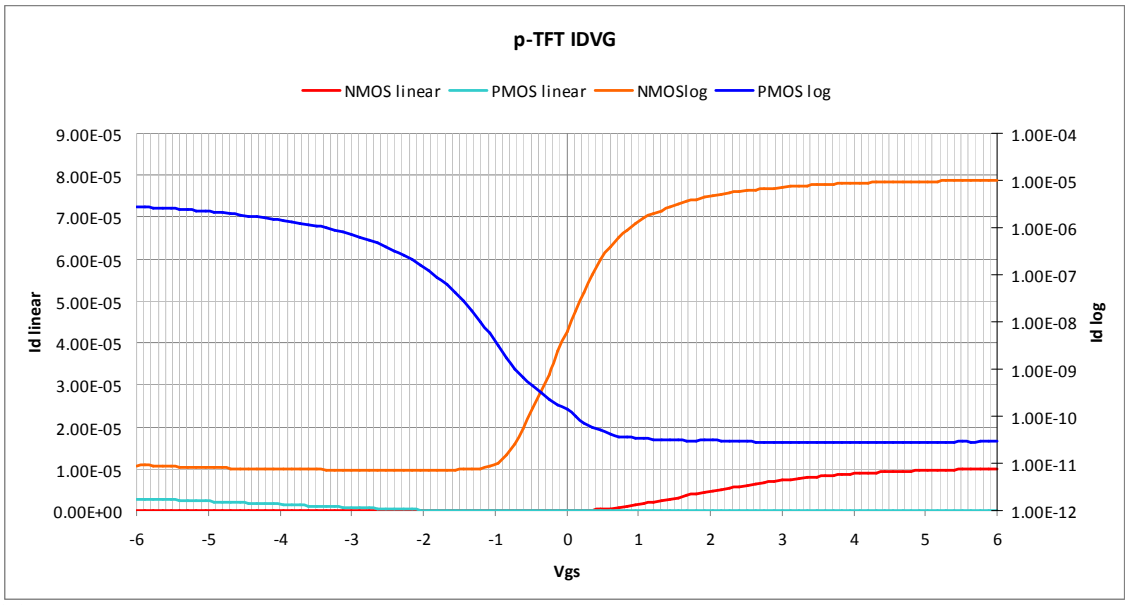


Figure 5.8: NMOS SG-TFT IDVD curve showing non-linear region for high Vds.

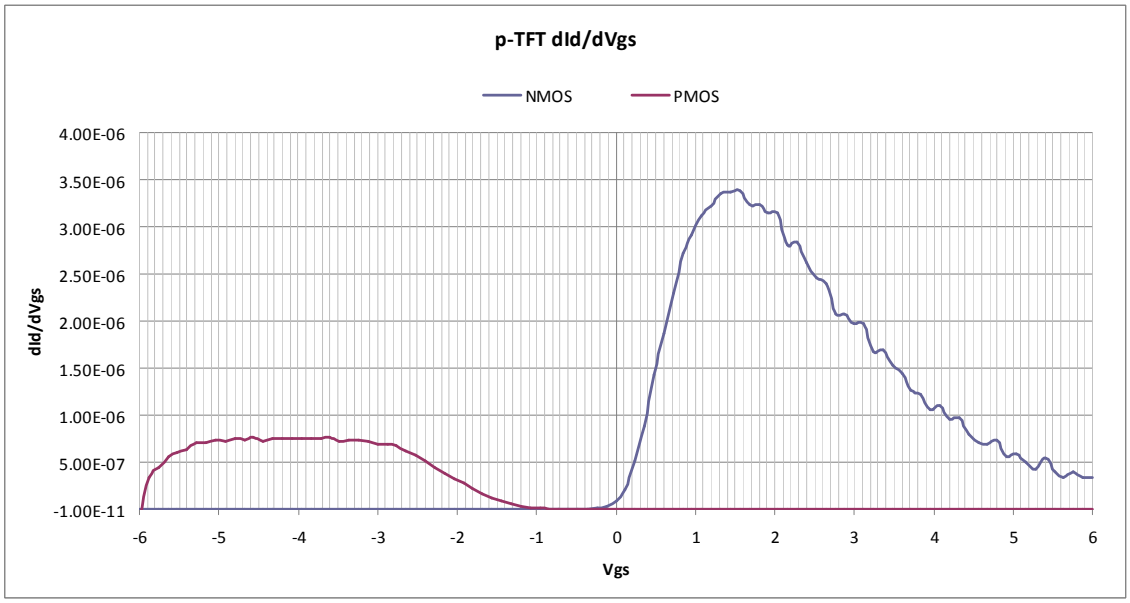
5.3 Measurement 2: p-Si TFT characteristics

In chapter 4 we have already explained that traditional TFT's are from a-Si or p-Si because the silicon has to be deposited. We used a Vds of 0.2V. Since these transistors have negative influence by the grain boundaries, we should see worse transistor characteristics than the SG-TFT's. The layout of the device on the wafer we used is the same as the SG-TFT layout. We expect the p-TFT to have a mobility up to 100 cm^2/Vs [10]. The particular p-TFT we used for these measurements had the following characteristics:

- a gate oxide thickness (t_{OX}) of 27nm;
- manufactured with TEOS;
- has 250 nm of silicon thickness;
- channel width is 4µm, and length is 2µm.



(a)



(b)

Figure 5.9: Linear and logarithmic scaled IDVG graphs for both NMOS and PMOS p-TFT's in (a). p-TFT dId/dVgs curves for PMOS and NMOS in (b).

Table 5.2: p-TFT NMOS and PMOS characteristics.

Transistor type	Mobility (μ)	Subtheshold Swing (S)	Off-current	On-current	Threshold Voltage
NMOS	65.6 cm^2/Vs	300 mV/dec	7.3e-12	1.0e-5 A	0.6V
PMOS	14.8 cm^2/Vs	600 mV/dec	2.7e-11	2.7e-6 A	-2V

Id-Vgs
The Id-Vgs graph looks similar to the SG-TFT Id-Vgs. This can be observed from Figure 5.9(a). Especially the NMOS curves look alike, however, the PMOS curves of the p-TFT looks wider than the SG-TFT PMOS which could mean that the mobility and swing are worse than the SG-TFT PMOS. Again the same colours have been used for the types of transistor graphs: orange and red describe the NMOS transistor on logarithmic and linear scale respectively, and the dark blue and light blue curves describe the PMOS transistor also on logarithmic and linear scale respectively. The linear curves are kept on the same scale to compare the Id-Vgs graphs of the transistors on the same scale.

dId/dVgs
The dId/dVgs curves, shown in Figure 5.9(b), compared to the SG-TFT version of the curves look also very similar. Both of them however have a bit lower maximum than the SG-TFT transistors. The maximum value for the NMOS transistor is 3.4e-6, and for the PMOS transistor it's 7.7e-7.

Discussion on the obtained parameters
Table 5.2 represent the parameter values of the p-TFT transistors obtained from the Id-Vgs graph. These parameters are compared to the SG-TFT parameters from table 5.1. In the sense of speed of the transistors, the SG-TFT's are much faster and therefore of higher quality than the p-TFT's when focused only on the NMOS transistors. This is due to the lower Vds which will alter the function value. The on- off-current ratios of the NMOS transistors from both types are very similar.

The PMOS transistors of the p-TFT are of much poorer quality compared to the SG-TFT PMOS. The mobility is again much higher in the SG-TFT PMOS. The subthreshold voltage swing is much higher for the p-TFT PMOS which means that the transition from off to on-current and vice versa is much slower than the SG-TFT. The on- off-current ratio for the PMOS is much higher for the SG-TFT type than the p-TFT type. Threshold voltages are similar to the SG-TFT's where the PMOS transistors of both types of transistors are just outside the -1V to –V range.

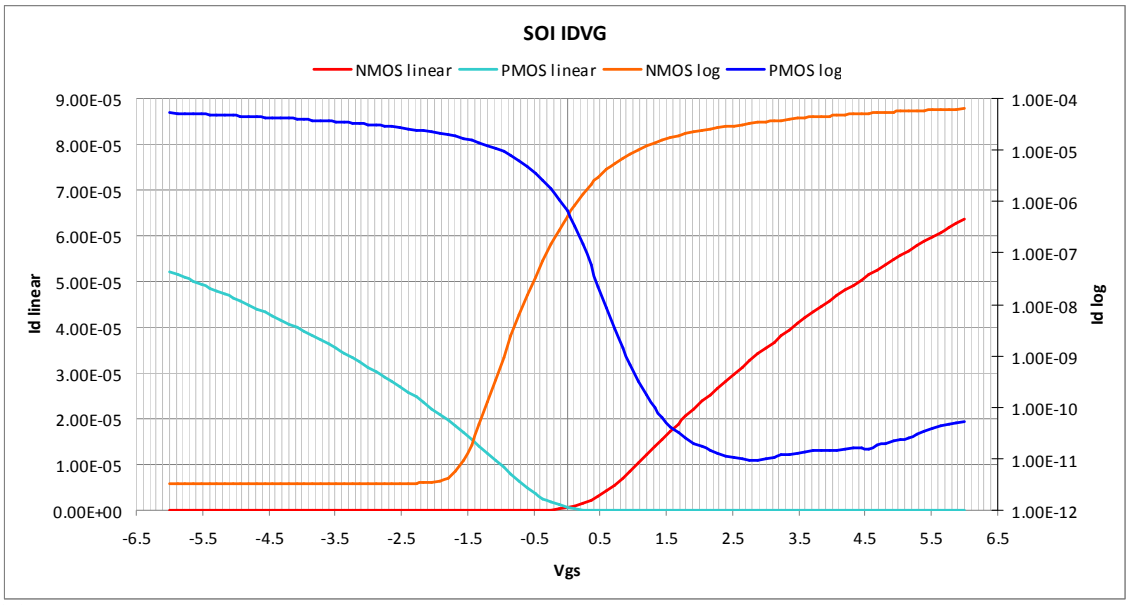
5.4 Measurement 3: SOI characteristics

Silicon-on-insulator (SOI) transistors are high quality single grain transistors. This can therefore be noted as the optimum version of SG-TFT's.

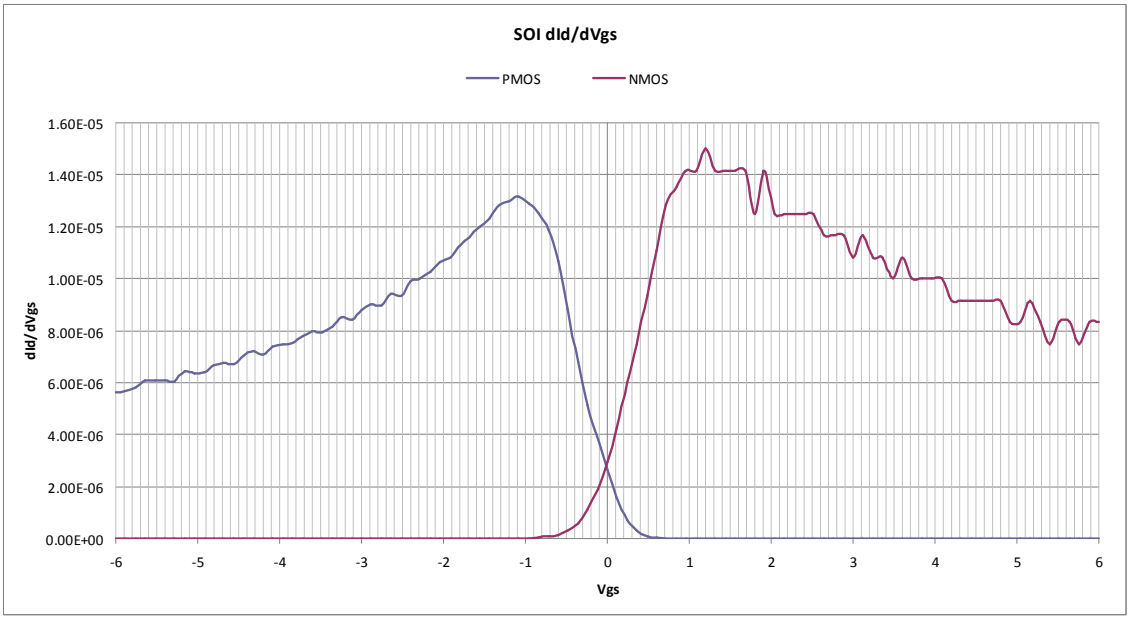
Difference in manufacturing process
This type of transistor is grown using thermal oxide on a pure silicon layer. The silicon layer is heated and by adding oxygen, a layer of silicon-dioxide is formed. The SG-TFT and p-TFT transistors used for the other measurements are made with TEOS (tetra-ethyl-ortho-silicate). TEOS is a liquid that reacts with oxygen. The resulting products are silicon-dioxide and ethanol[18]. The process with TEOS is cheaper however, it brings negative effects such as a hysteresis in the capacitance to voltage (CV) curve of the transistor [19].
Again the layout of this transistor was similar to the layout of the two other transistors we measured. The SOI transistors we used have the following features:

- a gate oxide thickness of 33nm;
- is grown
- has 350 nm of silicon layer thickness
- has a channel width and length of 4µm and 2µm respectively.

We measured with a Vds of 0.2V. Expected is a mobility ranging from 700 to 1000 cm^2/Vs [10]



(a)



(b)

Figure 5.10: Linear and logarithmic scaled IDVG graphs for both NMOS and PMOS SOI transistors in (a). SOI dId/dVgs curves for PMOS and NMOS in (b).

Table 5.3: SOI NMOS and PMOS characteristics.

Transistor type	Mobility (μ)	Subtheshold Swing (S)	Off-current	On-current	Threshold Voltage
NMOS	353.6 cm^2/Vs	300mV/dec	3.2e-12 A	6.4e-5 A	0.3V
PMOS	306.4 cm^2/Vs	300 mV/dec	9.2e-12 A	5.2e-5 A	-0.2V

Id-Vgs

Figure 5.10(a) shows the measurement results of the SOI transistors. Again, the orange and red lines define the same NMOS result only on a logarithmic and linear scale respectively. Similarly, the dark blue and light blue lines represent the logarithmic and linear results of the PMOS measurements respectively.

The Id-Vgs graph of the SOI transistors is quite symmetrical, only the PMOS has a slightly lower drain current than the NMOS, and while the off-current of the PMOS transistor is stable, the off-current of the NMOS increases for increased gate-source voltage. Since the linear scale hasn't been adjusted to fit the linear lines in all previous Id-Vgs graphs, it is clear that the SOI results show a lot higher drain current than the p-TFT or SG-TFT graphs.

dId/dVgs

The maximum value of the dId/dVgs graph isn't simply the top of a lump. As can be seen from Figure 5.10(b), the graph shows a peak and a slowly declining slope after the peak. This means that the mobility is still quite high when the gate-source voltage is set somewhere on this slope. High mobility for different gate-source voltages is a sign of a quality transistor. The peak of the NMOS is at 1.5e-5 and the PMOS at 1.3e-5.

Discussion on the obtained parameters

Comparing the transistor parameters shown in table 5.3 with the parameters of the SG-TFT transistors and the p-TFT transistors, it is clear that the mobility of the particular SOI transistor we measured has worse characteristics than the SG-TFT. However, theoretically the SOI should have a mobility ranging from 700 to 1000cm²/Vs [10]. So probably the quality of silicon in this transistor wasn't as good.

5.5 Conclusion

The Single Grain Thin-Film Transistor (SG-TFT) technology proves to be far better than p-Si Thin-Film Transistor (p-TFT). The SG-TFT has higher mobility, higher on-off-current ratio, and a lower swing.

Compared to the silicon-on-insulator (SOI) transistors, the SG-TFT has also a much higher quality when looked at every single parameter. However, we assume that this is because of the particular SOI transistor that we measured, since theoretically this type of transistor should have a mobility in the range of 700 to 1000 cm²/Vs.

The SG-TFT technology's quality is required for a better refresh rate of the Super E-paper, the possibility of stacking of the transistors for 3D integration of IC's so that all electronics are integrated behind the screen, and it's flexibility due to the low temperature manufacturing process. SOI's are manufactured in high temperature processes so that a plastic substrate can not be used.

6. Level shifter: Supply for the Super E-paper

In chapter 4 we have discussed that in order to drive the QR-LPD, a high voltage of 70V is required. However, low voltage digital circuits are used for controlling the pixels. A level shifter that converts 0 - 5V pulses to 0 - 70V pulses is required. When 70V is applied, the pixel turns into one colour, to convert the pixel to the opposite colour, -70 to 0V pulses may be used. On the other side, we could also simply switch the connection of the electrodes. Such a level shifter can be realized; by creating a circuit using MOSFET's that can withstand high voltage levels. Several circuits were designed before the optimal circuit was found. The primary requirement of our level shifter is for it to produce pulses of at least 35 volts.

In this chapter we will describe various designs of the level shifter, and the steps towards our optimization of this circuit. Section 6.1 will elaborate on our first design of the level shifter; section 6.2 will explain our slight modification to our basic level shifter. In section 6.3 we will describe our final level shifter that we used. Finally, a conclusion will be given in section 6.4.

6.1 Level shifter 1: Basic Design

For designing our level shifter circuit we used the circuit simulation software PSpice. Here we designed the level shifter based on the level shifter in [6] on p.32. This design made in PSpice is shown in Figure 6.1(a) and in Figure 6.1(b) the original design is shown. The basic working of this level shifter circuit is that a pulse is introduced to one of the NMOS gates and the same pulse passed through an inverter is put at the other NMOS gate. When the pulse is high, the first NMOS gate passes through its ground voltage to one of the outputs, which in turn is connected to the drain of one of the PMOS transistors and the gate of the other PMOS transistor, which passes through the high voltage to the other output as soon as the ground level reaches the PMOS gate. When the input pulse is low, the first NMOS opens, and the other NMOS closes giving the exact same effect only providing the ground voltage and high voltage to the opposite outputs. The methods of circuit design were explained in [20]

After designing this circuit, the simulation was compiled in PSpice to cross-check if the outcomes met the expected results. For this first level shifter circuit, we used:

- 2 high voltage NMOS transistors
- 2 high voltage PMOS transistors
- 74LS04 HEX-inverter
- Pulse generator for 0 to 5V pulses
- 70V DC voltage

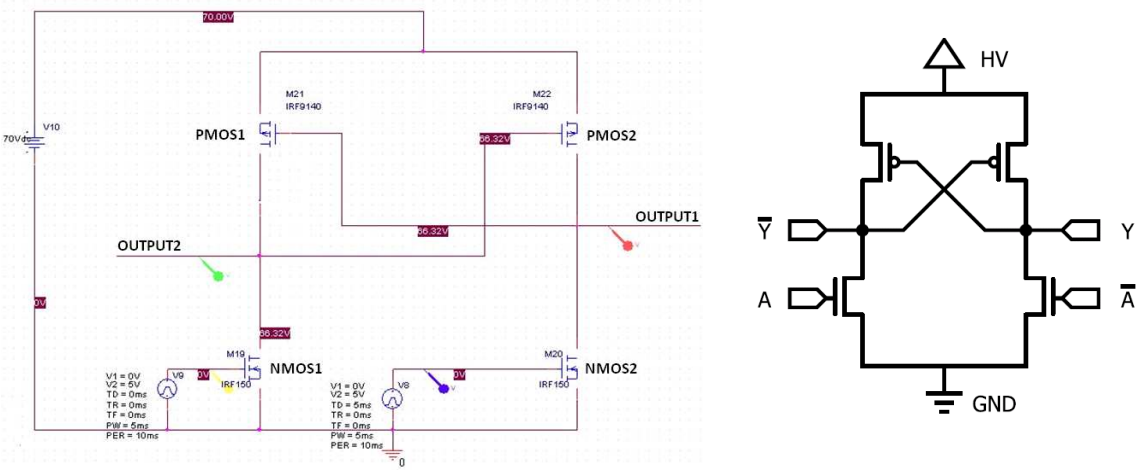


Figure 6.1: Level shifter design number 1: basic level shifter circuit designed in PSpice in (a) and the basic modelling scheme in (b) [6]

When we designed the circuit in PSPice, the supply voltage of the inverter was fixed at 3.5V, so the output of the inverter resulted in 3.5V when the input is low. To avoid this, we replaced the inverter with an extra pulse generator which is delayed for half the period time, giving the same result as a 5V supplied inverter. We also need to keep in mind that the transistors used in our simulation, are slightly different than the ones we used in practice. The PMOS used in the simulation is IRF9140, and the NMOS is IRF150.

6.1.1 Circuit Analysis

Situation 1: Pulse generator 1 = 0V, Pulse Generator 2 = 5V

The pulse generator (pulse 1) will give pulses of either 0 or 5V. When 0V is sent by pulse 1, 5V shall be sent by pulse generator 2 (pulse 2) and vice versa, because the second pulse generator is delayed for exactly half the period time. When pulse 1 sends a 0V pulse to the gate of NMOS1, the drain and the source aren't directly linked. Since the drain of NMOS1 is connected to OUTPUT2 and the source of NMOS1 to ground, at a high gate voltage, 0V would be seen at OUTPUT2.

In this first situation pulse 2 will therefore generate a 5V pulse at the same time when pulse 1 sends 0V. When this pulse arrives at the gate of NMOS2, this transistor shall be triggered to be conducting and shall pass the ground voltage (0V) from its source to its drain. As the drain of NMOS2 is connected to OUTPUT1, this output therefore in this case becomes 0V. The drain of NMOS2 is also connected to the drain of PMOS2 and the gate of PMOS1. As a PMOS will conduct for low signals, the 70V voltage, provided by the 70V source, shall be passed from PMOS1 source to its drain. As this drain is connected to OUTPUT2 this output shall receive 70V. This output is also connected to the drain of NMOS1 and the gate of PMOS2. A high voltage at the PMOS gate makes the drain and source of the PMOS not conducting. OUTPUT1 is 0V and OUTPUT2 is 70V: the 70V difference is realized.

Situation 2: Pulse generator 1 = 5V, Pulse Generator 2 = 0V

In this second situation pulse 1 will be sending 5V, and pulse 2 will generate 0V at the same time. As the NMOS1 shall be closed when receiving a 5V voltage at its gate, the ground voltage of 0V shall be passed from its source to its drain. As this drain is connected to OUTPUT2, it shall therefore have the same value as the drain; 0V. This node is also connected to the gate of PMOS2. Getting a 0V signal at the gate, would cause PMOS2 to be closed and therefore passing on the 70V signal from its source to its drain. As the drain is connected to OUTPUT1, an OUTPUT1 signal of 70V shall be realized.

At the same time pulse 2 shall generate a 0V pulse. As the output of pulse 2 is connected to the gate of NMOS2, a 0V signal would cause NMOS2 to be open and therefore not passing OUTPUT1 to the ground. OUTPUT1 is 70V and OUTPUT2 is 0V, exactly the opposite from situation 1.

6.1.2 Problem encountered: overloading

Our simulation on PSPice showed strange results, however since basically it should be functioning correctly, we assumed this might be due to the different transistors used, and the second pulse generator in stead of the usage of an inverter.

We decided to build the circuit in practice. For our actual circuit, we used PMOS IRF9540 and its dual NMOS IRF540 for the datasheets please refer to Appendices 4 and 5 respectively. The inverter we used was 74LS04 HEX-inverter. The supply voltages simulated were the same as the ones we used for this small test, however we could only use a maximum DC voltage source of 15V; for this first test this should be enough to check if it works.

Upon building the circuit and applying the 15V voltage, a constant overloading was observed. The overloading was caused by a direct link between the supply voltage of 15V and the ground. In our circuit two transistors were placed in these connections. The transistors and inverters have different threshold voltages, which could mean that somewhere in one period of the pulse generated, both transistors (PMOS1 and NMOS1 or PMOS2 and NMOS2) are conducting and the 15V supply voltage is linked to the ground causing the overloading.

6.2 Level shifter 2: Protective resistors added

Due to the different threshold voltages of the NMOS and PMOS transistors somewhere in one period of time, a short circuit takes place. This overloading phenomenon can be avoided by placing resistors in the circuit.

With regards to selecting appropriate resistors for this circuit, the following should be considered:

- The available resistors can withstand a maximum power of 0.25 W [21].
- The resistors should be able to handle high voltages up to and including 70V.

With keeping in mind the criteria as mentioned above, the magnitude of these resistors can be calculated by using Ohm's law. The power can be calculated by the following formula:

$$P = \frac{V^2}{R} \tag{6.1}$$

The required resistance for a high voltage of 70V with maximum power of 0.25W would therefore be $70^2/0.25$=19.6 kΩ. In the following designs the resistors have a value of 22 kΩ, this is done to keep an extra margin.

6.2.1 Circuit Design

Now that the value for the resistors is known, their ideal placement has to be found out. The resistors needed to be placed in the line from 15Vdc to the ground. The PMOS transistors need to have clear 0V to be switched on, so the resistor shouldn't be placed between the OUTPUT and the corresponding NMOS drains. So there are two places left for us to put the resistor or resistors: between the 15V voltage supply and the source of the PMOS transistors, or between the drain of the PMOS transistors and the OUTPUT's.

We designed the circuit in which we placed the resistors between the drain of the PMOS transistors and the outputs. Our simulation results seemed to be all fine as expected initially. The design of this circuit in PSpice can be observed in Figure 6.2(a), the circuit is shown in Figure 6.2(b) and its simulation in Figure 6.3. We could have placed one single resistor between the source voltage and the drains, but the reason we didn't do this, was that a small percentage of voltage will be applied on the resistor. We can put our output connections, if we would use our two-resistor design, above the resistors, to take the full voltage of the resistor including the opened NMOS transistor.

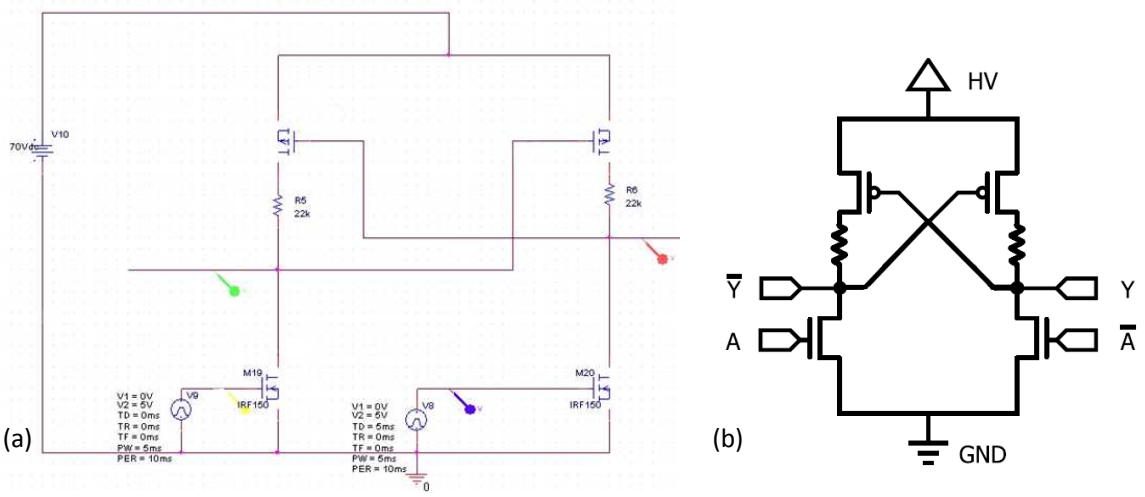


Figure 6.2: Level shifter design number 2: resistors placed to prevent overloading, in PSpice in (a) and the basic modelling scheme in (b)

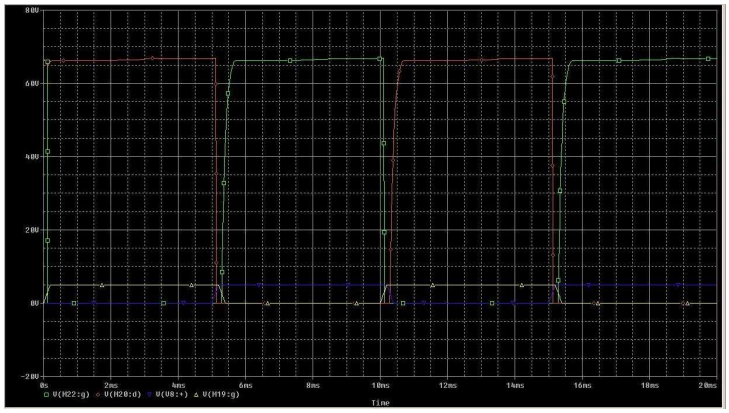
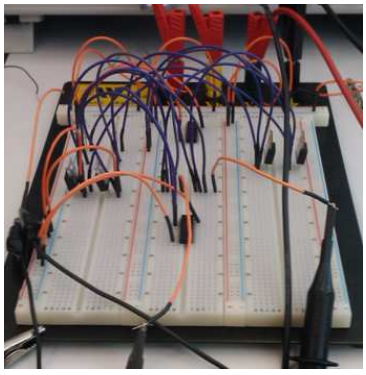


Figure 6.3: Simulation result of level shifter design number 2

The colours of the graphs in Figure 6.3 can be related to the coloured pins in Figure 6.2. Therefore the red graph shows the output1, the green graph shows output2, the yellow graph indicates the pulses of pulse generator 1 and the purple graph depicts the same pulses but then delayed by 5ms coming from pulse generator 2.

6.2.2 Problem encountered: maximum PMOS gate-source voltage

After the successful simulation results, this circuit was built on a breadboard. Figure 6.5a shows an image of this circuit.

(a) 

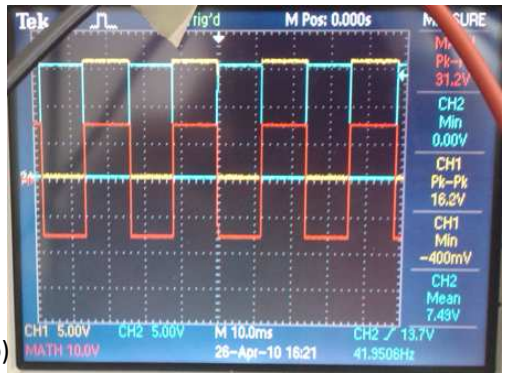
(b) 

Figure 6.4: Realization of our second level shifter circuit, showing the circuit built in (a), and the outputs on the oscilloscope screen in (b)

Once this circuit was built on a breadboard as shown in Figure 6.4(a), all elements were manually one by one tested to ensure the proper construction of the circuit. As can be seen in Figure 6.4b, the outputs were indeed meeting the expectations, the blue line shows OUTPUT1, and the yellow line shows OUTPUT2. When the two outputs are connected with respect to each other, the latter output is subtracted from the first, and the total output can be seen in the figure as a red line. Notice, that the volts per division for the red line are twice as large as those for the blue and yellow lines.

After the successful testing with 15V, a high voltage of 70V was applied to the circuit. Initially all seemed to work fine, however after continuously applying this high voltage for several minutes, the transistors started heating up after which they broke. After analyzing this unforeseen happening, it turned out that the PMOS transistors had a maximum gate source voltage (Vgs) of 20V as can be seen from its Appendix 2. As when applying 70V to the sources of the PMOS transistors, when 0V were passed from the NMOS source to the NMOS drain, following to the PMOS gate; a Vgs of -70V was realized, the breaking of the transistors was obvious and clarified.

6.3 Level shifter 3: Breakdown Vgs avoided

Following the successful simulation of the circuit in PSpice, but the unsuccessful results once building the circuit and applying high voltages, a new circuit had to be designed. This circuit unlike the previous ones should avoid the 70Vgs of the PMOS transistors. With the help of PhD N. Saputra, we designed another level shifter. Figure 6.5(a) shows the PSpice schematic of this circuit, and in Figure 6.5(b) the original schematic is provided.

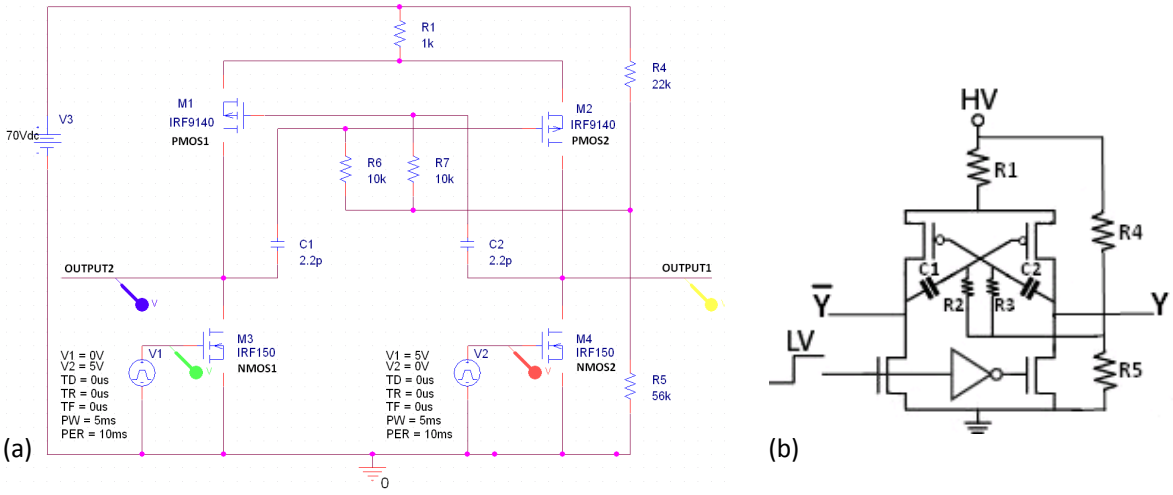


Figure 6.5: Level shifter design circuit 3: avoiding high PMOS Vgs in PSpice in (a), and the original modelling scheme in of N. Saputra (b)

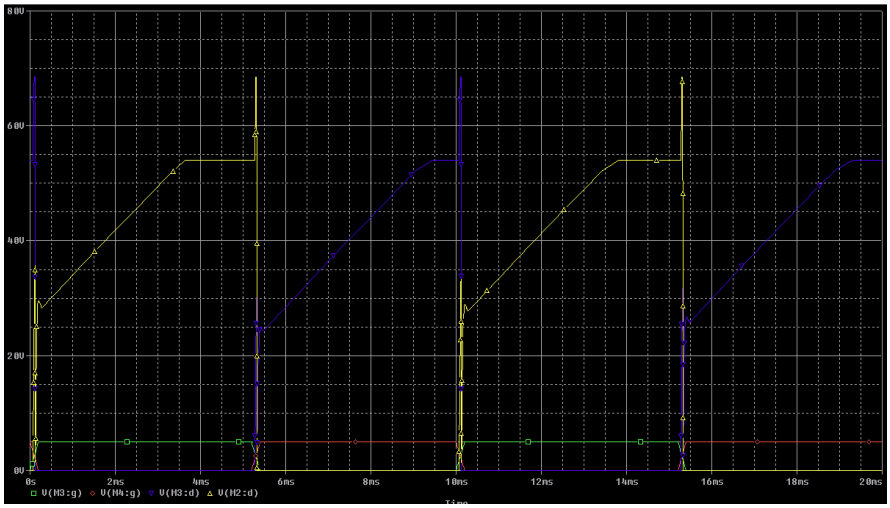


Figure 6.6: Simulation result of level shifter design number 3

6.3.1 Circuit Analysis

The resistor and capacitor placement and values need to be explained by using Figure 6.5(b). First, to avoid repeating the same mistake, R1 is placed right after the 70V supply to avoid overloading, since again the PMOS and NMOS transistors are the only components between the source voltage and ground apart from resistor R1. This resistor has been set to the value of 1kOhms. In this circuit we would like to send a constant voltage to both the PMOS gates. For simplicity of using the circuit, the resistors R4 and R5 form together a pod meter. Between the two PMOS gates, two resistors are used so that the PMOS gates aren't directly linked to each other. In this case both resistors have the same value because the same type of PMOS is used. We take for our circuit 10kOhms resistors. The capacitors are used to switch the PMOS gates and are chosen to be as low as possible so that the RC-time is short. The simulation result of the third level shifter is shown in Figure 6.6.

Situation1: pulse1 = 0V, pulse 2 = 5V

The closing and opening of an NMOS can be modelled as a switch. We assume in this analysis that the pod meter is adjusted in such a way that it provides 50V DC voltage. We can analyze the design from Figure 6.6 differently as in Figure 6.7.

When 50V is delivered by the pod meter, this 50V passes to the gate of both PMOS transistors. Both will therefore close at first. However, since the drain of PMOS1 is connected to the ground because of the NMOS, the value of OUT1 stays at 0V. PMOS2 has now a drain of HV which is 70V. This 70V pushes the top value of the capacitor up to HV+50V which opens PMOS1 so that no HV is led to the ground. OUT2 is equal to HV and OUT1 is equal to 0V. A difference of 70V is realized.

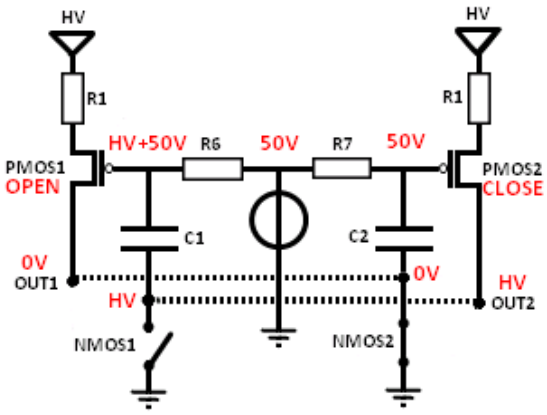


Figure 6.7: Levelshifter 3 analyzed from a different perspective, situation1: pulse1 = 0V, pulse2 = 5V, corresponding to NMOS switching

Situation2: pulse1 = 5V, pulse 2 = 0V

When both NMOS transistors switch, the outputs should switch as well. Figure 6.8, explains this second situation. Again the pod meter gives 50V. But, now that NMOS1 is closed, 0V is passed to OUT2 and the HV+50V on the capacitor goes to 50V. The rate at which it diminishes is dependent on the RC value, so the value of R6 and C1 multiplied with each other give the time constant. As soon as HV+50 reaches a value that crosses the threshold voltage of PMOS1, the HV is passed to OUT1, which in return causes C2 to rise the voltage to HV+50V and open PMOS2. Both output values are now switched.

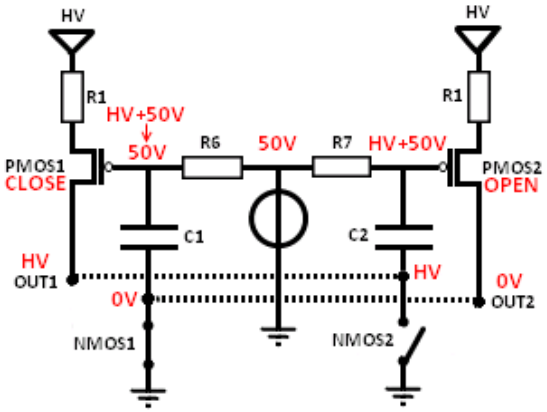


Figure 6.8: Levelshifter 3 analyzed from a different perspective, situation2: pulse1 = 5V, pulse2 = 0V, corresponding to NMOS switching

6.4 Conclusion

In this chapter we have analysed three types of level shifters. The first type has been replaced by the second due to overloading. The threshold voltages of the PMOS and NMOS transistors used are not the same, so there will be a moment that a direct link between high voltage and ground is made. To prevent this, a resistor has been introduced in the line of the link.

The second level shifter has been used for most of the measurements for the next chapter. However, near the end, the circuit did break down, and we did notice that we couldn't keep the circuit active for a longer period of time. This was due to the high gate-source voltage applied at the PMOS transistor.

Finally, the third transistor has been designed to pass this problem. The gradual decrease from HV+50V to 50V causes a gradual closing of the PMOS. This should happen as fast as possible. The simulation with PSpice and in practice both show a gradual increase of the output from approximately 30V. The threshold voltage of the particles in the Quick-Response Liquid Powder Display (QR-LPD) that we will be using is 35V. So as long as the pulses go higher than 35 volts we should have some effect on the display. Although, according to the hysteresis curve discussed in section 4.2, the screen will turn to its full colour when either 70V or -70V is reached. The effect by using this level shifter will therefore be less than when using a level shifter that brings full 70V pulses. However, the primary requirement of producing pulses of at least 35V is met.

7. Active Matrix measurements with Bridgestone's E-paper

Pixels need to be activated by putting a voltage difference between the electrodes with particles in between them. There are various ways to do this, but when specific pixels need to be accessed, specific circuitry is needed. When these pixels are activated, research is possible by applying different types of input voltages and analyzing which type gives the most change of colour in the pixels. The theory used for this chapter is mainly from [6].

In this chapter we will analyse Bridgestone's E-paper front plane on TU Delft's E-paper backplane which represents the Super E-paper. For our measurements we use a wafer that is not flexible since the substrate is silicon. The final product however, will have a flexible plastic substrate. We will first explain how active matrix addressing works in section 7.1. Then in section 7.2 we will describe the layout of the wafer that is used to drive Bridgestone's E-paper front plane. In section 7.3 we will discuss our measurement results and the problems that have occurred. Finally in section 7.4 an in depth conclusion is made about these measurements.

7.1 Active Matrix addressing

There are two common ways of addressing pixels: Active Matrix and Passive Matrix.
Passive Matrix addressing is in short the activation of pixels through direct row and column lines, more of this will be discussed in the next chapter.

Active Matrix addressing is a pixel addressing method that uses transistors for switching each pixel. An example of this is shown in Figure 7.1. The figure shows a situation where one transistor controls the activation of the corresponding pixel. The column data voltage will only activate the pixels which have their transistors conducting the voltage to the top electrode of the pixel. The non-activated pixels should be completely isolated when other pixels are changing. The capacitor within every pixel ensures its robustness and helps against noise. Active Matrix addressing is also much faster than Passive Matrix addressing, making it possible to reach higher frame rates.

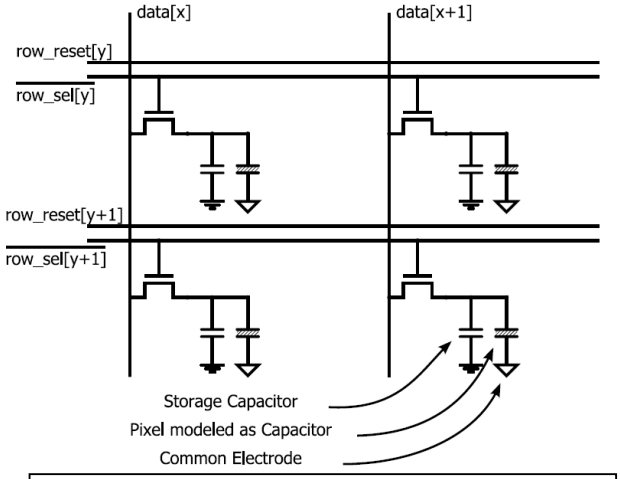


Figure 7.1: Example of an active matrix addressing scheme with 4 pixels [6]

The Super E-paper that we will be testing on uses Active Matrix addressing because of its robustness and speed.

7.2 Layout of the wafer

For active matrix addressing, every pixel of the E-paper screen has a circuit driving it. A pixel must be manipulated by giving a voltage difference between the electrode running under the pixel, and the common electrode which is stuck on top of the pixel. However, in this case it would be difficult to address individual pixels. With the use of transistors that can be switched on or off, individual pixels can be addressed.

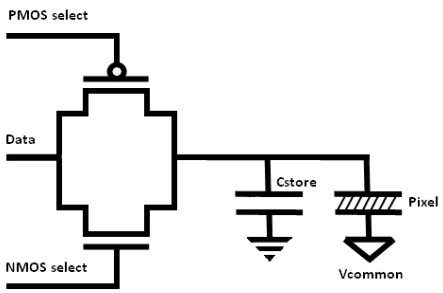


Figure 7.2: circuit for driving a single pixel

Behind every single pixel, the scheme as shown in Figure 7.2 is set to drive it. The pixel is modelled as a

capacitor, since the pixel basically consists of two electrodes with air and particles in between them. The data is passed through to the top electrode in the figure when both PMOS select is 0V and NMOS select is 70V. The transistors used in this circuit are HV SG-TFT's, and are capable of withstanding such high voltages. The common electrode can have either 0V or 70V, depending on the desired colour. A PMOS can pass through a stronger HV, and the NMOS can pass through a stronger 0, together they form a Transmission-Gate [17]. In section 7.2 we will discuss why a different scheme is more useful. For our research however we used this driving scheme.

While the scheme in Figure 7.1 shows how the E-paper is modelled on paper. The wafer we used had some different orientation. For our active matrix measurements we used the wafer which is a silicon substrate; Super E-paper will eventually be produced on a flexible plastic substrate. The first thing that one has to keep in mind with these measurements, is that the Vcommon as shown in Figure 7.1 is the rectangular shaped piece that is positioned on the centre of the wafer, as shown in Figure 7.3(a). The diameter of the wafer is four inches. The Vcommon electrode is an Indium Tin Oxide (ITO) plane and is not only conductive but also optically transparent. The Vcommon connectors shown in the same figure are copper tapes sticking from underneath the top plastic layer to access the Vcommon electrode. The figure also shows that the Vcommon electrode is transparent, making the pixels visible. Underneath this E-paper layer we have the driving circuitry that can activate the pixels: the E-paper backplane. These two technologies together form the Super E-paper. A cross-section of the common electrode area is shown in Figure 7.3(b). The top layer of the wafer isn't conducting with the bottom layer or the chuck. So that the electric field between common electrode and wafer electrode is bigger than the wafer electrode and chuck. The paper placed between the cupper tape and wafer isolates the voltage from each other.

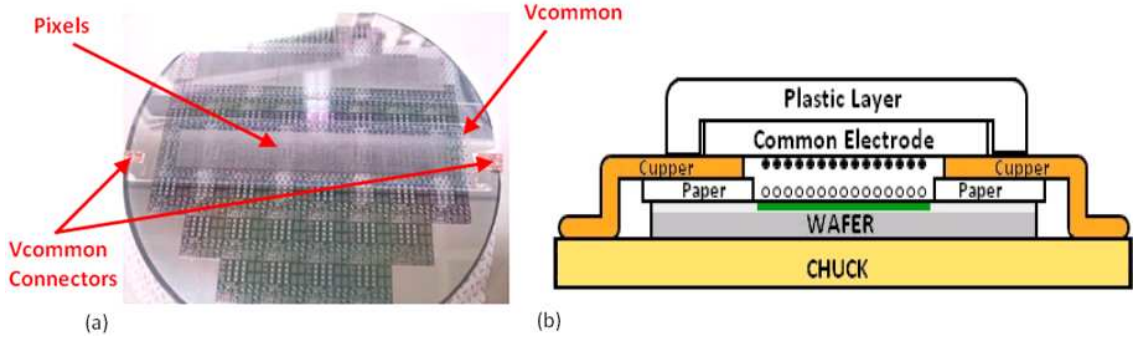


Figure 7.3: Picture of the Super E-paper used for our research in (a) and a schematic cross-section sketch of the wafer with the different layers of material place on a chuck in (b)

Figure 7.2 showed the driving circuit for driving a single pixel. Naturally, these circuits aren't simply put next to each other on the wafer. The lines for selecting the PMOS and NMOS pair, and the data lines need to be accessed in some way, since measurement pins can not go through the plastic, pixel, and particles to activate the specific lines. These lines are pulled up for access and can not be crossed since they are on the same metallic level. The complete matrix of pixels can not be activated all at once with this particular circuit layout on the wafer. On the wafer, matrices of 25 circuits of Figure 7.2 are built on the wafer. The idea is that every cell (electrode driven by the circuit from Figure 7.2) on the layout covers a single pixel, so that the pixel is activated only when that particular combination of data line, NMOS select and PMOS select is activated. This cell has a length and width of 125micron[1]. A part of the layout design of the wafer for activating the pixels is shown in Figure 7.4. The cell in the figure contains the bottom electrode, and when this cell is covered with the pixel and the common electrode on top, we should have a functioning pixel driver.

1. micron = micrometer

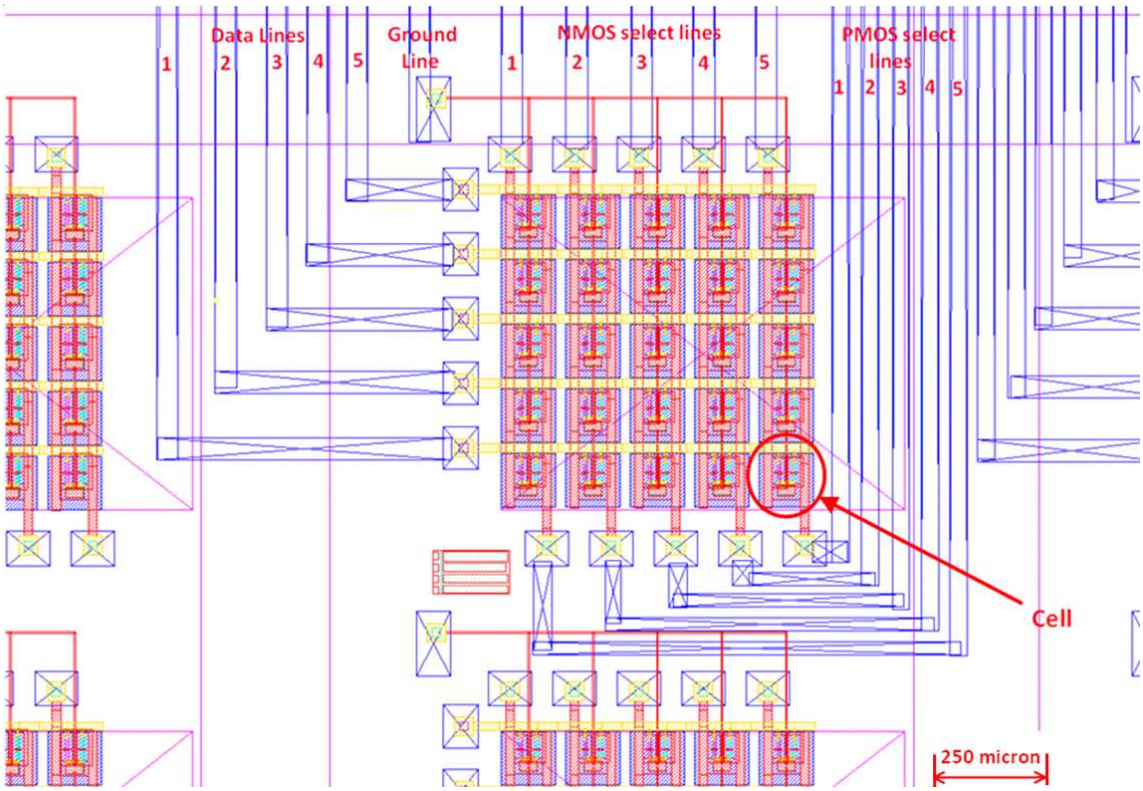


Figure 7.4: The design of the layout of the Super E-paper backplane

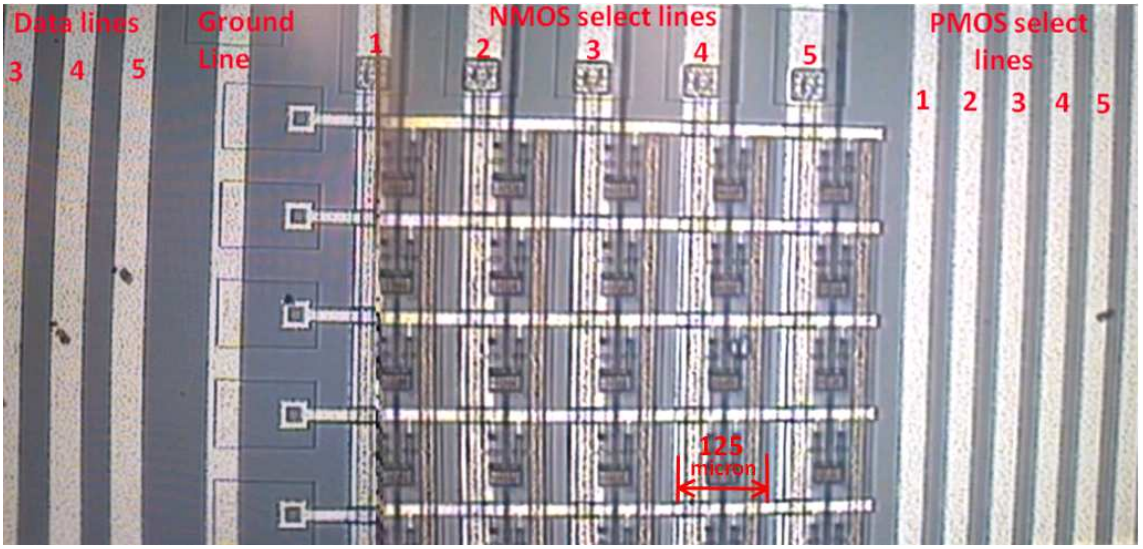


Figure 7.5: The picture of the layout that was taken from the image visible under the microscope. The picture was taken on a matrix of cells that was situated above the pixel area.

As shown in Figure 7.4, five data lines, five NMOS select lines, five PMOS select lines and one ground line are needed for driving a matrix of 25 pixels. For a much bigger matrix, a lot more lines are needed. For testing purposes, the matrix of 25 cells will suffice. In the same figure, other matrices below, above, and next to this matrix are shown, but not all of them are connected to the lines. The matrix of cells needs to be put underneath the pixels in order for them to drive the pixels. Creating more data lines for multiple matrices will make it more complicated to look for the right matrix of cells, or matrix of pixels that are being driven. Therefore, even though multiple matrices of cells are

manufactured, only the matrices that are positioned in the horizontal centre (underneath the pixels) are connected to the relevant lines. In Figure 7.5 a matrix of cells is shown that is positioned above the pixels. Notice that the data lines are not connected to the cells and that the NMOS lines are running through the cells. Eventually when the right matrix is reached a layout similar to Figure 7.4 is realized. When the right matrices are found, we are able to manipulate the 25 pixels that are driven by the corresponding 25 cells, and pixel changes can be analyzed.

7.3 Measurement analysis and discussion

The previous research on Super E-paper used a supply voltage of 70Vdc on the data line and 0V on the common electrode. Changes were identified; however, these changes weren't visible for the naked eye. The changes identified were not as big as hoped for. When contacting Bridgestone, they advised us to use a 70V pulse at first, for at least a 1000 pulses on the data line. The idea here is that the pulses trigger more and more particles, and chances of the desired particles breaking through a bundle of oppositely charged particles are bigger.

We have built a level shifter capable of sending these high voltage pulses. The circuit is capable of running on 500Hz, which means that for 1000 pulses we would only have to wait 2 seconds. We found the data lines, NMOS lines, PMOS lines and ground line and we followed the lines to the pixels trying to look for the matrix of pixels that are being driven by those lines. We will discuss some problems we have encountered during our research and the measures we have taken.

We started our measurements first by finding the matrix of pixels that are driven behind the pixels. After that we measured a vertical array of pixels using the data lines running to the driven matrix. Our third measurement used changes observed under the microscope to analyze the change in pixels and to observe which parameter causes how much change. We first tried to switch the source on and off multiple times to see if this had any effect on the movement in pixels. Then we looked at the frequency, duty cycle, and amplitude of the supply voltage to conclude the optimum driving method of the Super E-paper. We could also analyse the refresh rate of a grain moving from one electrode to the other. We will discuss problems encountered, measurements and the results of each measurement in this section.

Problem 1: Used pixels

Before our research, other researchers such as W. Chim and A. Baiano, tested the Super E-paper 2 years ago. Pixels got scrambled during this research, and while the pixels were rather clear in the past, the pixels we had to test had a lot of particles that got dropped to the level of the lines, or pulled up to the common electrode. As the circuitry is placed behind the pixels, it was very difficult for us to identify the matrix of cells driving a matrix of pixels. Figure 7.6 shows a microscopic picture of the pixels. Notice the grains covering the bigger part of the circuitry.

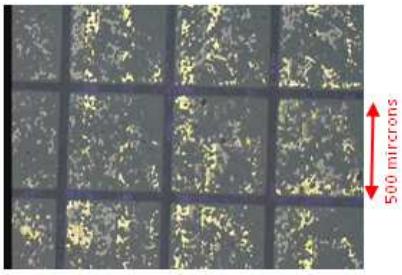


Figure 7.6: Microscopic picture of the pixels of the Super E-paper

Problem 2: Cell size vs. Pixel size

The circuits were built for each cell to drive a single pixel. However, the size of the pixels delivered by Bridgestone was approximately four times bigger than the size of a cell. This would mean that multiple cells should be activated in order to drive a single pixel. Identifying a change in the matrix of 25 pixels compared to the rest of the pixels was difficult as it was. Now, because of the bigger pixel size, a much smaller matrix of pixels can be driven. With the size of the pixels being 500µm, visible changes are still difficult to identify.

Problem 3: Lines running to the circuit under the pixels

Identifying the matrix of cells that are activated shouldn't be that difficult when all the cells are activated at once, and only in that area changes occur. When looking for changes, the cells can then be easily found. The next problem is the lines running to the cells. These lines are metallic and have a certain voltage with respect to the common electrode; in particular the data lines have the exact same voltage as the activated cells that form the bottom electrode. These data lines will also attract and repulse particles, so changes also occur in the pixels covering the data lines. Also the NMOS lines have a DC voltage of 70V, so minor changes will occur in the pixels covering those lines.

Problem 4: PMOS select are always active

When the data value needs to pass through the transmission-gate, either one of the transistors is active, or both of them are active. A PMOS is conducting when no voltage is applied at the gate with respect to the source. This would mean that in default, all PMOS transistors are conducting. To avoid this, the PMOS lines that need to be inactive, should have a voltage applied that switches these transistors off. However the machines we are using only has 4 measuring pins that can apply voltage; this makes it impossible to select specific columns from a matrix of cells.

7.3.1 Measurements 1: Finding the matrix of pixels that are driven

For our research we have used CASCADE31 which is connected to the Parameter Analyser. These machines can be observed in Appendix 7. Figure 7.7 shows the schematic representation of the measurement arrangements. Since CASCADE31 has 4 measurement pins, we can use 3 of them as SMU's. We can use the cupper tape which is connected to the common electrode, and stick this to the chuck of the machine holding the wafer. The chuck is again connected to the parameter analyzer and forms the 4th SMU. The remaining pin can be used as Voltage Source Unit. The Parameter Analyzer can not send a pulse of 70V, so from this machine we need to send one SMU output to the 70Vdc supply of our level shifter circuit. This level shifter circuit sends the 70V pulse to one of the pins of CASCADE 31. We made contact with this pin to the data line 5. We connected the remaining pins to NMOS select 1, PMOS select 5 and GND. The voltages applied were: a pulse of 70V to the data line, 70Vdc to NMOS select, 0V to PMOS select and 0V to GND. The frequency used for the level shifter was 500Hz. Since we only have 4 SMU's to work with, activating all the cells at once is impossible

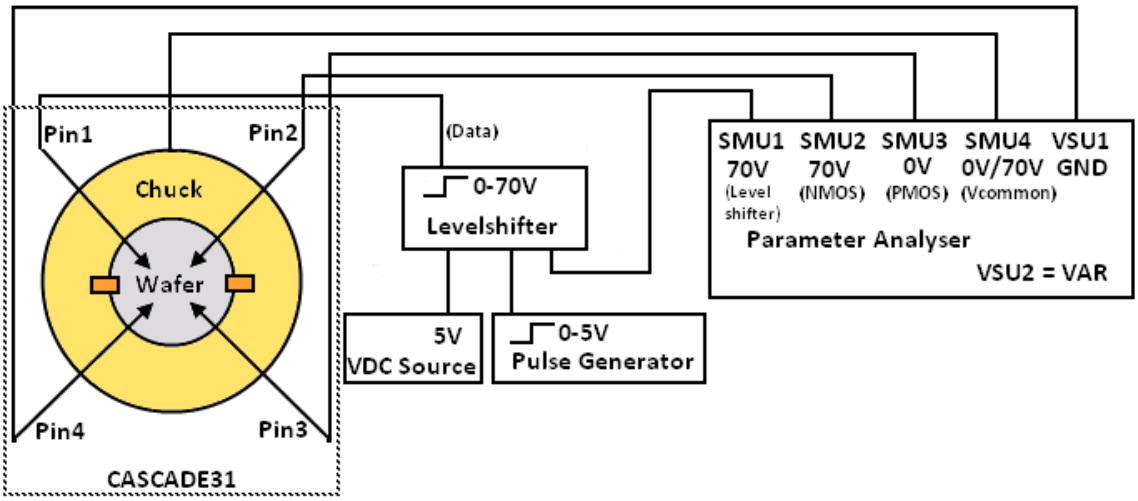


Figure 7.7: The measurement model of the connections between the machines used.

Result of measurements 1: Finding the matrix of pixels that are driven
As we expected, not only a matrix of a group of pixels (less than 25 because of the smaller cell size), changed, but also all the pixels where lines from data and NMOS select were running through changed. Every time a single cell is driven, multiple pixels showed changes. Also, changes were too little; the exact area of the cells can not be specified. However, since the pixels with data lines changed also, we can test these for our research on the optimum driving method.

Problem 4: Data lines cover only part of the pixel
Data lines used for driving the pixel are in total covering about 40% of the total area in the pixel. Changes of the pixel due to the data lines are therefore at most about 40% of the pixel. Of course, changes may be observed in a small area surrounding the data lines. But, basically only part of the pixel can be driven in this way. One might wonder how much change can be observed by the naked eye if only 40% of the pixel can be changed at most. This can only be observed if the change is big enough.

7.3.2 Measurements 2: Activating a vertical array of pixels with data lines
When we simply ignore the PMOS and NMOS Lines, we can focus solely on the changes occurring due to the vertically running data lines that are running underneath an array of vertically positioned pixels. One pixel has two or three data lines running through it. We wanted to put the data line on all five lines one by one so that when we take out the wafer, we will see a thin black or white line running vertically through the E-paper. Under the microscope a large area of the pixels were observed, and on the computer monitor a matrix of about 9 pixels were monitored, including the pixels where the line is running underneath. After checking the wafer we put 70V on the chuck to get white coloured pixels.

Result of measurement 2: Activating a vertical array of pixels with data lines
Each time a data line was activated, only minor changes were noticeable under the microscope. We tried waiting for a longer time period but this had very little effect. When we took out the wafer, it was very difficult to find the two columns of pixels that were activated. This was due to the little change we noticed under the microscope and because only 2 pixels were partly manipulated.

When the chuck was brought to 70V we could notice again some minor changes, but again after looking at the wafer with the naked eye we couldn't observe any significant changes.

Problem 5: Black and white particles under the microscope
Under the microscope both black and white particles are seen as black dots, this is due to the light emission of the microscope itself, which causes the shadow of the particles to be reflected on the wafer. This makes it difficult to find out what triggers which colour particles most. Also, we do not know for sure if changes we see under the microscope are the relevant particles being attracted, the opposite particles being deflected, or simply a rearrangement of the particles.

7.3.3 Measurements 3: Use microscopic changes for research
Even though, we didn't find any visible changes for the naked eye. We could observe some changes under the microscope. We can use this to test different variables to see which variable causes the most change in a pixel. First we will turn the system on multiple times to check on transient behaviour. Afterwards, we will try 5 different frequencies at first: 30Hz, 50Hz, 500Hz and 1kHz. Then we will try 5 different duty cycles: minimum duty cycle, duty cycle of approximately 25%, duty cycle of 50%, duty cycle of approximately 75%, and DC voltage. Finally we will try to increase the amplitude to such an extent that no more changes in the pixels can be observed. For every experiment we will try both the situation where black particles are attracted to the common electrode as well as when the white particles are, and we will also put the pulse on the common electrode, so that in total we will have four different connection arrangements as shown in Figure 7.8.

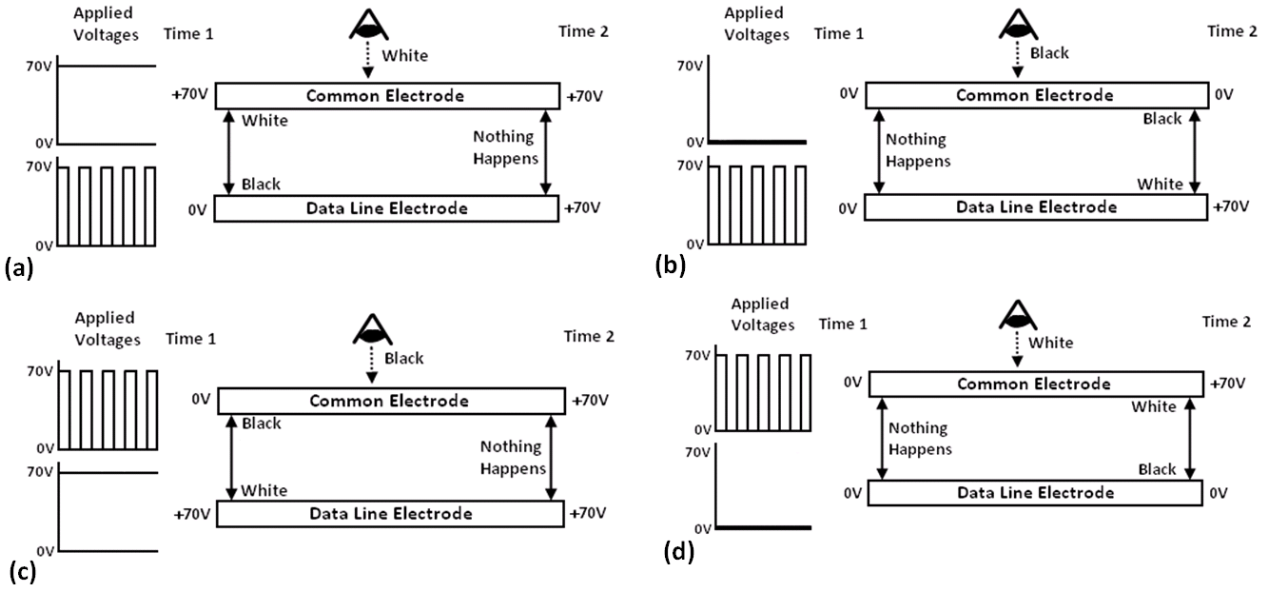


Figure 7.8: Four different connection arrangements. In (a) 70V DC is applied to the common electrode, and the 70V pulse is applied to the data line electrode. (b) Has the same arrangement as (a) but the common electrode is supplied with 0V. The two connections are switched in (c), and 70V DC is applied to the bottom electrode. Finally, (d) is similar to (c), but the DC voltage at the bottom electrode is set to 0V.

Result of measurement 3.1: transient behaviour

We started actually with the transient behaviour of the Super E-paper; Figure 7.9 shows an example of a transient behaviour. For this test we used a frequency of 500Hz, a data supply of 70V pulses, and 50% duty cycle. We switched the data line on, waited a few seconds, switched it off, waited another few seconds, and repeated this sequence until we couldn't observe any changes in the pixel under both the microscope and the monitor.

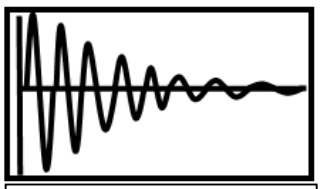


Figure 7.9: Example of typical transient

With the first activation, there were only little changes, approximately 3 grains per array as shown in Figure 7.10. Then when we waited a few seconds and activated the data line again, we saw 1 or 2 more grains moving. We repeated this test for with 3 different lines and all had approximately the same result.

After our first test, we wanted to know what would happen if we would wait a longer period of time between the multiple switching. So we waited 5 minutes between the switching; minor changes were noticed, and we switched it off after a few seconds of no change on the pixel. We repeated this test three times on the same data line; minor changes of about 2 grains occurred.

It is too fast to conclude that these results prove that more changes occur when voltage is switched on at the data line, since changes were very little. Of course, Bridgestone did mention that the Super E-paper front plane would need at least 1000 pulses, so we can only assume that the particles have effect on transient situations. The little changes we observed could also be the result of rearrangement on the common electrode, which can't be proven because of the dark appearance of both coloured grains under the microscope. Another point is that we are giving pulses of 70V and not a 70Vdc voltage. So basically we are switching a voltage of 70V on and off at relatively high speeds; if the particles are affected by their transient behaviour they should be moving for a while after voltage is applied, but shouldn't move again if voltage is switched on and off after the changes have stopped. Since movement did take place after waiting a short while before turning the voltage back on, we can assume that the frequency we used was too high for the particles to break through oppositely charged particles or to be fully attracted to the electrode. But again changes were too little to conclude anything from this test.

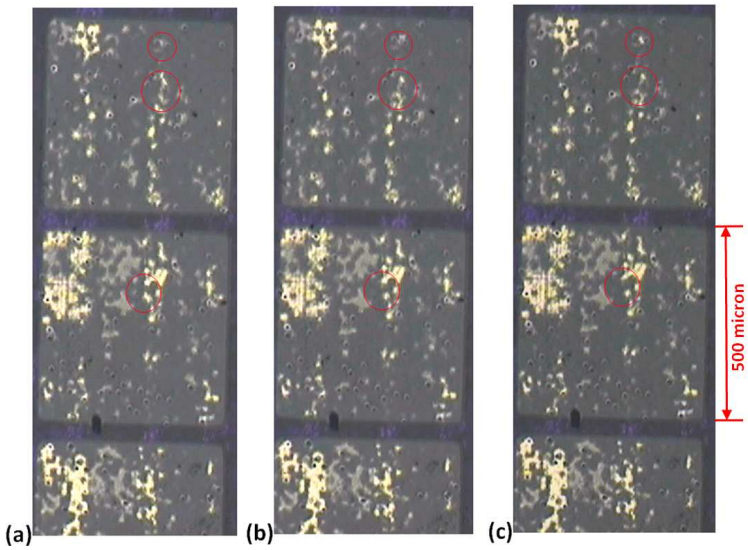


Figure 7.10: changes observed in array of pixels during the multiple attempt test; from (a) to (b) the first attempt is observed, and from (b) to (c) the second

Result of measurement 3.2: frequency dependency

Our next step was to see at which frequency the pixels were experiencing the most change; Figure 7.11 shows an example of pulse frequencies. Again the data supply was 70V pulses, and we had 50% duty cycle. This time we waited after switching the data voltage on for 20 seconds per frequency, this should meet the requirements of Bridgestone (1000pulses). We tested all the frequencies on three data lines. Again the changes were carefully monitored under the microscope, and on the monitor of the pc.

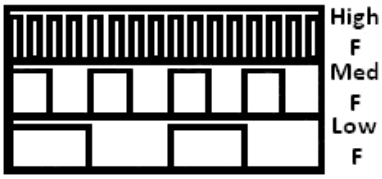


Figure 7.11: Example of various frequency pulses

For every frequency we would find approximately the same amount of minor changes in the pixel. These changes were too little to conclude that a definite frequency was optimal for driving the Super E-paper. We weren't able to test with much higher frequencies because of the inverter specifications in the level shifter as described in Appendix 7. Again the changes might be due to rearrangement or attraction. It is also unfortunate that we can't reset all the changes per frequency, to reference the changes with regards to one common state for all the frequencies.

Result of measurement 3.3: duty cycle dependency

We manipulated duty cycles from almost 0% to almost 100%. Figure 7.12 shows an example of these various duty cycles. We set the frequency of the pulse to 500Hz again and the data line voltage amplitude to 70V. We expected that since 100% duty cycle would be the same as DC voltage, that the change at 100% duty cycle would be less than the change with a lower duty cycle percentage. On the other side when 0% duty cycle is applied, the supply would be similar to no supply voltage whatsoever, so again low expectations for this very low duty cycle. We started with a duty cycle of 50%, and by changing the duty cycle when no changes were visible anymore, we could find out at which percentage movement of the particles still take place.

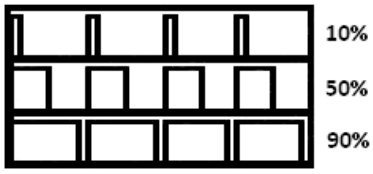


Figure 7.12: Example of various duty cycles

Changes were again minor, and nothing could be concluded. Sometimes changes occurred, sometimes they didn't, this could have various reasons, and again it's a pity that we don't have a common reference situation to test the duty cycles independently.

Result of measurement 3.4: pulse amplitude

Finally we applied a higher pulse voltage than the theoretical 70V. An example of different amplitude pulses is shown in Figure 7.13. As we have discussed in chapter 5, particles move from the moment that the threshold voltage is applied, the higher the voltage difference between the electrodes from this point, the more the particles get attracted and repulsed. In this sense, maximum change will occur when a voltage of 70V is applied. We expect that when we apply a higher voltage, the change will be more rapid and bigger. For our final test we wanted to apply voltages of 70V, 80V, 90V, and 100V, but we wanted primarily to know if there was any noticeable influence at all. So we brought the supply voltage up to 100V to see if the change is really significant, if so, we can do the other tests again while using the 100V supply voltage.

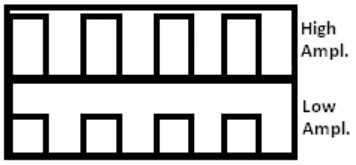


Figure 7.13: Example of high and low amplitude pulses

The changes were minimal, change increased by approximately 3 grains. Again this might be due to the coincidental situation we had, but after applying the 100V a multiple times on different data lines, it is very difficult to conclude that the 100V makes a difference at all.

Problem 6: Too little changes

The changes that we observe are far too little to be able to make definite conclusions on the effect of different parameters we used, as we can see in Figure 7.10. This is partly because the colour particles can not be observed under the microscope so that the difference between rearrangement of particles and the attracting and repulsing of particles can't be observed. Another reason is that, because there is no common "reset" to test the change in a particle with the exact same conditions when a variable is changed. The most important restriction is that simply the change of pixels is very little. Other tests with minimum changes can be observed in Appendix

Problem 7: Impossible to calculate the refresh rate

When calculating the refresh rate, one would have to observe a grain in a pixel that is attracted by the common electrode. The refresh rate could have been calculated when filming the grain movements. The time is taken from the moment that a transparent area turns slightly grey, until it turns all the way black. This would cause however two problems: the first one is that the starting point and the ending point of timing such a movement is very objective, the slightest miss-observation could easily make a huge difference for the theoretically obtainable refresh rate of 0.2 ms.

The second problem is that particles are moving from different grey scale levels, and are also moving horizontally for reorganization as stated in problem 6.

Remarkable observations

During our research we tried switching the connections between the chuck which was connected to the common electrode, and with the data line. We noticed that when the applied voltages of the parameter analyser are switched on movement in the pixels occurs, but sometimes movement also occurs the moment the voltages are switched off as shown in Figure 7.14. This occurred in 2 of the 4 different electrode arrangements. Figure 7.7 shows all the different arrangements of the electrodes; in situation (a) and (c), changes occurred when the applied voltages were switched off. The settings that these two situations had in common were the 70Vdc voltages.

Our explanation for this is that when the voltages are switched off, the DC voltage shuts down earlier than the pulse voltage. When we take a look at situation (a), when the voltages are switched off, and the DC voltage switches off first, the common electrode would be set to 0V, while the data line electrode is still at 70V, which causes the charges to run in opposite directions than when the voltages were both active. Same goes for situation (c).

For our product, the Super E-paper, we assume that DC voltages of 70V aren't necessary since the 70V pulse can simply be connected to the opposite electrode.

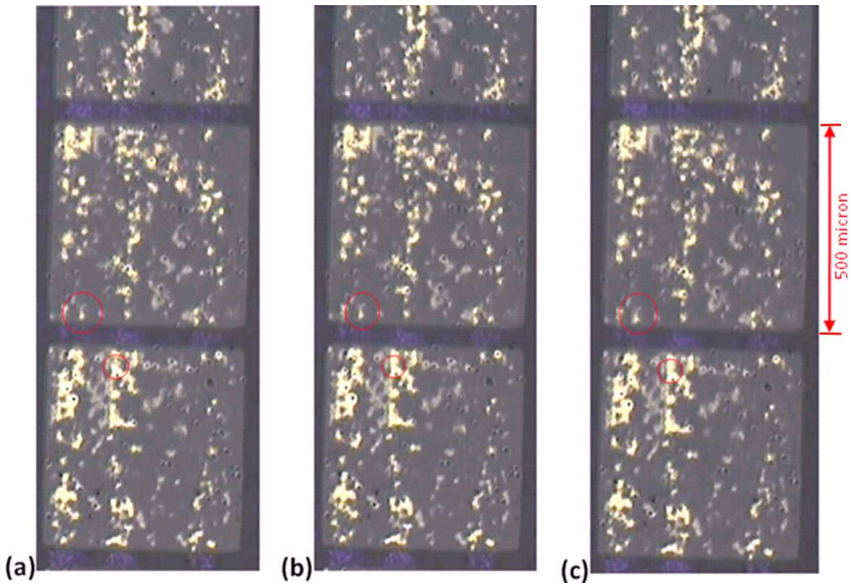


Figure 7.14: Array of pixels changing when voltage is applied from (a) to (b), and when voltage is switched off from (b) to (c).

Another remarkable observation was that when the electrodes were connected to opposite sources, the first change after the switch showed a lot of particle movement. This can be observed from Figure 7.15. However, this movement can not be tested for variation in types of power since again no common reference situation can be made. We wanted to change the screen into a full black or white colour by doing multiple tests with the same voltage setting. By switching the connections, this common reference situation has to be obtained once more for a fair and equal test. Notice that in Figure 7.15, particles within the whole pixel are moving since the pulse is now supplied by the common electrode.

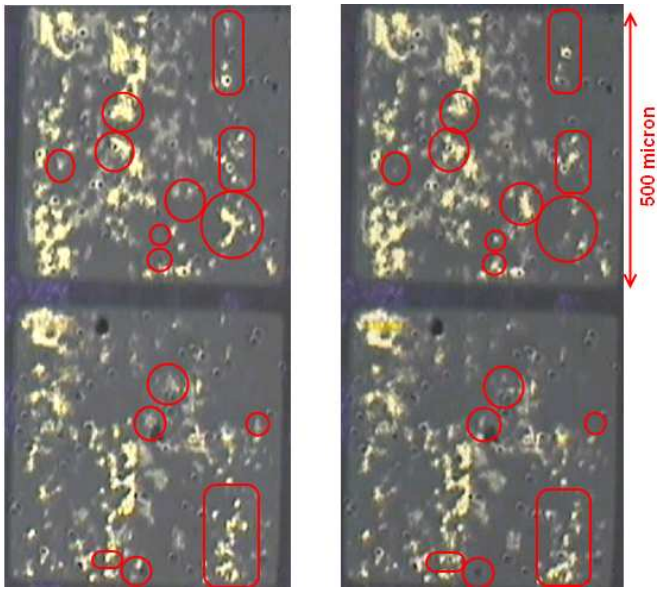


Figure 7.15: Change in pixels under the microscope, increased particle movement due to switching of the sources to the electrodes.

7.4 Conclusion

During our research we have discovered the most change so far compared to previous research in the movement of grains in the pixels, especially when during our research we switched the polarities of the electrodes. We could assign this progress to the fact that we used 70V pulses, whereas previous research was based on applying a 70V DC voltage. We can therefore conclude that applying a pulse to the electrodes is definitely better than applying a DC voltage, which would mean that the duty cycle of the source voltage should be less than 100%.

Also we saw minor increases in particle movement when voltages were turned up. We can therefore also say that a higher voltage causes a bigger electric field which has a bigger effect on the particles.

We also discovered a strange change when switching off the applied voltage in the situations where both electrodes had a voltage applied. The reason for this change is accounted to the slight delay between switching off of both sources.

We started these measurements with the goal of using active matrix addressing, however, halfway through we discovered that this was impossible and passive array addressing was the only way to get a fair amount of results. A few problems during our research however did occur; these problems will be discussed and analyzed.

We can not make detailed conclusions from the results of our active matrix (and passive array) measurements. There are three main problems that prevented us from making precise conclusions:

- The biggest problem was that the changes occurring in the pixels were too little to mark them as causal effects;
- Another important problem was the fact that there was no common reset on the pixel states. The lack of changes could be accounted to the fact that most particles were already touching the electrode. Test results can only be compared if the change in variable can be measured on equal reference points, unless of course the change is overwhelming which the case due to our first problem isn't;
- Finally, the lack of colour distinction of the particles, made it impossible to see if the changes were due to rearrangements of the particles, or due to change of colour.

Our schedule of requirements stated that high amounts of change are required, and a common reference situation is needed for a fair measurement. Both of these requirements couldn't be met. However compared to previous research done by W. Chim and A. Baiano, much more particles have moved due to the usage of pulse voltages. Therefore one aspect of the optimum driving method can be concluded: use pulses in stead of DC voltage to drive pixels.

8. Passive Matrix Measurement with Bridgestone's E-paper

In order to set an image on a display, the pixels forming such an image need to be controlled. One way of controlling the pixels efficiently is by organizing them in a matrix. These pixels can then be controlled, by addressing them by row and column lines. Doing so, the number of wires required for such a matrix organized display is equal to the sum of the number of rows and columns. With regards to controlling and addressing the pixels, two methods can be applied; Passive Matrix addressing and Active Matrix addressing. In this chapter Passive Matrix addressing shall be explained in section 8.1, and our research on the Super E-paper with the Passive Matrix addressing method shall be reviewed in section 8.2. Section 8.3 will give a short conclusion on our results.

8.1 Passive Matrix addressing

One speaks about passive matrix addressing, once the row and column lines are directly used to control pixels of a display. With regards to the E-paper display, by sending pulses on the rows and columns its crossing generates the required electrical field making the grain particles change its state. Figure 8.1 shows an example of passive matrix addressing.

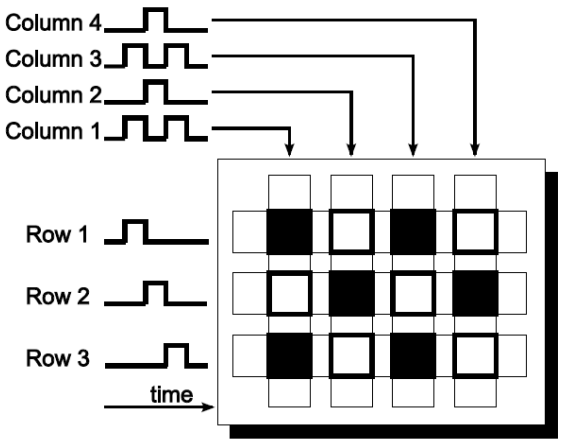


Figure 8.1: Basic passive matrix driving scheme [6]

The Passive Matrix addressing has both its advantage as well as its disadvantage. The best thing about Passive Matrix addressing is its simplicity. In order to control a display and therefore its pixels, only horizontal and vertical wires stretching across the whole screen are required. With this advantage a major drawback comes along; crosstalk among the wires. As the Liquid-Powder in the Quick Response Liquid-Powder Display (QR-LPD) has a high and clear threshold compared to many other displays, this drawback is of less trouble in this case. Another disadvantage is its slow speed and lack of robustness of refreshing the whole display. For our measurements however, speed is not of essence.

8.2 Printing an image on flexible E-paper

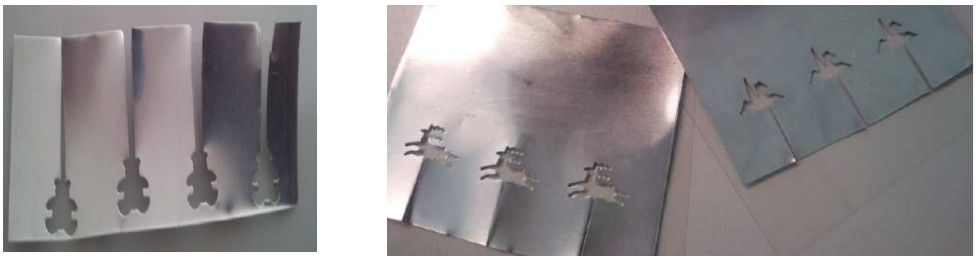
With the help of Passive Matrix addressing an image is hoped to be seen on the E-paper. This image printing on the E-paper is tried to be realized by creating a metallic shaped image on a plastic substrate and put this plastic substrate between the E-paper and the wafer. The colour of this newly created image on the E-paper can be either black or white coloured. This colour depends on the voltage applied, as can be read in chapter 4.

The following parts explain the approach taken to get these images printed and also what the outcomes were.

What was the initially thought approach?

As explained above, in order to get an image printed on the E-paper such an image should have been placed between the E-paper and the wafer to have the image as one electrode, and the common electrode as the other. In order to do so, the Quick-Response Liquid Powder Display (QR-LPD) stuck on the wafer had to be removed.

The image which had to be printed on the E-paper had to be designed. This image designing process went as follows. First the to be printed images had to be cut on a thick aluminium foil, as depicted in Figure 8.2



(a) (b)

Figure 8.2: Images in form of bears in (a) and swans and reindeers in (b) are cut on a thick aluminium foil

After cutting these images on the aluminium foil, the masks were used to cover a plastic substrate. Where the mask wasn't covered by the aluminium foil, 300nm of aluminium was deposited by an electron beam evaporation system in DIMES. Figure 8.3 shows the resulting substrates.

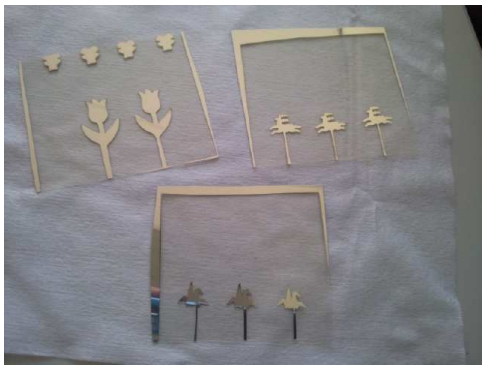
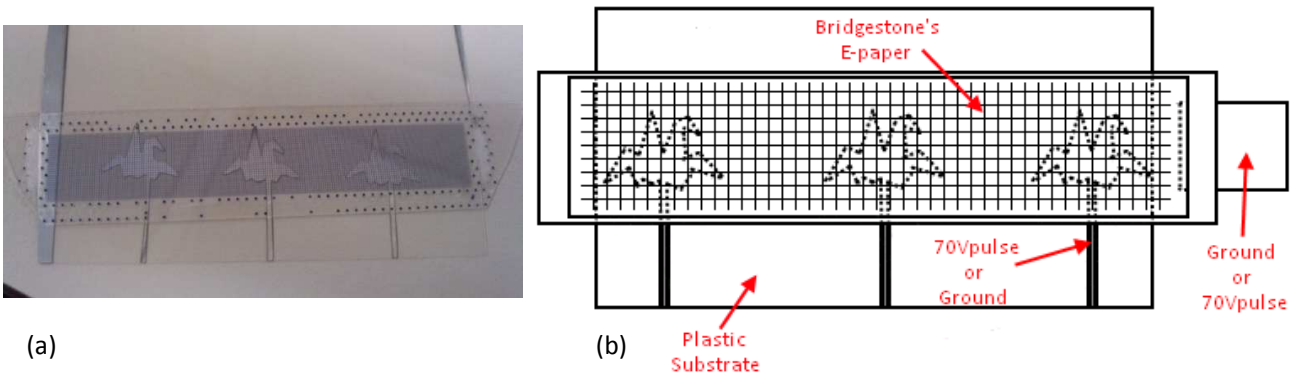


Figure 8.3: The plastic substrate with a layer of 300 nm aluminium shapes deposited on top by electron beam evaporation

These masks had to be stuck between the E-paper and the wafer in order to get that particular shaped image displayed on the E-paper once a voltage was applied. This would be either 70V or -70V, depending on the colour the image had to be given. Figure 8.4 shows Bridgestone's E-paper on top of the plastic substrate with metallic images.



(a) (b)

Figure 8.4: Bridgestone's E-paper taken from the wafer and placed on top of the substrate. In (a) a picture is taken from the E-paper and the plastic substrate, and in (b) the settings are described.

In Figure 8.4b a schematic of the initially thought measurement is shown. The plastic mask with metallic images is placed underneath Bridgestone's E-paper. Either on the metallic image or on the common electrode 0V or 70V is applied (depending on the desired colour).

What actually happened

We initially thought the E-paper was double sided plastic which in between had the grains placed. However once the E-paper was removed, this turned out not to be the case. Bridgestone had put the grains on the wafer and covered it with a single plastic layer on top of it. We think the reason for this is to maximize the effect of the wafer as an electrode. This can be seen from the following.

Suppose the grains were enclosed by a plastic layer from both sides (upper side and lower side), then the distance between the electrode and the grains would be larger. The electric field can be calculated using Coulombs law [22] in the following way:

$$E = k_e \cdot \frac{q}{r^2} \tag{8.1}$$

$$k_e = \frac{1}{4\pi\varepsilon_0} = 8.987 \cdot 10^9 \frac{Nm^2}{C^2} \tag{8.2}$$

We can see that the electric field becomes smaller if the distance between the electrode and the particle becomes bigger. As the distance between the electrode and the grains would be larger by the extra plastic layer, the electric field would therefore become less. This would then result in the effect that the grains would get a lower electric field, which means change will be smaller

As when we removed the E-paper from the wafer, all the grains evaporated. Therefore unfortunately the measurement for the passive matrix had only minimal effect. Despite this, we tried to continue the measurements with the removed E-paper assuming the remaining grain particles on the E-paper would be sufficient for the measurement. However once measured the effects were too little and could not be observed.

Lastly, we still tried doing the measurement with the passive matrix addressing by using the 2nd E-paper stuck on the same wafer. This was attempted by pushing the aluminium layer of the plastic underneath Bridgestone's E-paper, in the hope to see the effects of image printing on the E-paper.. This was tried both ways; by applying a 70V voltage hoping to attract the negative white charged particles as well as applying -70V to attract the positive black charged particles. Once the voltage was applied again no effect was observed

There are two reasons for this:

- The fact that when the aluminium part was pushed into the E-paper, the grains got pushed away. Because of this there were no or at least too little grain particles around the aluminium part, to make it change the colour of the E-paper.
- The grain particles got covered under the aluminium strip once we pushed it in. Due to their limited moving space, because the aluminium strip obstructing it, they therefore couldn't get attracted or repelled to and from the electrodes.

In Figure 8.5 the schematic of this measurement is shown.

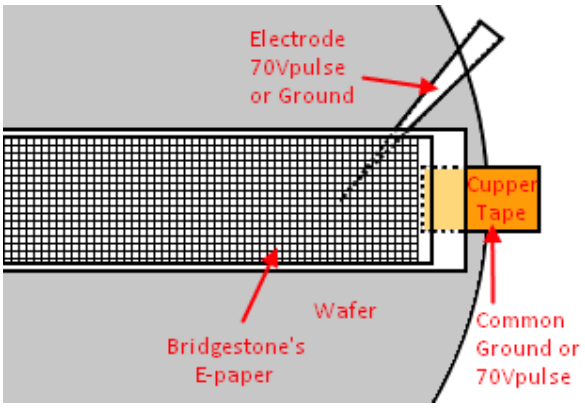


Figure 8.5: The schematic for the 2nd E-paper on the wafer with the aluminium strip pushed inside.

8.3 Conclusion

Passive Matrix addressing is a good way to test the quality of an image. For creating patterns on a flexible substrate, electron beam evaporation has been used to deposit a layer of 300nm thick aluminium. The Quick-Response Liquid-Powder Display (QR-LPD), which is at itself flexible, can then be pasted on this substrate with aluminium lines sticking out to form a model of the flexible Super E-paper.

The only problem is that when pulling off the QR-LPD from the Super E-paper prototype on silicon, the grains that were assumed to be kept in its place through double sided layers of plastic comes out, because grains are simply loosely placed on the wafer and then covered with an Indium-Tin-Oxide and plastic layer.

The requirement for the possibility of sticking the QR-LPD to a flexible substrate is met. The QR-LPD was itself flexible, so could easily be pasted on the flexible display. Sadly, there were not enough particles left to do the passive matrix measurements on.

9. Conclusions and recommendations

The goal of our project was to investigate what the optimum driving method of the Super E-paper is by applying different types of power to the product.

Conclusions

During our research we have discovered the most change so far compared to previous research in the movement of colour in the pixels. Previous research by W. Chim and A. Baiano were based on applying a constant voltage of 70V one of the electrodes. We on the other hand used 70V pulses that triggered more particles and caused their heavier movement compared to the constant voltage. We can therefore conclude that a pulse is required rather than a constant voltage for driving the Super E-paper. We have also observed that a higher amplitude of the source voltage causes more particles to move. This is due to the fact that the higher voltage applied creates a stronger electric field which has a bigger effect on the charged particles. The optimum driving method is therefore:

- *To apply a pulse voltage rather than a constant voltage;*
- *To apply a higher voltage amplitude rather than a lower amplitude for heavier change in the pixels.*

We also noticed a remarkable situation. The particles showed movement in some situations when the applied power was switched off. This occurred only when we used a pulse on one of the electrodes and a DC voltage of 70V on the opposite electrode. We think that this might be due to the short delay of switching off both applied voltages producing at a very short time an opposite electric field.

A few problems during our research however did occur; these problems will be discussed and analyzed. We will also give in this section a list of recommendations for future research.

The specific details for the optimum driving method of Super E-paper can not be made because of several difficulties that we have experienced.

1. Lack of change in pixels when voltage applied: During our tests, we tried changing the value of our variables, however the changes were so little that when one or two grains more had moved, this could be due to rearrangements of the particles or simply because the particles were coincidentally close to the electrode.
2. No common reference point to be able to compare different situations: When we tried to change a single variable, comparison can only be made when every change in variable can be measured with a common starting situation as a reference. The pixels could not be put in this condition since the change of particles again was too little, and the pixels could not be set to all white for example.
3. No visibility of the colour of the grains under the microscope: The microscope uses a strong light that causes both the white as well as the black particles to appear as dark particles. This problem makes it unclear if the movement of the particles during the measurement is due to rearrangement or to the attraction and repulsion of the correct particles by the electrode.
4. Circuitry underneath the pixels was invisible and of incorrect size: The Super E-paper that we used to do our measurements has been used before, and because of this, most pixels were filled with grains on different levels. This made it impossible to see where the matrix of cells was placed for active matrix addressing. Also, the size of a single active matrix addressing cell was much smaller than the size of a pixel which was not the original designed intention.
5. No plastic layer keeping the Liquid Powder at its place: For our Passive Matrix experiment, we were hoping to use Bridgestone's E-paper front plane as a passive matrix by simply using the common electrode that was already glued on the top layer of plastic of the pixels, and our

custom designed electrode in a special shape. When we separated the front plane from the back plane of the Super E-paper however, we discovered that the grains weren't supported o the wafer side, but simply placed on the wafer without another plastic layer that kept the grains in their places. So most of the particles got lost when the front plane was removed. Measurements on the remaining particles gave only little results.

Recommendations

For future research we have a number of recommendations:

1. Use a new front plane that makes the underlying circuitry visible so that active matrix addressing can be checked correctly.
2. This new front plane should have equal active matrix addressing cell size as pixel size.
3. Ask from Bridgestone a separate piece of E-paper front plane that can be used for passive matrix addressing.
4. Use a magnifying glass in stead of a microscope to see the movement of different coloured particles.

Schedule of requirements

During our research we have met most of our requirements for the features that the Super E-paper can provide. The requirements met for chapters 7 and 8 are described in the conclusion. The other requirements that are met in the other phases of our research will be described.

Chapter 4: Explained the benefits of the two technologies used: Single Grain Thin-Film Transistor (SG-TFT) technology and Quick-Response Liquid-Powder Display (QR-LPD) technology.

- Full flexibility of the final product is realized
- Higher refresh rate is possible
- Integrated circuits can be placed behind the display, this ensures that the final product would have no edges and still be fully flexible

Chapter 5: Proved the quality of the SG-TFT

- High speeds can be reached using this transistor

Chapter 6: Described the design of our level shifter

- The requirement of minimum amplitude of 35 volts has been met
- The requirement of producing pulses has been met.

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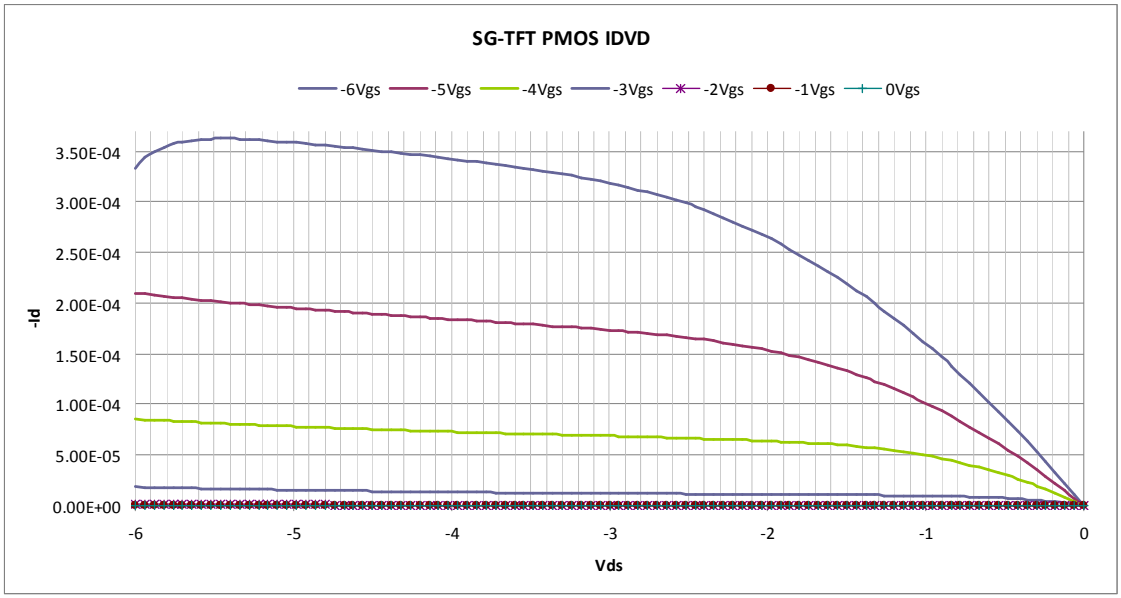
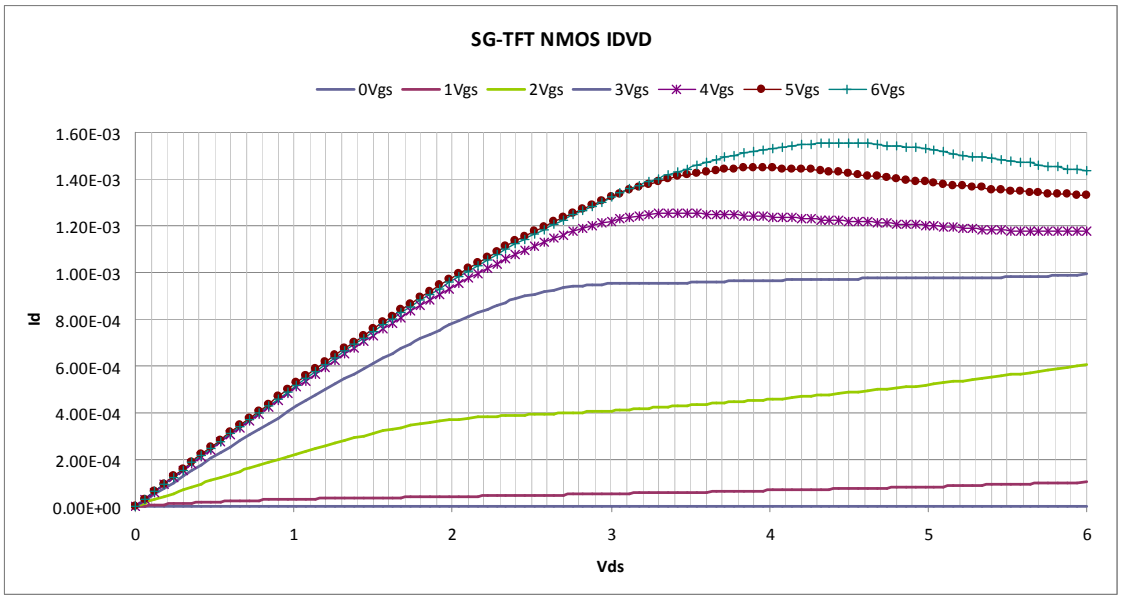
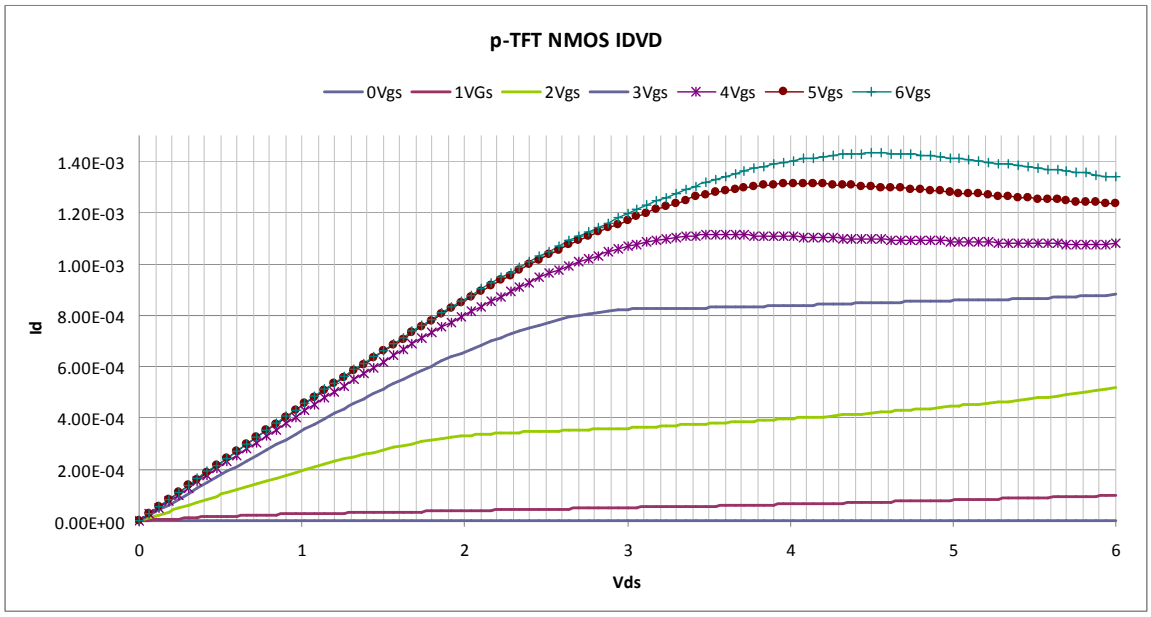
Appendix 1: Measurement results SG-TFT

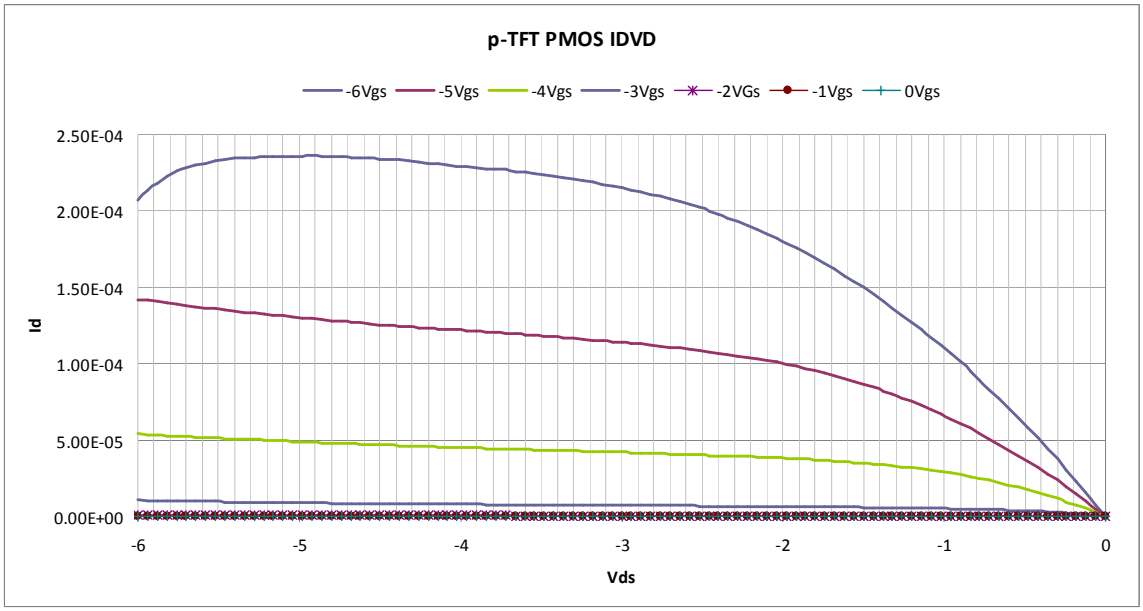




Vstep = 60mV
Number of points = 101
Notice that for the PMOS IDVD the y-axis scale is –Id.

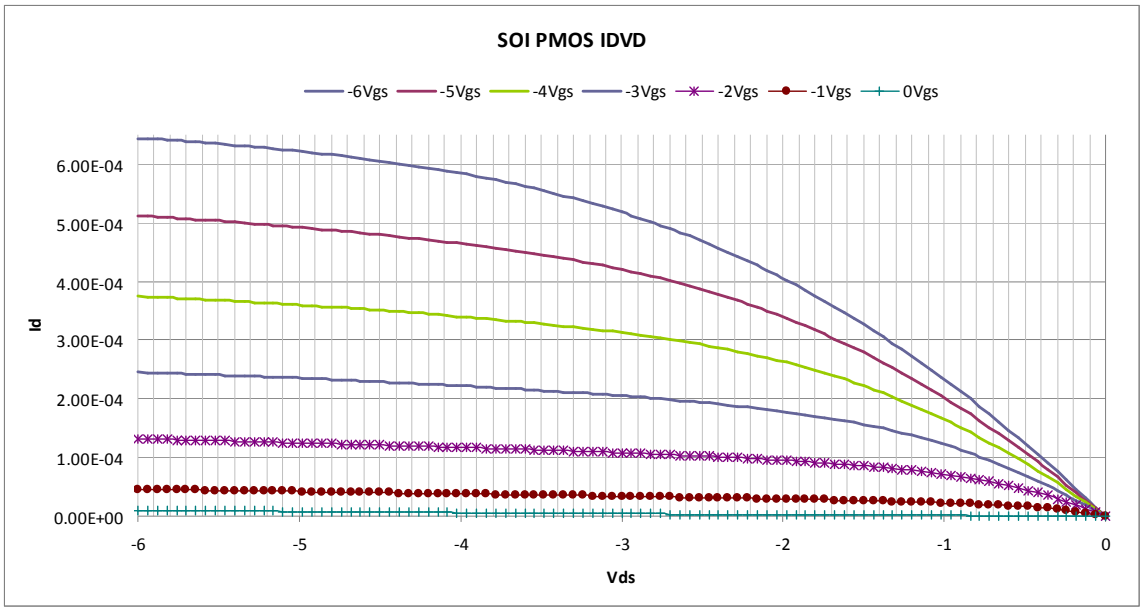
Appendix 2: Measurement results p-TFT

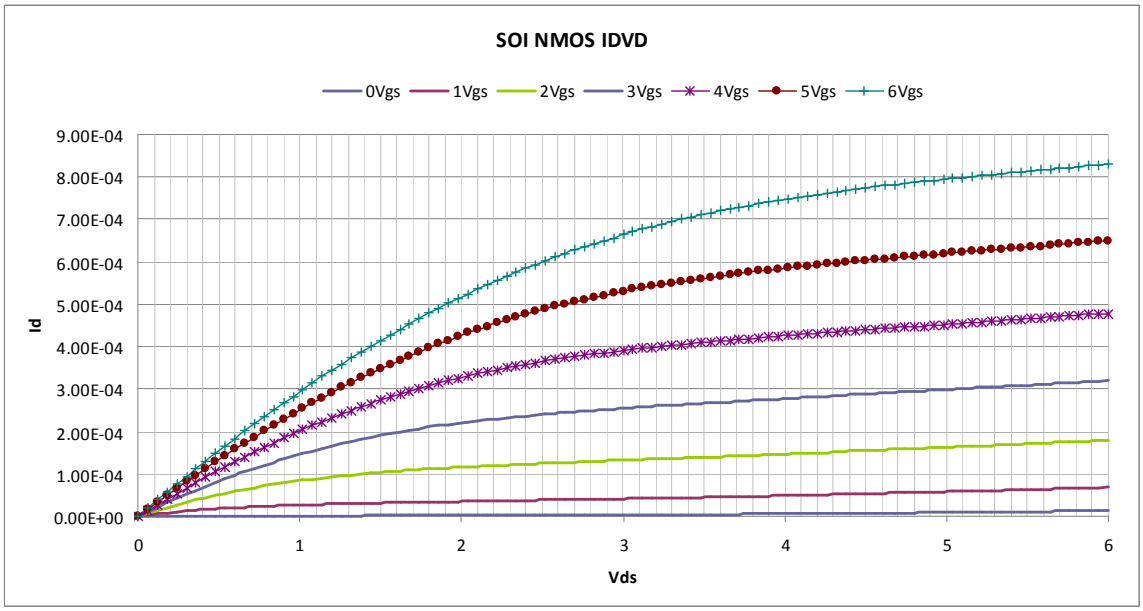




Vstep = 60mV
Number of points = 101
Notice that for the PMOS IDVD the y-axis scale is –Id.

Appendix 3: Measurement results SOI transistors





Although the threshold voltages of the SOI transistors are closer to 0V than the SG-TFT's, the SG-TFT's have a wider on and off current range, a lower subthreshold swing, and a better mobility.
The IDVD graph doesn't show any non-linearity for high drain voltages because the silicon layer is much bigger, with a length of 350nm. Again due to the short channel length, velocity saturation occurs, and the graph grows steadily in a linear way.

Vstep = 60mV
Number of points = 101
Notice that for the PMOS IDVD the y-axis scale is –Id.

Appendix 4: IRF540 Datasheet

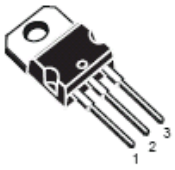
Only the page with the specifications we needed has been copied here

IRF540

N-CHANNEL 100V - 0.055 Ω - 22A TO-220
LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF540	100 V	<0.077 Ω	22 A

- TYPICAL $R_{DS}(on)$ = 0.055Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW GATE CHARGE
- APPLICATION ORIENTED CHARACTERIZATION



TO-220

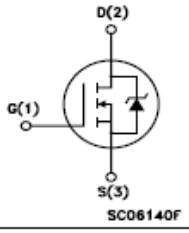
DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL

INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
IRF540	IRF540&	TO-220	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	22	A
I_D	Drain Current (continuous) at T_C = 100°C	15	A
I_{DM}(•)	Drain Current (pulsed)	88	A
P_{tot}	Total Dissipation at T_C = 25°C	85	W
	Derating Factor	0.57	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	9	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	220	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area.

1) I_{SD} ≤22A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}
(2) Starting T_j = 25 °C, I_D = 12A, V_{DD} = 30V

NEW DATASHEET ACCORDING TO PCN DSG/CT/1C16 MARKING: IRF540 &

Appendix 5: IRF9540 Datasheet

Only the page with the specifications we needed has been copied here

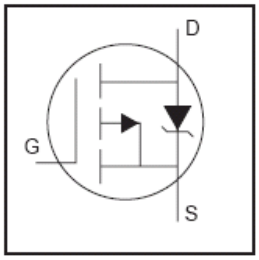
International
IOR Rectifier

PD - 91437B

IRF9540N

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated



V_{DSS} = -100V

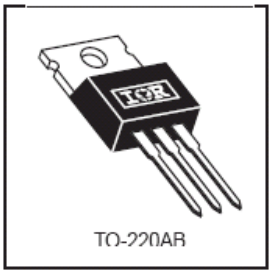
$R_{DS(on)}$ = 0.117Ω

I_D = -23A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-23	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-16	
I_{DM}	Pulsed Drain Current ①	-76	
P_D @T_C = 25°C	Power Dissipation	140	W
	Linear Derating Factor	0.91	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	430	mJ
I_{AR}	Avalanche Current①	-11	A
E_{AR}	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

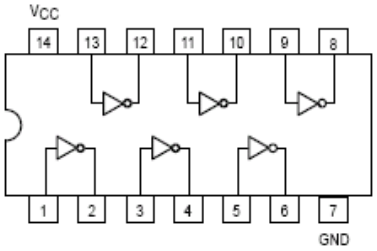
5/13/98

Appendix 6: 74LS04 HEX inverter Datasheet

MOTOROLA

HEX INVERTER

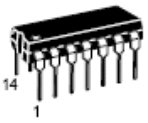
SN54/74LS04



HEX INVERTER

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

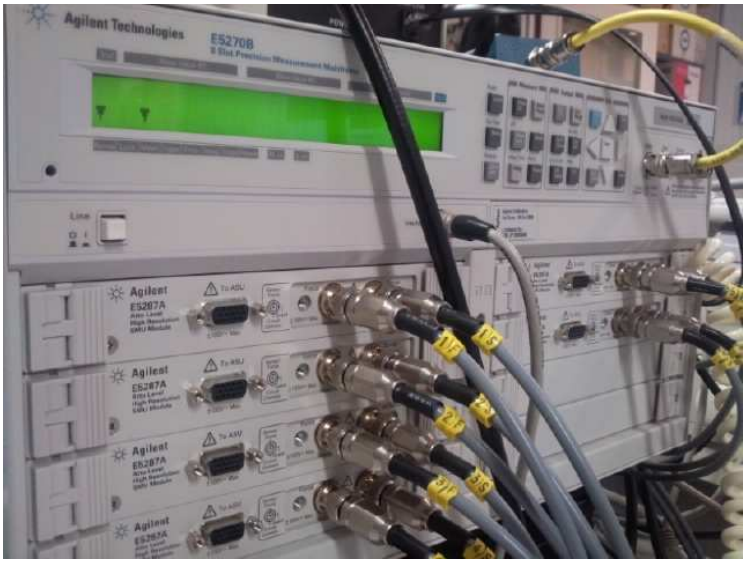
Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				2.4	mA	V_{CC} = MAX	
	Total, Output LOW				6.6			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

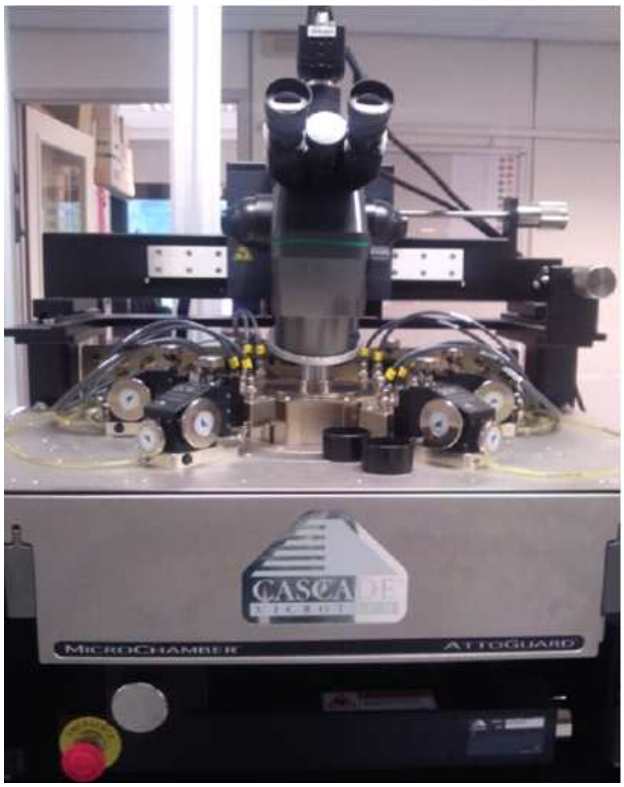
AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		10	15	ns	

Appendix 7: Devices and Components



Agilent Technologies: E5270B
8 Slot Precision Measurement Mainframe
Used for: Transistor measurements in chapter 5.

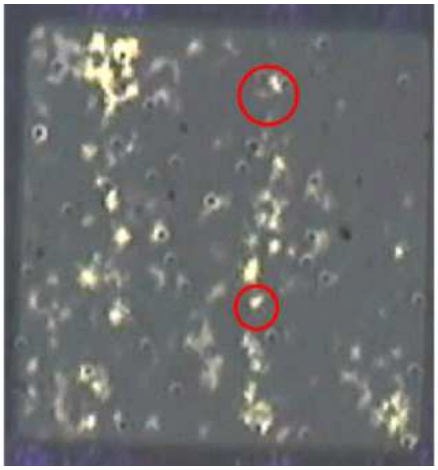


CASCADE MICROTECH
Probe Station 34
Used for: Transistor measurements of chapter 5

Agilent 4156C
Precision Semiconductor Parameter Analyzer
Used for: Active Matrix measurements in chapter 7

CASCADE MICROTECH
Probe Station 31
Used for: Active Matrix measurements in chapter 7

Appendix 8: More images of changes in pixels



Before

After

Before

After

Before

After