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Energy-Efficient Bridge-to-Digital Converters

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***Abstract*—This paper presents an overview of energy-efficient analog-to-digital converters (ADCs) specifically intended for the readout of Wheatstone bridge sensors. Apart from achieving good energy-efficiency, such bridge-to-digital converters (BDCs) must achieve low input-referred offset, drift and noise; high gain accuracy, stability and linearity; as well as high immunity to power-supply and common-mode variations. Various BDC architectures are discussed, beginning with traditional designs, in which an instrumentation amplifier is used to drive an ADC, and moving on to more recent work, which attempt to increase energy efficiency and reduce complexity by eliminating the instrumentation amplifier. The performance of these topologies, and in particular their energy-efficiency, will be compared and summarized.**

Keywords—Wheatstone bridge sensor; energy-efficiency; instrumentation amplifier; analog-to-digital converter; bridge-to-digital converter.

I. Introduction

Although more than 180 years old, the Wheatstone bridge is still widely used to measure resistances (impedances) due to its simplicity, stability and accuracy [1,2]. Wheatstone bridges are often used to sense physical quantities such as pressure, strain, temperature and magnetic field via their effect on sensor impedances [3-8]. In such cases, the output of the bridge will typically be a mV-level differential signal superimposed on a much larger common-mode (CM) voltage, which must then be digitized by a so-called bridge-to-digital converter (BDC). To avoid corrupting the bridge output, a BDC should also achieve low input-referred offset, drift and noise; high input impedance, gain accuracy, stability and linearity; as well as high immunity to power-supply and common-mode variations. This challenging task is somewhat relaxed by the fact that sensor signals are quite slow, and so bandwidths of a few kHz are often quite sufficient.

Considerable efforts have been made to improve the energy-efficiency of BDCs, i.e. the amount of energy that they need to achieve a certain input-referred noise level [3-10]. This is mainly due to the proliferation of battery-powered sensing systems, e.g. in mobile and IoT applications, in which energy efficiency is critical, and, to a lesser extent, by the need to reduce self-heating errors in precision mechatronic systems.

As shown in Fig. 1a, a conventional BDC consists of an instrumentation amplifier (IA) followed by an analog-to-digital converter (ADC). The IA boosts the amplitude of the bridge output to levels that are large enough to drive the succeeding ADC. Being the first stage, the IA defines the BDC's input characteristics and in particular, its input-referred noise, and so will usually determine its energy-efficiency.

Much effort has been devoted to improving the energy-efficiency of IAs. The number of high-gain amplifiers they require has been reduced from three, as in the classic three opamp IA [3], to one, as in the more recent capacitively-coupled IA (CCIA) [6-8]. Furthermore, chopping has been widely applied to suppress in-band 1/*f* noise [3-10].

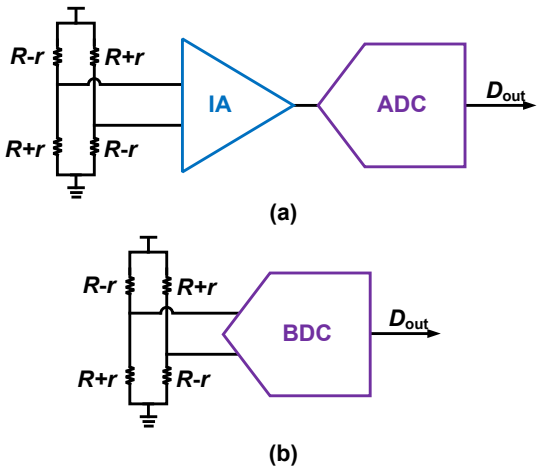

Fig. 1. Conventional BDCs (a); Direct BDCs (b).

Recently, BDCs that eliminate the IA entirely have been proposed [11-18] (Fig. 1b). The motivation for such direct BDCs is to eliminate the associated high-gain amplifiers and thus achieve lower complexity and reduced area. To avoid the aliasing and kT/C noise issues of discrete-time ADCs, direct BDCs usually consist of a high-resolution continuous-time (CT) ADC. Then in order to achieve good gain accuracy and stability, as well as low input-referred offset, drift and noise, dynamic compensation techniques such as chopping and dynamic element matching (DEM) are often employed [19].

This paper presents a non-exhaustive review of energy-efficient BDCs, with the aim of discussing architectural and circuit-level innovations that have advanced the state of the art. The paper is organized as follows. Energy-efficiency metrics for BDCs are discussed in Section II, together with some general design considerations in Section III. Section IV discusses the energy-efficiency of conventional BDCs (Fig. 1a), while some recent direct BDCs are discussed in Section V (Fig. 1b). Comparisons of state-of-the-art BDCs are given in Section VI. Finally, some conclusions are drawn.

II. Energy-Efficiency Metrics For BDCs

In a so-called "full" Wheatstone bridge sensor (Fig. 1), all four bridge resistances change in tandem in a manner that maximizes bridge sensitivity. In this case, the output voltage V_{out} is given by

$$V_{out} = \frac{V_{bias} \times r}{R_{bridge}}, \quad (1)$$

where V_{bias} is a DC biasing voltage, R_{bridge} is the nominal bridge resistance and r is their resistance change. So-called "half" bridges are also used, in which two of the resistors are fixed. In this case, V_{out} will be a non-linear function of the ratio r/R_{bridge},

$$V_{out} = \frac{V_{bias} \times r}{2R_{bridge} + r}. \quad (2)$$

However, this ratio will often be less than 1%, and so this non-linearity can be neglected.

With V_{bias} in the order of a few Volts, V_{out} will usually be at the mV-level and so must be boosted by an IA before being applied to an ADC. This should be done efficiently, i.e. the BDC's input-referred noise should be made as low as possible while consuming the least amount of energy. Some of the metrics for evaluating the energy-efficiency of IAs and ADCs will be discussed in the following.

The energy-efficiency of IAs is often evaluated by calculating their noise efficiency factor (NEF) [9], as given by

$$NEF = V_n \sqrt{\frac{2I_{tot}}{\pi \cdot V_t \cdot 4kT \cdot BW}}, \quad (3)$$

where V_n is the amplifier's input-referred noise voltage, I_{tot} is its supply current, BW is its bandwidth and V_T is the thermal voltage kT/q. The NEF expresses how an amplifier's noise performance compares to that of a single bipolar transistor with the same current consumption [9]. Thus, a smaller NEF corresponds to better energy-efficiency. However, the NEF does not take the IA's supply voltage V_{DD} into account, which is application and process dependent, and so a more accurate metric is the power efficiency factor (PEF), defined as PEF = $NEF^2 \times V_{DD}$ [20].

BDCs typically employ high-resolution ADCs, whose resolution will then be thermal-noise limited. For such ADCs, the appropriate metric of energy-efficiency is the Schreier figure of merit (FoM_S) [21], defined as

$$FoM_S = DR + 10\log\left(\frac{BW}{P}\right), \quad (4)$$

where DR is the ADC's dynamic range, and P is its power dissipation. It is often expressed in terms of SNDR, since, in many practical situations, distortion is just as bad as noise.

It should be noted that FoM_S is expressed in terms of *relative* noise (or distortion) levels. However, BDCs are usually designed to achieve an *absolute* level of input-referred noise, which should be commensurate with that of the bridge. Furthermore, the IA of a BDC will typically have significant gain (> 10), and so will determine the BDC's noise performance. As such, when evaluating the energy-efficiency of BDCs, the NEF and/or PEF are better metrics than FoM_S.

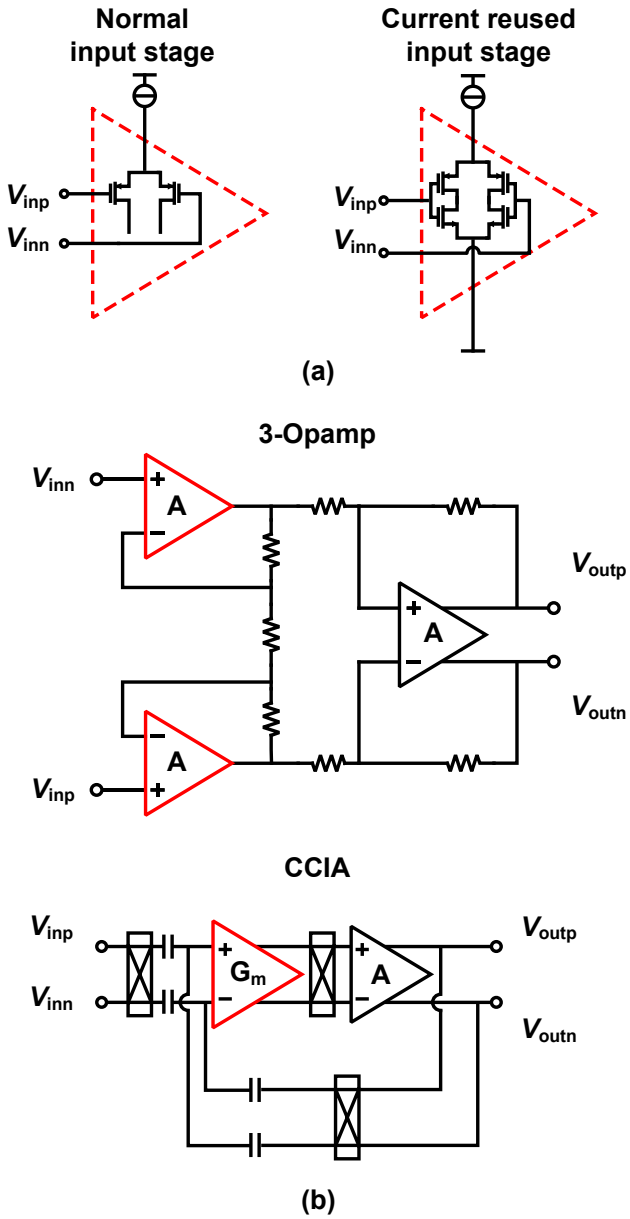

Fig. 2. A conventional input stage and a current-reuse input stage (a); A classic 3-Opamp IA and a CCIA (b). Noise-critical stages are indicated in red.

III. General Design Rules for Energy-Efficiency

In terms of energy efficiency, the most critical block of an IA is usually its input stage. This will usually have significant gain, and thus will minimize the noise contribution of succeeding stages. As shown in Fig. 2a, current-reuse input stages are more efficient than conventional input stages since they provide roughly double the transconductance for the same supply current. This comes at the expense of less output swing. But this is usually not a significant drawback in BDCs, since their IAs employ multi-stage topologies for high open-loop gain and thus high closed-loop gain accuracy.

The number of noise-critical input stages in an IA depends on the chosen architecture. For example, the classic 3-Opamp IA and the CFIA [22], have two, while the CCIA [23] only has one (Fig. 2b). As a result, CCIAs are in general more energy-efficient than either 3-Opamp IAs or CFIAs.

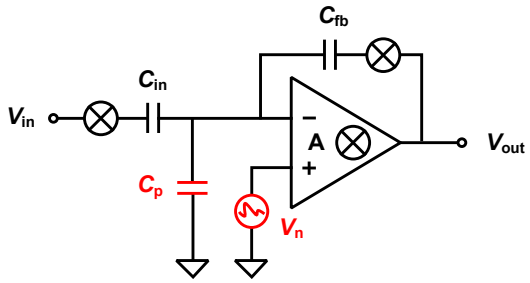

Fig. 3. Noise analysis of a CCIA.

However, CCIAs are usually configured as inverting amplifiers, and so their noise gain will be higher than their signal gain, thus degrading their energy efficiency. From Fig. 3, the signal gain, G_{CCIA}, and the noise gain, NG, of a CCIA can be calculated as follows:

$$G_{CCIA} = -\frac{C_{in}}{C_{fb}}, \tag{5}$$

$$NG = -\frac{C_{in} + C_p + C_{fb}}{C_{fb}}, \tag{6}$$

where C_{fb} is the feedback capacitance, C_p is the parasitic capacitance of the input stage and V_n is its input noise. Compared to the input signal V_{in}, the input-referred noise will be amplified by a noise factor, F, which is given by

$$F = \frac{G_{CCIA}}{NG} = \frac{C_{in} + C_p + C_{fb}}{C_{in}}. \tag{7}$$

For $G_{CCIA} > 10$, C_{in} will be much larger than both C_p and C_{fb}, which means that $F \sim 1$. However, if large input devices are required, e.g. in low-noise applications, C_p may be quite large, thus increasing F and reducing energy-efficiency.

By definition, $F = 1$ for open-loop amplifiers, which thus achieve the highest energy efficiencies. However, this comes at the expense of reduced gain accuracy, linearity and stability, making them unsuitable for bridge readout applications. In general, improving the energy-efficiency of IAs involves reducing the number of noise-critical stages and reducing the effect of feedback and parasitic impedances on the noise factor F, while taking care to preserve other key BDC specifications.

IV. Conventional BDCs

A traditional 3-Opamp IA can provide a well-defined gain and high input impedance. However, its energy efficiency is relatively poor because its input stage consists of two high-gain opamps. Moreover, its CM input level is restricted by its output voltage range, making it difficult to sense CM levels close to the supply rails. In bridge readout applications, this limits the maximum value of V_{bias}, and, in turn, limits bridge sensitivity. Both CFIAs and CCIAs are much better in this regard.

A. CFIA based BDCs

In a CFIA (Fig. 4), the input and feedback voltages are first converted to currents by transconductance stages G_{min} and G_{mfb}, respectively. Their difference is then nulled by the amplifier's overall gain. The voltage gain of the IA can then be expressed in terms of its feedback resistors R_1 and R_2 as,

$$A_{Gain} = \frac{G_{min}}{G_{mfb}} \times \frac{R_1 + R_2}{R_2}. \tag{8}$$

A CFIA has higher CMRR and input impedance than a 3-Opamp IA. Its CMRR is mainly determined by the CMRR of G_{mfb} and can often exceed 120 dB [4]. It is also capable of handling input CM voltages that include either of the supply rails [22]. It is also more energy efficient, since both input stages share a single output stage

The main disadvantage of the CFIA is its limited gain accuracy. Even with precision feedback resistors, this will be limited by the matching of G_{min} and G_{mfb}, which will vary over PVT, as well as CM voltage, and is limited to about 0.5% [4].

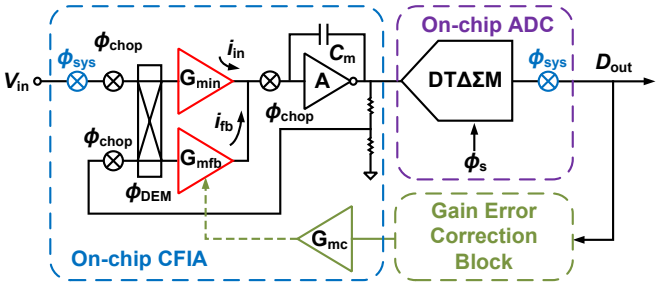

Fig. 4. BDC based on CFIA with DTADC.

As shown in Fig. 4, the gain accuracy of CFIA's can be improved by dynamic element matching (DEM) and digitally assisted gain error-correction [4,5]. In this way, the mismatch between G_{min} and G_{mfb} is averaged out and CM-dependent gain errors are minimized. In [4], such a CFIA was followed by a SC incremental delta-sigma (ΔΣ) ADC, resulting in 5 ppm INL and a 0.7 ppm/ºC gain drift. The best reported NEF for a CFIA-based BDC is 10.4 [4].

B. CCIA based BDCs

As discussed in Section III, CCIAs are usually more energy-efficient than 3-Opamp IAs and CFIAs [3,23,24]. Furthermore, their input capacitors naturally block CM voltages, allowing them to have CM voltage ranges that exceed their own supply rails [6]. Moreover, the gain of a CFIA is set by a ratio of capacitors, rather than resistors, and so is usually more stable and accurate.

The main drawback of the CCIA is its limited input impedance. This is because its input capacitances C_{in} are periodically charged/discharged by the chopped input voltage $\pm V_{in}$. The resulting input impedance $Z_{in} \propto 1/f_{chop}C_{in}$, where f_{chop} is the chopping frequency. Z_{in} is typically in the order of a few mega-Ohms [6], which is somewhat low for bridge readout.

Boosting a CCIA's input impedance involves finding ways to ensure that the currents required to charge/discharge C_{in} are *not* drawn from the input signal V_{in}. In [6], this was achieved

by a capacitively-coupled positive feedback loop, which was driven by the output of the CCIA. In [7], an auxiliary pre-charge buffer was used. The latter solution requires active blocks which cannot operate beyond the supply rails, and thus limit the CCIA's CM input range.

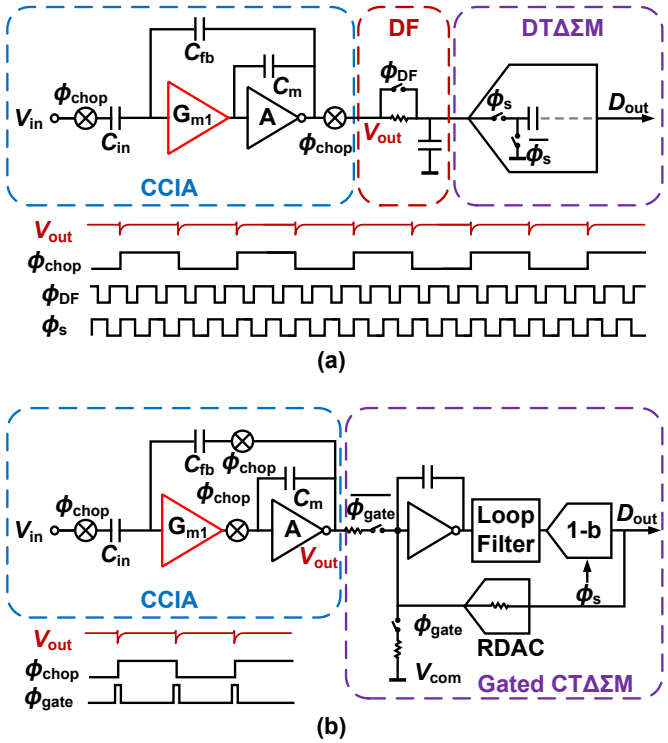

Fig. 5. BDC based on CCIA with DTADC using a dynamic filter (a); BDC based on CCIA with gated CTADC (b).

Another drawback of CCIAs is that they generate output spikes at $2f_{chop}$. These are caused by the finite slew rate of their output stages, which cannot instantaneously generate the chopped output voltage $\pm V_{out}$ dictated by the feedback loop and the choppers [6].

To avoid introducing extra offset and non-linearity, the output spikes of a CCIA should *not* be digitized. In a discrete-time ADC, this can be readily achieved by sampling the output of the CCIA just before the chopping transitions [6]. But the CCIA's bandwidth then needs to be wide enough to ensure complete settling, which leads to increased noise aliasing. Furthermore, the ADC's sampling frequency f_s is now the same as $2f_{chop}$, which limits design flexibility. In [7], a dynamic filter (DF) was used to limit the noise bandwidth while maintaining settling accuracy (Fig. 5a). The resulting IA achieved an NEF of 6.4, at the expense of increased design complexity.

Alternatively, the input of a continuous-time delta-sigma modulator (CTΔΣM) can be gated to avoid the spikes [8]. As shown in Fig. 5b, the ADC's input is shorted to a CM voltage during the spikes, and connected to the CCIA after the spikes have died out. Since the spikes are quite short, the use of gating only results in a small (2.5%) reduction in the CCIA effective gain. The design in [8] achieves an NEF of 5, as well as 12.5 nV/ºC offset drift and 28 ppm INL, which represents the state of the art for this level of stability and linearity.

C. Open- loop VCO-based BDCs

Recently, VCO-based BDCs have been proposed. As shown in Fig. 6, these consist of an input transconductor G_{min}, whose output current drives a pair of current-controlled oscillators $CCO_{1,2}$, whose output phase can then be sampled and differentiated to realize a 1st order sigma-delta modulator [24]. The open-loop input G_m stage confers high input impedance and energy-efficiency. In [10], an NEF of 4.6 was achieved with a simple and compact design.

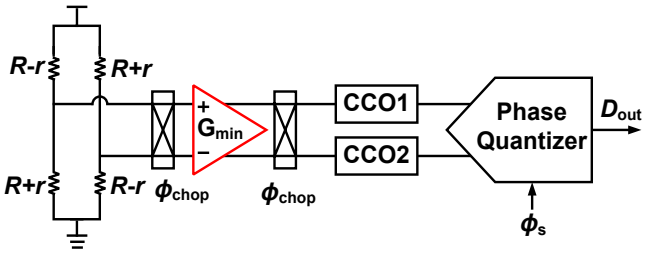

Fig. 6. Open-loop VCO-based BDC.

However, the use of an open-loop Gm stage also results in poor gain accuracy and non-linearity (INL of 348 ppm). Moreover, CCO mismatch results in a residual offset of about 50 µV, which is quite large for a BDC.

V. Direct BDCs

A conventional BDC usually requires two feedback loops, one around its IA and the other around its ΔΣ ADC. Each loop should have enough gain to obtain high linearity, which typically requires at least two high gain amplifiers, and hence, increased complexity and area. Moreover, the BDC's overall gain will be defined by at least two resistor/capacitor ratios [3-8,10], making it twice as hard to achieve gain accuracy. To address these issues, a number of direct BDC architectures have been proposed, in which the IA and ADC have been embedded in a single feedback loop.

A. Closed-loop CFIA-like BDCs

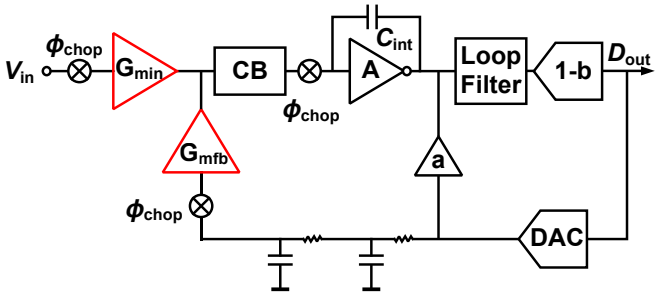

Fig. 7. Closed-loop CFIA-like BDC: Gm-C CTΣΔM BDC.

In [11], a CFIA and an ADC were embedded in the feedback loop of a single sigma-delta modulator. The result is shown in Fig. 7. Matched transconductors (G_{min} and G_{mfb}) were used in both the signal and feedback paths, giving the modulator the high input impedance and CMRR of a CFIA. To accommodate the limited input range of G_{mfb}, however, the large-amplitude quantization noise generated by its 1-bit DAC

was first filtered by a 2nd order RC filter. This in turn required an extra feedback path to compensate for the extra delay in the feedback path. Compared to a conventional CFIA-based BDC with similar performance [4], the design in [12] required less area, but achieved a somewhat worse NEF of 12. To save more area, the combination of the 1-bit DAC and an analog filter could be replaced by a FIR filter [25].

B. Closed-loop CCIA-like BDCs

A CCIA and an ADC can also be merged into a single sigma-delta modulator by embedding them in a CCIA-like capacitively-coupled feedback loop [26]. Like a CCIA, the resulting BDC only has a single noise-critical stage and so should inherit its energy efficiency, as well as its input characteristics: wide input CM range, high gain accuracy, but only moderate input impedance. The latter can be boosted with the same techniques used for CCIAs [6,7]. As in a closed-loop CFIA-like BDC, however, measures must be taken to ensure that the quantization noise fed back from the modulator's DAC does not overload the input stage.

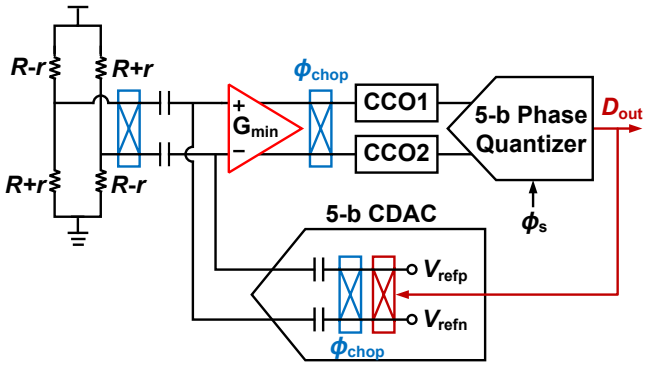

Fig. 8. Closed-loop CCIA-like BDC: Closed-loop VCO BDC.

As shown in Fig. 8, a VCO-based ADC is embedded in a chopped and capacitively-coupled feedback loop [15]. A 5-bit DAC is used to ensure that the feedback quantization noise does not overload the input transconductor. Compared to the open-loop VCO-based BDC in [10], it achieves better linearity and a (10×) larger input range. However, it only achieves an NEF of 22.6, probably due to the non-idealities of its capacitive DAC such as charge injection and non-linearity. Although not intended for bridge readout, the design in [27] embedded a Gm-C integrator and a 5-bit SAR into a similar feedback loop. Compared to [15], it achieves better energy efficiency (an NEF of 7.8).

C. Current-mode BDCs

Instead of reading out the open-circuit output voltage of a Wheatstone bridge, another approach is to read out its short-circuit output current. One example of this current-mode approach is shown in Fig. 9a, in which the bridge is connected to the input of a transimpedance amplifier (TIA). The output voltage V_{out} will then be a non-linear function of r,

$$V_{out} = \frac{2 \times V_{bias} \times r}{R_{bridge}^{\ 2} - r^2} R_f \,. \qquad (9)$$

In many cases, however, r/R_{bridge} will be less than 1%, and so this non-linearity can be neglected. To achieve high gain, the feedback resistance R_f, will be much larger than R_{bridge}, and so the BDC's input-referred noise will be mainly determined by the TIA. A possible drawback is the fact that the BDCs gain will now be determined by R_f, whose temperature dependency and stability may not match that of the bridge.

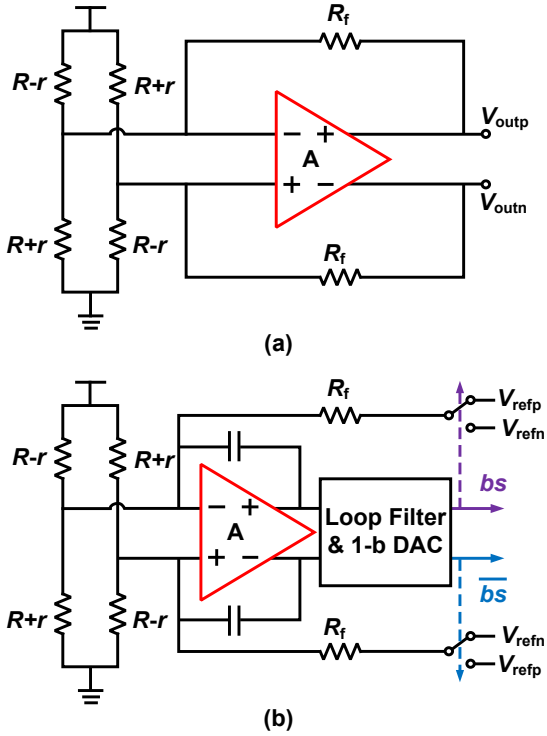

Fig. 9. Wheatstone bridge interface with analog feedback (a); Wheatstone bridge interface with digital feedback (b).

As shown in Fig. 9b, another variant on current-mode readout is to use a resistive DAC to balance the output of the bridge, and thus null its short-circuit output current. Balancing the bridge also maximizes its immunity to to variations in V_{bias} [16]. In [17], a Wheatstone bridge made from resistors with opposite temperature coefficients was used to realize a CMOS temperature sensor. The bridge was readout by connecting it to the virtual ground formed by the 1st integrator of a CTΔΣM. In the ratiometric case, i.e. when $V_{refp} = V_{bias}$ and $V_{refn} = GND$, the modulator's bitstream average μ is given by

$$\mu = \frac{2 \times r}{R_{bridge}^{\ 2} - r^2} R_f \,. \qquad (10)$$

In [17], the energy efficiency of the CTΣΔM could have been improved by chopping the 1st integrator and thus suppressing its 1/*f* noise. However, care should then be taken to avoid quantization noise fold-back, and the subsequent degradation of the modulator's in-band noise. The usual approach is to choose $f_{chop} = f_s$, or, in the case of a FIR-DAC, ensuring that f_{chop} coincides with one of its frequency-domain notches [28,29]. Alternatively, f_{chop} can be chosen more flexibly by arranging the chopping transitions to coincide with the "zero" phases of a return-to-zero (RZ) DAC [30].

By chopping the 1st integrator at f_s, the temperature sensor in [18] achieves 10× more energy efficiency than the one in [17]. Its NEF is still only about 10, mainly because the DAC resistors degrade the noise factor of the 1st integrator ($F \sim 1.4$).

VI. Comparison

The performance of some selected BDCs is summarized in Table I. Note that none of the presented BDCs in this overview uses a current-reuse input stage, and so the differences in their energy-efficiency is mainly due to architectural differences.

In general, conventional BDCs achieve better energy-efficiency, than direct BDCs, as well as better accuracy and stability [8,10]. This is because their input stages can be optimized for the efficient and accurate amplification of small DC signal. Although the open-loop VCO-based BDC demonstrates good technology scalability and state-of-the-art energy-efficiency, it suffers from poor gain accuracy and linearity [10]. Direct BDCs are usually simpler and more compact than their conventional counterparts [12,15]. However, preserving this advantage, while achieving a competitive trade-off between energy efficiency and other important specifications, remains an open problem.

TABLE I

THE STATE-OF-THE-ART BDCS

	[4]	[7]	[8]	[10]	[12]	[15]	[18]
Architecture	CFIA+ DTΔΣM	CCIA+ DTΔΣM	CCIA+ CTΔΣM	Open-loop VCO	Gm-C CTΣΔM	Closed-loop VCO	Current-mode CTΔΣM
Input stage	PMOS	NMOS	PMOS	PMOS	PMOS	PMOS	PMOS
Technology	0.7 µm	0.18 µm	0.18 µm	40 nm	0.7 µm	40 nm	0.18 µm
Area (mm^2)	6	0.53[1]	0.73	0.0145	3	0.06	0.73
Supply Voltage (V)	5	3.3	1.8	1.2	5	1.2	1.8
Supply Current (mA)	0.27	0.075[1]	1.2	0.015	0.24	0.0175	0.082
±Input range (mV)	40	20	10	4	40	50	579[3]
DC CMRR (dB)	140	109	134	91	120	--	--
CM Input Range (V)	0–2.5	0–3	0–3.3	0.15–0.65	0–2.5	--	0.9
INL (ppm)	5	5	28	288[2]	15	79[2]	--
Gain Drift (ppm/ ºC)	0.7	0.81	8.9	--	--	--	--
Offset (µV)	0.05	1.8	7	50	1	300	--
Offset Drift (nV/ºC)	6	70	12.5	--	--	--	--
Input noise density (nV/√Hz)	16.2	19	3.7	32	20	140	36
NEF	10.4	6.41	5.0	4.8	12	22.6	10

1. Without taking account of the ADC. 2. Estimated from THD. 3. Normalized to Eq. 1.

As discussed in Section III, reducing the number of input stages is one way to improve energy-efficiency. For example, although the input stages of [4] and [8] both employ the PMOS-input folded-cascode topology. However, the CFIA [4] requires two input stages, while the CCIA [8], only requires one. This results in an NEF difference of about 2×.

The noise factor also plays an important role in BDCs' energy-efficiency. In Table I, the best NEF is achieved by an open-loop design (F = 1) [13], while the efficiency of [18], which also employs a single input stage, is degraded by a poor noise factor (F = 1.4).

Among the selected BDCs, the CCIA-based designs [7,8] achieve a well-balanced performance in terms of energy-efficiency, accuracy, and stability. However, to achieve this, efforts must be put to avoid digitizing the CCIA's output spikes. Moreover, the CCIA's input impedance needs to be boosted to properly amplify the bridge signal.

CONCLUSION

This paper has presented an overview of several recently developed BDCs that target high energy-efficiency, including conventional BDCs, which consist of an IA followed by an ADC, and direct BDCs, which do not have an IA. As discussed in the paper, although direct BDCs are usually more compact, they are not as energy efficient as their conventional counterparts. The main reason stems from the fact that the noise-critical input stage of a direct BDC has to process both the output of the bridge and the output of a feedback DAC. The latter is then a source of extra input-referred noise. Furthermore, special care must be taken to ensure that chopping the input stage does not cause quantization noise fold-back and thus to even more in-band noise. Compared to conventional BDCs, this results in more complex designs, with multiple trade-offs between energy-efficiency and other important BDC parameters such as accuracy, stability and linearity. However, the energy efficiency gap is not that large and so will probably be bridged by future direct BDC designs.

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