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5.4 A Hybrid Thermal-Diffusivity/Resistor-Based Temperature Sensor with a Self-Calibrated Inaccuracy of ±0.25°C (3σ) from –55°C to 125°C

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Resistor-based temperature sensors can achieve higher resolution and energy-efficiency than traditional BJT-based sensors. To reach similar accuracy, however, they typically require 2-point (2-pt) calibration, compared to the low-cost 1-pt calibration required by BJT-based sensors. This paper presents a hybrid temperature sensor that uses an inherently accurate, but power-hungry, thermal-diffusivity (TD) sensor [1] to self-calibrate an inaccurate, but efficient, resistor-based sensor [2]. The use of an on-chip reference obviates the need for accurate temperature stabilized ovens or oil baths, drastically reducing calibration time and costs. Furthermore, by sharing most of the readout circuitry, the associated area overhead can be reduced. After self-calibration at room temperature (RT, ~25°C) and at an elevated temperature (~85°C), the proposed hybrid temperature sensor achieves an inaccuracy of 0.25°C (3σ) from –55°C to 125°C.

A block diagram of the hybrid sensor is shown in Fig. 5.4.1 (top). The resistor-based sensor is built around a Wien-bridge (WB) bandpass filter realized from silicided polysilicon resistors (R_{WB} = 64kΩ, ~0.3%/°C) and MIM capacitors (C_{WB} = 5pF, <100ppm/°C). The filter is driven by a square wave at a fixed frequency (f_{drive} = 500kHz) and its temperature-dependent phase shift (φ_{WB}) is digitized by a phase-ADC [1]. The TD sensor is built around an electrothermal filter (ETF), whose temperature-dependent phase shift is very well-defined, as it is determined by the thermal diffusivity of highly pure bulk silicon (D_{si}) and by lithography [1]. As shown in Fig. 5.4.2 (bottom left), the ETF consists of a heater (n+ diffusion) and a thermopile (p+ diffusion/metal thermocouples) in close proximity (heater/hot-junction distance s = 24um). When driven by a fixed-frequency square wave (f_{drive} = 31.25kHz), the heater generates a phase-shifted temperature gradient in the substrate, which is detected by the thermopile and results in a weak output signal. Since the signal amplitude (~500μV) is much smaller than that of the WB, it is boosted by an OTA before being applied to the ADC.

As shown in (Fig. 5.4.1, bottom), the phase-ADC consists of a 2nd-order phase-domain delta-sigma modulator (PDΔΣM) [2,3]. Choppers in the feedback path of the 1st integrator (f_{chop} = f_{drive}) detect the difference between the phase of the input current and the output of a 1-bit phase DAC. Depending on the bitstream output (BS), the choppers are driven by one of two phase references $\varphi_{0,1}$ derived from an on-chip clock divider. At steady-state, the average current flowing into the 1st integrator is zero, and so the bitstream average is a digital representation of the input signal's relative phase. In ETF mode, $\varphi_{0,1}$ are set to cover an input phase range of 45°to 90°, while in WB mode a range of –22.5° to 22.5° is covered. Although the integrator's 1/f noise is mitigated by the choppers, it still dominates that of the WB [3]. In this work, the residual 1/f noise in WB mode is suppressed by system-level chopping (CHL, 100Hz), implemented by periodically inverting the polarity of both f_{drive} and the phase DAC selection.

The accuracy of the resistor-based sensor is limited by the spread of the 1st integrator's input impedance Z_{in}, as it is effectively in series with the WB. The 1st integrator is based on a Miller-compensated opamp, and so Z_{in} can be reduced by either increasing its unity-gain BW or by increasing the size of the integration capacitors (= 23pF). In this work, the former is efficiently boosted by using a buffer to reduce the opamp's capacitive load (a switched-capacitor CMFB circuit and the 2nd stage), as shown in Fig. 5.4.1 (bottom-left). The buffer (a PMOS source-follower) consumes only 1.1μA compared to the opamp's 16μA, but allows the opamp's BW to be doubled.

To facilitate low-cost calibration, the ETF needs to achieve a resolution (<20mK) commensurate with its target accuracy (0.2°C) in a reasonable conversion time (T_{conv} ≤1s). Compared to [1], the ETF's resistance and, thus, its dominant thermal noise are significantly reduced by using an octagonal layout [4] (Fig. 5.4.2, bottom left). The associated OTA (gm ~1.8mS, BW ~600MHz) is designed so that its noise is lower than that of the ETF, and so that its phase shift contributes negligible temperature error (<0.03°C). After chopping, the OTA's offset appears as ripple at the output of the 1st integrator, and so to prevent it from clipping, the OTA is auto-zeroed [1].

In this work, a telescopic OTA is used (Fig. 5.4.2), which is more area and power-efficient than the folded-cascode OTA used in [1]. To minimize its own 1/f noise, PMOS input transistors and resistor-degenerated NMOS current sources are used. An auxiliary OTA branch (gm ~0.06mS) is used for auto-zeroing. Its hold capacitors (C_H ~7pF) are large enough to ensure that auto-zeroing is only needed at the start of each CHL phase (every 0.5s).

The hybrid sensor was fabricated in a standard 0.18μm CMOS process (Fig. 5.4.7). In ETF mode, the sensor consumes 5.1mW (4.2mW heater, 0.9mW analog, and 0.6μW digital) from a 1.8V supply. In WB mode, when both the heater and the OTA are turned off, its power consumption drops to 66μW at room temperature (RT). The sensor has an active area of 0.2mm², with ~40% occupied by the ETF and OTA. For flexibility, the decimation filters (sinc²) are implemented off-chip. Four WB sensors and four TD sensor variants were implemented on the same chip.

After ceramic DIL packaging, 20 samples from one wafer were characterized in a temperature-controlled oven from –55°C to 125°C. To limit the effect of the oven's temperature drift, the samples were mounted in good thermal contact with a large aluminum block. Furthermore, the resolution of the WB sensor was determined by making differential measurements on two sensors on the same die [3]. As shown in Fig. 5.4.4 (right), the WB sensor achieves 450μK_{rms} resolution with T_{conv} =10ms, which corresponds to a 0.13pJ·K² resolution FoM. After enabling system-level chopping (f_{CHL} =100Hz), its 1/f noise corner drops from ~1Hz to below 10mHz (Fig. 5.4.4, left). In comparison, the ETF sensor's resolution is only 15mK with T_{conv} =1s and f_{CHL} =1Hz, which corresponds to a resolution FoM of 1.2μJ·K². However, this still represents a 6× improvement on [1].

As shown in Fig. 5.4.3, top, the phase shift of the TD sensor varies by ~30° (f_{drive}=31.25kHz), while that of the WB sensor varies by ~23° (f_{drive}=500kHz). The ETF sensor achieves a no-trim inaccuracy of 0.2°C (3σ) around RT (Fig. 5.4.3, bottom left), which is similar to that of [1]. On the other hand, the WB sensor's no-trim inaccuracy is larger than 10°C. After mapping the BS output to resistance, the WB sensor achieves 0.5°C (3σ) inaccuracy after a correlated 1-pt trim [2] (Fig. 5.4.5, top left). After a 2-pt trim at –35°C and 105°C this improves to 0.03°C (3σ), which represents the state-of-the-art (Fig. 5.4.5, top right). However, this requires an external reference sensor. Using the ETF as an internal reference (at RT and ~85°C) results in an inaccuracy of 0.25°C (3σ), Fig. 5.4.5 (bottom right). For somewhat better inaccuracy 0.15°C (3σ), (Fig. 5.4.5, bottom left), an external reference can be used to calibrate the hybrid sensor at RT, allowing the TD sensor to be offset-trimmed before it is used to calibrate the WB sensor at another elevated, but not well defined, temperature (85°C).

Figure 5.4.6 summarises the performance of the proposed hybrid sensor and compares it with state-of-the-art BJT- [5,6], resistor- [2,3], and ETF- [1] based sensors. The WB sensor achieves a state-of-the-art relative inaccuracy after a 2-pt trim, the lowest reported 1/f noise corner, and a competitive resolution FoM. It obtains a 3σ inaccuracy of 0.25°C from –55°C to 125°C after a cost-effective self-calibration, which is comparable to that of BJT-based sensors [5,6]. In contrast to BJT-based sensors, however, the scalability of TD sensors means that even better performance can be expected in nanometer CMOS processes.

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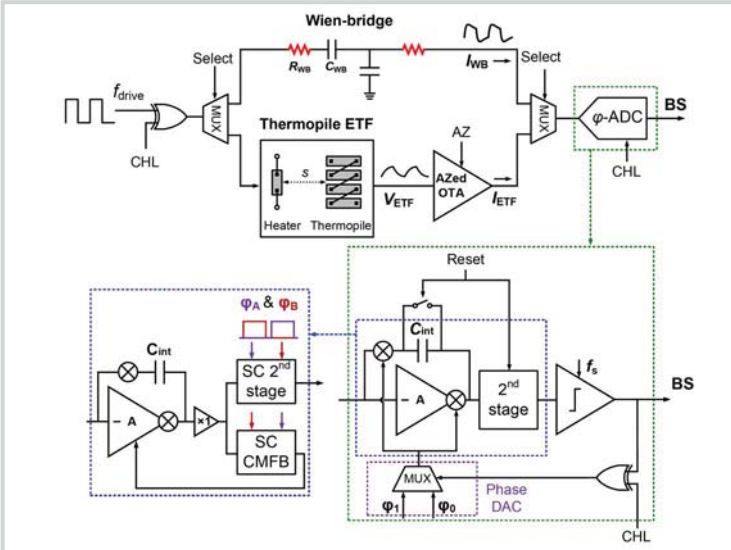

Figure 5.4.1: Simplified schematic of the hybrid sensor (top), phase-domain delta-sigma modulator (bottom right) and the use of a buffer to extend the 1st-stage opamp's bandwidth (bottom left).

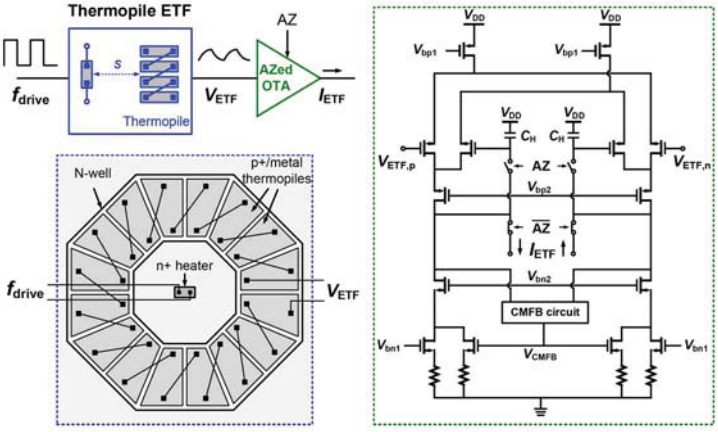

Figure 5.4.2: Octagonal layout of the thermopile ETF (bottom left) and simplified schematic of the auto-zeroed (AZ) OTA (right).

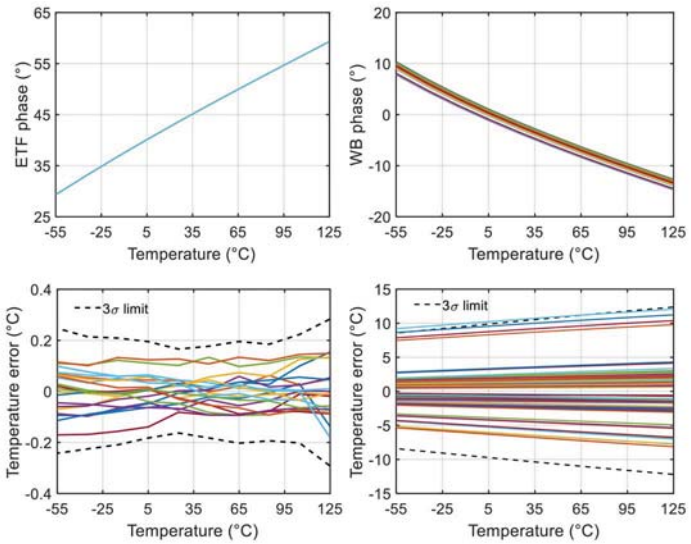

Figure 5.4.3: Phase output characteristic (top) and no-trim temperature inaccuracy (bottom) of the ETF (left, 20 samples) and WB (right, 80 samples) temperature sensors.

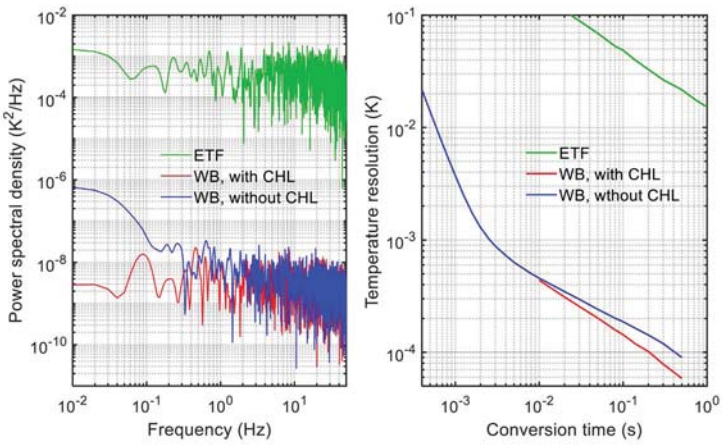

Figure 5.4.4: Power spectral densities of both sensors (left) and resolution vs. conversion time (right). The WB sensor's 1/f noise is suppressed by system-level chopping (CHL).

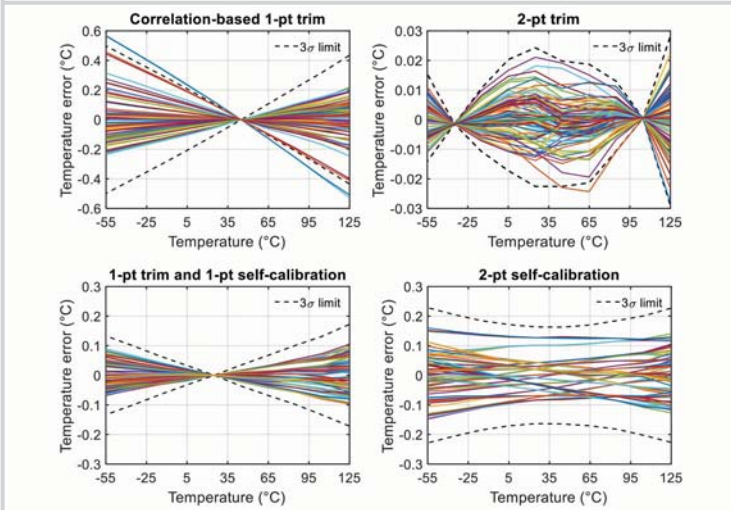

Figure 5.4.5: WB inaccuracy (80 samples) after a correlation-based 1-pt trim (top left), a 2-pt trim at -35°C and 105°C (top right), a 1-pt trim at 25°C and a 1-pt self-calibration at 85°C (bottom left), and a 2-pt self-calibration at 25°C and 85°C (bottom right).

	van Vroonhoven ISSCC'10 [1]	Souri JSSC'13 [6]	Yousefzadeh ISSCC'17 [5]	Pan JSSC'18 [2]	Pan ISSCC'19 [3]	This work	
Sensor type	Thermal diffusion	BJT	BJT	Resistor WB	Resistor WB	**Thermal diffusion**	**Resistor WB**
Technology	0.18µm	0.16µm	0.16µm	0.18µm	0.18µm	**0.18µm**	
Area [mm²]	0.18	0.08	0.17	0.72	0.12	**0.20**	
Temp. range	−55°C to 125°C	−55°C to 125°C	−55°C to 125°C	−40°C to 85°C	−40°C to 180°C	**−15°C to 105°C**	**−55°C to 125°C**
3σ inaccuracy [°C] (Temp. trimming points [a])	0.2 (0)	0.15 [b] (0)	0.3 [b] (0)	0.03 (2)	0.1 (2)	**0.2 (0)**	**0.25 (0)** / **0.03 (2)**
1/f noise corner [Hz]	--	--	<1	~1	--	**--**	**<0.01**
Power [mW]	3	0.005	0.007	0.16	0.052	**5.1**	**0.066**
Conv. time [ms]	6250	5.3	5	5	10	**1000**	**10**
Resolution [mK]	20	20	15	0.41	0.46	**15**	**0.45**
Resolution FoM [pJ·K²] [c]	7.5M	11	7.8	0.13	0.11	**1.2M**	**0.13**

[a] Trimming points that require accurate temperature information.
[b] Requires a voltage reference
[c] FoM = Energy / Conversion x (Resolution)².

Figure 5.4.6: Performance summary and comparison with previous work.

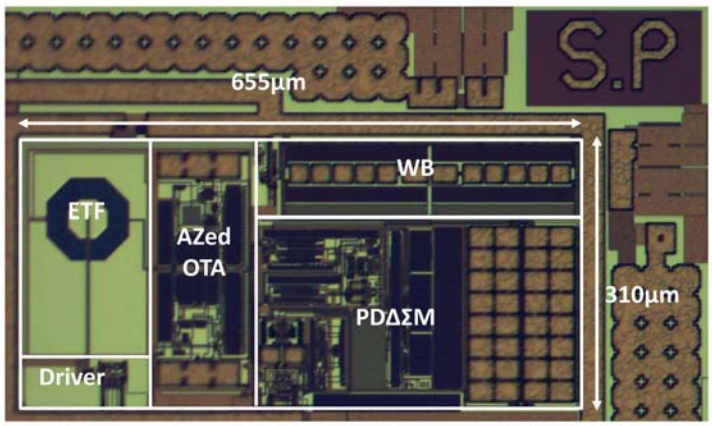

Figure 5.4.7: Die micrograph of the fabricated sensor.

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