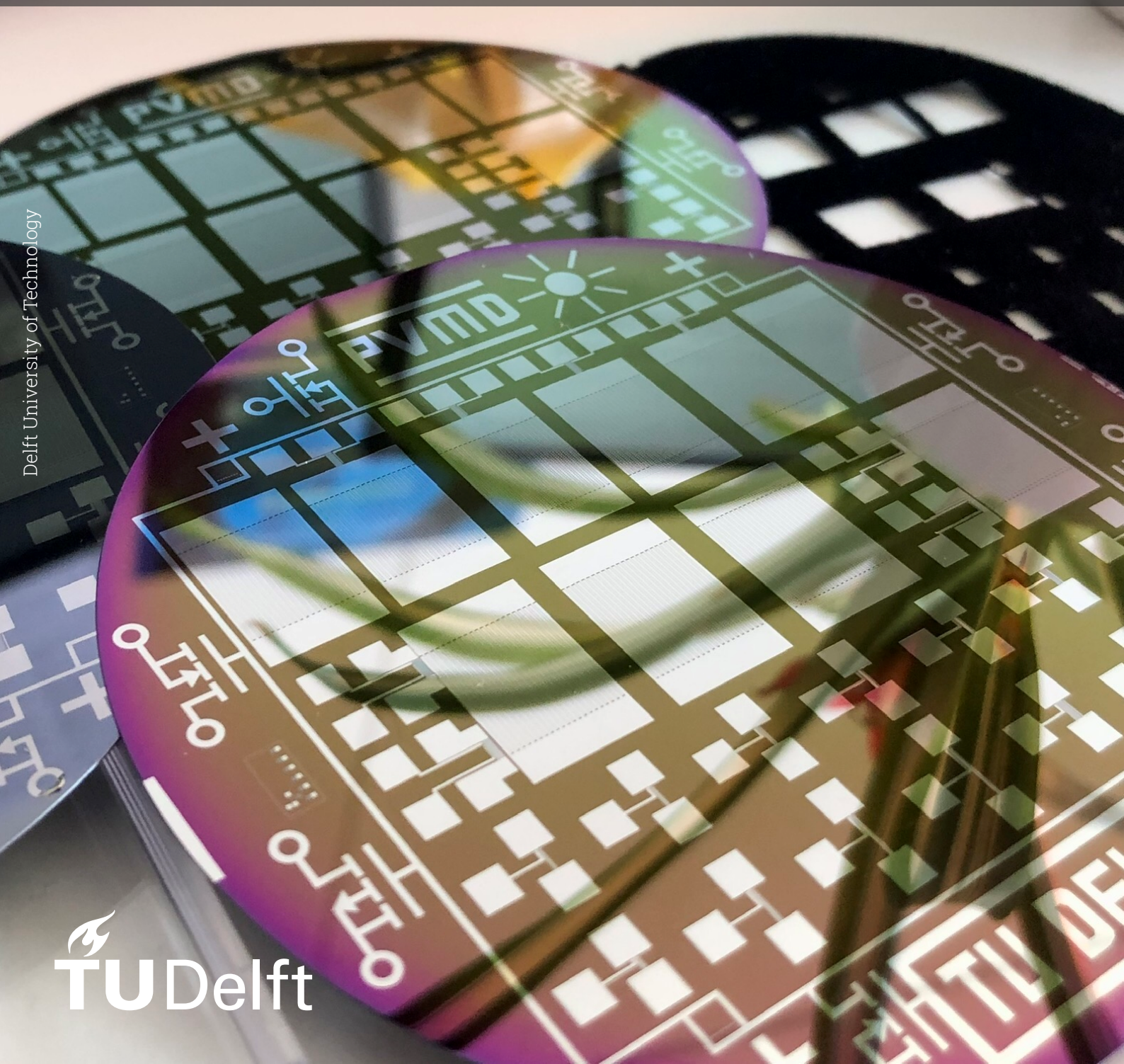
Integrating a MOSFET into a c-Si IBC Solar Cell

Tristan Stevens



Delft University of Technology

TU Delft

Integrating a MOSFET into a c-Si IBC Solar Cell

by

Tristan Stevens

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Preface

This report marks the achievement of an eight-month-long thesis project and by the same time the end of my two years of SET Master at TU Delft. Studying there has been a unique experience for me. Above the scientific knowledge I acquired, traveling outside France and meeting fellow students from all places of the world was an amazing opportunity for personal enrichment. Working on that thesis was for me an unforgettably challenging and passionate experience. Integrating a MOSFET into an IBC solar cell required me to go deeper in my knowledge of PV technology but especially to learn from the beginning about the MOSFET design and operation. Furthermore, I had the opportunity to work in cleanroom laboratories, which was a total discovery.

Although it might sound like it, a thesis is nothing but an individual project. I would thus like to thank the numerous persons without whom I would not have achieved the end of the project. The first person I want to thank is my daily supervisor, David van Nijen. The work presented in this report is a direct part of his Ph.D. project, aiming to integrate power converter components into solar cells. David has continuously supported me, showing, explaining, and commenting on every step of the project. I hope that my contribution will help him toward his Ph.D. goals. Then, my gratitude comes to my supervisor, Patrizio Manganiello. The clarifying, inspiring, and supportive meetings we had helped me define my framework and progress in my work. Both David and Patrizio demonstrated investment and availability that were crucial to me. Furthermore, I would like to thank the numerous persons who assisted me during my work in the cleanroom laboratory. Paolo Sberna, Mehmet Karaman, Hugo Schellevis, Katerina Kovačević, and Daniel van der Plaats have especially helped me several times during the project.

A special thank comes to my fellow Master's students who also had graduation projects at the PVMD. They are the reason why it was a pleasure to come every morning to the university. First, to my office mates: Maria, Rahul, Mohua, and Shloka. Shloka is one of the most hardworking people I know who managed to keep me motivated by coming early in the morning and sometimes leaving late at night. A special thank you to her and Maria who generously provided free coffee all throughout the year. Moreover, along with Shriram, Mehdi, Mathijs, Mathias, Devansh, Alex, and Anson, we all formed a special lunch team that gave super fun times. I shall not forget the support provided by my friends and housemates as well. Finally, I would like to thank my family and my girlfriend for everything they did for me before and during this Master's.

Tristan Stevens
Delft, July 2023

Summary

Several promising photovoltaic (PV) concepts are supported by transistors. Along with the growth of PV capacity in the urban environment, issues related to partial shading highlight the interest in more shade-tolerant PV systems. An example of technologies improving a PV module's energy yield under partial shading is the submodule power optimizer, including a power converter that operates sub-module maximum power point tracking (MPPT). Alternately, reconfigurable PV modules enable dynamic reconfiguration of the solar cells' interconnections to optimize the energy yield depending on the irradiance distribution. Both technologies make use of transistors as fundamental components. Integrating the latter into the solar cell wafer might be a solution for cost reduction and reliability improvement and thus support such concepts. Moreover, that kind of transistor integration can have applications in solar cell-embedded electronic and digital devices.

In this thesis, a lateral metal-oxide-semiconductor field-effect transistor (MOSFET) and an interdigitated back-contacted (IBC) solar cell are integrated into the same crystalline silicon (c-Si) wafer. A combined process flow is developed to manufacture both components with a minimum number of additional steps compared to single-component manufacturing processes. One criterion for this is a high similarity in the design of the device. Therefore, a tunneling oxide passivated contact (TOPCon) solar cell structure is used, involving polycrystalline silicon (poly-Si) at the device's backside. Similarly, the MOSFET's gate is made of a highly doped poy-Si film. Ion implantation is used as a common doping process.

Both solar cells and transistors that were manufactured with the combined process flow are first characterized separately. The highest efficiencies obtained for n-type and p-type solar cells are 20.29% and 20.66%, respectively. This is achieved thanks to multiple combined passivation approaches including TOPCon, wet poly-Si etching, a front-side hydrogenated amorphous silicon (a-Si:H) film, and hydrogenated silicon nitride on both sides of the device. Different MOSFET layouts are explored to make the device able to handle relatively large currents. It is found that introducing several drain-source pairs in parallel is more efficient than increasing the channel width to reduce the on-resistance. The on-resistance is further minimized with a gate length reduction and wet chemical poly-Si etching. As expected, the comparison of PMOS and NMOS (MOSFETs built on n-type and p-type wafers, respectively) shows better on-performance for the latter. A minimum on-resistance value of 1 Ω is then obtained. However, a higher leakage current consistently seems to come along with reduced on-resistance; i.e., higher on-performance is coupled with lower off-performance. Finally, experiments are performed combining both components. Under illumination, the MOSFET exhibits lower off-performance due to the photovoltaic effect. However, this effect does not affect the on-performance of the component. The monolithically connected components exhibit I-V characteristics that depend on the applied MOSFET's gate potential.In the on-mode, the solar cell maintains more than 95% of the conversion efficiency compared to the efficiency measured with the same solar cell without the transistor. However, a non-zero current is obtained in the off-mode, exhibiting low transistor blocking capability. Nevertheless, the large difference in characteristics obtained between the on- and off-modes proves the feasibility of integrating a solar cell and a transistor on the same substrate with a minimum number of additional processing steps.

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Nomenclature

Abbreviations

Abbreviation	Definition
:H	Hydrogenated
a-Si	Amorphous Silicon
AC	Alternative Current
ARC	Anti-Reflective Coating
AM	Air Mass
B	Boron
BHF	Buffered Hydrogen Fluoride
BJT	Bipolar Junction Transistor
BSF	Back-Surface Field
c-Si	Crystalline Silicon
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapor Deposition
DC	Direct Current
EKL	Else Kooi Laboratory
ESP	Electrical Sustainable Power
FBC	Front-Back Contacted
FSF	Front-Surface Field
HTJ	HeTeroJunction
IBC	Interdigitated Back-Contacted
IC	Integrated Circuit
IEA	International Energy Agency
LCOE	Levelized Cost Of Electricity
LPCVD	Low-Pressure Chemical Vapor Deposition
MEMS	MicroElectroMechanical Systems
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MSE	Mean Square Error
NAOS	Nitric Acid Oxidation of Silicon
NMOS	p-type MOS
OSC	Organic Solar Cell
PE	Power Electronics
PECVD	Plasma-Enhanced Chemical Vapor Deposition
Ph	Phosphorus
PMOS	n-type MOS
poly-Si	Poly-crystalline Silicon
PV	Photovoltaic
QSSPC	Quasi-Steady State PhotoConduction
SE	Spectroscopic Ellipsometry
Si	Silicon
SiO_x	Silicon Oxide
Si_xN_y	Silicon Nitride
SRH	Shockley-Read-Hall
STC	Standard Test Conditions

Abbreviation	Definition
TMAH	TetraMethylAmmonium Hydroxide
TOPCon	Tunnel Oxide Passivated Contact
UV	Ultraviolet

Symbols

Symbol	Definition	Unit/Value
A	Area	[m^2]
C	Capacitance	[F]
E_C	Conduction energy	[eV]
E_V	Valence energy	[eV]
E_F	Fermi energy	[eV]
E_g	Bandgap energy	[eV]
E_{ph}	Photon energy	[J]
FF	Fill factor	[-]
G	Irradiance	[W/m^2]
g_m	Transistor gain	[Ω^{-1}]
I_D	Drain current	[A]
I_{MP}	Maximum power current	[A]
I_{SC}	Short-circuit current	[A]
L	Gate length	[μm]
P_{in}	Input power	[W]
P_{MP}	Maximum power	[W]
Q'_{SD}	Inversion layer charge surface density	[C/m^2]
Q'_{SD}	Equivalent oxide charge surface density	[C/m^2]
R_{ON}	ON-resistance	[Ω]
t	Time	[s]
t_{ox}	Oxide thickness	[nm]
V_{bi}	Built-in voltage	[V]
V_{DS}	Drain-source voltage	[V]
V_{GS}	Gate-source voltage	[V]
V_{MP}	Maximum power voltage	[V]
V_{OC}	Open-circuit voltage	[V]
V_T	Threshold voltage	[V]
$V_{T(N/P)}$	(N/P)MOS threshold voltage	[V]
W	Gate width	[μm]
θ	Angle	[°]
λ	Wavelength	[nm]
η	Efficiency	[%]
$\mu_{n/p}$	Electron/hole mobility	[cm^2/(V.s)]
ϵ_{ox}	Oxide permittivity	[F/m]
$\phi_{f(p/n)}$	Intrinsic-(p/n)type Fermi level difference	[V]
ϕ_{ms}	Metal-semiconductor work function difference	[V]
τ	Lifetime or duration	[s]
c	Light celerity	3.10^8 m/s
h	Planck's constant	$6.626.10^{-34}$ J.s

1

Introduction

1.1. An Energy-Dependant Society

Our modern industrialized society experiences exponential global growth. In 1972, Meadows et al. analyzed trends in major categories, namely the world population, food, industry, capital, and non-renewable resources consumption, and concluded that their growth would eventually hit the physical world limits, leading to a collapse of society before 2100 [1]. These five sectors have in common a direct or indirect need for energy to develop. Hence, one observes an increase in energy production, regardless of the resource, as shown in Figure 1.1. The latter displays the global energy production evolution, from 1971 to 2019, according to the International Energy Agency (IEA) [2]. Despite the growth of nuclear and renewable energies, fossil fuel-based energies (coal, oil, and natural gas) have always dominated more than 80% the global energy production. However, it causes important emissions of greenhouse gases, altering the climate and thus threatening the conditions that make human life possible in many areas on Earth [3].

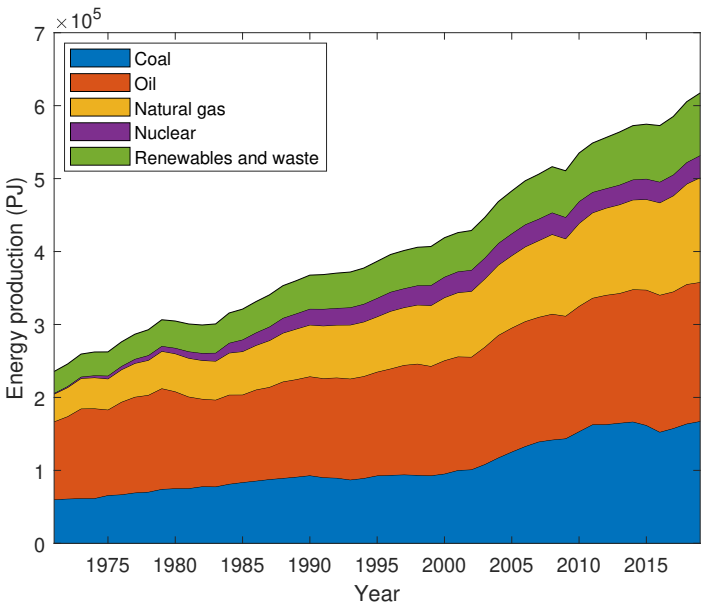


Figure 1.1: Simplified global energy production per energy resource from 1971 to 2019 [2].

The need to tightly reduce fossil fuel consumption is thus motivated by both the finite amount of such non-renewable natural resources and limiting climate change. To that end, the United Nations has defined a set of 17 goals for sustainability, among which the one for affordable and clean energy. That goal includes the target of increasing substantially the share of renewable energy in the global energy

mix by 2030 [4].

1.2. Solar Energy Potential

Solar energy is one form of renewable energy, consisting of converting the Sun's radiation into electricity or heat. According to Perez et al., that source has, by far, the highest energy yield potential among all forms of energy sources [5]. Figure 1.2 shows that solar energy received by emerged continents only has an energy production potential of 23000 TW-yr/year, much higher than the World energy use, which is 16 TW-yr/year.

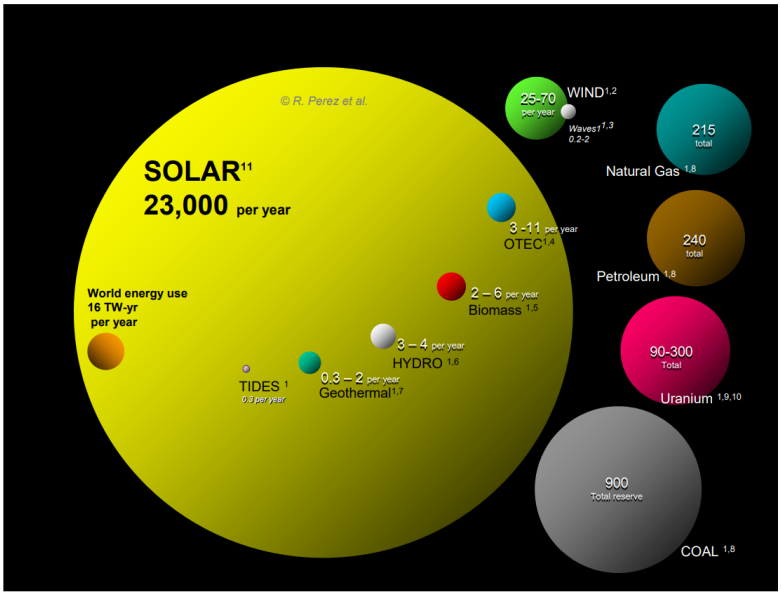


Figure 1.2: Comparing finite and renewable planetary energy reserves (Terawattyears). Total recoverable reserves are shown for finite resources. Yearly potential is shown for the renewables [5].

Another advantage of solar energy over the other forms of energy is the low cost. According to the Fraunhofer Institute, the levelized cost of electricity (LCOE) of photovoltaics (PV) was among the lowest LCOEs in Germany in 2021. As depicted in Figure 1.3, large PV systems (at utility-scale) produce the cheapest electricity among all the different types of renewable energy and conventional power plants. Including batteries and reducing the PV system size increase the LCOE; however, even in the most expensive case (small PV system on rooftops with a battery), it competes with most of the electricity generated from fossil fuels. Worldly, the global weighted average LCOE was 0.041 €/kWh. That value has decreased by about 17% on a year-to-year basis in the last 11 years [6]. Along with the LCOE decrease, global PV installation increases at an accelerating pace. Hence, according to the International Renewable Energy Agency (IRENA), the World PV generation was 1,047 GW in 2013, against 137 GW in 2022 [7].

1.3. Power Electronics in Solar Systems

Power electronics (PE) plays a major role in the operation of photovoltaic (PV) systems. One of the main applications of PE is maximum power point tracking (MPPT), using a DC-DC converter. Since the PV current-voltage characteristic depends on variable parameters such as solar irradiance and temperature, the voltage for which the output power is maximum needs to be adjusted constantly. MPPT optimizes the power output of the PV system. To do so, the DC-DC converter regulates the input and output voltage ratio via a high-frequency switch that operates according to a duty cycle controlled by an algorithm [9]. Another fundamental application of PE is converting the direct current (DC) produced by the solar panels into an alternating current (AC) through DC-AC converters, also called inverters. This is necessary for grid-connected PV systems, which represent more than 99% of the overall worldwide PV installations [10]. Along with the recent rapid growth of the PV capacity through several sizes of PV systems [7], a large variety of PE architectures in PV systems have been developed. The inverter topol-

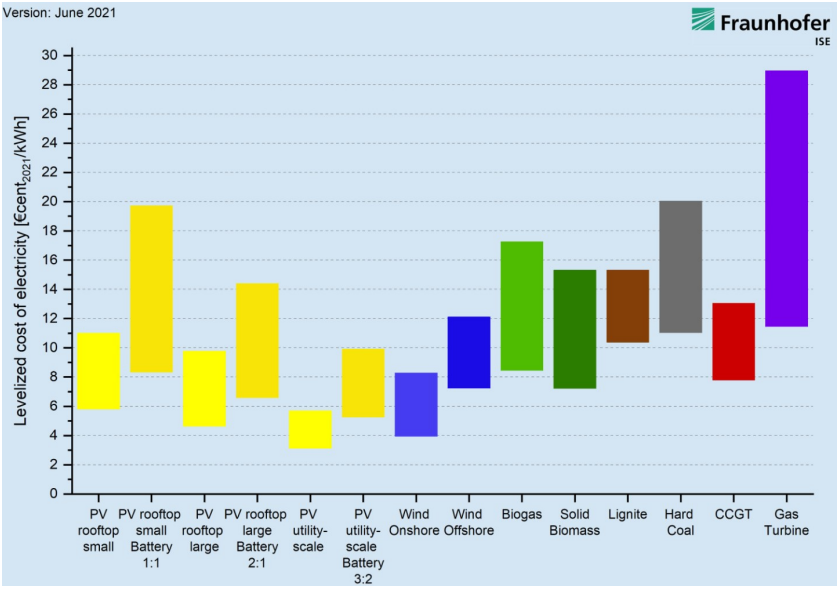


Figure 1.3: LCOE of renewable energy technologies and conventional power plants at locations in Germany in 2021 [8].

ogy is classified following the scale of the PV system to which it is connected. String and multi-string inverters are connected to one and several strings of PV modules (series connected PV modules), respectively; central inverters work with PV arrays (parallel connected strings); module inverters or micro-inverters are adapted to one or a few PV modules [10]. Figure 1.4 illustrates an example of inverter unit for residential use [11]. It includes for MPPT a type of DC-DC converter, called boost converter, and a PWM bridge for DC to AC conversion. A data interface monitors the whole conversion process.

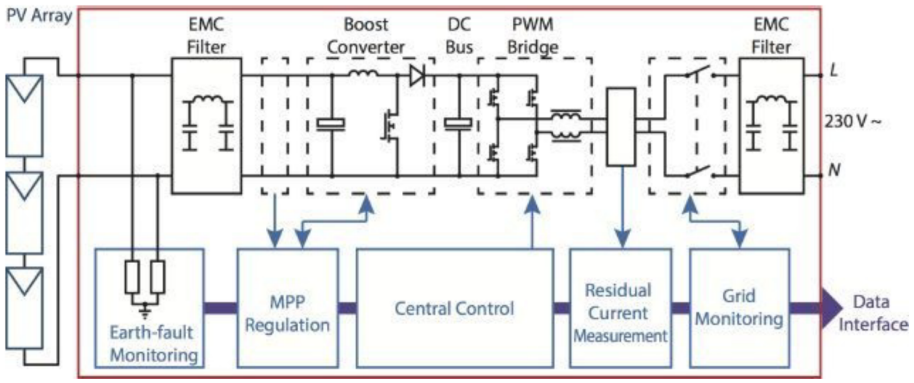


Figure 1.4: An example of a transformer-less inverter unit as could be used for residential PV systems [11].

Several criteria must be taken into account to correctly choose the topology and size of the PV system inverter, usually requiring a cost-benefit analysis [12]. Generally, one seeks consequent energy harvesting and minimum cost. Location-related irradiance non-uniformity and partial shading scenarios affect the former point. If modules of one string are unequally irradiated, the string current is typically limited by the one from the least irradiated module. The power output of the modules with higher irradiation is thus lower than at their maximum power point. Consequently, while central inverters are preferable for PV arrays subjected to a uniform irradiance thanks to their higher efficiency and low cost, smaller-scale inverters can be preferable for systems that suffer from non-uniform irradiance or partial shading and hence need to be more resilient [10]. For small PV systems surrounded by an urban environment, MPPT with higher granularity is necessary. This can be done by either implementing more DC-DC converters or smaller inverters such as module inverters, forming so-called AC modules [13].

However, partial shading can also occur at a module scale. Since PV modules generally include single strings of series-connected solar cells, non-uniform irradiance or minor partial shading on one cell reduces the string current, hence a reduced global output power. If the cell is more severely shaded, the string current mismatch results in that cell consuming the energy produced by the unshaded other cells. The problematic cell thus achieves a high reverse voltage that can cause a breakdown, which in turn causes local overheating that can imply irreversible damage. Besides, the whole string does not produce any output power [11, 14]. Partial shading effects are generally limited by separating solar cell strings into several substrings, each containing one bypass diode [10, 15]. Consequently, if a substring is shaded, the current flows through the related bypass diode to not perturb the unshaded substrings. However, the three-bypass-diodes architecture results in the power loss of one-third of a module in the case of only one partially shaded cell. Another drawback is that modules containing many high-efficiency solar cells still can reach very high temperatures if only three bypass diodes are used [15]. Several alternative approaches aim to increase the partial shading tolerance of PV modules. The first idea is introducing more bypass diodes, shortcutting either a smaller group of cells or even one single cell [16]. A second possible solution is to introduce submodule power converters. In [17], Leuenberger et al. propose AC modules integrating three parallel substrings DC-DC converters to proceed in submodule MPPT. The investigated topology reveals an achievable efficiency of 94.5% using high-performance electronic devices. Besides improving the partial shading resilience of PV modules in an urban environment, module-embedded PE can boost a solar farm's energy production per land area. [18] introduces submodule MPPT to allow resilience to PV array interrow shading. Consequently, the distance between rows can decrease, hence a better ground-cover ratio. Finally, a third approach is a reconfigurable series-parallel PV module architecture. The idea is to keep the cells fully connected in series for current minimization when the module is unshaded and switch to a parallel connection of solar cell strings when shading occurs. Calcabrini et al. have investigated and module topology of 6 reconfigurable blocks of solar cells and found that it can increase the energy yield by 12.7% compared to a module with 6 bypass diodes, for a module shaded 32% of the time [19].

However, all these latter approaches need the integration of PE components that is not yet optimal. They are usually included in the junction box, or laminated or mounted to the module frame. One drawback is then an increased wiring complexity [20]. Solar cell-embedded electronic components appear to be a promising solution that can facilitate further implementation of PE in PV. Above the less bulky integration and simpler wiring that help the device be more portable, the reliability can be improved. Although integrated components are less accessible and thus less replaceable, integrated components into the cell can allow monolithic electrical connections instead of solder joints. The latter is one main cause of failure in transistors [21, 22], which have today the most critical reliability of the power converter [23]. In turn, the latter has the lowest lifetime of the PV system [24]. Another argument is the potential cost reduction. Integrating a power converter into cells avoids the installation cost of such a device in the PV system, usually separated from the modules. In proportion, the fraction of a PV system cost related to this cost has recently increased due to the important cost decline in PV panels [10]. Manufacturing electrical components and a solar cell on the same substrate could also reduce production costs. However, for this, the manufacturing processes of the solar cells and the electrical components must be similar to minimize the number of necessary additional processes to build such a device. Solar cell-embedded PE components can support the integration of power converters that work for a small number of cells, hence increasing the MPPT granularity and making PV systems more shade resilient. Finally, besides PE, integrating electronic components such as diodes and transistors can have applications for modern cell-level bypass circuits, which aim to replace simple diodes to reduce power losses [16, 25].

To the best of the author's knowledge, solar cell-integrated components of power converters have been little explored. Shawly et al. have developed a complete on-chip cell-level MPPT system, including a DC-DC converter and a Ripple Correlation Control circuit that controls the converter [26]. However, this integrated circuit (IC) is not built on the same substrate as the solar cell. Imtiaz et al. have made efforts towards integrating power transistors, inductors, capacitors, and diodes on solar cells [27]. Nevertheless, this thesis is based on the work of van Nijen et al., who explored the integration of power converter components into c-Si solar cells and considered ease of integration as an essential criterion [28]. That work explores solar cell native capacitance and inductance as potential components for a

power converter. Diodes can easily be integrated thanks to their very similar structure to solar cells and mature research on that subject [29]. Finally, the transistor may be the least similar component to solar cells, and one must closely investigate its integration.

1.4. Integration of a Transistor

This thesis specifically focuses on integrating a transistor into a solar cell. Combining both components on a single c-Si-based device has recently been explored, especially from integrating a solar cell into ICs perspective, giving the name of on-chip solar cells [30–34]. Most of these works are based on the structure of complementary metal oxide semiconductor (CMOS) technologies, being similar to one of the solar cells, both involving PN junctions. This similarity was already exploited decades ago, as Mouthan fabricated integrated cascade micro-solar cells on ICs in 1984 [30]. More recently, concrete applications of on-chip solar cells emerged with the growing interest in the Internet of Things, which connects real and virtual objects which perform machine-to-machine communication [35]. Micro-solar cells are thus on-chip integrated to harvest energy for digital devices, as done by Ghosh et al. [31], Steffan et al. [32], and Zenibayashi et al. [33], who also use the solar cell as a light signal sensor for communication. These solar cells have the structure of CMOS chips. Hence, despite the advantage of not adding and processing steps in chip IC manufacturing, they are not optimized for energy harvesting. Besides, it is worth noting that these structures are adapted to very low energy production levels since these digital devices consume little power.

Organic materials can also be adequate solutions for combining both components. Organic semiconductors having a delocalized π electron system are known to support organic solar cells (OSCs) [36] and organic transistors [37]. Multiple semiconducting polymer materials have been synthesized, resulting in electronic properties allowing to have applications in both organic field-effect transistors and OSC [38, 39]. It is thus possible to imagine a device based on such material and receiving different local treatments to create solar cells and transistors on the same organic wafer. The advantages of using organic materials are the low-cost synthesis and easy manufacturing processes. The very large flexibility in shape, orbitals, energy levels, and electron densities offered by polymers make this material very promising for OSCs. However, they are still an immature technology facing several issues, such as still low power conversion efficiency, non-adapted absorption spectra, short exciton diffusion distance, and short lifespan [40]. Likewise, despite rapid development in the past decades, organic transistors still face challenges to achieving realistic applications in daily life [37]. In this thesis, the maturity of existing technologies is essential to focus on their combination. Therefore, organic materials are not further explored here.

For this reason of necessary maturity, we aim to integrate the transistor into a c-Si solar cell. The arguments supporting the choice of the transistor and solar cell provided in this paragraph are raised in more detail by van Nijen et al. [28]. One must here distinguish the two main architectures of c-Si solar cells. First, the front-back contacted (FBC) solar cells, which are the most usual ones, include metal contacts at both the top and bottom sides of the device. Second, the interdigitated back-contacted (IBC) solar cells carry positive and negative metal contacts on the backside of the cell only. Depending on these architectures, different transistor types are best suited for integration into the same c-Si wafer. For FBC cells, since the positive and negative metal contacts have opposite sides, vertical transistors, which also contain terminals at both sides of the wafer, are more easily integrable. IBC cells can more easily integrate lateral transistors, which hold all their terminals on the same side. Most transistors adopted for power converters are power transistors, which are vertical components. However, their architectures have many differences from FBC solar cells, and embedding them would thus require a significant number of additional processing steps. On the contrary, lateral transistors such as the metal-oxide-semiconductor field-effect transistor (MOSFET) and the bipolar junction transistor (BJT) would require few additional processing steps as compared with the manufacturing method of an IBC solar cell. MOSFETs have the advantage over BJTs to perform correctly until a higher limiting switching frequency, the latter being an important criterion for power converter applications. Another advantage is the nature of transistor control: while the BJT is a current-controlled device, the MOSFET is voltage-controlled, allowing for lower losses.

Consequently, it is chosen for this thesis to integrate a MOSFET on an IBC solar cell. More specifically, the solar cell involves a tunnel oxide passivated contact (TOPCon) structure, which is chosen for its proven high efficiency and close structural similarity with the MOSFET design [41]. Before this work, Yavuzhan Mercimek optimized the MOSFET size for solar cell integration and manufactured the component with processes used for TOPCon IBC solar cell manufacturing [42]. The challenge is now to manufacture these two components with a minimum number of processing steps while still having satisfying solar cell and transistor performances.

1.5. Research Questions and Report Outline

The objective of this Master's thesis is to carry out a combined fabrication of both an IBC solar cell and a MOSFET on one substrate and to characterize them. To explore different possibilities and hence allow a better understanding of their behavior, we use both n-type and p-type substrates, and both components can be either connected or characterized separately. The project aims to answer the following research questions:

1. How does integrating both components on the same substrate simultaneously affect their performance?
2. How does the doping nature (n- or p-type) of the substrate affect the performance of both components?
3. How does illumination affect the MOSFET performance?
4. How do the monolithically interconnected components perform, compared to separated ones?

The following outline is used in this report to address these questions. Firstly, this chapter provided context and motivation for the research. Secondly, chapter 2 provides the necessary theoretical knowledge to understand the physics and technologies involved. Then, fabrication and measurement methods are described in chapter 3. Measurement results are provided as follows: chapter 4 refers to the characterization of the solar cell; chapter 5 provides an analysis of the MOSFETs; chapter 6 presents the behavior of the MOSFET in illuminated condition and related to solar cell and MOSFET characterization, respectively. Finally, chapter 7 concludes the work and discusses the potentials, challenges, and limitations of the investigated combined fabrication for further applications.

2

Solar Cell and MOSFET Theory

This chapter aims to provide theoretical insight into the technologies studied in the thesis, namely the IBC solar cell and the MOSFET. Fundamental physical mechanisms, design, and parameters are described for both components. First, section 2.1 provides a basis for both technologies by introducing the semiconductor. Next, sections 2.2 and 2.3 describe the solar cell and the MOSFET, respectively.

2.1. Semiconductors

The semiconductor is a material from which many technologies emerged in the 20th century, including solar cells and transistors. It is introduced in this section, first in subsection 2.1.1 by defining essential concepts, then in subsection 2.1.2 by introducing the p-n junction, and in subsection 2.1.3 describing charge carriers' generation and recombination. Unless otherwise stated, all the content given in this section derives from the book *Semiconductor Physics and Devices: basic principles*, by Neamen [43].

2.1.1. Definition

Semiconductors are solid-state materials having an electrical conductivity higher than insulators and lower than metals. In both PV and IC industries, silicon (Si) is by far the most used semiconductor material for reasons including its high abundance [44]. In this thesis, the study focuses on Si material. Crystalline and poly-crystalline semiconductors have ordered atomic structures with a lattice having the dimensions of the whole solid and many atoms, respectively. On the contrary, amorphous semiconductors do not have an atom structure.

Atoms of Si have 4 valence electrons, orbiting around the nucleus and creating covalent bonds with neighboring atoms. If they have enough energy, valence electrons can move from one atom to another, thus breaking the covalent bond. This process would create a lack of electrons, called "holes", around the first atom and electron excess around the second atom. This free electron with such high energy is able to conduct electricity; hence, it is called a "conduction electron". Both holes and conduction electrons are charge carriers. Their energies belong to specific ranges: while holes belong to the valence band, conduction electrons belong to the conduction band. These bands are sketched in Figure 2.1(a). The figure also includes the conduction energy E_C and the valence energy E_V, which are the lowest energy of the conduction band and the highest energy of the valence band, respectively. Between these two energy levels, is located the bandgap, which is a forbidden band for charge carriers. The range of this bandgap is:

$$E_g = E_C - E_V \tag{2.1}$$

The Fermi energy E_F is the energy below which all states are filled with electrons and above which all states are empty at T = 0 K.

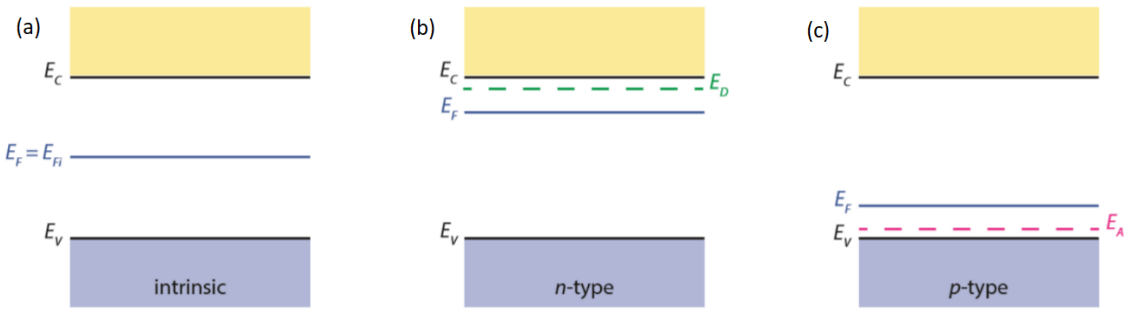


Figure 2.1: Energy band diagram for: (a) intrinsic semiconductor; (b) n-type doped semiconductor; (c) p-type doped semiconductor [11].

Figure 2.1(a) shows the case of an intrinsic semiconductor, i.e., a semiconductor without doping. Contrarily, a doped semiconductor has a fraction of the native atoms replaced by atoms (dopants) possessing another number of valence electrons. It creates a lack or surplus of electrons. Consequently, the Fermi level value changes, so there are more conduction electrons and fewer holes, or vice versa. In n-type semiconductors, the dopant has 5 valence electrons, such as phosphorus (Ph), so conduction electrons are more numerous, and the Fermi level is higher. Inversely, in p-type semiconductors, the dopant has 3 valence electrons, such as boron (B), so holes are more numerous, and the Fermi level is lower. Figure 2.1(b) and (c) sketch n-type and p-type energy band diagrams, respectively. In the following, conduction electrons will be simply called electrons.

2.1.2. The P-N Junction

A p-n junction is the metallurgical junction of p-type and n-type semiconductors. Figure 2.2(a) displays the energy diagram of such a junction without applied bias. Three regions are distinguished: the p-type and the n-type semiconductors, respectively on the left and the right, and a depletion region in the middle. Since no bias is applied, the Fermi level is constant; hence, the conduction and valence levels are higher in the p-type than in the n-type material. The energy difference is proportional to the built-in voltage V_{bi}. A depletion region, free of charge carriers, is formed at the interface between the p- and n-type materials. Consequently, an electric field is created, justifying the slope of E_C and E_V in the figure. In Figure 2.2(b), a negative voltage is applied to the p-type region, corresponding to a reverse bias voltage at the junction. It results in a difference between the Fermi levels, an increased conduction and valence levels variation, and an increased depletion region width. In Figure 2.2(c), a positive voltage is applied to the p-type region, corresponding to a forward bias voltage, hence a reduction of the energy level variation, and a decreased depletion region width.

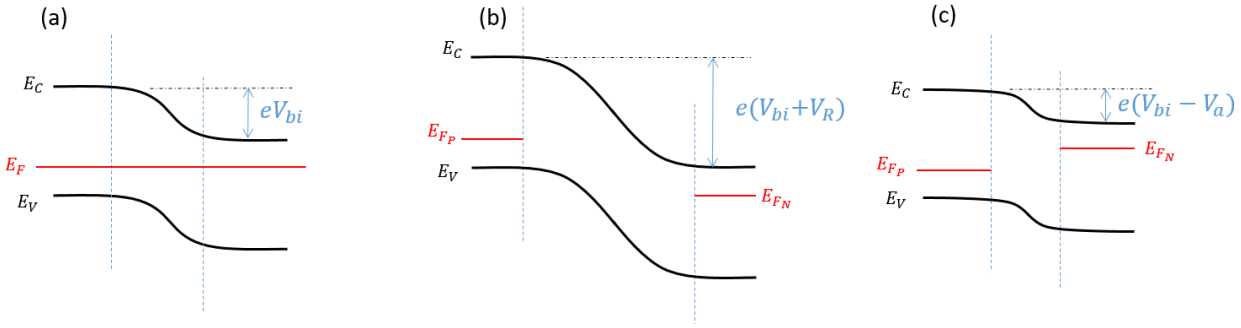


Figure 2.2: Energy band diagrams of a p-n junction for (a) zero bias; (b) reverse bias; (c) forward bias.

Charge carriers displace from one side of the junction to another according to two antagonistic mechanisms. Firstly, drift is the transport of charge carriers subjected to an electric field. It implies electrons and holes present in the depletion region move from the p- to the n-side and from the n- to the p-side, respectively. Secondly, diffusion is the transport of charges due to a concentration gradient. It implies the electrons and holes move from the n- to the p-side and from the p- to the n-side respectively. When

no bias is applied, the thermal equilibrium is achieved, and both mechanisms compensate for each other. Consequently, no current is globally observed. If a positive voltage is applied to the p-type region, diffusion dominates; hence, a current flows through the junction.

2.1.3. Charge Carrier Generation and Recombination

Generation and recombination are defined by the creation and the annihilation of an electron-hole pair, respectively. At the thermal equilibrium, generation is only due to thermal effects and is compensated by recombination. Outside thermal equilibrium conditions, excess carriers are generated, by external forces such as illumination. These carriers then recombine after a random time, the average of which, called the minority carrier lifetime, is a parameter of the recombination rate. The lifetime also affects the diffusion length, defined by the mean free path the charge carriers browse before recombining. Recombination can be due to different mechanisms [11]:

- *Radiative and direct recombination* mechanisms are prominent for direct semiconductors but negligible for semiconductors with an indirect band gap. A semiconductor is indirect if a hole at the valence energy does not have the same crystal momentum as an electron at the conduction energy. Silicon is an indirect semiconductor; hence, these mechanisms are not significant.
- *Shockley-Read-Hall (SRH) recombination* is a process in which the electron-hole pair recombines at an energy level, called 'trap state', belonging to the bandgap. Such trap states are present due to impurity atoms in the crystal.
- *Auger recombination* is a mechanism involving 3 carriers. As an electron recombines with a hole, the energy and momentum transfer to a third particle, which can either be a hole or an electron. Depending on the semiconductor quality, SRH or Auger recombinations can be dominant for indirect semiconductors such as c-Si.
- *Surface recombination* occurs at the surface of the material. If the crystal abruptly ends, the atoms at the surface cannot create 4 covalent bonds; hence, dangling bonds appear instead. These dangling bonds are defects and cause the creation of trap states. As well as for SRH recombination, these trap states cause recombination.

2.2. Photovoltaic Technology

This section introduces PV technology, from fundamental concepts to the technology used in this thesis. First, subsection 2.2.1 introduces the sun's radiation. The solar cell is then introduced, first with subsection 2.2.2, explaining its fundamental physical mechanisms, then with subsection 2.2.3, presenting the external parameters, and with subsection 2.2.4, introducing crystalline silicon (c-Si) solar cell. Finally, subsection 2.2.5 focuses on the interdigitated back-contacted solar cell, which is the technology used in this thesis. Unless otherwise specified, all the content of this section is available in *Solar energy: the physics and engineering of photovoltaic conversion, technologies, and systems*, by Smets et al. [11].

2.2.1. Solar Radiation

The Sun can be approximated by a blackbody model, with a surface temperature of roughly 6000 K. In Figure 2.3, the back curve shows the spectral irradiance of such a perfect blackbody, while the blue curve shows the "AM0 radiation", meaning the measured Sun radiation received at the top of the Earth's atmosphere. Finally, the orange curve shows the "AM1.5 radiation", considered as the standard reference for solar cell efficiency measurement. The differences between the blue and the orange curves result from some parts of the spectrum absorbed by the atmosphere and the orientation of the surface of the Earth. AM1.5 is verified when:

$$\frac{1}{\cos\theta} = 1.5 \tag{2.2}$$

With θ the angle between the Zenith and the direction of the Sun. If the Sun is at the Zenith, i.e., $\theta = 0$, AM1 is verified, and the amplitude of the spectral irradiance is larger. The quantum theory considers that elementary particles of light, called photons, behave as both a wave and particles. Each photon carries energy, which is inversely proportional to the wavelength, as written in Equation 2.3, with λ the wavelength, h the Planck's constant, and c the light celerity.

$$E_{ph} = \frac{hc}{\lambda} \tag{2.3}$$

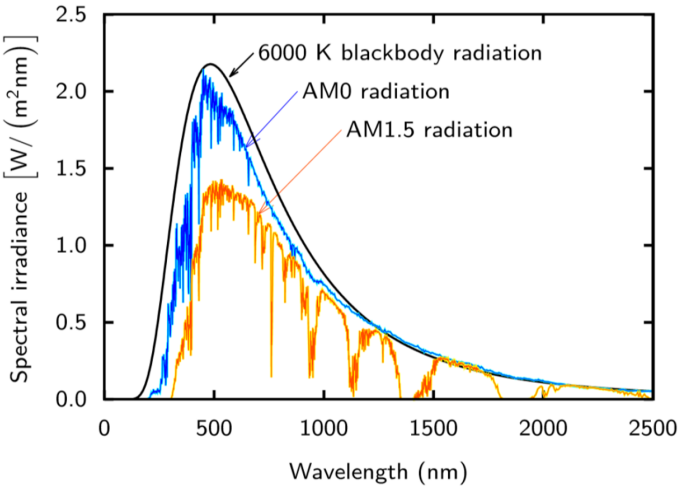


Figure 2.3: Solar spectrum [11].

2.2.2. Working Principle of a Solar Cell

A solar cell, also called a PV cell, is an electronic device that converts the energy of the light directly into electricity by the photovoltaic effect [45]. To do so, 4 fundamental mechanisms successively occur:

1. Absorption of a photon by the semiconductor. Competing mechanisms can also occur, such as reflection and transmission, limiting absorption. To restrain reflection, solar cell top surfaces are usually textured and coated by a layer with a specific thickness and refraction index such that the reflection coefficient is minimum. To decrease transmission, the semiconductor substrate thickness can be increased.
2. Creation of an electron-hole pair from the absorbed photon. It can only happen if the energy of the photon is higher than the semiconductor bandgap:

   $$E_{ph} \geq E_g \tag{2.4}$$

   According to this equation and Equation 2.3, the wavelength must be small enough. For c-Si, at 300 K, the bandgap is 1.12 eV. Consequently, only photons with a wavelength lower than 1107 nm can cause the creation of charge carriers. The part of the solar spectrum above that value is thus lost; Si is then transparent. On the other hand, if the inequation is valid, i.e. the photons contain more energy than the bandgap energy, charge carriers lose the energy difference $E_{ph} - E_g$ through thermalization; hence, only E_g eventually converts into electricity. Transparency and thermalization are prominent causes explaining the overall solar cell efficiency. Higher efficiency PV technologies involve several semiconductor materials to take advantage of several bandgaps and thus reduce transparency and thermalization impacts. Such technologies are called multi-junction solar cells.
3. Separation of the electron-hole pair at the p-n junction. According to the mechanisms described in subsection 2.1.2, holes and electrons flow in opposite directions that depend on the applied voltage. Charge carriers must be separated as much as possible to avoid recombination mechanisms, as described in subsection 2.1.3. Ideally, the junction should be as close to the pair creation location as possible. Consequently, the choice of the semiconductor substrate thickness must take the diffusion length into account.
4. Collection of the carriers at the electrodes. One thus has to ensure that low surface recombination occurs at the metal-semiconductor interface.

2.2.3. Solar Cell External Parameters

To characterize the electrical performance of solar cells, external electrical parameters are defined in this section. Figure 2.4 illustrates typical I-V and P-V curves of a solar cell. In this figure, the short-circuit current I_{SC} is the current obtained at zero voltage, and the open-circuit voltage V_{OC} is the voltage corresponding to a zero current. The maximum power point (MPP) is the point (V_{MP}, I_{MP}) of the I-V curve for which the power created by the solar cell $P_{MP} = V_{MP} \times I_{MP}$ is maximum.

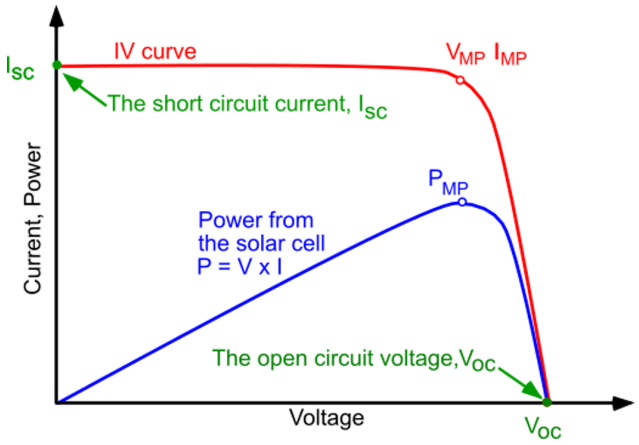


Figure 2.4: Solar cell I-V and P-V curves [46].

For high solar cell performance, the MPP must be as close to (V_{OC}, I_{SC}) as possible. However, this is not possible because a dark current flowing in the opposite direction compared to the photocurrent inevitably increases with the voltage. To quantify the difference between the real and the ideal situations, the fill factor FF is defined as:

$$FF = \frac{V_{MP} \cdot I_{MP}}{V_{OC} \cdot I_{SC}} \tag{2.5}$$

The value of FF is always lower than 1. The solar cell receives power from the light. The input power P_{in} is the product of the solar cell area A_{cell}, and the irradiance G. As a result, the solar cell efficiency is:

$$\eta = \frac{P_{MP}}{P_{in}} = \frac{I_{SC} \cdot V_{OC} \cdot FF}{A_{cell} \cdot G} \tag{2.6}$$

In laboratories, the solar cell efficiency is measured using Standard Test Conditions (STC). Under STC, the light must have a AM1.5 radiation spectrum, with as irradiance of G = 1000 W.m^{-2}. The solar cell must have a temperature of 25 °C.

2.2.4. Crystalline Silicon Solar Cell

c-Si solar cells are a type of solar cell responsible for about 95 % of worldwide PV production [6]. They are constructed from n- or p-type c-Si wafers, also called a ”substrates”. The front-back contacted (FBC) solar cell is the most usual architecture of c-Si. Figure 2.5 shows the basic schematic of such a cell based on a p-type wafer. The latter is below a thin layer of highly doped n-type c-Si, called an ”emitter”. Both surfaces allow the creation of a p-n junction at which the charge carriers can separate. Since the wafer is p-type, the front contact collects the electrons at the top. However, because the light comes from the top, that contact is a metal grid designed to minimize optical losses. An antireflective coating (ARC) layer is also present at the top to minimize the optical losses that are due to reflection. At the back surface, a thin and highly doped p-type layer called the ”back surface field” (BSF), is situated below the wafer and ensures that electrons are repelled from the back. Beneath it, the back contact collects the holes. The overall thickness of the cell is chosen to limit recombination but still absorb as much light as possible.

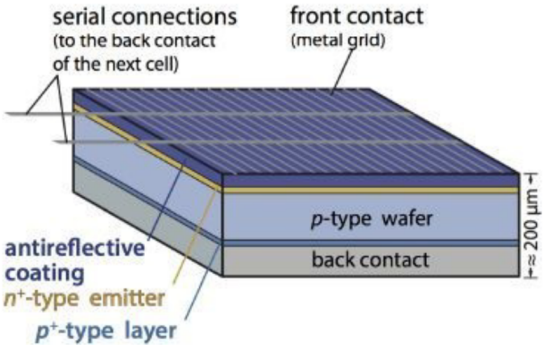


Figure 2.5: Scheme of an FTC crystalline silicon cell, with a p-type wafer [11].

2.2.5. Interdigitated Back-Contacted Solar Cell

This thesis focuses on interdigitated back-contacted (IBC) solar cells, which are among the promising high-efficiency c-Si solar cell technologies [47]. Figure 2.6(a) illustrates the structure with the example of an n-type substrate. The latter is the central layer, expected to absorb the photons that come from the top and generate the carriers. Under this, comes an alternation of highly doped n- and p-type silicon materials, forming the BSF and the emitter, respectively. The resulting p^+-n and n^+-n junctions allow the separation of the charge carrier pairs, as the holes and the electrons flow towards the emitter and the BSF, respectively. Metal contacts then collect the charge carriers and transfer them to the backside electrodes. The main difference between IBC and FBC is that all the charge carriers are collected at the back of the cell, avoiding inevitable shading losses caused by the front metal grid in FBC solar cells.

Other optical losses are minimized by an ARC and texturing that reduce the reflectance. A backside mirror reflecting the unabsorbed photons to reduce the wafer's transmittance can also be introduced. Electrical losses are kept low by reducing recombination rates. Passivating layers are present to avoid surface recombination. Surface passivation treatment consists of the thin film of a material that can restore the bonding environment at the semiconductor surface to avoid dangling bonds [48]. For c-Si, the main passivation materials are silicon oxide (SiO_x), silicon nitride (Si_xN_y), or hydrogenated amorphous silicon (a-Si:H). One passivation layer is at the top of the cell. On the backside, passivation must restore the c-Si substrate bonding environment and keep the semiconductor-metal interface small to reduce the undesired recombination at this defect-rich interface. In Figure 2.6, both requirements are met by one passivation layer between the BSF/emitter and the electrodes, containing small openings that allow metal contact. Alternatively, the passivation layer can be between the substrate and the BSF/emitter. This layer can be for instance ultra-thin SiO_x for tunnel oxide passivated contact (TOPCon) [49, 50], or intrinsic a-Si:H for heterojunction (HTJ) architectures [47]. In the latter cases, the BSF and the emitter are no longer c-Si but poly-Si or a-Si:H. Top surface recombination is further reduced by the n^+ top layer, called the front surface field (FSF), which repeals the minority charge carriers. Auger and SRH recombination effects remain low thanks to the thinness and quality of the substrate, respectively. Finally, the backside electrodes, as shown in Figure 2.6(b), follow larger and simpler patterns that enable better electrical conductivity than the ones of FBC cells [47].

2.3. MOSFET

Transistors are semiconductor-based electrical devices and central components of most analog and digital electronic systems. Among all the different transistor technologies, the MOSFET can handle the highest switching frequency; hence, this technology is used in power converters [51]. This chapter introduces the MOSFET, with first a presentation of the structure in subsection 2.3.1 and a description of the operation in subsection 2.3.2. Then, subsection 2.3.3 and subsection 2.3.4 elaborate on the main MOSFET static and dynamic electrical parameters, respectively. Except otherwise stated, the content given in this chapter is sourced from *Semiconductor Physics and Devices: basic principles*, from Neamen [43].

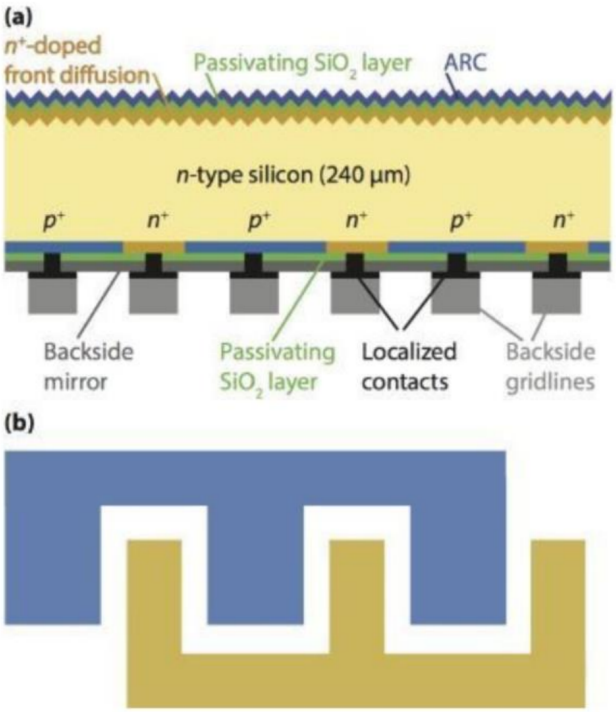


Figure 2.6: (a) Side view of the structure of an n-type IBC solar cell; (b) backside contact [11].

2.3.1. Structure

A Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) is a semiconductor electronic device containing four parts: the Source (S), the Gate (G), the Drain (D), and the Body (B) or Substrate. While S, G, and D are directly connected terminals, a fourth terminal, the grounding contact, controls the potential B. The source, the drain, the grounding contact, and the body are made of doped semiconductors, while the gate is in a metal or doped semiconductor. In this device, the current flowing from the drain to the source is controlled by the voltage between these two terminals and the one between the gate and the body. It is thus possible to switch on and off the current by controlling the gate voltage.

Different categories of MOSFETs are related to the type of substrate and the mode. First, the substrate can be either p- or n-type, giving the name to NMOS or PMOS devices, respectively. Second, the transistor can be an enhancement mode or a depletion mode device, in case it is switched off or on when there is no voltage between the gate and the body, respectively. The architecture of an n-type enhancement mode MOSFET can be seen in Figure 2.7, which displays its cross-section. The drain and the source are highly doped n-type semiconductors. They are separated by the substrate, above which there is an insulating layer, such as SiO_x, and the gate. For a PMOS device, the substrate is n-type, and the source and the drain are p+ -type. In the following sections of this chapter, only formulas about NMOS are given for more simplicity, except if stated otherwise.

2.3.2. Operation

The separation of the gate and the substrate by an oxide layer is typically called a Metal Oxide Semiconductor (MOS) structure. In this structure, which is also the basis of MOS capacitors, the oxide is an insulator so no charge can flow through it; instead, charges accumulate above or underneath the oxide layer when a bias is applied. For an NMOS, if that bias is higher than a so-called threshold voltage V_T (or lower for a PMOS), an electron inversion layer appears and acts as a channel connecting the drain to the source. In this condition, a current can flow between the drain and the source, and the MOSFET is ”turned on”. Otherwise, the absence of an inversion layer prevents the current to flow since the drain-substrate junction is in reverse bias. In practice, the grounding contact and the source terminals are usually connected, so the source and the body have the same potential. The current I_D depends

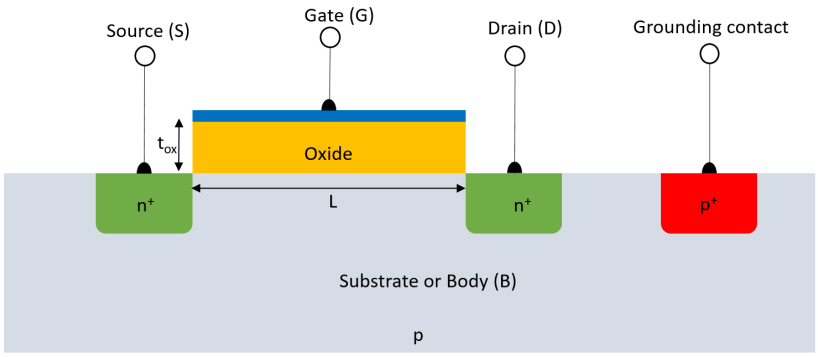


Figure 2.7: Architecture of an N-channel enhancement mode MOSFET.

on both the voltage applied between the gate and the body (i.e., the voltage between the gate and the source, $V_{DB} = V_{DS}$) and on the voltage applied between the drain and the source V_{DS}:

$$I_D = \begin{cases} \frac{W\mu_n C_{\text{ox}}}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] & \text{if } V_{DS} < V_{GS} - V_T \\ \frac{W\mu_n C_{\text{ox}}}{2L}(V_{GS} - V_T)^2 & \text{if } V_{DS} \geq V_{GS} - V_T \end{cases} \tag{2.7}$$

With μ_n the electron mobility, W and L the width and the length of the MOSFET, respectively, and C_{ox} the oxide layer capacitance. The equation is illustrated with Figure 2.8, plotting $I_D - V_{DS}$ characteristics for several values of V_{GS}. The curves are separated into two regions: a non-saturated, called “triode region”, for $V_{DS} < V_{GS} - V_T$, and a “saturation region” for $V_{DS} \geq V_{GS} - V_T$ [52].

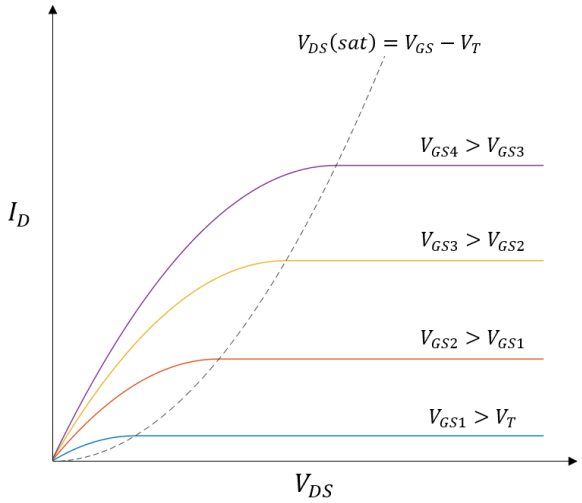


Figure 2.8: Abacus of $I_D - V_{DS}$ curves for an n-channel enhancement mode MOSFET.

2.3.3. Static Electrical Parameters

Threshold voltage

To create the inversion layer, the energy levels (E_C and E_V) at this specific region must be more similar to n-doped semiconductors than p-doped semiconductor energy levels. The threshold voltage is usually defined as the gate voltage for which the interface is “as much n-type as the substrate is p-type” [52]. The threshold voltage value can be calculated from the equations below, the first for NMOS and the second for PMOS.

$$V_{TN} = \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}}(|Q'_{SD}(\text{max})| - Q'_{ss}) + \phi_{ms} + 2\phi_{fp} \tag{2.8}$$

$$V_{TP} = \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}}(-|Q'_{SD}(\text{max})| - Q'_{ss}) + \phi_{ms} - 2\phi_{fn} \tag{2.9}$$

With t_{ox} and ϵ_{ox} the thickness and the permittivity of the oxide layer, respectively; ϕ_{ms} the difference between the metal and the semiconductor work functions; ϕ_{fp} and ϕ_{fn} the gap between the Fermi level and the intrinsic Fermi level in the doped semiconductor; Q'_{SS} the equivalent oxide charge; and $Q'_{SD}(\text{max})$ the charge in the inversion layer, the latter two expressed per unit of area.

On-resistance
In the triode region, a linear relationship can be approximated between the drain current and the drain voltage when the latter is low enough ($V_{DS} \ll V_{GS} - V_T$). The transistor thus behaves like a resistor in this so-called linear region. The on-resistance, defined as the resistance between D and S when the device is on, can be expressed as [52]:

$$R_{ON} = \frac{V_{DS}}{I_D} = \frac{L}{W\mu_n C_{\text{ox}}(V_{GS} - V_T)} \tag{2.10}$$

Transconductance
The MOSFET transconductance g_m is defined by the drain current variation with respect to the corresponding gate voltage change. This parameter is sometimes referred to as the transistor gain:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \begin{cases} \dfrac{W\mu_n C_{\text{ox}}}{L} V_{DS} & \text{if } V_{DS} < V_{GS} - V_T \\ \dfrac{W\mu_n C_{\text{ox}}}{L}(V_{GS} - V_T) & \text{if } V_{DS} \geq V_{GS} - V_T \end{cases} \tag{2.11}$$

Breakdown voltage
Breakdown mechanisms can occur at several voltage levels. It is thus necessary to always make sure that these voltages are never reached to ensure a good use (and sometimes lifetime) of the MOSFET. Breakdown mechanisms are listed below:

- **Oxide breakdown**: In reality, the oxide is not a perfect insulator. If a high electric field is applied, the oxide can break irreversibly, damaging the transistor [52]. In thermal oxide (see subsection 3.1.1), breakdown occurs at a gate voltage of approximately 30 V for an oxide thickness of 50nm. To ensure a safety margin, a maximum gate voltage of 10 V should be considered for this thickness.
- **Avalanche breakdown**: The avalanche breakdown is a non-destructive effect occurring at any p-n junction under high reverse bias. The high electric field resulting from the applied voltage provides enough energy to electrons or holes located at the space charge region to collide with atomic electrons within the depletion region. They then ionize the atoms and create electron-hole pairs that separate and flow in opposite directions through the junction, thus creating a reverse current. The newly generated carriers can, in turn, have enough energy to cause the same process on other atomic electrons, and thus create an avalanche effect. In an ideal planar one-side junction (n+ -p or p+ -n), the breakdown voltage can be expressed by:

  $$V_B = \frac{\epsilon_S E_{crit}^2}{2eN_B} \tag{2.12}$$

  With E_{crit} the critical electric field at the breakdown and N_B the doping concentration in the low-doped region of the junction. For the MOSFET, avalanche breakdown occurs in the space charge region near the drain terminal. The difference with the ideal planar junction case is that the highly doped drain may be a shallow diffused region with a large curvature, as shown in Figure 2.9(a) This structure tends to concentrate the electric field in the depletion region at the curvature, which lowers the breakdown voltage.

- **Near Avalanche** and **Snapback breakdown**: This breakdown mechanism is due to the n(source)-p(body)-n(drain) structure in the MOSFET that forms a parasitic bipolar transistor. This parasitic transistor is activated at a high drain voltage and is responsible for the S-shape curve, as shown in Figure 2.9(b). Avalanche breakdown initiates the effect; as the current flows from the drain to the substrate, a voltage drop appears in the substrate, especially close to the source. The p(body)-n(source) junction thus gets forward biased; hence, electrons flow from the source to the body, and part of them achieve the drain.
- **Punch-Through** and **Near Punch-Through** effects: Punch-through is the situation in which both the source-to-substrate and the drain-to-substrate depletion regions become in contact. It would result in a very high drain current. However, the latter starts increasing rapidly before reaching punch-through. The so-called near punch-through is the condition in which both depletion regions are close enough for the current to increase rapidly.

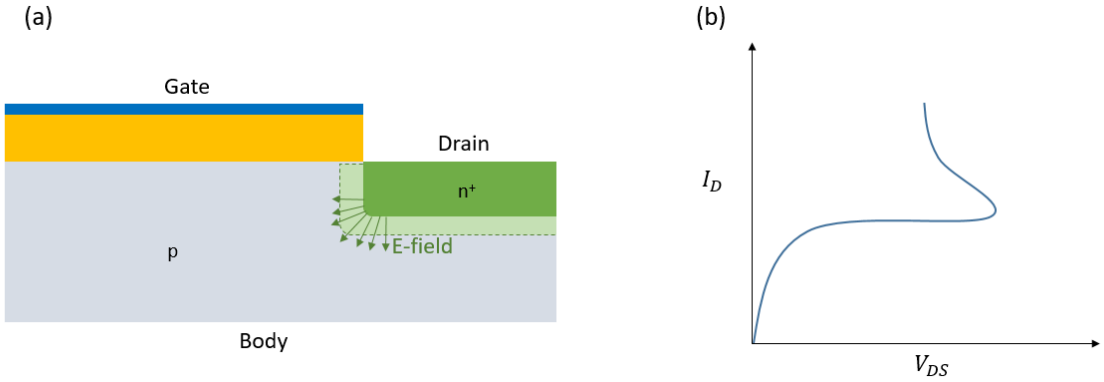


Figure 2.9: (a) curvature effect on the electric field in the drain junction; (b) current-voltage characteristic showing the snapback breakdown effect.

2.3.4. Dynamic Electrical Parameters

In many applications, such as power converters, MOSFETs are used as high-frequency switches. It means that the device is periodically switched on and off. In these conditions, one must consider additional dynamic model of the MOSFET.

Oxide capacitance

As explained in subsection 2.3.2, the gate-oxide-substrate structure forms a capacitor. Its capacitance depends not only on the material properties and dimensions but also on the gate voltage and the switching frequency. For $V_G < 0$, charge accumulation occurs, and the per unit of area capacitance can be determined by:

$$C'_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} \tag{2.13}$$

For V_G close to 0, charge depletion occurs, and the capacitance of the MOS capacitor decreases if V_G increases. Finally, for $V_G > 0$, the situation depends on the frequency. At low frequencies, the capacitance is the same as for the accumulation regime. At high frequencies, inversion happens, and the capacitance of the MOS capacitor converges to a low value.

Parasitic capacitance

At high frequencies, the effects of parasitic capacitances appear due to the basic MOS geometry. Figure 2.10(a) and (b) illustrate the symbolic equivalent circuit of a MOSFET in a high-frequency regime and the capacitances in a MOS device according to its geometry, respectively. One can notice that every terminal (G, B, S, and D) are connected via a capacitance. The source-body and drain-body capacitances, $C_{SB} = C_1$ and $C_{DB} = C_2$, are formed due to the depletion region that appears around the source and the drain. The gate-source and gate-drain capacitances, $C_{GS} = C_4$ and $C_{GD} = C_5$, are

due to an inevitable overlap between the gate and the drain or the source. Finally, C_3 and C_6 combined to form the gate-body capacitance C_{GB}, with C_6 the oxide capacitance described previously and C_3 appearing with the inversion layer.

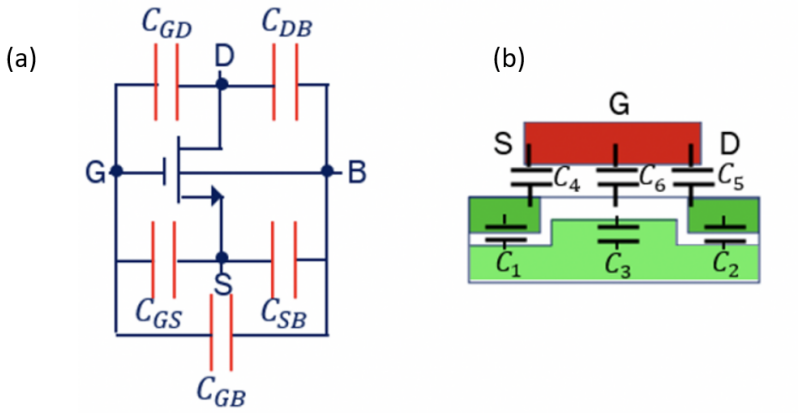


Figure 2.10: (a): symbolic equivalent circuit of a MOSFET in high-frequency regime; (b): Representation of capacitances in a MOS device [53].

3

Device Fabrication and Characterization Methods

This chapter describes how the device is experimentally manufactured and characterized. To do this, section 3.1 introduces the microfabrication processes involved in the flow. Most tools and chemical wet benches are used in the TU Delft Else Kooi Laboratory (EKL) cleanrooms, namely the class 100 IC Processing Lab (cleanroom 100) and the class 10000 Solar Cell Lab (cleanroom 10000). Additional processes are operated at TU Delft Kavli Nanolab cleanroom and the company Ion Beam Services. Second, the measurement methods are detailed in section 3.2. The laboratories involved are the EKL cleanroom 100, the EKL microelectromechanical systems (MEMS) laboratory, and the TU Delft electrical sustainable power (ESP) laboratory. Then, section 3.3 provides a step-by-step description of the combined process flow. Finally, section 3.4 explicates the wafers' layout, including the solar cell and MOSFET dimensions.

3.1. Microfabrication Processes

3.1.1. Thermal Oxidation

Thermal oxidation is a way to produce a thin layer of oxide, mostly silicon dioxide (SiO_2) on the surface of a wafer [54]. Processed at a temperature usually between 900 and 1100 °C, it uses either oxygen with water vapor or dry oxygen. In the first case, the process, called "wet oxidation", has a the chemical reaction is shown in Equation 3.1; in the second case, the process, called "dry oxidation", has a chemical reaction shown in Equation 3.2 [55].

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \tag{3.1}$$

$$Si + O_2 \rightarrow Si0_2 \tag{3.2}$$

The oxide layer thickness t is a function of the thermal oxidation time τ, following the Deal-Grove model [56]:

$$\tau = \frac{t^2 + At}{B} \tag{3.3}$$

With A and B, parameters depend on the oxidation conditions, such as the temperature, the pressure, the gas flow, the type of oxidation, or the type of silicon wafer. For wet oxidation, the time is smaller; hence, this method is preferred for the growth of a thick layer of silicon oxide. However, the resulting material quality is better using dry oxidation, which is thus preferred for critical steps that define the device's quality [55]. In this thesis, thermal oxidation is used to create the MOSFET's gate oxide. The latter being a key element of the component, dry oxidation is used. A Tempress furnace from the EKL cleanroom 100 performs that process.

3.1.2. Plasma-Enhanced Chemical Vapor Deposition

Plasma-enhanced chemical vapor deposition (PECVD) is a type of chemical vapor deposition (CVD) process, consisting of thin film deposition involving the chemical reaction of volatile precursors [55]. Standard CVD uses heat to provide energy to the precursors for the chemical reaction to occur; hence, the process is performed at temperatures in the order of 600 to 800 °C [57]. Instead, PECVD uses plasma, i.e., gas with a high proportion of ions, to enhance the reaction. Consequently, PECVD can be performed faster and at a lower temperature (from ambient temperature to 400 °C). It is thus preferred on wafers that high temperature can harm and has lower energy consumption. Figure 3.1 illustrates a processor reactor of direct PECVD. The substrate is placed in a hot low-pressure deposition chamber between two electrodes: the bottom one is grounded and the top one is radio-frequency energized. From one side, precursor gases are mixed with inert gases; from another side, the plasma is generated by an electronic discharge between the electrodes. In the chamber, precursor gases react in the plasma by colliding with highly energized electrons and are then adsorbed on the substrate [57]. In the thesis, PECVD is carried out for (SiO_x), silicon nitride (Si_xN_y), and hydrogenated intrinsic amorphous silicon ((i)a-Si:H) deposition, using the Novellus Concept 1 in the EKL cleanroom 100 and the Oxford Plasmalab80Plus in the Kavli Nanolab cleanroom.

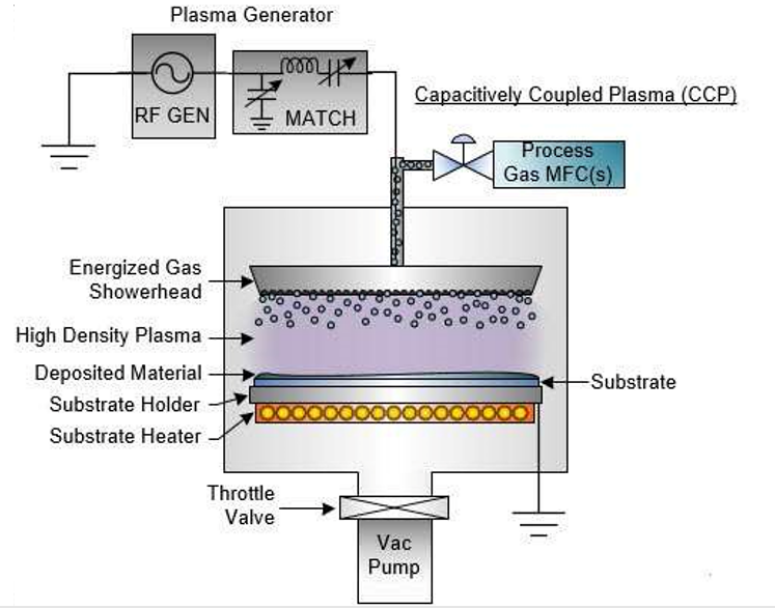


Figure 3.1: Diagram of direct PECVD processor reactor [57].

3.1.3. Low-Pressure Chemical Vapor Deposition

Low-pressure chemical vapor deposition (LPCVD) is another type of CVD. It is a thermal process performed at sub-atmospheric pressure [58]. Like thermal oxidation, a furnace carries out this process. The advantages of LPCVD over PECVD are a higher level of deposition uniformity, fewer defects, and better step coverage. However, it is more time-consuming and is operated at higher temperatures. In this thesis, LPCVD is performed to deposit poly-Si using silane (SiH_4) in a Tempress furnace from the EKL cleanroom 100. The process temperature is around 600 °C.

3.1.4. Evaporation

Evaporation is another deposition method that is also called physical vapor deposition (PVD). When a material (or source) is heated under very low pressure, it evaporates and releases vapor particles, which travel straight to the target substrate, on which they condense back into a solid state [55]. In this thesis, evaporation enables aluminum (Al) deposition and is done using the PROVAC tool in the EKL cleanroom 10000.

3.1.5. Photolithography

Photolithography is a three-step process meant to create a two-dimensional space pattern on the top surface of a wafer. It is done before processes such as etching or ion implantation that will be performed selectively, only on the created pattern. Figure 3.2 illustrates the successive steps involved in the process.

- Firstly, a thin layer of photo-sensitive polymer, called ”photoresist”, is deposited via spin coating. This means that the liquid polymer is added in the center of the surface, and the wafer spins to spread it uniformly over the whole area. Then, soft baking is performed to solidify the photoresist and enhance its adherence with the substrate, at a temperature in the range of 90 to 100 °C.
- Secondly, the wafer is exposed to ultraviolet (UV) light. A mask, placed between the light source and the wafer, contains the pattern to be created by being either UV opaque or transparent. The exposure time defines the exposure energy.
- Finally, development is carried out to strip away part of the photoresist, using a spray developer. In the case of a positive photoresist, its exposed part is stripped away, while it is the contrary for a negative photoresist. Post-exposure baking can be performed before this to amplify chemical reactions within the photoresist and hard baking can be done at the end to strengthen the photoresist structure, at a temperature of 120 to 180 °C [55].

The main advantage of photolithography over other types of patterning processes is the very high resolution. However, due to its high cost and hard scalability, other types based on laser technologies are more competitive for solar cell patterning [59]. Nevertheless, since photolithography is still necessary for MOSFETs due to the much smaller dimensions of the device, it is used in the MOSFET and IBC cell fabrication of this thesis. In the EKL cleanroom 100, automatic coating and development are performed with EVG 120, and exposure is done either via the ASML PAS 5500/80 Waferstepper for the zero-layer step (see subsection 3.3.1) or via the SUSS MicroTec MA/BA8 mask aligner.

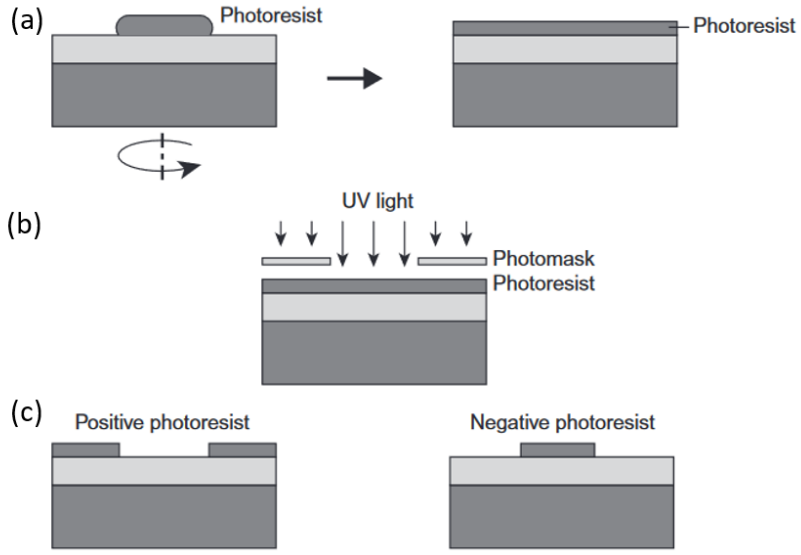


Figure 3.2: Photolithography process: (a) photoresist coating; (b) exposure; (c) development [55].

3.1.6. Etching

Etching is a process that transfers a pattern onto a structural layer underneath the top masking layer [55]. The mask can be photoresist or any other material that resists the etching process. Two types are distinguished: dry and wet etching. The first one, also called plasma etching, is performed with a tool similar to the PECVD chamber. Reactive ions originating from the plasma bombard the material. Alternately, wet etching involves a chemical reaction. The chemicals, called ”etchant”, dissolve the film material where it is not protected by the mask. Selectivity is a key parameter since neither the mask nor any other layer from the wafer must react with the etchant. Unlike dry etching, a unidirectional process,

wet etching spreads in every direction. Consequently, as shown in Figure 3.3, the layer to be patterned is also etched under the mask. The etching time must thus be sufficient to fully remove the layer at the correct region, but small enough to minimize the so-called under-etching effect.

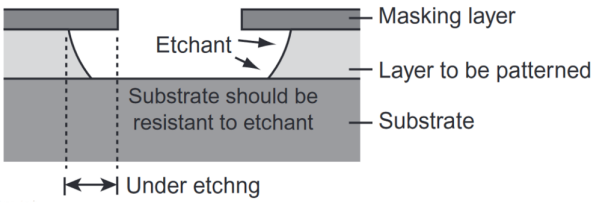


Figure 3.3: Wet etching (side view) [55].

Wet etching can either be isotropic or anisotropic. In the second case, the etching rate depends on the family of directions of the crystal. A family of directions is a set of orientations defining a plane in the lattice coordinates [55]. On c-Si, tetramethylammonium hydroxide (TMAH) is an anisotropic etchant; its etching rate is much higher in the family of direction $\langle 100 \rangle$ than $\langle 111 \rangle$. Consequently, if etched by TMAH, a $\langle 111 \rangle$ oriented polished c-Si wafer, i.e., with a single surface orientation that belongs to $\langle 100 \rangle$, results in having a surface with multiple directions belonging to $\langle 111 \rangle$. This latter situation is a pyramidal structure: the surface is thus textured. Consequently, TMAH etching is one method for texturing the surfaces of a wafer [55].

3.1.7. Lift-Off

Lift-off is another method for creating a pattern on a target thin layer material. This process uses a sacrificial layer that is inversely patterned. One then deposits the target material. Finally, the sacrificial layer is removed, leaving a desired pattern of the target material [55]. In this thesis, the sacrificial layer is a thick (4 to 8 μm) positive photoresist patterned via photolithography. After the deposition of a metal layer, it is then removed by sonication in acetone.

3.1.8. Ion Implantation

Ion implantation is one technique of ion doping that consists in accelerating dopant atoms and implanting them into a semiconductor [55]. Figure 6 displays the setup of an ion implanter. Atoms are first excited to form ions. Then, they are extracted from their source, accelerated by an electrostatic field, and sorted by an analyzer. The analyzer is made up of a magnet and a slit. It first applies a magnetic field to deviate the ions, the trajectory of which depends thus on their mass, charge, and velocity, and selects the desired particles with the slit. The ion beam is then shaped by a series of electrostatic and magnetic lenses to scan the surface of the substrate [55]. Ion implantation allows the control of two parameters: the dose and the energy. The dose, commanded by the beam intensity and duration of the process, is the density of ions in the crystal in units of at/cm^2. The energy, in units of keV, is related to the implantation depth. After implantation, a high-temperature process, called 'annealing' is carried out to reform the crystalline lattice of the doped semiconductor.

3.2. Measurement Tools

Many characterization tools are used in this work. Although measurements are done after fabricating the device, as shown in the next chapters, other measurements are performed during the fabrication for better process control. For this reason, the measurement theory and tools are introduced before the process flow description.

3.2.1. Lifetime Measurement

The minority carriers' lifetime is one the most crucial solar cell parameters that directly affect its performance since it is directly related to the minority carriers' recombination. In that view, lifetime measurements are carried out to verify the passivation quality of a device. In the example of p-type material,

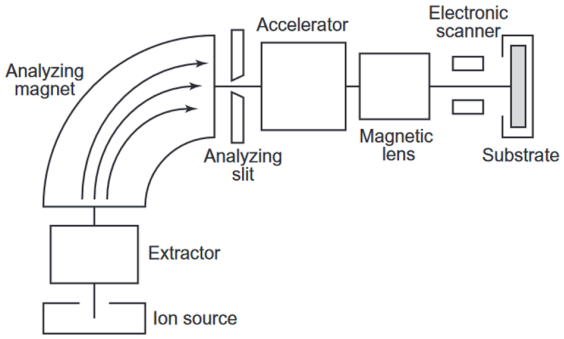


Figure 3.4: Ion implantation setup [55].

for uniform photogeneration and zero surface recombination, the electric field is zero. The effective minority carriers' lifetime can thus be written [60]:

$$\tau_{eff} = \frac{\Delta n}{G - \frac{\mathrm{d}\Delta n}{\mathrm{d}t}} \tag{3.4}$$

Two different measurement modes are possible. First, the quasi-steady state photoconductance (QSSPC) mode involves a light pulse that varies very slowly compared to the effective lifetime of the sample [61]. In that case, the term $\mathrm{d}\Delta n/\mathrm{d}t$ is negligible, hence a simplification of the above equation. Second, the transient mode involves a very short light pulse and the minority carriers decay is measured once the light is off. Consequently, $G = 0$, hence another simplification of the equation. This measurement can also determine the implied open-circuit voltage iV_{OC}. Once τ_{eff} is measured, Δn can be directly derived. Then, the following equation [62]:

$$iV_{OC} = \frac{kT}{q} \ln\left(\frac{\Delta n[N_{dop} + \Delta n]}{n_i^2}\right) \tag{3.5}$$

is applied to derive iV_{OC}. This value is the theoretical open circuit voltage value that the solar cell would have according to this model. Minority carriers' lifetime measurements are carried out in the EKL cleanroom 10000 with the Sinton WCT120.

3.2.2. Spectroscopic Ellipsometry

Spectroscopic ellipsometry (SE) is a measurement method used for characterizing properties of a film on the substrate, such as its thickness, based on the spectral and polarimetric properties of reflected light. Figure 3.5 illustrates the physical principle of the measurement. An incident linearly polarized light is sent towards the sample, reflected by the sample, and then received by a system analyzing the polarized resulting light. Since all light can be decomposed into two linearly polarized waves oscillating in distinct planes, the resulting light is here decomposed into the plane of incidence p and its perpendicular one s. Complex Fresnel reflection coefficients r_p and r_s are measured for both p- and s-polarized lights, respectively, as a function of the wavelength λ. Finally, the angles Ψ and Δ are derived for each λ, following the following equation [63]:

$$\tan\Psi e^{i\Delta} = \frac{r_p}{r_s} \tag{3.6}$$

One then obtains a spectral profile of Ψ and Δ, with which software fits the curves from a predefined model by varying parameters through an iterative calculation. In this thesis, SE measurements are carried out to determine the thickness of a film; hence, the thickness is the variable parameter of the model. The iterative calculation seeks the best fitting, i.e., the lowest mean square error (MSE) between the model values (Mod) and the experimental values (Exp), defined as [63]:

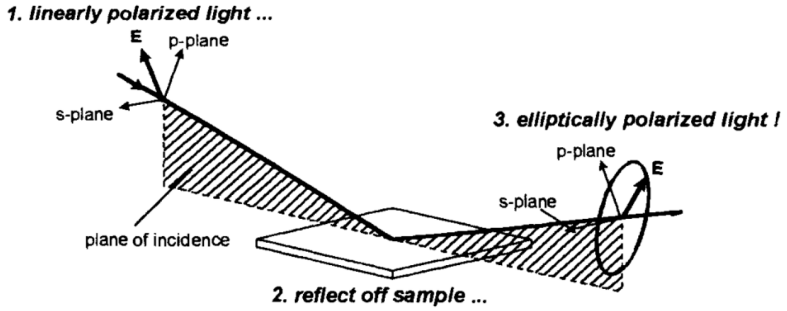


Figure 3.5: Interaction of polarized light with a sample [63].

$$MSE = \sqrt{\frac{1}{2N-M}\sum_{i=1}^{N}\left[\left(\frac{\Psi_i^{Mod}-\Psi_i^{Exp}}{\sigma_{\Psi,i}^{Exp}}\right)^2+\left(\frac{\Delta_i^{Mod}-\Delta_i^{Exp}}{\sigma_{\Delta,i}^{Exp}}\right)^2\right]} \tag{3.7}$$

3.2.3. Microelectronics Components Measurement

The MOSFETs are characterized in the EKL microelectromechanical systems (MEMS) laboratory. The setup includes a Cascade probe station, which can connect multiple probes to the electronic device. Thanks to an integrated microscope, it is able to establish connections with contact pads smaller than 100 μm. The Agilent 4156 Precision Semiconductor Parameter Analyzer is connected to the station to generate the electrical power and measure current and voltage. MOSFET I_D-V_{GS} and I_D-V_{DS} characteristics are obtained from that setup.

3.2.4. Solar Simulation

Solar simulator Wacom WXS-156S AAA is used to measure the solar cell's current-voltage characteristic in standard test conditions. The solar AM1.5 spectrum is reproduced from a xenon lamp and a halogen lamp combined. Both produce a total irradiance of 1000 W.m^{-2}. Before the measurement, the setup is calibrated using two cells that were in turn calibrated at Fraunhofer ISE CalLab. The operating temperature is kept between 24 °C and 30 °C.

Besides solar cells, the setup is used to characterize MOSFETs under illumination and the monolithically connected solar cell and MOSFET. However, since the tool initially only includes two probes, an additional Keithley 2601 System SourceMeter generator is introduced, along with two probes. They are meant to control the gate-to-source voltage, while the drain-to-source voltage and drain current are obtained with the original setup. Negative probes of both generators are connected to avoid floating voltages.

3.3. Combined Manufacturing Process Flow

In this thesis, we use 280 ± 20 nm thick, $\langle 100 \rangle$ oriented FZ c-Si wafers, having 1 − 5 Ωcm resistivity and 100 mm diameter. Both n-type (P-doped) and p-type (B-doped) wafers are investigated in this work. 10 wafers of each type are processed, respectively identified by n1 to n10 and p1 to p10. The IBC solar cell manufacturing method is inspired by G. Yang et al. [41], who created the BSF and emitter using intrinsic poly-Si, deposited on an ultra-thin (< 1.5 nm thick) SiO_x layer that allows TOPCon. Then, poly-Si is patterned, doped via ion implantation, covered by Si_xN_y, and finally metallized with aluminum (Al). The MOSFET is integrated on the backside of the wafers, videlicet, on the same side as the solar cell BSF and emitter. It enables easy metal connection on the same side of the substrate and uniform texture on the front side. The process is similar to the work of Y. Mercimek [42]. SiO_x and poly-Si layers are successively created, then patterned together to create the gate. The component is then doped via ion implantation, covered by Si_xN_y, and metallized. Finally, the wafer's top side is uniformly textured, passivated, and anti-reflection coated. In the following subsections, a step-by-step description of the process flow is provided. The schematics illustrating the processes represent the solar cell and the

transistor manufacturing on the right and left figure sides, respectively.

3.3.1. Zero-Layer

The fabrication of the combined IBC + MOSFET device is supported by a total number of 7 photolithographic steps, responsible for patterning the multiple layers. However, the superimposed patterns must be well-aligned. The zero-layer definition is a preliminary process aimed to provide a common reference for the mask alignment. The markers are created via an extra photolithographic step, using the ASML PAS 5500/80 waferstepper, followed by 120 nm deep plasma etching of the c-Si wafer, using the Trikon Ωmega 201 plasma etcher

3.3.2. MOSFET gate oxide

The MOSFET gate requires the creation of a SiO_x layer. That is done via dry thermal oxidation at 1000 °C, during 1h 06min 25s, for a resulting oxide thickness of 54 nm, uniformly on both sides of the wafer, as shown in Figure 3.6(a). The targeted eventual layer thickness is 40 nm minimum. However, the processes described in subsection 3.3.3 involve SiO_x etching, reducing the layer thickness. Oxidizing to a 54 nm thick layer is thus meant to compensate for the subsequent etching step effects. Since the SiO_x layer is solely part of the MOSFET, it is then removed from the other areas. To do so, photolithography protects the oxide at the MOSFET areas, as shown in Figure 3.6(b). Wet etching follows in a buffered hydrogen fluoride (BHF 7:1) bath, used for its excellent etching selectivity [64]. Finally, the photoresist is stripped by using an acetone bath, for a result sketched in Figure 3.6(c).

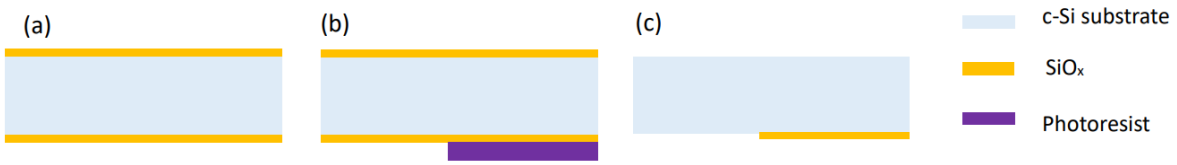


Figure 3.6: Gate oxide layer creation: (a) dry thermal oxidation; (b) photolithography; (c) oxide etching and photoresist stripping.

3.3.3. Passivated poly-Si Contact and Texture

The back-side passivated poly-Si contact formation and the subsequent front-side texturing processes are presented in Figure 3.7. First, a native SiO_x layer that naturally forms at the interface between c-Si and air must be removed. This is done by dipping the wafer into hydrogen fluoride (HF), 0.55% for 4 min. This process also reduced the gate oxide thickness; the latter value reduces to 45 nm. Then, an ultra-thin SiO_x layer is grown using the nitric acid oxidation of silicon (NAOS) method [65] for TOPCon. This process is equivalent to the ”standard cleaning” carried out anytime a cleaning is needed during the fabrication: the wafer is successively dipped into nitric acid (HNO_3, 99%) for 10 min at room temperature; DI water for 5 min; HNO_3 (69%) for 10 min at 110 °C; DI water for 5 min. This process results in a 1.3 nm thick SiO_x layer on the substrate, sketched in Figure 3.7(a). The next step, shown in Figure 3.7(b), is poly-Si LPCVD, for 1 h 53 min. It results in a thickness of about 250 nm. The back-side is then protected with a 1 μm thick SiO_x layer (Figure 3.7(c)), using the Novellus Concept 1 for PECVD, at 400 °C. This protection ensures that the following processes, namely poly-Si stripping, and texturing, are only applied on the front side. Poly-Si removal, shown in Figure 3.7(d), is done via poly-Si etching bath (48% HNO_3 and 0.75% HF) dipping for 2 min. This solution also etches SiO_x; hence, the protection layer is thick enough to remain after the chemical bath. Texturing is done in TMAH (1/5 volume, 120 mL Alkatex 8) at 80 °C for 12 min. The resulting wafer, sketched in Figure 3.7(e), is then subsequently cleaned, dipped in 0.55% HF for 3 min, cleaned, dipped in BHF 7:1 for 5 min to remove the remaining SiO_x, and cleaned again. The result figures in Figure 3.7(f).

3.3.4. Back Contacts and Gate Patterning

Patterning the IBC solar cell back contacts and the MOSFET gate is achieved via etching the solar cell poly-Si layer and the MOSFET poly-Si and SiO_x layers. We investigate here two trajectories, supporting different poly-Si etching methods. The first trajectory, illustrated in Figure 3.8(1a) to (1c), includes

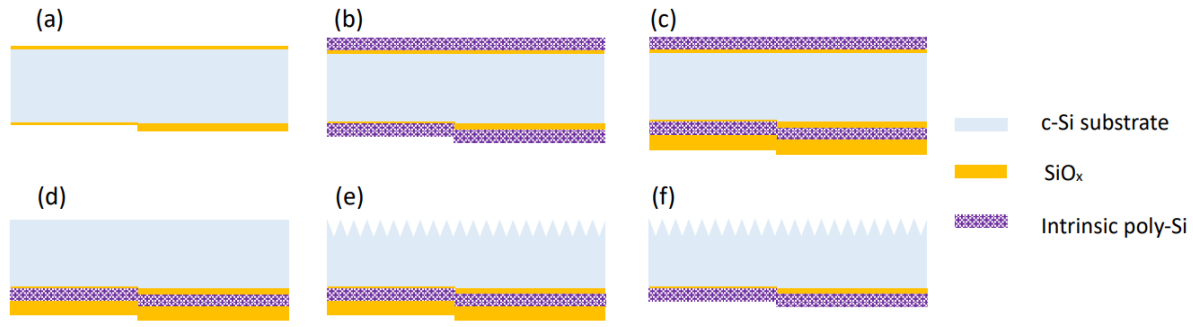


Figure 3.7: Passivated poly-Si contact and texturing: (a) NAOS; (b) poly-Si LPCVD; (c) back-side SiO_x PECVD; (d) Front-side poly-Si stripping; (e) Front-side texturing; (f) Back-side SiO_x stripping.

poly-Si dry-etching and is performed on wafers N1-5 and P1-5. First, the pattern is defined by photolithography (Figure 3.8(1a)). The poly-Si layer is next etched using the Trikon Ωmega 201 plasma etcher. To completely etch the layer, the time process is designed for over-etching; hence, the gate oxide is also partially etched by approximately 13 nm, and the NAOS SiO_x is fully etched. Then, the photoresist layer is stripped in the Tepla Plasma 300 (Figure 3.8(1b)). Finally, the remaining oxide is stripped in a BHF 7:1 bath for 1 min 20 s (Figure 3.8(1c)).

In the second trajectory, wet-chemical poly-Si etching is used. As shown in Figure 3.8 (2a) to (2e), this method requires an additional SiO_x sacrificial layer. This is supported by the photoresist material that can be removed if dipped into a poly-Si etching solution. Consequently, SiO_x is the etching mask. After deposition via PECVD of a 600 nm thick SiO_x layer (Figure 3.8(2a)), photolithography creates the pattern (Figure 3.8(2b)), followed by dry etching of SiO_x with the Drytek Triode 384T plasma etcher, and photoresist stripping with the Tepla Plasma 300 (Figure 3.8(2c)). The next step is wet poly-Si etching, in the HNO_3/HF bath (Figure 3.8(2d)). The etching time, which varies according to the wafer, is tabulated in Table 1. Finally, the remaining SiO_x, present at the etching mask and the gate layers, is stripped in a BHF 7:1 bath for 2 min (Figure 3.8(2e)).

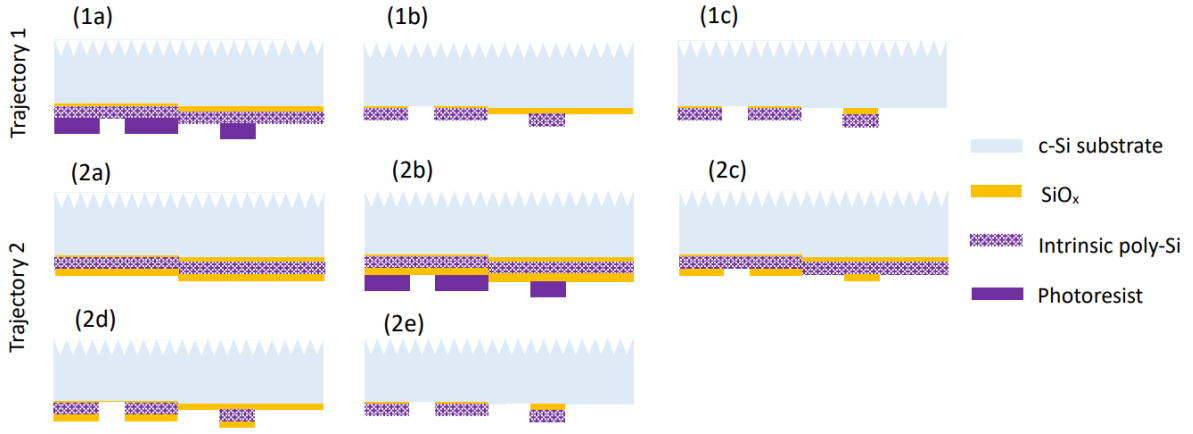


Figure 3.8: Back-contacts and gate patterning: (1a) - (1c) dry poly-Si etching trajectory; (2a) - (2e) wet poly-Si etching trajectory.

Wafer id	N6, P6	N7, P7	N8, P8,	N9, P9	N10, P10
Wet etching time (min:ss)	2:00	1:20	1:40	2:30	3:00

Table 3.1: Wet poly-Si etching time.

Both trajectories have advantages and drawbacks related to the type of poly-Si etching. Wet poly-Si

etching is preferred for solar cell manufacturing since the Trikon Ωmega 201 plasma etcher is used for various process flows that are not related to solar cell manufacturing and may thus be contaminated by undesired particles. That would increase the solar cell surface defect density and harm the passivation quality. Oppositely, wet etching involves here a freshly mixed poly-etch solution, which ensures a very low contamination level. However, dry poly-Si etching is more uniform and unidirectional. It is thus more reliable, especially for manufacturing the MOSFET, the pattern of which has very small dimensions. In Figure 3.9(a), a microscope picture displays part of one MOSFET gate on the left, close to one solar cell on the right. It shows in yellow the remaining poly-Si after etching. Figures 3.9(b) and 3.9(c) provide pictures with a closer zoom of the MOSFET gate, taken after wet and dry poly-Si etching, respectively. It is visible that for wet etching, under etching occurs at the edges of the gate and represents an unneglectable area. Consequently, the actual gate length was reduced. That effect may be strengthened for a longer etching time and might differ from one transistor to another on the same wafer due to the non-uniformity of the process.

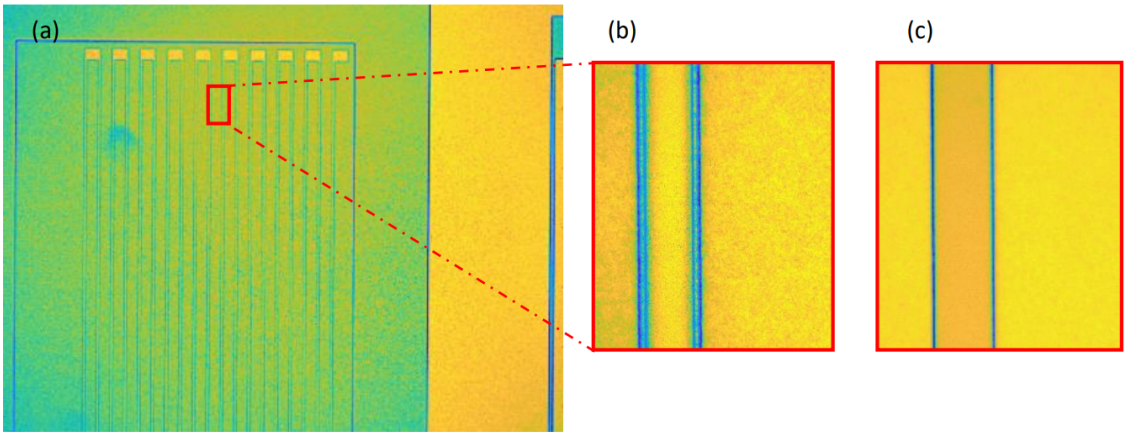


Figure 3.9: poly-Si pattern. (a) part of one MOS gate (left) and part of one solar cell (right); (b) wafer N6 wet poly-Si etched MOS gate; (c) wafer N1 dry poly-Si etched MOS gate.

3.3.5. Backside Implantation

Doping the solar cell BSF and emitter and the MOSFET source, drain, ground, and gate are carried out via ion implantation. As shown in Figure 3.10, pattern definition happens before each implantation step by means of photolithography. Two implantations are performed; the first one is phosphorus (Ph) implantation for n^+ doping, with an energy of 20 keV and a dose of 6.10^{15} at/cm^2; while the second one is boron (B) implantation for p^+ doping, with an energy of 15 keV and a dose of 5.10^{15} at/cm^2. The reason for lower values in the second case is that boron penetrates more easily into the semiconductor material. Both implantations are executed in the company Ion Beam Services, located at Peynier (France) [66]. The device is then annealed at 950 °C for 5 min in an O_2 atmosphere (3 SLM of O_2 gas flow). This results in a better crystalline structure of the poly-Si, a lattice reformation of the implanted c-Si, and a thin superficial SiO_x layer formed because of the oxidation. This layer is finally etched in an HF 0.55% bath. The parameters choice (implantation doses and energies, annealing time, temperature, and atmosphere) is issued from the optimization work done by Yang et al. [49].

The passivation quality was verified with an n-type test wafer receiving at both sides NAOS, poly-Si LPCVD, uniform boron implantation, and annealing, in the same conditions as the ones used for building the device. The minority carriers' lifetime is then measured, using the transient model and 10^{15}cm^{-1} minority carriers' density. A lifetime of 4.56 ms was found using the QSSPC measurement mode.

3.3.6. Surface Passivation and ARC Treatment

The next processes are related to the front and backside passivation and ARC treatment. As mentioned in section 3.4, two front-side passivation methods are explored. In the first one, an FSF is introduced through ion implantation with the same doping type as the BSF (p^+ in the figure). Note that this step is performed at the same time as the implantation indicated in subsection 3.3.5, so also before the

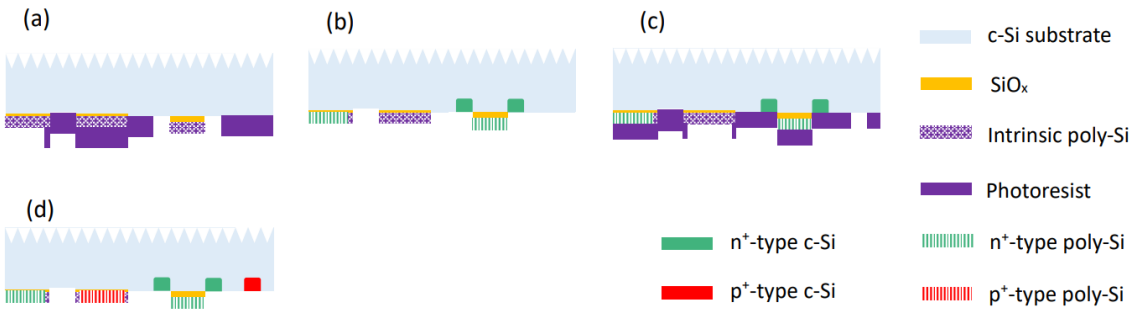


Figure 3.10: Back-side doping process. (a) photolithography before Ph implantation; (b) Ph implantation and PR stripping; (c) photolithography before B implantation; (d) B implantation and PR stripping.

thermal anneal. FSF is introduced on wafers N1, N2, P2, and P3. Table 3.2 reports the implantation atoms, energies, and doses, in each case. After that comes an ultra-thin oxide layer creation through the NAOS process for a TOPCon passivation. Finally, Si_xN_y is deposited on both sides through PECVD at 400 °C, using the Novellus Concept 1. The layer thickness at the front and back side is 75 nm and 300 nm, respectively. These successive steps are illustrated in Figure 3.11(1a) to (1c). The second method involves Si HTJ passivation. First, a $\simeq$ 5 nm (i)a-Si:H film is deposited via PECVD at 150 °C, using the Oxford Plasmalab80Plus in the Kavli Nanolab cleanroom. Then, the same tool deposits Si_xN_y on both sides. The layer thickness at the front and back side is 75 nm and 100 nm, respectively.

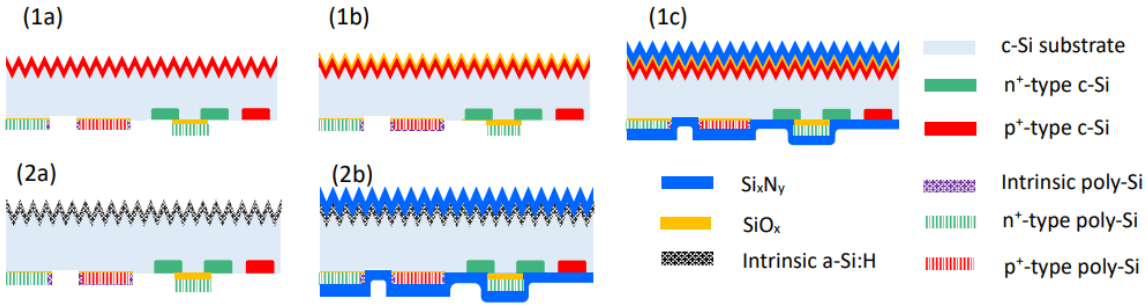


Figure 3.11: Surface passivation: (1a) ion implantation; (1b) NAOS; (1c) double-side Si_xN_y PECVD; (2a) (i)a-Si:H PECVD; (2b) double-side Si_xN_y PECVD.

Wafer	Implanted atom	Energy (keV)	Dose (at/cm^2)
N1	Ph	10	1.10^{14}
N2	Ph	10	5.10^{14}
P2	B	5	1.10^{14}
P3	B	5	5.10^{14}

Table 3.2: Implantation atoms, doses, and energies for the wafers including an FSF.

Openings in the backside silicon nitride are then created. Patterning is carried out via photolithography; then, the film is etched. In the FSF case, dry etching is performed, using the Drytek Triode 384T plasma etcher in the EKL cleanroom 100. In the Si HTJ case, wet chemical etching is chosen: the wafers are dipped in a 7:1 BHF solution for 10 min.

3.3.7. Metallization

In this work, the metallization consists of a three-step process depicted in Figure 3.12. Firstly, photolithography defines the metal pattern with a photoresist that acts as a sacrificial layer for further lift-off. The photoresist thickness is between 4 μm and 8 μm. We use here a positive AZ ECI 3027 photoresist. Secondly, a 2 μm thick Al layer is deposited via metal evaporation with the Provac tool in the

EKL cleanroom 10000. Such thickness ensures low resistive losses. Then, lift-off, operated in sonic acetone, removes the photoresist and the area-related metal. Post-metallization thermal annealing is then carried out at 350 °C on a hotplate for 5 min.

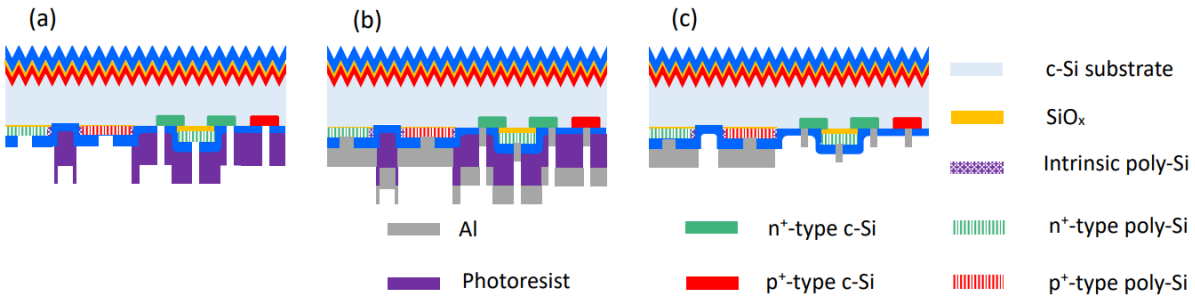


Figure 3.12: Metallization: (a) Photolithography; (b) Al evaporation; (c) Lift-off.

3.3.8. Process flow summary

Variations in the poly-Si etching, Si_xN_y etching, Si_xN_y deposition, and front side passivation techniques have been introduced above. Therefore, one can distinguish three different fabrication flows. Table 3.3 summarizes the processes involved for the three groups of wafers.

Wafers	Processes
n1, n2, p2, p3	• Dry poly-Si etching • FSF passivation • Novellus Concept 1 deposited Si_xN_y • Dry Si_xN_y etching
n3 to n5, p4, p5	• Dry poly-Si etching • Si HTJ passivation • Oxford Plasmalab80Plus deposited Si_xN_y • Wet Si_xN_y etching
n6 to n10, p6 to p10	• Wet poly-Si etching • Si HTJ passivation • Oxford Plasmalab80Plus deposited Si_xN_y • Wet Si_xN_y etching

Table 3.3: Process flows comparison.

3.4. Wafer's Layout

The wafers fabricated in this thesis each contain 10 solar cells and 22 transistors. The backside layout, shown in Figure 3.13, was designed by David van Nijen for this thesis. The solar cells are either isolated from the transistors (C1, C6, C8, C9), disconnected but close to transistors (C7, C10), or connected to transistors (C2, C3, C4, C5). Likewise, the transistors are mostly totally separated from the cells (T1 to T14), but some of them are close to cells (T15 to T18), or connected to them (T19 to T22). Figure 3.14(a) provides a closer visual of the solar cell design. The interdigitated BSF and emitter have a respective width of 180 μm and 280 μm. Metal contacts are situated over the BSF and the emitter,

and meet at the top and bottom of the cell, respectively, in pads that enable the contact between the electrodes and the measurement tool. The solar cell surface area is 1x1 cm^2. Transistors T15 to T22 have 4 metal pads (to connect the gate, drain, source, and body), while transistors T1 to T14 only have 3 pads, the body being then connected to the source. Figure 3.14(b) plots the top of T2, for which two pairs of drain and course can be observed. The top metal pad is connected to the drains. The left pad is connected to the gates, that separate drains and sources. Finally, a bottom pad, not visible in this figure, is connected to both the source and the grounding contact. The gate length is 4 μm, except for T14, for which it is 3 μm. The gate width and the number of MOS in parallel are variable, as summarized by Tables 3.4 and 3.5 for the transistors T1-14. Transistors T15-22 share the same parameters: 10 drain-source couples with 2 mm gate width.

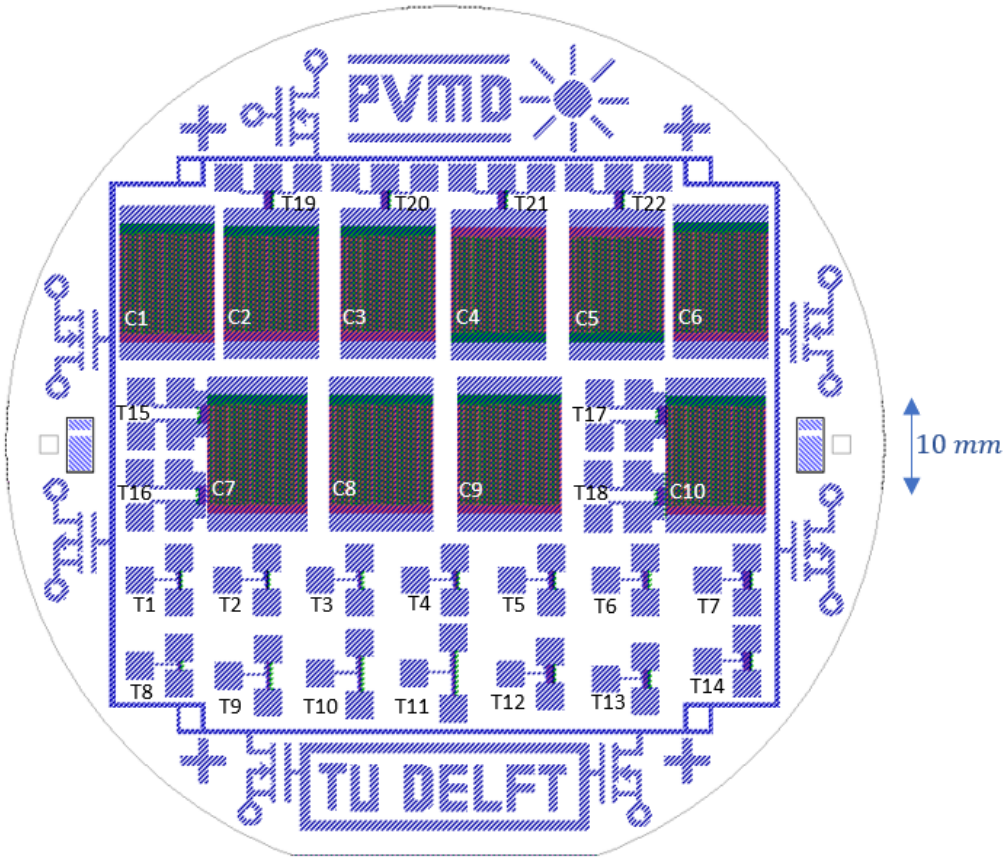


Figure 3.13: Full view of the device backside, from L-Edit software.

Transistor id	Number of drain-source pairs
T1	1
T2	2
T3	3
T4	4
T5	5
T6	7
T7	10
T12	10
T13	5
T14	10

Table 3.4: Parallel MOS number for transistors T1-7 and T12-14. Common gate width: 2mm.

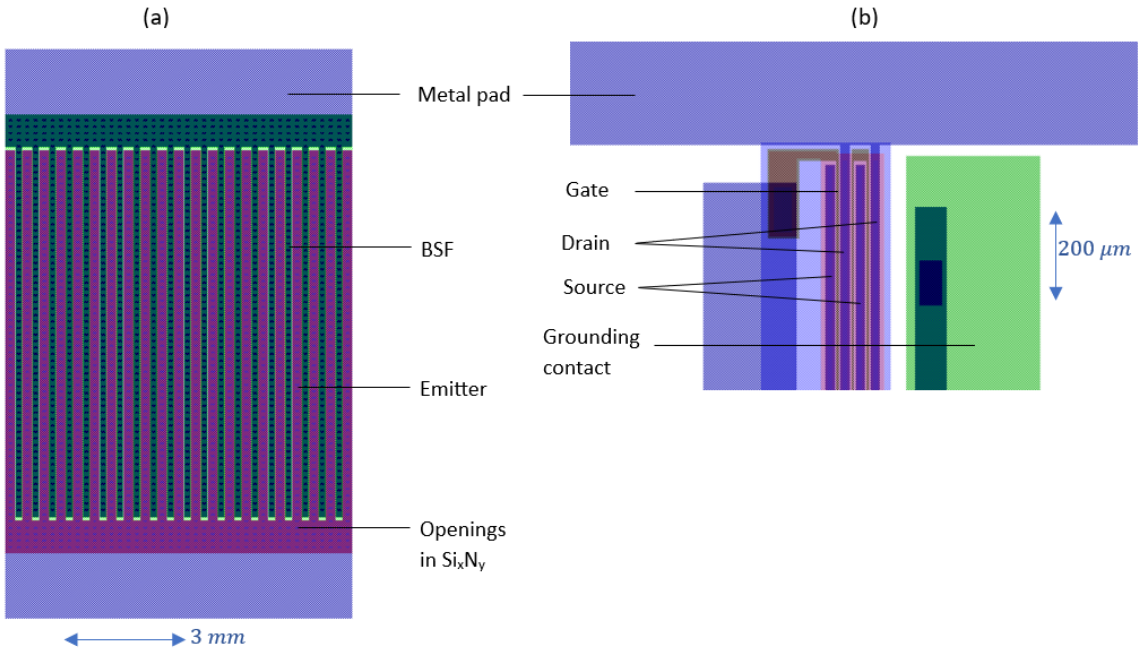


Figure 3.14: Layouts from L-Edit software: (a) solar cell C1; (b) top of transistor T2.

Transistor id	Gate width (mm)
T8	1
T9	3
T10	4
T11	5

Table 3.5: Gate width for transistors T8-11. 3 parallel MOS.

4

Solar Cell Characterization

This chapter presents the results of the solar cell characterization. First, unexpected kinks in the J-V characteristics are described, and hypotheses aiming to explain them are provided. Then, the effect of thermal annealing on n-type and p-type wafers is described. Finally, the effect of process flow variation is analyzed.

4.1. Kinks in the J-V Characteristics

Before properly presenting the results and solar cell performance, we first describe a parasitic effect that is observed on the solar cell J-V characteristics and that may limit the analysis. All the measured solar cells exhibit unexpected kinks in the high current and relatively low voltage J-V region. This effect is illustrated by Figure 4.1(a) displaying the J-V curves and Figure 4.1(b) focusing on the kinks region. Instead of being a constantly decreasing function of the voltage, the current density first increases until it reaches an angular point, that we propose to call the ”kink point”. This point is characterized by a discontinuous current variation and a current decrease after it.

Several hypotheses are proposed to explain that behavior:

- The curve behavior may be caused by parasitic capacitance effects coming from either the measurement setup or the cell. In the case of voltage sweep, the dynamic nature of the measurement involves dynamic parameters such as capacitance. Such sweeps involving high capacitance also exhibit kinks due to transient capacitance discharge [67]. That effect could explain the difference between forward and reverse voltage sweeps. However, solar cell intrinsic capacitance is usually observed on a large area (>100 cm^2) solar cells for very short flash measurements (I-V scan times in the range of a few milliseconds) [67]. On the contrary, the solar cells studied in this thesis have a 1 cm^2 area and are subject to much longer scans (several seconds). Finally, the kink should only be observed in one sweep direction and not in both, as observed here. Alternatively, the effect could be attributable to the measurement setup.
- The exponential current increase preceding the kink point recalls a diode behavior. Therefore, the presence of reversed parasitic diodes could contribute to the observed trend. They could be caused either by the solar cell design itself or by consistent manufacturing errors. However, it would not explain the abrupt current variation change at the kink point.
- One last possibility is unreliable voltage or current measuring capability of the measurement setup at a relatively constant current.

In practice, the presence of kinks results in the possible erroneous estimation of the short-circuit current density since it is supposed to be the maximum measured value. For that reason, we tackle that issue by giving a range of values that includes $J(V = 0)$ and J_{max}, rather than a specific number. For instance, we can deduce from the characteristic in Figure 4.1 that 36 mA/cm^2 $< J_{SC} <$ 37.7 mA/cm^2. Likewise, the fill factor cannot be precisely estimated but rather belong to an interval. Nevertheless, the data are assumed to be reliable after the kink point. Hence, the behavior does not affect the maximum power point and open-circuit voltage.

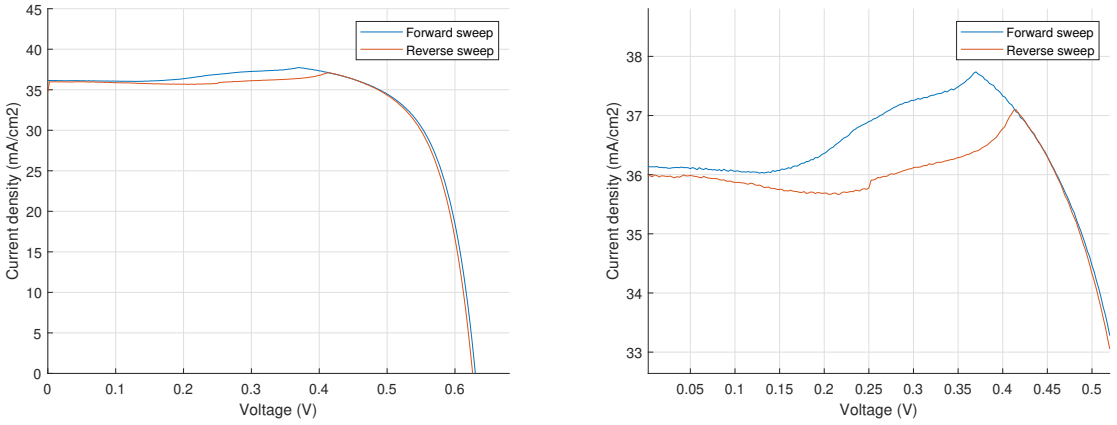


Figure 4.1: Kinks in the J-V characteristic obtained from forward and reverse voltage sweeps: (a) full characteristic; (b) zoom in the kink region.

4.2. Effect of Post-Metallization Thermal Annealing

As described in section 3.3, the last combined process step is annealing, operated at around 350 °C. This subsection aims to analyze the effect of annealing on solar cell performance by comparing the efficiencies measured before that step with the ones measured after. Figure 4.2 provides the box plot of the efficiency of n-type and p-type solar cells, obtained before (w/o) and after (w/) annealing. Solar cells from all the manufacturing methods and included in the data, explaining the high range of efficiency values (see section 4.3). One can notice that the n-type solar cells glocally experience a slight efficiency increase after annealing since the median and the values of the quartiles increase. On average, the efficiency increases by a relative percentage of 3.28%. On the contrary, the average p-type solar cell efficiency drops by 10.1%.

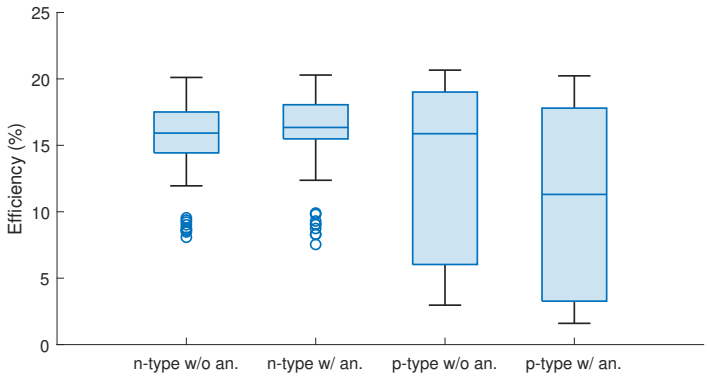


Figure 4.2: Impact of post-metallization annealing on n-type and p-type solar cells.

The difference in results caused by annealing between n-type and p-type solar cells supports the necessity to distinguish the solar cell type. Figure 4.3(a) and (b) plots J-V characteristics obtained before and after annealing an n-type and for a p-type solar cell, respectively.

- N-type solar cells exhibit an improved contact resistance balanced by decreased open-circuit voltage. Both can be explained by interdiffusion effects at the poly-Si/aluminum interface [68]. Overall, the gain in FF being larger than the loss in V_{OC} supports the power conversion efficiency rise.
- P-type solar cells undergo a much faster current decrease with regards to the voltage increase after annealing. Consequently, lower FF and V_{OC} are observed, signifying increased recombination. Since the backside structure is similar to one of the n-type solar cells (the metal is in

contact with both B- and Ph-implanted poly-Si), the recombination increase must be from either the p-type c-Si bulk or the front-side surface. The former hypothesis is not likely because the bulk withstood higher temperature annealing earlier in the process (after ion implantation). Therefore, front-side surface recombination increase due to post-deposition thermal anneal at 350 °C. This must be originated by increased defect density at the (p)c-Si/(i)a-Si:H interface.

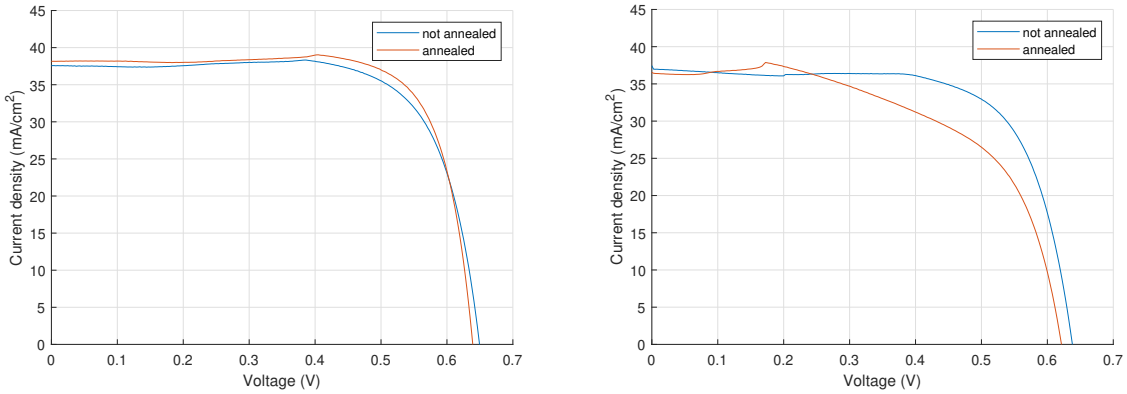


Figure 4.3: J-V curves before and after annealing: (a) n-type substrate; (b) p-type substrate.

4.3. Effect of the Manufacturing Method

This section presents the impact of the different explored processes on solar cell performance. As described in section 3.3, the process flow used for manufacturing the solar devices varied into three categories, respectively involving: (i) dry poly-Si etching, dry Si_xN_y etching, FSF; (ii) dry poly-Si etching, wet Si_xN_y, front-side HTJ passivation; (iii) wet poly-Si etching, wet Si_xN_y, front-side HTJ passivation. Figure 4.4 displays the power conversion efficiency obtained for solar cells of each wafer. The shunted solar cells are excluded from this plot. Blue, red, and green rectangles indicate the manufacturing methods (i), (ii), and (iii), respectively. Finally, since post-metallization thermal anneal is proven to enhance the n-type but highly worsens the p-type solar cells, the reported p-type results are without annealing and n-type results with annealing.

Solar cells involving FSF as a front-side passivation technique exhibit the worst performance. Especially an important gap is noticeable between wafers n1 and n2, as well as between p2 and p3. This is explained by the difference in the implantation dose used in the FSF doping. Both n1 and p2 had a Ph and B dose of 1.10^{14} at/cm^2, respectively, while n2 and p3 had 5.10^{14} at/cm^2 dose. Hence, it comes out that doping atoms' density must remain low to minimize the recombination in that region. A trade-off needs to be found in the doping density. Heavier doping repels the minority carriers more efficiently and thus reduces surface recombination; however, it increases the defect density, resulting in higher bulk recombination. The trade-off is found for light doping [69]. Increased global recombination for cells n2 and p3 results in lower V_{OC} and J_{SC}, hence the efficiency reduction. However, wafer p2 also exhibits very low (<7%) cell efficiencies. Two assumptions may explain this. First, too high implantation dose or energy might still result in important bulk recombination. Second, a manufacturing mistake may have occurred.

Process (ii) gave better performances than (i). Table 4.1 provide the open-circuit voltage, short-circuit current density, fill factor, and efficiency of n-type and p-type best performing solar cells from each process. It shows that lower V_{OC} and J_{SC} are responsible for the smaller η in case (i). Several differences can explain the difference in recombination rate and possibility in photocurrent:

- Different front side passivation techniques: (ii) includes intrinsic a-Si:H on the front side instead of FSF. It repels minority carriers without increasing bulk recombination.

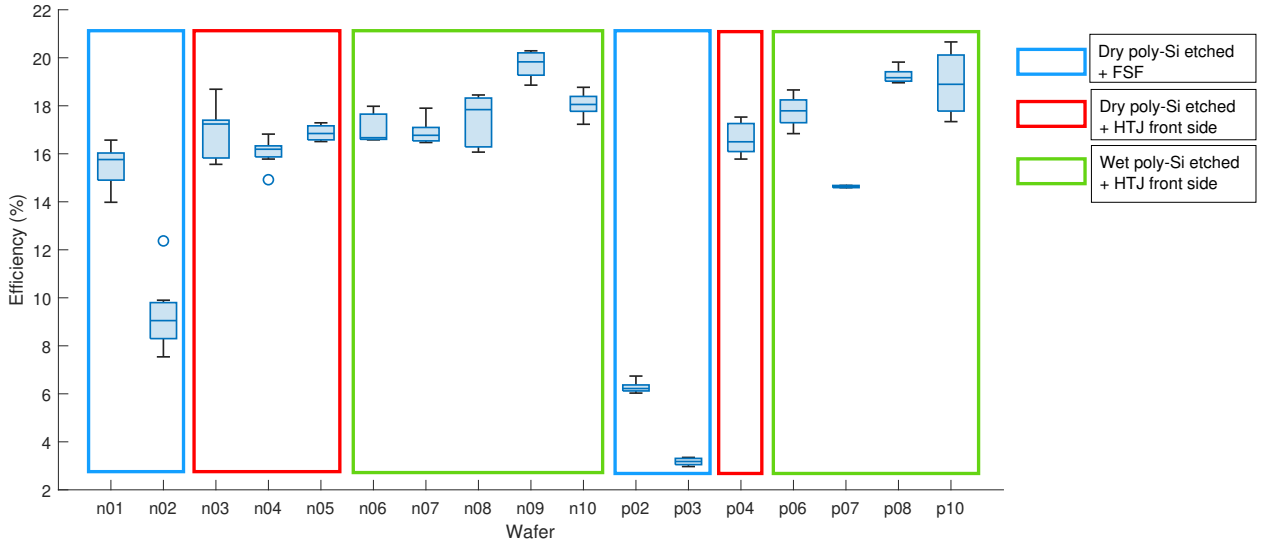


Figure 4.4: Comparison of solar cell power conversion efficiencies issued from different processes.

- Different Si_xN_y quality: the Novellus Concept 1 and the Oxford Plasmalab80Plus carry out the PECVD in (i) and (ii), respectively. Therefore, changes in optoelectrical properties are expected. Besides, the use of different deposition recipes probably resulted in different film thicknesses. Better light absorption and/or electrical passivation might happen in (ii).

- Different Si_xN_y etching methods: dry and wet etching are performed in (i) and (ii) respectively. Since the plasma etcher (Drytek Triode 384T) is also used to etch other materials, contamination can occur, leading to an increased contamination rate at the solar cell backside.

Process (iii) produced the best-performing ($\eta > 20\%$) n-type and p-type solar cells of the thesis. In Table 4.1, the (iii) cells differ from (ii) by a further increase of V_{OC}, J_{SC}, and FF, the latter in case of p-type. Consequently, since only the poly-Si etching method differs, surface passivation improvement at the c-Si/Si_xN_y interface can be assumed.

Finally, although (ii) and (iii) result is similar ranges of efficiency between n- and p-type cells, type-related differences can be pointed out. While Table 4.1 shows better V_{OC} and J_{SC} on p-type, the n-type solar cell fill factors are higher. Part of this can be explained by final-step annealing, which is only applied to the n-type cells. Indeed, section 4.2 showed that it leads to increased FF and decreased V_{OC}. Unequal BSF and emitter conductivity and passivation quality between n- and p-type cells can also explain the differences, while their surface areas do not vary from n-type to p-type design. Lastly, the substrate doping nature and density can also cause various bulk recombination.

Substrate	Process	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	η (%)
n-type	(i) Dry poly-Si etched + FSF	625	34.0 ± 0.8	78.1 ± 1.9	16.57
	(ii) Dry poly-Si etched + front side HTJ	639	36.6 ± 1.3	80.0 ± 2.8	18.69
	(iii) Wet poly-Si etched + front side HTJ	642	39.8 ± 0.2	79.4 ± 0.3	20.29
p-type	(i) Dry poly-Si etched + FSF	574	16.6 ± 0.2	70.7 ± 0.7	6.74
	(ii) Dry poly-Si etched + front side HTJ	647	38.6 ± 0.3	70.2 ± 0.6	17.53
	(iii) Wet poly-Si etched + front side HTJ	674	41.0 ± 0.1	74.8 ± 0.2	20.66

Table 4.1: Best-performing n-type and p-type solar cells per manufacturing process.

4.4. Conclusion

In this chapter, the results related to the device's solar cell performance were presented. First, a kink that was observed in multiple of the J-V curve was described. It occurs at relatively high currents and low voltages. Its cause remains unexplained; however, assumptions were provided. Parasitic diodes or capacitance inherent to the device or the measurement setup could explain it. The kink makes the short-circuit current and fill factor determination difficult. However, the open-circuit voltage and the maximum power point are not affected; the solar cell efficiency can thus still reach high values. The effect of post-metallization annealing on the solar cell was also inspected, highlighting different effects on n- and p-type cells. While the former exhibited post-annealing better performance, which is related to improved contact resistance, the latter suffered a large efficiency drop. This can presumably be explained by increased top-side surface recombination. Finally, the process flow variation was investigated. The worst-performing approach was the one involving an FSF, especially for p-type solar cells. Decreasing the implantation dose could be one promising option. On the contrary, the approach combining wet poly-Si and Si_xN_y etching and Si HTJ front side passivation exhibited the best performance, with maximum efficiencies of 20.29% and 20.66% reached for n-type and p-type substrates, respectively. N-type-based cells demonstrated the best fill factors, but the higher open-circuit voltages were achieved with p-type. The efficiencies reached demonstrate the potential for manufacturing high-efficiency solar cells using the combined process flow proposed in the thesis.

5

MOSFET characterization

This chapter reports the MOSFET characterization. To do so, the subsequent sections investigate how the variation in manufacturing or conditions affects the MOSFET DC parameters. First section 5.1 describes the methods that derive the DC parameters. Then, sections 5.2, 5.3, and 5.4 study the effect of post-metallization thermal annealing, the MOS design, and the manufacturing method on the parameters, respectively.

5.1. Parameters Derivation Methods

Before analyzing the effect of different features on the MOSFET parameters, we first explain how these parameters are extracted from the measurements. Two characteristics are obtained: I_D-V_{GS} describes the drain current evolution with the gate-to-source voltage at V_{DS} = 0.1 V; I_D-V_{DS} shows the relation between the drain current and the drain to source voltage. It is measured at several gate voltages. Figure 5.1 displays examples of both characteristics obtained from an NMOS. This chapter focuses on the three following steady-state parameters: the threshold voltage V_T, the on-resistance R_{ON}, and the leakage current I_{leak}.

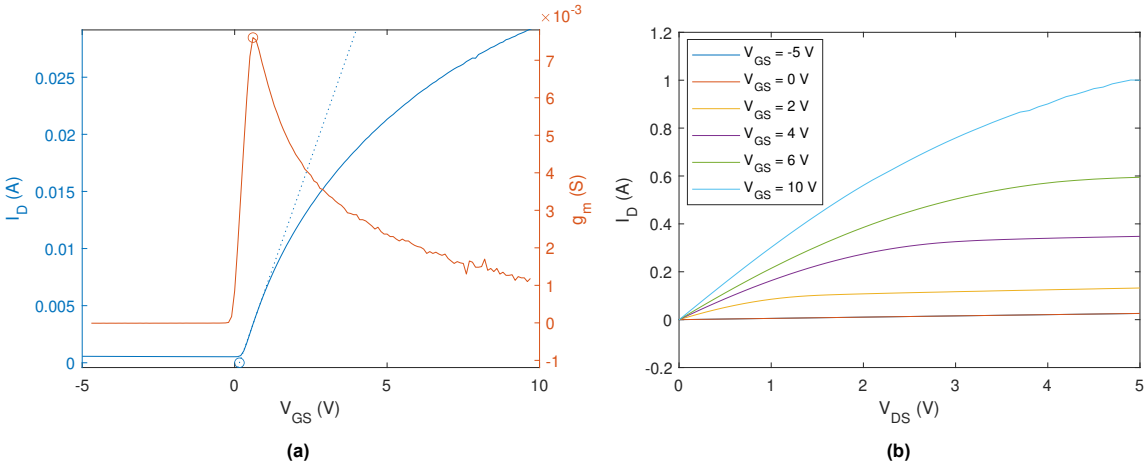


Figure 5.1: Characteristics of NMOS T2 from wafer N8: (a) I_D-V_{GS} characteristic in solid blue; g_m-V_{GS} in red; tangent at the maximum slope in dotted blue. (b) I_D-V_{DS} characteristics for increasing gate voltage.

According to the theory in subsection 2.3.2, no current flows between the drain and the source for a gate voltage below the threshold (in the NMOS case). However, in reality, subthreshold conduction occurs, in which little current can flow due to a relatively low channel resistivity [43]. Therefore, the threshold voltage cannot be defined as the first x-axis value for which the drain current starts increasing in the

I_D-V_{GS}. Instead, it is derived from the I_D-V_{GS} characteristic, using a linear extrapolation method [42]. First, the transconductance is derived from that characteristic, using Equation 2.11. Then, the I_D-V_{GS} curve's tangent corresponding to the maximum transconductance is drawn. The threshold voltage is the x-axis value for which that tangent is zero. Figure 5.1(a) illustrates that method. In that example, V_T = 0.157 V. Moreover, the on-resistance is derived from the linear region of the I_D-V_{DS} characteristic. Figure 5.1(b) shows an example of such characteristics from an NMOS. Following Equation 2.10 and at a 10 V gate voltage, R_{ON} = 3.18 Ω. The leakage current is the current that flows from the drain to the source in the absence of an electric field applied at the gate. That value varies with the drain voltage; however, we estimate it at V_{DS} = 0.1 V. Therefore, it is also determined from the I_D-V_{GS} curve. In Figure 5.1(a), I_{leak} = 528 μA.

5.2. Effect of Thermal Annealing

This section analyses the effect of post-metallization thermal annealing described subsection 3.3.7. To this end, one p-type and one n-type wafer were characterized before and after that process. Figure 5.2(a) and (b) plot I_D-V_{GS} characteristic of several NMOS and PMOS, respectively. The dashed and solid lines correspond to pre-annealing and post-annealing measurements, respectively. Those graphs show important changes occurring due to the process. Table 5.1 details the extracted threshold voltages, leakage currents, and maximum transconductance. The latter parameter is presented instead of the on-resistance for two reasons. First, it simplifies the analysis by extracting parameters from one characteristic only. Second, the on-resistance depends on the difference between the gate and the threshold voltages (Equation 2.10). Since the latter is altered by annealing, comparing on-resistances at the same gate voltage would not be relevant. Alternatively, they could be compared by keeping the difference between the gate and the threshold voltages constant. However, it would require a very large quantity of I_D-V_{DS} data. The following relation between the transconductance and the on-resistance (derived from Equation 2.10 and Equation 2.11 at low drain-to-source voltages) shows that similar information on channel conductivity can be derived:

$$g_m = \frac{1}{R_{ON}} \cdot \frac{V_{DS}}{V_{GS} - V_T} \tag{5.1}$$

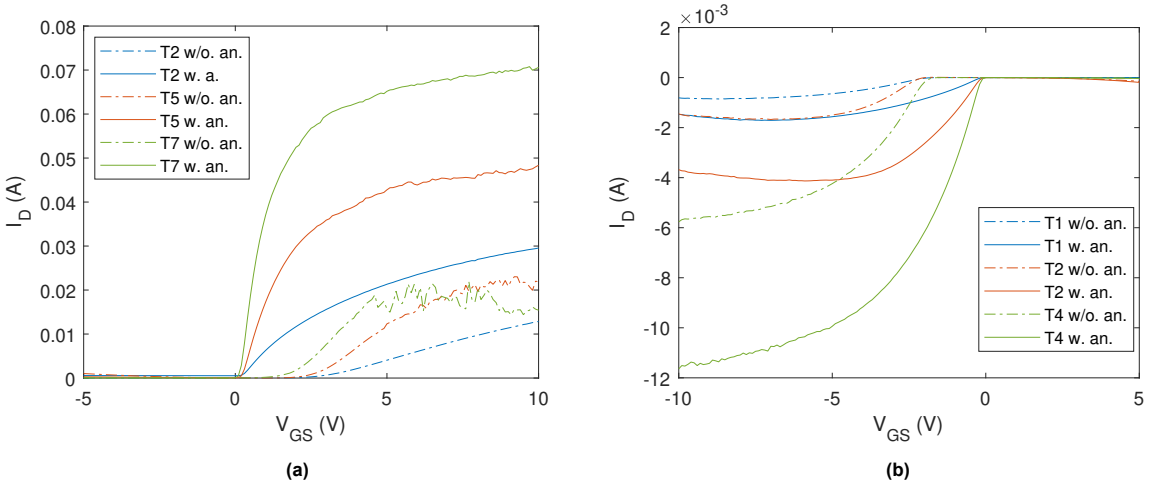


Figure 5.2: I_D-V_{GS} characteristics of several MOS. Dashed lines: before annealing; solid lines: after annealing. (a) NMOS from wafer P8; (b) PMOS from wafer N2.

The threshold voltage is strongly affected by thermal annealing. Its value experiences a shift in the negative direction for the NMOS and in the positive direction for the PMOS. Over the presented results, the largest shift for each MOS type is -2.82 V for NMOS T2 and +2 V for PMOS T2. However, the value always keeps the same sign (positive for NMOS and negative for PMOS); therefore, the device is still a channel enhancement mode transistor. This threshold shift can be disadvantageous to keep the switch in off-mode at 0 V gate potential, which is not well below the threshold voltage. Another drawback is the leakage current exhibits a global increase due to annealing. This is particularly

noticeable for NMOS T2, the post-annealing leakage current being significantly higher than the other values, and for PMOS, for which the increase is more significant. That effect is an annealing drawback since the transistor then conducts more current in the off-mode, which increases the off-mode power losses. Finally, the maximum transconductance rises with annealing. In particular, NMOS T2, T5, and T7 exhibit an increase by factors 4, 4.5, and 7.3, respectively. This can be related to the noisy curves observed in Figure 5.2(a) before annealing. The PMOSs show a raise by an approximate factor of 2.1. Improved transconductances mean that the same gate voltage variation involves more drain current change. This, along with the reduced threshold voltage, supports highly reduced on-resistances for the same gate voltage. Hence, it causes reduced on-resistance and thus improved performance.

Such changes in the parameters can be caused by multiple physical effects that result from this process. Thermal annealing is known to reduce the defect density of solid-state materials [43]. Therefore, in general, the change in performance can be explained by a decrease in dangling bonds at the film interfaces and of (charged) defects in some materials. In particular, as supported by Equations 2.8 and 2.9, the shift in the threshold voltage can be explained by less equivalent oxide charge. However, since V_{TN} and V_{TP} shift in opposite directions, the equivalent oxide charge would have opposite signs depending on the type of the transistor. A possible reason explaining that difference could be that the trap properties created during the oxide growth depend on the substrate's type. Furthermore, the increased transconductance and leakage current could be due to enhanced metal-semiconductor contacts at the drain and source terminals. This could also explain the reduction of NMOS T5 and T7 noisy behavior observed in Figure 5.2(a).

MOS id.	Annealing (w/o. or w.)	Threshold voltage (V)	Leakage current (μA)	Maximum transconductance (mS)
NMOS T2	w/o.	2.97	23.4	2.02
	w.	0.154	528	8.08
NMOS T5	w/o.	2.75	34.5	5.41
	w.	0.203	49.5	24.4
NMOS T7	w/o.	1.96	24.6	7.49
	w.	0.0878	56.4	54.9
PMOS T1	w/o.	-1.58	-0.0117	0.274
	w.	-0.146	-0.323	0.555
PMOS T2	w/o.	-2.14	-0.271	0.799
	w.	-0.141	-1.01	1.75
PMOS T4	w/o.	-1.93	-2.89.10^{-4}	2.03
	w.	-0.131	-2.61	4.34

Table 5.1: Comparison of the threshold voltage, leakage current, and maximum transconductance of annealed and not annealed MOSs. The NMOSs and the PMOSs are from wafers P8 and N2, respectively.

5.3. Effect of the Design

The different MOSFET designs described in section 3.4 explore multiple drain-source pairs, MOS widths, and MOS lengths. Besides, two additional designs (transistors T12 and T13) were explored. Figure 5.3 schematizes the different MOS patterns. In (a), representing the standard design, the gate has an S-shape and several interdigitated drain and source pairs (three in the diagram) are included. In (b), representing the transistor T12, several gates parallel-connected gates are present. The component's design includes an Si_xN_y layer between the gate and the drain are source to avoid connection where they overlap. In (c), representing the transistor T13, the drain-source pairs are separated from each other by a larger distance. In this section, the effect of the MOSFET design is on the electrical parameters is characterized. The on-resistance being expected to vary the most through the designs, it is subjected to a specific focus. However, impacts on the leakage current were also observed. Therefore, the latter is studied in a second subsection.

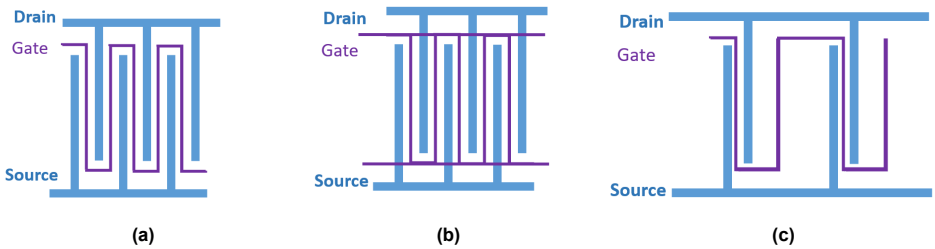


Figure 5.3: MOSFET design patterns: (a) interdigitated drain-source pairs with an S-shape gate; (b) several gates in parallel (T12); (c) separated drain-source pairs.

5.3.1. On-Resistance

The MOS structure is made of several interdigitated drains and sources that are separated by the gate. Therefore, it cannot be assimilated to several simple MOSs (i.e. MOS including only one drain-source pair) connected in parallel. The latter structure, built for T13 only, is however more convenient to theoretically predict the on-resistance. A number N_{pairs} of pairs with width W should be similar to a single pair with width $N_{\text{pairs}}W$. Accordingly, the on-resistance can be calculated from Equation 2.10. On the contrary, the mainly explored structure would require a more complex model involving more simple MOSs. In this structure, the current from a drain that is not at the extremity of the component can flow in two directions, since that drain is surrounded by two gates and sources. Hence, one can expect a higher drain current. If this is the case, increasing the number of drain-source pairs should decrease the on-resistance more sharply than with simple MOS' in parallel, in which case the on-resistance is an inverse function of the number of the pairs. Figure 5.4(a) confirms this expectation. That figure plots the on-resistance as a function of the drain-source pairs number for several gate-source voltages. One case notice that R_{ON} is no longer a reverse function of N_{pairs}. Instead, the trend can fit with a function such as:

$$R_{ON} \propto N_{\text{pairs}}^{-\alpha} \tag{5.2}$$

with $\alpha > 1$, a decreasing function of V_{GS}. The fitting is done with the software Microsoft Excel with a power trendline. It only includes transistors from wafer N6. The correlation coefficient (r^2) is consistantly higher than 0.995. According to these data, $\alpha(V_{GS} = 1V)$ = 1.39 and $\alpha(V_{GS} = 9V)$ = 1.15. It can thus be inferred that this MOS design is more efficient to reduce the on-resistance than the simple parallel MOS' design, but that the difference decreases at higher gate-source voltages. The observation is confirmed by Figure 5.4(d) that compares the on-resistance of an interdigitated drain-source structure with a separated drain-source pairs structure (T13). The former structure is less resistive; however, that relative difference diminishes at higher gate-source voltages.

Another method to decrease the on-resistance is the increase the channel width. However, that method is not as efficient as in theory according to chapter 2. A large channel width causes a lateral voltage drop due to the increased path length of the current [42]. Figure 5.4(b) illustrates the effect of an increased width on the on-resistance at several gate-source voltages. In a similar way as above, one can derive the following fitting function, with β < 1, a function of V_{GS} (with $r^2 \geq 0.99$):

$$R_{ON} \propto W^{-\beta} \tag{5.3}$$

Finally, another design parameter that affects the on-resistance is the channel length. According to Equation 2.10, R_{ON} ideally increases linearly with L. Figure 5.4(c) plots R_{ON} as a function of V_{GS} for two gate lengths: $4\ \mu$m in blue and $3\ \mu$m in yellow. One should expect values from the blue curve 1.33 times larger than the ones of the yellow curve, but the relative difference is in reality slightly smaller (the factor is 1.2 on average). However, only two components are compared here, a quantitative conclusion is thus not possible. That figure also shows a third curve in red, which is related to a MOS with a different gate design. That MOS is T12, it involves several gates connected in parallel instead of a single S-shape gate. That design results in an increased on-resistance. However, R_{ON} also decreases with V_{GS} more sharply than the one of the standard design. The smaller gate total width may explain that effect. In reality, since a very small current inevitably flows through the gate, a voltage drop might be

noticed at the end of very wide gates such as the standard S-shaped ones. That voltage drop would be more significant at higher gate-source voltages. Connecting several narrower gates in parallel may reduce the latter issue. Consequently, the parallel-gates design appears to be an interesting solution if high V_{GS} is employed.

On wafer N6, PMOS T7 exhibits an on-resistance of 1.86 Ω at V_{GS} = -10 V. A reflection on the possible integration of with a solar cell is possible. Assuming that this transistor is connected to a 1 cm^2-area solar cell that generates a 40 mA current, the drain-source voltage would be 74.4 mV and the dissipated power 2.98 mW. If one further assumes that the solar cell efficiency is 20% and thus generates a 20 mW power, 14.9% of that power would be dissipated by the transistor. To reduce that power dissipation, the on-resistance could be further reduced using the strategies that are described above. Alternatively, integrating several solar cells in series would also reduce the relative power dissipation.

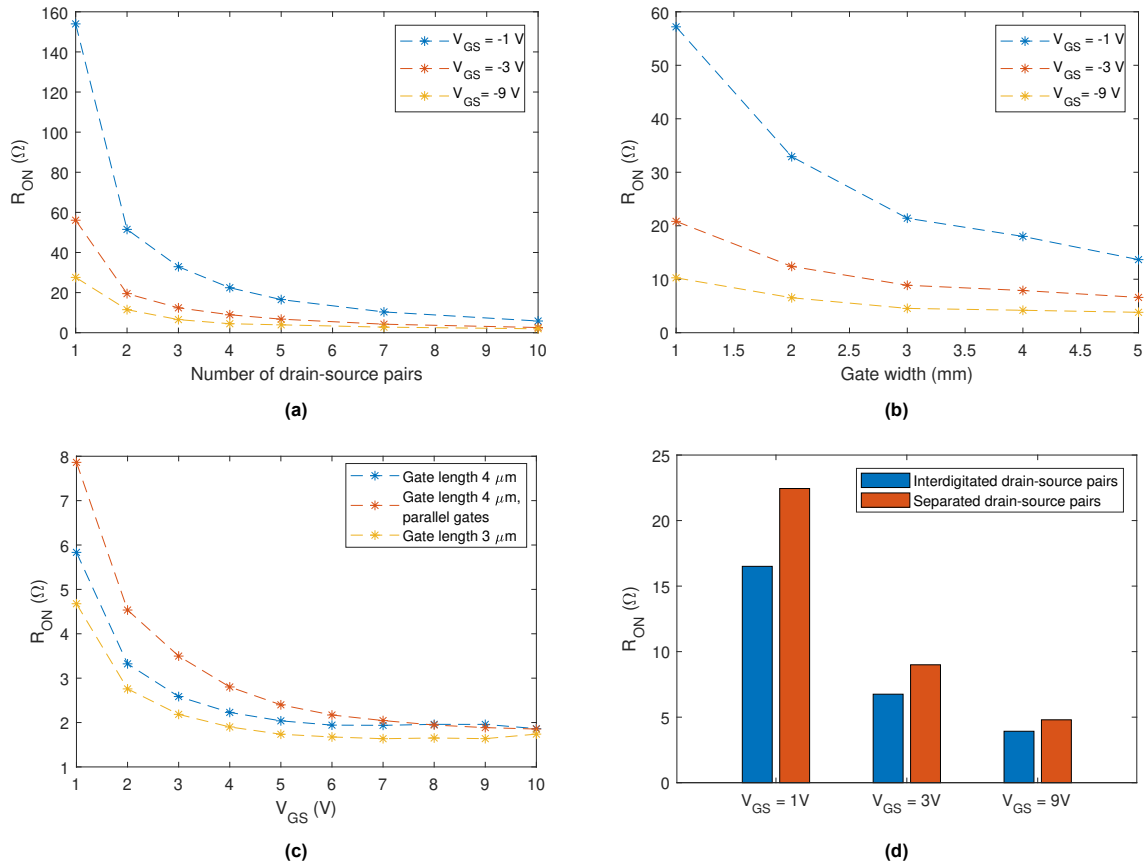


Figure 5.4: On-resistances of PMOSs from wafer N6 at several gate-source voltages for (a) variable drain-source voltage pairs, $L = 4$ μm, $W = 2$ mm; (b) variable gate widths, $L = 4$ μm; 3 drain-source pairs; (c) several gate lengths and designs, $W = 2$ mm; 10 drain-source pairs; (d) Interdigitated and separated drain-source pairs, $L = 4$ μm, $W = 2$ mm; 5 pairs.

5.3.2. Leakage Current

Although the design variation seeks to target the lowest possible on-resistance, it also affects the leakage current. Similarly to the above, the leakage current-design relationship is evaluated by extracting that value for the MOSs T1 to T14 from one wafer. From the collected data, similar categories have been extracted. Figure 5.5 illustrates that relationship. Since the displayed values are extracted from one wafer only, a quantitative evaluation must require precaution because part of the variations might be due to a lack of uniformity from a manufacturing process. However, clear trends can be observed. Figure 5.5(a) and (b) display the leakage current dependency of the drain-source pairs number and the gate width, respectively. It appears that the leakage current increases with both the pair's number and the width. This might be because the area that the total drain and source share with the body

increases, so the latter can conduct more charges. In Figure 5.5(c) the effects of a smaller gate length and of parallel gates are presented. The difference between the obtained leakage currents seems too insignificant to conclude any variation. Especially, a shorter gate does not seem to affect the leakage current. Finally, Figure 5.5 compares the interdigitated versus separated pairs designs. The latter involves less leakage, which is explained by the same reason provided in subsection 5.3.1.

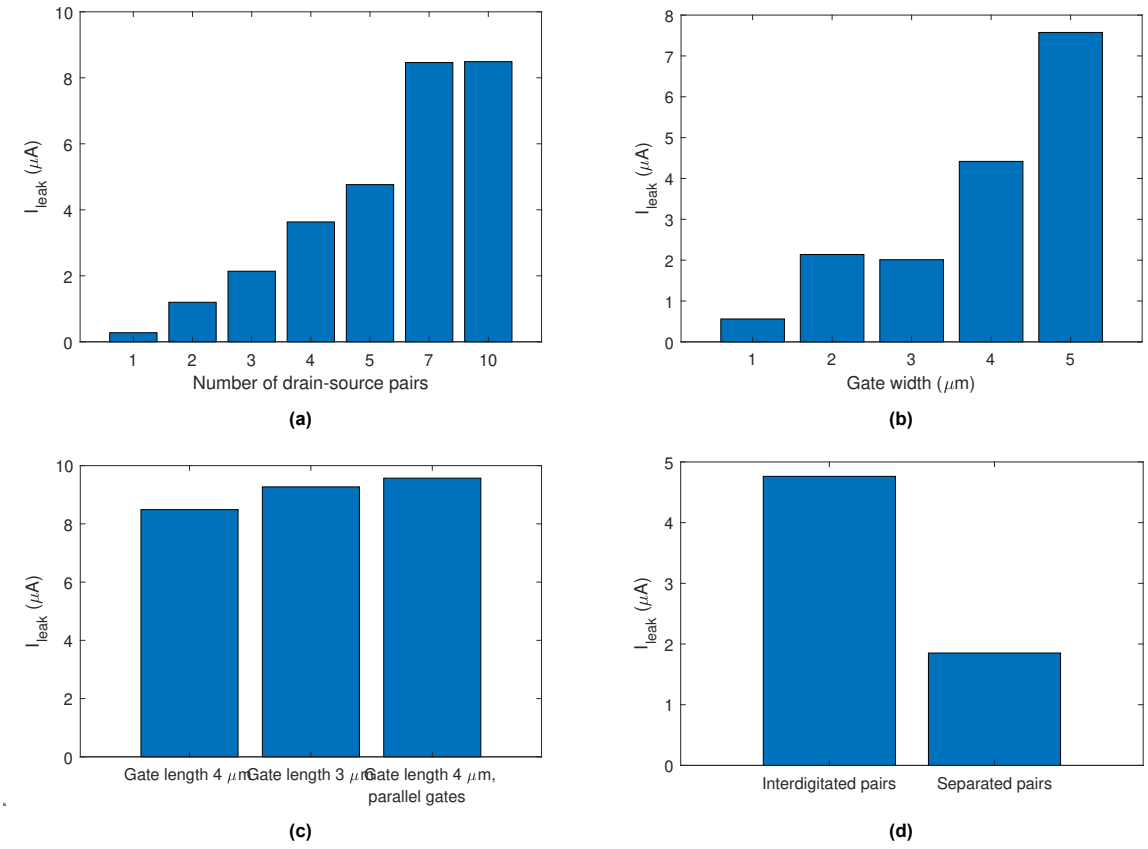


Figure 5.5: Leakage current of PMOS's from wafer N5 for: (a) variable drain-source voltage pairs, $L = 4$ μm, $W = 2$ mm; (b) variable gate widths, $L = 4$ μm, 3 drain-source pairs; (c) several gate lengths and designs, $W = 2$ mm, 10 drain-source pairs; (d) Intricated and separated drain-source pairs, $L = 4$ μm, $W = 2$ mm, 5 pairs.

5.4. Effect of the Manufacturing Methods

This section describes the impact of the three different manufacturing methods on the MOSFET parameters. To do so, the following subsections focus on the threshold voltage, on-resistance, leakage current, and breakdown voltage, respectively, of differently processed wafers. The parameters are statistically compared to exhibit average and standard deviation values. The former refers to the MOSFET performance, while the latter identifies the process uniformity and reproducibility.

5.4.1. Threshold Voltage

This section aims to verify whether the threshold voltage gets impacted by the differences in the manufacturing methods. Table 5.2 reports the average values of threshold voltage and their standard variation from PMOS and NMOS for each process. The values do not enable any conclusion on a variation of V_T with the process since the mean values of one MOS type are well within the uncertainty ranges set for the calculated standard deviations. Likewise, no significant trend can be extracted from the standard variations. Higher values are explained by smaller sets of data. Therefore, the threshold voltage uniformity and value are similar along the different processes. This is explained by Equations 2.8 and 2.9 that allow theoretical calculation of V_T. They highlight that this parameter depends on the gate thickness and quality, the metal and semiconductor work functions, and the Fermi levels. Hence,

the only processes affecting V_T are gate oxide growth and the gate poly-Si, drain, and source doping. These processes remain unchanged through the three compared process flows so no V_T variation is to be expected.

Type	Process	V_T (V)	σ_{V_T} (V)
PMOS	(i) Dry poly-Si etched + FSF	-0.164	0.030
	(ii) Dry poly-Si etched + front side HTJ	-0.179	0.058
	(iii) Wet poly-Si etched + front side HTJ	-0.141	0.022
NMOS	(i) Dry poly-Si etched + FSF	0.148	0.069
	(ii) Dry poly-Si etched + front side HTJ	0.186	0.088
	(iii) Wet poly-Si etched + front side HTJ	0.206	0.126

Table 5.2: Average and standard deviation of PMOS and NMOS threshold voltages per manufacturing process.

5.4.2. On-Resistance

The previous section proved no correlation between the threshold voltage and the process flow variations. The reason was that those differences do not affect the properties of the materials involved in the value of V_T. On the contrary, they can affect the gate dimensions and thus alter the on-resistance. Figure 5.6 compares the R_{ON} of PMOS T10 obtained at V_{GS} = -8 V and NMOS T10 obtained at V_{GS} = 8 V for differently processed wafers. On both PMOS and NMOS, a large R_{ON} drop is observed between the third (green rectangles) and the two first (blue and red rectangles) process flows. This is explained by the difference in poly-Si etching. As detailed in subsection 3.3.4, due to its multi-directional aspect, wet chemical etching also laterally operates under the mask and thus reduced the gate length. In turn, shorter length causes shorter R_{ON}. This effect is amplified if the etching time increases. Consequently, the R_{ON} evolution from wafer n6 to n10 verifies the expectation. Indeed, Table 3.1 reports different etching times; and combining these values with the result from Figure 5.6 correlates etching time increase with on-resistance decrease. Less R_{ON} variation is observed between the first (blue rectangles) and the second (red rectangles) process flows. One can assume smaller R_{ON} in the second case. This can be attributed to the different Si_xN_y techniques since the first and the second method involve dry and wet nitride etching, respectively. In the latter case, the previously mentioned side under-etching can occur and result in larger Si_xN_y openings, hence better contacts between the metal contact and both the drain and source. Thus, a possible explanation for the on-resistance fluctuation between n3, n4, and n5 could be found in the higher nonuniformity of wet etching compared to dry etching. However, the lack of displayed data limits any conclusion. Finally, Figure 5.6 exhibits unequal resistance between NMOS and PMOS. This can be caused by the difference in mobility between minority holes and electrons. Since the electrons' mobility is higher than the holes, NMOSs carry more current than PMOSs; the latter is, therefore, more resistive.

Combining the comparison between the wafers with the MOS design analysis that was presented in subsection 5.3.1, it is possible to select the PMOS and NMOS exhibiting the lowest on-resistance. PMOS T7 of wafer N10 has an on-resistance of 1.29 Ω at V_{GS} = -10 V. NMOS T12 of wafer P10 has an on-resistance of 1.01 Ω at V_{GS} = 10 V.

5.4.3. Leakage Current

The dependence of the leakage current on the processing method and MOS type is explored in this section. Table 5.3 provides average and standard deviation values of the leakage current related to the three different processing methods. Noticeable differences in average and standard deviation appear between NMOS and PMOS (in absolute values), with the latter having average leakage current smaller by two orders of magnitude. This effect may be explained by different dopant densities between the n^+ and p^+ poly-Si gates. To understand that effect, a closer look at the MOS junction band diagram involving that gate material is necessary. It is displayed in Figure 5.7 [70], representing the case of n^+ poly-Si gate with a p-type body. The left, middle, and right parts schematize the gate, oxide, and body, respectively. On the body side, a curvature of the energy levels is observed, which ensures the vacuum energy continuity (represented by the top line). It results in a switched order between the intrinsic and the actual Fermi levels close to the gate: $E_{Fi} < E_F$. This is called a "weak inversion regime": close

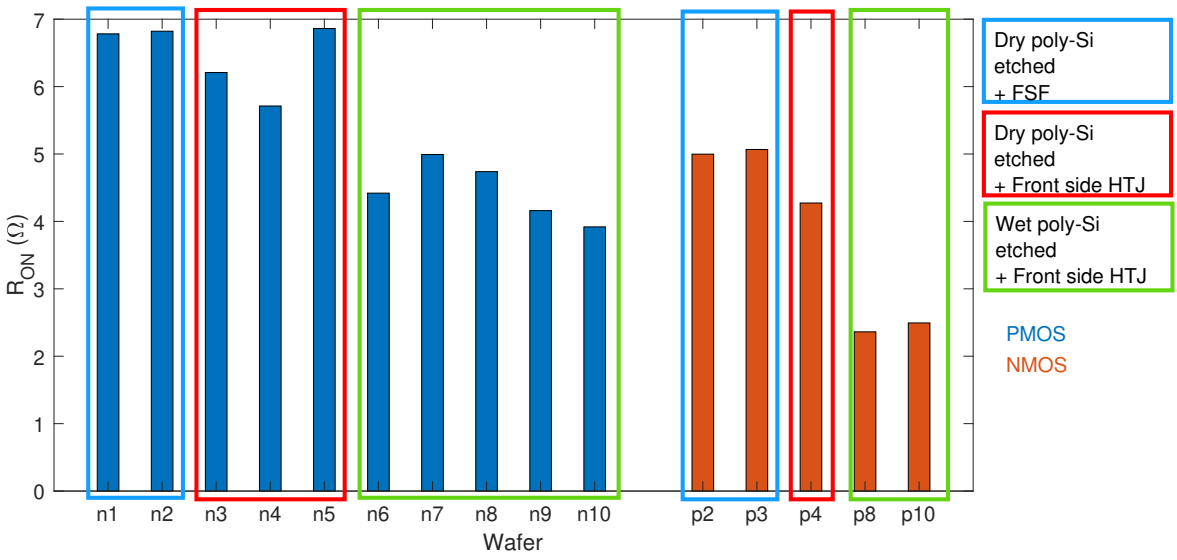


Figure 5.6: On-resistance of PMOS at V_{GS} = -8V and NMOS at V_{GS} = 8V.

to the oxide, the body acts more like an n-type semiconductor [43]. That regime explains conducting capability of the body even at V_{GS} = 0 V. This effect is here illustrated for an NMOS and it is similar for a PMOS. However, in the figure, the dopant concentration is considered high enough to approximate $E_F \simeq E_C$ in the left-hand corner. For lesser doping, $E_F < E_C$, resulting in less curvature of the energy levels on the body side. Therefore, a less doped p^+ than n^+ poly-Si gate could result in weaker inversion, hence a lower leakage current. Alternatively, the leakage current difference could also be caused by different defect densities between the substrate types.

Type	Process	Wafer	I_{leak} (μA)	$\sigma_{I_{leak}}$ (μA)
PMOS	(i) Dry poly-Si etched + FSF	n1, n2	-4.06	4.99
	(ii) Dry poly-Si etched + front side HTJ	n3 to n5	-3.18	2.60
	(iii) Wet poly-Si etched + front side HTJ	n6 to n10	-8.40	10.1
NMOS	(i) Dry poly-Si etched + FSF	p2, p3	110	125
	(ii) Dry poly-Si etched + front side HTJ	p4	124	117
	(iii) Wet poly-Si etched + front side HTJ	p8, p10	154	204

Table 5.3: Average and standard deviation of PMOS and NMOS leakage current per manufacturing process.

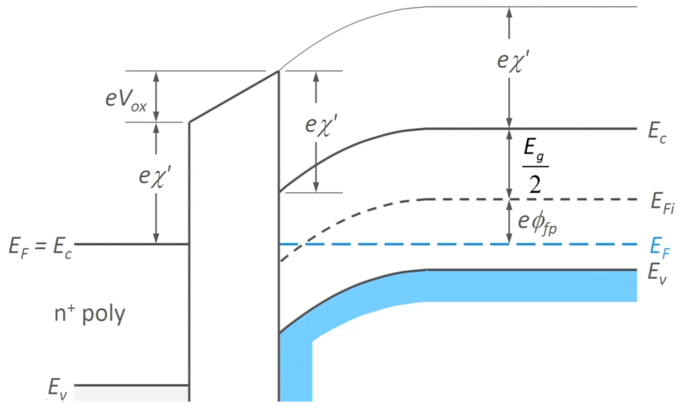


Figure 5.7: Energy band diagrams of MOS junctions involving highly doped n^+ poly-Si as the gate and p-type body [70].

No consistent variation can be observed between processes (i) and (ii). However, Larger I_{leak} are

observed for the method (iii). This can be explained by the gate length reduction, which reduced the distance and thus the resistance between the drain and the source. It also causes the standard variation increase, which is amplified by the nonuniform nature of wet poly-Si etching that results in more various values. However, that change is not significant. Figure 5.8 displays a heatmap of $|I_{leak}|$ obtained from the MOSFETs of each wafer. This representation is convenient to represent the variation of I_{leak} along with two parameters. A column contains the values for varying MOS designs on the same wafer. A row contains the values for varying wafers with a fixed design. The process flows related to the wafers are reported in Table 5.3. The dark blue pixels are related to dysfunctional MOSFETs. The results exhibit a higher dependence on the MOS design (see section 5.3) than the wafer number. Relative reproducibility can thus be concluded. Consequently, the effect of a process flow change on the leakage current is minor.

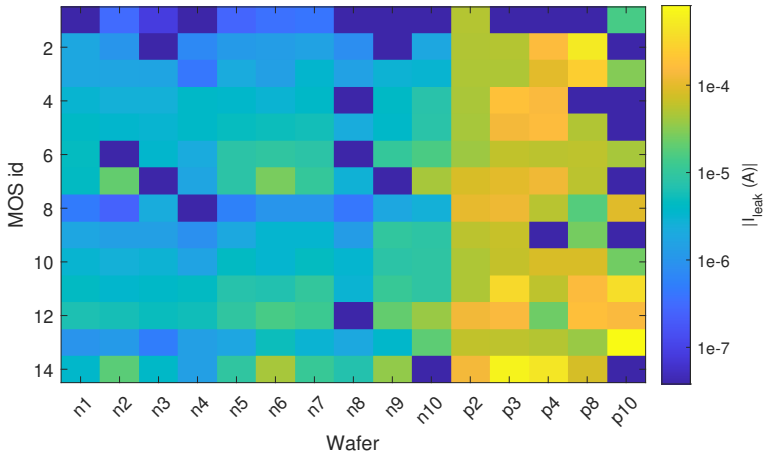


Figure 5.8: Heatmap of the leakage current absolute value for all MOSFETs of each wafer. Dark blue pixels are related to dysfunctional devices.

5.5. Conclusion

This chapter analyzed the effect of thermal annealing, design, and process flow variation on the MOSFET steady-state performance. First, post-metallization thermal annealing was demonstrated to reduce the NMOS threshold voltage by up to 2.82 V in the negative direction, and increase the PMOS threshold voltage by up to 2 V in the positive direction. The process also increases the transconductance, hence improving conductive capabilities in the on-mode. However, the off-mode performances seem to be reduced due to an increased leakage current. Those parameter variations can be supported by an improved metal-semiconductor interface that reduces ohmic contacts and a reduced defect density at the oxide-semiconductor interface. Second, the explored MOS designs exhibited a reduced on-resistance with increased drain-source pairs and gate width or a decreased gate length. Alternative designs involving separated drain-source pairs or parallel gates have been explored. The former resulted in a higher on-resistance, while the latter can be interesting at high applied gate voltages. However, designs improving the on-resistance also exhibited higher leakage current, hence worsened off-performance. Furthermore, the comparison of different process flows indicated that smaller on-resistances can be achieved by performing wet instead of dry poly-Si etching. Here again, increased leakage current seems to be a counterpart. Larger on-resistances were observed on NMOSs than on PMOSs, which can be related to the difference in mobility between electrons and holes. Combining optimal design with optimal process flow, the NMOS and PMOS on-resistance values reached 1.01 Ω and 1.29 Ω, respectively. Finally, the PMOS showed leakage currents almost two orders of magnitude lower than the NMOS. This could be due to unequal poly-Si gate doping density, resulting in a more important weak inversion regime at the zero gate voltage for the NMOS.

6

Interactions Between the MOSFET and the Solar Cell

This chapter analyses the interactions between the MOSFET and the solar cell. To that end, the performances of a MOSFET in illuminated conditions are first presented. Second, the combined monolithically interconnected MOSFET and solar cell are tested.

6.1. Effect of Light on the MOSFET

The behavior of illuminated MOS transistors was studied in [42], with a light source illuminating the component's side that involves the source, drain, and gate. A consequent leakage drain current increase was observed. The explanation is that electron-hole pairs are created due to the absorption of a photon and resulting minority charge carriers get collected by the drain. In our design, the same effect is expected to happen. However, in this work, the other side of the wafer is illuminated, and more light is absorbed due to the ARC and texturing treatment. The solar simulator described in subsection 3.2.4 being used, the illumination conditions are a 1000 W/m^2 irradiance for an AM 1.5 spectrum. Figure 6.1 displays in (a) and (b) the dark and illuminated I_D-V_{GS} characteristics obtained for an NMOS and a PMOS, respectively. A y-axis logarithmic scale is used to enable easier comparison of very small currents. Similarly to [42]'s observation, the off-current increases significantly due to illumination. At V_{GS} = -2 V, the NMOS drain current increases by a factor of 17 due to illumination. At V_{GS} = 2 V, the PMOS drain current increases by a factor of 8 due to illumination. Note that these relative differences are lower than the ones reported in [42] (the factors were 34 and 4.10^6, respectively). It is mainly due to noticeably higher leakage currents in the dark in our case (especially for the PMOS). No noticeable difference is observed once the gate voltage surpasses the threshold. This is because the photocurrent becomes negligible compared to the current that the channel can conduct in a strong inversion regime.

The consequence of this on the MOSFET's operation is that its blocking capability that is expected in off-mode is reduced, while the on-performance is unchanged. To seek optimal performance, that effect should therefore be avoided. An optical filter could be introduced on top of the transistor to prevent photons to be absorbed. Alternatively, a new design in which the device is less sensitive to this effect can be investigated.

6.2. Monolithically Connected MOSFET and Solar Cell

The monolithically connected MOSFET and solar cell characterization is performed using the setup described in subsection 3.2.4. The components are connected in series. In the wafer layer provided in Figure 3.13, the solar cells and transistors that can be involved are C2 to C5 and T19 to T22, respectively. As described in section 3.4, these transistors have 4 metal pads since the body is not in contact with the source. Therefore, the drain and source terminals are interchangeable. However, in practice, they have to be chosen such that the solar cell's current flows in the right direction. Figure 6.2 illustrates the connections between the characterized components. Both a PMOS with an n-type cell and

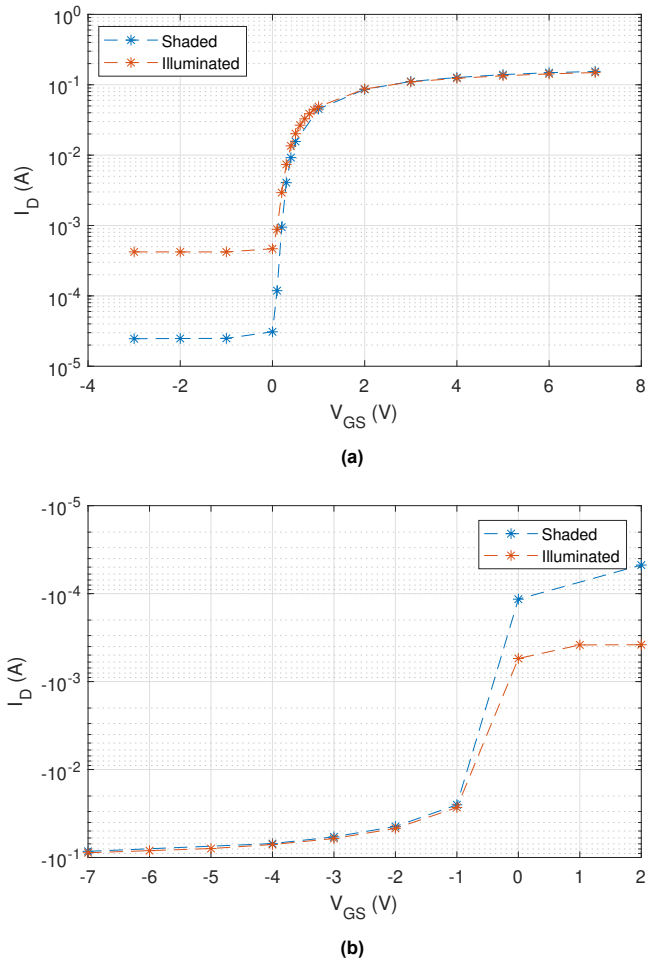


Figure 6.1: I_D-V_{GS} characteristics for dark and illuminated: (a) NMOS T22 from wafer p8; (b) PMOS T21 from wafer n9.

an NMOS with a p-type cell are measured. In the PMOS, a negative current conventionally flows from the drain to the source. Thus, the drain is connected to the negative contact (cathode) of the solar cell: $I_D = -I_{PV} < 0$. In the NMOS, a positive current flows from the drain to the source. Thus, the drain is connected to the positive contact (anode) o the solar cell: $I_D = I_{PV} > 0$. During measurements, a voltage sweep is applied to the combined components. That sweep includes the solar cell's and the drain-to-source transistor's voltages:

$$V_{\text{sweep}} = V_{PV} - |V_{DS}| \tag{6.1}$$

The involved solar cells and transistors are also measured separately. However, even though the notations "MOS alone" and "solar cell alone" are then used, note that the monolithic interconnection remains, meaning that electrical interactions between the components are still possible The subsequent subsections analyze the behavior of the monolithically interconnected components for both types with shaded and illuminated MOSFET conditions, respectively. This is achieved with different measurement masks, one without and out with an opening above the MOSFET.

6.2.1. Shaded MOSFET

Figure 6.3(a) and (b) plots the I-V characteristics of the components introduced in the introduction of this section, related and the n-type and p-type substrates, respectively, measured at several gate potentials. The figures also include the characteristics of the solar cells alone that act as references. One can notice the presence of kinks as described in section 4.1. For simplicity, the short-circuit current is defined by the maximum current value achieved by the curve. In both figures, the open-circuit does not seem to vary with the gate-to-source voltage. In fact, the MOS is operated at a low drain-to-source

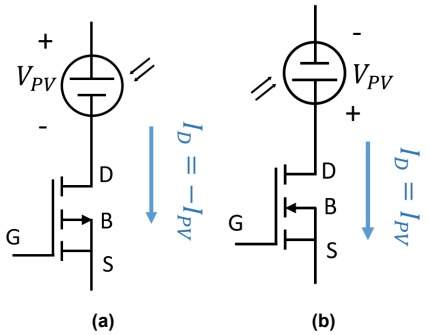


Figure 6.2: Connections between the solar cell and the transistor: (a) C3 and PMOS T20 of wafer n6; (b) C2 and NMOS T19 of wafer p6.

voltage regime; hence, it is similar to a resistor. Since the components are connected in series, the combined device is similar to a solar cell with a larger series resistance that depends on the gate voltage. Increasing series resistance results in decreasing fill factor and efficiency values. The largest obtained fill factors are cases (a) and (b) are for -7 V and 7 V gate voltages, respectively. Table 6.1 reports their values. They can be compared with the ones obtained without the MOSFET, for which the fill factors and thus the efficiencies are higher due to lower series resistance. Whereas the n-type cell's efficiency drops by 1.67% (absolute value) with the introduction of the MOSFET, the p-type cell drops by 0.75%. Therefore, in the latter case, the relative efficiency drop is 4.4%. For gate potentials close to 0 V ($|V_{GS}| < 0.5$ V), the series resistance becomes high enough to reduce the short-circuit current. The lowest values are obtained at 0 V and are reported in Table 6.1. However, the current is not zero, as it would have been desired from an ideal switch operation. This is due to the relatively low off-resistance of the MOSFETs. That issue is analyzed in more detail in the next paragraphs.

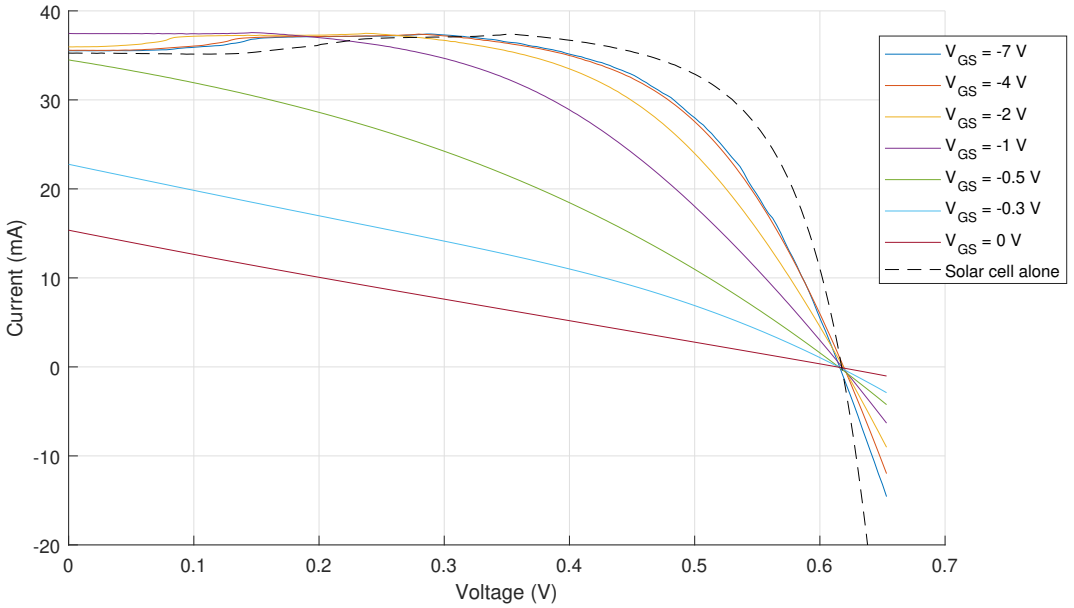
cell type	V_{GS} / no MOSFET	FF (%)	I_{SC} (mA)	η (%)
n-type	cell alone	71.4	37.4	16.46
	-7 V	64.2	37.4	14.79
	0 V	24.2	15.4	2.28
p-type	cell alone	68.6	39.0	17.09
	7 V	66.1	39.0	16.34
	0 V	25.0	12.8	2.00

Table 6.1: Performance of the n- and p-type solar cells with or without the MOSFET. Comparison of the fill factor, short-circuit current, and efficiency.

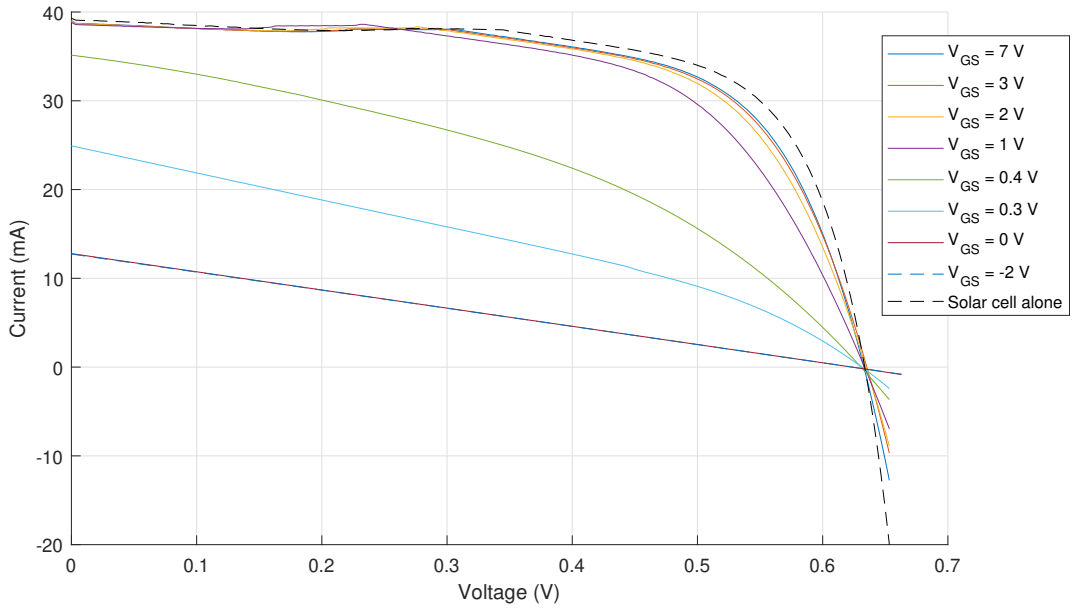
A quantitative study of the MOSFET's on- and off-performance requires deriving its equivalent resistance. It is derived from the data displayed in Figure 6.3 via series resistance derivation. The global series resistance is obtained by calculating the derivative of the voltage with respect to the current at the open-circuit voltage. Then, it is subtracted by the solar cell's one to derive the MOS resistance:

$$R_{\text{MOS}} = -\left.\frac{\mathrm{d}V}{\mathrm{d}I}\right|_{V=V_{OC}} + \left.\frac{\mathrm{d}V}{\mathrm{d}I}\right|_{V=V_{OC}}^{\text{cell alone}} \tag{6.2}$$

This value can then be compared with the reference off- or on-resistance, obtained from standard I_D-V_{DS} characteristics. Figure 6.4 includes both in a logarithmic scale as a function gate-to-source voltages, for the PMOS and the NMOS. The plots exhibit a consistent gap between the MOS + solar cell and MOS-alone curves. It suggests that, when the PV cell is included in the measurement, the MOS equivalent resistance is multiplied by a factor of 2.7 average value. That factor does not vary with the type of transistor. Such a higher resistance is a drawback in the on-mode but advantageous in the off-mode of the transistor. A possible explanation supporting the observed multiplication could be a lack of reliability of one of the resistance derivation methods. For example, the approximation of Equation 6.2 could cause a consistent overestimation of the resistance. Otherwise, it could be due to unexpected



(a)



(b)

Figure 6.3: I-V characteristics of monolithically connected solar cell and transistor: (a) n-type solar cell and PMOS; (b) p-type solar cell and NMOS. The transistor is in the dark.

electronic interactions between both components. One can also notice relatively low resistance values. At a 0 V gate potential, the I_D-V_{DS}-derived off-resistances of the PMOS and NMOS are 13.3 Ω and 15.6 Ω, respectively, while an expected value should be over 1 kΩ to ensure satisfying insulating capabilities. Moreover, the on-resistances obtained from the same components at -7 V and 7 V are 0.50 Ω and 0.19 Ω, respectively. In comparison, the lowest value presented in chapter 5 for an NMOS with the same gate width and drain-source pairs is 1.01 Ω. Such low values could be explained by electronic interactions between the MOSFET and the solar cell. Indeed, both components remain monolithically interconnected and in close proximity. Therefore, charge carriers could flow from the MOSFET to the solar cell through the metal connection or through the bulk. Alternatively, the low resistance could be

caused by high MOSFET conductive capabilities, which would also result in low blocking capabilities in the off-mode.

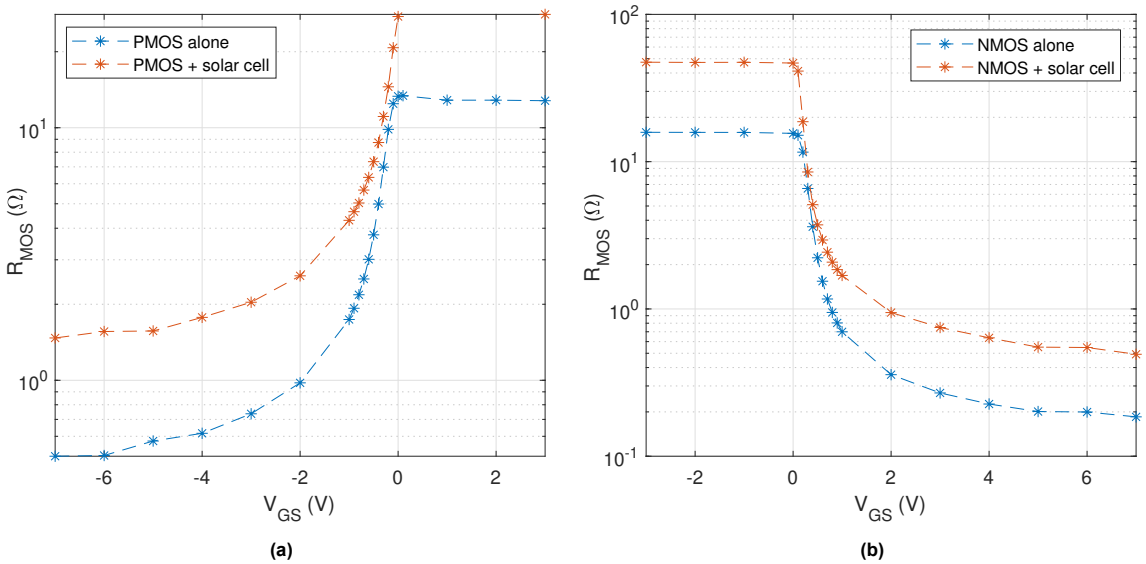
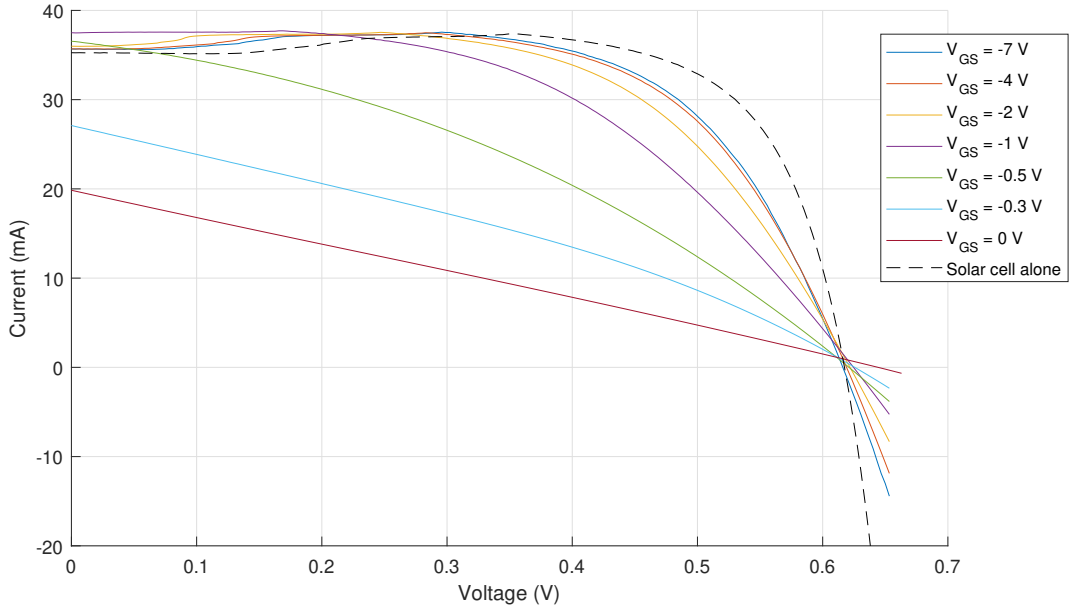


Figure 6.4: Comparison of the MOS equivalent resistance (off- and on-resistance) with and without including the solar cell in the measurement: (a) PMOS case; (b) NMOS case.

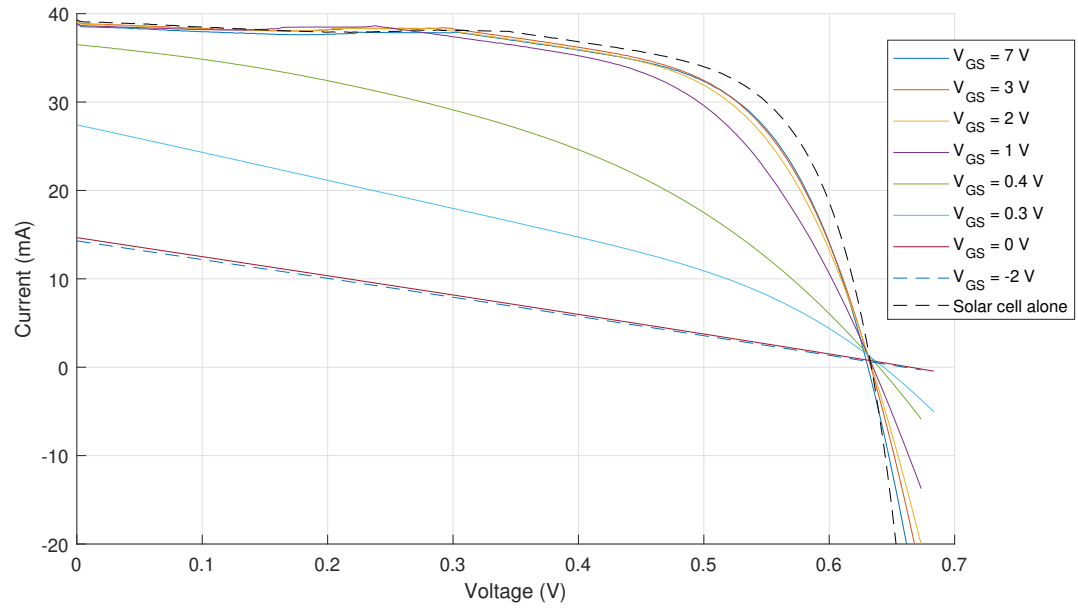
6.2.2. MOSFET Under Illumination

Sections 6.1 and 6.2.1 presented the impact of illumination and monolithic connection with a solar cell on the MOSFET, respectively. This subsection presents the behavior of that MOSFET when both conditions are cumulated. Figure 6.5(a) and (b) display characteristics of the same connected MOSFETs and solar cells as described in subsection 6.2.1, but with the MOSFETs under illumination. Only the reference curves related to the cell alone are kept unchanged. The description is similar to the above. Especially, in the on-mode of the transistor, the characteristics seem to remain unchanged compared to the ones with the shaded MOSFETs. This results in equal efficiency results. This observation was expected since section 6.1 showed that illumination does not affect the transistor in the on-mode. However, differences with subsection 6.2.1 are visible at gate voltages close to 0 V. In particular, the short-circuit currents are increased. Figure 6.6(a) and (b) show that the difference in I_{SC} between illuminated and dark conditions increases when the gate voltage of the PMOS increases and when the gate voltage of the NMOS decreases. The illuminated short-circuit current then becomes larger. In Figure 6.6(a), the difference reaches a maximum value of 4.48 mA at V_{GS} = 0 V. This is directly related to a decrease of the MOS resistance from dark to illuminated condition at that gate potential range, as observed in Figure 6.6(c) and (d). Also there, the maximum change occurs at zero gate-to-source potential.

One possible explanation supporting the shift in MOS equivalent resistance could be that, under illumination, the MOSFET acts as a secondary current source due to the photovoltaic effect, that adds up with the solar cell's photocurrent. To verify this, the PMOS's behaviors at zero gate potential in both illuminated and dark conditions are compared. Figure 6.7 plots I_D-V_{DS} characteristics at V_{GS} = 0 V under both conditions. The curve corresponding to dark conditions exhibits a relatively sharp slope that illustrates the poor resistive quality of that MOSFET in off-mode, as previously mentioned. In comparison, the illuminated characteristic exhibits a sharper slope, which illustrates that the off-resistance is further decreased. However, a photo-generated current does not depend on the drain-to-source voltage; therefore, a constant current difference between both conditions could have been expected instead of increasing for a decreasing drain-to-source voltage. Nevertheless, the observation could be justified by a voltage-dependent charge carriers flow. At V_{DS} = 0 V, the source and the drain are at the same potential; hence, the photo-generated holes are indifferently collected by both p-type regions



(a)



(b)

Figure 6.5: I-V characteristics of monolithically connected solar cell and transistor: (a) n-type solar cell and PMOS; (b) p-type solar cell and NMOS. The transistor is illuminated.

beneath the source and drain contacts that act like solar cell emitters. However, at V_{DS} < 0 V, the drain's potential is lower than the source's and the depletion region at the drain-body junction is wider than at the source-body junction. Therefore, holes would be more likely to drift toward the drain than toward the source. Thus, the drain would collect more holes than the source, hence further decreasing I_D.

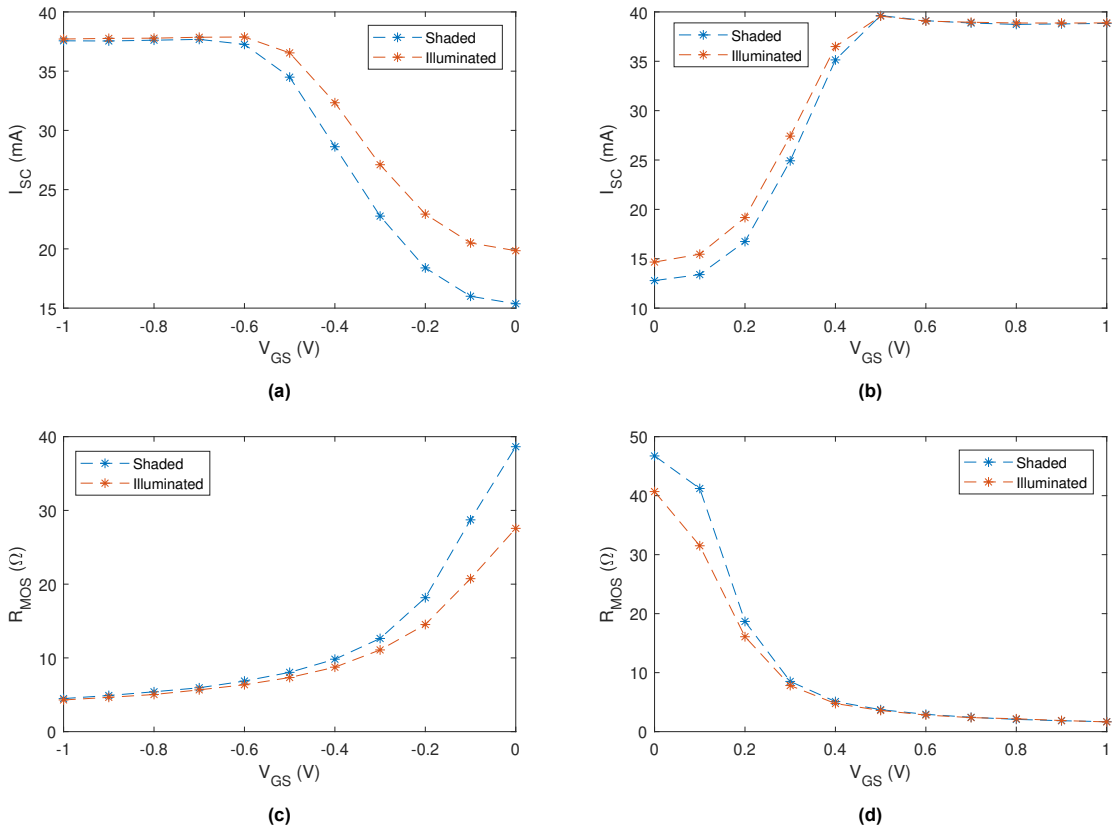


Figure 6.6: Evolution of the short-circuit current and MOS equivalent resistance with the gate potential in the dark and under illumination: (a) short-circuit current with the n-type solar cell and PMOS; (b) short-circuit current with the p-type solar cell and NMOS; (c) PMOS resistance; (d) NMOS resistance.

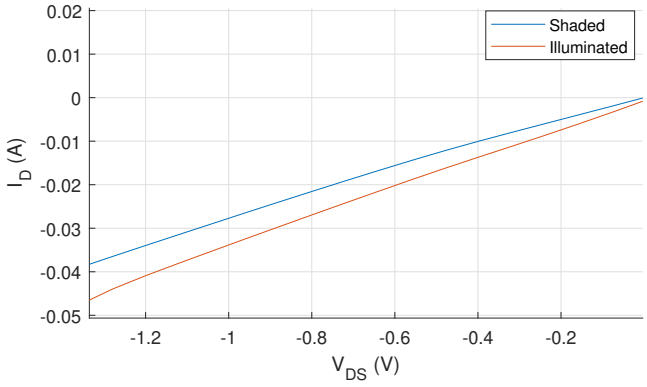


Figure 6.7: Illuminated and dark MOS I_D-V_{DS} characteristic at V_{GS} = 0 V.

6.3. Conclusion

In this chapter, the MOSFET's behavior under illumination and in the presence of a solar cell has been studied. When subjected to light, results have shown that the transistor's leakage current is increased, which may be caused by photogenerated charge carriers. This reduces the off-mode transistor's performance. On the contrary, no change was observed in the on-mode. When monolithically connected to a solar cell, the influence of the MOSFET on the solar cell energy generation was proved, with I-V characteristics directly depending on the gate potential. Compared to isolated transistors, the monolithically connected MOSFET exhibits lower on- and off-resistances. In the on-mode, this helps reduce the power dissipated by the transistor. Hence, the on-resistance of the NMOS leads to a 4.4% relatively lower efficiency of the PV/MOSFET combination compared to just the PV generator. However, in the off-mode, the low resistance results in poor blocking capabilities of the transistors. These observations could be explained by electronic interactions between both components through the bulk of the wafer. Finally, the results exhibited that, under illumination, the MOSFET conducts more current in the off-mode. Therefore, its performance is further reduced.

7

Conclusions and Recommendations

This thesis studied the fabrication of both a TOPCon IBC solar cell and a lateral MOSFET into the same c-Si wafer. To do this, a process flow was introduced to perform the combined manufacturing. To the best of the author's knowledge, monolithically connected high-performance designed solar cells and transistors were created for the first time. Both components were separately characterized; then, connected components were analyzed. In this chapter, the main findings of this thesis are summarized in line with the research questions defined in the introduction. Then, recommendations aiming to support further research on the subject are provided.

7.1. Conclusion

The thesis's first research question was how integrating the solar cell and the MOSFET on the same substrate simultaneously affects their performance. Several variations in the process flow are explored and the resulting devices are first characterized separately. First, wet and dry processes are considered for etching the poly-Si layer, which is used as the solar cell's emitter and BSF and as the MOSFET's gate. For both components, wet poly-Si etching results in the best performance. In particular, this process affords better passivation quality of the solar cell, hence increasing the open-circuit voltage and power conversion efficiency. The MOSFET benefits from a collateral effect of the etching method, which decreases the gate length and thus the on-resistance. However, it means that the gate length control is more challenging since its actual value is different from the designed one. Furthermore, different front-side passivation approaches were tested. Lightly doped FSF combined with SiO_x/Si_xN_y:H ARC and (i)a-Si:H with Si_xN_y:H ARC are compared. The latter approach results in the best efficiencies obtained. Finally, the effect of post-metallization thermal annealing is inspected. It highly reduces the MOSFET's threshold voltage absolute value and increases the transconductance. Therefore, the device can work at a lower gate voltage regime, and lower on-resistances are achieved. However, the near-zero threshold voltage would make it necessary to operate the transistor the NMOS (or PMOS) at negative (positive) gate potentials to ensure off-mode. Finally, post-metallization annealing affects the solar cell differently depending on the substrate's type. While n-type solar cells exhibit better performance after annealing thanks to reduced contact resistance, p-type solar cells' efficiency globally reduces noticeably. Further optimization of that step is thus necessary on that substrate type to ensure MOSFET performance enhancement while not harming the PV cell.

The second research question was aiming to find the effect of the substrate type on the devices' performance. Over the measurements performed, the best-performing solar cell is a p-type, for 20.66% efficiency. On the other hand, the best n-type solar cell reaches 20.29% efficiency. Despite the similar performance, p- and n-type PV cells differ in two parameters. While the former exhibit larger open-circuit voltages, the latter are higher in fill factor. These observations could be explained by better passivation and contact resistance, respectively. For the transistor, the NMOS exhibits lower on-resistance than the PMOS. The respective lowest reached values are 1.01 Ω and 1.29 Ω. This is presumably related to the higher charge carrier mobility of electrons compared to the holes. It would eventually result in better on-mode performance. However, the NMOS also demonstrates higher leakage currents, which

could be explained by different doping concentrations in the poly-Si gate.

The third research objective was to characterize the effect of illumination on the MOSFET. In our design, since the transistor has architectural features similar to a solar cell, photons are absorbed, electron-hole pairs are created, and their separation could occur. Therefore, a photocurrent was expected. The results exhibit increased leakage currents and reduced off-resistances. However, the on-performance is not altered by illumination. Further study into the mitigation of these effects would be required.

Finally, the fourth research question was how the components perform when they are monolithically connected. An influence of the MOSFET on the solar cell's characteristics is verified since the overall efficiency is directly related to the applied gate voltage. In the on-mode, the solar cell combined with the transistor maintains up to more than 95% of the conversion efficiency of the solar cell alone. However, a noticeable current remains in off-mode. This is due to the globally lower on- and off-resistances of the MOSFET that is monolithically connected to the solar cell combined with an isolated MOSFET, which could be due to interactions with the solar cell through a pathway in the bulk. This could be related to poor intrinsic MOSFET qualities or unexpected electronic interactions with the solar cell. This would result in noticeable off-mode power losses.

7.2. Recommendations

Despite the promising results exhibited in the thesis, integrating a MOSFET and a solar cell on the same wafer is not yet industrially applicable. Further research is necessary to improve the performance and demonstrate the interest of that technology in commercial applications. Therefore, this section provides recommendations based on ideas that came up during the project and that were not carried out due to lack of time.

First, the characterization of the fabricated MOSFETs should be pursued to derive important parameters. The breakdown voltage must be measured to find the component's voltage limits. In particular, the maximum drain voltage value directly indicates the maximum number of solar cells that can eventually be connected to one transistor. The dynamic behaviors must also be characterized to derive the transistor's switching speed and hence find its frequency limitation.

Second, strategies aiming to enhance MOSFET's on-performance have to be explored and studied. This is necessary to adapt the component to larger-area solar cells. Reducing the gate length and increasing the number of drain-source pairs are efficient strategies. However, the consequences of those changes should be anticipated. For example, reducing the gate length under a certain value could no longer be compatible with the current process methods and tools, such as the post-implantation thermal annealing process. Therefore, it would require new optimization of the impacted processes.

Third, the results have exhibited diminished p-type solar cell performance after post-metallization annealing. However, since that still improves the transistor's performance, optimization of the process (temperature and duration) must be carried out to make it compatible with both components.

Fourth, the measurement including the monolithically connected solar cell and transistor exhibited unexpected changes in the on- and off-resistance compared to the transistors built alone. Understanding the interactions between the components should be sought. This might involve an analysis based on simulations.

Fifth, alternative MOSFET designs could be introduced to make it more illumination-resilient. For example, a filtering layer could be introduced on top of the component to block the light. Alternatively, an inversely doped well can be introduced to act as a charge carriers barrier. This could also be exploited to reduce the MOSFET-PV bulk interactions.

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