A Review on Gate Oxide Failure Mechanisms of Silicon Carbide Semiconductor Devices

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DOI
10.1109/TED.2024.3482252

Publication date
2024

Document Version
Final published version

Published in
IEEE Transactions on Electron Devices

A Review on Gate Oxide Failure Mechanisms of Silicon Carbide Semiconductor Devices

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***Abstract*— In this article, we provide a comprehensive review of defect formation at the atomic level in interfaces and gate oxides, focusing on two primary defect types: interface traps and oxide traps. We summarize the current theoretical models and experimental observations related to these intrinsic defects, as they critically impact device performance and reliability. By integrating theoretical insights with experimental data, this review provides a thorough understanding of the atomic-scale interactions that govern defect formation.**

***Index Terms*— Acceleration model, failure mechanisms, silicon carbide (SiC) MOS devices, time-dependent dielectric breakdown (TDDB).**

I. Introduction

THE drive toward higher efficiency and performance in electronic devices has brought silicon carbide (SiC) to the forefront of semiconductor technology. SiC-based devices offer superior electrical and thermal properties compared to traditional silicon (Si) devices [1], making them highly attractive for applications in power electronics, automotive, and aerospace industries [2], [3], [4], [5], [6], [7], [8]. One of the critical aspects determining the reliability and lifetime of these devices is the integrity of the gate oxide. Therefore, understanding the breakdown and failure mechanisms of SiC gate oxides is crucial for the advancement and broader adoption of SiC technology.

Compared to Si, SiC gate oxides are subject to harsher operational environments due to the inherent properties of SiC, such as higher electric fields and increased operating temperatures. These conditions worsen the stress on the gate oxide, potentially accelerating degradation processes. In addition, the interface quality between SiC and the gate oxide (typically silicon dioxide, SiO_2) plays a pivotal role in device performance and reliability [9]. Unlike Si, which benefits from an exceptionally high-quality SiO_2 interface due to the near-perfect lattice match, the gate oxide in SiC devices suffers from a high density of defects, which can trap charges and further degrade the device performance.

Recent studies have shown that the dominant failure mechanisms in SiC gate oxides include field-driven related bond breakage and current-driven related charge trapping, both contributing to premature breakdown. Unfortunately, reliability investigations of breakdowns in various fabrication processes and applications have evolved separately for many years, leading to confusion and misunderstandings. The unique material properties of SiC necessitate a thorough reevaluation of existing models and the development of new predictive tools for gate oxide reliability.

This review aims to synthesize the current understanding of SiC gate oxide breakdown and failure mechanisms, contrasting it with the well-established knowledge of Si gate oxides. By examining the similarities and differences in failure behaviors, we seek to highlight the specific challenges associated with SiC gate oxides and clarify prospective research fields. Through this comprehensive overview, we intend to provide a road map for future studies to enhance the reliability of SiC-based electronic devices.

This article is organized as follows. Section II provides a comprehensive overview of dielectric breakdown models, detailing the E model, $1/E$ model, the combined $E + 1/E$ model and trap-assist-tunnel model, with a focus on their theoretical foundations, strengths, and limitations. In addition, this section discusses how device performance is influenced by oxidation conditions, oxide materials, and annealing processes. Section III delves into defects at the atomic level, examining their impact on semiconductor materials, particularly at the SiO_2/SiC interfaces and within gate oxides. This section discusses the formation and effects of carbon-related defects, oxide traps, and the transformation of oxygen vacancies.

II. Voltage, Temperature, and Process Dependency of Breakdown Time

The breakdown time (T_{BD}) of gate oxides in SiC devices is influenced by several factors, including operating voltage, temperature, and intrinsic fabrication process variables. Understanding these dependencies is essential for predicting device lifetime and improving fabrication techniques.

Received 8 August 2024; revised 25 September 2024; accepted 13 October 2024. Date of publication 25 October 2024; date of current version 2 December 2024. The review of this article was arranged by Editor T. Kimoto. *(Corresponding author: Jinglin Li.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2024.3482252.

Digital Object Identifier 10.1109/TED.2024.3482252

Long-term stress tests over years or decades are impractical, so higher-than-operational stress conditions are applied to induce breakdown within a manageable time frame. However, these accelerated conditions may introduce stress mechanisms different from those encountered during normal device operation, potentially leading to inaccuracies in lifetime projections. Therefore, while acceleration tests are invaluable for rapid reliability assessment, it is crucial to interpret their results with caution and to complement them with models that account for the discrepancies between accelerated and operational conditions.

A. Physical Breakdown Models

In this section, we discuss four breakdown time models: the E model, the $1/E$ model, the combined model, and the trap-assisted tunneling (TAT) model. The selection of the appropriate model, particularly the debate between the E and $1/E$ models, remains unresolved [10], [11].

1) E Model: The E model supposes the dielectric breakdown is a field-driven mechanism. To investigate the model, a fixed voltage is typically applied to the gate oxide and the time until breakdown (T_{BD}) is recorded. The breakdown event is usually characterized by a sudden increase in leakage current, indicating a catastrophic failure of the oxide layer. The constant voltage time-dependent dielectric breakdown (CV-TDDB) is commonly applied to evaluate the field-induced degradation. This degradation is based on the concept of oxygen vacancies and molecular precursors with strong dipolar coupling in intrinsic defects. These weak bond states can be broken by thermochemical processes induced by the local electric field in the gate oxide [10].

It is widely reported that T_{BD} under CV has an exponential dependency on the electric field in the gate oxide (E_{ox})

$$T_{\mathrm{BD}} = T_{\mathrm{BD},0} \cdot \exp\left(\frac{\Delta H_0}{kT} - \gamma E_{\mathrm{ox}}\right) \tag{1}$$

where ΔH_0 is the activation energy for bond breakage, k is Boltzmann's constant, T represents the temperature, and γ represents the acceleration factor, which represents the rate at which stress conditions (such as elevated temperature or increased electric field) accelerate the degradation mechanisms compared to normal operating conditions. It is typically used in reliability assessments to project the lifetime of a device under normal use based on accelerated test data. In most TDDB studies, the acceleration factor is electrical field-dependent or voltage-dependent, assuming that the gate voltage on a certain oxide with thickness t_{ox} is $V_{\mathrm{ox}} \approx E_{\mathrm{ox}} t_{\mathrm{ox}}$.

Fig. 1(a)–(c) shows the evolution of gate leakage current in a variety of CV-TDDB tests [12], [13], [14], with three distinct phases labeled. In Phase I, the gate leakage currents exhibit a slight decrease or remain nearly constant. In Phase II, particularly for higher electric fields $E_{\mathrm{ox}} \geq 9.5$ MV/cm, seeing 37.5 V in Fig. 1(a) and 43 V in Fig. 1(b), the gate leakage current increases with time and forms a peak. At this field, impact ionization-generated holes are trapped, leading to the increase of electric field within the oxide, which in turn shortens the tunneling distance [15], [16]. In Phase III, the leakage current shows exponential decay due to trapped electrons being captured by the newly generated defects throughout the tests [17]. The trapped holes in Phase II are recombined with electrons injected via Fowler–Nordheim tunneling. Both mechanisms release energy within the oxide, generating additional defects, which results in a net accumulation of negative charge in the oxide, leading to a gradual decline in current density [17].

Accurate projection of lifetime necessitates a better understanding of accelerate factor γ. $T_{\mathrm{BD},63\%}$, where the time that 63.2% of the sample population fails, is extracted from the Weibull plots in Fig. 1(d) and (f) and [15]. Fig. 2 illustrates $T_{\mathrm{BD},63\%}$ as a function of $\mathbf{E}_{\mathrm{ox}}$. The data reveal a significant overestimation of lifetime predictions when relying solely on high electric field data, and the large disparity in γ suggests different breakdown mechanisms.

In lower electrical field stress, the Si–O bonds are deformed by local electrical field $\mathbf{E}_{\mathrm{loc}}$, as the Si–O bond can be regarded as a dipole [10], [15]. This deformation indicates the stretching of SiO_2 bonds by the local electrical field, described by the dipole moment $\mathbf{P}$ under the local electrical field $\mathbf{E}_{\mathrm{loc}}$

$$\mathbf{E}_{\mathrm{loc}} = \mathbf{E}_{\mathrm{ox}} + L(\mathbf{P}/\epsilon) \tag{2}$$

where L represents the Lorentz factor and ϵ is the permittivity of free space. For instance, data from [15] show that the acceleration factor decreases to 5.414 cm/MV as the electrical field reduces from 8.21 to 7.55 MV/cm. The effective dipole moment extracted from the acceleration factor under lower electrical field stress is given by the following equation:

$$P_{\mathrm{eff}} = kT\gamma = 19.75e \text{ Å} \tag{3}$$

where e is the elementary charge and Å $= 10^{-10}$ (m). Based on the Mie–Grüneisen analysis of molecular bonding states in the silica-based dielectric, Si–O remains covalent with a bonding coefficient $\eta(9, 2) = 1.07$ [15], [18]. The calculated effective dipole moment agrees with the value extracted in (3), yielding $P_{\mathrm{eff}} = 19.96e$ Å. P_{eff} can be expressed by the following equation:

$$P_{\mathrm{eff}} = \frac{(eZ^*)r_0}{\eta(9, 2)} \cdot [1 + L_{\mathrm{eff}} \cdot (K_{\mathrm{ox}} - 1)] \tag{4}$$

where $Z^* = 2.4$ represents the number of electron charges of Si ions [18], [19], $r_0 = 1.7$ Å stands for the equilibrium Si–O bond distance [15], [18], [19], $L_{\mathrm{eff}} = 1.46$ is the effective Lorentz factor [15], and $K_{\mathrm{ox}} = 3.9$ is dielectric constant for silicon dioxide. It suggests that Si–O bonds remain covalent bonding when $E_{\mathrm{ox}} \leq 8$ MV/cm [18]. The covalent nature in the silicon dioxide system may also arise from Si–Si bonds (oxygen vacancies) or hole-captured Si–O bonds [15], [18].

The transition in γ at higher electrical field stresses suggests a different breakdown mechanism. According to [18], 70% of the Si–O bond energy comes from ionic bonds, and the bonding coefficient drops to $\eta(9, 1) = 0.6$ [18]. The extracted effective dipole moment increases dramatically to $37.65e$ Å, which is consistent with the calculated value of $35.59e$ Å. It is noteworthy that the effective dipole moment P_{eff} of SiC gate oxides is larger than that of Si devices (from $7e$ to $13e$ Å), as reported previously [18]. A larger P_{eff} indicates greater bond stretching and local electric field effects, even under

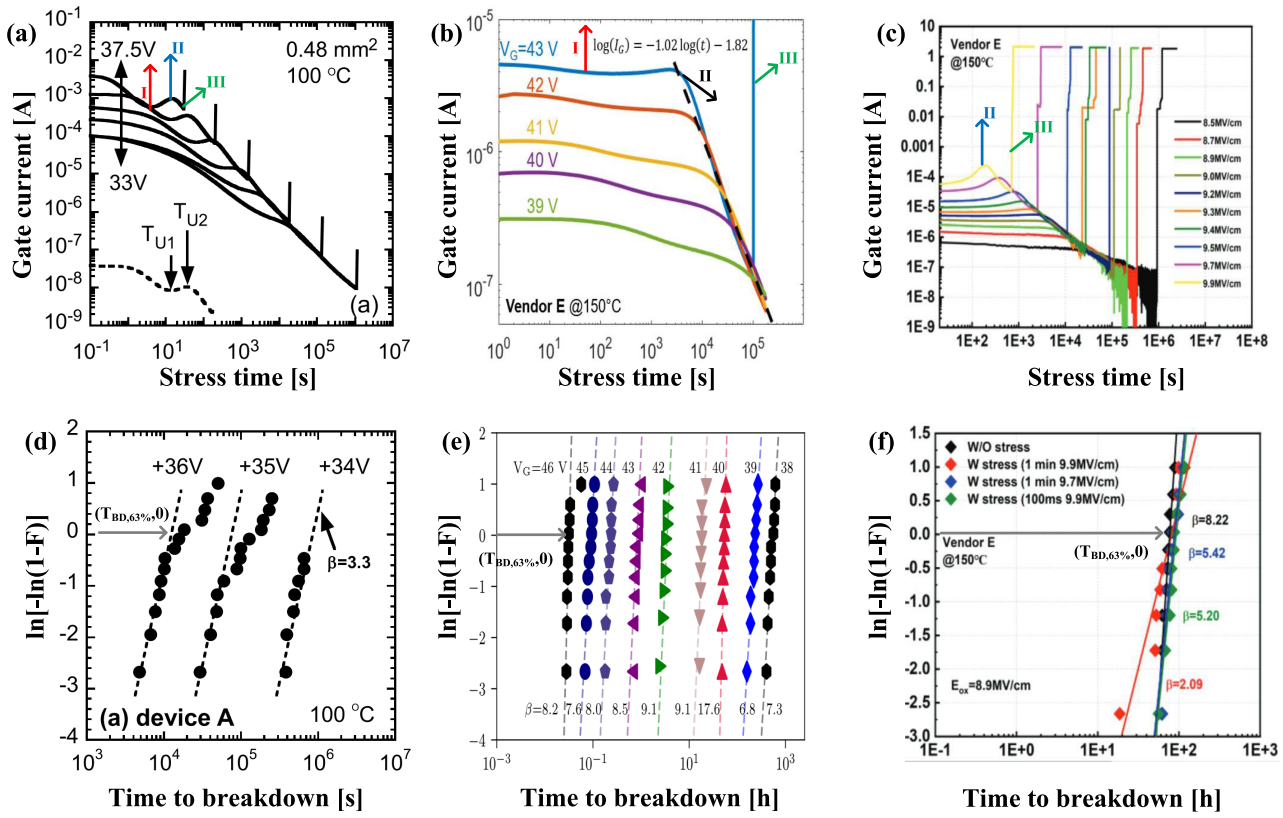

Fig. 1. Time-dependent dielectric breakdown tests and Weibull plots using CV stress [12], [13], [14]. (a)–(c) Gate oxide thicknesses are 38, 46, and 45 nm, respectively. The electrical field stress ranges from 8.68 to 9.9 MV/cm for (a), from 8.48 to 9.35 MV/cm for (b), and from 8.5 to 9.9 MV/cm (c). (d)–(f) Weibull plots.

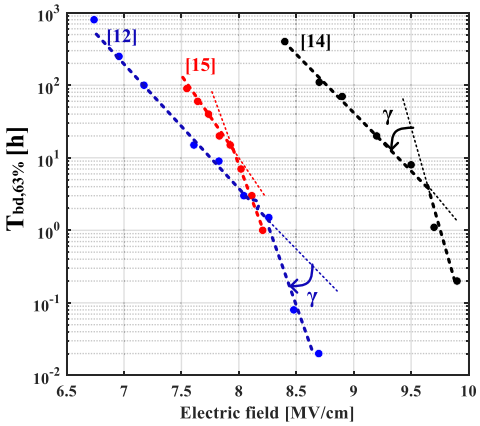

Fig. 2. $T_{BD,63\%}$ with respect to E_{ox}, indicating overestimation of the lifetime due to the electrical field dependency of γ. Reproduced from [12] and [14], [15]. The acceleration factors decrease from 9.99 to 4.126 cm/MV [12], from 9.22 to 3.556 cm/MV [14], and from 10.32 to 5.414 cm/MV [15] when reducing the electrical field.

the same external electrical field. This suggests enhanced Fowler–Nordheim (FN) tunneling and impact ionization. Due to the small barrier height (2.8 eV) between SiC and gate oxide [20], the FN tunneling is triggered around 8 MV/cm in SiC gate oxides, whereas impact ionization is not predicted in thin gate oxides of Si devices until reaching 14 MV/cm [21].

2) 1/E Model: Even though the average electric field remains constant during CV stress, the local field near the anode and the SiC/SiO_2 interface can still fluctuate [22]. Furthermore, the E model fails to account for the polarity effects observed in TDDB tests, where discrepancies arise when the anode and cathode are reversed [23]. As a result, the $1/E$ model and the charge-to-breakdown approach have regained interest.

The $1/E$ model is based on an injected-charge-driven mechanism. Degradation occurs due to the flow of conduction current and the injection of charges into the dielectric. Before Si–O bonds break, injected electrons and activated holes are first captured by defect precursors. Subsequently, the local electric field disrupts these deteriorated bonds [24], [25]. The conduction current is typically modeled as FN tunneling, leading to a lifetime model T_{BD} under constant current (CC) that follows an exponential law of reciprocal electric field dependency:

$$T_{BD} = T_{BD,0} \cdot \exp\left(\frac{B+H}{E_{ox}}\right) \tag{5}$$

where B and H are coefficients related to the FN tunneling current and impact ionization, respectively [11]. Impact ionization occurs under a high electrical field, where electrons gain sufficient energy to create new electron–hole pairs in the polysilicon layer via interband transition [26], [27]. The newly generated holes tunnel back to oxide vacancies, causing lattice damage [28]. The anode hole injection (AHI) mechanism is illustrated in Fig. 3 [11], [29]. However, in the case of metal gates, such as aluminum (with zero bandgap), the intraband transition dominates, which indicates the threshold energy of

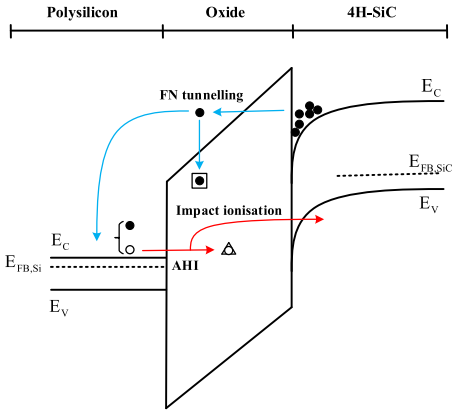

Fig. 3. Accumulated electron tunnel through the triangular-shaped barrier by FN tunneling under a high electrical field. Some high-energy electrons reaching polysilicon activate electron–hole pairs, and again, the hot holes can be tunneled back and trapped in the gate oxide. Reproduced from [11] and [29].

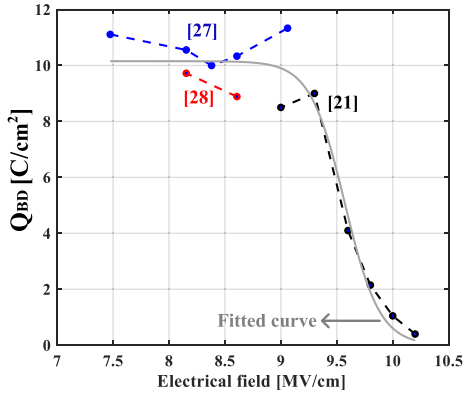

Fig. 4. Q_{BD} with respect to E_{ox}, indicating a critical breakdown charge existing under lower electrical field, with 10 C/cm^2 [22], 11.1 C/cm^2 [31], and 9.4 C/cm^2 [32]. Meanwhile, the transition in the high electrical field suggests holes capturing in the gate oxide. Reproduced from [22], [31], and [32].

anode electron direct excitation in metal electrodes is almost zero. The above threshold energies for metal anode electron direct excitation are much smaller than the threshold energies for oxide hole current generated in polysilicon, leading to a large gate leakage current [27], [30].

The gate oxide fails when the cumulative injected charges in the oxide reach a critical value (Q_{BD}), which serves as a breakdown criterion. Fig. 4 illustrates the Q_{BD} data extracted from Weibull plots [22] as a function of E_{ox} [31], [32]. The charge-to-breakdown $Q_{BD} = \int_0^{T_{BD}} I_g dt$ shows a weak dependence on stress when $E_{ox} \leq 9$ MV/cm, with Q_{BD} values approximately 10, 11.1, and 9.4 C/cm^2 in [22], [31], and [32], respectively. However, relying solely on lower electric field data can lead to significant underestimation [22]. A clear transition in Fig. 4 shows a dramatic drop in Q_{BD} under high electrical field stress. In [31], commercial 1200-V planar MOSFETs were applied to CC TDDB, with $\Delta V_{g,BD}$ monitored. Here, $\Delta V_{g,BD}$ represents the voltage difference from the initial V_g to the breakdown V_g during CC-TDDB. The agreement between the electron trapping model and experiment data at 3.43 μA (9.06 MV/cm) indicates that Q_{BD} is primarily influenced by electron trapping, whereas discrepancies suggest that holes trapping induced by AHI become significant when the applied field exceeds 9.06 MV/cm. At that electrical field, the trapping of hot electrons and the generation of hot holes induced by AHI become dominant. These trapped holes reduce the tunnel distance by altering the electrical field and cause further oxide damage, which is evident in the I_g–t curves where a peak in leakage current is observed in phase II in Fig. 1(a)–(c). In addition, the phenomenon of charge capture results in an interesting effect; Q_{BD} slightly decreases with increasing injected current density in CC TDDB tests [29]. The modified Q_{BD} model, incorporating electron trapping, demonstrates high-density electron capture, which leads to nonuniform current flows near the localized defects [29].

The $1/E$ model has its limitations. It must be considered that higher electrical fields may induce a different breakdown mechanism to what would be the case in operation at smaller fields. Specifically, the rate of hole generation is negligibly small at low electric fields, particularly under typical operating conditions, and defect generation induced by hot holes does not significantly contribute to oxide breakdown. Contradictory findings arise from studies investigating the impact of hot holes on gate oxide breakdown. Devices subjected to CV stress with varying amounts of pre-injected substrate hot holes show that oxide breakdown is independent of the quantity of these pre-injected hot holes [33].

3) $E + 1/E$ Model: Early research suggested that the E and $1/E$ models are complementary; the electrical field can thermally stretch the polar Si–O bonds, while the current injected holes can be captured by oxide traps, further contributing to degradation [15]. For instance, the acceleration factor γ is field dependent (see the transition in Fig. 2), indicating that the $1/E$ model and E model are not mutually exclusive but rather applicable within different ranges of electric field stress. Consequently, researchers are exploring ways to integrate both models to provide a more comprehensive understanding of TDDB across varying electric field conditions.

Fig. 5 illustrates the potential processes for Si–O breakage. The Si–O bonds can be directly broken through field-driven thermochemical processes with a reaction rate k_1 or through current-based hole capture [34]. The reaction rate k_1 is given by the following equation:

$$k_1 = \nu_0 \cdot \exp\left(-\frac{\Delta H_0 - \gamma E_{ox}}{kT}\right) \tag{6}$$

where ν_0 represents the characteristic collision frequency with the lattice [24], [25]. Surprisingly, although the hot holes may possess sufficient energy, they cannot break the bonds or cause dislocation of much heavier Si and O atoms [24], [25]. Instead, the captured holes in oxide traps assist degradation by lowering the hole-catalyzed activation energy by at least $\Delta H_0/2$. Consequently, the effective reaction rate k_{eff} is the sum of the reaction rate for hole-captured Si–O bonds k_{2b} and k_1 [25].

As previously emphasized, the acceleration factor γ exhibits a dependence on the electric field. To address this, a model that

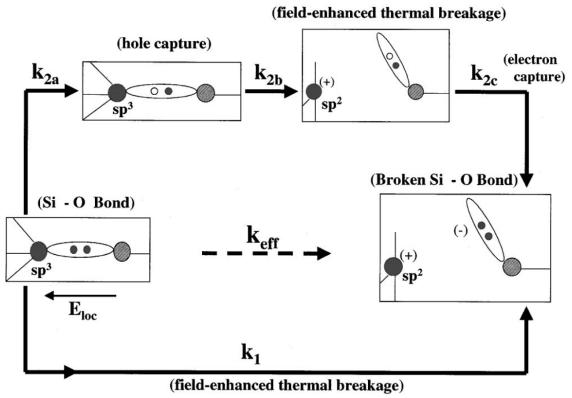

Fig. 5. Two parallel breakage paths for Si–O bonds: The Si–O bond can directly break by field-driven thermochemical process or assisted by hole capture by hole injection [24].

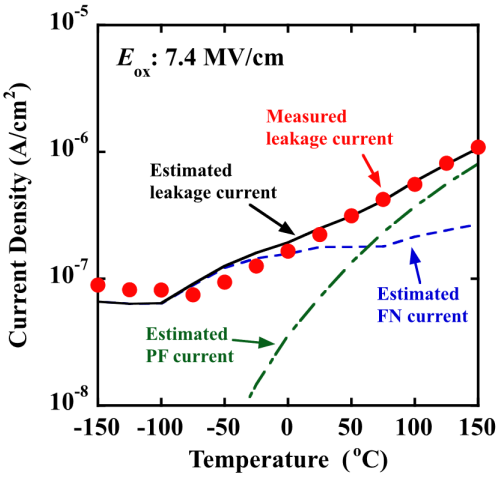

Fig. 6. Temperature dependency of measured gate leakage current and calculated PF/FN current [39].

accounts for the combined effects overextended ranges was proposed in [15]. The author used TDDB data at the critical gate voltage $V_{\mathrm{GS,crit}}$ (the transition point in Fig. 2, red line) to derive modulated parameters beyond $V_{\mathrm{GS,crit}}$, The relationship is given by the following equation:

$$\Delta H_0' - \Delta H_0 = kT\left(\gamma' - \gamma\right)V_{\mathrm{GS,crit}} \tag{7}$$

where γ' represents the modulated acceleration factor and $\Delta H_0'$ is the modulated bond breakage energy. In addition, a lifetime prediction model that integrates the joint effect across extended ranges was proposed as follows [15]:

$$T_{\mathrm{BD,total}} = \frac{T_{\mathrm{BD},E} \times T_{\mathrm{BD},1/E}}{T_{\mathrm{BD},E} + T_{\mathrm{BD},1/E}}. \tag{8}$$

4) Trap-Assisted Tunnel Model: Under normal operational voltage ranges and room temperature, the probability of electron injection that can overcome the tunnel barrier is negligibly low [35]. However, in dielectrics with a high density of defects, especially shallow traps, TAT becomes significant. This is due to charge transport facilitated by lattice relaxation and electron–phonon coupling [36]. TAT can arise from the elongated Si–O–Si bond upon electron capture [37], a phenomenon observed in ammonia (NH_3) annealed SiC trench MOSFETs [38]. Compared to devices annealed with nitric oxide (NO), those treated with ammonia exhibit additional trap-assisted leakage paths [38]. The conduction current described by the Poole–Frenkel (PF) equation is given by the following equation [39]:

$$J_{\mathrm{PF}} \propto \exp\left(-\frac{E_t - q\sqrt{qE_{\mathrm{ox}}/\pi\epsilon}}{kT}\right) \tag{9}$$

where E_t represents the thermal activation energy, typically a few tenths of electronvolts. Fig. 6 shows the temperature dependence of gate leakage current components, including the PF current and FN tunneling current, measured from −150 °C to 150 °C [39]. Below −75 °C, the pure FN current dominates as the PF current decreases significantly, and the overall leakage current becomes independent of temperature. However, at higher temperatures, the PF current increases and contributes to the total leakage current, indicating that relying on room temperature data alone can lead to an underestimation of the FN tunneling barrier height [39]. The purpose of applying this model is not merely to "curve-fit" the TDDB data but to provide a physical explanation for extrinsic failures and leakage currents at intermediate fields ($E_{\mathrm{ox}} \approx 5$ MV/cm) [37]. For instance, the lucky defect model, based on TAT, successfully explains the anomalous early TDDB failures observed in SiC power MOSFETs [40].

5) Summary: Table I summarizes the key characteristics of various TDDB models, including the underlying field and temperature dependencies, and conduction mechanisms to drive the breakdown processes. Each model has its strengths and weaknesses, with the combined E and $1/E$ model offering a more comprehensive description of experimental observations, yet still requiring refinement for precise predictive capabilities.

B. Temperature Dependency

Temperature significantly impacts the breakdown process in TDDB tests. Measurements conducted under constant field stress at temperatures ranging from 150 °C to 300 °C reveal that both $\ln(T_{\mathrm{BD}})$ and the acceleration factor γ are linearly proportional to the reciprocal of temperature [41]. It is well documented that T_{BD} decreases with increasing temperature [41], [42]. The temperature dependence of each component of the gate leakage current has been extensively reviewed.

Temperature tests on I_{gss} versus V_{gs} characteristics illustrate the impact of temperature on leakage current [43], [44]. Measurements conducted up to $E_{\mathrm{ox}} = 8$ MV/cm across temperatures ranging from 25 °C to 300 °C reveal that the FN tunneling current exhibits minimal temperature dependence [44], [45]. However, the tunnel barrier Φ_B decreases from 2.7 to 2.44 eV for nMOS and from 1.4 to 0.86 eV for pMOS [44], which is also supported in [22]. This reduction in the tunnel barrier at higher temperatures facilitates an increase in electron-induced FN tunneling current and enhances the generation of hot electron–hole pairs in the polygate. At lower and intermediate electric field ranges, the electron hopping conduction (occurring under $E_{\mathrm{ox}} = 2$ MV/cm) and electron direct

TABLE I
SUMMARY OF BREAKDOWN MODELS

TDDB models	E model	1/E model	E+1/E model	Trap assist tunnel model
Mechanisms	Thermochemical	Hole induced defect generation	Combined	Percolation path through traps
Conduction	Bond stretch	FN tunnel	Combined	PF tunnel
Driven	Field	Field and energy	Field and energy	Field
Field dependent	Yes	Yes	Yes	Yes
Temperature dependent	Strong	Weak	Yes	Yes
Explain polarity	No	Yes	Yes	?

tunneling (occurring between $E_{ox} = 2$ MV/cm and $E_{ox} = 5$ MV/cm) are dramatically enhanced at 300 °C [44], [46].

The strong temperature dependency in gate leakage current complicates the accurate prediction of useful remaining lifetime. In the E model, the acceleration factor γ is linearly related to the reciprocal of temperature, and the activation energy of oxide traps follows the Arrhenius temperature dependency [41], [47]. The Arrhenius behavior is typically observed within a limited electrical field ($E_{ox} = 7$ MV/cm) and temperature (usually below 200 °C) [46]. Conversely, in the $1/E$ model, the charge to breakdown (Q_{BD}) also exhibits a negative temperature dependence. For instance, as the temperature increases from 25 °C to 300 °C, Q_{BD} in nMOS decreases from 81.61 to 0.59 C/cm^2, while in pMOS devices, it drops from 3.04 to 0.23 C/cm^2 [44].

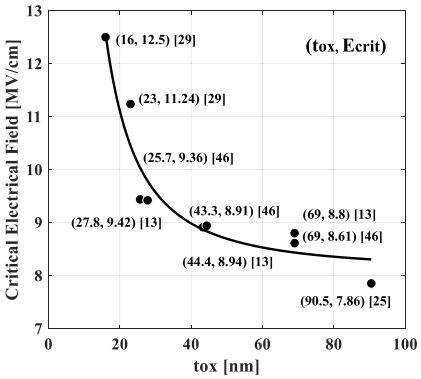

Fig. 7. Critical electrical field as a function of gate oxide thickness. At least $E_{ox} \geq 9$ MV/cm is required for the electron to gain sufficient energy to trigger FN tunneling, in which impact ionization happens.

C. Process Dependency

Accurately predicting the lifetime of gate oxides requires a deep understanding of the fabrication process and its dependencies. In this section, the recent developments that have contributed to advancements in channel mobility and interface trap density are reviewed, making them relevant to industry and academia.

1) Oxide Geometric Parameters: Oxide thickness is a crucial factor in gate oxide reliability, as the time to breakdown (T_{BD}) is influenced by the generation of bond breakages and defects within the oxide, which eventually form percolation paths that lead to the leakage current conduction [48]. The formation of these percolation paths is dependent on oxide thickness. Fig. 8 shows the relationship between normalized breakdown time and electrical field for oxide thicknesses ranging from 7.6 to 44 nm [49]. The data indicate that oxide thickness between 7.6 and 13.6 nm exhibit similar slopes, while $t_{ox} \geq 22.5$ nm show proportionally increased slopes. Fig. 7 presents the critical breakdown field (E_{crit}), the electric field required for impact ionization, across various oxide thicknesses [13], [26], [29], [50]. Thin-film gate oxide demonstrate $E_{crit} \geq 9$ MV/cm, which varies significantly with oxide thickness [13], [29], [49]. In thicker gate oxide, electrons have a greater distance to accumulate kinetic energy, thus facilitating impact ionization [26]. While early studies focused on ultrathin SiO_2 films in silicon devices [51], there are fewer models addressing these phenomena in SiC devices.

In Fig. 8, a noticeable nonlinearity appears in the Weibull plots when the stress exceeds 35 and 36 V [49]. This nonlinearity is attributed to the nonuniformity of the gate oxide [52], which arises from thermal oxidation processes and is further exacerbated by nonuniform breakdowns [52], [53]. Such nonuniformity distorts the SiO_2 lattice, contributing to increased leakage currents [52], [53]. In addition, the formation of percolation paths is a statistical phenomenon, with breakdown time being influenced by the device area. Smaller device areas tend to have fewer percolation paths, impacting the breakdown characteristics. For instance, it was reported that a device with the smallest size of 0.2 mm^2 exhibited the highest critical breakdown field ($E_{ox} \geq 9$ MV/cm) [54].

2) Oxide Materials: The use of high-k insulation layers has been proposed to enhance the reliability of the gate oxide. According to Gauss's law, the electrical field within the SiO_2 layer is intensified by a factor of $\epsilon_{high\text{-}k}/\epsilon_{SiO_2}$ compared to that within the high-k material itself. Consequently, high-k insulators can reduce the electrical field and oxide thickness. Hino et al. [55] demonstrated the metal-organic chemical vapor deposition (MOCVD) to form Al_2O_3 on a SiC lattice resulted in peak mobility of 64 cm$^2 \cdot$ V^{-1}s^{-1} at 190 °C and 14 cm$^2 \cdot$ V^{-1}s^{-1} at 230 °C in Al_2O_3/SiC

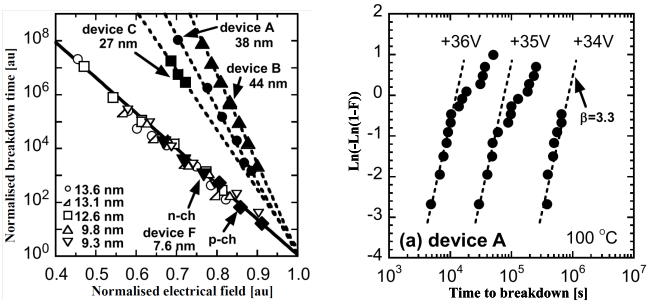

Fig. 8. Effect of the gate oxide thickness under constant electrical field test, where the normalized breakdown time with respect to the electrical field is plotted. Thin-film gate oxides have identical slope means indicating strong impact ionization [49].

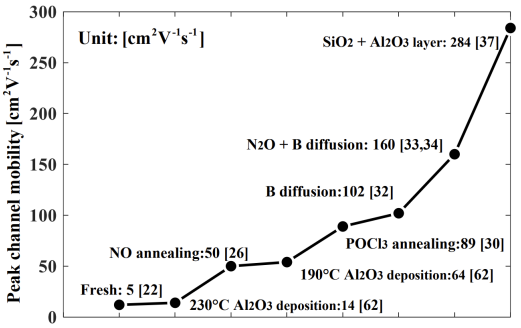

Fig. 9. Channel mobility improvement of SiC MOSFETs, from less than 10 to 284 $cm^2 \cdot V^{-1}s^{-1}$ [55], [60], [70], [71], [72], [73].

MOSFETs. An improved method involves applying atomic layer deposition (ALD) to deposit a thin SiO_2 layer between SiC and Al_2O_3. The benefit is that no abrupt interface between SiO_2 and Al_2O_3 was observed [56]. Using this structure, the channel mobility was boosted to 284 $cm^2 \cdot V^{-1}s^{-1}$ [55].

Materials with high dielectric constants, such as aluminum oxide (Al_2O_3), which has a dielectric constant of approximately 8–10, are particularly appealing for gate oxides. Generally, materials with high dielectric constants tend to have smaller bandgaps and small conduction band offset (ΔE_c) between gate oxide material and SiC [57]. It leads to a large leakage current, suggesting a tradeoff between high-k and ΔE_c: Al_2O_3/SiC ($\Delta E_c = 1.76$ eV) compared with SiO_2/SiC ($\Delta E_c = 1.9$ eV). The aluminum oxynitride AlON/SiO_2 stacked gate dielectric in SiC planar and trench MOSFETs has demonstrated [58]. The AlON has a bandgap of 6.23 eV and $\Delta E_c = 2.42$ eV; as a result, it achieved a reduced flat-band voltage shifts and gate leakage current compared with Al_2O_3 gate [58].

3) Oxidation Conditions: In the conventional process, the gate oxide is processed by either wet or dry oxidation and then followed by nitridation [59], [60], [61], [62], [63]. The peak channel mobility is even less than 10 $cm^2 \cdot V^{-1}s^{-1}$ without NO/N_2O annealing due to high interface trap density (more than 3×10^{12} $cm^{-2} \cdot eV^{-1}$) at $E_c - 0.2$ eV [59], [60]. Although the nitridation process is commonly employed, the peak channel mobility is still around 30 $cm^2 \cdot V^{-1}s^{-1}$ [59], [60], [61], [62], [63]. It was proved that H_2 etching the SiC surface before oxidation can improve the smoothness effectively [64], [65]. Mikami et al. [66] and Tachiki et al. [67] proposed oxidation-minimizing process (H_2-CVD-NO): H_2 treatment is performed under 1350 °C in 8 min before plasma-enhanced chemical vapor deposition (PECVD) and NO annealing. Compared with the devices with dry oxidation without H_2 etching, the interface trap density reduces from 2×10^{11} to 7×10^{10} $cm^{-2} \cdot eV^{-1}$ at $E_c - 0.2$ eV, and the peak channel mobility increases from 25 to more than 40 $cm^2 \cdot V^{-1}s^{-1}$ [67].

4) Annealing Conditions: Compared to Si, most defects in SiC gate oxides arise from oxygen deficiency during thermal oxidation. Introducing additional oxygen atoms into defect precursors, such as weak Si–Si bonds, has proven to be an effective method for mitigating gate oxide defects caused by this deficiency. NO annealing has become a widely adopted technique in the production of SiC devices, particularly due to its impact on improving MOS interface properties. This process leverages annealed nitrogen (N) atoms to neutralize activated oxide traps. Annealing in a NO environment is particularly effective, significantly reducing interface traps by an order of magnitude to less than 3×10^{11} $cm^{-2} \cdot eV^{-1}$ and increasing channel mobility to around 30 $cm^2V^{-1}s^{-1}$ [59], [60]. In addition, the annealing process of N_2 and N_2O also attracts attention. A 3-h N_2O annealing under 1200 °C reduces the interface trap density to 1×10^{12} $cm^{-2} \cdot eV^{-1}$ [61], [62]. Ultrahigh-temperature annealing in N_2 ambient also shows potential in channel mobility optimization [63], [68]. The 2–8-h O_2 pre-annealing was performed upon CVD deposited oxide layer and then followed by N_2 annealing in 1300 °C [68]. They achieved a peak channel mobility of more than 50 $cm^2 \cdot V^{-1}s^{-1}$ with interface trap density less than 5×10^{11} $cm^{-2} \cdot eV^{-1}$ [68].

Various annealing environments have been explored to enhance channel mobility and improve the interface quality of SiC MOSFETs. Oxygen plasma re-oxidation annealing, in particular, has been reported to effectively eliminate carbon- and Si-related defects. The devices with oxygen plasma treatments under 500 °C, 800-W plasma power, and 120-sccm oxygen flow rate have achieved a high breakdown field of 12.40 MV/cm, a moderate interface trap density of 7.2×10^{11} $cm^{-2} \cdot eV^{-1}$ at $E_c - 0.2$ eV, and improved voltage stability in C–V measurements [69]. The Si-rich region, often regarded as an indicator of gate oxide quality, was reduced by 0.1 nm after a 10-min oxygen plasma annealing process, further indicating the effectiveness of this treatment in enhancing the quality of SiC gate oxides [69].

The atomic structure of the SiO_2/SiC interface can be optimized by annealing in a nonnitride ambient. Annealing with CO_2 environment improves both the breakdown field and the flat-band voltage shift by recovery of oxide vacancies [74]. During thermal oxidation, CO_2 and carbon monoxide (CO) molecules are released and can become trapped in the gate oxide. If the partial pressure of CO_2 exceeds that of CO, the CO_2 molecules can further oxidize the oxygen vacancies [74]. For example, devices that underwent post-nitridation annealing in a CO_2 ambient demonstrated superior threshold voltage stability [75]. In addition, annealing in a phosphorus oxychloride $POCl_3$ environment has been shown to significantly boost

channel mobility. Okamoto et al. [71] achieved a mobility of 89 $cm^2V^{-1}s^{-1}$ by using this method, reducing the density of interface states near the conduction band edge to less than 10^{11} $cm^{-2} \cdot eV^{-1}$, which is an improvement over the 3–4×10^{11} $cm^{-2} \cdot eV^{-1}$ typically observed after NO annealing alone. However, this approach introduced challenges, such as threshold voltage instability and increased gate leakage current due to the formation of phosphosilicate glass, which can trap negative charges [62]. Okamoto et al. [72] further advanced this work by using boron passivation to relax interface stress and reduce defect density to approximately 10^{10} $cm^{-2} \cdot eV^{-1}$, achieving a peak mobility of 102 $cm^2 \cdot V^{-1}s^{-1}$. Remarkably, when boron diffusion was combined with rapid thermal oxidation in a N_2O environment, peak channel mobility was further enhanced to 160 $cm^2 \cdot V^{-1}s^{-1}$ [73]. However, at high temperatures, boron can activate mobile ions, leading to unexpected threshold voltage shifts [76]. In addition, boron-related processes can contribute to bias temperature instability (BTI), as boron directly captures charges from the channel and indirectly facilitates charge trapping [77].

Fig. 9 demonstrates how mobility improves with different processing techniques. However, it is important to note that higher mobility can sometimes come at the expense of long-term reliability. However, the annealing conditions must be carefully managed, as improper conditions can introduce additional defects. For example, overannealing might introduce more defects compared to annealing in an argon environment [78]. The annealing time is also a crucial factor in determining the reliability and performance of the device. In a comparison of I_{gs} versus V_{gs} characteristics and I_g–t during CV TDDB tests [79], devices that underwent heavy NO annealing (1250 °C for 60 min) exhibited shorter time-to-breakdown T_{BD} and higher gate current than those that were lightly annealed (1250 °C for 10 min). This reduction in T_{BD} is attributed to hole trapping during the annealing process, which weakens the Si–N bonds and leads to the formation of a Si–C–N–O interlayer around the Si atoms [78], [79], [80].

5) Fabrication Process Summary: Table II summarizes the recent developments, including annealing conditions, oxidation, interface trap density and achieved peak channel mobility that have contributed to academia and industry.

III. Defects and Failure Mechanisms

Defect formation at the atomic level can be better understood through the lens of nanoscale physics and chemistry. As depicted in Fig. 10, the band diagram highlights the failure locations and corresponding mechanisms associated with the SiO_2/SiC interface and gate oxide. These mechanisms include the formation of interface traps, oxide traps, mobile charges, and fixed charges. This article provides an extensive review of two primary types of physical defects: 1) interface traps and 2) oxide traps, offering both theoretical models and experimental observations to explain the nature and impact of these intrinsic defects.

A. Interface Traps

The interface traps on 4H-SiC, illustrated as Fig. 10(b), are primarily associated with carbon-related defects resulting from

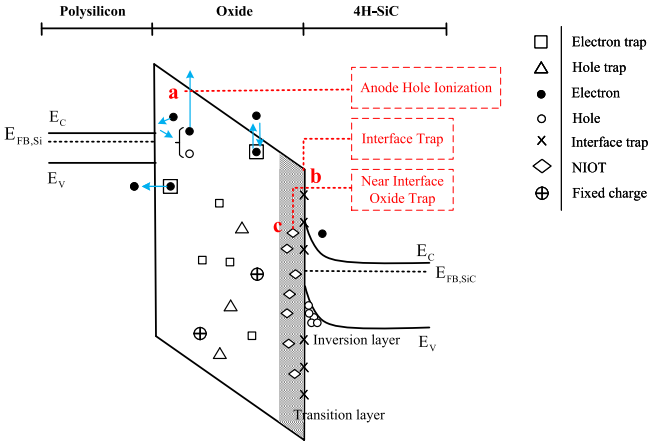

Fig. 10. Charge transportation and defect distribution in SiO_2/SiC interface and gate oxide, with all defects labeled in the band diagram. E_c, E_v, and E_{FB} represent the edge of the conduction band, valance band, and the Fermi level of polysilicon and SiC, respectively.

deficient oxidation. These defects significantly reduce channel mobility due to interactions between interface traps and hot electrons [84], [85]. Specifically, the mobility of the dry oxide channel is found to be less than 10 $cm^2 \cdot V^{-1}s^{-1}$ [70]. This reduction in mobility is attributed to the capture of electrons by nanochemical defects at the SiO_2/SiC interface, which in turn enhances Coulomb scattering within the channel. Two primary types of defects have been identified at the SiO_2/SiC interface: 1) active carbon clusters or graphitic regions and 2) the transition layer.

During the thermal oxidation of SiC, oxygen atoms substitute carbon atoms within the SiC lattice, leading to the release of CO molecules. However, some high-energy carbon atoms become trapped at the SiO_2/SiC interface, which further deteriorates the integrity of the SiO_2 network. Early experimental findings attributed the high defect density in SiC devices to the presence of "graphite-like" structures and oxygen-deficient carbon clusters [84], [86].

The energy positions of these carbon clusters have been the subject of extensive research [84]. Specifically, the clusters with Sp_2 bonds have energy levels that range from the valence band edge up to the midband, while the graphite-like clusters are spread throughout the bandgap [84]. The capture of electrons by these trap states is contingent on whether the trap states are above the Fermi level, which in turn influences the probability of their occupancy [87]. The interface state energy level, denoted as E_n, has been estimated to be approximately 3.5 eV below the conduction band of SiO_2 [87]. Under a certain electrical field, electrons from the SiC bulk can flow into these interface traps when the Fermi level in SiC $E_{FB,SiC}$ drops below E_n. This condition can be achieved by varying the magnitude of the applied stress or by altering the lattice temperature.

Transition layers between the SiC lattice and the SiO_2 layer can form when there is an excess of carbon atoms, particularly under conditions of oxygen deficiency. In such scenarios, a carbon atom bonded to three carbon neighbors and one oxygen neighbor is often unstable due to

TABLE II
SUMMARY OF FABRICATION PROCESS TECHNOLOGY OF SiC MOS DEVICES

Oxidation	Annealing	D_{it} at E_c-E ($cm^{-2}eV^{-1}$)	Channel mobility ($cm^2V^{-1}s^{-1}$)	Ref
Wet oxidation	NO @ 1175 °C + 2h	—	25-47	[59]
	Without NO annealing	—	5-14	[59]
Dry oxidation	Without annealing	3×10^{12} @ 0.2eV	less than 10	[60]
	NO @ 1175 °C + 7.5min	1×10^{12} @ 0.2eV	less than 30	[60]
	NO @ 1175 °C + 30min	8×10^{11} @ 0.2eV	around 35	[60]
	NO @ 1175 °C + 4h	3×10^{11} @ 0.2eV	around 45	[60]
	N_2O @ 1200 °C + 3h	1×10^{12} @ 0.2eV	20-25	[61, 62]
	N_2 @ 1300 °C + 30min	3×10^{12} @ 0.2eV	—	[63]
	N_2 @ 1350 °C + 30min	3×10^{12} @ 0.2eV	—	[63]
	N_2 @ 1400 °C + 30min	1×10^{12} @ 0.2eV	—	[63]
	Ar @ 1500 °C + 5min	1.5×10^{12} @ 0.2eV	less than 10	[81]
	$POCl_3$ @ 1000 °C + 30min	1×10^{11} @ 0.2eV	89	[62, 71]
	BN diffusion @ 1150 °C + 10min	1×10^{11} @ 0.2eV	102	[72]
	N_2 @ 1400 °C + 30min	1×10^{12} @ 0.2eV	—	[63]
RTO in N_2O	BN @ 1150 °C	1×10^{11}	160	[73]
PECVD	NO @ 1250 °C + 1h	1.5×10^{11}	—	[82]
	N_2 @ 1250 °C + 1h	3×10^{12}	—	[82]
	N_2O @ 1300 °C	2×10^{11}	—	[83]
	Ar @ 1300 °C	2×10^{12}	—	[83]
MOCVD of Al_2O_3	— @ 1700 °C	—	284	[55]

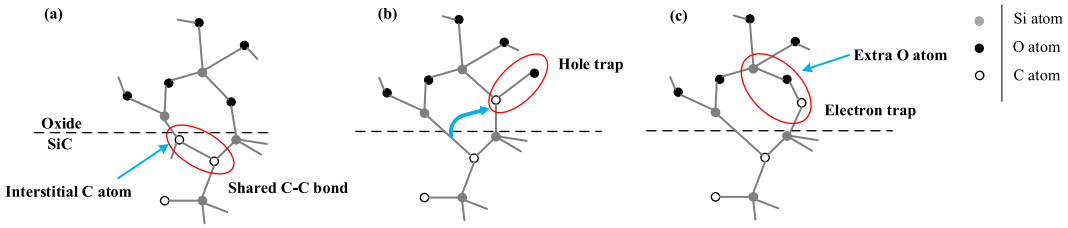

Fig. 11. Atomic view of the carbon clusters near the SiO_2/SiC interface. (a) Long C–C bond with higher energy is metastable. (b) Carbon atom activated to the oxide side releases energy to reach the lowest energy and form a hole trap. An extra oxygen atom inserted in (c) makes the C atom unpaired and forms an electron trap. Reproduced from [86].

the presence of long carbon–carbon (C–C) bonds [86]. This instability can lead to the formation of various defect states, which can transition into electrically active traps.

The transformation process of a metastable neutral defect into an electrically activated trap is depicted in Fig. 11. In Fig. 11(a), interfacial carbon atoms in the SiC lattice share unstable C–C bonds. This configuration is prone to losing energy and transitioning into a different structure. Fig. 11(b) shows the configuration after this energy loss, where the excess carbon atoms on the oxide side settle into a low-energy state, becoming capable of capturing holes. In another stable configuration, shown in Fig. 11(c), an extra oxygen atom is inserted, which creates a site capable of capturing an electron. This demonstrates that the SiC lattice and the SiO_2 layer are not strictly separated; instead, excess carbon atoms tend to form a stable intermediate Si–O–C interlayer. This phenomenon has been observed using angle-resolved X-ray photoelectron spectroscopy, which revealed the formation of such interlayers [88]. Eventually, these metastable carbon-related defects transition into a stable $Si_xC_yO_z$ layer, which is typically only 1–2 atomic layers thick. This transition layer can be detected by microscopic Z-contrast imaging of the SiC/SiO_2 interface, providing insight into the atomic-scale

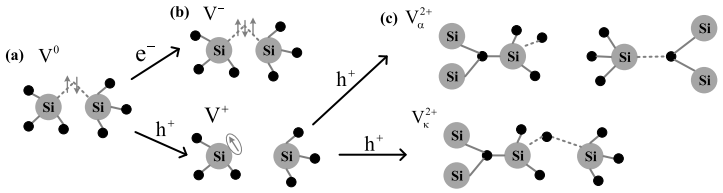

Fig. 12. Formation of oxygen vacancy. In Step 1, the electrical neutral structure in (a) capturing electrons or holes transfers to charged vacancies in (b). In Step 2, structure in (b) is activated by hole injection during NBTS. The structure in (c) is flexible and further deforms the silicon dioxide network. Reproduced from [94].

interactions that contribute to defect formation and device degradation [86].

B. Oxide Traps and Gate Oxide Failures

The oxide traps are defects located within the oxide layer, close to the SiC/SiO_2 interface, in a region shallow enough to easily capture or tunnel charge carriers from the interface and the channel, as illustrated in Fig. 10(c) [89]. Near-interface traps reside within the oxide, close to the interface, and primarily affect the long-term reliability of the device by contributing to charge trapping and detrapping, impacting BTI [90] and long-term threshold voltage shifts [91]. Interface traps, on the other hand, located at the SiC/SiO_2 interface, directly interact with the channel carriers, leading to mobility degradation [84], [85], threshold voltage instability [92], and increased subthreshold slope [93].

The formation and origin of these oxide traps have been extensively studied, with research focusing on the various microscopic processes involved in oxidation and the physical nature of the resulting defects [94], [95], [96], [97], [98], [99]. Several types of intrinsic oxide defects can form during thermal oxidation, each contributing differently to the device's behavior. Below is a brief description of the key defect types: silicon interstitial (Si_i) [95], carbon dimer interstitial ($C_i = C_i$) [95], carbon dimer interstice oxygen O ($C_o = C_o$) [96], and O vacancies (known as E' precursors) [94]. Efforts to mitigate these defects through optimized oxidation processes and post-oxidation treatments are key areas of ongoing research in the field.

Insufficient oxidation leads to the aggregate of silicon atoms near the interface, resulting in a high density of Si atoms replacing oxygen atoms. The interstitial defects, denoted as Si_i, shift toward oxygen atoms, altering the bond angles. Defects with a larger O–Si–O angle are particularly effective at capturing electrons [97]. These Si_i defects adopt a threefold coordination, enabling the trivalent oxygen atom to donate electrons.

Carbon-related defects in the oxide are significant because carbon atoms can form carbon dimers, which act as acceptors by capturing holes from the SiC lattice [95], [97]. However, carbon dimers are metastable, particularly in the presence of neighboring oxygen atoms. When a carbon dimer captures four electrons, it can reconstruct into $C_o = C_o$, releasing a negatively charged oxygen interstitial (O^{2-}). These metastable structures are sensitive to applied stresses; under positive stress, carbon dimers readily capture electrons from the conduction band [95], [96]. The system eventually reaches a steady state when no oxygen neighbors are present near the carbon dimer

$$(C_i = C_i)^0 + 4e^- \Rightarrow (C_o = C_o)^0 + 2O^{-2}. \tag{10}$$

Oxygen vacancies play a critical role as precursors in the formation of oxide defects under various bias conditions. As illustrated in Fig. 12, injected holes can transform neutral oxygen vacancies $O_3 \equiv Si = Si \equiv O_3$ (V^0) into positively charged V^+ centers ($O_3 \equiv Si + \cdots Si \equiv O_3$) [94]. Following this transformation, additional ionization can lead to two possible configurations based on the V^+ centers: V_α^{2+} and V_κ^{2+}, which differ in the initial Si–Si distance and positions after hole capture [94]. The formation of double-ionized oxide vacancies, or E' centers, causes significant mismatches in the silicon dioxide network. These E' centers, detected using electrically detected magnetic resonance (EDMR) measurements [98] are formed when high-energy holes are captured by weak Si–Si bonds, with an activation energy of approximately 1.1 eV [99]. Consequently, E' centers act as hole traps [94].

The threshold voltage reflects the presence of trapped charges and often serves as an early indicator of gate oxide degradation. This can result in a threshold voltage shift (ΔV_{th}) [100], C–V curve shift [101], and hysteresis [102]. Threshold voltage shifts can be measured by comparing conditions before and after stress application or by altering the measurement conditions. The variation in threshold voltage due to defects inside the gate oxide Q_{ot} and interface D_{it} is expressed as follows [103]:

$$V_{\text{th}} = V_{\text{th0}} - \frac{Q_{\text{ot}}}{C_{\text{ox}}} + \frac{q D_{\text{it}}}{C_{\text{ox}}} \tag{11}$$

where C_{ox} represents the gate oxide capacitance measured in accumulation mode, q is the elementary charge, and V_{th0} stands for the threshold voltage without any defects. Threshold voltage instability is highly sensitive to measurement conditions, so the sweep rate and direction of measurements must be carefully controlled. For example, experimental data show that a slow sweep rate (1-s sweep time) results in smaller threshold voltage instability ($\Delta V_{\text{th}} = 0.4$ V) compared to a fast sweep rate (10^{-4} s) after applying positive stress. This difference arises because slower measurements allow sufficient time for neutralization and recovery of charged near-interface oxide traps (NIOTs) [104].

The activation energies of traps vary depending on their energy level. Charge trapped in deep states can only be activated under high-magnitude, long-duration stress tests. At low and medium electrical fields [91], electron trapping in NIOTs

TABLE III
SUMMARY OF FAILURE MECHANISMS OF SiC MOS DEVICES

Failure locations	Defect origins	Experimental supports	D_{it} at E_c-E ($cm^{-2}eV^{-1}$)	Ref
Near interface	Interface traps	C-V + thermal relaxation	5×10^{12} @ 0.2eV	[108]
	Transition layers	Microscopic Z-contrast image	1×10^{11} @ 0.2eV	[86]
		Angle-resolved x-ray photoelectron spectroscopy	6×10^{11} @ 0.2eV	[88, 109]
		electron-energy-loss (EELS)	—	[86]
	Carbon clusters	IPE current	8×10^{12} @ 0.2eV	[84, 110]
	Heavy nitridation	Small Weibull slope + short t_{BD} + anomalous I_g	2×10^{12} @ 0.2eV	[79]
		Worse $-\Delta V_{th}$	—	[92]
Oxide	Si_i	DFT calculations	5×10^{12} @ 0.2eV	[95, 96]
	E' centres	EPR	—	[94]
		Arrhenius plot + ΔV_{th}	—	[99]
		Holes injection current	2.5×10^{12} @ 0.2eV	[78]
		Electron spin resonance	8×10^{11} @ 0.2eV	[80]

induces a positive threshold voltage shift. However, under large magnitude stress (+30 V) [105], the hot holes generated at the polysilicon surface lead to impact ionization [106]. These hot holes are subsequently trapped by oxygen vacancies in the gate oxide, resulting in a negative ΔV_{th}, even under positive stress [107].

C. Failure Mechanisms Summary

Table III provides an overview of the causes of device failure and the underlying microscopic physics. Key contributors to device failure include interface traps and oxide traps. Interface defects, which significantly degrade oxide near the interface, are primarily attributed to transition layers and carbon clusters at the SiO_2/SiC interface. The formation of oxide traps is influenced by interstitial atoms and vacancies within the silicon dioxide network. These defects often form metastable structures that produce E' centers, which have a strong propensity to capture holes. Understanding these failure mechanisms is crucial for improving the reliability and performance of SiC-based devices.

IV. CONCLUSION

In summary, understanding dielectric breakdown in gate oxides is crucial for predicting the reliability of semiconductor devices. The E model, $1/E$ model, and TAT model each offer distinct perspectives on breakdown mechanisms and have their respective strengths and limitations. The E model emphasizes the role of electric fields in driving the thermochemical degradation of the oxide, where the breakdown time exhibits an exponential dependence on the electric field. This model is useful for understanding breakdown under CV but may overestimate lifetime predictions. The $1/E$ model, focusing on charge injection and tunneling effects, provides a different perspective by considering how conduction current and injected charges contribute to breakdown. This model is advantageous for explaining observed polarity effects and discrepancies in breakdown data. The combined $E + 1/E$ model proposes a more comprehensive approach by integrating both field- and charge-driven mechanisms. This hybrid model acknowledges that both the electric field and charge injection play roles in oxide degradation, offering a more nuanced view that can be applied across a broader range of conditions.

A comprehensive understanding of defects at the atomic level in semiconductor materials, particularly in the context of SiO_2/SiC interfaces and gate oxides, reveals crucial insights into device performance and reliability. Near-interface oxide traps are primarily influenced by carbon-related defects, which arise from incomplete oxidation and result in reduced channel mobility. The formation of active carbon clusters and transition layers leads to the capture of electrons and enhancement of Coulomb scattering. Oxide traps, including silicon interstitial, carbon dimers, and oxygen vacancies, can capture or tunnel charge carriers, affecting the flow of current and overall device performance. The transformation of neutral oxygen vacancies into charged states and their role as precursors in defect formation highlights the complex interplay of microscopic processes during oxidation.

REFERENCES

[1] J. Casady and R. W. Johnson, "Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review," *Solid-State Electron.*, vol. 39, no. 10, pp. 1409–1422, 1996.

[2] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath, and C. A. Teixeira, "The benefits of SiC MOSFETs in a T-type inverter for grid-tie applications," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2808–2821, Apr. 2017, doi: 10.1109/TPEL.2016.2582344.

[3] J. Millán, P. Godignon, X. Perpi na, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[4] Z. Zeng, X. Zhang, F. Blaabjerg, H. Chen, and T. Sun, "Stepwise design methodology and heterogeneous integration routine of air-cooled SiC inverter for electric vehicle," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3973–3988, Apr. 2020.

[5] H. Zheng, X. Wang, X. Wang, L. Ran, and B. Zhang, "Using SiC MOSFETs to improve reliability of EV inverters," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2015, pp. 359–364.

[6] T. Iwanaga, H. Omori, K. Sakamoto, T. Morizane, and N. Kimura, "A study of a newly developed Kelvin-source driven SiC-VMOSFET on a high-power single-ended wireless EV charger," in *Proc. 8th Int. Conf. Renew. Energy Res. Appl. (ICRERA)*, Nov. 2019, pp. 717–721.

[7] V. Van Cuong, T. Meguro, S. Ishikawa, T. Maeda, H. Sezaki, and S.-I. Kuroki, "Amplifier based on 4H-SiC MOSFET operation at 500°C for harsh environment applications," *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4194–4199, Aug. 2022.

[8] J. Mo, L. M. Middelburg, B. Morana, H. W. van Zeijl, S. Vollebregt, and G. Zhang, "Surface-micromachined silicon carbide Pirani gauges for harsh environments," *IEEE Sensors J.*, vol. 21, no. 2, pp. 1350–1358, Jan. 2021, doi: 10.1109/JSEN.2020.3019711.

[9] R. Pascu, M. Kusko, O. Ionescu, G. Pristavu, and G. Brezeanu, "Electrical defects in grown oxide on SiC and from the oxide/SiC interface," in *Proc. Int. Semicond. Conf. (CAS)*, Oct. 2020, pp. 37–40.

[10] J. W. McPherson and H. C. Mogul, "Underlying phySiCs of the thermochemical e model in describing low-field time-dependent dielectric breakdown in SiO_2 thin films," *J. Appl. Phys.*, vol. 84, no. 3, pp. 1513–1523, Aug. 1998.

[11] I.-C. Chen, S. E. Holland, and C. Hu, "Electrical breakdown in thin gate and tunneling oxides," *IEEE Trans. Electron Devices*, vols. ED-32, no. 2, pp. 413–422, Feb. 1985.

[12] T. Liu, S. Zhu, M. H. White, A. Salemi, D. Sheridan, and A. K. Agarwal, "Time-dependent dielectric breakdown of commercial 1.2 kV 4H-SiC power MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 633–639, 2021, doi: 10.1109/JEDS.2021.3091898.

[13] K. Okada, K. Kurimoto, and M. Suzuki, "Anomalous TDDB statistics of gate dielectrics caused by charging-induced dynamic stress relaxation under constant-voltage stress," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2268–2274, Jun. 2016.

[14] L. Shi et al., "Effects of oxide electric field stress on the gate oxide reliability of commercial SiC power MOSFETs," in *Proc. IEEE 9th Workshop Wide Bandgap Power Devices*, Nov. 2022, pp. 45–48.

[15] O. Aviñó-Salvadó et al., "PhySiCs-based strategies for fast TDDB testing and lifetime estimation in SiC power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 71, no. 5, pp. 1–10, May 2023.

[16] M. Gurfinkel et al., "Time-dependent dielectric breakdown of 4h-SiC/SiO_2 MOS capacitors," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 4, pp. 635–641, May 2008.

[17] M. Le-Huu et al., "Investigation of the reliability of 4H–SiC MOS devices for high temperature applications," *Microelectron. Rel.*, vol. 51, no. 8, pp. 1346–1350, Aug. 2011.

[18] J. W. McPherson, "Determination of the nature of molecular bonding in silica from time-dependent dielectric breakdown data," *J. Appl. Phys.*, vol. 95, no. 12, pp. 8101–8109, Jun. 2004.

[19] J. W. McPherson, "Time dependent dielectric breakdown phySiCs-models revisited," *Microelectron. Rel.*, vol. 52, nos. 9–10, pp. 1753–1760, Sep. 2012.

[20] P. Fiorenza et al., "Temperature-dependent fowler-nordheim electron barrier height in SiO_2/4H-SiC MOS capacitors," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 38–42, May 2018.

[21] D. Arnold, E. Cartier, and D. J. DiMaria, "Theory of high-field electron transport and impact ionization in silicon dioxide," *Phys. Rev. B, Condens. Matter*, vol. 49, pp. 10278–10297, Apr. 1994.

[22] P. Moens, J. Franchi, J. Lettens, L. D. Schepper, M. Domeij, and F. Allerstam, "A charge-to-breakdown (QBD) approach to SiC gate oxide lifetime extraction and modeling," in *Proc. 32nd Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Sep. 2020, pp. 78–81.

[23] J. W. McPherson, "Polarity dependent thermochemical E-model for describing time dependent dielectric breakdown in metal-oxide-semiconductor devices with hyper-thin gate dielectrics," *J. Appl. Phys.*, vol. 120, no. 10, Sep. 2016, Art. no. 104102.

[24] M. Masunaga, Y. Sasago, Y. Mori, and D. Hisamoto, "Time-dependent dielectric breakdown of SiC-CMOS technology for harsh environments," *Appl. Phys. Lett.*, vol. 124, no. 4, Jan. 2024, Art. no. 042103.

[25] J. W. McPherson, R. B. Khamankar, and A. Shanware, "Complementary model for intrinSiC time-dependent dielectric breakdown in SiO_2 dielectrics," *J. Appl. Phys.*, vol. 88, no. 9, pp. 5351–5359, Nov. 2000.

[26] U. Schwalke, M. Pölzl, T. Sekinger, and M. Kerber, "Ultra-thick gate oxides: Charge generation and its impact on reliability," *Microelectron. Rel.*, vol. 41, no. 7, pp. 1007–1010, Jul. 2001.

[27] T. Miyakawa, T. Ichiki, J. Mitsuhashi, K. Miyamoto, T. Tada, and T. Koyama, "Study of time dependent dielectric breakdown distribution in ultrathin gate oxide," *Jpn. J. Appl. Phys.*, vol. 46, no. 7L, p. L691, Jul. 2007.

[28] S. Zhu, "Investigation of gate leakage current behavior for commercial 1.2 kv 4H-SiC power MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, May 2021, pp. 1–7.

[29] E. Rosenbaum, J. C. King, and C. Hu, "Accelerated testing of SiO_2 reliability," *IEEE Trans. Electron Devices*, vol. 43, no. 1, pp. 70–80, Apr. 1996.

[30] P. Samanta, "Calculation of the probability of hole injection from polysilicon gate into silicon dioxide in MOS structures under high-field stress," *Solid-State Electron.*, vol. 43, no. 9, pp. 1677–1687, Sep. 1999.

[31] J. Qian et al., "Modeling of charge-to-breakdown with an electron trapping model for analysis of thermal gate oxide failure mechanism in SiC power MOSFETs," *Materials*, vol. 17, no. 7, p. 1455, Mar. 2024.

[32] J. Qian et al., "Investigation of the constant current stress for charge-to-breakdown extraction in commercial SiC power MOSFETs," in *Proc. IEEE 10th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Dec. 2023, pp. 1–4.

[33] D. Heh, E. M. Vogel, and J. B. Bernstein, "Impact of substrate hot hole injection on ultrathin silicon dioxide breakdown," *Appl. Phys. Lett.*, vol. 82, no. 19, pp. 3242–3244, May 2003.

[34] E. Van Brunt, D. J. Lichtenwalner, J. H. Park, S. Ganguly, and J. W. McPherson, "Lifetime modeling of the 4H-SiC MOS interface in the HTRB condition under the influence of screw dislocations," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2023, pp. 1–4.

[35] H. Nemoto et al., "Conduction mechanisms of oxide leakage current in p-channel 4H-SiC MOSFETs," *Jpn. J. Appl. Phys.*, vol. 59, no. 4, Mar. 2020, Art. no. 044003.

[36] L. Larcher, A. Padovani, F. M. Puglisi, and P. Pavan, "Extracting atomic defect properties from leakage current temperature dependence," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5475–5480, Dec. 2018, doi: 10.1109/TED.2018.2874513.

[37] C. Schleich et al., "Single- versus multi-step trap assisted tunneling currents—Part II: The role of polarons," *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4486–4493, Aug. 2022.

[38] J. Berens, M. V. Mistry, D. Waldhör, A. Shluger, G. Pobegen, and T. Grasser, "Origin of trap assisted tunnelling in ammonia annealed SiC trench MOSFETs," *Microelectron. Rel.*, vol. 139, Dec. 2022, Art. no. 114789.

[39] M. Sometani et al., "Temperature-dependent analysis of conduction mechanism of leakage current in thermally grown oxide on 4H-SiC," *J. Appl. Phys.*, vol. 117, no. 2, Jan. 2015, Art. no. 024505.

[40] J. Chbili et al., "Influence of lucky defect distributions on early TDDB failures in SiC power MOSFETs," in *Proc. IEEE Int. Integr. Rel. Workshop (IIRW)*, Oct. 2017, pp. 1–4.

[41] Z. Chbili et al., "Massively parallel TDDB testing: SiC power devices," in *Proc. IEEE Int. Integr. Rel. Workshop (IIRW)*, Oct. 2015, pp. 91–94.

[42] V. Mulpuri and S. Choi, "Degradation of SiC MOSFETs with gate oxide breakdown under short circuit and high temperature operation," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2017, pp. 2527–2532.

[43] H. Chen et al., "A unified 4H-SIC MOSFETs TDDB lifetime model based on leakage current mechanism," in *Proc. China Semicond. Technol. Int. Conf. (CSTIC)*, Jun. 2020, pp. 1–3.

[44] X. Chen et al., "Deep understanding of negative gate voltage restriction for SiC MOSFET under wide temperature range," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8622–8627, Aug. 2021, doi: 10.1109/TPEL.2021.3056435.

[45] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, "Reliability issues of SiC MOSFETs: A technology for high-temperature environments," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 4, pp. 418–426, Dec. 2010.

[46] G. Wang, B. Peng, L. Yuan, Y. Zhang, and R. Jia, "Impact of process on gate leakage current and time-dependent dielectric breakdown failure mechanisms of 4H-SiC MOS capacitors," *IEEE Trans. Electron Devices*, vol. 71, no. 7, pp. 4039–4044, Jul. 2024.

[47] S. Jiang, M. Zhang, X. Meng, X. Zheng, S. Feng, and Y. Zhang, "Trap characterization of trench-gate SiC MOSFETs based on transient drain current," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6555–6565, May 2023, doi: 10.1109/TPEL.2023.3242950.

[48] Y. Xu, T.-M. Lu, and J. L. Plawsky, "A transport model describing how defect accumulation leads to intrinSiC dielectric breakdown and post-breakdown conduction," *Microelectron. Rel.*, vol. 128, Jan. 2022, Art. no. 114459.

[49] J.-W. Hu, P.-C. Huang, P.-W. Huang, J.-Y. Jiang, C.-F. Huang, and T.-L. Wu, "Toward understanding thickness dependence on dielectric breakdown mechanism under forward gate bias in 4H-SiC MOS technologies," *IEEE Trans. Electron Devices*, vol. 70, no. 4, pp. 2175–2178, Apr. 2023.

[50] Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky, "Measurement of fowler-nordheim tunneling currents in MOS structures under charge trapping conditions," *Solid-State Electron.*, vol. 28, no. 7, pp. 717–720, Jul. 1985.

[51] R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, "A consistent model for the thickness dependence of intrinSiC breakdown in ultra-thin oxides," in *IEDM Tech. Dig.*, Dec. 1995, pp. 863–866.

[52] E. Y. Wu, B. Li, J. H. Stathis, and C. LaRow, "Time-dependent clustering model versus combination-based approach for BEOL/MOL and FEOL non-uniform dielectric breakdown: Similarities and disparities," in *Proc. IEEE Int. Rel. Phys. Symp.*, Jun. 2014, pp. 5B.2.1–5B.2.7.

[53] E. Wu, B. Li, J. H. Stathis, R. Achanta, R. Filippi, and P. McLaughlin, "A time-dependent clustering model for non-uniform dielectric breakdown," in *IEDM Tech. Dig.*, Dec. 2013, pp. 1531–1534.

[54] J. Verweij and J. Klootwijk, "Dielectric breakdown I: A review of oxide breakdown," *Microelectron. J.*, vol. 27, no. 7, pp. 611–622, 1996.

[55] S. Hino, T. Hatayama, J. Kato, E. Tokumitsu, N. Miura, and T. Oomori, "High channel mobility 4H-SiC metal-oxide-semiconductor field-effect transistor with low temperature metal-organic chemical-vapor deposition grown Al_2O_3 gate insulator," *Appl. Phys. Lett.*, vol. 92, no. 18, May 2008, Art. no. 183503.

[56] A. Siddiqui, R. Y. Khosa, and M. Usman, "High-k dielectrics for 4H-silicon carbide: Present status and future perspectives," *J. Mater. Chem. C*, vol. 9, no. 15, pp. 5055–5081, 2021.

[57] R. Ravichandran, A. X. Wang, and J. F. Wager, "Solid state dielectric screening versus band gap trends and implications," *Opt. Mater.*, vol. 60, pp. 181–187, Oct. 2016.

[58] T. Hosoi et al., "Performance and reliability improvement in SiC power MOSFETs by implementing AlON high-k gate dielectrics," in *IEDM Tech. Dig.*, Dec. 2012, pp. 741–744.

[59] C.-Y. Lu et al., "Effect of process variations and ambient temperature on electron mobility at the SiOEffect of process variations and ambient temperature on electron mobility at the SiO_2/4H-SiC interface," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1582–1588, Jul. 2003.

[60] J. Rozen et al., "Scaling between channel mobility and interface state density in SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3808–3811, Nov. 2011.

[61] L. A. Lipkin, M. K. Das, and J. W. Palmour, "N_2O processing improves the 4H-SiC: SiO_2 interface," in *Proc. Mater. Sci. Forum*, vol. 389, 2001, pp. 985–988.

[62] P. Fiorenza et al., "Comparative study of gate oxide in 4H-SiC lateral MOSFETs subjected to post-deposition-annealing in N_2O and $POCl_3$," *Appl. Phys. A, Solids Surf.*, vol. 115, no. 1, pp. 333–339, Apr. 2014.

[63] A. Chanthaphan, T. Hosoi, T. Shimura, and H. Watanabe, "Study of SiO_2/4H-SiC interface nitridation by post-oxidation annealing in pure nitrogen gas," *AIP Adv.*, vol. 5, no. 9, Sep. 2015, Art. no. 097134.

[64] R. Li et al., "Hydrogen etching of 4H–SiC(0001) facet and step formation," *Mater. Sci. Semiconductor Process.*, vol. 149, Oct. 2022, Art. no. 106896.

[65] J. T. Wolan et al., "Effect of hydrogen etching and subsequent sacrificial thermal oxidation on morphology and composition of 4H-SiC surfaces," *J. Electron. Mater.*, vol. 31, no. 5, pp. 380–383, May 2002.

[66] K. Mikami, K. Tachiki, M. Kaneko, and T. Kimoto, "Insight into mobility improvement by the oxidation-minimizing process in SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 71, no. 1, pp. 931–934, Jan. 2024.

[67] K. Tachiki, K. Mikami, K. Ito, M. Kaneko, and T. Kimoto, "Mobility enhancement in heavily doped 4H-SiC (0001), (1120), and (1100) MOSFETs via an oxidation-minimizing process," *Appl. Phys. Exp.*, vol. 15, no. 7, Jun. 2022, Art. no. 071001.

[68] S. Asaba, T. Schimizu, Y. Nakabayashi, S. Fukatsu, T. Ito, and R. Iijima, "Novel gate insulator process by nitrogen annealing for Si-face SiC MOSFET with high-mobility and high-reliability," *Mater. Sci. Forum*, vol. 924, pp. 457–460, 2018.

[69] Z. Yin, C. Yang, F. Zhang, Y. Su, F. Qin, and D. Wang, "Low-temperature re-oxidation of near-interface defects and voltage stability in SiC MOS capacitors," *Appl. Surf. Sci.*, vol. 531, Nov. 2020, Art. no. 147312.

[70] G. Y. Chung et al., "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide," *IEEE Electron Device Lett.*, vol. 22, no. 4, pp. 176–178, Apr. 2001, doi: 10.1109/55.915604.

[71] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, and T. Fuyuki, "Improved inversion channel mobility in 4H-SiC MOSFETs on Si face utilizing phosphorus-doped gate oxide," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 710–712, Jul. 2010, doi: 10.1109/LED.2010.2047239.

[72] D. Okamoto, M. Sometani, S. Harada, R. Kosugi, Y. Yonezawa, and H. Yano, "Improved channel mobility in 4H-SiC MOSFETs by boron passivation," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1176–1178, Dec. 2014.

[73] M. Cabello, V. Soler, J. Montserrat, J. Rebollo, J. M. Rafí, and P. Godignon, "Impact of boron diffusion on oxynitrided gate oxides in 4H-SiC metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 111, no. 4, pp. 1–20, Jul. 2017.

[74] K. Chokawa, M. Araidai, and K. Shiraishi, "Effects of annealing with CO and CO_2 molecules on oxygen vacancy defect density in amorphous SiO_2 formed by thermal oxidation of SiC," *J. Appl. Phys.*, vol. 124, no. 13, Oct. 2018, Art. no. 135701.

[75] T. Hosoi et al., "Impact of post-nitridation annealing in CO_2 ambient on threshold voltage stability in 4H-SiC metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Exp.*, vol. 15, no. 6, May 2022, Art. no. 061003.

[76] M. Cabello, V. Soler, G. Rius, J. Montserrat, J. Rebollo, and P. Godignon, "Advanced processing for mobility improvement in 4H-SiC MOSFETs: A review," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 22–31, May 2018.

[77] C.-T. Yen et al., "Negative bias temperature instability of SiC MOSFET induced by interface trap assisted hole trapping," *Appl. Phys. Lett.*, vol. 108, no. 1, Jan. 2016, Art. no. 012106.

[78] J. Rozen et al., "Increase in oxide hole trap density associated with nitrogen incorporation at the SiO_2/SiC interface," *J. Appl. Phys.*, vol. 103, no. 12, Jun. 2008, Art. no. 124513.

[79] E. Murakami and M. Okamoto, "Anomalous behavior of gate current and TDDB lifetime by constant voltage stress in NO-annealed SiC-MOSFETs," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1207–1213, Mar. 2021, doi: 10.1109/TED.2020.3049114.

[80] J. Rozen, S. Dhar, M. E. Zvanut, J. R. Williams, and L. C. Feldman, "Density of interface states, electron traps, and hole traps as a function of the nitrogen density in SiO_2 on SiC," *J. Appl. Phys.*, vol. 105, no. 12, Jun. 2009, Art. no. 124506.

[81] S. Harada et al., "Relationship between channel mobility and interface state density in SiC metal–oxide–semiconductor field-effect transistor," *J. Appl. Phys.*, vol. 91, no. 3, pp. 1568–1571, Feb. 2002.

[82] H. Yano, T. Hatayama, Y. Uraoka, and T. Fuyuki, "High temperature no annealing of deposited SiO_2 and SiON films on n-type 4H-SiC," in *Proc. Mater. Sci. Forum*, vol. 483, 2004, pp. 685–688.

[83] T. Kimoto, H. Kawano, M. Noborio, J. Suda, and H. Matsunami, "Improved dielectric and interface properties of 4H-SiC MOS structures processed by oxide deposition and N₂O annealing," *Mater. Sci. Forum*, vols. 527–529, pp. 987–990, Oct. 2006.

[84] V. V. Afanasev, M. Bassler, G. Pensl, and M. Schulz, "IntrinSiC SiC/SiO_2 interface states," *Phys. Status Solidi (a)*, vol. 162, no. 1, pp. 321–337, Jul. 1997.

[85] G. Liu, B. R. Tuttle, and S. Dhar, "Silicon carbide: A unique platform for metal-oxide-semiconductor phySiCs," *Appl. Phys. Rev.*, vol. 2, no. 2, Jun. 2015, Art. no. 021307.

[86] S. T. Pantelides, "Si/SiO_2 and SiC/SiO_2 interfaces for MOSFETs—Challenges and advances," in *Proc. Mater. Sci. Forum*, 2006, pp. 935–948.

[87] M. Bassler, G. Pensl, and V. Afanasev, "Carbon cluster model for electronic states at SiC/SiO_2 interfaces," *Diamond Rel. Mater.*, vol. 6, no. 10, pp. 1472–1475, 1997.

[88] A. Ekoué, "Study of the wet re-oxidation annealing of SiO_2/4H-SiC (0001) interface properties by AR-xps measurements," in *Proc. Mater. Sci. Forum*, vol. 433, 2003, pp. 555–558.

[89] N. Tega, S. Sato, and A. Shima, "Comparison of extremely high-temperature characteristics of planar and three- dimensional SiC MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1382–1384, Sep. 2019, doi: 10.1109/LED.2019.2930712.

[90] J. Xin, M. Du, Z. Ouyang, and K. Wei, "Online monitoring for threshold voltage of SiC MOSFET considering the coupling impact on BTI and junction temperature," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 1772–1777, Apr. 2021, doi: 10.1109/TED.2021.3056634.

[91] L. Yang et al., "Gate oxide instability of 4H-SiC p-channel MOSFET induced by AC stress at 200 °C," *IEEE Trans. Electron Devices*, vol. 70, no. 1, pp. 379–382, Jan. 2023.

[92] H. Yano, N. Kanafuji, A. Osawa, T. Hatayama, and T. Fuyuki, "Threshold voltage instability in 4H-SiC MOSFETs with phosphorus-doped and nitrided gate oxides," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 324–332, Feb. 2015.

[93] S. M. Thomas et al., "Enhanced field effect mobility on 4H-SiC by oxidation at 1500 °C," *IEEE J. Electron Devices Soc.*, vol. EDS-2, no. 5, pp. 114–117, Sep. 2014.

[94] A. Kimmel, P. Sushko, A. Shluger, and G. Bersuker, "Positive and negative oxygen vacancies in amorphous silica," *ECS Trans.*, vol. 19, no. 2, pp. 3–17, May 2009.

[95] J. M. Knaup, P. Deák, T. Frauenheim, A. Gali, Z. Hajnal, and W. J. Choyke, "Defects in SiO_2 as the possible origin of near interface traps in the SiC/SiO_2 system: A systematic theoretical study," *Phys. Rev. B, Condens. Matter*, vol. 72, no. 11, Sep. 2005, Art. no. 115323.

[96] P. Deák, J. M. Knaup, C. Thill, T. Frauenheim, T. Hornos, and A. Gali, "The mechanism of defect creation and passivation at the SiC/SiO_2 interface," *J. Phys. D, Appl. Phys.*, vol. 41, no. 20, Oct. 2007, Art. no. 6242.

[97] F. Zhang, C. Yang, Y. Su, and D. Wang, "Carrier capture and emission properties of silicon interstitial defects in near SiC/SiO_2 interface region," *Appl. Surf. Sci.*, vol. 514, Jun. 2020, Art. no. 145889.

[98] M. A. Anders, P. M. Lenahan, and A. J. Lelis, "Negative bias instability in 4H-SiC MOSFETs: Evidence for structural changes in the SiC," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2015, pp. 3E41–3E45.

[99] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "BaSiC mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron. Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015.

[100] S. Yu et al., "Bias-induced threshold voltage instability and interface trap density extraction of 4H-SiC MOSFETs," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2019, pp. 420–424.

[101] Z. Guo et al., "Study of vertical capacitance in an n-type 4H-SiC stepped thick-oxide trench MOS structure," *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4617–4623, Aug. 2022.

[102] G. L. Rødal, Y. V. Pushpalatha, D. A. Philipps, and D. Peftitsis, "Capacitance variations and gate voltage hysteresis effects on the turn-ON switching transients modeling of high-voltage SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 38, no. 5, pp. 6128–6142, May 2023, doi: 10.1109/TPEL.2023.3243951.

[103] X. Ye, C. Chen, Y. Wang, G. Zhai, and G. J. Vachtsevanos, "Online condition monitoring of power MOSFET gate oxide degradation based on Miller platform voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4776–4784, Aug. 2017.

[104] A. J. Lelis, D. B. Habersat, R. Green, and N. Goldsman, "Two-way tunneling model of oxide trap charging and discharging in SiC MOSFETs," in *Proc. Mater. Sci. Forum*, vol. 717, 2011, pp. 465–468.

[105] M. Xie, P. Sun, K. Wang, Q. Luo, and X. Du, "Online gate-oxide degradation monitoring of planar SiC MOSFETs based on gate charge time," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 7333–7343, Jun. 2022.

[106] A. G. M. Das, "Hot-electron induced impact-ionisation damage at the interface of sub-micron silicon MOS devices: Model and monitor," *Phys. B, Condens. Matter*, vol. 404, no. 22, pp. 4393–4396, Dec. 2009, doi: 10.1016/j.physb.2009.09.038.

[107] M. Noguchi, A. Koyama, T. Iwamatsu, H. Amishiro, H. Watanabe, and N. Miura, "Gate oxide instability and lifetime in SiC MOSFETs under a wide range of positive electric field stress," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2020, p. 23, doi: 10.1109/IEDM13553.2020.9371992.

[108] E. Pippel, J. Woltersdorf, H. Ö. Ólafsson, and E. Ö. Sveinbjörnsson, "Interfaces between 4H-SiC and SiO_2: Microstructure, nanochemistry, and near-interface traps," *J. Appl. Phys.*, vol. 97, no. 3, Feb. 2005, Art. no. 034302.

[109] R. Kosugi, T. Umeda, and Y. Sakuma, "Fixed nitrogen atoms in the SiO_2/SiC interface region and their direct relationship to interface trap density," *Appl. Phys. Lett.*, vol. 99, no. 18, Oct. 2011, Art. no. 182111.

[110] V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitrijev, "Mechanisms responsible for improvement of 4H–SiC/SiO_2 interface properties by nitridation," *Appl. Phys. Lett.*, vol. 82, no. 4, pp. 568–570, Jan. 2003.