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DOI
10.1109/LSSC.2023.3286779

Publication date
2023

Document Version
Final published version

Published in
IEEE Solid-State Circuits Letters

Citation (APA)
Rooijers, T., Huijsing, J. H. H., & Makinwa, K. A. A. (2023). A Chopper-Stabilized Amplifier with a Relaxed Fill-In Technique and 22.6pA Input Current. *IEEE Solid-State Circuits Letters*, *6*, 165 - 168. https://doi.org/10.1109/LSSC.2023.3286779

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A Chopper-Stabilized Amplifier With a Relaxed Fill-In Technique and 22.6-pA Input Current

Thije Rooijers, *Graduate Student Member, IEEE*, Johan H. Huijsing, *Life Fellow, IEEE*, and Kofi A. A. Makinwa, *Fellow, IEEE*

***Abstract*—In chopper amplifiers, the interaction between the input signal and the chopper clock can cause intermodulation distortion (IMD). This is mainly due to finite amplifier bandwidth, which causes signal-dependent output spikes at the chopping transitions. Such chopper-induced IMD can be mitigated by the fill-in technique, which involves ping-ponging between the outputs of two identical OTAs chopped in quadrature, thus generating a spike-free output. In this letter, a relaxed implementation is proposed in which the output of a fill-in OTA is only briefly used to avoid the spikes of a chopped main OTA. As a result, the fill-in OTA does not need to be chopped, and so it can be duty-cycled to save power. Furthermore, the chopper ripple caused by the main OTA can now be suppressed by a single low-noise ripple-reduction loop, rather than the two AZ loops required in a previous ping-pong implementation of the fill-in technique. Compared to the latter, the proposed amplifier achieves similar IMD performance (−125.7 dB), a 25× lower input current (22.6 pA), and a flat noise floor (12 nV/√Hz).**

***Index Terms*—Chopping, duty-cycled OTA, intermodulation distortion (IMD), relaxed fill-in technique.**

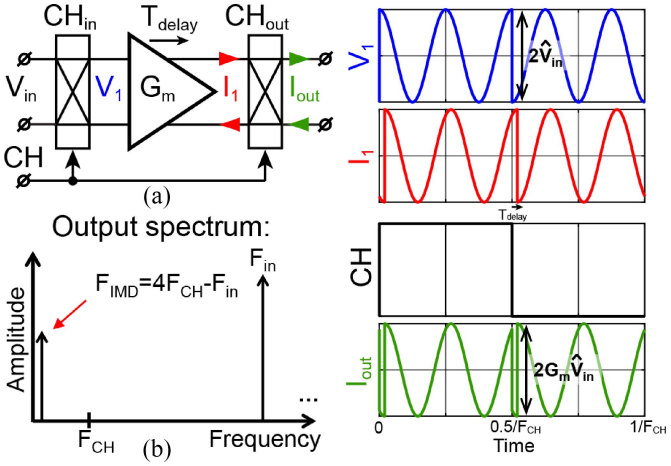

Fig. 1. (a) Chopped OTA with the resulting voltage and current waveforms. (b) Resulting output spectrum.

I. Introduction

Chopping is often used to reduce the offset and 1/*f* noise of CMOS amplifiers. However, in the presence of finite amplifier bandwidth (BW), chopping may cause intermodulation distortion (IMD) [1]. This can be understood by considering the signals in a chopped OTA (Fig. 1). Due to its finite BW, the OTA's output current I_1 will be a delayed version of the chopped input signal V_1. As a result, the polarity reversals in I_1 no longer coincide with those of the output chopper, causing large spikes in the output current I_{out}. These spikes occur at twice the chopping frequency ($2F_{\text{CH}}$) and thus give rise to IMD tones at $F_{\text{IMD}} = |nF_{\text{CH}} \pm F_{\text{in}}|$, where F_{in} is the input frequency and n is an even integer.

Out-of-band chopping ($F_{\text{CH}} >> F_{\text{in}}$) is often used to ensure that such tones can be easily filtered out. But increasing F_{CH} leads to increased offset and input current. In this letter, in-band chopping ($F_{\text{in}} < F_{\text{CH}}$) is used to avoid this tradeoff. However, when $F_{\text{in}} \sim nF_{\text{CH}}$ [Fig. 1(b)], the resulting IMD tones will fall in-band, and so cannot be filtered out.

In prior art [3], [4], spread spectrum chopper clocks have been used to address the problem. However, this only converts IMD tones into noise-like signals, thus lowering their effective amplitude, but at the expense of an increased noise floor.

Recently [1], the fill-in technique has been introduced to effectively eliminate IMD tones. It involves ping-ponging between the outputs of two identical OTAs that are chopped in quadrature, thus generating an output current that is free of chopping spikes.

Manuscript received 13 April 2023; revised 5 June 2023; accepted 9 June 2023. Date of publication 15 June 2023; date of current version 10 July 2023. This article was approved by Associate Editor Jiawei Xu. *(Corresponding author: Thije Rooijers.)*

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Digital Object Identifier 10.1109/LSSC.2023.3286779

In [1], each OTA is used 50% of the time. As a result, both their offsets contribute chopper ripple, and so both were reduced by auto-zeroing. However, the noise folding due to auto-zeroing then resulted in an up-modulated noise bump around F_{CH} in the amplifier's noise spectrum. Furthermore, the combination of chopping and auto-zeroing required ten input switches, whose activity resulted in a relatively high maximum input current of 600 pA.

In this letter, an extension of [6], a chopper-stabilized amplifier with a relaxed fill-in technique is proposed. It uses a simpler architecture to achieve similar IMD performance, as well as a flat noise spectrum and 25× lower input current.

II. Relaxed Fill-In

The implementation of the relaxed fill-in technique is shown in Fig. 2. The spikes in the output (I_{out1}) of a chopped main OTA (G_{m1}) are filled in by the output (I_{out2}) of a fill-in OTA (G_{m1}). As shown in Fig. 2(c), I_{out2} is only used briefly, greatly relaxing the requirements on G_{m2} compared to the implementation in [1], Fig. 2(b). The low duty-cycle suppresses the offset and 1/*f* noise of G_{m2}, which means that it does not need to be chopped. The 1/*f* noise and offset of G_{m1} can then be reduced by a ripple-reduction loop (RRL) without incurring a noise folding penalty. The lower limit of the duty cycle is set by the BW of G_{m1} (∼16.5 MHz). In this letter, a duty cycle of 0.4% was chosen to comfortably accommodate this over PVT.

The proposed chopper-stabilized amplifier is shown in Fig. 3. It consists of a main amplifier (A_{MAIN}), whose offset (and 1/*f* noise) appears between its input terminals when it is used in a negative feedback configuration, where it can be sensed and corrected by a chopped auxiliary amplifier. In this letter, the offset of a two-stage main amplifier (folded-cascode 1st stage and Class AB 2nd stage) is suppressed by a three-stage auxiliary amplifier. To mitigate its own offset (V_{os1}), the auxiliary amplifier employs a chopped OTA (G_{m1},

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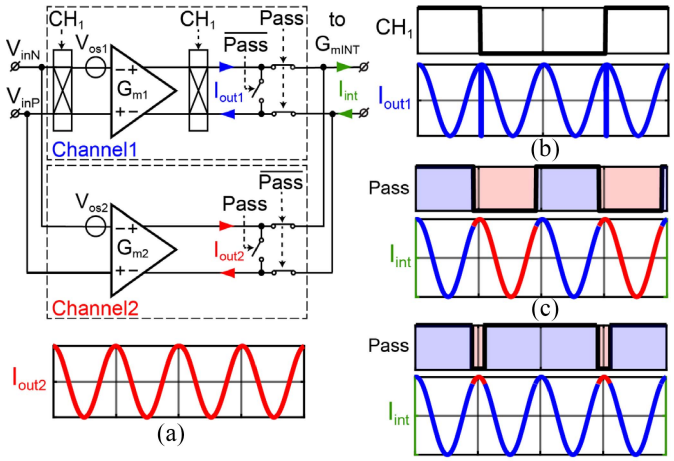

Fig. 2. (a) Fill-in implementation with two OTAs and multiplexing switches, the chopping signals, and the resulting output current with spikes. (b) Pass signal and resulting current for the prior art. (c) Pass signal and resulting current for the relaxed fill-in.

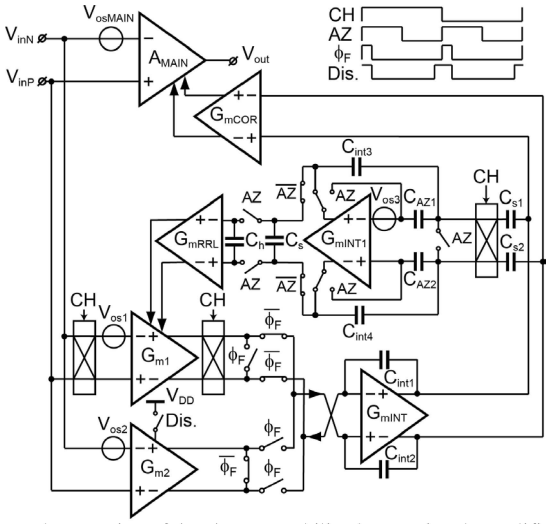

Fig. 3. Implementation of the chopper stabilized operational amplifier.

folded-cascode), followed by an integrator (G_{mINT}, folded-cascode, $C_{\mathrm{int1,2}} = 36$ pF), and a correction OTA (G_{mCOR}, telescopic). The fill-in OTA (G_{m2}) is a nonchopped replica of G_{m1}. Simulations show that its offset (< 1 mV) has a negligible effect on the residual offset of the overall amplifier and causes only a small (< 3 μV_{rms}) tone at $2F_{\mathrm{CH}}$ (40 kHz). Similarly, its $1/f$ noise also has a negligible effect, resulting in an overall $1/f$ noise corner of only 2 Hz in simulation. All required clocks are generated from a single off-chip 80-kHz clock by on-chip logic.

A. Low-IMD Ripple-Reduction Loop

The RRL consists of two capacitors $C_{s1,2}$ (3.6 pF) that sense the ripple due to V_{os1} at the output of the integrator formed by G_{mINT} and $C_{\mathrm{int1,2}}$. The resulting current is then demodulated and integrated by the RRL integrator formed by G_{mINT1} and $C_{\mathrm{int3,4}}$ (9 pF each). Its output is applied to G_{mRRL}, which cancels V_{os1} by injecting a correction current into G_{m1}. Since the amplitude of the ripple is limited by the offset of G_{mINT1}, this is auto-zeroed with the help of C_{AZ1} and C_{AZ2} (4 pF each).

However, the RRL can also create chopper-induced IMD, since the signal transitions caused by its ripple-demodulating choppers are delayed by the RRL integrator before they reach the output choppers

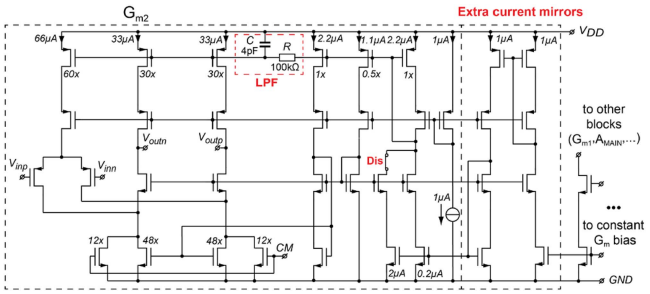

Fig. 4. Simplified implementation of G_{m2}.

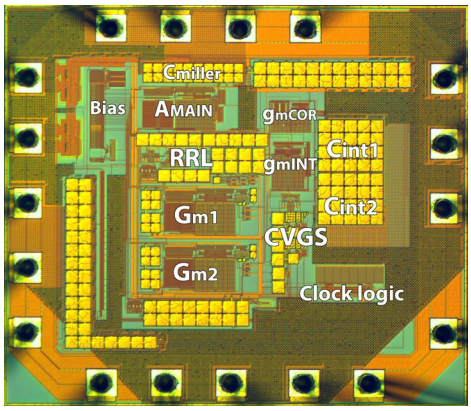

Fig. 5. Die micrograph of the fabricated chip.

of G_{m1}. In this design, this extra source of IMD is suppressed in two ways. First, the contribution of the RRL to the output current of G_{m1} is minimized by using a large G_{m1}/G_{mRRL} ratio. However, this is limited to ~600× by the swing of G_{mINT1} and the expected magnitude of V_{os1}. In the simulation, this limits the resulting IMD to −100 dB. To lower this further, a sample-and-hold is used to freeze the input of G_{mRRL} just before each chopping transition. Further low-pass filtering is achieved by using a small sampling capacitor C_s (=0.5 pF) to drive a larger hold capacitor C_H (=7.2 pF). These measures ensure that the overall IMD is not limited by the RRL.

B. Duty-Cycled OTA

Since G_{m2} is only used briefly, it can be turned "off" most of the time. The implementation of G_{m2} is shown in Fig. 4. To ensure that the process of turning it "on" and "off" does not itself cause input spikes and more distortion, three measures are taken. First, the OTA's main bias current is not completely turned off but just reduced 11× by switching it from 2.2 to 0.2 uA to mitigate the change in the various biasing voltages. Second, a lowpass filter (R = 100 kΩ and C = 4 pF) at the gates of the switched bias current sources of G_{m2} is used to slow down the bias-current transitions. Third, the transitions in these bias sources are isolated from the main bias-current generator and other circuit blocks by an extra set of current mirrors.

Simulations show that these measures ensure that the resulting spikes are well below the noise floor while incurring only a small power penalty. Switching the bias current of the fill-in OTA with a 20% duty-cycle (to allow sufficient settling) then results in a 76% power saving for G_{m2}.

III. Measurement Results

The opamp is realized in a 0.18-μm CMOS BCD process (Fig. 5) and has an active area of 0.57 mm^2. It draws 620 μA from a 5-V supply, which drops to 530 μA when the fill-in OTA is duty-cycled,

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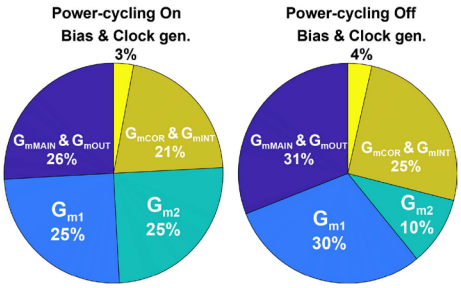

Fig. 6. Power breakdown with and without power-cycling.

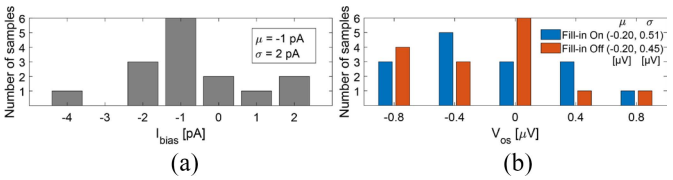

Fig. 7. (a) Histogram of the input current and (b) offset at 2.5 V for 15 samples.

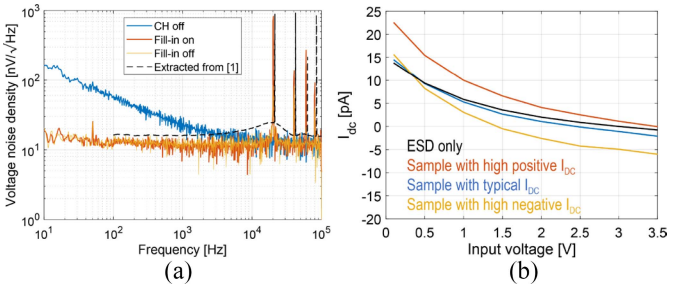

Fig. 8. (a) Voltage noise density versus frequency. (b) Input current versus input voltage.

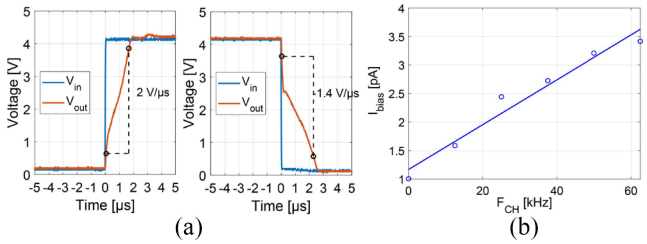

Fig. 9. (a) Slew rate with a 4-V input voltage step (0.2 to 4.2 V) in a buffer configuration. (b) Input current versus chopping frequency.

a 15% power saving. The power breakdown (Fig. 6) shows that the contribution of the fill-in OTA is then only 10%.

Measurements on 15 samples with a 2.5-V input CM voltage and F_{CH} = 20 kHz show that the opamp's input current remains below 4 pA [Fig. 7(a)] and that its offset does not exceed 0.8 μV [Fig. 7(b)]. Enabling and disabling ill-in only changes the offset slightly, confirming that not chopping the fill-in OTA does not significantly worsen the overall offset.

The opamp's voltage noise density is shown in Fig. 8(a) without chopping, with chopping, and with the fill-in OTA turned on and off. The measured voltage noise density of the opamp in [1] is also shown. Without chopping, the opamp has a 1/f noise corner frequency of about 2 kHz. With chopping, the use of an RRL eliminates the noise bump seen in [1], resulting in a flat noise floor with a lower (12 nV/$\sqrt{}$Hz) spectral density. The latter is mainly due to the higher biasing current used in the input stages of this design. The measured 1/f corner is below 10 Hz and is not affected when the fill-in OTA is enabled. Furthermore, no extra tones are created when it is duty-cycled, confirming the effectiveness of the various spike mitigation

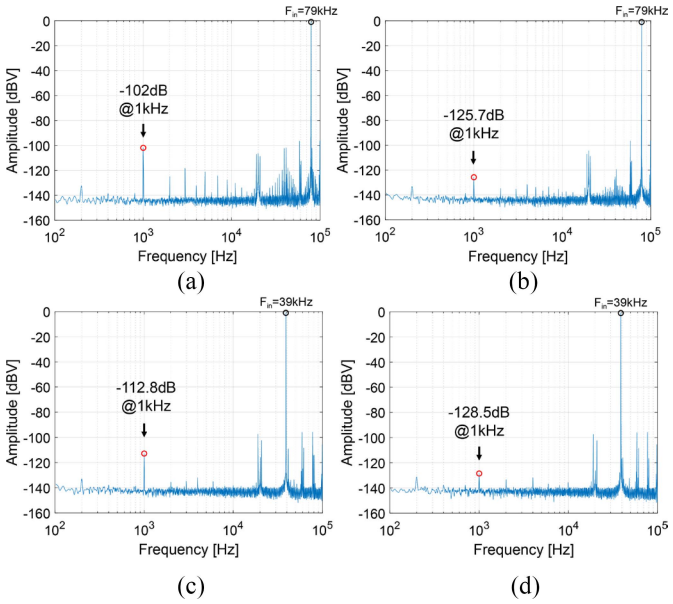

Fig. 10. (a) and (b) Measured amplitude spectrum with a single 79 kHz or (c) and (d) 39 kHz tone (a) and (c) without and (b) and (d) with the fill-in technique.

measures. Some crosstalk from the external clock can be observed at 20, 60, and 80 kHz.

Fig. 8(b) shows the input current versus input voltage characteristic of three samples: a typical sample, and two worst-case samples. All three draw more input current at low input voltages. Measurements of an un-connected pad show a similar trend, indicating that most of the input current at low input voltages is due to ESD diode leakage.

A step response measurement [Fig. 9(a)] shows that the opamp has a slew rate of 2 V/μs (up) and 1.4 V/μs (down), with no extra ringing due to the RRL. The input current at mid-supply is about 4 pA, which, as predicted in [7], is roughly 4× larger than that of an AZ-stabilized amplifier realized in the same process [7]. Measurements show that the input current at mid-supply increases linearly with F_{CH} [Fig. 9(b)], indicating that it is mainly due to the charge injection mismatch of the input chopper switches.

With the opamp configured as a buffer, a single 1V_{rms} 79 kHz ($\sim 4F_{CH}$) input tone results in the output amplitude spectrum shown in Fig. 10(a) and (b). Without the fill-in technique (a), a large −102-dB IMD tone is present at 1 kHz ($4F_{CH} - F_{in}$). Enabling the fill-in technique reduces this by 24 dB, to −125.7 dB (b). Measurements on 5 samples show that the achieved IMD spreads between 123 and 134.4 dB, demonstrating good robustness. With a similar 39 kHz tone ($\sim 2F_{CH}$), the IMD tone is –112.8 dB without fill-in and −128.5 dB with fill-in, a 16-dB improvement. At lower input frequencies (<5 kHz), the IMD tones are below the −140-dB noise floor.

When two input tones are applied (79 and 80 kHz, 0.5 V_{rms} each), the resulting amplitude spectrum is shown in Fig. 11. Without chopping, the IMD at 1 kHz is –112.4 dB, which increases to –106.9 dB with chopping and with fill-in disabled. Enabling the fill-in technique restores the IMD to –112.4 dB, demonstrating that it effectively suppresses chopper-induced IMD. Without fill-in, measurements show that the residual ripple amplitude at $2F_{CH}$ is around 0.7 μVrms. With fill-in, this increases to 2.5 μVrms for a worst-case sample with the largest fill-in OTA offset.

Table I summarizes the opamp's performance and compares it to state-of-the-art chopper and auto-zero amplifiers. It achieves similar IMD (−125.7 dB @ 79 kHz $\sim 4F_{CH}$) to [1], with a much simpler architecture. Among the chopper amplifiers, it achieves the lowest input current (22.6-pA max), only beaten by an AZ amplifier [5], with a trimmed input current and much worse IMD (−44 dB). Compared

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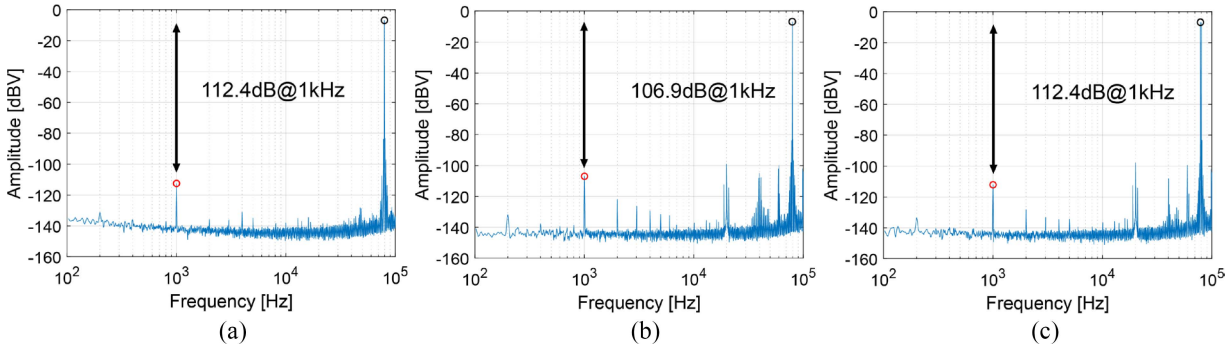

Fig. 11. Two-tone test all in a noninverting buffer configuration for (a) no chopping, (b) chopping without fill-in, and (c) chopping with fill-in.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	This work	Rooijers 2021 [1]	AD8551 [2]	AD8571 [3]	Ivanov [4]	Rooijers [5]
DOC technique(s)	**Chopping + RRL**	Chopping + AZ	AZ	AZ	Chopping + RRL	AZ + Chopping
DOC frequency (kHz)	**20**	20	4	2 to 4	50 to 150	15
Chopper-induced IMD tone (dB)	**f_{in}=79 kHz -102 (No Fill-in) -125.7 (Fill-in)**	f_{in}=79 kHz -97.7 (No Fill-in) -125.9 (Fill-in)	f_{in}=0.5 kHz -80 (Single) -	f_{in}=0.5 kHz - -90 (Spread)	f_{in}=1 kHz -103 (Single) -122.7 (Spread)	f_{in}=16 kHz -44 (Single) -
Offset (Max)	**0.8 µV**	0,8 µV	5 µV	5 µV	3.5 µV	0.6 µV
Input current (Max)	**22.6 pA**	**600 pA**	50 pA	50 pA	200 pA	1 pA (untrimmed) 0.2 pA (trimmed)
Voltage noise density (nV/√Hz)	**12**	**16**	42	51	6.5	20
Supply voltage	**5 V**	**5 V**	5 V	5 V	1.8 - 5.5 V	1.8 V
Supply current	**0.55 mA**	**0.55 mA**	0.85 mA	0.85 mA	1.65 mA	0.21 mA
Die Area (mm^2)	**1.25**	**1.25**	-	-	1.626	1.4

to [1], it achieves 25× less input current and a lower flat white noise level (12 nV/√Hz) at similar supply current levels.

IV. CONCLUSION

This letter proposes a chopper-stabilized amplifier with a relaxed implementation of the fill-in technique. It achieves a similarly low level of IMD as a previous implementation, −125.7 dB with an input frequency of 79 kHz. However, it also achieves 25× less input current, with a maximum of 22.6 pA. Finally, it achieves a flat lower noise floor of 12 nV/√Hz, while consuming the same power (2.75 mW).

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