Precision Temperature Measurement Using CMOS Substrate PNP Transistors

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***Abstract*—This paper analyzes the nonidealities of temperature sensors based on substrate pnp transistors and shows how their influence can be minimized. It focuses on temperature measurement using the difference between the base-emitter voltages of a transistor operated at two current densities. This difference is proportional to absolute temperature (PTAT). The effects of series resistance, current–gain variation, high-level injection, and the Early effect on the accuracy of this PTAT voltage are discussed. The results of measurements made on substrate pnp transistors in a standard 0.5-μm CMOS process are presented to illustrate the effects of these nonidealities. It is shown that the modeling of the PTAT voltage can be improved by taking the temperature dependency of the effective emission coefficient into account using the reverse Early effect. With this refinement, the temperature can be extracted from the measurement data with an absolute accuracy of $\pm$0.1 °C in the range of $-$50 to 130 °C.**

***Index Terms*—CMOS substrate pnp transistors, effective emission coefficient, proportional to absolute temperature (PTAT) voltage, reverse Early effect, temperature measurement.**

I. Introduction

In MOST integrated CMOS temperature sensors, a substrate bipolar transistor is used to measure temperature. When such a transistor is operated at two different emitter currents, the difference in base-emitter voltage is proportional to absolute temperature (PTAT) [1]. This PTAT voltage is, however, affected by various nonidealities. This paper gives an overview of these nonidealities and shows how their influence can be minimized. We have performed measurements on substrate pnp transistors fabricated in a standard 0.5-μm CMOS process. The results are used to show the effects of the nonidealities and the PTAT accuracy that can be obtained when they are taken into account.

Several nonidealities of the PTAT voltage in CMOS have been discussed in [2]. There, it has been shown that an accuracy of $\pm$0.1% can be obtained, which is equivalent to $\pm$0.3 °C at room temperature. This paper shows that the accuracy can be improved by taking the reverse Early effect into account. The importance of the reverse Early effect for the design of bandgap references has been pointed out in [3]. In this paper, we show its importance for PTAT temperature measurement.

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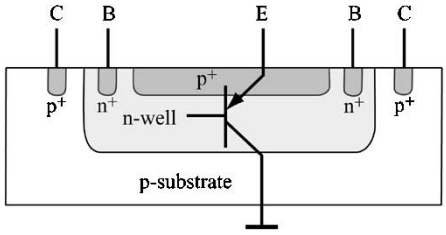

Fig. 1. Substrate pnp in n-well CMOS technology.

Specifically, we show that it leads to a temperature-dependent definition of the effective emission coefficient. Using this definition and compensating for other nonidealities, the temperature can be extracted from the measurement data with an absolute accuracy of $\pm$0.1 °C in the temperature range of $-$50 to 130 °C.

This paper is organized as follows. We first introduce the principle of PTAT temperature measurement. Then, we describe the experimental setup we have used to characterize the substrate pnp transistors. This is followed by a discussion of the various nonidealities and how their effect on PTAT temperature measurement can be reduced. This discussion is illustrated using the measurement results. The paper ends with conclusions.

II. Measurement Principle

A. Substrate Bipolar Transistors in CMOS Technology

It has been known for a long time that bipolar transistors can be used for temperature sensing. In CMOS technology, two types of bipolar transistors are available: lateral and substrate transistors. Because of their more ideal behavior and their lower sensitivity to stress [4], [1], substrate transistors are preferred for temperature sensing.

In a typical n-well CMOS process, substrate pnp transistors are formed by a p^+ drain-source diffusion in an n-well, as shown in Fig. 1. Compared to lateral transistors, these devices have two main disadvantages: their collector is formed by the substrate and is, thus, grounded, and their current gain is low, typically below 10 for modern CMOS processes. We will show that these disadvantages are not a problem for their application in temperature sensors.

B. V_{BE}-Based Temperature Measurement

The most straightforward way to use a bipolar transistor as a temperature sensor is to use its base-emitter voltage as a measure of temperature [5], [6]. If a transistor is biased in its forward active region, the relation between its collector current I_C and its

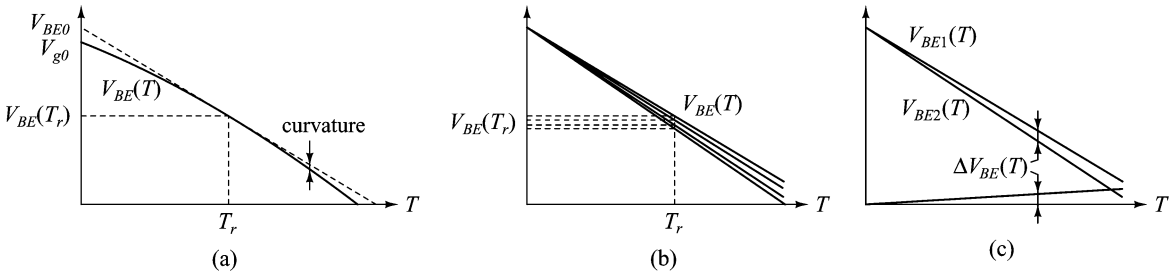

Fig. 2. (a) Temperature dependence of the base-emitter voltage $V_{\rm BE}$. (b) Variation of the sensitivity due to process spread. (c) Temperature dependence of the difference $\Delta V_{\rm BE}$ in base-emitter voltage for two collector current densities.

base-emitter voltage $V_{\rm BE}$ is given by the following well-known equation:

$$I_C(T) = I_S(T)\exp\left(\frac{qV_{\rm BE}}{kT}\right) \tag{1}$$

where k is Boltzmann's constant, q the electron charge, and I_S the saturation current of the transistor. Taking the strong temperature dependence of I_S into account, (1) can be written as

$$I_C(T) = A_E C T^{\eta}\exp\left(\frac{q(V_{\rm BE}-V_{g0})}{kT}\right) \tag{2}$$

where A_E is the emitter area, C, and η are process-dependent constants, and V_{g0} is the extrapolated bandgap voltage at 0 K [6].

Expressing $V_{\rm BE}$ as a function of I_C, we find

$$V_{\rm BE}(T) = V_{g0}\left(1-\frac{T}{T_r}\right)+\frac{T}{T_r}V_{\rm BE}(T_r) - \eta\frac{kT}{q}\ln\left(\frac{T}{T_r}\right)+\frac{kT}{q}\ln\left(\frac{I_C(T)}{I_C(T_r)}\right) \tag{3}$$

where $V_{\rm BE}(T_r)$ is the base-emitter voltage at a reference temperature T_r

$$V_{\rm BE}(T_r) = V_{g0}+\frac{kT_r}{q}\ln\left(\frac{I_C(T_r)}{A_E C T_r^{\eta}}\right). \tag{4}$$

As shown in Fig. 2(a), $V_{\rm BE}$ is an almost linear function of temperature. For most transistors, the sensitivity is about -2 mV/K. The nonlinearity, or curvature, is represented by the last two terms in (3). This curvature is a problem for accurate absolute temperature measurement, as it can result in a measurement error up to 2 °C. This mainly systematic error can be reduced, for instance, by using a temperature dependent collector current which compensates for the temperature dependence of I_S [5].

A more important problem is that $V_{\rm BE}(T_r)$, and, therefore, the sensitivity is process dependent, as illustrated in Fig. 2(b). As a result, $V_{\rm BE}(T_r)$ can spread as much as 10 mV, depending on the process [5], resulting in a 1.7% spread of the sensitivity. Therefore, every individual $V_{\rm BE}$-based temperature sensor needs to be calibrated.

C. $\Delta V_{\rm BE}$-Based Temperature Measurement

The process dependence can be largely eliminated by using the difference $\Delta V_{\rm BE}$ between the base-emitter voltages of a transistor operated at two current densities [7]. If two collector currents I_{C1} and I_{C2} are successively applied to a transistor, the difference in base-emitter voltage $\Delta V_{\rm BE}$ is

$$\Delta V_{\rm BE} = V_{\rm BE2}-V_{\rm BE1} = \frac{kT}{q}\ln\left(\frac{I_{C2}}{I_{C1}}\right). \tag{5}$$

Provided the collector-current ratio is constant, $\Delta V_{\rm BE}$ is PTAT. Moreover, it is independent of process parameters and the absolute value of the collector currents. These properties make it very suitable for use in integrated temperature sensors.

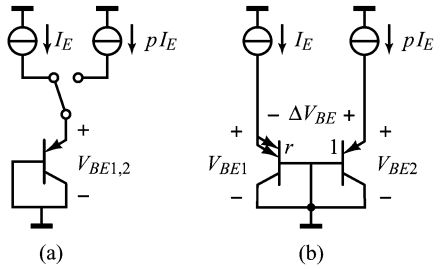

Fig. 3. Generation of $\Delta V_{\rm BE}$ using (a) a single or (b) two diode-connected substrate pnps.

As the collector of a substrate pnp is not accessible, it has to be biased via its emitter, as shown in Fig. 3(a). Assuming that the current gain is constant (this assumption will be discussed later), this results in a $\Delta V_{\rm BE}$ of $kT/q\ln(p)$, where p is the emitter current ratio. Alternatively, two transistors with an emitter area ratio of $1:r$ can be used, as shown in Fig. 3(b). In this case, $\Delta V_{\rm BE}$ is $kT/q\ln(pr)$. For proper matching, the larger transistor should consist of a parallel combination of r identical unit transistors.

For a typical value of $pr = 10$, the sensitivity of $\Delta V_{\rm BE}$ is 198 μV/K. This relatively small value means that offset cancellation techniques have to be applied in the readout circuitry. Dynamic element matching techniques can be applied to prevent mismatches between the transistors or current sources affecting the measurement [8], [1]. Assuming such measures are taken, the accuracy of $\Delta V_{\rm BE}$-based temperature measurement depends on the nonidealities of the transistor itself. They are the focus of the rest of this paper.

III. Characterization Setup

To investigate the nonidealities of substrate pnp transistors, we have measured devices fabricated in a standard 0.5 μm n-well CMOS process with a 15 $\times$ 15 μm emitter. The results presented in this paper are for one transistor and are typical for the five transistors that have been measured.

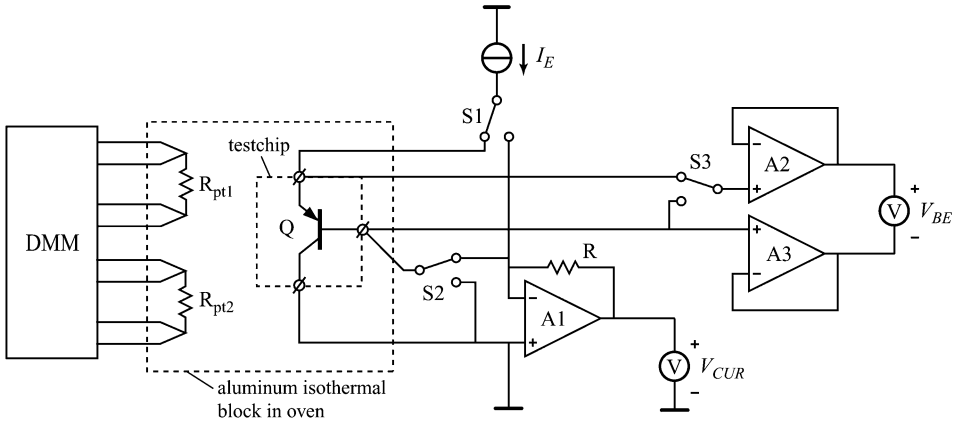

Fig. 4. Experimental setup used for characterizing substrate pnp transistors.

Fig. 4 shows the experimental setup used to characterize the transistors. A test chip with transistor Q is placed inside an aluminum isothermal block along with two platinum resistors $\mathrm{R_{pt1}}$ and $\mathrm{R_{pt2}}$. The platinum resistors are used to measure the temperature of the block and have been calibrated with an uncertainty of 20 mK. Their resistance is measured with a digital multimeter. The isothermal block is placed inside an oven.

The electronics to bias and measure the transistor are located outside the oven. A programmable current source is used to provide a test current I_E. Using switch S1, this current can be directed either to the emitter of the pnp, or to the current–voltage (I–V) converter around opamp A1. Using switch S2, the base current of Q can also be directed to the I–V converter, so that both the emitter and the base current can be measured with the same circuit. The output of the I–V converter is read out by a digital voltmeter. The offset of the I–V converter is measured by disconnecting both the current source and the base from its input.

The base and emitter voltages of the pnp are measured using sense wires and two unity-gain amplifiers around opamps A2 and A3. The difference between the buffered voltages is measured with a digital voltmeter. The offset of the amplifiers is measured by shorting their inputs using switch S3.

The opamps A1–3 are low-noise opamps with input bias currents less than 100 pA. Relays are used for the switches to avoid leakage currents. Shielded wires are used to minimize interference.

All instruments are controlled using a PC. The temperature of the oven was varied between -50 to 130 °C in steps of 20 °C. For every temperature, bias currents in the range of 0.5 to 500 μA were applied to the transistor and its base-emitter voltage and its currents were measured.

IV. Error Reduction

A ΔV_{BE} measurement with substrate pnp transistors is affected by various nonidealities, the most important of which are series resistance, current–gain variation, high-level injection, and the Early effect. These will be discussed in the following sections.

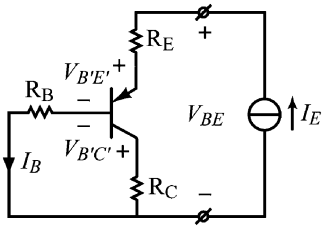

Fig. 5. Diode-connected substrate pnp with parasitic series resistances.

A. Series Resistance

Fig. 5 shows a diode-connected substrate pnp with base, emitter, and collector resistances. The voltage drop across the base and emitter resistances is added to the intrinsic base-emitter voltage $V_{B'E'}$ and results in an offset on the PTAT voltage

$$\Delta V_{\mathrm{BE}} = (I_{B2} - I_{B1})R_S + \frac{kT}{q}\ln\left(\frac{I_{C2}}{I_{C1}}\right) \tag{6}$$

where the series resistance $R_S = R_B + R_E(B_F + 1)$, where B_F is the transistor's current gain. R_S is usually dominated by the base resistance R_B. With $I_{E2} = 10$ μA, $I_{E1} = 1$ μA, and a typical current gain $B_F = 6$, the offset corresponds to 6.4 mK/Ω. With a typical base resistance of 100 Ω, this results in a 0.64 °C offset.

As pointed out in [7], the series resistance R_S can be determined by measuring V_{BE} at *three* instead of two bias currents (this technique, elaborated on in [9] and [10], is equivalent to the technique described in [2] and is a variation of the series resistance compensation technique for translinear circuits presented in [11]). This yields two equations

$$\Delta V_{\mathrm{BE21}} = (I_{B2} - I_{B1})R_S + \frac{kT}{q}\ln\left(\frac{I_{C2}}{I_{C1}}\right) \tag{7}$$

$$\Delta V_{\mathrm{BE32}} = (I_{B3} - I_{B2})R_S + \frac{kT}{q}\ln\left(\frac{I_{C3}}{I_{C2}}\right) \tag{8}$$

which can be solved for R_S and T.

We have measured V_{BE}, I_B, and I_C for various emitter currents. From the results, we have extracted the series resistance using various combinations of emitter currents, as shown in Fig. 6. The series resistance decreases with increasing emitter

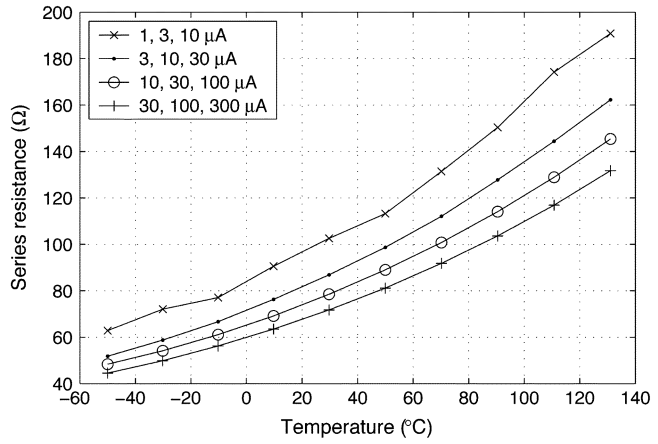

Fig. 6. Series resistance versus temperature, extracted from measurements at various emitter currents (I_{E1}, I_{E2}, I_{E3}).

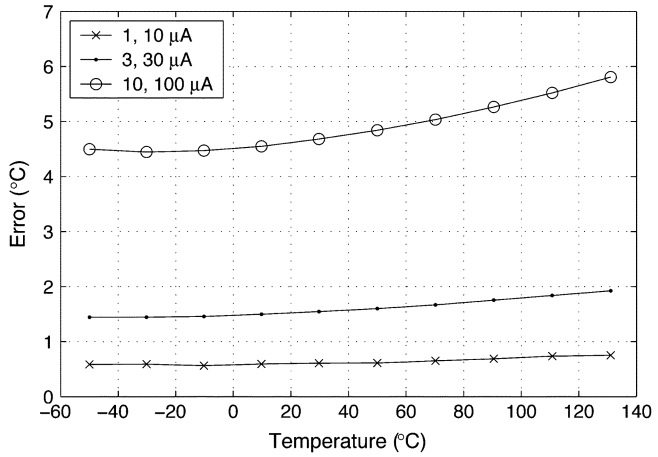

Fig. 7. Temperature error due to the voltage drop across series resistances for various combinations of emitter currents (I_{E1}, I_{E2}).

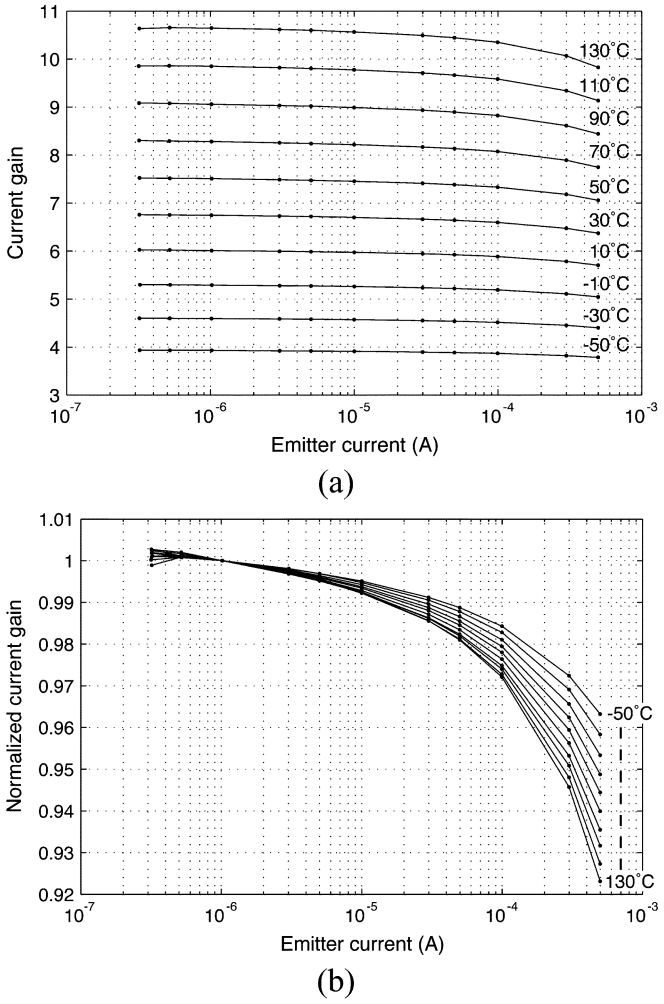

Fig. 8. (a) Measured current gain versus emitter current as a function of temperature and (b) relative to the current gain at 1 μA.

current due to the decrease of the base resistivity with the onset of high-level injection [12].

Fig. 7 shows the temperature error that corresponds to the voltage drop across the measured series resistance in a two-current measurement as described by (6). Even for currents in the microampere range, a significant error is found. There are three ways to reduce the error due to series resistance.

- Reduce the series resistance by changing the transistor's geometry (e.g., by using a fingered structure or multiple transistors in parallel).
- Reduce the bias currents. This, however, will increase the noise and susceptibility to interference.
- Compensate for the series resistance using the three-current technique described above or a similar technique [11]. Note that, for ease of implementation, it is also possible to use four currents. With $I_{C4} = 2I_{C2}$ and $I_{C3} = 2I_{C1}$, the error due to series resistance can be easily removed by taking $2\Delta V_{\mathrm{BE21}} - \Delta V_{\mathrm{BE43}}$.

The voltage drop across the collector resistance R_C changes the base-collector voltage. Because substrate pnp transistors do not have a buried layer, their collector resistance is quite large, typically a few hundred ohms. This affects the base-emitter voltage via the forward Early effect, as will be discussed below.

B. Current–Gain Variation

Fig. 8(a) shows how the large-signal current gain B_F changes with the emitter current I_E for the transistors that we have measured. The current gain increases with increasing temperature and decreases with increasing I_E.

Due to the change in B_F with I_E, the collector-current ratio will not equal the emitter-current ratio, and an error in the PTAT voltage will result

$$\begin{aligned}\Delta V_{\mathrm{BE}} &= \frac{kT}{q}\ln\left(\frac{I_{C2}}{I_{C1}}\right)\\ &= \frac{kT}{q}\ln\left(\frac{I_{E2}}{I_{E1}}\frac{B_{F2}(B_{F1}+1)}{(B_{F2}+1)B_{F1}}\right)\end{aligned} \tag{9}$$

where B_{F1} is the current gain at I_{E1}, and B_{F2} that at $I_{E2} = pI_{E1}$.

Fig. 8(b) shows the relative change in B_F with respect to B_F at 1 μA. At currents below 10 μA, B_F decreases linearly with the logarithm of I_E. This effect can be attributed to the reverse Early effect [13]. Above 10 μA, however, a much stronger decrease can be observed, resulting from the onset of high-level injection.

The temperature error caused by the resulting change in the collector-current ratio is shown in Fig. 9 for various choices of I_{E1} and I_{E2}. The error increases with the difference between the emitter currents. The error can be reduced in two ways.

- Choose the emitter currents close together in the region where the current dependency of B_F is smallest. The remaining error of -0.1 °C is almost temperature independent and can be treated as a systematic offset.
- Compensate for the base current or measure it to indirectly determine the exact collector-current ratio.

C. High-Level Injection

At high emitter-current densities, the concentration of minority carriers in the base becomes significant compared to the majority-carrier concentration. This effect is called high-level injection. With the onset of high-level injection, the slope of the $\ln(I_C)$ versus $V_{\rm BE}$ characteristic changes gradually from kT/q to $2kT/q$ [13]. In this transition region, accurate PTAT temperature measurement is not possible.

Because high-level injection also results in a decrease in the current gain, we can use the measured current gain to identify at which current level high-level injection starts. As mentioned earlier, Fig. 8 shows that this happens above 10 μA. Therefore, it is important to keep the emitter currents below that level, or to increase the emitter area if higher currents are used.

D. Early Effect

The Early effect describes the base-width modulation by the base-collector and base-emitter voltages. In the Gummel-Poon model, this is modeled by the forward Early voltage V_A and the reverse Early voltage V_B, respectively [13], [14]

$$I_C = \frac{I_S}{1 + V_{B'C'}/V_A + V_{B'E'}/V_B} \exp\left(\frac{qV_{B'E'}}{kT}\right) \tag{10}$$

which can be rewritten as

$$V_{B'E'} = \frac{kT}{q}\left\{\ln\left(\frac{I_C}{I_S}\right) + \frac{V_{B'C'}}{V_A} + \frac{V_{B'E'}}{V_B}\right\} \tag{11}$$

provided that $V_{B'C'} \ll V_A$ and $V_{B'E'} \ll V_B$. Typical values are $V_A = 100$ V, and $V_B = 10$ V. Note that for our purposes, V_B is *not* the Early voltage of the transistor operated in its inverse active region, but the Early voltage for the forward biased base-emitter junction [15]. Therefore, the reverse Early voltage available in the model parameters of a given substrate pnp may not be suitable for designing an accurate $\Delta V_{\rm BE}$ circuit.

1) Forward Early Effect: The intrinsic base-collector voltage $V_{B'C'}$ of a diode-connected transistor changes due to the voltage drop across the base resistance R_B and the collector resistance R_C (Fig. 5)

$$V_{B'C'} = (B_F R_C - R_B) I_B. \tag{12}$$

Substituting (12) in (11) gives

$$V_{B'E'} = \frac{kT}{q}\left\{\ln\left(\frac{I_C}{I_S}\right) + \frac{V_{B'E'}}{V_B}\right\} + \frac{kT}{qV_A}(B_F R_C - R_B) I_B. \tag{13}$$

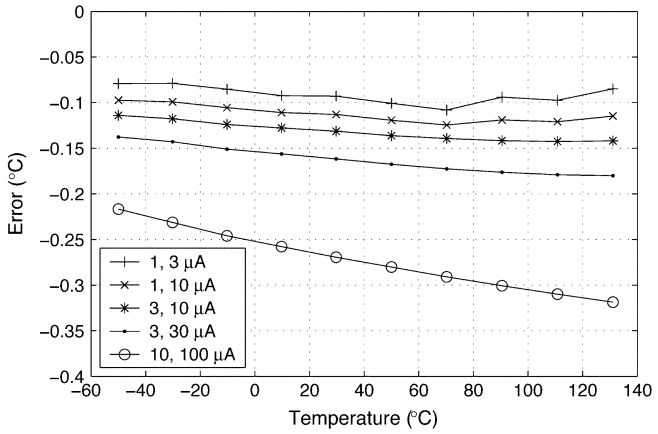

Fig. 9. Temperature error due to current–gain variation for various combinations of emitter currents.

This shows that the effect on $V_{\rm BE}$ is approximately equivalent to that of a resistor $(B_F R_C - R_B)kT/qV_A$ in series with the base. As $kT/q \ll V_A$, this effect is negligible (a typical value for the resistance is 1 Ω compared to a typical base resistance of 100 Ω). In addition, a series resistance compensation technique as described above will also compensate for this effect.

2) Reverse Early Effect: If the forward Early effect is ignored, (11) can be rewritten as

$$V_{B'E'} = \frac{kT/q}{1 - kT/qV_B} \ln\left(\frac{I_C}{I_S}\right). \tag{14}$$

Thus, a multiplicative factor

$$n = \frac{1}{1 - kT/qV_B} \tag{15}$$

is introduced in the expression for $\Delta V_{\rm BE}$

$$\Delta V_{\rm BE} = \frac{\mathbf{n}kT}{q} \ln(pr) \tag{16}$$

where pr is again the current density ratio. The factor n is usually called the effective emission coefficient or the nonideality factor. It is close to 1, but can deviate from 1 by 0.1% [2], which is equivalent to a temperature error of 0.3 °C at room temperature. Therefore, it is important to take n into account.

We will compare two ways of using the emission coefficient n. The usual way is to assume that n is a temperature-independent constant and use it as a fitting parameter to minimize the temperature error of the $\Delta V_{\rm BE}$ voltage. The temperature can then be calculated using

$$T = \frac{q}{k}\frac{\Delta V_{\rm BE}}{\ln(pr)}\frac{1}{n}. \tag{17}$$

We propose to define n according to (15), which makes it *temperature dependent* due to the presence of T in the denominator. The reverse Early voltage V_B is then assumed to be a temperature-independent constant and is used as a fitting parameter to minimize the temperature error of the PTAT voltage. In this case, the temperature can be calculated using

$$T = \frac{q}{k}\frac{\Delta V_{\rm BE}}{\ln(pr)}\frac{V_B \ln(pr)}{\Delta V_{\rm BE} + V_B \ln(pr)}. \tag{18}$$

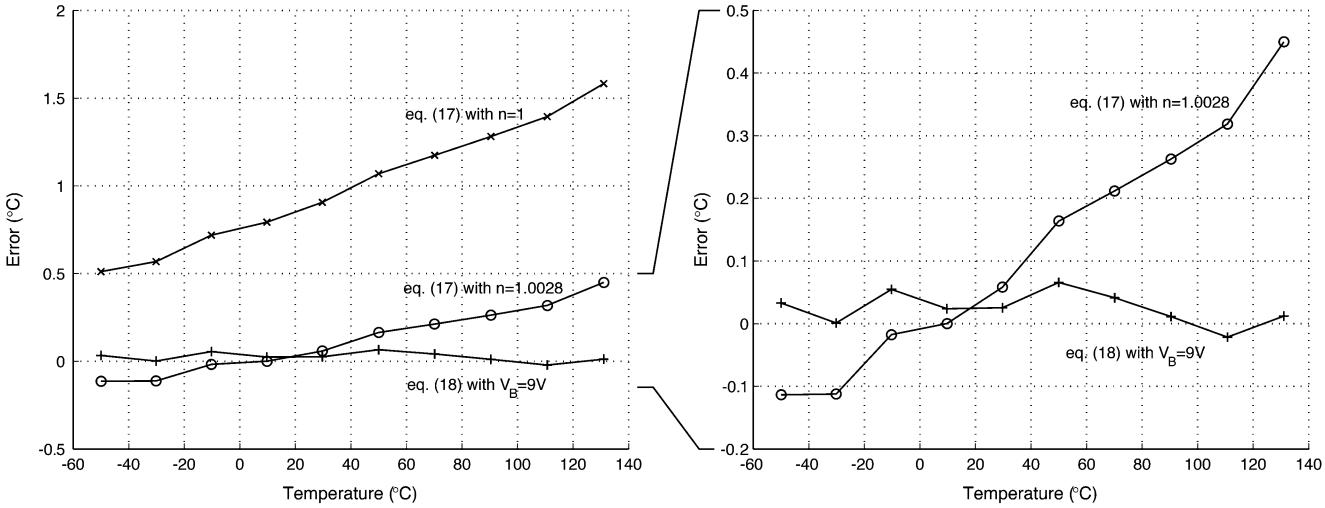

Fig. 10. Error in the temperature extracted from measurements at 1, 3, and 10 μA using a temperature-independent $n = 1$ and $n = 1.0028$, and using a temperature-dependent n with $V_B = 9$ V.

For $\Delta V_{\rm BE}/\ln(pr) \approx kT/q \ll V_B$, which is usually the case, (18) may be simplified to

$$T = \frac{q}{k}\frac{\Delta V_{\rm BE}}{\ln(pr)}\left(1 - \frac{\Delta V_{\rm BE}}{V_B \ln(pr)}\right). \tag{19}$$

To compare the two ways of using n, we extracted the temperature from our measurement data using (17) and (18). We measured the base-emitter voltage and the base current for emitter currents of 1, 3, and 10 μA. By using three currents, we compensated for series resistances. Using the measured base current, we could calculate the collector current so that the temperature extraction was not affected by current–gain variation. The emitter currents were chosen to avoid high-level injection.

Fig. 10 shows the error in the calculated temperatures for both definitions of n. The curve for $n = 1$ represents the total error due to the reverse Early effect. The curve for $n = 1.0028$ represents the error that remains due to the fact that the temperature dependence of n is not taken into account. It increases with temperature to over 0.4 °C at 130 °C. In contrast, the error in the temperature calculated using (18) with $V_B = 9$ V is less than ± 0.1 °C over the full temperature range of -50 to 130 °C.

V. Conclusion

We have presented an analysis of bipolar transistor nonidealities involved in $\Delta V_{\rm BE}$-based temperature measurement using CMOS substrate pnp transistors, and we have shown how these nonidealities can be reduced or taken into account. The most important nonidealities are series resistance, current–gain variation, high-level injection, and the Early effect.

The effect of series resistance and high-level injection can be minimized by choosing the bias currents as low as possible. This is limited by noise and interference considerations. In an integrated temperature sensor, bias currents in the order of 1 μA can be used. If higher currents are needed, the effect of series resistance can be compensated for by using three bias currents instead of two.

The current gain of substrate pnp transistors is quite flat over a wide temperature range. However, for accuracy in the order of 0.1 °C, the error due to current–gain variation needs to be taken into account. This can be done by treating this error as a systematic offset, or by measuring the emitter and base currents and compensating for it.

The forward Early effect has a negligible effect on the accuracy of the PTAT voltage. The reverse Early effect, however, has a significant effect. This can be accurately modeled by making the effective emission coefficient n a function of temperature and the reverse Early voltage V_B. This results in better accuracy over temperature than when the usual assumption is made that n is a temperature-independent constant.

By taking all the mentioned nonidealities into account, the temperature of substrate pnp in a 0.5-μm CMOS process can be extracted from measurement data with an accuracy of ± 0.1 °C in the range of -50 to 130 °C.

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