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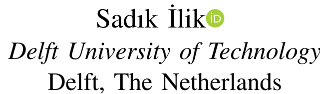
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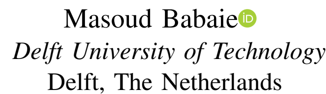
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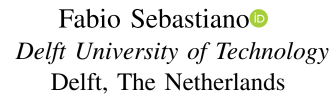
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***Abstract*—A reliable cryogenic device model is still missing despite the increasing demand for high-performance cryo-CMOS circuits. Although prior work proposed capacitance-voltage (CV) characterization to gain insights into the device cryogenic behavior, no accurate and comprehensive data is yet available. Moreover, the significant inconsistencies between the simulations using the available models and characterization data have not been investigated. To circumvent those shortcomings, this paper presents an extensive and accurate CV characterization over multiple geometries, frequencies, AC excitation voltages, and temperatures. Furthermore, we provide explanations for the observed deviations from the room-temperature characteristics and propose a model for a more accurate surface-potential calculation. Thanks to those data and the model, we can successfully simulate the CV curve of a transistor at cryogenic temperatures, which represents an essential step toward a complete cryogenic transistor model.**

***Index Terms*—Cryogenic electronics, Cryo-CMOS, quantum computing, incomplete ionization, cryogenic modeling.**

I. Introduction

Quantum computers have the potential to solve computational problems that are intractable by classical computers. However, such a promise would require quantum processors with a much larger number of qubits than are available today, thus also requiring a large-scale cryo-CMOS electrical interface. Cryogenic device models are essential for reliably designing those cryo-CMOS circuits, but they are not readily available yet [1]. Despite the availability of a cryogenic extension of the BSIM-CMG model for FinFETs [2] and some preliminary effort to adapt the EKV model [1], there is still no standard model for bulk CMOS devices at cryogenic temperatures. Among the widely adopted models for extended room temperature simulations, models based on the surface potential, such as PSP [3], are strong candidates for the implementation of the cryogenic behaviour thanks to their physics-based nature. Surface-potential models can be easily verified by using the MOS capacitance-voltage (CV) characterization thanks to their advantage of not needing extra parameters, such as mobility.

The CV behavior at cryogenic temperature is significantly different than at room temperature, as shown in Fig. 1, where a dip in the depletion capacitance (V_{GB} =−1.2 V) at 35 K and a hump in the inversion capacitance (V_{GB} = 0.45 V) at 4.2 K are visible. Identifying the physical background of these phenomena is essential to implement those effects into a scalable model. However, prior work on cryogenic CV characterization was scarce and not comprehensive.

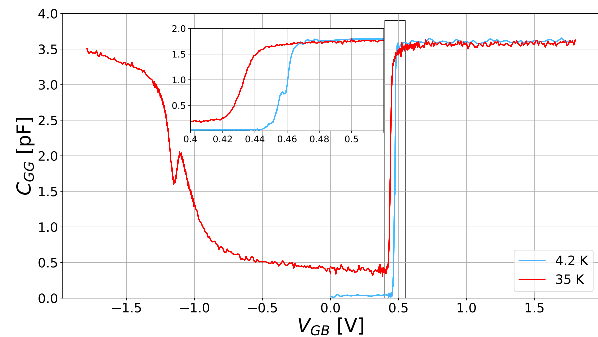

Fig. 1. CV characteristics of an NMOS (W/L=20 μm/20 μm) at 4.2 K and 35 K ($V_{DB} = V_{SB} = 0$ V).

Due to the fine features of the depletion dip and the inversion hump, measurement parameters, such as the frequency and amplitude of the AC excitation and V_{GS} voltage step sizes, strongly affect the observed behavior. The accurate control of those crucial details may have previously hindered a full understanding of either the depletion dip [4] or the inversion hump [4]–[7], or even led to missing the depletion dip completely [7], [8].

On the modeling side, there have been multiple attempts to model the surface potential and the channel charge by including incomplete ionization effects at cryogenic temperatures and using those models to simulate the CV curve. In [9], [10], the incomplete ionization model assumes a single energy value for the allowed density of states (DoS) for the dopants, modeled with a Dirac-delta function. This model predicts a bump near the flat-band voltage due to the field-effective ionization. Yet, [9] lacks measurement results to compare with the model, whereas measurements in [10] are limited to above 70 K.

To overcome those limitations, this paper investigates the effects of key experimental parameters on the CV characterization at cryogenic temperatures, including sweeping the amplitude and frequency of the AC excitation and adopting an extra fine gate-voltage sweep. For the first time, a cryogenic CV characterization over multiple device geometries and multiple samples is reported. Using such an extensive dataset,

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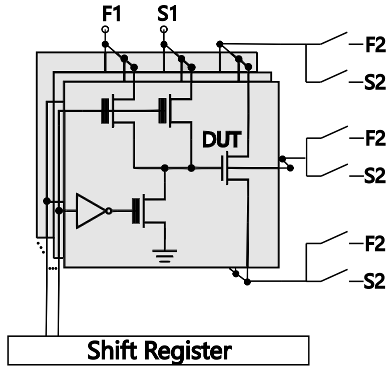

Fig. 2. Circuit diagram of the multiplexed NMOS DUTs with force (F) and sense (S) terminals connected to pads. A complementary structure is used for the PMOS.

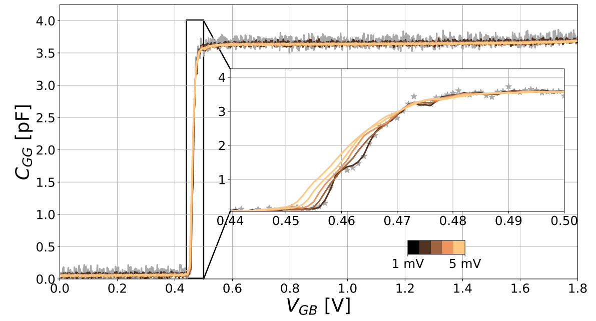

Fig. 3. Inversion capacitance of NMOS (W/L=20 μm/20 μm) at 4.2 K for different amplitudes of the 30 kHz AC excitation from 1 mVrms to 5 mVrms (solid lines, color coded) and 0.5 mVrms (gray star symbols).

this work highlights the cryogenic anomalies, discusses their origin, and proposes new models for them.

II. Test Chip and Measurement Setup

Using a 160-nm bulk CMOS technology, a multiplexed Device Under Test (DUT) structure has been designed for efficient and fast characterization of a large number of devices. A shift register addresses the gates of each DUT, while their drain, source, and bulk contacts are shared, as shown in Fig. 2. To minimize parallel leakage in highly populated configurations, DUTs are grouped into three groups, reducing the leakage associated with shared terminals. The selected DUT's gate is connected to the pads, while the remaining DUT gates are held at 0 V for NMOS or 1.8 V for PMOS. Each DUT is electrically isolated using a deep n-well and a guard ring for NMOS, or a p-well and a guard ring for PMOS. 3.3 V thick-oxide MOS devices are used for the switches to enable reliable operation for DUT drain/source voltage up to the thin-oxide nominal supply (1.8 V). Each of the DUT's terminals has been connected to a pair of force/sense pads for four-point measurements of the CV characteristics using the Keysight E4980A LCR meter. Other switches (not shown) are connected to the pads for additional tests but are left unused in the measurements described below.

For inversion-capacitance (depletion-capacitance) measurements of NMOS (PMOS) DUTs, the gate voltage is swept from 0 V to 1.8 V with 1 mV steps while keeping the drain, source, and bulk grounded. To measure the depletion-capacitance (inversion-capacitance) of NMOS (PMOS) DUTs, the drain, source, and bulk are swept from 0 V to 1.8 V with the same step size while holding the gate at 0 V. This approach allows for a full gate capacitance spectrum from -1.8 V to 1.8 V without requiring negative voltage biasing, which is not allowed for the designed structure. Because of the cryogenic effects in the bulk, the depletion capacitance cannot be accurately measured at deep cryogenic temperatures, i.e., below $\approx$ 30 K. At 4.2 K, only the inversion capacitances ($V_{GS} > 0$ V for NMOS, $V_{GS} < 0$ V for PMOS) are then reported.

For the cryogenic characterization, the chips are bonded to a ceramic dual-in-line package (DIP) and mounted on a PCB. The PCB is then placed on a dipstick equipped with a Lake Shore DT-670 silicon diode cryogenic temperature sensor and submerged in liquid helium for measuring at 4.2 K. To conduct measurements at elevated temperatures between 4.2 K and 300 K, the dipstick is raised above the liquid helium surface and kept in the helium vapor.

III. Results and Discussion

A. Inversion Mode

To highlight the need for a small amplitude of the AC excitation, Fig. 3 shows clear bumps for small AC voltages, which disappear for larger excitation amplitudes. This is attributed to more charge contributors, either traps or dopants, contributing for larger AC swings, thus resulting in higher capacitance. The higher number of charge states also averages out and masks single contributions. Since the 0.5 mVrms curve overlaps with the 1 mVrms one in the region of interest, V_{AC} is set to 1 mVrms for the rest of the paper, unless otherwise mentioned, for a better measurement sensitivity.

The dependence of gate capacitance on device geometry is explored in Fig. 4. While the largest device (W/L=20 μm/20 μm) is measured individually, eight identical smaller devices are connected in parallel to circumvent the limited measurement sensitivity. The transition from depletion to strong inversion has a steeper slope for NMOS compared to PMOS. Also, while all devices in Fig. 4 b),d),f), and h) have the same area, shorter devices tend to have steeper transitions and less variation with frequency. The frequency-dependent shift is clearly visible for the largest devices (Fig. 4,c-g). Successive measurements corroborated the repeatability of this behavior. Device-to-device variations of this behavior are investigated in Fig. 5.

The dependence with frequency is explained considering that a charge contributor affects the CV behavior only if its time constant is smaller than the AC excitation period ($\tau < 1/f_{AC}$) and if it falls within the range covered by the AC swing for a given V_G bias. Each device shows a unique

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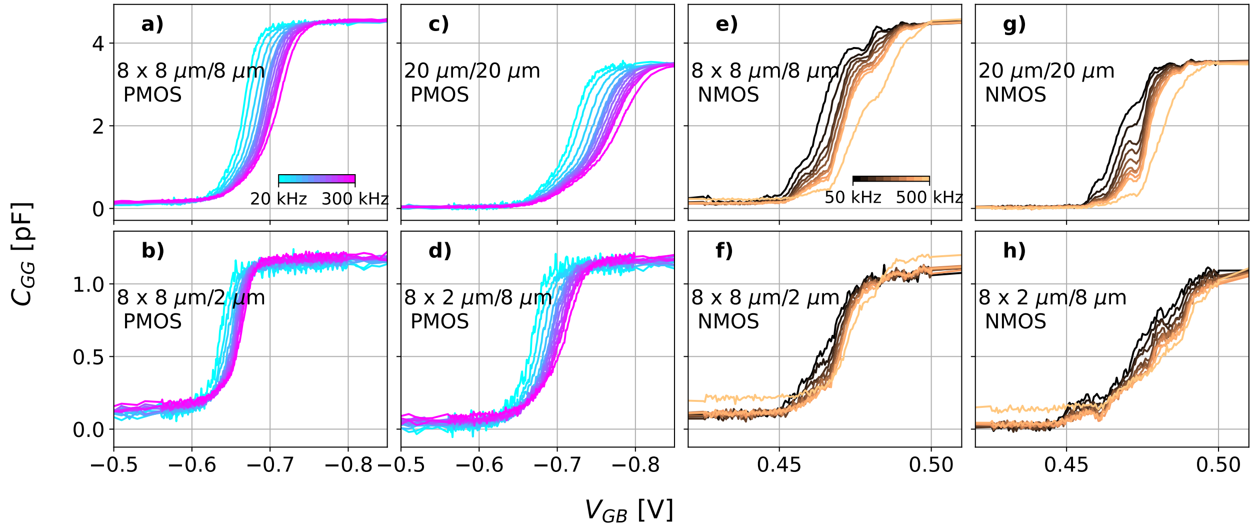

Fig. 4. Inversion capacitance at 4.2 K for PMOS (a, b, c, d) and NMOS (e, f, g, h) devices with varying geometries. In a, b, d, e, f, and h, 8 equal devices are measured in parallel.

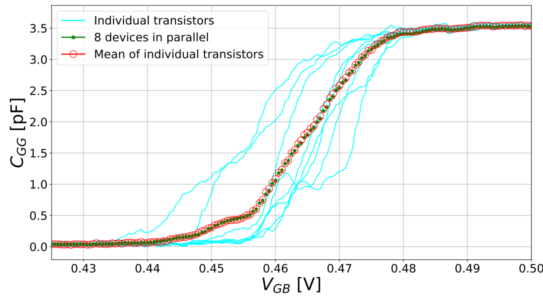

Fig. 5. Device-to-device capacitance variations for 8 identical NMOS (W/L=20μm/20μm) at 50 kHz and 4.2 K.

signature (Fig. 5) due to its unique trap/dopant configuration. Moreover, fewer traps can contribute for higher frequency, thus causing the signature shift. At cryogenic temperatures, traps in the insulator tend to be slow due to the tunneling energy barrier. Although further investigations may be required, we suggest band-tail states and extra energy states created by dopant atoms in the structure as the origin of those charge contributors [11], [12].

B. Depletion Mode

The depletion capacitance in Fig. 6 shows a clear dip at around ± 1.15 V for both PMOS and NMOS independently from the choice of the individual device, with capacitances decreasing for an increasing frequency for NMOS, similar to [8]. The difference between NMOS and PMOS devices can be attributed to their different doping profiles.

While prior works manage to attribute the CV dip to field-dependent ionization at the flat-band voltage [4], [9], [10], they fail to predict the depth of the dip, which is expected to be more pronounced than the ones shown in Fig. 6 and also in [13]. In such a model, the ionized dopant concentration can be expressed as

$$N_A^- = \int_{E_V}^{E_C} \frac{N_A}{1 + g_A e^{\frac{E-E_f}{U_T}}} f(E) dE \tag{1}$$

where E_C is the conduction-band energy, E_V the valence-band energy, g_A the degeneracy factor, E_f the Fermi energy, $U_T = kT$ with k the Boltzmann constant, T the absolute temperature, and $f(E)$ is the allowed DoS for dopants. In widely used models [1], $f(E)$ is expressed as a single state at energy level E_A, i.e., $f(E) = \delta(E - E_A)$, resulting in

$$N_A^- = \frac{N_A}{1 + g_A e^{\frac{E_A - E_{F,n}}{U_T}}} \tag{2}$$

However, a more physical approach would require a Gaussian-shaped distribution [14], i.e., $f(E) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(E-E_A)^2}{2\sigma^2}}$ where σ is the standard deviation of the DoS. As shown in the inset of Fig. 7, Gaussian and Dirac-delta approaches overlap well at high temperatures. However, while the model in (2) turns into a step function that predicts a more abrupt shift from freeze-out to ionization for lower temperatures, the model with Gaussian-shaped energy states saturates and does not fully turn into a step function.

Although the model with a Gaussian-shaped energy state is more physically accurate, it is computationally expensive and not suitable for use in compact models. So, an approximation that can predict the saturation effect observed in Fig. 7 and still is computationally efficient is needed. To achieve this, we propose the use of the rectangular-shaped distribution $f(E) = \{u(E - E_a + \Delta/2) - u(E - E_a - \Delta/2)\}/\Delta$ with $u(\cdot)$ the step function and Δ the energy width of the distribution that models the effect of σ in the Gaussian DoS. Using this approach, we get

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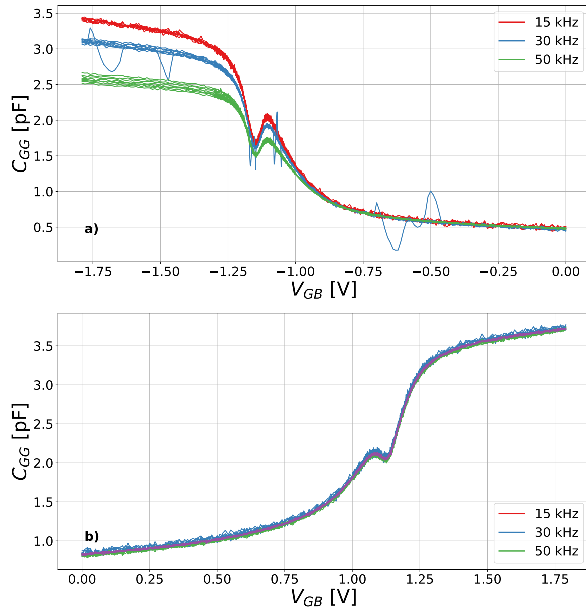

Fig. 6. Depletion capacitance of 8 identical devices with W/L=$20\mu m/20\mu m$ while V_{AC} = 2 mVrms, at 35 K, and various frequencies a) NMOS, b) PMOS.

$$\frac{N_A^-}{N_A} = 1 - \frac{U_T}{\Delta} \ln \frac{1 + g_A e^{\frac{E_f + E_a + \Delta/2}{U_T}}}{1 + g_A e^{\frac{E_f + E_a - \Delta/2}{U_T}}} \quad (3)$$

Both models with the Dirac-delta and the proposed rectangular-shaped energy states are compared with the measurement results in Fig. 7. PSP-based surface potential calculations, as in the [15], are used for the CV simulation, although the model can be adapted to other models, such as EKV. It is shown that, with increasing Δ values, the bump gets shallower and achieves a better prediction of the measured behavior. Due to the lack of information about the exact shape of the DoS, the Δ can also be used for fine-tuning the bump. The best fit is for Δ =50 meV, which is comparable to the experimentally extracted Gaussian distribution's σ value in [14]. These results can support a more accurate follow-up modeling of the CV behavior, which is essential for later steps in the modeling.

IV. Conclusions

This paper presents extensive CV characterization at cryogenic temperatures and proposes a model explaining its behavior. The effect of the frequency and amplitude of the AC excitation on the CV characteristics is investigated, as well as its dependence on device geometry. Device-to-device variations are analyzed, and a possible mechanism is proposed to explain the observed effects. Furthermore, the depletion-capacitance measurements at 35 K are used to build an alternative incomplete ionization model. The proposed model predicts the capacitance behavior near the flatband region more accurately while still being computationally cost-effective, thus representing the basis for a future cryo-CMOS compact model.

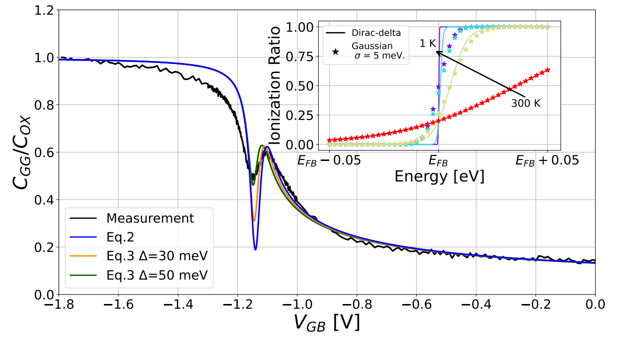

Fig. 7. Comparison between the depletion-capacitance experimental characterization and the models using the Dirac-delta-shaped energy states or the proposed model. In the inset, the Gaussian and Dirac-delta models are compared in terms of predicted ionization ratio over temperature as a function of Fermi level. E_{FB} is the Fermi level at the flatband condition.

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