

Document Version

Final published version

Licence

Dutch Copyright Act (Article 25fa)

Citation (APA)

Ma, H., Zhang, H., & Fan, Q. (2026). A -82.3dB THD+N 60V Fully Integrated Shunt-Resistor-Based In-Line Current Sensor with DLL-Assisted Dynamic Body-Biasing Technique. In *2026 IEEE International Solid-State Circuits Conference, ISSCC 2026* (pp. 380-382). (Digest of Technical Papers - IEEE International Solid-State Circuits Conference; Vol. 69). IEEE. <https://doi.org/10.1109/ISSCC49663.2026.11409178>

Important note

To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Copyright

In case the licence states "Dutch Copyright Act (Article 25fa)", this publication was made available Green Open Access via the TU Delft Institutional Repository pursuant to Dutch Copyright Act (Article 25fa, the Taverne amendment). This provision does not affect copyright ownership.
Unless copyright is transferred by contract or statute, it remains with the copyright holder.

Sharing and reuse

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

Takedown policy

Please contact us and provide details if you believe this document breaches copyrights.
We will remove access to the work immediately and investigate your claim.

21.9 A -82.3dB THD+N 60V Fully Integrated Shunt-Resistor-Based In-Line Current Sensor with DLL-Assisted Dynamic Body-Biasing Technique

Heng Ma, Huajun Zhang, Qinwen Fan

TU Delft, Delft, The Netherlands

Abstract

Floating- G_m -based current sensors are effective in rejecting PWM common-mode voltage. But their linearity drops at high voltages due to substrate-current-induced body effect in LDMOS devices. To address this issue, this work introduces a DLL-assisted dynamic body biasing sensor in 0.18 μ m BCD, improving HD2 by 31dB and THD+N by 14dB. And a peak

THD+N of -82.3dB is achieved in the meanwhile. It supports 60V common-mode, rejects PWM up to 2MHz, and enables high-linearity sensing for high power audio and motor-driver systems.

High-linearity current sensors are essential for high-performance audio systems and precision motor drivers, etc. In particular, in-line shunt-resistor-based current sensors are gaining popularity due to their potentially high linearity [1]. To achieve high power efficiency, such systems often rely on switched power stages—e.g., power inverters or Class-D amplifiers—, controlled by pulse-width-modulated (PWM) signals to drive the load. The inline current sensor, placed between the power stage and the load, is then directly exposed to fast, high-voltage (HV), common-mode (CM) PWM pulses at the output of the power stages, which can induce severe glitches at the sensor output and significantly degrade linearity [2]. To mitigate this issue, a floating G_m stage can be used to effectively reject the HV fast PWM voltage [3,4], followed by an HV LDMOS buffer stage that transfers the signal from the floating voltage domain to the low-voltage (LV) domain. High linearity together with PWM rejection up to 2MHz was demonstrated in [3], but its low input voltage range (14.4V) makes it incompatible with many switching systems that operate under the increasingly common 48V supply standard and above [2]. Increasing the PWM voltage will lead to higher V_{DS} stress on the LDMOS transistors, which can cause severe body leakage current—a phenomenon known as substrate current-induced body effect (SCBE) shown in Fig. 21.9.1 top [5]. This can, surprisingly, but significantly increase the second-order harmonic distortion (HD2). To mitigate this, a DLL-assisted dynamic-body-biasing (DBB) technique is proposed, which yields up to 31dB improvement in HD2 and 14dB improvement in THD+N. Implemented in a 180nm BCD process, the proposed current sensor achieves a peak THD+N of -82.3dB with a 4A, 1kHz input signal, while rejecting HV PWM signal up to at least 2MHz. It offers a 60V input voltage range with a DC CMR of 132dB, while consuming 1.7mA current.

The proposed inline current sensor is shown in Fig. 21.9.1 bottom, which consists of an on-chip shunt resistor R_S , a floating G_m (FG_m) stage powered by the bootstrap voltage V_{BST} (commonly available in high-power switching amplifiers for high-side gate driving), an HV LDMOS current buffer ($M_{D1,2}$), and an LV (5V) transimpedance amplifier (TIA) built around A1. 70V LDMOS are chosen to allow 60V input CM range with extra safe margin. A resistor thermal compensation scheme is employed to mitigate nonlinearity due to R_S self-heating [3]. A DLL-assisted timing generator monitors the PWM voltage V_{SW} and generates control signals for the DBB circuit, which dynamically adjusts the LDMOS body voltage during V_{SW} transitions, effectively suppressing SCBE-induced distortion.

Figure 21.9.2 illustrates the proposed DBB scheme and compares it with conventional approaches. Conventionally, the body of $M_{D1,2}$ is either connected to the supply FVDD (BTF) or to its own source (BTS). In the former configuration (Fig. 21.9.2 top-left), where FVDD is 5V above V_{SW} , a body current I_{SCBE} is generated due to SCBE, which is dependent on V_{DS} : the higher V_{DS} , the higher I_{SCBE} . Since V_{DS} changes with V_{SW} , which is a PWM-modulated version of I_{SIG} , I_{SCBE} becomes signal dependent. At first glance, this appears to be a CM error. However, I_{SCBE} also depends on I_{SIG} directly, due to the fact that higher I_{SIG} induces more impact ionization—the origin of I_{SCBE} [5]. Consequently, I_{SCBE} contains a differential component proportional to $\sim I_{SIG}^2$, which can result in an HD2 distortion ~ 67 dB with a 4A current in this design. In the BTS configuration (Fig. 21.9.2, top-middle), I_{SCBE} would circulate inside the LDMOS, leaving the drain current undistorted. However, HV LDMOS devices are typically fabricated directly on the substrate (in non-SOI processes) without an additional isolation well, resulting in a parasitic body-to-substrate capacitance C_p . During high slew rate PWM transitions, the C_p charging and discharging current I_{LEAK} (up to mA_p level) can lead to large voltage glitches on V_{CAS} (Fig. 21.9.1 bottom) and can drive the circuit shortly into a nonlinearity region and degrade performance. This effect becomes more severe with increasing PWM frequency (f_{PWM}): a trend that has become prevalent in many switching power systems to reduce system bulk.

To address the limitations discussed above, DBB is proposed, which combines BTS with a body-to-source buffer (BTB) path and is shown in Fig. 21.9.2 bottom with its control timing diagram. When V_{SW} is high, the BTS path is selected, preventing additional I_{SCBE} from being injected into the drain. During the PWM transitions, the body is switched to the BTB path, which allows I_{LEAK} to be sourced from V_{S_BUF} , where V_{S_BUF} is a buffered version of the source voltage. The source buffer is implemented using a floating Class-AB source follower to ensure fast settling during PWM transients. Native NMOS devices are used to reduce the voltage difference between V_S and V_{S_BUF} , allowing smooth switching transition and

preventing additional glitches on V_{CAS} . It should be noted that while it is crucial to stay in BTS configuration during V_{SW} is high to minimize I_{SCBE} injection into the drain, it is much less of an issue when V_{SW} is low, as I_{SCBE} is significantly lower. As a result, a BTB configuration is chosen when V_{SW} is low for simplicity in control as shown in Fig. 21.9.2 bottom-right. Simulations in Fig. 21.9.2 top-right show that with a 48V, 2MHz PWM signal under a slew rate ranging between 1 and 10V/ns, the proposed DBB can effectively reduce the V_{CAS} glitch from up to 2.3V to 0.5V compared to BTS.

To realize the proposed DBB operation, the control signal ϕ_0 (Fig. 21.9.2 bottom-right) must switch on immediately after the rising edge and shortly before the falling edge of the V_{SW} , so that BTS is active as long as possible when V_{SW} is high, while BTB is immediately active before each PWM switching. The former switching operation can be realized by timing the V_{SW} rising edge using an inverter buffer; the latter switching operation, however, requires the knowledge of the incoming V_{SW} falling edge in advance, which can be tricky for standalone current sensors since the internal PWM clocks of the switching power stage may not be accessible. To solve this issue, a DLL-based timing generator is employed to predict the PWM falling edge, which is shown in Fig. 21.9.3. The input V_{SW} is first attenuated by a 1/11 voltage divider to limit its swing within 5V. A hysteresis digital buffer then reshapes the PWM waveform and suppresses ringing due to parasitic inductance and high di/dt during transients, producing a clean digital signal DIN as the DLL input. The DLL consists of a phase-frequency detector (PFD), a charge pump (CP), a filter capacitor C_{FILT} , a voltage-controlled delay line (VCDL), and fixed delay cells t_{DELAY} . The PFD compares DIN with the feedback signal DFB, and the resulting phase error is integrated by the CP and C_{FILT} . Once locked, DIN and DFB are phase-aligned and the intermediate node DOUT, located before the fixed delay cell, leads DIN by a constant delay t_{DELAY} . Finally, by logically combining DOUT and a delayed version of DIN (DIN_{DELAY}) using an AND gate, the body control signal ϕ_0 is generated. t_{DELAY} should be long enough to ensure the LDMOS switch to BTB before the falling edge of V_{SW} , while tolerating slow rate variations of V_{SW} and phase errors due to the finite DLL bandwidth. However, a long t_{DELAY} will shorten the BTS duration when V_{SW} is high, producing un-negligible I_{SCBE} and HD2. This effect becomes more pronounced at higher PWM frequencies f_{PWM} , since a shorter PWM period makes t_{DELAY} contribute proportionally more I_{SCBE} . To minimize phase-lock error such that a shorter t_{DELAY} can be allowed especially for higher f_{PWM} , the DLL bandwidth is set as high as possible to extend the gain at the current signal frequency (f_{SIG}), but is still kept $< 0.1 \cdot f_{PWM}$ for stability [6]. Finally, t_{DELAY} is chosen to be ~ 50 ns to accommodate a range of V_{SW} slew rate (> 1 V/ns) and f_{PWM} (384kHz to 2MHz) such that the proposed current sensor is compatible with a wide range of commercial Class-D audio amplifiers. Figure 21.9.3 bottom presents measured results at $f_{PWM} = 38 \cdot f_{SIG}$ and $200 \cdot f_{SIG}$, respectively, where f_{SIG} is 10kHz and the current amplitude is 4A. In both cases, the ϕ_0 falling edge is successfully locked to lead DIN by t_{DELAY} . It's worth noting that the proposed scheme can also be applied to other use cases with different f_{SIG} and f_{PWM} ranges as long as $f_{PWM} \gg f_{SIG}$, which is often the case.

The sensor was fabricated in a standard 0.18 μ m BCD process and occupies an area of 2mm² (Fig. 21.9.7). It is measured with a commercial Class-D audio amplifier TAS6684, which allows a wide range of internal f_{PWM} (384kHz to 2MHz) to demonstrate the versatility of the proposed design, but its maximum supply voltage (48V) and unadjustable slew rate also limit the setup. Figure 21.9.4 top-left shows the measured spectrum of V_{OUT} under a 4A, 1kHz input current and 1MHz f_{PWM} . Compared to BTB where I_{SCBE} is added to I_{SIG} similar to BTF, the proposed DBB improves HD2 by 27dB. The measured HD2 with 1kHz signal frequency versus signal amplitude (6mA to 6A) is shown in Fig. 21.9.4 top-middle and the HD2 with 4A signal amplitude versus signal frequency (20Hz to 10kHz) is shown in Fig. 21.9.4 top-right, both demonstrating significant HD2 improvements using DBB. V_{OUT} spectrum with 4A, 1kHz signal current is measured with various f_{PWM} (384kHz to 2MHz) and is shown in Fig. 21.9.4 left-bottom, proving the robustness and versatility of the proposed DBB. THD+N with 1kHz signal frequency versus signal amplitude and with 4A signal amplitude versus signal frequency are shown in Fig. 21.9.4 bottom-middle and right, demonstrating 14dB improvement with DBB. Figure 21.9.5 top-left shows that the measured THD+N versus signal amplitude of 3 samples varies only by < 2 dB. Figure 21.9.5 bottom-left illustrates the improved THD+N with a 4A, 1kHz signal varies negligibly over temperatures (-40°C to 85°C), using DBB. Figure 21.9.5 top-right shows the transient response of V_{OUT} under a 2MHz, 48V V_{SW} . It can be seen that DBB effectively reduces the

PWM switching glitches compared to BTS. The difference is expected to be more significant if a higher slew-rate power stage is used. Figure 21.9.5 bottom-right shows the measured DC CMR of the current sensor, demonstrating a 0V-to-60V input CM operating range and a 132dB CMR.

Figure 21.9.6 summarizes the sensor performance and compares it to state-of-the-art designs. Compared to [3], the proposed design extends the supply voltage capability from 14.4V to 60V while maintaining similar PWM rejection frequency and THD+N. Compared to other prior works with >40V input range, it achieves at least 16dB better THD+N, 16× higher PWM rejection frequency and 10dB higher DR, while consuming comparable current.

References:

- [1] M. Mauereer et al., "Voltage/current measurement performance and power supply rejection in all-digital Class-D power amplifiers," *IECON*, pp. 666-673, Oct. 2016. <http://doi.org/10.1109/IECON.2016.7793041>
- [2] Texas Instruments, *INA253 High Voltage, Bidirectional, Zero-Drift, Current-Shunt Monitor with Integrated, 2-mΩ, Precision, Low Inductive Shunt Resistor*, [Online]. Available: <https://www.ti.com/product/INA253>. <https://www.ti.com/product/INA253>
- [3] H. Ma et al., "A -87.2 dB THD+N 89.1 dB DR Fully-Integrated Shunt-Resistor-Based In-Line Current Sensor with up to 2 MHz 14.4 V PWM Rejection," *IEEE Symp. VLSI Circuits*, pp. 1-2, June 2025. <http://doi.org/10.23919/VLSITechnologyandCirc65189.2025.11075038>
- [4] C. Larsen et al., "High Common Mode Rejection Ratio (CMRR) Current Monitoring Circuit Using Floating Supplies," U.S. Patent US11296666B1, Apr. 2022. <https://patents.google.com/patent/US11296666B1>
- [5] S. Salahuddin et al., *BSIM4 4.8.3 MOSFET Model User's Manual*, [Online]. Available: <https://bsim.berkeley.edu/models/bsim4/>. <https://bsim.berkeley.edu/models/bsim4/>
- [6] B. Razavi, "The Delay-Locked Loop [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 10, no. 3, pp. 9-15, Aug. 2018. <http://doi.org/10.1109/MSSC.2018.2844615>
- [7] V. Binet et al., "A Fully Integrated Class-D Amplifier in 40nm CMOS with Dynamic Cascode Bias and Load Current Sensing," *ESSCIRC*, pp. 319-322, Sep. 2014. <http://doi.org/10.1109/ESSCIRC.2014.6942086>

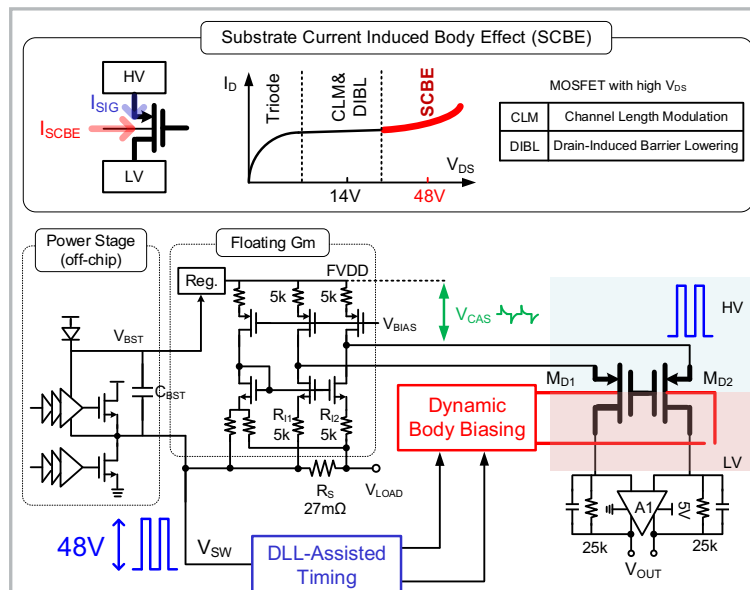


Figure 21.9.1: LDMOS's Substrate-Current-Induced Body Effect (top), and the proposed current sensor with DLL-assisted dynamic body-biasing technique (bottom).

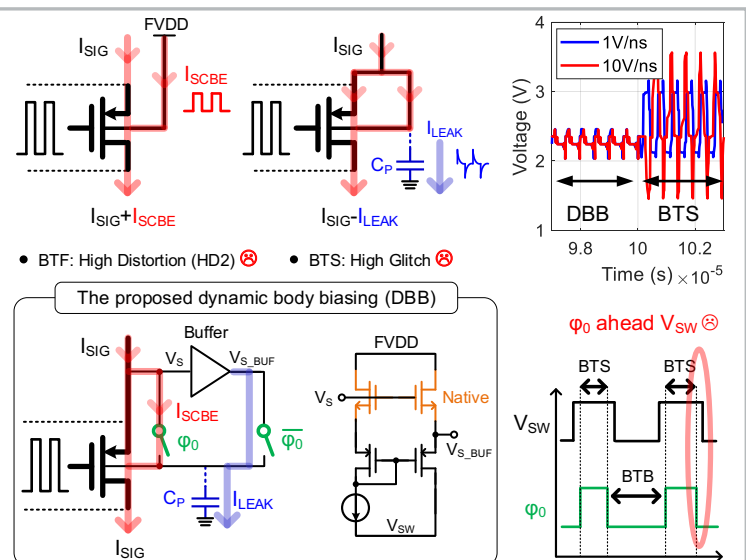


Figure 21.9.2: Different body biasing schemes: BTF (top-left); BTS (top-middle); the simulated V_{CAS} glitch (top-right); the proposed DBB (bottom-left); and its control timing (bottom-right).

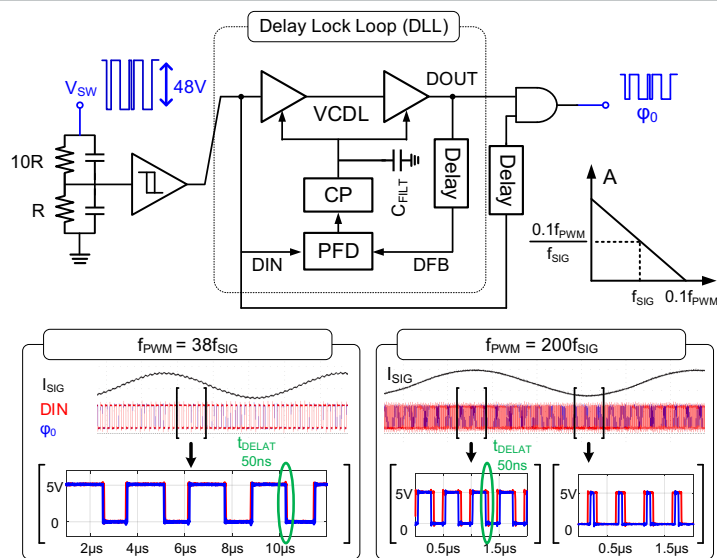


Figure 21.9.3: The proposed DLL-assisted timing control block (top), and the measured transient waveform under different PWM frequencies and different pulse duty cycles (bottom).

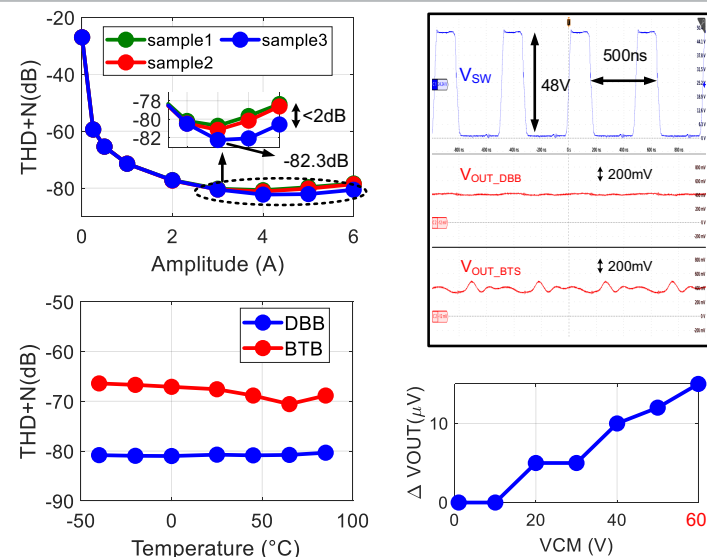


Figure 21.9.5: Measured THD+N with different samples (top-left) and temperatures (bottom-left); the transient waveform with DBB versus BTS (top-right); measured CMR (bottom-right).

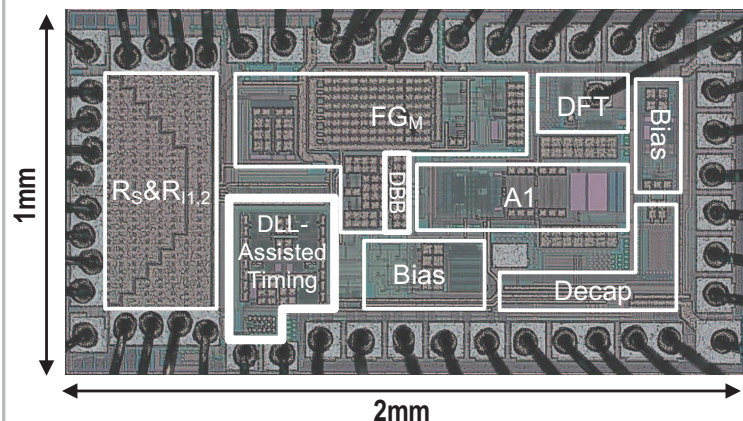


Figure 21.9.7: Die micrograph.

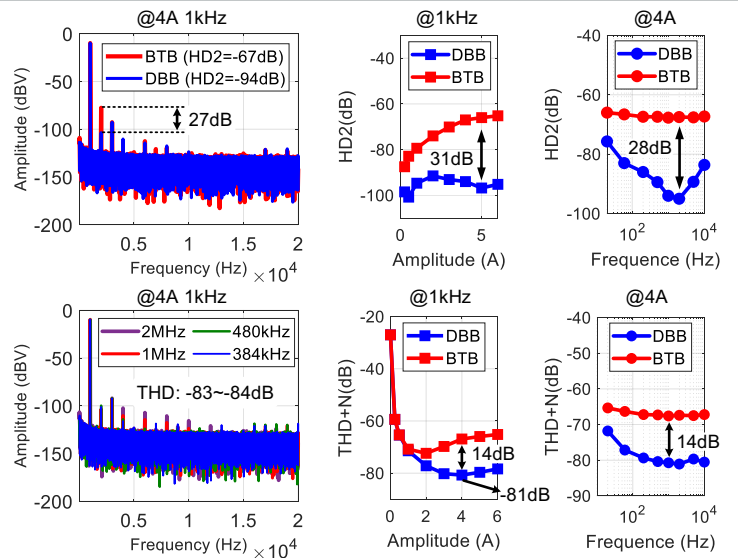


Figure 21.9.4: Measured output spectrum (top-left); measured THD with various f_{PWM} (bottom-left); measured HD2 and THD+N versus current amplitude and frequency (middle and right).

	This work	INA253	INA241	VLSI'25 [3]	MAX98388	ESSCIRC'14 [7]
Fully Integrated?	Yes	Yes	No	Yes	Yes	Yes
In-line sensing?	Yes	Yes	Yes	Yes	/	No
Input CM voltage	60V	80V	110V	14.4V	10V	5V
PWM rejection frequency	2MHz	/	125kHz	2MHz	/	/
Peak THD+N @1kHz	-82.3dB	-66.4dB ^{1,2}	/	-83.1dB	-63dB ¹	-58dB ¹
DR ³	A: 87dB Un: 84.5dB	/	/	89.1dB 86.9dB	/	77.5dB
Current Consumption	1.7mA	1.8mA	2.5mA	1.2mA	/	0.8mA ¹
Current Range	±6A	±15A ⁴	/	±6A	±3A	±0.5A ¹

¹Estimated from data/graph

²Measured at 90% full scale

³A-weighted (A) or unweighted (un)

⁴DC current

Figure 21.9.6: Comparison to the state-of-the-art current sensors for switched power systems.