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***Abstract*—Resistive Random-Access Memories (ReRAMs) represent a promising candidate to complement and/or replace CMOS-based memories used in several emerging applications. Despite all the advantages of using these novel memories, mainly due to the memristive device's CMOS manufacturing process compatibility, zero standby power consumption, as well as, high scalability and density, the use of them in real applications depends on being able to guarantee their quality after manufacturing. As observed in CMOS-based memories, ReRAMs are also susceptible to manufacturing deviations, defects, and process variations, that can cause faulty behaviors different from the ones observed in CMOS technology, increasing not only the manufacturing test complexity but also the time required to perform the test. In this context, this paper proposes to study the use of temperature to facilitate fault propagation in ReRAMs, reducing the required test time. A case study composed of a 3x3 word-based ReRAM with peripheral circuitry implemented based on a 130 nm Predictive Technology Model (PTM) library was adopted. During the proposed study, a total of 17 defects were injected in different positions of the ReRAM cell, and their respective faulty behavior was classified into traditional and unique faults, considering three temperatures (25, 100, and -40°C). The obtained results show that the temperature can, depending on the position of the defect, facilitate fault propagation, which reduces the time required for performing manufacturing testing.**

***Index Terms*—ReRAMs, Manufacturing Testing, Unique Faults.**

I. Introduction

As technology nodes reach sizes close to that of atoms, miniaturization of Integrated Circuits (ICs) has become challenging. With the parallel increasing demand for emerging applications requiring high-performance with rigid area and power consumption constraints, significant challenges arise for device technology and computer architecture [1]. Reliability, leakage, and cost represent the device technology walls that need to be addressed [1]. In addition, memory, power, and Instruction Level Parallelism (ILP) walls affect computer architectures, posing limits to von Neumann architecture [1]. In this scenario, memristive devices represent one of the most promising candidates to complement and/or replace CMOS technology in certain applications, such as Flash memories, mainly due to their CMOS manufacturing process compatibility, zero standby power consumption, as well as high scalability and density [1, 2]. Another important factor is that beyond memory these devices can be used also as computing elements [1]. When adopted as memory elements, a block composed of memristive devices is named Resistive Random-Access Memory (ReRAM), a non-volatile memory [3]. Nevertheless, the use of these emerging memories depends on being able to guarantee their quality after manufacturing as well as reliability during their lifetime. Despite the lack of information regarding realistic manufacturing deviations, literature already describes that ReRAMs can be affected by unique faults [4–6], demanding the development of new manufacturing test procedures [7, 8]. In [9], the authors provide a review of the memristive device manufacturing process and a discussion related to possible defects that may affect these novel devices, identifying the relation between manufacturing defects and faulty behaviors. In the last few years, some new manufacturing test strategies for ReRAMs were proposed in literature [10, 11], since traditional March Tests, which explore the execution of predefined read and write operations applied at each memory cell, are extremely time-consuming and moreover not able to guarantee the detection of all unique faults. Thus, the manufacturing test of emerging memories is challenging due to not only the fact that these memories are affected by novel faults with a parametric nature but also the fact that fault propagation of this kind of faults is not easy and can be time-consuming.

In this context, this paper proposes to analyze the use of stress conditions to facilitate fault propagation and consequently avoid possible test escapes. In addition, this analysis will allow us to properly understand what is the ideal temperature to be adopted during manufacturing testing, which will reduce the time required for testing. A case study composed of a 3x3 word-based ReRAM implemented using a 130 nm Predictive Technology Model (PTM) was adopted. A total of 17 defects were injected assuming the Resistive Defect (RD) model and 3 different temperature conditions (25, 100, and -40°C) were investigated. The obtained results show that temperature can facilitate fault propagation depending on the defect position. In more detail, weak defects are more easily propagated considering extreme temperatures during testing.

The remainder of this paper is structured as follows. Section II presents the background related to redox-based memristive devices, fault models, and defect injection schemes. In Section III the experimental setup is detailed and in Section IV a further classification of unique faults is presented. Section V

summarizes the obtained results and finally, in Section VI, we conclude the paper.

II. Background

This Section introduces the main concepts regarding redox-based memristive devices and summarizes the existing fault models and defect injection schemes that can be adopted for modeling manufacturing defects in ReRAMs.

A. Redox-based Memristive Devices

A redox-based memristive device is a passive element that consists of a metallic oxide between two metallic electrodes [12]. Physically, the working principle of redox-based memristive devices is based on the reversible formation of a Conductive Filament (CF) composed of oxygen vacancies generated during a Forming Stage. It is important to mention, the absence or presence and the size of CF directly influence the current flow in the device [12]. Also, the CF remains in the redox-based memristive device even when no voltage is applied, which classifies the device as non-volatile [12]. Polarizing the device in one direction increases the CF, which is moving atoms to the active electrode and as a consequence increases the current flow, leading to the Low Resistance States (LRS). Polarizing it in the opposite direction will reduce the CF and the current flow, leading to the High Resistance States (HRS) [12].

The operation that causes the switching from HRS to LRS is called SET and occurs when applying a voltage V_{SET} with a value larger than its threshold voltage (V_{th}). The operation responsible for the LRS switch to HRS is called RESET, occurring when applying a V_{RESET} voltage of opposite polarity to the device [12]. To perform a read operation in the redox-based memristive device, a small V_{READ} voltage lower than both thresholds is applied, and the generated current is sensed, allowing the identification of the device's state. This voltage can be applied in any direction of electrodes, and it needs to be lower so as not to change the state of the device [12].

B. Fault Models

Like any other device, memristive devices are prone to manufacturing deviations, including process variation and manufacturing defects, that may result in different faulty behaviors [8, 9, 13]. Thus, a ReRAM cell can be affected by faults common in CMOS-based memories [5], but also by faulty behaviors that are not observed in traditional memory technologies. In more detail, ReRAMs can be affected by faulty behaviors initially classified into two main fault models: (a) Conventional and (b) Unique [7]. Fig. 1 depicts the resistive states' intervals associated to LRS, HRS as well as the faulty states (Undefined State, Extreme LRS, and Extreme HRS). Note that the conventional logical faults are the regions highlighted in green and red ('1' and '0'), which can present for example stuck-at and transition faults, and the regions highlighted in blue represent the areas of emerging faults related to the unique fault [14]. It can be noticed in the figure the U state, the state between HRS and LRS, which is a region

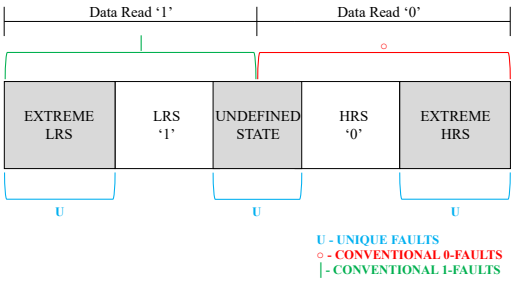


Fig. 1. Resistive states and faulty resistance intervals of ReRAM cells [14].

not ideal for the correct reading for the read circuit. So, this U state needs to be detected because it indicates misbehavior in the memristive device [8, 15]. According to the literature, four unique faults of ReRAMs are already described:

1) Undefined Write Fault (UWF), after a writing operation, the memristive device is in an undefined state U between '0' and '1' (HRS and LRS) [8];
2) Deep State Fault (DeepF) occurs when the resistance in the cell is deep inside the boundaries of one state, being called Extreme HRS and Extreme LRS [15];
3) Unknown Read Fault (URF) occurs when the read operation's output is not reliable. Because it presents a random logic value as a result. A URF can occur when the memristive device stores a resistance very close to or exactly in the U state;
4) Intermittent Undefined State Fault (IUSF), in which the memristive device switches its mechanism intermittently from bipolar to complementary leading to a U state after a write operation [16].

Finally, it is important to mention that all unique faults derive from parametric faults since these faulty behaviors represent a change of electrical parameters' values associated with the resistive states of the ReRAM cell from nominal or expected values.

C. Defect Injection Schemes

In favor of properly simulating all possible faulty behaviors associated to manufacturing deviations, methods for injecting defects in a ReRAM cell are needed. Currently, two defect models are well established in the literature, the Defect Oriented (DO) and the Resistive Defect (RD) model. The DO model focuses on changing parameters in the memristive device itself to simulate faulty behaviors, being able to represent the non-linearity of the memristor device. In contrast, the RD model works by introducing a resistor at one specific point in the circuit to model. A resistor in parallel with the ReRAM cell can lead to an U state during a write operation, for example. Note that the resistor values correspond to the strength of the defects [7]. Finally, it is important to note that for this work, due to its simplicity, the RD model was chosen to be used to inject defects in ReRAM cells.

III. Experimental Setup

In order to understand if the use of stress conditions can facilitate fault propagation, reducing the time required for

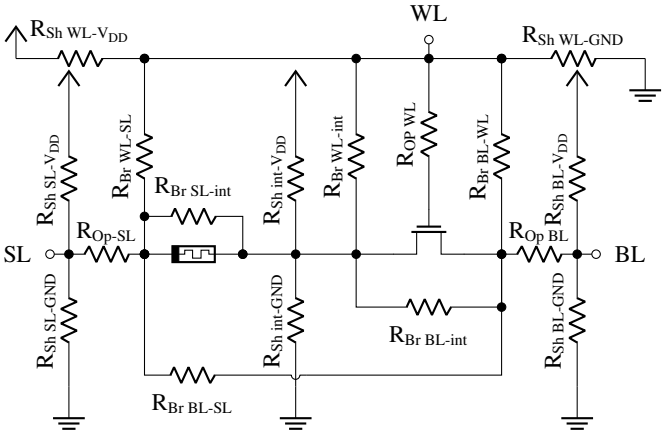


Fig. 2. Defect positions in a 1T1R cell.

performing manufacturing tests of ReRAMs, a case study composed of a 3x3 word-based ReRAM was adopted. The case study was implemented using a 130 nm Predictive Technology Model (PTM) for the CMOS-based circuits and the Valence Change Mechanism (VCM) ReRAM compact model v1b proposed in [17, 18]. The block is the same used in our previous work published in [14, 19]. Every word consists of three 1T1R ReRAM cells, storing one bit of data, as in Fig. 2. Note that the writing methodology adopted always performs a RESET operation at the beginning of each write operation (write '0' or write '1'), this ensures that the cells are not over-SET, which may lead to low reliability [20]. This RESET operation is performed by driving the SL to V_{reset} and the corresponding BL to Gnd. When the data to be written is a '1', a SET operation is subsequently performed on the ReRAM cell only. This is done by setting the BL to V_{SET} and the SL to Gnd. Fig. 3 depict the resistance value regions defined in this work for each resistive state (LRS, HRS, U, ELRS, and EHRS).

A total of 17 defects were injected in a single ReRAM cell according to the RD model. Fig. 2 shows the resistors used to model the possible manufacturing defects in a ReRAM cell. It is important to note that this work introduces the manufacturing defects based on the work presented in [21]. In more detail, in [21], the authors identified all possible positions where to introduce a resistor able to model manufacturing defects in ReRAM cells. Basically, assuming a defect-free ReRAM cell, one resistor at a time was introduced and its size was varied in order to represent different defect strengths and consequently, propagate different faulty behaviors. Note that this analysis does not consider possible impacts in neighbor cells. Fig. 2 depicts a ReRAM cell including the resistors used to model all possible manufacturing defects that can affect the cell. The resistors were named as in [21], and can be classified into three categories: shorts, bridges, and opens. Finally, it is important to mention that the simulations were performed by a tool developed in Python, where a script inserts the defects in the proper position and executes the simulation. In addition, the script is also able to properly classify the observed faulty behavior. Note that the tool changes the resistors' values, from

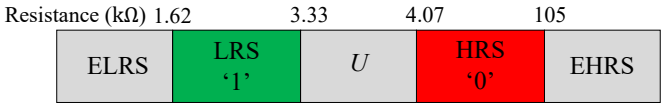


Fig. 3. Resistive states intervals of ReRAM cells.

1 Ω to 10 GΩ. After injecting the defect, the case study is simulated using Cadence's Spectre. The tool follows the test principle based in [22]. Thus, for each defect size, when the simulation is concluded, the faulty behavior is identified and all faults are categorized as conventional or unique. Details about this classification are provided in Section IV.

IV. Fault Analysis and Classification

The faulty behaviors observed during simulations were classified as conventional and unique, where the conventional faults follow the standard classification of memory faults described in [22]. In the proposed analysis we observed the following conventional faults: Stuck-at Fault (SF), Transition Fault (TF), and Incorrect Read Fault (IRF) [22]. For the unique faults, the following classification based on the observed faulty behaviors is adopted:

- Unique State Fault (USF) occurs when the ReRAM cell state goes to the U state, without performing any operation. Note that USF can be further classified as USF0 and USF1, when the expected ReRAM cell value is '0' or '1', respectively;
- Unique Transition Fault (UTF) happens when the ReRAM cell state goes to the U state when switching the cell, or in other words when performing a transition. This type of fault can be UTF0 or UTF1;
- Unique Read Disturb Fault (URDF) occurs when the cell is in a U state, or changes to a U during the read operation, and the read output indicates a wrong logical value when assuming the expected ReRAM state considering the previous write operation;
- Unique Deceptive Read Disturb Fault (UDRDF) is observed when the cell is in a U state, or changes to an U during the read operation, and the read output shows the expected logical value when assuming the expected ReRAM state considering the previous write operation.

Note that USF0, USF1, UTF0, and UTF1 correspond to S0FU, S1FU, W0TFU, and W1TFU defined in [21], respectively.

V. Results and Discussion

This section summarizes the results obtained during the case study's simulations. Fig. 4 summarizes all faulty behaviors observed based on the adopted defect position and strength (resistor value), considering three different temperatures, 25, 100, and -40°C. In the x-axis, the defect's resistance is presented in a logarithm scale. In the next paragraphs, a more complete explanation of the faulty behavior and the type of manufacturing defect is provided. Notice that for short and bridge defects, the faults happen with small resistance values for the injected resistors, and for open, the opposite behavior

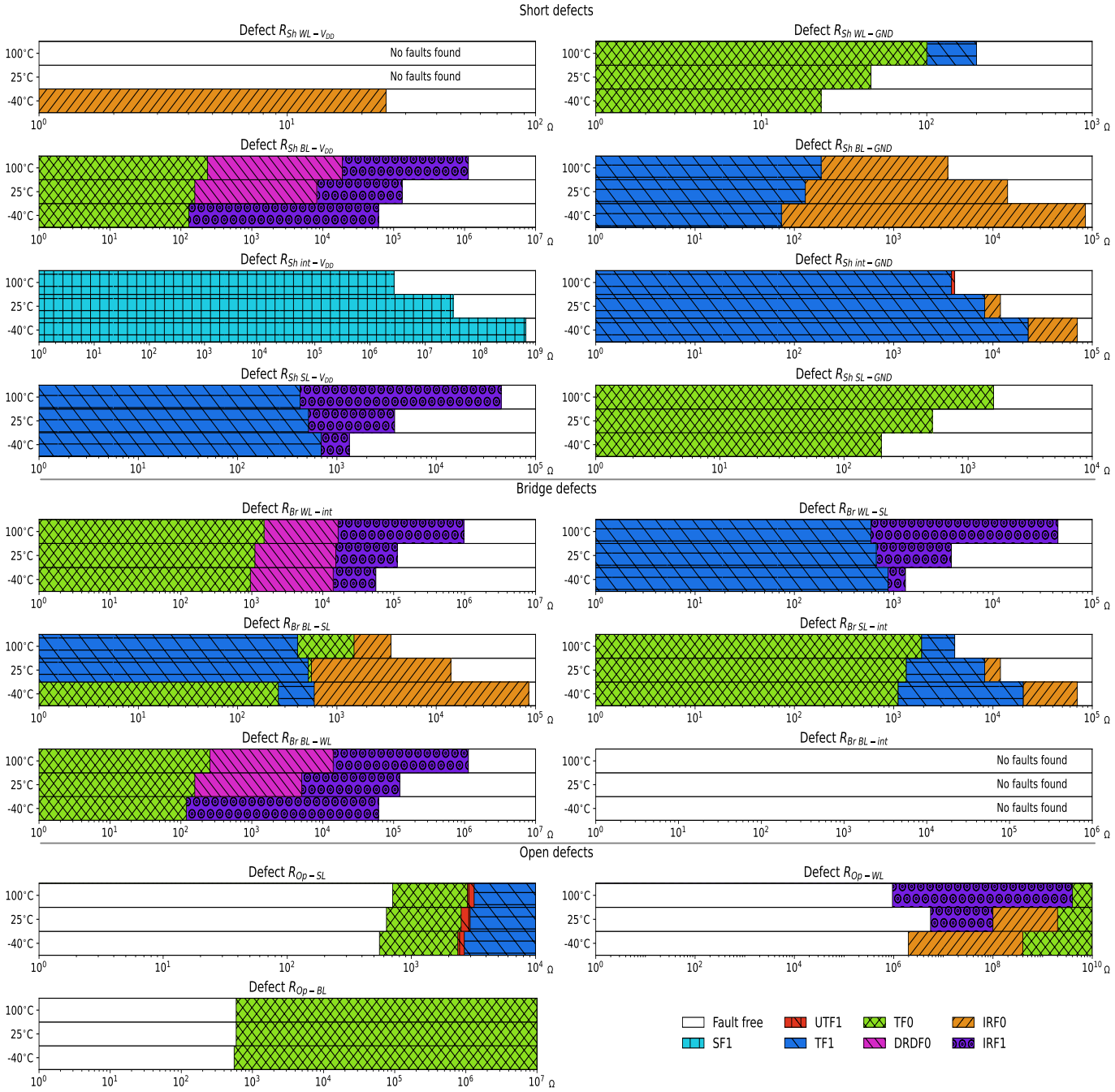


Fig. 4. Bar graphs of faults detected by resistive strength.

is observed. The adopted highest temperature of 100°C was selected based on case study stability aspects.

Short defects: These defects are an unintended resistive path that connects anode to V_{dd} or ground [23].

1) **$R_{Sh\ WL\text{-}V_{DD}}$:** This defect does not impact the cell during writing operations, but it causes IRF0 when assuming a small defect's resistance values (strong defect) at -40°C. This occurs because at lower temperatures the current coming from the SA discharges earlier than expected during the read operation, putting the SA at '1'. This same SA behavior is also observed when considering other defect positions.
2) **$R_{Sh\ WL\text{-}GND}$:** When assuming small defect sizes, the transistor does not turn on during the write cycles and read cycles, causing mainly TF1 and TF0. However, the TF0 was visible first due to the adopted block's write protocol, which always executes a RESET before performing a write operation. Note that in this situation, temperature influences fault propagation, some faults are propagated only when operating at 100°C.
3) **$R_{Sh\ BL\text{-}V_{DD}}$:** The first expected faulty behavior is a degraded SET operation performance because the BL cannot go to ground, and consequently, a TF0 is propagated, and later IRF1. The temperature variation plays

a more significant role in fault propagation. At higher temperatures, a DRDF0 fault can be observed.

4) **$R_{Sh\ BL\text{-}GND}$:** When considering this defect, the fault behavior follows a pattern with respect to changing temperatures. At smaller defect sizes, TF1 occurs and as expected, as the temperature increases the fault boundary becomes bigger. Note that the IRF0 has its behavior affected by temperature in the opposite way.
5) **$R_{Sh\ int\text{-}V_{DD}}$:** Until significant defect sizes are reached, the fault causes an SF1 since the path created through the memristive device causes the ReRAM cell to SET during any operation. Temperature plays a crucial role when considering this specific defect because, at lower temperatures, it is significantly difficult to observe a defect-free operation.
6) **$R_{Sh\ int\text{-}GND}$:** This defect impacts the cell behavior similarly to defect $R_{Sh\ BL\text{-}GND}$. However, here the defect range able to cause faults is bigger and, when assuming 100°C, UTF1 is observed for a smaller defect range. Further, at this temperature, IRF0 is masked by the TF1 fault, hence, not observed.
7) **$R_{Sh\ SL\text{-}V_{DD}}$:** This defect propagates faults during the SET operation, thereby, causing TF1 initially and IRF1 when assuming big defect sizes. The temperature has an inverse impact on the fault propagation of IRF1 with respect to the behavior observed when injecting defect $R_{Sh\ BL\text{-}GND}$.
8) **$R_{Sh\ SL\text{-}GND}$:** As expected, assuming smaller defect sizes, the SL cannot be pulled up to significant voltages, and consequently, a satisfactory RESET can not be performed, causing the cell to exhibit a conventional TF0. Further, although for a very small range of defect sizes not visible in this graph, the cell exhibits a UTF0.

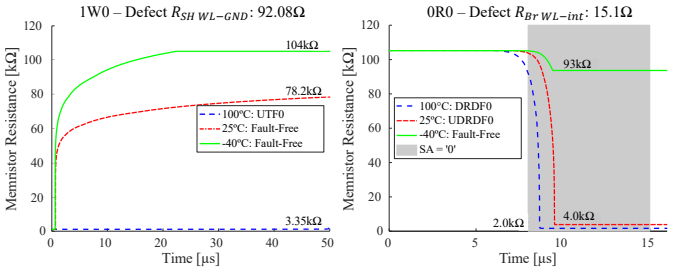
Bridge defects: They are defects that form a parallel resistance between two nodes that not should be connected [23].

1) **Defect $R_{Br\ WL\text{-}int}$:** When injecting small defects in this specific position, it is expected the occurrence of TF0 because, during any operation, the internal node of the ReRAM cell is pulled up when WL is active. This creates a current path through the memristive device, causing a constant SET. At bigger defect sizes, this current path becomes weak. Further increasing the defect size, a DRDF0 fault, followed by an IRF1 fault is observed. The reason is that the SA receives the wrong current due to the *int* being pulled up during the READ operation. The ReRAM cell becomes fault-free as the defect size further increases, weak defects. It is worth noting that temperature plays a crucial role here. As the temperature ranges from -40ºC to 100ºC, the fault boundary increases by 10 folds.
2) **Defect $R_{Br\ WL\text{-}SL}$:** As expected, for small defect's resistance values, the SET operation is affected and a TF1 is observed. Afterwards, an IRF1 is propagated.
3) **Defect $R_{Br\ BL\text{-}SL}$:** When defect sizes are small in this specific position, no write or read operations are allowed due to the created short path between the BL and the SL, hence, both the TF0 and TF1 faults are propagated. Further, at higher defect sizes, an IRF0 fault is observed because the SA receives wrong current.
4) **Defect $R_{Br\ SL\text{-}int}$:** This defect is also similar to $R_{BR\ BL\text{-}SL}$, where both TF1 and TF0 faults coexist. The difference here is that at high temperatures, the IRF0 fault is masked and hence, not observed here.
5) **Defect $R_{Br\ BL\text{-}WL}$:** This defect causes faults similar to the $R_{BR\ WL\text{-}int}$ defect. When there is no defect, the WL is supposed to be pulled down during the reset stage. However, these kinds of defects pull up the WL or int nets causing a reset stage error in the cell. Hence, similar behavior is observed both in terms of temperature and defect size variations. In this defect, at lower temperatures, the DRDF0 fault does not occur.
6) **Defect $R_{Br\ BL\text{-}int}$:** As expected, this defect is not able to cause any write and read issues because the current easily passes through the memristive device.

Open defects: Defects in series within a connection on the cell nodes [23].

1) **Defect $R_{Op\text{-}SL}$:** This defect disconnects the memristive device and the SL. For small defect sizes, no fault is found, as expected. However, for higher defect sizes, transition faults, conventional and unique are observed. Here, the defect can hinder the current from flowing through the ReRAM cell, preventing the cell from SET/RESET correctly.
2) **Defect $R_{Op\text{-}WL}$:** It is necessary for a high defect value to cause a fault during the write. Before that, it is probable to see IRF happen due to the read operation being so short when compared to the write. Interesting to notice that the temperature variation changes the manifestation of the IRF, where at -40ºC IRF0 is dominant, and for 100°C it is the IRF1, for 25°C both happen. Analyzing the TF0 the temperature is also relevant, at -40ºC the fault starts to manifest at 300 MΩ, then 3 GΩ at 100ºC, being a variation of the fault manifestation of 10 times of resistance.
3) **Defect $R_{Op\text{-}BL}$:** For this defect, small defects are not able to propagate any faulty behavior. When increasing the defect size, TF0 can be observed which continues to propagate for the entire analysis range.

Analyzing the obtained results, it is possible to see that open defects cause more unique faults than the other two types. In addition, the temperature can be adopted as a stress condition for facilitating fault propagation, since the same defect size can in some situations propagate or not propagate faults. Note that some faults, such as RDF and URF, were also observed during the simulations, even if they do not appear in Fig. 4. This occurs because the defect size region able to propagate these faults is too small and consequently, not visible in the bar graphs. To exemplify a fault detection situation, in Fig. 5(a) it is possible to see the occurrence of a UTF0 at 100ºC, where the resistive state of the 1T1R ReRAM cell is about 3.35 kΩ,



(a) (b)

Fig. 5. Faults Detection: (a) 1w0; (b) 0r0.

inside the U region. Note that when considering the other two analyzed temperatures, the transition was successful for the same injected defect. Fig. 5(b) depicts two different faults assuming different temperatures for the same injected defect. In more detail, a DRDF0 occurs at 100ºC, and a UDRDF0 happens when simulating at 25ºC, at -40°C no fault is observed in the ReRAM cell, demonstrating the analysis of the fault propagation at different temperatures. Finally, it is important to highlight that DeepFs were not observed during the performed simulations because the RD model is not able to properly cause these faults.

VI. Final Remarks

This paper analyzed the possibility of using temperature as a stress condition to facilitate fault propagation of manufacturing defects in ReRAM cells, reducing the time required for testing ReRAMs at time zero. The detection of unique faults increases the complexity of manufacturing test strategies due to their parametric nature and consequently, not being propagated at the logic level. The obtained results show that depending on the defect position and size, temperature can make the propagation of different faulty behaviors easier. As a future work, we intend to extend the proposed analysis by considering also the possible impact of single ReRAM cell defect on neighbor ReRAM cells as well as other case studies implemented using commercial technology libraries. Finally, we also intend to explore a new memristive device model presented in [18] to implement the 1T1R ReRAM cells and DO model to inject possible manufacturing defects. Note that the new model in [18] includes aspects related to read noise.

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