Compact Low-Voltage Power-Efficient Operational Amplifier Cells for VLSI

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Abstract— Compact low-voltage power-efficient operational amplifiers are described that are very suitable as very-large-scale-integration library cells because of the small die area of 0.08 mm^2 and the minimum supply voltage of 1.8 V. A key part of the circuit is the rail-to-rail class-AB output stage with folded mesh feedback control that combines power efficiency with operation down to 1.8 V and allows sufficient gain in a compact two-stage topology. A version with rail-to-rail input stage features a rail-to-rail input range for supply voltages down to 2.5 V. The dc gain of the op-amps is more than 80 dB while driving 10 kΩ, and the unity-gain frequency is 4 MHz with phase margin of 67° while driving 5 pF. The equivalent input noise voltage is 38 nV/$\sqrt{\text{Hz}}$ at a frequency of 100 kHz. The amplifiers have been implemented in a standard digital 1.6-μm complementary metal–oxide–semiconductor process.

Index Terms— Analog integrated circuits, CMOS integrated circuits, operational amplifiers, very-large-scale integration.

I. INTRODUCTION

APPLYING simple topologies in order to obtain high efficiency is the key design technique for future analog cells in mixed-mode very-large-scale-integration (VLSI) circuits. As the reduction in feature size of complementary metal–oxide–semiconductor (CMOS) processes continues steadily, the supply voltage has to be reduced while the higher integration density enforces lower power consumption per cell. Digital cells benefit from the size reduction, yielding improved digital performance. Analog cells, on the other hand, only benefit marginally because minimum size transistors cannot be used due to noise and offset requirements. Further, the low supply voltage complicates the design, yielding often more complex circuit solutions, which may even result in a performance reduction. The only way for analog cells to keep up with the digital performance and the supply-voltage reduction is by using very efficient topologies that combine low-voltage operation with high power efficiency and small die area.

Existing op-amps can either operate well below 3 V but use a complex structure [1], [2] or employ a simple two-stage topology [3]–[5] but require a supply voltage of the order of 2.7–3.0 V depending on technology. However, as is shown in Section II, the minimum required supply voltage for a compact two-stage op-amp is equal to one gate-source voltage and two saturation voltages, which is of the order of 1.6–2.0 V. This

is only one saturation voltage more than the ultimate lowest supply voltage. But this lowest limit can only be obtained by using at least four stages [2]. The subject of this paper is to develop an amplifier topology that combines operation down to a supply voltage equal to one gate-source voltage and two saturation voltages using a compact two-stage structure offering high power efficiency and small die area.

In Section II the basic low-voltage compact topology is presented. Thereafter, low-voltage class-AB control circuits are discussed, and a suitable control circuit is selected in Section III. In Section IV, the low-voltage topology is extended to allow an optional rail-to-rail input stage. Two op-amp implementations are presented in Section V, together with the measurement results. In Section VI, conclusions are drawn.

II. LOW-VOLTAGE COMPACT TOPOLOGY

The basic topology of a low-voltage compact op-amp is shown in Fig. 1. The amplifier consists of a P-channel (P)MOS input stage M_{20}, M_{22}, a current mirror M_8, M_{10} with cascodes M_4, M_6, and a rail-to-rail output stage M_1, M_2. A PMOS input stage is used to allow common-mode voltages down to and below the negative supply rail. The current mirror is needed to sum the opposite-phase signals of the differential input stage in order to drive the gates of the rail-to-rail output stage in phase. The cascodes provide the necessary level shift between input and output stage. Further, M_6 provides gain by leaving the high input impedance of the gates of the output stage intact. The rail-to-rail output stage allows rail-to-rail output-signal swing, making efficient use of the supply voltage. By biasing the output stage in class AB, the supply current is used efficiently. The class-AB biasing is in principle represented by the voltage source V_{AB}, which expresses all its important properties. To set the quiescent current, the sum of the gate-source voltages of the output stage can be controlled in such a way that it is equal to the sum of a reference PMOS gate-source voltage $V_{GS,P}$ and an N-channel (N)MOS gate-source voltage $V_{GS,N}$, which is obtained by giving V_{AB} the value [6], [7]

$$V_{AB} = V_{DD} - V_{SS} - V_{GS,P} - V_{GS,N}. \tag{1}$$

Note that V_{AB} can be negative at low supply voltages; and, depending on the type of class-AB behavior, V_{AB} may be signal dependent. Sufficient quiescent current is important to guarantee stability when the output voltage crosses the common-mode output voltage and no signal current is drawn by the load. Further, a smooth switchover from one transistor
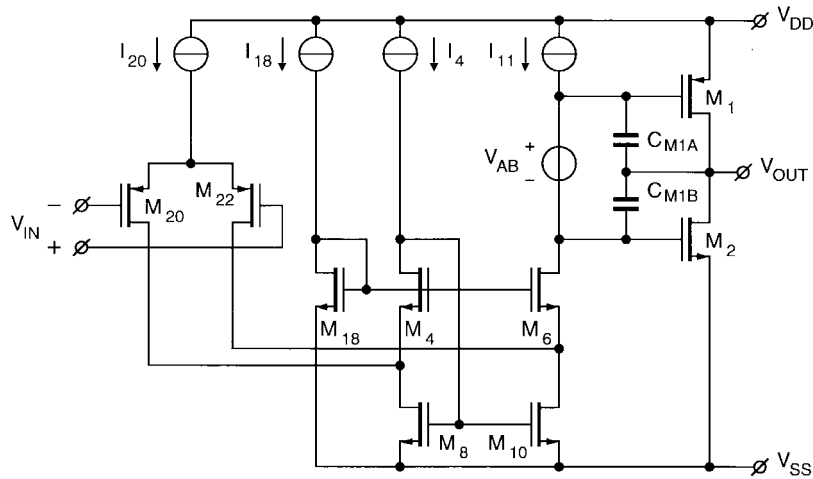
Fig. 1. Compact low-voltage operational amplifier principle.

to the other is obtained, avoiding gross crossover distortion, because the output transistors are gradually switched on and off. A final property is that the signal from cascode M_6 is distributed over the two output transistors in such a way that all the signal contributes to the output voltage independent of which transistor is active. By biasing the class-AB control circuit by the current mirror, no extra current is needed and no extra noise and offset are generated by adding the class-AB function. Because of the simple two-stage topology, Miller compensation is sufficient to compensate the op-amp as indicated by Miller capacitors C_{M1A} and C_{M1B}, which are connected across each output transistor. Thus, no difficult compensation scheme is needed that would require large bandwidth reduction or more bias current in the output stage.

The minimum supply voltage is in general limited by the output stage because it needs to drive high output currents requiring large gate-source voltages. The supply voltage of the output stage is equal to the sum of the gate-source voltage of M_1, the voltage V_{AB}, and the gate-source voltage of M_2, as can be concluded from Fig. 1. Since V_{AB} can be negative, theoretically, the minimum supply voltage needed by the output stage can be very small. Practically, however, the gate of an output transistor is always at least connected via a current source to the supply rails. Because we need to obtain sufficient gain in only two stages, the current source should not deteriorate the impedance and must be cascoded. To allow the lowest possible supply voltage, the transistors of the current source should be biased at the edge of the triode region, resulting in a minimum supply voltage limited by a gate-source voltage and two saturation voltages.

Concluding, each component of the compact op-amp shown in Fig. 1 has at least one important function: proving the high efficiency in terms of the number of components. Because of the low number of components and the two-stage topology, which can be efficiently compensated using Miller compensation, a relatively small bias current is required.

An existing realization of the principle shown in Fig. 1 is presented in Fig. 2. This circuit is used in conventional compact op-amps [4]. The class-AB voltage source V_{AB} is implemented using two complementary head-to-tail con-

nected transistors M_{13} and M_{14} together with biasing transistors M_{15}–M_{18} [8]. The biasing of the output transistors M_1 and M_2 is strongly controlled by two MOS translinear loops $M_1, M_{13}, M_{15}, M_{17}$ and $M_2, M_{14}, M_{16}, M_{18}$, respectively, fixing a well-defined quiescent current. Further, cutoff is prevented, because if one output transistor is driven hard, the gate-source voltage of the other output transistor is clamped by one of the control transistors M_{13} or M_{14}, leaving a certain minimum bias current in the inactive output transistor. Last, it is interesting to consider the signal behavior of the mesh M_{13}, M_{14}. Does this circuit really implement the floating voltage source V_{AB}? The mesh is truly floating since it is only connected to high impedances, the gates of M_{13} and M_{14}, the gates of output transistors M_1 and M_2, current source I_{13}, and cascode M_6. Therefore, signal flowing through the mesh cannot leak to ground and is always used to drive M_1 or M_2. To find out if the small-signal impedance of the mesh is sufficiently low to implement a voltage source, we calculate the impedance $z_{g1,g2}$ between the gates of M_1 and M_2. The impedance is found by dividing the signal voltage $v_{g1} - v_{g2}$ across the gates of M_1 and M_2 by the current flowing through the mesh transistors and is given by

$$z_{g1}, z_{g2} = \frac{v_{g1} - v_{g2}}{g_{m13}v_{g1} - g_{m14}v_{g2}} \qquad (2)$$

where g_{m13} is the transconductance of M_{13}, g_{m14} is the transconductance of M_{14}, v_{g1} is the voltage at the gate of M_1, and v_{g2} is the voltage at the gate of M_2. In the quiescent state, (2) reduces to

$$z_{g1}, z_{g2} = \frac{1}{g_{m13}} \qquad (3)$$

where it is assumed that g_{m13} and g_{m14} are approximately equal. For balancing reasons, M_{13} and M_{14} are usually designed in such a way that their transconductance is equal in the quiescent state. As we see, the impedance of the mesh is low, certainly compared to the high output impedances of current source I_{13} and cascode M_6. As a result, the gates of M_1 and M_2 are practically connected in parallel by the operation of the class-AB control. If, on the other hand, one output transistor—for example, M_1—is handling a large
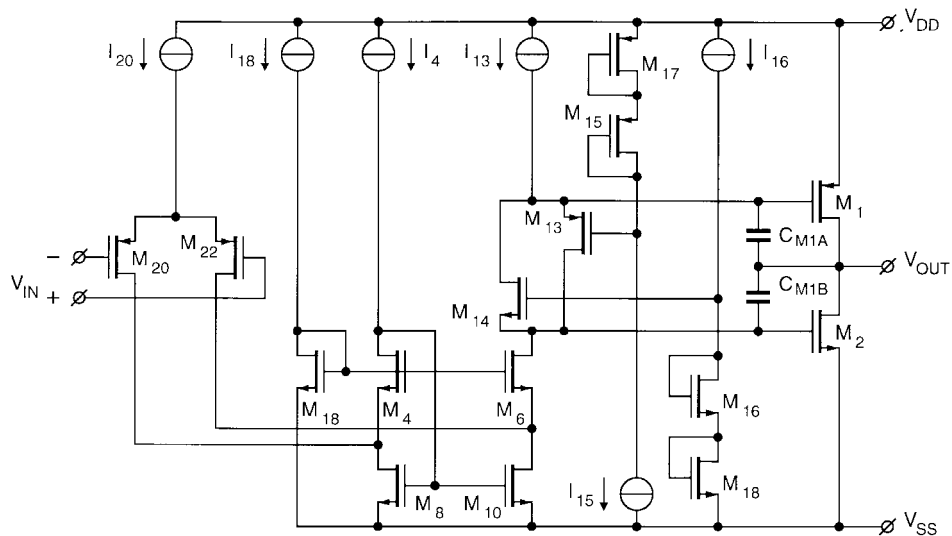
Fig. 2. Conventional compact two-stage operational amplifier with rail-to-rail feed-forward class-AB output stage with mesh.
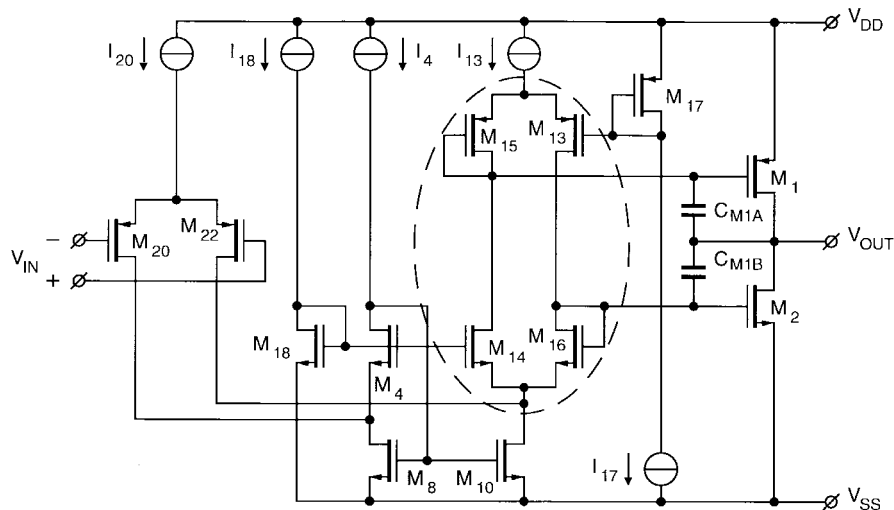

Fig. 3. Low-voltage compact two-stage operational amplifier with rail-to-rail feed-forward class-AB output stage with level shift in mesh.

output current, the other output transistor M_2 is regulated at a constant minimum current. Coupling of the gates of the two output transistors using a mesh with low impedance is not possible because M_1 handles all the signal and has a large signal swing at its gate, while M_2 has a constant gate-source voltage. Consequently, the small-signal voltage v_{g2} at the gate of M_2 is very small. Because the gate-source voltage of M_1 is large, M_{13} is off and its transconductance is very small. Using (2), it can be concluded that the mesh impedance is very large, so that there is no coupling between the two gates of the output transistors. However, transistor M_{14} is still active, operating as a cascode that steers all the signal current delivered by M_6 to the active output transistor M_1. Summarizing, the class-AB control circuit couples the gates of the output transistors in the quiescent mode of operation by generating a low impedance. When one output transistor delivers a large output current, the other output transistor is regulated at a constant drain current and the gates of the output transistors are decoupling by generating a large impedance. At the same time, however,

the class-AB control circuit steers all the signal to the active output transistor.

Another important property of the class-AB control circuit is the contribution to the noise and offset. Fortunately, the class-AB control transistors M_{13} and M_{14} are biased by using the bias current, which is already needed to bias the summing circuit $M_4 - M_{10}$ and M_{14}, M_{16}. Therefore, no additional bias-current sources are required that would increase the noise and offset and also would reduce the gain [4]. The remaining disadvantage of the circuit is that the minimum supply voltage is equal to two gate-source voltages and one saturation voltage. For example, we need to bias the gate-source voltages of M_1 and M_{13} and sufficient voltage across current source I_{16} inside the supply voltage.

To allow lower supply voltages, the voltages at the gates of M_{13} and M_{14} should be one gate-source voltage closer to the supply rails, which can be obtained by removing transistors M_{15} and M_{16} and placing these transistors as a level shift in the mesh. The result is shown in Fig. 3, where the mesh
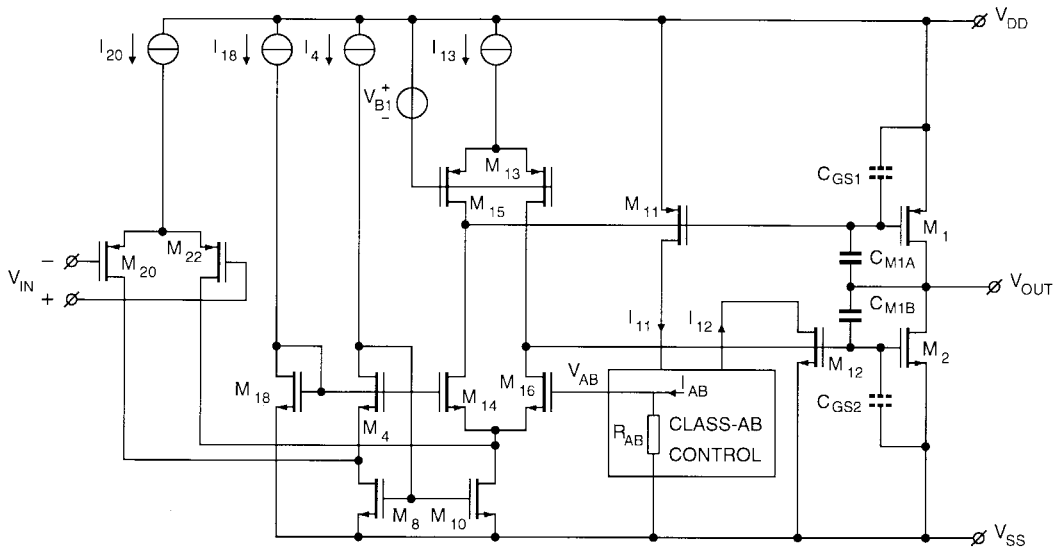
Fig. 4.   Low-voltage compact two-stage operational amplifier with rail-to-rail feedback class-AB output stage with folded mesh and class-AB control.

is indicated by the dashed line. The mesh now consists of transistors M_{13} and M_{14} and diode-connected transistors M_{15} and M_{16}. The output transistors are biased by MOS translinear loops $M_1, M_{15}, M_{13}, M_{17}$ and $M_2, M_{16}, M_{14}, M_{18}$. Some of the properties of the previous circuit are maintained. However, the diode level shifts introduce two problems. First, cutoff of the output transistors occurs when the output stage is driven hard. If, for example, M_1 delivers a high output current, its gate-source voltage is large and all the current in the mesh flows through M_{15} and M_{14} while no current flows through M_{13} and M_{16}. The voltage across M_{16} is very small, and therefore the gate-source voltage of M_2 is small and cutoff occurs. A second problem is that there is almost no room to bias the current source I_{13} and transistor M_{10}. This is especially so when we note that the output transistors usually have large W/L ratios in order to drive large output currents. Therefore, in the quiescent state, the gate-source voltage of the output transistors is relatively small, and room for M_{10} and I_{13} can only be created by making the W/L ratio of M_{13}, M_{14}, M_{15}, and M_{16} very large. There is certainly no room to insert cascodes. Due to the diode connection, M_{15} and M_{16} also do not function as a cascode, so that the obtainable gain is too low in a two-stage topology.

The problems discussed above are related to the diode connection of M_{15} and M_{16}. If we can remove this diode connection, we can make transistors M_{15} and M_{16} operate as cascodes, and room for M_{10} and I_{13} can be created more easily. The principle of the resulting low-voltage compact topology is presented in Fig. 4. The mesh consisting of transistors $M_{13} - M_{16}$ is folded and biased independent of the output transistors. To obtain the desired class-AB biasing, a feedback loop is created consisting of measuring transistors M_{11} and M_{12} and a class-AB control block containing a circuit that implements the desired class-AB control law and generates a control voltage V_{AB} to drive folded-mesh transistors M_{14} and M_{16}. The current of output transistor M_1 is measured by M_{11} and is fed into the control block. The current of output transistor M_2 is measured by M_{12} and is also fed into

the control block. Transistors M_{14} and M_{16} form a control amplifier that regulates the signal at the inputs of the output transistors in such a way that the control voltage is equal to a reference voltage formed by M_{18}. In this way, a feedback loop is created that enforces the desired class-AB behavior. Voltage source V_{B1} forms a fixed bias voltage for transistors M_{13} and M_{15}. Preferably, the class-AB control block contains a circuit that not only controls the quiescent current of the output stage but also maintains a minimum current. Such a circuit is usually called a minimum selector circuit.

The feedback class-AB control circuit with folded mesh has all the desired properties. The minimum supply voltage is one gate-source voltage and two saturation voltages. We need, for example, one gate-source voltage for M_1, a saturation voltage to bias M_{14}, and another saturation voltage to bias M_{10}. Further, the folded mesh $M_{13} - M_{16}$ distributes the signal from the input stage over both output transistors; and, because the mesh is only connected to high impedances, the signal cannot be lost, and all the signal is used to drive the output transistors. This is also the reason why the mesh transistors function as cascodes. Normally, when we tie the sources of two cascodes together, the output impedances are degraded. If we consider, for example, M_{14}, M_{16} as a differential pair and connect the gate of M_1 to a low impedance, the output impedance at the gate of M_2 would be of the order of the output impedance r_d of the transistors. But because the mesh is only connected to high impedances, M_{16} functions as a cascode, and the impedance at the gate of M_2 is of the order of r_d of M_{10} multiplied by the voltage gain μ of M_{16}.

Again, we can investigate the mesh impedance. To calculate the impedance, we first need to model the behavior of the control block. The output voltage V_{AB} of the control block is controlled partly by input current I_{11} and partly by input current I_{12} depending on the state of the output stage. The small-signal transfer function of the control block can be expressed by

$$v_{AB} = r_{AB}(k_1 i_{11} + k_2 i_{12}) \qquad (4)$$

where r_{AB} represents the current-to-voltage conversion of the control block, and k_1 and k_2 are variables that depend on the state of the output stage and determine the influence of the small-signal input currents i_{11} and i_{12} on the class-AB control voltage. In the quiescent state, the control voltage is equally controlled by i_{11} and i_{12}, and k_1 and k_2 are equal. To find the values of k_1 and k_2, we should consider an example of a minimum selector circuit. A suitable example having a simple transfer function is the conventional bipolar minimum selector circuit [9]. The class-AB characteristic of the conventional circuit is described by

$$I_{\mathrm{REF}}(I_1 + I_2) = I_1 I_2 \qquad (5)$$

which also describes the CMOS version of the circuit operating in weak inversion. The transfer function of the minimum selector circuit used to implement the class-AB behavior as described by (5) is given by

$$I_{AB}(I_{11} + I_{12}) = I_{11} I_{12} \qquad (6)$$

where I_{AB} is the output current of the minimum selector circuit. Examining (6) for small signals yields

$$v_{AB} = r_{AB} \left(\frac{1}{\left(1 + \dfrac{I_{11}}{I_{12}}\right)^2} i_{11} + \frac{1}{\left(1 + \dfrac{I_{12}}{I_{11}}\right)^2} i_{12} \right). \qquad (7)$$

In the quiescent state, I_{11} and I_{12} are equal. By comparing (7) with (4), we conclude that k_1 and k_2 are equal to $1/4$ in this case. If one output transistor—for example, M_1—is handling a large output current, the class-AB circuit only controls the biasing of the other one, M_2, and therefore k_1 is zero and k_2 is one. This can also be concluded by examining (7) and noting that I_{11} is much larger than I_{12} in this case.

We now return to the main problem of calculating the mesh impedance. By examining the remaining part of the control loop consisting of differential pair M_{14}, M_{16} and transistors M_{11} and M_{12} and using (4), the mesh impedance $z_{g1,g2}$ is found as

$$z_{g1,g2} = \frac{v_{g1} - v_{g2}}{g_{AB} r_{AB}(k_1 g_{m11} v_{g1} - k_2 g_{m12} v_{g2})} \qquad (8)$$

where g_{m11} is the transconductance of M_{11}, g_{m12} is the transconductance of M_{12}, and g_{AB} is the transconductance of class-AB control amplifier M_{14}, M_{16}. In the quiescent state, k_1 and k_2 are both equal to $1/4$, and for balancing reasons, the transconductance of transistors M_{11} and M_{12} is equal, yielding

$$z_{g1,g2} = \frac{1}{g_{AB} r_{AB} k_1 g_{m11}} = \frac{4}{g_{AB} r_{AB} g_{m11}} \qquad (9)$$

which confirms the low impedance of the mesh. When one output transistor is delivering a large output current—for example, M_1—the voltage at the gate is regulated constant so that v_{g2} is very small. Further, k_1 is zero, and thus the mesh impedance is very large. All the signal current generated by M_{10} and M_{22} is steered by cascode M_{14} to the active output transistor M_1 or by cascodes M_{13}, M_{15}, M_{16}.

It is interesting to consider the contribution of the mesh transistors to the noise and offset. In the same way as in the conventional circuit, the mesh transistors use the bias current of the summing circuit. Therefore, no additional bias current is required, and no extra noise or offset is generated. The differential pair M_{14}, M_{16} may give reason for concern since differential-pair transistors normally contribute to the noise. However, these transistors operate only as differential pairs for class-AB signals, which do not contribute to the output signal. For normal signals, the mesh transistors operate as cascodes, which do not contribute to the noise.

Because a feedback loop is used to implement the class-AB control, also the stability of the class-AB loop should be considered. The loop consists of class-AB amplifier M_{14}, M_{16}, measuring transistors M_{11} and M_{12}, and the class-AB control block. Basically, the class-AB loop can be considered as a single-stage amplifier with transconductance stage M_{14}, M_{16} and with the Miller capacitors and the gate-source capacitors as load capacitors. Since the output transistors are driven out of phase by the class-AB amplifier, there is no class-AB signal voltage at the output node. Therefore, the Miller capacitors can be considered as if they are connected to ground in parallel with the gate-source capacitance. The unity-gain frequency of the class-AB loop is therefore given by

$$\omega_{0,AB} = g_{AB} r_{AB} \cdot \left(\frac{k_1 g_{m11}}{C_{M1A} + C_{GS1}} + \frac{k_2 g_{m12}}{C_{M1B} + C_{GS2}} \right) \qquad (10)$$

where C_{GS1} is the gate-source capacitance of transistor M_1 and C_{GS2} is the gate-source capacitance of transistor M_2. In the quiescent state, k_1 and k_2 are both equal to $1/4$, yielding

$$\begin{aligned} \omega_{0,AB,Q} &= g_{AB} r_{AB} \cdot k_1 \left(\frac{g_{m11}}{C_{M1A} + C_{GS1}} + \frac{g_{m12}}{C_{M1B} + C_{GS2}} \right) \\ &\approx \frac{1}{2} g_{AB} r_{AB} \frac{g_{m11}}{C_{M1A} + C_{GS1}} \end{aligned} \qquad (11)$$

where it is assumed that the transconductance of M_{11} and M_{12} are equal and the capacitance terms $C_{M1A} + C_{GS1}$ and $C_{M1B} + C_{GS2}$ are equal. The gate-source capacitances of the two output transistors are normally not equal; however, the Miller capacitors have usually relatively large values, and therefore the capacitance terms can be assumed to be equal in a first-order approximation. When one output transistor is handling a large current—for example, M_2—the class-AB control circuit is controlling the minimum current of the other output transistor. Then k_1 is one and k_2 is zero, and the unity-gain frequency is given by

$$\omega_{0,AB\max} = g_{AB} r_{AB} \frac{g_{m11}}{C_{M1A} + C_{GS1}} \qquad (12)$$

which is a factor of two larger than the value given by (11) in the quiescent state. However, it should be noted that M_{11} is biased by a current that is a factor of two smaller than in the quiescent state. Therefore, in bipolar technology and in CMOS technology with transistors operating in weak inversion g_{m11} is a factor of two smaller, and the unity-gain frequency is independent of the state of the output stage. In CMOS with transistors operating in strong inversion, the transconductance changes only by a factor of $\sqrt{2}$, and therefore the bandwidth is a factor of $\sqrt{2}$ larger than in the quiescent state. To assure

that the biasing of the output transistors is controlled over the whole bandwidth, the unity-gain frequency of the class-AB loop should be larger than the unity-gain frequency of the main amplifier. However, the unity-gain frequency of the class-AB loop should be fixed at a frequency well below the parasitic poles of the minimum selector circuit in order to obtain a stable class-AB loop. Concluding, when using CMOS in strong inversion, the bandwidth of the class-AB loop is the smallest in the quiescent state, and therefore it should be checked in the quiescent state if the bandwidth is sufficient. In which state the phase margin is minimum depends on the implementation of the minimum selector, and this is discussed in the next section, where the minimum-selector circuits are discussed. As can be concluded from (11) and (12), the bandwidth of the class-AB loop can be manipulated by adjusting the transconductance g_{AB} of the class-AB amplifier.

Concluding, we have found a low-voltage compact op-amp topology with the same properties as the conventional op-amp topology. Good class-AB behavior is obtained without reducing the gain and without extra noise contribution, but with operation down to lower supply voltages of one gate-source voltage and two saturation voltages. We now have to find suitable minimum-selector circuits that can operate at these low supply voltages. This will be considered in the next section.

III. LOW-VOLTAGE OP-AMP IMPLEMENTATION

A. Minimum-Selector Circuit

A class of well-known reliable class-AB control circuits uses a decision pair to control the minimum bias current in the output stage [9]. A low-voltage CMOS version of this circuit uses a PMOS decision pair in combination with an NMOS control amplifier [10]. A disadvantage of this arrangement is the bad matching between PMOS gate-source voltage and NMOS gate-source voltage, which makes this circuit unreliable at very low supply voltages [7]. A solution to this problem is to replace the PMOS decision pair by an NMOS diode-coupled decision pair. The result is a first complete implementation of a folded-mesh class-AB output stage, as shown in Fig. 5. As indicated in the figure by the input currents I_{IN1} and I_{IN2}, the input signal can be fed into the sources of the PMOS mesh transistors as well as into the sources of the NMOS mesh transistors. The current of M_1 is measured by M_{11} and is used to generate a voltage across R_{13}. The current of M_2 is measured by M_{12}, flows through mirror M_{19}, M_{17}, and generates a voltage across R_{15}. The lower of the two voltages across the resistors, which corresponds to the lower of the bias currents of the output transistors, controls the output of the decision pair M_{13}, M_{15}, which is connected to the gate of M_6. This voltage steers the class-AB amplifier M_4, M_6, which is part of the previously discussed mesh. The amplifier regulates the control voltage equal to a reference voltage created by M_{14} and R_{14} by controlling the signal at the gates of the output transistors. Thus, a feedback loop is created that controls the minimum current of the output transistors. By using an NMOS diode-coupled decision pair,
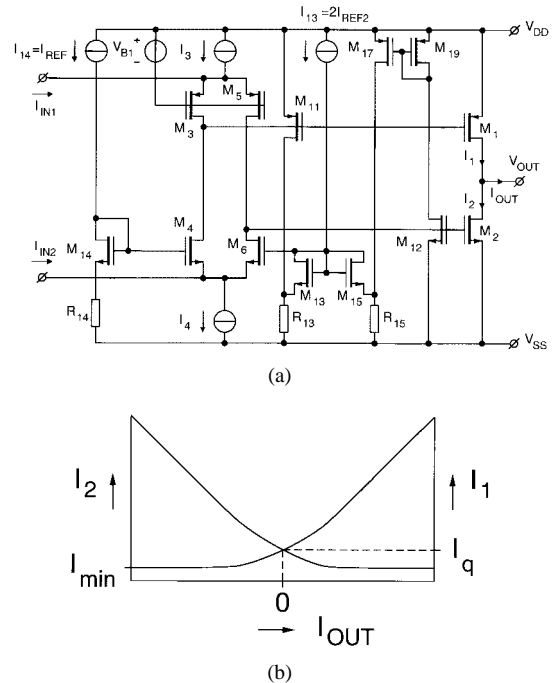

(a)

(b)

Fig. 5. Low-voltage feedback class-AB output stage with folded mesh and diode-coupled minimum selector. (a) Circuit. (b) Class-AB characteristic.

the voltage across current source I_4 is accurately determined by the voltage across R_4. The voltage across I_4 is very important because it must be sufficient to allow I_4 to function properly, but it must be as small as possible to allow low supply voltages. The minimum supply voltage of the output stage is equal to the sum of the gate-source voltage of M_1, the voltage across I_4, and the minimum voltage required to bias M_{14} in saturation. However, a drawback is that care must be taken to obtain a well-defined minimum current. As can be concluded from the relation between minimum current $I_{\min}$ and quiescent current I_Q

$$I_{\min} = \left(1 - \frac{I_{REF2}}{I_{REF} - I_{REF2}} - \frac{2 - \sqrt{2}}{R_{13,15}(I_{REF} - I_{REF2})} \right.$$
$$\left. \cdot \sqrt{\frac{I_{REF2}L_{14}}{\mu_n C_{ox} W_{14}}} \right) I_Q \qquad (13)$$

where I_{REF} and I_{REF2} are the currents of the current sources as indicated in Fig. 5(a), I_{REF2} should be taken small, and R_{13} and R_{15} should be taken large to obtain sufficient minimum current. The resulting class-AB characteristic is depicted in Fig. 5(b). The need for large resistors is the main disadvantage of this circuit, since accurate large resistors are not always available in CMOS processes and require a large die area.

A CMOS minimum selector circuit without resistors exists [2] but is quite complex and requires a relatively large amount of bias current. Recently, a very simple and compact minimum selector circuit has been proposed that also does not use resistors [11]. An output stage which incorporates this minimum selector in a folded mesh feedback class-AB circuit is shown in Fig. 6(a). The current of M_2 is measured by M_{12}. The drain current of M_{12} flows through mirror M_{17}, M_{15}, which is part of the minimum selector circuit M_{11}, M_{15}, M_{17}. Transistor

M_{15} of the minimum selector circuit operates mainly in the linear region. Only when M_1 handles large output current does M_{15} operate in saturation. M_{11} measures the current of M_1 and is also part of the minimum selector. The drain current of M_{11}, which is the output of the minimum selector, flows through M_{13} and steers the class-AB amplifier M_4, M_6. The class-AB amplifier regulates the signals at the gates of the output transistors in such a way that the current through M_{13} is equal to the reference current I_{REF} that flows through M_{14}. If the output stage is in the quiescent state, the drain current of M_1 is equal to the drain current of M_2. In this situation, transistors M_{11}, M_{15}, and M_{17} should be designed such that their gate-source voltage is equal. Then, because transistor M_{15} operates in the linear mode, the combination M_{11}, M_{15} can be considered as a single transistor with a double length. Therefore, the current through M_{17} and M_{12} is a factor of two larger than the current through M_{13}, which is regulated to I_{REF} by the class-AB amplifier. Thus, the quiescent current is given by

$$I_Q = 2 \frac{W_2 L_{12}}{L_2 W_{12}} I_{REF}. \qquad (14)$$

When M_1 delivers a large output current, its gate-source voltage will be large, and the voltage between the positive rail and the source of M_{11} will be sufficient to allow M_{15} to operate in saturation. Transistors M_{17}, M_{15}, M_{11} now function as a cascoded current mirror and simply mirror the current of measuring transistor M_{12} into M_{13}. Thus, the bias current of the inactive transistor M_{12} is regulated to a constant value equal to half the quiescent current. When M_2 delivers a large output current, much current flows through M_{12} and M_{17}. M_{15} then pulls the source of M_{11} to the positive supply rail. Now M_1 and M_{11} operate as a current mirror and the current of M_1 attenuated by a possible scaling factor of mirror M_1, M_{11} flows through M_{13}. Consequently, the current of inactive transistor M_1 is controlled and is equal to half the quiescent current yielding the minimum current

$$I_{min} = \frac{W_2 L_{12}}{L_2 W_{12}} I_{REF} = \frac{1}{2} I_Q \qquad (15)$$

where it is assumed that the scaling between M_1, M_{11}, and M_2, M_{12} is equal. Another way to investigate the class-AB behavior is by finding the relation between the drain current I_1 of M_1, the drain current I_2 of M_2, and I_{REF}. We can express the transfer function from the drain current of M_1 to the drain current of M_{11} as a function of the drain-source voltage of M_{15}. Then the expression for M_{15} in the linear region is used to find V_{DS}. After substitution of V_{DS} in the previous relation, the result is

$$I_1 = \left(\frac{I_{REF} - \sqrt{I_2}\left(\sqrt{I_{REF}} - \sqrt{\frac{1}{4}I_2}\right)}{\sqrt{I_2} - \sqrt{I_{REF}}} \right)^2 \qquad (16)$$
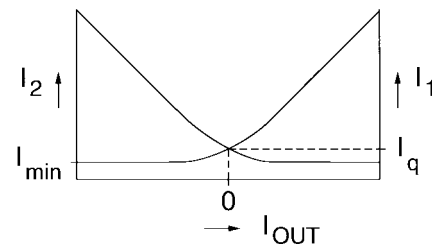
where it is assumed that all W/L ratios are equal and all transistors are operating in strong inversion. In weak inversion, the class-AB characteristic is described by (5) [11]. It should be noted that (16) is only valid if M_{15} is operating in the
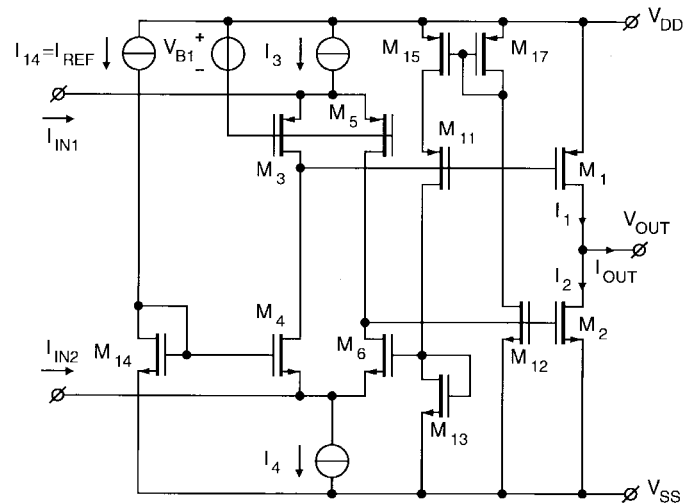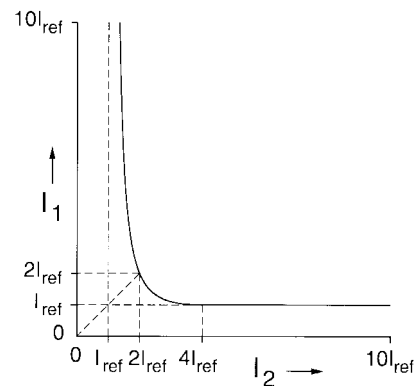
Fig. 6. Low-voltage feedback class-AB output stage with folded mesh and simple minimum selector. (a) Circuit. (b) Plot of I_1 as a function of I_2. (c) Class-AB characteristic.

linear region. The edge of the linear region is reached for $I_2 = 4I_{REF}$. For larger values of I_2, M_{15} enters the saturation mode and I_1 is constant and equal to I_{REF}. From (16), it can be concluded that there is an asymptote for $I_2 = I_{REF}$. Another interesting point is found when I_1 is equal to I_2. Then both currents are equal to $2I_{REF}$. The relation described by (16) is plotted in Fig. 6(b). The resulting class-AB plot is shown in Fig. 6(c). A good class-AB behavior is obtained using an absolute minimum of components and only very little current since we only need to bias the two branches needed to measure the currents in the output transistors. Also, this minimum selector circuit can operate on the lowest supply voltage possible since only one gate-source voltage and one
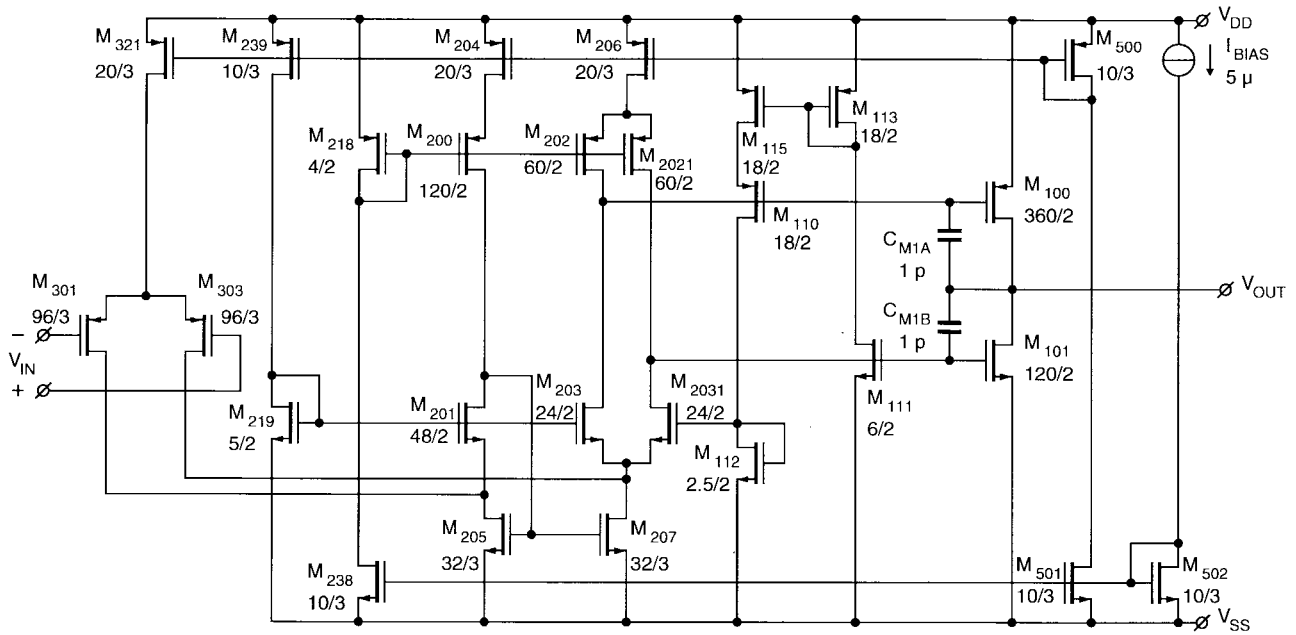
Fig. 7. Low-voltage compact op-amp with PMOS input stage and folded mesh with simple minimum selector (PMOS).

saturation voltage is needed. Of course, in combination with the folded mesh, an additional saturation voltage is required.

Using (11), the unity-gain frequency of the folded-mesh class-AB loop with simple minimum selector in the quiescent state can be calculated as

$$\omega_{0,AB,Q} = \frac{1}{2} \frac{g_{m4,6}}{g_{m13}} \cdot \frac{g_{m12}}{C_{M1} + C_{GS1}} \tag{17}$$

where $g_{m4,6}$ is the transconductance of the class-AB amplifier M_4, M_6, g_{m13} is the transconductance of transistor M_{13} and, g_{m12} is the transconductance of measuring transistor M_{12}. When M_2 handles large currents we find for the unity-gain frequency

$$\omega_{0,AB,\max} = \frac{g_{m4,6}}{g_{m13}} \cdot \frac{g_{m12}}{C_{M1} + C_{GS1}}. \tag{18}$$

As discussed in the previous section, the unity-gain frequency is a factor of $\sqrt{2}$ larger than in the quiescent state if the transistors are operating in strong inversion. Therefore, the minimum phase margin of the class-AB control loop is found in the situation that one of the output transistors delivers a large output current. By investigating the control loop of the circuit shown in Fig. 6(a), we see that the loop for controlling the minimum current of the PMOS output transistor is shorter than the loop for controlling the NMOS transistor. Thus, the minimum phase margin is found when M_1 handles a large current and the bias current of M_2 is controlled by the class-AB circuit. In that case, the bandwidth is limited by the pole of current mirror M_{15}, M_{17} and the pole of cascode M_{11}. If necessary, the unity-gain frequency of the class-AB loop must be reduced by reducing the transconductance $g_{m4,6}$ of the control amplifier in order to obtain sufficient phase margin.

B. Complete Op-Amp

Because of the low number of components and the low current consumption, the class-AB control with simple minimum

selector has been selected to be applied in a complete op-amp implementation, as shown in Fig. 7. The op-amp has a PMOS input stage M_{301}, M_{303}, allowing common-mode input voltage down to the negative rail. The input stage drives a cascoding and summing circuit consisting of a current mirror M_{205}, M_{207} and cascodes $M_{200} - M_{203}, M_{2021}, M_{2031}$. The summing circuit drives the output stage M_{100}, M_{101} with class-AB control $M_{110} - M_{115}$. The class-AB control uses the simple minimum selector $M_{110}, M_{113}, M_{115}$, as discussed in Section III. The minimum selector drives the class-AB amplifier M_{203}, M_{2031} using transistor M_{112}. The class-AB amplifier is part of the folded mesh $M_{202}, M_{203}, M_{2021}, M_{2031}$. Frequency compensation is obtained using Miller capacitors C_{M1A} and C_{M1B}. The Miller capacitors determine the unity-gain frequency ω_0 of the amplifier as given by

$$\omega_0 = \frac{g_{m2}}{C_M} \tag{19}$$

where g_{m2} is the transconductance of the input stage and C_M is the total value of the Miller capacitors. The second pole is shifted to a frequency of

$$\omega_2 = \frac{g_{m1}}{C_{GS} + C_L + \frac{C_{GS}}{C_M} C_L} \tag{20}$$

where g_{m1} is the transconductance of the output stage, C_{GS} is the gate-source capacitance of the output stage including all parasitics connected to the gates, and C_L is the load capacitance including all parasitic capacitance connected to the output. The phase margin is given by

$$\varphi_m = \operatorname{atan}\left(\frac{\omega_2}{\omega_0}\right) = \frac{g_{m1}}{g_{m2}} \frac{C_M}{\left(C_{GS} + C_L + \frac{C_{GS}}{C_M} C_L\right)}. \tag{21}$$

With C_{GS} of 1.4 pF, C_L of 8 pF, C_M of 2 pF, and g_{m1} of 1 mA/V, the second pole is shifted to 10 MHz. To achieve
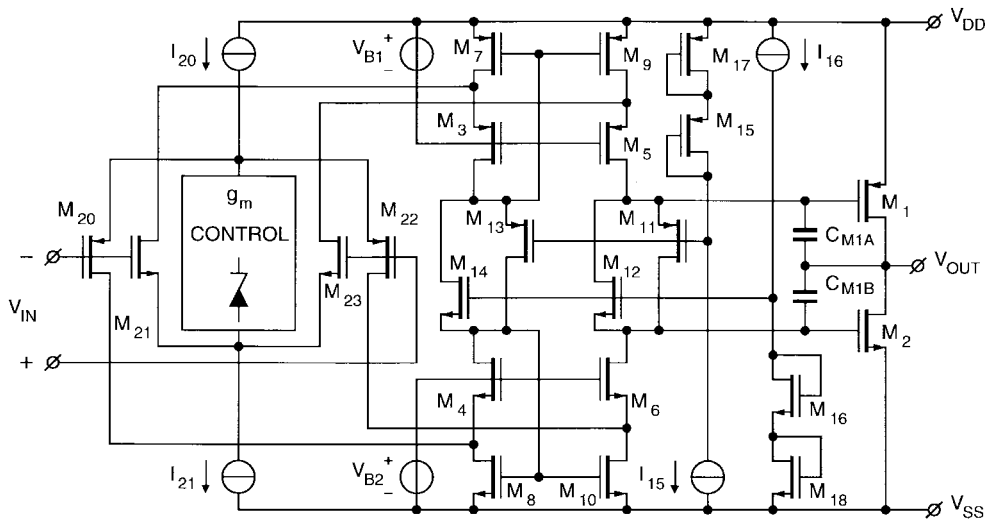
Fig. 8.   Conventional compact operational amplifier with rail-to-rail input stage and two meshes.

sufficient phase margin of about 60°, the unity-gain frequency should be a factor of two lower than the second pole, which yields a realizable unity-gain frequency of approximately 5 MHz. Further, we should investigate the influence of the right-half-plane zero. The frequency of the zero ω_z is given by

$$\omega_z = \frac{g_{m1}}{C_M}. \tag{22}$$

The influence of ω_z on the phase margin depends on the ratio ω_z/ω_0. Combining (19)–(22) and using that the second-pole frequency is a factor of two larger than the unity-gain frequency, the influence of ω_z can be expressed as a phase shift $\Delta\varphi$ given by

$$\Delta\varphi = -\text{atan}\left(\frac{\omega_0}{\omega_z}\right) = -\text{atan}\left(2\,\frac{C_M}{C_{GS} + C_L + \dfrac{C_{GS}}{C_M}\,C_L}\right). \tag{23}$$

Substituting the values for C_{GS}, C_L, and C_M as listed above yields a phase shift of only 4° at the unity-gain frequency. Therefore, measures to remove the right-half-plane zero are not required.

Last, the accuracy of the bias current of the output stage may have an important influence on the stability of the amplifier. As given by (21), the phase margin depends on the matching of the transconductance of the output stage and the input stage. The transconductance is determined by the bias currents, and therefore the phase margin is affected by the matching of the following transistors: M_{321}/M_{239}, M_{219}/M_{112}, M_{110}/M_{100}, M_{111}/M_{101}, M_{113}/M_{115}, M_{203}/M_{2031}. The mismatch in drain currents of two transistors with equal gate-source voltage can be estimated at 5%. For the transistor pair M_{110}, M_{100}, a larger mismatch is assumed because their sources are not biased at the same voltage. Further, a relatively large offset for class-AB amplifier M_{203}, M_{2031} of 20 mV is taken into account because the loop gain of the class-AB loop is relatively low and the drains of the transistors are biased at different voltages. The offset of the class-AB amplifier

increases the mismatch between transistors M_{219} and M_{112} to 15%. Assuming the mismatch terms are not correlated, the total mismatch is found by taking the square root of all the squared mismatch terms, yielding a total mismatch of the order of 20%. Using (21), this gives a reduction of the phase margin of 5° in weak inversion and only 2° in strong inversion. It can therefore be concluded that the influence of mismatch on the stability is small if the circuit is designed with sufficient phase margin of about 60°.

IV. OPTIONAL RAIL-TO-RAIL INPUT STAGE

In this section, we discuss the extension of the low-voltage compact op-amp topology to a circuit with a rail-to-rail input stage. For full rail-to-rail operation, a rail-to-rail input stage requires a supply voltage of two gate-source voltages and two saturation voltages, which is higher than the minimum supply voltage of the basic low-voltage compact op-amp. Because the currents handled by the input stage are relatively small, the minimum supply voltage can be lower than the supply voltage required by conventional output stages. Therefore, it is interesting to consider a low-voltage compact op-amp with rail-to-rail input stage.

The main problem of the rail-to-rail input stage is that the output currents vary as a function of the common-mode voltage. To process these signals without affecting the biasing of the output stage, a special structure of the summing circuit is required. Therefore, we first examine the conventional compact op-amp with rail-to-rail input stage, and thereafter this circuit is modified to allow lower supply voltages using the same techniques as used for the class-AB output stage. A second solution is applying a g_m-control circuit that keeps the output currents of the rail-to-rail input stage constant, so that a standard summing circuit can be applied. This technique is discussed afterwards.

A conventional compact op-amp with rail-to-rail input stage is shown in Fig. 8 [4]. A PMOS input pair M_{20}, M_{22} is placed in parallel with an NMOS input pair M_{21}, M_{23} to process signals from rail to rail. As indicated by the g_m-control block,
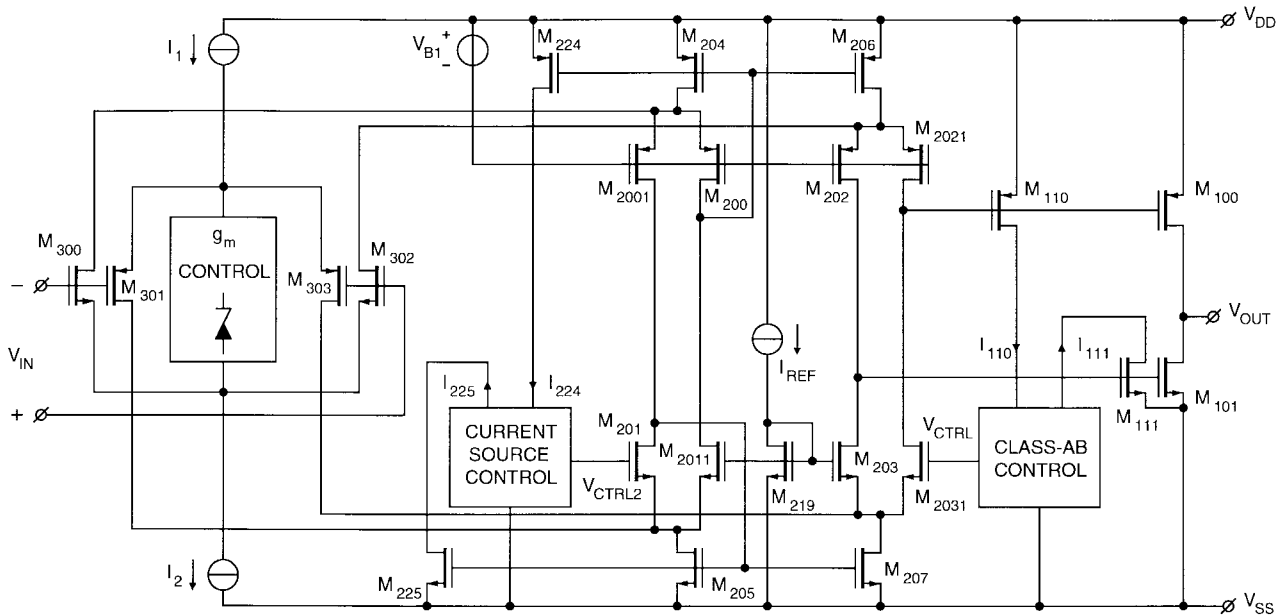
Fig. 9. Principle of low-voltage compact operational amplifier with rail-to-rail input stage and two folded meshes.

a control circuit is needed to make the transconductance as a function of the common-mode input voltage constant. Without g_m-control, the g_m of the input stage is a factor of two larger in the middle of the common-mode range where both input stages are operating than in the other part of the common-mode range when only one stage functions. Therefore, the bandwidth also changes by a factor of two. Because the op-amp has to be compensated for the worst case situation, the bias current in the output stage must be increased by a factor of two. Since the transconductance of CMOS transistors operating in strong inversion is proportional to the gate-source voltage, constant g_m can be obtained by regulating the sum of the gate-source voltages of the PMOS input pair and the NMOS input pair constant, which explains the zener diode shown in the control block [12]. We will consider g_m-control circuits at the end of this section. First, we discuss the summing circuit.

As shown in Fig. 8, a special summing circuit is required consisting of two current mirrors M_7, M_9 and M_8, M_{10} with cascodes M_3, M_5, and M_4, M_6, respectively, and a floating current source M_{13}, M_{14} in order to handle the changing currents of the input stage. The current generated by the floating current source M_{13}, M_{14} flows through M_3 and M_4. At the source of M_3, the bias current of the NMOS input pair is added, and the current is mirrored by M_7, M_9. At the source of M_5, the bias current of the NMOS input pair is subtracted again. At the NMOS current mirror M_8, M_{10}, the same addition and subtraction occurs. Consequently, the current through M_5, M_6 and the class-AB control transistors M_{11} and M_{12} is constant and equal to the current set by the floating current source. By using this configuration, the biasing of the output stage is not affected by the common-mode input voltage [4].

To obtain the same behavior at lower supply voltages, the basic topology of the rail-to-rail compact op-amp is combined with the folded-mesh circuit as discussed in the previous section. In the low-voltage rail-to-rail op-amp as shown in
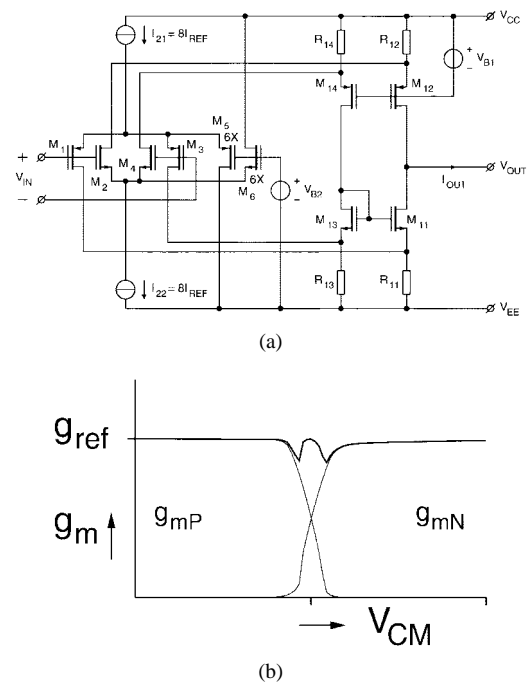

(a)

(b)

Fig. 10. Constant-g_m rail-to-rail input stage with current switches. (a) Circuit. (b) Plot of g_m as a function of the common-mode input voltage.

Fig. 9, a second mesh is used to implement the floating current source. The circuit consists of a PMOS input pair M_{301}, M_{303}, an NMOS input pair M_{300}, M_{302}, a summing circuit $M_{200} - M_{207}, M_{2001}, M_{2011}, M_{2021}$ and M_{2031}, and an output stage M_{100}, M_{101}. A class-AB control circuit and a g_m-control circuit still have to be inserted and are indicated by the blocks. A first mesh $M_{202}, M_{203}, M_{2021}, M_{2031}$ is used to implement the class-AB control by controlling the gates of the output transistors M_{100}, M_{101}. The summing circuit has the same topology as in the conventional compact rail-to-rail op-amp with two current mirrors M_{204}, M_{206} and
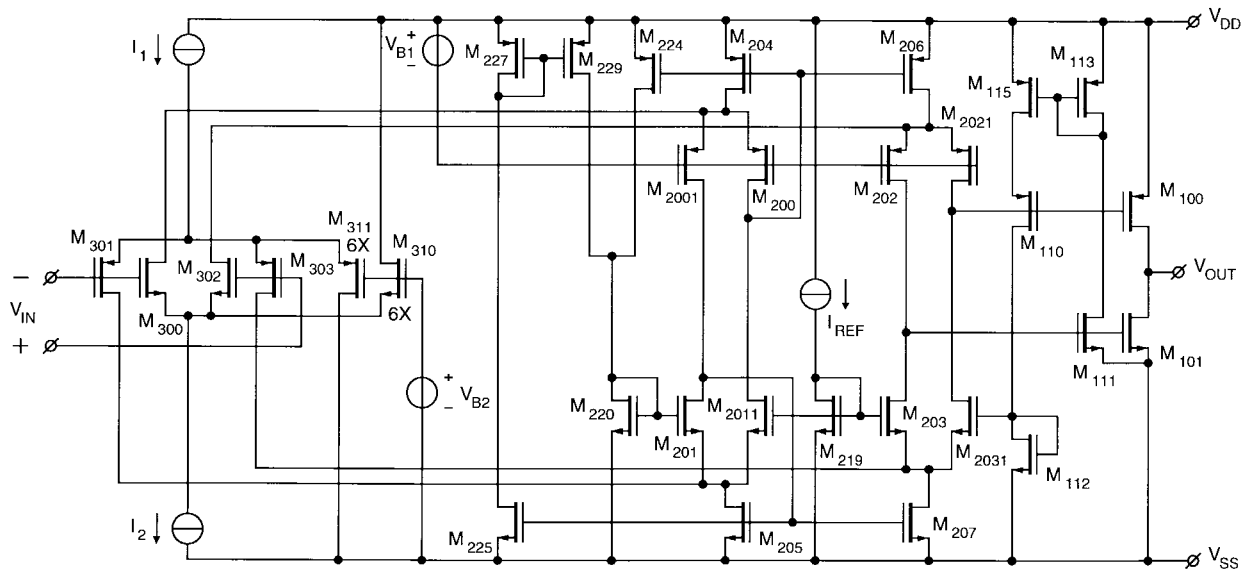
Fig. 11.   Low-voltage compact operational amplifier with two folded meshes and rail-to-rail input stage with g_m-control circuit using current switches.
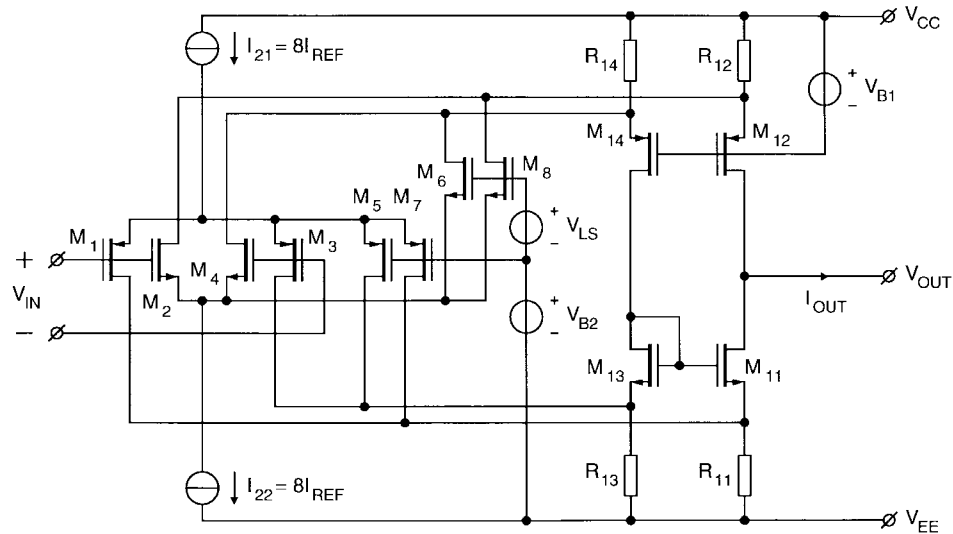

Fig. 12.   Constant-g_m rail-to-rail input stage with current switches and constant common-mode output current.

M_{205}, M_{207} and a floating current source. A second mesh $M_{200}, M_{201}, M_{2001}, M_{2011}$ is used to create the floating current source by controlling the gates of the mirror transistors M_{204}, M_{206} and M_{205}, M_{207}. The biasing of these mirrors is controlled in the same way as with the class-AB control by means of a feedback loop. The bias current of the PMOS mirror M_{204}, M_{206} is measured using M_{224}. The biasing of the NMOS current mirror M_{205}, M_{207} is measured by M_{225}. The drain currents of M_{225} and M_{224} flow into the current-source control block, which completes the feedback loop by driving the gate of M_{201}. The current-source control can be implemented by using the same circuits as used for controlling the output stage.

As discussed before, constant input-stage transconductance can be obtained by regulating the sum of the gate-source voltages of the two input stages constant by using an electronic implementation of a zener diode [12]. However, such a circuit is quite complex and requires another feedback loop. A simple

feed-forward method to control the g_m of the input stage is applying current switches as shown in Fig. 10(a) [7], [13]. In this circuit, a part of the bias current of the PMOS pair M_1, M_3 is removed in the middle of the common-mode input-voltage range by the current switches M_5, M_7. At the same time, switches M_6, M_8 remove part of the bias current of the NMOS input pair M_2, M_4. For high common-mode input voltages, the NMOS input pair operates and the PMOS input pair is off, while the bias current of the PMOS pair completely flows through the switches M_5, M_7. For low common-mode input voltages, the PMOS input stage functions and all the bias current of the NMOS pair flows through the switches M_6, M_8 so that the NMOS input stage is off. In the middle of the common-mode range, when the common-mode voltage is equal to the reference voltage V_{B2}, both input stages are operating together, and therefore the g_m of each input stage should be a factor of two smaller than when only one input stage functions. Consequently, the current through the input
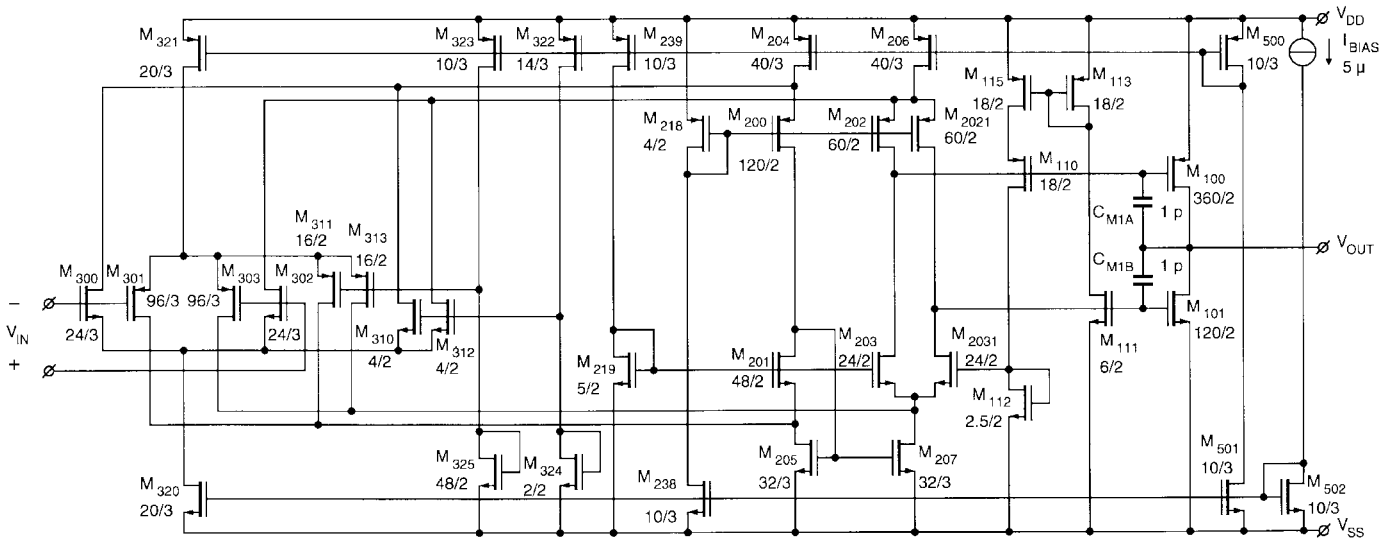
Fig. 13. Low-voltage compact op-amp with folded mesh and constant-g_m rail-to-rail input stage using current switches with constant common-mode output current (R-R).

stage transistors should be a factor of four smaller, which can be obtained by assuring that three-fourths of the bias current flows through the current switches. This is obtained if the W/L ratio of the current switches is a factor of three larger than the W/L ratio of the input transistors. The current switches form a MOS translinear loop together with the input-stage transistors, which gives the relation

$$\sqrt{I_{1,3}} + \sqrt{I_{2,4}} = \frac{\sqrt{8I_{\text{REF}} - I_{1,3}} + \sqrt{8I_{\text{REF}} - I_{2,4}}}{\sqrt{3}} \quad (24)$$

where $I_{1,3}$ is the current flowing through M_1 and M_3 and $I_{2,4}$ is the current flowing through M_2 and M_4. It can be easily verified that the case where $I_{1,3}$ and $I_{2,4}$ are both equal to $2I_{\text{REF}}$ satisfies (24). Another interesting situation is found when one of the currents $I_{1,3}$ or $I_{2,4}$ is zero. In that case, it can be calculated using (24) that the other current is equal to $6I_{\text{REF}}$ instead of $8I_{\text{REF}}$, which would be required to obtain constant g_m. This causes a deviation of 13%, which can also be concluded from the g_m plot shown in Fig. 10(b).

Fig. 11 shows a complete op-amp with rail-to-rail input stage with g_m control using current switches and with a summing circuit using two folded meshes. The circuit consists of a PMOS input pair M_{301}, M_{303}, an NMOS input pair M_{300}, M_{302} with g_m-control current switches M_{310}, M_{311}, a summing circuit $M_{200} - M_{207}, M_{2001}, M_{2011}, M_{2021}$, and M_{2031} with current source control $M_{224} - M_{229}$, and an output stage M_{100}, M_{101} with class-AB control circuit $M_{110} - M_{115}$ and class-AB amplifier M_{203}, M_{2031}. The mesh $M_{200}, M_{201}, M_{2001}, M_{2011}$, which implements the floating current source, is biased using a class-A control consisting of measuring transistors M_{224}, M_{225} and current mirror M_{227}, M_{229}. A class-A control is sufficient because the bias current in the summing circuit is relatively small. The bias current of the PMOS mirror M_{204}, M_{206} is measured using M_{224}. The biasing of the NMOS current mirror M_{205}, M_{207} is measured by M_{225}. The drain current of M_{225} flows through mirror M_{227}, M_{229} and is added to the drain current of M_{224}. The sum of these currents flows through M_{220} and steers
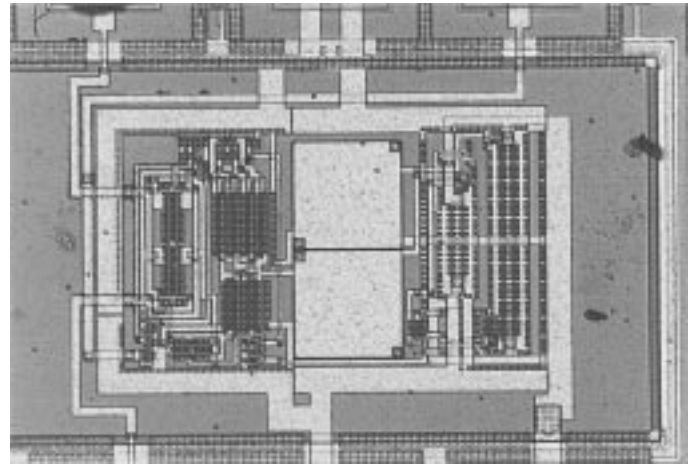
(a)
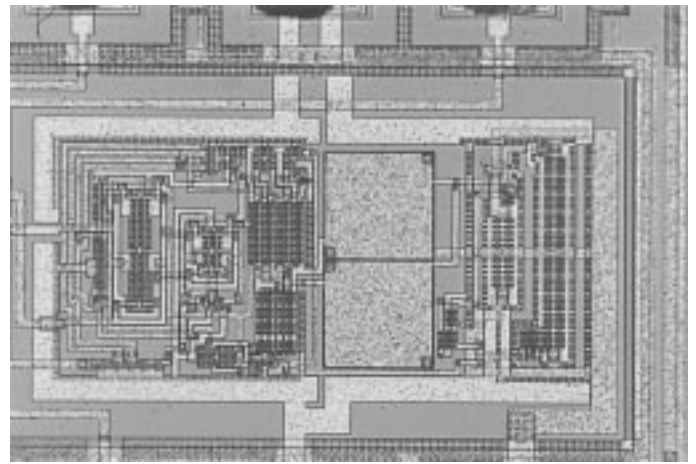
(b)

Fig. 14. Photomicrographs of compact low-voltage op-amp. (a) PMOS op-amp. (b) R-R op-amp.

the control amplifier M_{201}, M_{2011} that regulates the current through the current mirrors M_{204}, M_{206} and M_{205}, M_{207} in such a way that their sum is equal to a reference current
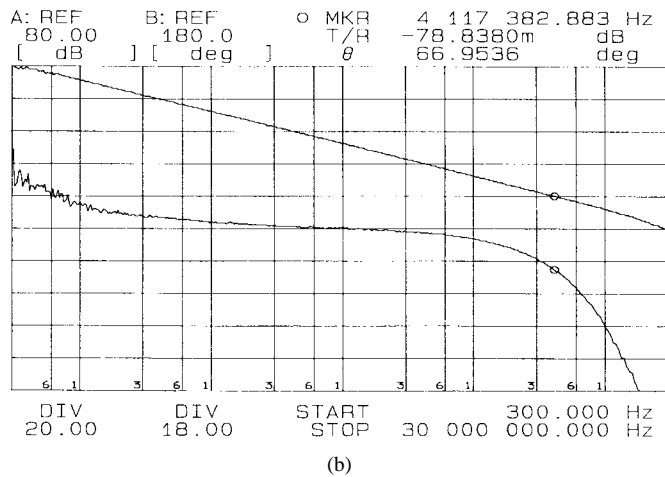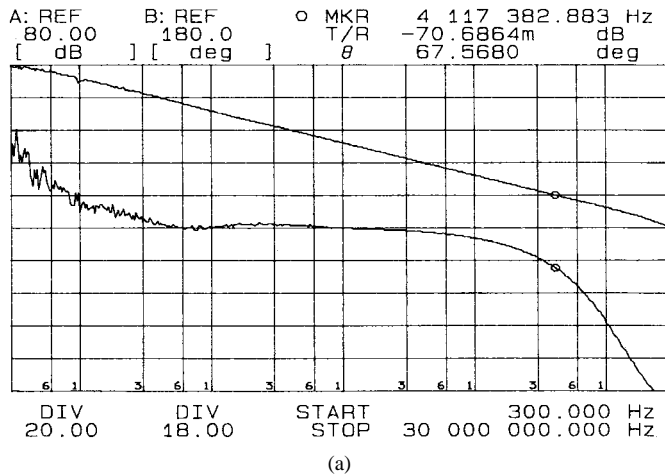
Fig. 15. Frequency response of compact low-voltage op-amps. (a) PMOS op-amp. (b) R-R op-amp.

Fig. 16. Step response ($V_{\mathrm{step}} = 1$ V) of compact low-voltage op-amps (y-axis scale $= 200$ mV/div). (a) PMOS op-amp. (b) R-R op-amp.

I_{REF}, which flows through M_{219}. Thus, the sum of the bias current of the PMOS mirror and the NMOS mirror is regulated constant, yielding a class-A biasing.

A disadvantage of the input stage used in the circuit shown in Fig. 11 is that the W/L ratio of the current switches is a factor of three larger than the sum of the W/L ratios of the two corresponding input-stage transistors. Therefore, a considerable die area is consumed by the g_m-control circuit. If we would apply current switches with a smaller W/L ratio, the gate-source voltage of the current switches in the middle of the common-mode input voltage range would be larger than the desired gate-source voltage. This, however, can be compensated by adding a level-shift voltage V_{LS} connected between the gates of NMOS current switch M_6 and PMOS current switch M_5 as shown in Fig. 12. Another modification depicted in Fig. 12 is that the current switches are divided into two transistors of which the drains are connected to the drains of the corresponding input-stage transistors. The advantage of adding the currents to the outputs of the input-stage transistors is that the output current of the rail-to-rail input stage does not change as a function of the common-mode input voltage. Therefore, the same summing circuit can be used such as in the first op-amp implementation. A disadvantage is that the current switches are connected in parallel with the input transistors and
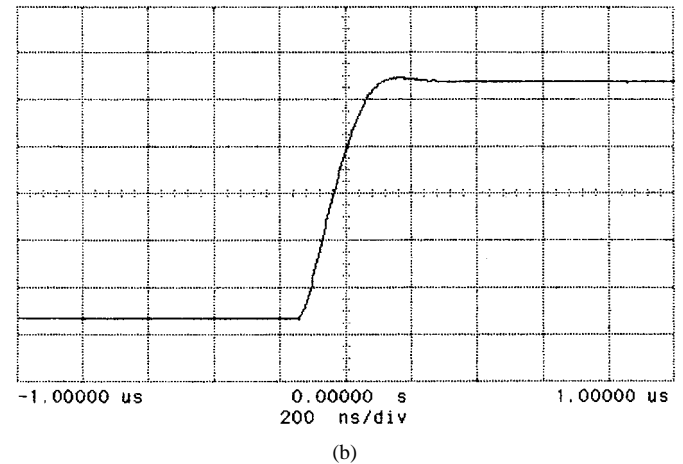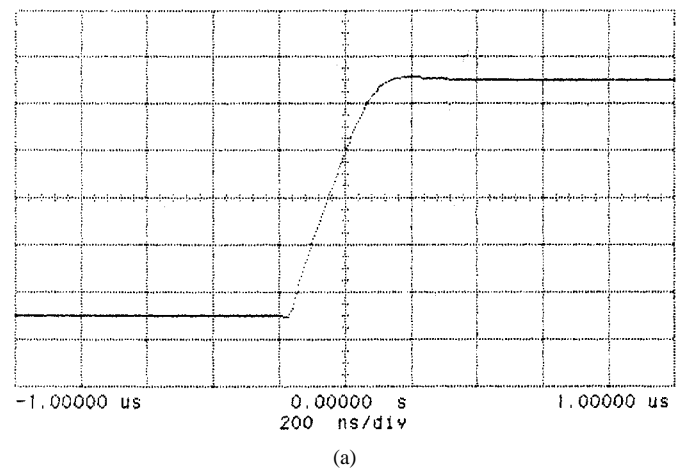
therefore contribute to the noise of the amplifier. Fortunately, because relatively small current-switch transistors can be used, their noise contribution can be made relatively small.

V. REALIZATIONS AND MEASUREMENT RESULTS

A. Realizations

Two op-amps have been designed and fabricated in a 1.6-μm CMOS process. The first op-amp with PMOS input stage (PMOS) was presented in Section III, and the complete schematic was shown in Fig. 7. The second op-amp uses the rail-to-rail input stage (R-R) with constant common-mode output current, which was discussed in the previous section, and the complete circuit diagram is presented in Fig. 13. The rail-to-rail input stage has a g_m-control circuit, as discussed in Section IV. Therefore, the simple summing circuit of the first op-amp can be used. The rail-to-rail input stage consists of PMOS input pair M_{301}, M_{303} and NMOS input pair M_{300}, M_{302}. The g_m-control consists of current-switch transistors $M_{310} - M_{313}$. The level shift between the gates of the PMOS and the NMOS current-switch transistors is created using M_{324} and M_{325}. The summing circuit and output stage are identical to those applied in the first op-amp.
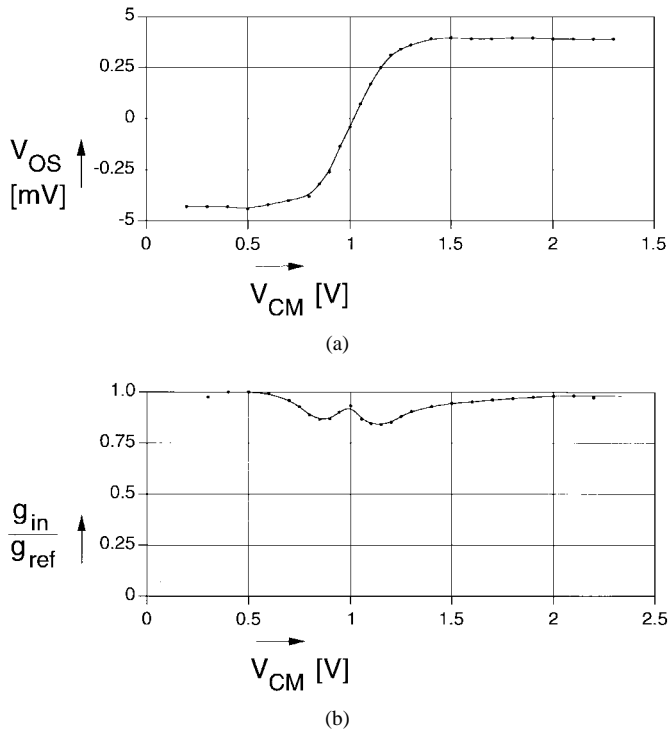
Fig. 17. Offset and input-stage transconductance of op-amp with rail-to-rail input stage as a function of common-mode input voltage. (a) Offset voltage. (b) Transconductance (based on measurement of unity-gain frequency).

TABLE I
MEASURED SPECIFICATIONS OF COMPACT LOW-VOLTAGE CMOS OP-AMPS

parameter		PMOS	R-R		unit
Die area		0.08	0.1		mm^2
Supply-voltage range		1.8 - 7.0	1.8 - 7.0		V
Supply current		184	230		μA
Peak output current		1.2	1.2		mA
input offset voltage		3	6		mV
input noise voltage (f = 100 kHz)		33	38		nV/$\sqrt{\text{Hz}}$
CM Input range	max.	V_{DD}-1.3	V_{DD}-1.3	V_{DD}+0.5	V
	min.	V_{SS}-0.5	V_{SS}-0.5^1	V_{SS}+1.2^1	
Output voltage range	max.	V_{DD} - 0.1	V_{DD} - 0.1		V
	min.	V_{SS} + 0.1	V_{SS} + 0.1		
THD (unity-gain feedback, f = 1 kHz, 1V)		-80	-41		dB
Unity-gain frequency		4	4		MHz
Phase margin		67	67		°
DC-gain		86	86		dB
Slew-rate		4	4.5		V/μs
Settling-time (1%, 1V)		380	370		ns
Settling-time (0.1%, 1V)		480	465		ns

[1] Rail-to-rail if V_{sup} > 2.5 V

B. Measurement Results

Photomicrographs of the two op-amps are shown in Fig. 14. The die area of the first op-amp is 0.08 mm^2, and the other op-amp has a die area of 0.1 mm^2.

The op-amps have been tested using a 10-kΩ resistive load and a 5-pF capacitive load. An HP 4195A network analyzer was used to measure the frequency response. The frequency response of the amplifiers is shown in Fig. 15. Both op-amps have a unity-gain frequency of 4 MHz and a phase margin of 67° while consuming a supply current of 184 and 230 μA, respectively. The power efficiency of the design can be expressed by using the bandwidth-to-power ratio as a figure of merit. A modified version of this figure is given by

$$F = \frac{B}{P_{\text{SUP}}} \frac{C_L}{C_{\text{REF}}} \tag{25}$$

where B is the unity-gain frequency, P_{SUP} is the quiescent power dissipation, and C_{REF} is an arbitrary reference capacitor. The capacitive term has been added to be able to compare circuits designed for different load capacitors. This way, we can compare the circuit with the conventional compact op-amp, which has a bandwidth-to-power ratio of 4 MHz/mW while driving a 10 pF load. Taking C_{REF} equal to 10 pF, the figure of merit for the first op-amp is 6 MHz/mW and for the rail-to-rail op-amp is 4.8 MHz/mW.

The response to a 1 V step is presented in Fig. 16. The op-amp with PMOS input stage has a 1% settling time of 380 ns, a 0.1% settling time of 465 ns, and a slew rate of 4 V/μs. The R-R op-amp has a 1% settling time of 370 ns, a 0.1% settling time of 465 ns, and a slew rate of 4.5 V/μs. The offset

and transconductance of the op-amp with rail-to-rail input stage as a function of the common-mode input voltage are shown in Fig. 17(a) and (b), respectively. The offset voltage changes as a function of the common-mode input voltage from the offset of the PMOS input stage for low values of the common-mode input voltage to the offset of the NMOS input stage for high values of the common-mode input voltage. The offset varies approximately 8 mV, which increases the total harmonic distortion of a unity-gain connected amplifier to about −40 dB for signals around the switch-over region of the g_m-control current switches. The transconductance plot is based on measurement of the unity-gain frequency. From the plot, it can be concluded that the g_m and the unity-gain frequency vary approximately 18%, which is slightly more than the 13% that was calculated in Section IV. An overview of the measurement results is given in Table I.

VI. CONCLUSION

A compact operational amplifier principle has been demonstrated that allows operation down to one gate-source voltage and two saturation voltages by using a folded mesh class-AB control circuit with a simple minimum selector. Using this principle, two op-amps have been designed that can operate

down to 1.8 V. The first amplifier has a PMOS input stage and occupies a die area of only 0.08 mm^2 in a standard 1.6-μm CMOS technology. The second op-amp has a rail-to-rail input stage that enables a rail-to-rail input range at supply voltages down to 2.5 V. Current switches are used to control the g_m of the rail-to-rail input stage, resulting in output currents of the input stage that are independent of the common-mode voltage in addition to yielding a constant g_m. This simplifies the design of the summing circuit. The op-amp with rail-to-rail input stage occupies a die area of 0.1 mm^2. Both amplifiers have a unity-gain frequency of 4 MHz while consuming a supply current of only 184 and 230 μA, respectively, and driving a load capacitance of 5 pF.

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