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Proefschrift

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To my family, whose unwavering love and support have been the pillar of my strength.

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Chapter 1

Introduction

1.1 Introduction

The wireless industry has experienced tremendous development over the past few decades, and it has now reached a point where wireless connectivity is regarded as an essential service. The development of high data rate wireless communication systems has been driven by a wide variety of applications, including mobile internet, gaming, networking, and multimedia streaming. Figure 1.1 displays a graph that illustrates the growing demands for high data rate communication for both long-range (cellular) and short-range (such as WLAN, Bluetooth, etc.) applications. As inferred from the figure, the required data rates have increased at an accelerating pace, and there is no end in sight to this trend. Mobile networks have developed over the past 40 years to connect people in new and enhanced ways. Although this evolution of new features and technologies is continuous, a new generation of mobile technologies is introduced approximately every ten years, which delivers a giant leap in performance, efficiency, and capability. Some of us can still recall the '1G era,' which was characterized by brick-sized phones and analog mobile communication. The system was analog, and it was intended for voice communication. Then in the early 1990s, the second generation (2G) took over and introduced digital communication for the first time. We transitioned into a wireless species around New Year's Day 2002 when the number of wireless subscribers for the first time in history outnumbered the number of wireline users. This brief history highlights how each generation of mobile standards has incorporated the most recent developments in wireless technology. Today, the information treasure accumulated by our ancestors over millennia is instantly accessible to the typical person. Thanks to mobile technology, we can order products and services from anywhere on the earth, at any time, and from any location. The most powerful kings of prior centuries could not even dream of such capabilities for themselves, let alone for all of humanity. Nevertheless,... we are not satisfied!

It is also interesting to overview this tremendous data rate growth by application category. Modern mobile phone customers no longer want to merely be able to make regular phone calls and send texts from wherever; they also want several more advanced features. As illustrated in Fig. 1.2, based on a study conducted by Ericsson on a selected number of commercial networks in the Americas, Asia, and Europe, regardless of device type, video is the most significant contributor to the data traffic volume [2]. Mobile video data traffic is forecast to grow by around 50% annually through 2022 to account for nearly 75% of all

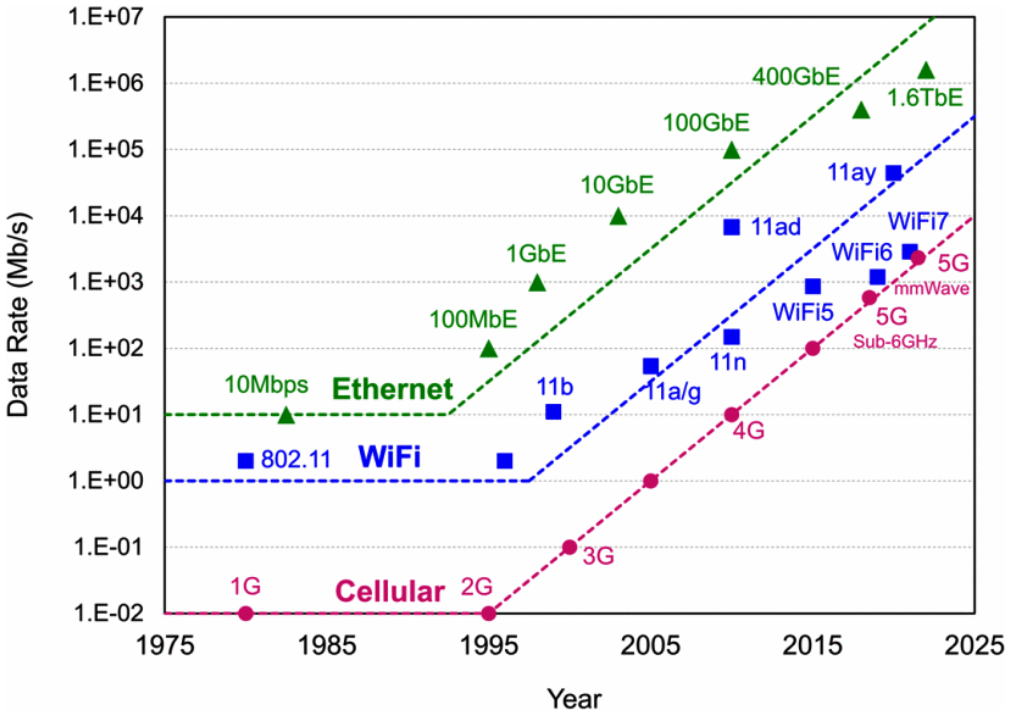
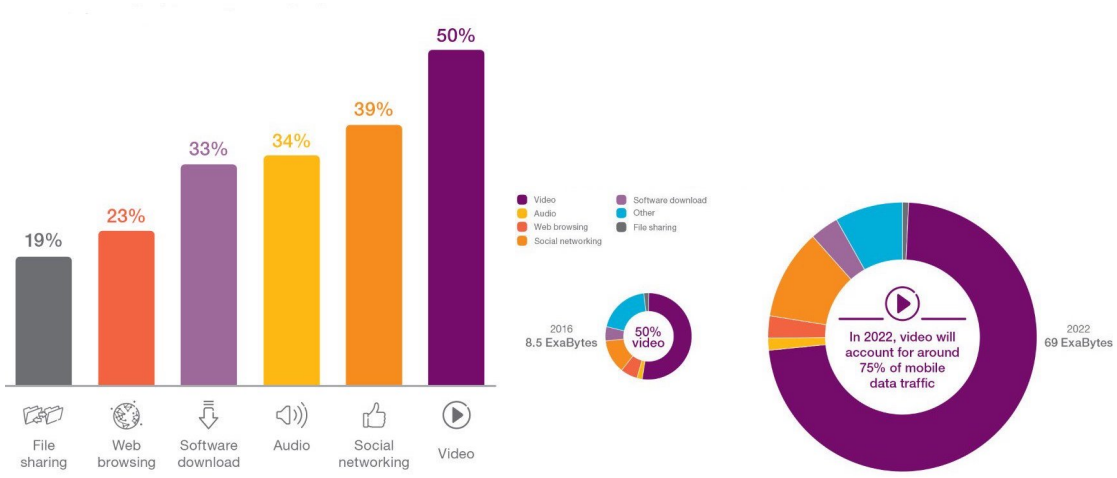


Figure 1.1: Increasing demand for high data rate communication systems [1].

mobile data traffic. Social networking is expected to grow by 39% annually over the coming four years. However, its relative share of traffic will decline from 15% in 2016 to around 10% in 2022 due to the more substantial growth in the video category. Other application categories have annual growth rates ranging from 19 to 34 percent. To sustain this trend, modern communication standards have been established that coexist with the previous ones and eventually replace them. The 5G New Radio (5G NR) standard [3], recently issued by the 3rd Generation Partnership Project (3GPP), intends to dramatically increase data rates and expand the number of applications compared to the preceding 4G Long-Term Evolution (LTE) standard.

Along with the ongoing evolutions in wireless standards, nanometer-scale complementary-metal-oxide-semiconductor (CMOS) integrated circuit (IC) technologies have been developing concurrently, allowing for faster operation and the ability to cram more functionality onto smaller die areas by reducing the size of the transistors. However, analog signals suffer be-



(a) (b)

Figure 1.2: Mobile traffic by application category (a) Percent, (b) ExaBytes [2].

cause of this trend's concomitant decrease in supply voltages. Moreover, passive components, which dictate the size of many typical analog circuits, are not affected by the down-scaling of physical dimensions. Consequently, employing digital circuits whenever possible is essential to fully benefit from scaling; therefore, the analog-based blocks have been reduced in many modern integrated systems.

Radio-frequency (RF) and millimeter-wave integrated circuit design now face new opportunities and challenges due to the trends toward ubiquitous, high data-rate wireless communication and highly integrated systems. From the standpoint of circuit designers, these situations increase the demand for wireless transceivers that can fulfill the growingly stringent requirements by genuinely utilizing the most recent advancements in IC technologies. Recently, the central goal has been to promote the adoption of digital circuitry, which is typically well-suited for modern CMOS technologies and aids in achieving the reconfigurability required by heterogeneous parallel standards. Furthermore, a system-on-chip (SoC) level of integration is preferred as it shrinks the system's size and mass production costs. So far, RF circuit designs did not profit much from Moore's law due to the lack of suitable digital-intensive design techniques capable of addressing the RF specifications/challenges. Thus, both industry and academia have made a tremendous effort to realize an actual single-chip

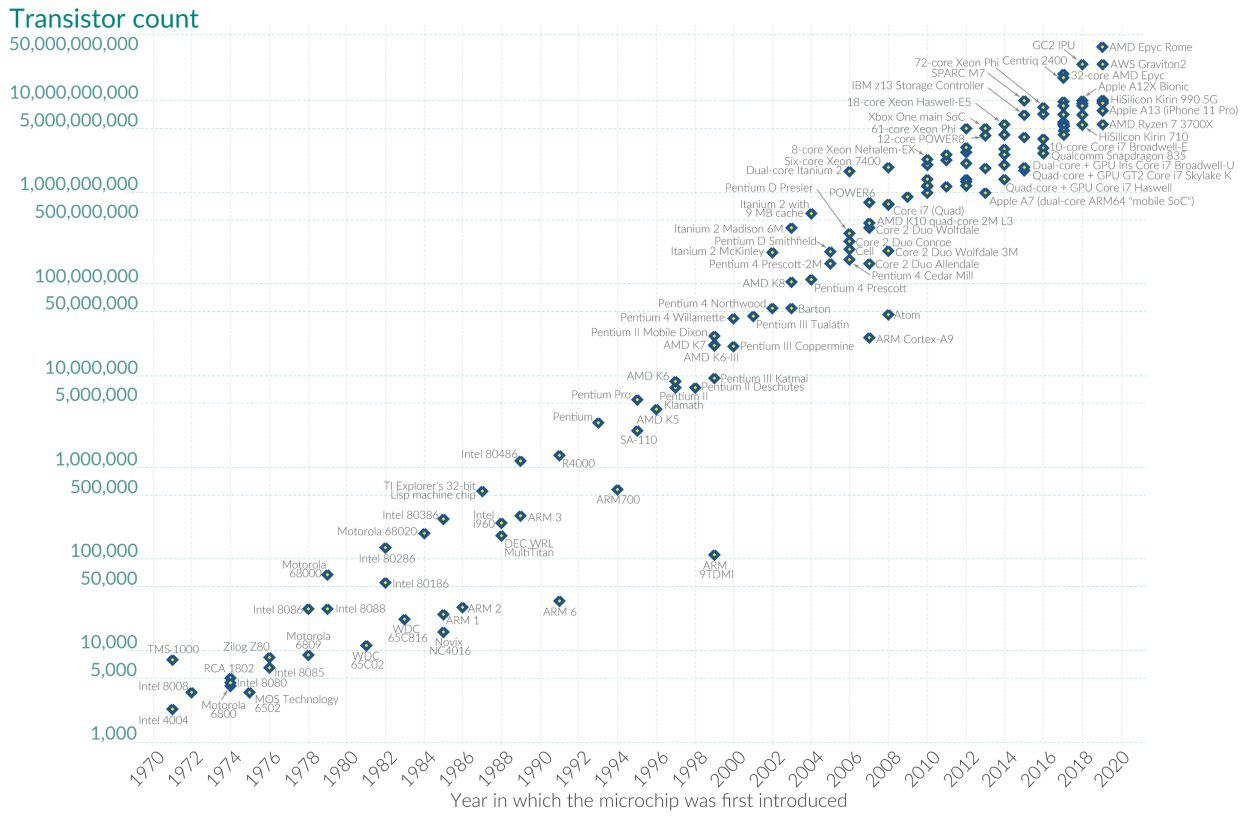


Figure 1.3: According to Moore's law, the number of transistors in microprocessors almost doubles every two years, as seen by a semi-log plot of transistor counts against dates of introduction [4].

radio in CMOS technology and, most recently, FD-SOI processes.

1.2 Digital-intensive transmitters challenges

Over the last two decades, most of the RF transceiver's building blocks have been successfully integrated digital-intensively into CMOS technology. However, one piece missing from the puzzle is the power amplifier (PA) which interfaces the transmitter systems and antennas and is emerging as the critical building block in RF front-ends. Besides the display, the transmitter (TX), in particular the PA block, is responsible for the most of the power dissipation in mobile wireless products. Namely, the PA characteristics such as the output

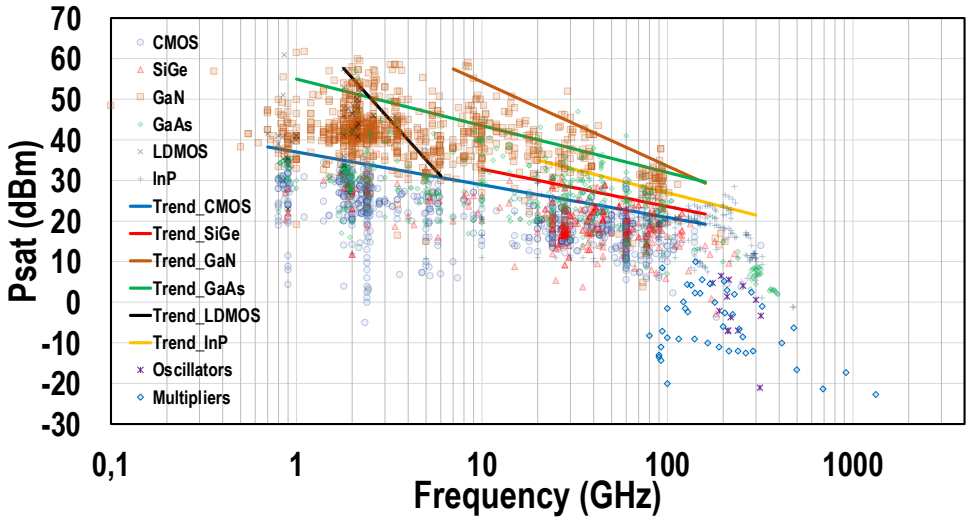


Figure 1.4: P_{Sat} comparison between different technologies over frequency [5].

power (P_{Out}), efficiency, operating bandwidth, and linearity are critical for overall system performance in terms of frequency agility and data error rate/spectrum compliance. The PA efficiency determines its dc power consumption for a specific output power level. The related self-heating of the PA can degrade its output power and cause thermally induced distortion, which appears as memory effects. Therefore, the PA efficiency and output power set the thermal handling requirement of its packaging solutions.

Figure 1.4 shows the saturated output power (P_{Sat}) comparison of PA designs implemented in different technologies [5]. Due to their intrinsic Johnson's limit[1], semi-conductor technologies offer different output power roll-offs versus frequency [7]. The PA is often implemented as a stand-alone module in high-performance III-V compound technologies, like GaN and GaAs. The primary incentives for this approach are to provide exceptional output power capability over a broadband frequency range, which is difficult to achieve in silicon-based technologies. Silicon technologies, such as CMOS and SiGe, offer lower output power

[1]Johnson's figure of merit is a measure of the suitability of a semiconductor material for high-frequency power transistor applications and requirements. More specifically, it is the product of the charge carrier saturation velocity in the material and the electric breakdown field under the same conditions, first proposed by Edward O. Johnson of RCA in 1965 [6].

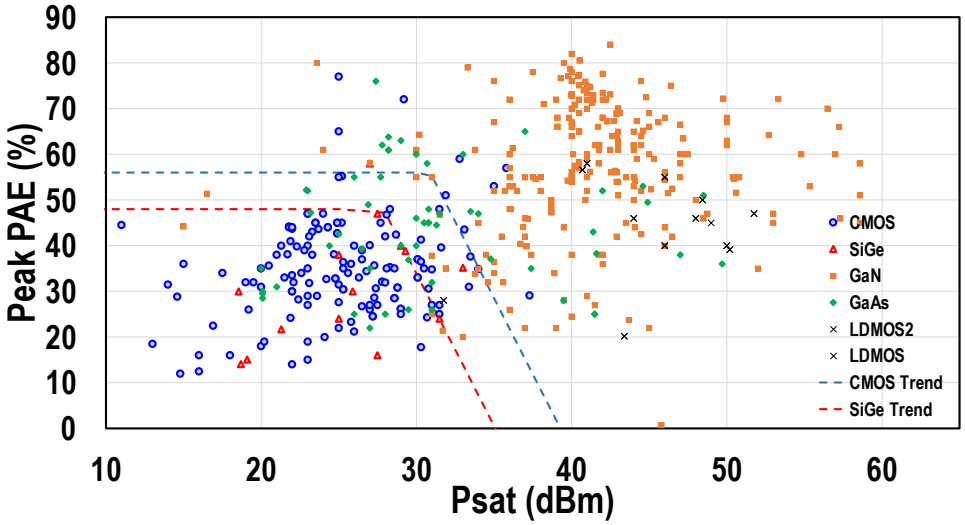


Figure 1.5: Peak PAE and P_{Sat} comparison for 2-6GHz PAs in different technologies [5].

due to the limited device breakdown voltage. Although technology scaling generally results in faster transistors, every technology node also observes a decrease in the breakdown voltage of the transistors. As a result, the power supply voltage must decrease, which increases the difficulty of high power generation in silicon at high frequencies. Additionally, on-chip passives are hampered by low-quality factors brought on by thin metals and the silicon substrate's low resistivity nature. The PA's output power and efficiency are both reduced as a result of these losses. The design of a fully-integrated transceiver that includes on-chip PA thus remains a daunting mission.

Despite the inferior output power capability, silicon-based PAs have shown competitive efficiency performance in low or medium output regimes over 2-to-6 GHz, as shown in Fig. 1.5. As can be gathered, for sub-6GHz silicon-based PAs, the peak PAEs plateau out around 55% for medium/low P_{sat} as the "device limited regime," limited by the intrinsic device-level large-signal efficiency and back-end passive loss [7]. Their PAEs rapidly drop at high P_{sat} as the "circuit/combiner limited regime" due to combiner loss and degraded device, emphasizing the need for circuit innovations.

On the other hand, high-order quadrature amplitude modulation (QAM) modulation schemes are employed in modern communication systems to achieve high spectral efficiency.

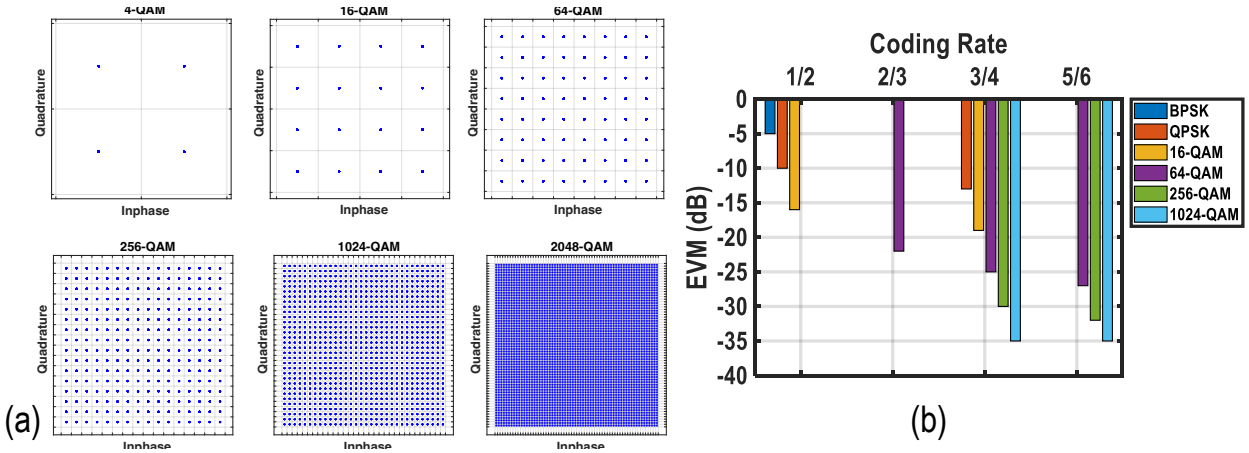


Figure 1.6: (a) High-order quadrature amplitude modulation (QAM) modulation schemes. (b) In-band linearity requirement verified by EVM.

As shown in Fig. 1.6(a), this makes it more difficult to distinguish between the different points in the constellation. As a result, it requires better signal quality, characterized by error vector magnitude (EVM). Fig. 1.6(b) shows the EVM requirement in modern communication systems [8]. It requires -32dB and -35dB EVM for 256QAM and 1024QAM, respectively, for the link, which is very stringent to meet.

In addition to high-order modulation schemes, orthogonal frequency-division multiplexing (OFDM), and carrier aggregation (CA), in which channels can be juxtaposed, leading to large modulation bandwidth (Fig.1.7), are extensively used to achieve high data rate and multipath robustness. However, the resulting highly complex modulation signals usually have a high peak-to-average power ratio (PAPR). Thus, PAs often need to operate in the power back-off (PBO) mode to accommodate the high PAPR and provide sufficient linearity. This makes both PA peak and PBO efficiencies highly critical for battery life and thermal management.

Moreover, spectral emission limits are incredibly stringent. As presented in Fig. 1.8, these spectral emission requirements include a spectral mask (Fig. 1.8(a)), leading to adjacent channel leakage ratio (ACLR) of better than -45dBc, and spurious emission (Fig. 1.8(b)), which for example should be better than 51dBc for a 20MHz signal with an average power of 24dBm [3].

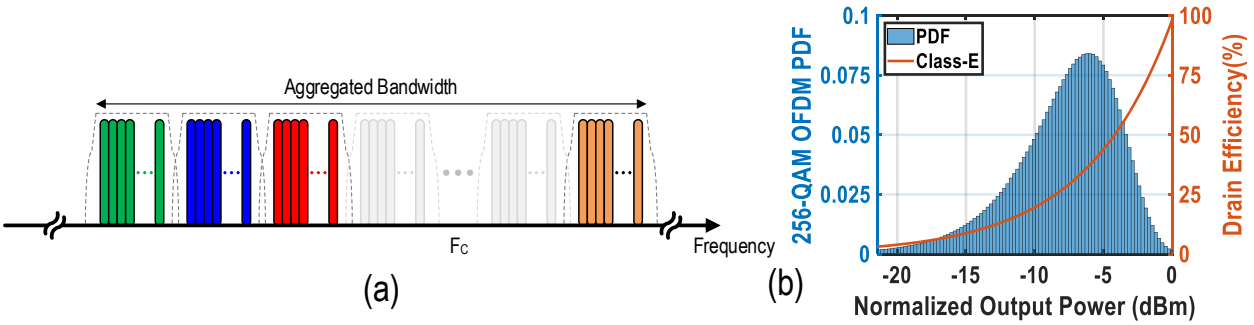


Figure 1.7: (a) Juxtaposed channels in carrier aggregation leading to large modulation bandwidth. (b) Complex waveforms with high PAPR affects average system efficiency.

Despite overcoming these challenges necessitating a significant amount of engineering effort, doing so enables an opportunity to create innovative solutions. Overall, there is a demand for research that considers potential new circuit solutions for digital-intensive transmitters and their associated power amplifiers in light of the technical advancement and desire for expanding capabilities mentioned above. This may result in a better grasp of emerging techniques, which will be extremely beneficial if they start to be employed more widely.

1.3 Thesis Objectives

The goal of this dissertation is to provide a fresh perspective on the theory and implementation of fully-integrated digital-intensive sub-6-GHz transmitters. Based on the abovementioned explanations, this work seeks explicitly to advance the research on digital transmitters managing wideband complex modulated signals to support multi-mode/multi-band communication standards. Moreover, along with generating adequate RF power, circuit innovations to improve efficiency at full power and back-off are presented to address the demand for high average efficiency for high PAPR signals. At the same time, to satisfy the inband signal accuracy and out-of-band spectrum emissions requirements, we introduce and investigate solutions that combine an innovative clocking scheme, high-order digital filters, and a low-complexity DPD technique requiring minimal computational power. Theoretical analysis, system-level and circuit simulations, integrated circuits, printed circuit board design, and

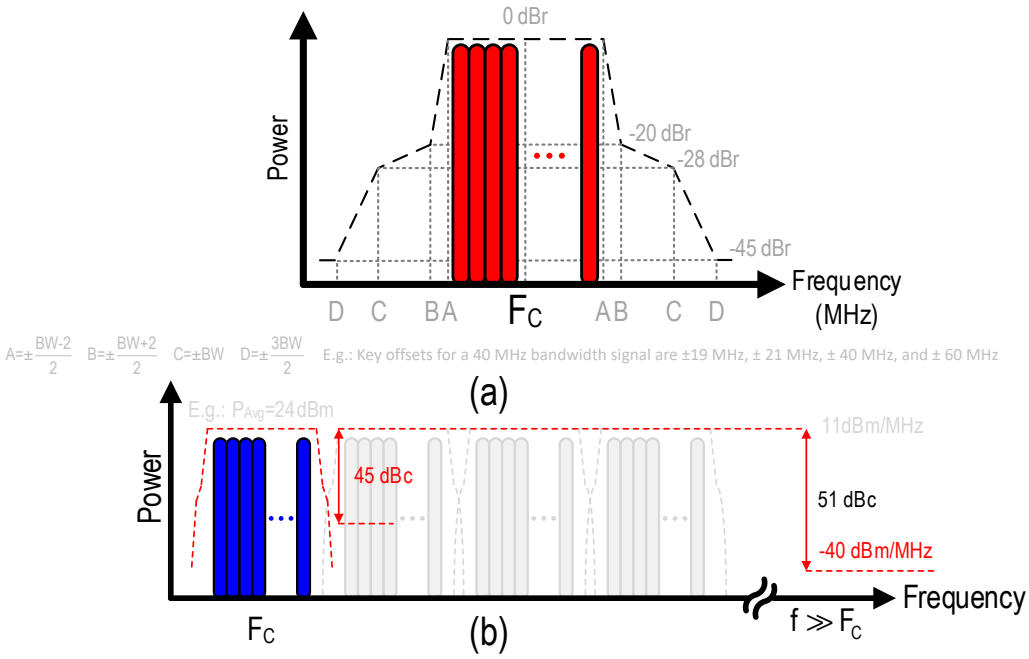


Figure 1.8: (a) Spectral mask. (b) Spurious emission.

measurements of fabricated prototype circuits verify the proposed techniques.

1.4 Thesis Outline

This dissertation is organized as follows:

- **Transmitter Architectures Fundamentals**
  Chapter 2 constructs the foundation for understanding the traditional transmitters and power amplifiers fundamentals. It continues with a brief discussion on the evolution from analog-intensive to digital-intensive TX line-ups. Moreover, this chapter briefly introduces efficiency enhancement approaches to enhance a wireless system's average efficiency while dealing with complex modulation signals like quadrature amplitude modulation (QAM) or an orthogonal frequency division multiplexing (OFDM) signal.

- **A Wideband Energy-Efficient Multi-Mode CMOS Digital Transmitter**
  Chapter 3 first provides a comprehensive comparison between the signed and un-signed DTX operation. Then, it continues with the extensive system-level discussion of the signed Cartesian and multi-phase operation principles. In light of these discussions, a wideband energy-efficient versatile transmitter has been demonstrated. It leverages the advantages of digitally-configured architecture to support a multi-mode/multi-band operation. It features various modes comprising Cartesian and multi-phase configurations utilizing LO clocks with different duty cycles in the interleaving and non-interleaving configurations. Accordingly, its different modes of operation are mathematically analyzed, and their power and efficiency performances are compared. The detailed DTX architecture, circuit design and implementation, and off-chip matching network are provided, followed by the extensive measurement results of the prototype. It has been shown that the multi-phase architecture inherits the advantages of the Cartesian DTX, such as wideband operation, symmetrical and synchronized I/Q paths with a drain efficiency behavior imitating the polar counterparts.

- **A Wideband Multi-Mode Digital Doherty Transmitter in 40nm CMOS**
  Chapter 4 combines the introduced multi-mode operation approach in chapter 3 with an off-chip Doherty combiner to improve the overall system efficiency over a wideband. The design and implementation details and the measurement results of the first-ever wideband multi-phase DTX in a two-way Doherty configuration are presented. Multi-phase operation is utilized to compromise the polar and Cartesian features by mapping the I/Q baseband signals into two non-orthogonal basis vectors with reduced relative phase difference, and magnitudes defined based on an appropriate I/Q mapping described in chapter 3. Consequently, this approach yields reduced complex loading compared to a Cartesian DTX resulting in relatively phase-independent efficiency behavior. Moreover, a wideband and efficient DTX is achieved by employing reactance compensated parallel-circuit push-pull class-E DPA, combined with a wideband Marchand balun-based inverted two-way Doherty power combiner exploiting re-entrant coupled lines with independent second-harmonic control.

- **A Wideband Four-Way Doherty Bits-In RF-Out CMOS Transmitter**
  Chapter 5 elaborates on the system-/circuit-level design considerations and extensive measurement results of the first fully-digital four-way Doherty transmitter. Two novel techniques, the 50%-LO signed I/Q interleaved up-converter and a compact four-way Doherty combiner, are proposed to achieve spectrally pure operation and enhance the deep back-off efficiency. The conventional phase selector operation with different clock duty-cycles is explained to understand their limitations. The proposed signed I/Q interleaved up-converter addresses these issues by exploiting global 50%-LO clocks, phase modulated by the sign-bits, along with a new single-sideband I/Q digital up-converter. This method's DTX quadrant selection (sign-mapping operation) is realized in two steps: 1) Global 50% duty-cycle quadrature clock mapping and 2) Local I/Q up-conversion and I/Q interleaving. Furthermore, the systematic approach to designing the four-way power combining network is comprehensively explained. Moreover, the TX architecture is described, followed by a demonstration of the measurement results.

- **A 2×1-D Digital Predistortion Technique**
  Chapter 6 establishes a fundamental knowledge of a digital TX's non-linearities and how to rectify them. Accordingly, a straightforward modified constellation-mapping DPD technique is introduced. Specifically, this DPD process can be deduced as an individual 1-D mapping of two I and Q signals, i.e., 2×1-D. Particularly, the DPD does not necessitate an exhaustive 2-D search of the complete constellation diagram due to the orthogonality of the I and Q path. The same DPD algorithm has been applied to the four-way Doherty DTX (described in chapter 5), and its measurement results are presented.

- **Conclusion**
  Chapter 7 concludes the main findings of this dissertation and presents suggestions for future developments.

Chapter 2

Transmitter Architectures Fundamentals

A digital baseband signal can be transformed into an amplitude- and phase-modulated RF signal using various TX circuitry options. Although many unconventional approaches were initially developed decades ago, some recently came to light again as researchers realized their potential for digital-intensive applications. Additionally, the PA, one of the most crucial circuit blocks in terms of overall efficiency and linearity, has design requirements that are directly influenced by the choice of TX architecture. Although it is debatable that the PA can be entirely digital because it must generate an analog output signal, the PA architecture can nevertheless play a significant role in attaining the overall goal of reducing the number of analog circuitry.

2.1 Transmitter Performance Metrics

2.1.1 Efficiency

Efficiency affects the handheld device's battery life, therefore it is crucial to the whole TX system. The power efficiency establishes a connection between the RF power delivered to the load, and the drawn power from the DC supply. In the literature, it is quantified for an output stage/module by drain efficiency (DE) or power-added efficiency (PAE). The following are the official definitions [9]:

$$DE(\%) = 100 \times \frac{P_{RF_{Out}}}{P_{DC}} \tag{2.1}$$

$$PAE(\%) = 100 \times \frac{P_{RF_{Out}} - P_{in}}{P_{DC}} \tag{2.2}$$

The system efficiency (SE), which applies to both digital and analog TXs, is determined by the ratio of the output RF power to the sum of the total DC supply power consumption of the entire TX chain:

$$SE(\%) = 100 \times \frac{P_{RF_{Out}}}{P_{DC-PowerCells} + P_{DC-All\ Blocks}} \tag{2.3}$$

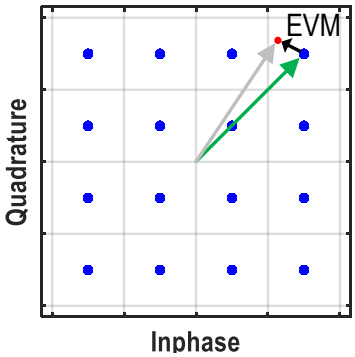


Figure 2.1: EVM illustration.

2.1.2 Signal Accuracy

An extremely critical metric of the transmitter performance that measures the channel's signal accuracy is the EVM. It is characterized as the vector error on the I/Q plane between the intended constellation point and the actual transmitted value (Fig. 2.1). The following is how it is defined mathematically:

$$EVM(dB) = 20\log\left(\frac{\sqrt{\frac{1}{N_{tot}}\sum_{i=1}^{N_{tot}}\left(I/Q_{BB,Out}(i) - I/Q_{BB,Ideal}(i)\right)^2}}{\sqrt{\frac{1}{N_{tot}}\sum_{i=1}^{N_{tot}}\left(I/Q_{BB,Ideal}(i)\right)^2}}\right) \tag{2.4}$$

Where $I/Q_{BB,Out}$ is the measured output baseband complex signal and $I/Q_{BB,Ideal}$ is the ideal input baseband complex signal. As it detects all types of impairments, including nonlinearity, I/Q imbalance, DC offsets, local oscillator (LO) phase noise (PN), and Additive white Gaussian noise (AWGN), EVM is an extensive metric and essential debugging tool in evaluating the transmitted signal fidelity. These impairments are manifested in the constellation diagram of Fig. 2.2. Larger output amplitudes are compressed by nonlinearity, mainly in the constellation's outermost points. I/Q imbalances tend to skew the constellation in a parallelogram shape, whereas DC offsets cause the entire constellation to deviate from its ideal center reference. PN rotates the whole constellation, while AWGN tends to scatter the constellation's points. These nonidealities independently affect the eventual EVM performance as formulated in (2.5). Therefore, as a rule of thumb, to obtain an EVM of better than -35dB, each factor must contribute with an accuracy of better than -46dBc.

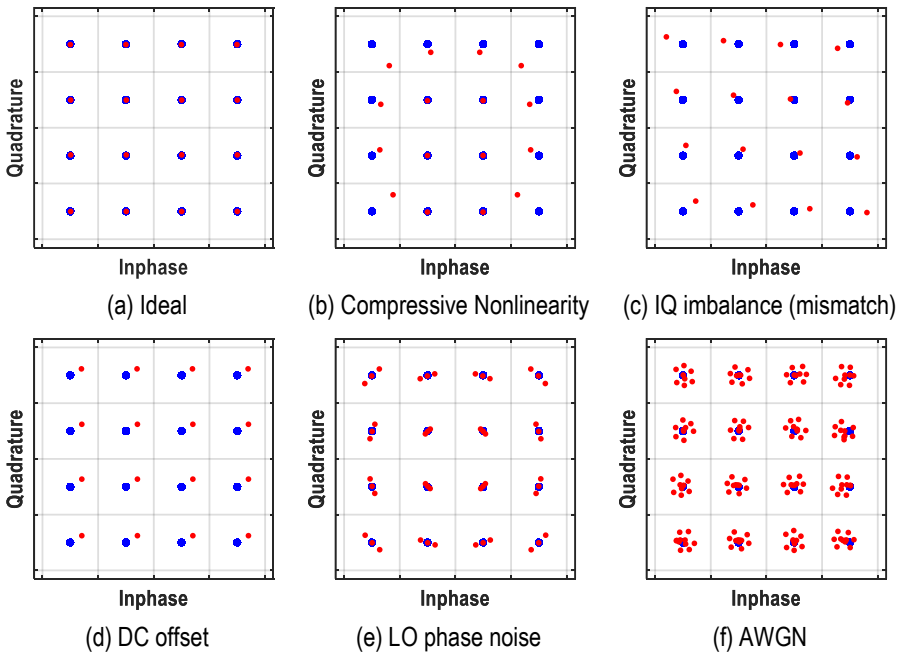


Figure 2.2: Implications of TX impairments on a 16-QAM constellation.

$$EVM_{TX} = \sqrt{\begin{array}{l}\left(10^{\text{IQ-Image }/20}\right)^2 + \left(10^{\text{LO-Leak }/20}\right)^2 \\ + \left(10^{QN/20}\right)^2 + \left(10^{AM-AM/20}\right)^2 + \\ \left(10^{AM-PM/20}\right)^2 + \left(10^{PN/20}\right)^2 + \cdots\end{array}} \tag{2.5}$$

2.1.3 Spectral Purity

2.1.3.1 Adjacent Channel Power Leakage Ratio (ACLR)

In order to guarantee reliable communication and peaceful coexistence between users, the total amount of leaked power from an assigned channel to its adjacent channel (or alternate adjacent) should be reduced to the greatest extent possible. This metric is evaluated by the adjacent channel leakage ratio (ACLR), or alternatively adjacent channel power ratio (ACPR), and mathematically can be expressed as:

$$ACLR = \frac{\int_{f_1}^{f_2} PSD(f)df}{\int_{f_C-B/2}^{f_C+B/2} PSD(f)df} \tag{2.6}$$

where the power spectral density of signal is represented by $PSD(f)$, the carrier frequency and channel bandwidth are respectively denoted by f_C and B, while $f_2 - f_1$ specifies the width of the adjacent channel. Third-order intermodulation (IM3) is the main contributor of ACLR, yielding significant spectral regrowth around the channel for wideband signals like OFDM. This feature necessitates TX with high linearity.

2.1.3.2 Spectrum Emission Mask (SEM)

The upper limits of spurious emissions are specified by the spectrum emission mask (SEM). LO spurs owing to a phase-locked loop (PLL) performance, or intermodulation products, can generate spurious tones [10, 11]. Each wireless standard specifies its SEM, which a transmitter must adhere to in order to be certified.

2.2 Transmitter Architectures

Wireless TX can be categorized in Cartesian or polar architectures. Each architecture has its advantages and disadvantages in terms of bandwidth, power efficiency, and linearity. Pragmatically, the intended application significantly influences the choice of the best architecture. As we will explore in the following sections, an analog transmitter architecture can be implemented in an equivalent digital counterpart, i.e., its digital transmitter version.

2.2.1 Analog-Intensive Transmitters

2.2.1.1 Analog Cartesian TX

The Cartesian, also known as I/Q architecture [10, 12], has traditionally been the outrunner of RF TXs. In comparison to alternative topologies like outphasing or polar, it can support the broadest modulation bandwidth. The foundation of Cartesian TXs is the idea that each RF waveform, $RF(t)$, can be split into an in-phase (I) and/or quadrature (Q) component using trigonometric identities:

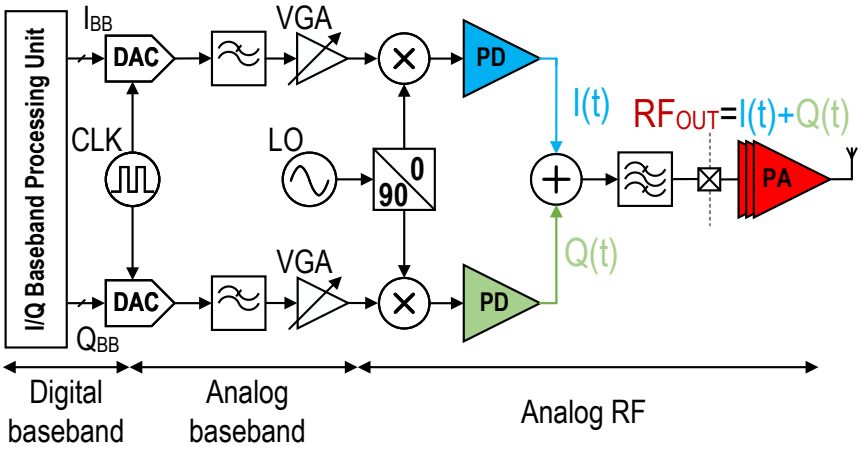


Figure 2.3: Direct conversion Cartesian TX.

$$\begin{aligned} RF(t) &= A(t)\cos(\omega_C t + \phi(t)) \\ &= I_{BB}(t)\cos(\omega_C t) + Q_{BB}(t)\sin(\omega_C t) \end{aligned} \tag{2.7}$$

$$I_{BB}(t) = A(t)\cos(\phi(t)) \tag{2.8}$$

$$Q_{BB}(t) = A(t)\sin(\phi(t)) \tag{2.9}$$

The amplitude and phase information are denoted by $A(t)$ and $\phi(t)$, respectively. $\omega_C = 2\pi f_C$ is the carrier frequency, while $I_{BB}(t)$ and $Q_{BB}(t)$ are respectively the in-phase and quadrature components. As explained below, it is possible to further categorize the Cartesian architecture into *direct conversion* or *heterodyne*, depending on the number of up-conversion stages.

Direct Conversion Cartesian TX: in this topology, up-conversion is accomplished in one stage by adjusting the LO equal to the carrier frequency. In a reasonably compact area, a clean spectrum can be achieved centered on the LO and its harmonics. Figure 2.3 illustrates the typical block diagram of such a TX. Using two DACs, the DSP's output digital I/Q data are transformed into corresponding analog form. These analog signals are subsequently low-pass filtered to suppress the sampling spectral replicas produced during the signal reconstruction. A variable gain amplifier (VGA) is incorporated after the filters to

enable accurate gain control to comply with the power control requirements of the intended standard. High-gain VGAs are simpler to implement at low frequencies, but if they are not precisely matched, the asymmetries after up-conversion could result in undesired spectra. To confront this issue, a single VGA can be used. An I/Q or single-sideband (SSB) mixer, which significantly suppresses the lower sideband of the up-converted waveform, performs the up-conversion. After combining the up-converted signals, the output power is increased using a linear PA (e.g., class-AB) to the level required by the antenna for transmission. A bandpass filter (BPF) is interposed between the PA and the antenna to eliminate any distortion produced by the PA. Off-chip surface acoustic wave (SAW) filters must be used here due to the high-quality requirements for this filter, which may increase the cost of the entire system and restrict the frequency-agile nature. To alleviate the PA's intermodulation requirements (IIP_3 and IIP_2), a BPF could optionally be incorporated beforehand [13]. Despite its competent performance, direct conversion has some downsides as well. Firstly, the constellation accuracy is inevitably distorted by any I/Q mismatch in the pathways leading (and including) the mixers, which degrades the achievable EVM. Additionally, if the sideband image is not attenuated sufficiently, it may distort nearby terminals. Effectively, a high image rejection ratio (IRR) (e.g., above 30dB) ensures a decent EVM performance [10]. On the other hand, DC offsets in the baseband cause carrier leakage in the spectrum quantified by the relative carrier leakage (CL), which is an essential metric in wireless communication. This effect can exacerbate the in-band distortion in wireless applications, where depending on the employed power control scheme, the power of the LO may mask the up-converted signal. Moreover, The mixer's baseband ports must be linear enough to prevent the output from compressing before the PA. However, a good design rarely has this problem. The impact of LO pulling is the primary drawback of direct conversion [14, 15]. Given that the PA and LO operate at the same frequency, the high voltage swings may couple to the VCO through the substrate and "injection pull" it away from the intended carrier frequency. This effect results in a "detuned" VCO, which oscillates periodically between various frequencies, resulting in undesirable spurs in the output spectrum. The phenomenon, known as "superharmonic pulling", causes LO pulling even when the PA operates at a multiple of the LO frequency [10]. Multiple strategies are typically used to mitigate LO pulling, including differential PA design, symmetrical layout, large LO swings, high PLL loop gain, high Q VCO tank use, and frequency mixing or dividing to offset the LO from the final RF carrier.

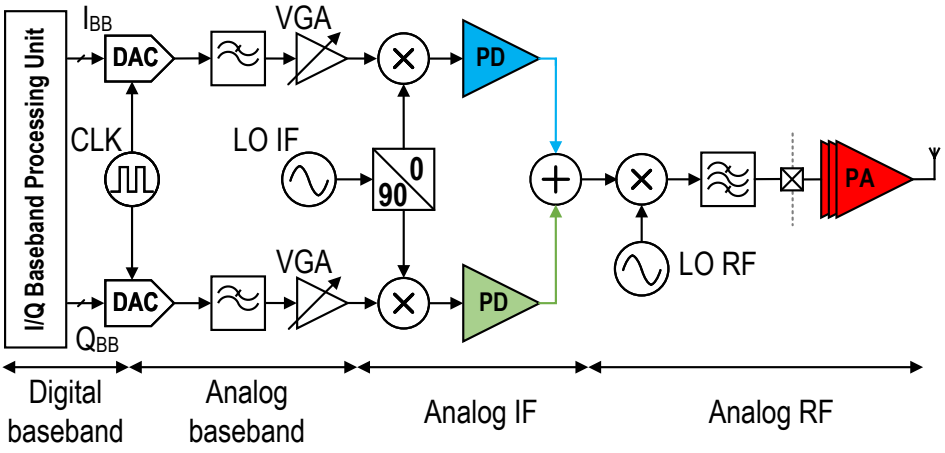


Figure 2.4: Heterodyne Cartesian TX.

Heterodyne Cartesian TX: the heterodyne design achieves up-conversion in two steps. An SSB mixer is used to up-convert the signal to an intermediate frequency (IF), followed by another up-conversion to the desired RF carrier. Consequently, the impact of LO pulling is drastically diminished because the IF frequency is located far from the carrier. Improved I/Q gain and phase matching are other benefits of up-converting to IF. However, As indicated in Fig. 2.4, a BPF, named as an image reject filter (IRF), is now required to be used prior to the PA to suppress the RF mixer's lower sideband image and the carrier leakage [16]. Nevertheless, this architecture's biggest drawback is the challenge of handling the mixing spurs caused by the harmonics of two LOs (at IF and RF). Therefore, this design is less desirable for multi-standard/multi-band TX due to the demanded rigorous frequency planning, which leads to stricter filtering requirements and less system design freedom [10].

2.2.1.2 Analog Polar TX

The polar TX in its most pure form, also referred to as Envelope Elimination and Restoration (EER) transmitter, was initially proposed by Khan in 1952 [17]. The key idea here is to decompose the envelope and phase of signal, and apply the constant envelope phase signal to a highly efficient switched-mode PA (SMPA). These amplifiers can attain a theoretical efficiency of 100% by using the power source as a switch rather than a current source [18,19]. As illustrated in Fig. 2.5, this is accomplished by modulating the SMPA's supply with

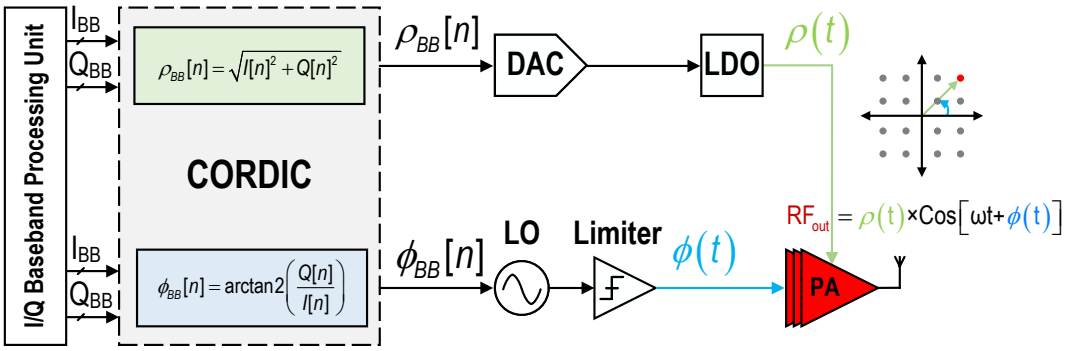


Figure 2.5: Polar or EER TX.

the envelope signal. The envelope modulator is implemented by a low-dropout regulator (LDO) [12], which produces a dynamic envelope RF waveform where the peak efficiency is always maintained by the PA operating in saturation.

$$RF(t) = \rho(t)\cos(\omega_C t + \phi(t)) \tag{2.10}$$

Although the theoretical system efficiency of polar modulation is relatively high, its practical (silicon) implementation has some drawbacks. For instance, spectral regrowth happens if the phase and envelope routes have any delay mismatch. [10, 12, 20]. This can be detrimental, as it is challenging to ensure accurate time alignment between the two different paths due to their different hardware nature. A limiter is deployed between the PA and the phase modulator to guarantee high efficiency from the SMPA. AM/PM distortion may occur if the limiter's bandwidth is insufficient [10, 12]. To prevent PM leaking to the output, the envelope amplifier's offset should be less than 0.2% of the peak $\rho(t)$ [21]. Another factor contributing to PM leakage is the fractional coupling of the phase-modulated signal from the VCO to the SMPA [21]. Moreover, the excessive bandwidth requirement in the phase and envelope pathways is one of the most severe drawbacks of this architecture for multiple standards applications. The digital I/Q bits are converted during signal decomposition to polar format using a coordinate rotation digital computer (CORDIC) block [22]. CORDIC transforms the I/Q data to envelope and phase as follows:

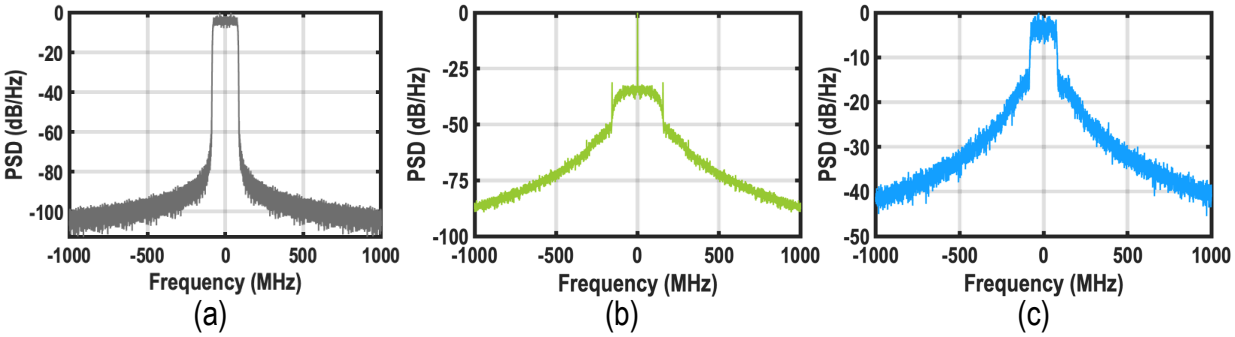


Figure 2.6: Signal bandwidth expansion of a polar TX. (a) I/Q(t) (b) $\phi(t)$ (c) $\rho(t)$.

$$\rho(t) = \sqrt{I_{BB}^2(t) + Q_{BB}^2(t)} \tag{2.11}$$

$$\phi(t) = \text{sign}\arctan\left(\frac{Q_{BB}(t)}{I_{BB}(t)}\right) \tag{2.12}$$

The non-linear nature of these transformations yields substantial spectral expansion. As depicted by simulations in Fig. 2.6, in contrast to a Cartesian implementation, the required circuits' instantaneous bandwidth in both paths is significantly larger. The polar structure cannot handle wide modulation bandwidths due to bandwidth restrictions imposed by some blocks, such as LDOs or DC-DC converters. Utilizing an offset-PLL as a phase modulator is an effective technique to ensure reduced out-of-band (OOB) noise emissions [23]. Nevertheless, a direct trade-off exists between the large instantaneous bandwidth required for accurate signal recombination at the antenna and the PLL's loop bandwidth for noise emissions.

2.2.2 Digital-Intensive Transmitters

2.2.2.1 Why Digital?

The attractive advantages of intensive CMOS technology scaling are the motion engine of digitizing the TX chain. Digital IC designs are predominantly implemented in CMOS technology since, comparing all other semiconductor technologies, CMOS technology is the most economical at massive production volumes. Notably, production costs are roughly cut in half when an (existing) digital design is transferred to the next CMOS node. This feature

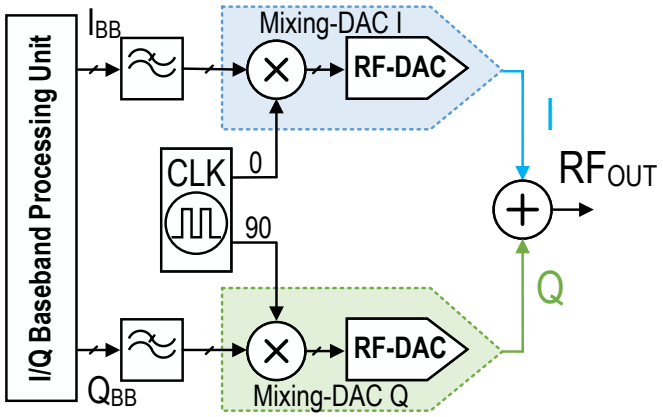


Figure 2.7: Block diagram of a Cartesian DTX.

is primarily attributable to Moore's law that every subsequent CMOS technology generation provides devices with a shorter channel length, enabling faster switching and higher gate density. Correspondingly, the digital gate delay decreases, and processing capability improves for a given silicon area. Additionally, as capacitance and supply voltage decrease, the dynamic power dissipation for a given operation is reduced.

Integrating as many RF functionalities into "digital-friendly" CMOS technologies, to the greatest extent possible, has been a central focus of the contemporary RFIC design. This trend paves the path toward using digital approaches to address various RF deficiencies (e.g., PA nonlinearity) through techniques like digital pre-distortion (DPD) [24]. Additionally, it provides the best system reconfigurability and makes it simpler to interface with the DSP core. As a result, shifting towards circuit topologies that favor digital signals over analog signals is the primary trend in modern CMOS RF IC design.

2.2.2.2 Digital Cartesian TX

Figure. 2.7 depicts a conceptual illustration of a Cartesian DTX. The digital Cartesian TX operates as follows. The I and Q digital samples drive the corresponding RF-DAC converters, which generate two RF signal components whose amplitudes are effectively proportional to the corresponding I/Q digital inputs. The desired composite RF output is subsequently created by combining the two amplitude-modulated RF components. After that, the output

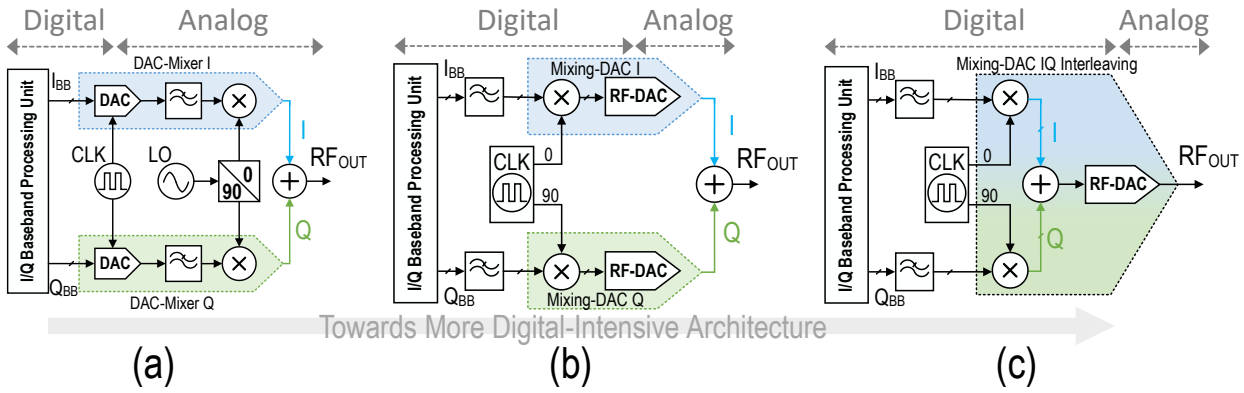


Figure 2.8: The evolution of digital-intensive Cartesian transmitters. (a) Analog Cartesian, (b) mixing of the data and LO in the digital domain, and (c) digital I/Q combination.

is either directed to an efficient power amplifier or the antenna. It should be noted that the phase of the resulting RF signal is implicitly determined by the fact that the Q and I RF-DACs are 90° out of phase.

The evolution of digital-intensive Cartesian transmitters is demonstrated in Fig. 2.8. The first structure, as shown before, is analog Cartesian. The second structure shows one step towards a digital-intensive transmitter, in which the functionalities of the analog to digital converters (DACs), low pass filters (LPF), and mixers in its analog counterpart are superseded with two parallel-connected RF-DACs for I and Q, wherein the mixing operation is also carried out in the digital domain. But still, the I and Q signals are combined in the analog domain. This structure is called the non-interleaving I and Q combination. The arrangement of Fig. 2.7(a) and (b) has several drawbacks. First, due to using separate DACs for I and Q, the power generation capability of the output stage is reduced. Moreover, it can lead to excessive parasitics at the output, attenuating the RF signal amplitude at high frequencies. Second, each I and Q path may not be well-matched, limiting the intrinsic image-rejection ratio (IRR). Finally and most importantly, the overlap between the I and Q signals causes unwanted I and Q interaction, degrading the I/Q modulator EVM and linearity. To move towards a more digitally intensive realization and address the challenges of analog-intensive I and Q RF signals summation, the I and Q combination can also be carried out in the digital domain, called the interleaving structure (Fig. 2.7(c)).

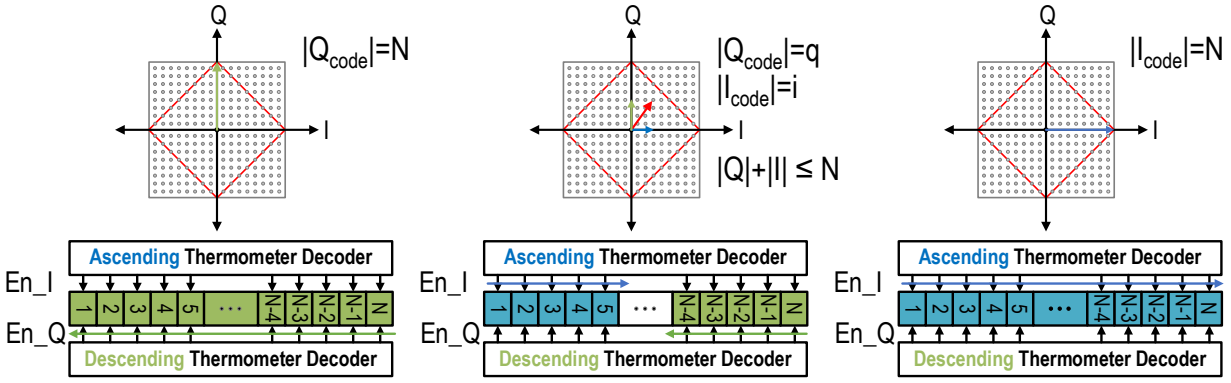


Figure 2.9: The I/Q-sharing concept.

It is worth mentioning that I/Q interleaving differs from I/Q-sharing, in which I and Q signals are not enabled simultaneously for the DPA cell. In this structure, as shown in this conventional example (Fig. 2.9), a diamond-shaped clipping technique is applied in the digital domain to minimize the chance of I/Q overlap and the impact on distortion. This means that the signal path only allows complex signals that satisfy $|I| + |Q| \leq N$ to go through, while other signal levels outside the boundary will be clipped. As a result, the I/Q overlap is avoided by correcting the baseband signal itself. If we have totally N unit cells, the I decoding scheme is in ascending order: if $|I_{Code}| = i$, the I enable signals from 1 to i are turned on. On the other hand, the Q decoding scheme is in descending order: if $|Q_{Code}| = q$, the Q enables signals from N to $N - q + 1$ to be turned on.

2.2.2.3 Digital Polar TX

Figure 2.10 exhibits a transmitter architecture compatible with digital nanoscale CMOS technology [25,26]. The LO is realized as an all-digital PLL (ADPLL) that produces a phase or frequency modulated digital clock carrier [26]. The clock is fed into an RF-DAC, which generates an RF output whose envelope varies proportionally with respect to the amplitude control word (ACW) or ρ. Hence, the architecture is termed a digital polar TX. Accordingly, "*digital polar*" TX is a name given to this architecture.

Wideband signals often cannot be handled by closed-loop phase modulators, e.g., an (AD)PLL, due to the loop bandwidth and VCO (DCO) nonlinearity. Although many meth-

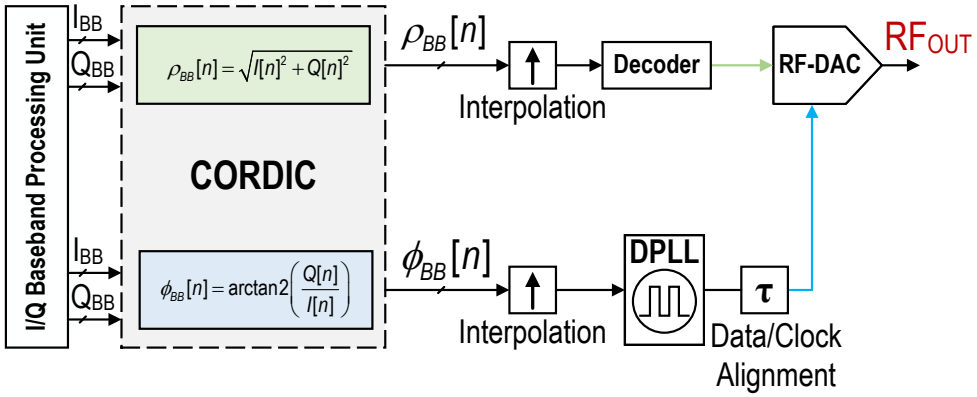


Figure 2.10: Block diagram of a polar DTX.

ods, including two-point injection and digital pre-distortion, have been developed to enhance the bandwidth [27], it is still extremely challenging for (AD)PLL-based approaches to achieve a PM bandwidth of 500MHz to support a 100MHz transmitted signal in a polar architecture. Various open-loop approaches have been put forth to achieve a wider bandwidth. They principally combine and/or multiplex multiple LO signals with different static phases to modulate the phase outside the PLL loop [28]. A direct-digital synthesizer (DDS) is a straightforward way to realize a wideband open-loop phase modulator. Nevertheless, compared to a PLL-based phase modulator, which is commonly employed for narrower modulation bandwidths, a DDS can consume significantly more power.

Typically, a high-efficiency DC-DC converter with an LDO serves as the AM modulator in an analog polar TX. Such a design has a substantially lower bandwidth than the quadrature mixer, typically used as the signal modulator in a Cartesian TX. Additionally, a transmit signal's bandwidth can only be half of an AM modulator's bandwidth (or only one-fifth of a phase modulator's, which is even smaller) due to bandwidth expansion in a polar structure. Here, amplitude modulation based on an RFDAC can also be employed to overcome this restriction. By eliminating the DAC, LPF, and DC-DC converter/LDO from the AM path in an analog polar TX (Fig. 2.5), an array of sub-PA cells can be directly controlled by the digital AM code-word (ACW) to modulate the output power [29]. In this approach, a digital PA (DPA), which operates as a direct amplitude modulator, combines the amplitude

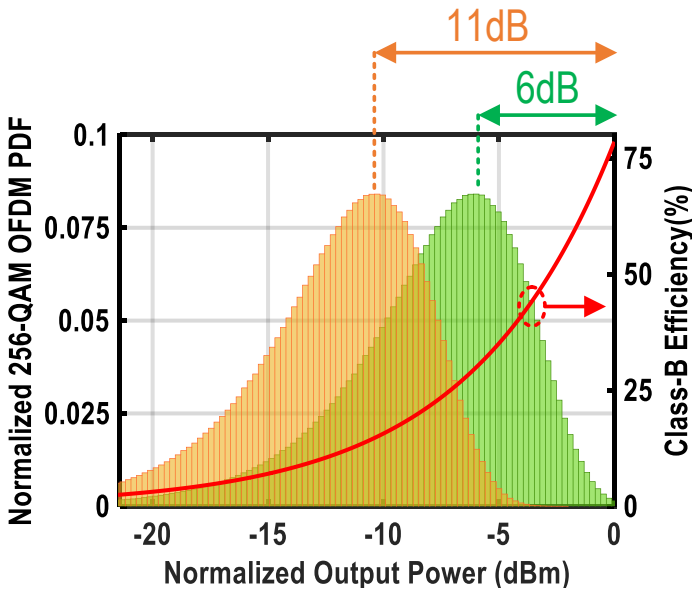


Figure 2.11: CW-efficiency of a class-B PA and the PDFs of an 11dB and a 6dB PAPR signal vs. normalized PBO level.

modulator and the PA into a cohesive block.

As previously stated, high power efficiency is a key benefit of the polar configuration. However, it is impractical for very wideband signals due to the significant bandwidth expansion resulting from CORDIC's nonlinear signal processing. This issue has prompted researchers to consider alternative architectures.

2.3 Efficiency Enhancement Techniques

Modern wireless communication standards in recent years are led to new challenges in designing power amplifiers. These communication systems employ spectral-efficient high data rate modulation schemes. The instantaneous power of these envelope-modulated signals rapidly changes over a relatively large dynamic range. The signal's peak power to its average power is called the PAPR, which can reach up to 12 dB in modern communication systems. The PA must operate at back-off power to avoid clipping of the signal peaks. Unfortunately, the PAs only provide high efficiency when operating close to their maximum output power.

In order to achieve high-efficiency performance for high PAPR signals, these PAs must be driven into saturation, which results in clipping of the signal peaks and distortion of the signal envelope. Consequently, the PA must operate at power back-off condition to avoid distortion. However, without any further action, the efficiency decreases dramatically with power back-off, which makes the PA inefficient when amplifying signals with high PAPR levels. For example, an idealized class-B amplifier's efficiency at maximum output power is 78.5%, which falls to its half at a 6dB output back-off. Low-efficiency PA operation leads to increased power consumption, yielding higher base station cooling costs and a mobile device battery life deterioration. PA efficiency enhancement techniques, such as the Doherty amplifier, Chireix outphasing TX, and envelope tracking (ET), have been developed to tackle this issue. The dynamic modulation of the load is the foundation for techniques such as the Doherty amplifier and PAs employing dynamic tunable matching networks. Other methods, like ET, rely on the bias adaptation concept, which dynamically adjusts the drain bias of the PA based on the input power level to achieve improved efficiency during back-off operation with a fixed load.

2.3.1 Doherty

The Doherty amplifier, initially proposed by W. H. Doherty in 1936 [30], is one of the most well-known and popular efficiency enhancement techniques due to its relatively straightforward circuitry and the significant efficiency improvement it can accomplish at back-off operation. Moreover, when it is carefully implemented, it can also be linear [31]. The active load-pull concept is the foundation of its operation, in which an RF current supplied from a second, phase-coherent amplifier dynamically modulates the load of an amplifier.

The active load-pull principle is illustrated in Fig. 2.12, where two amplifiers, represented by current sources generating the currents I_1 and I_2, are connected by a power combiner network to a common load R_L. In the most simple case, this voltage across the common load is expressed as

$$V_L(t) = R_L \left(I_1 + I_2\right) \tag{2.13}$$

The amplifier on the left observes the load impedance as

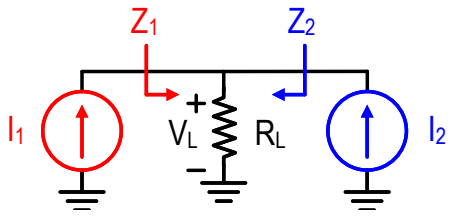


Figure 2.12: An illustration of the active load-pull concept.

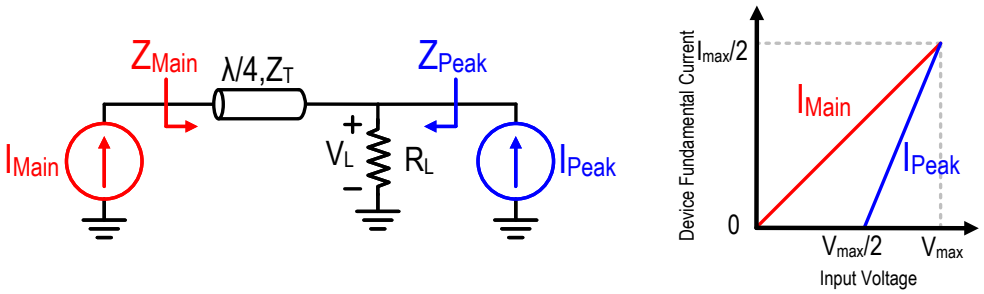


Figure 2.13: The simplified Doherty amplifier schematic and the corresponding main and peaking devices' fundamental current amplitudes.

$$Z_1 = R_L\left(\frac{I_1 + I_2}{I_1}\right) = R_L\left(1 + \frac{I_2}{I_1}\right) \tag{2.14}$$

whereas the other amplifier's impedance can be expressed as

$$Z_2 = R_L\left(\frac{I_1 + I_2}{I_2}\right) \tag{2.15}$$

It is clear from (2.14), altering the amplitude and/or phase of the current I_2, produced by the amplifier on the right, can change (pull) the impedance seen by the other amplifier on the left, Z_1. For instance, Z_1 can be changed to a higher value if I_2 and I_1 are in phase and to a lower value if they are out of phase.

The Doherty amplifier operates on the same concept discussed above. As illustrated in Fig.2.13, it consists of two PAs, the main (carrier) and the peaking (auxiliary) devices, which share a common load and are interconnected by a quarter-wave impedance inverter. The auxiliary device is designed to be activated at a specified input power level (activation point), generally a 6dB back-off from the maximum total output power of the (symmetrical)

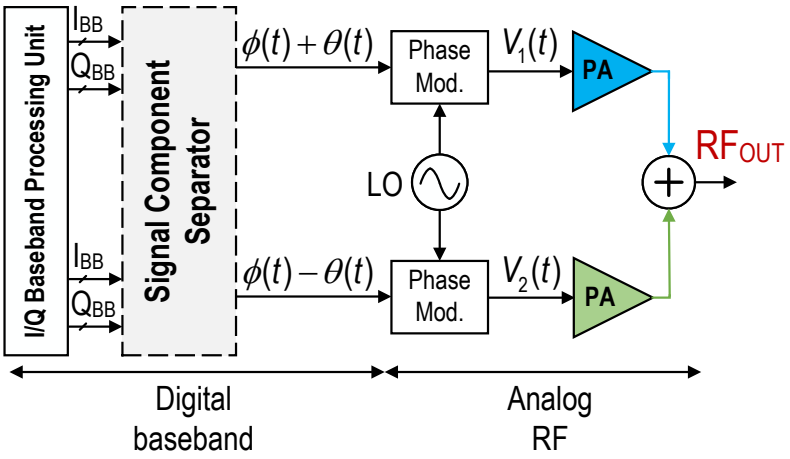


Figure 2.14: Outphasing or LINC efficiency enhancement architecture.

Doherty amplifier. Then it starts to generate the current I_2 that increases until it reaches the same maximum value of I_1 at full power operation as depicted in Fig.2.13. The auxiliary device turns off and produces no RF current below the activation point. The quarter-wave impedance inverter plays an essential role in transforming the increasing common load impedance into a decreasing impedance seen by the main device as the peaking current I_2 increases. We will discuss such an implementation in Chapter 5.

2.3.2 Outphasing

In 1935 [32], Chireix introduced the Linear Amplification with Non-linear Components (LINC) method, commonly referred to as outphasing. A LINC TX block diagram is displayed in Fig. 2.14. This design is founded on the notion that every waveform with variable amplitude can be split into two waveforms with constant envelope, which can then be amplified independently by high-efficiency SMPAs (class-D, E, etc.). Accordingly, the following relations are established:

$$RF(t) = \rho(t)\cos(\omega_C t + \phi(t)) = V_1(t) + V_2(t) \tag{2.16}$$

$$V_1(t) = \frac{V_p}{2}\sin(\omega_C t + \phi(t) + \theta(t)) \tag{2.17}$$

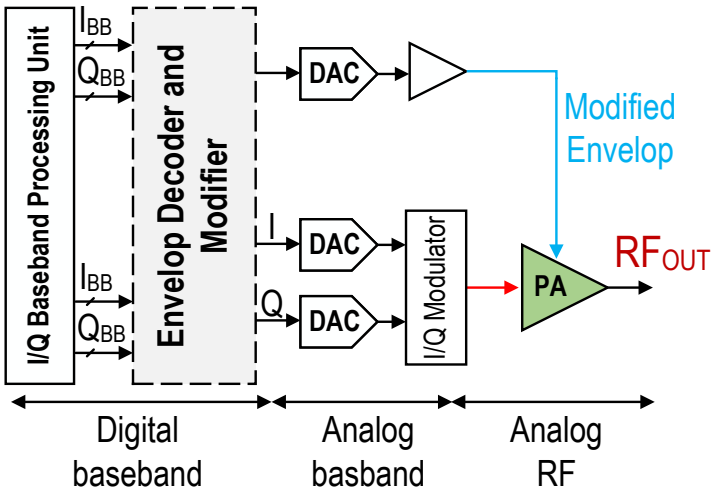


Figure 2.15: Envelope Tracking (ET) efficiency enhancement architecture.

$$V_2(t) = -\frac{V_p}{2}\sin(\omega_C t + \phi(t) - \theta(t)) \tag{2.18}$$

$$\theta(t) = \sin^{-1}\left(\frac{V_{env}(t)}{V_p}\right) \tag{2.19}$$

Where V_p is the envelope signal's peak amplitude, $\rho(t)$, and $\theta(t)$ is referred to as the outphasing angle. The word "*outphasing*" refers to the angle formed by the vectors $V_1(t)$ and $V_2(t)$, which is denoted by the symbol $\theta(t)$. The aforementioned non-linear transformations can be computed in advance using DSP technology and stored in memory [33, 34]. Compared to polar architecture, the outphasing design has the benefit of not requiring supply modulation. Therefore, there is no need for a fast DC envelope regulator, which may be the main performance bottleneck in the system [10].

In contrast, outphasing calls for two PAs. The interaction between the two PAs, besides the intended load modulation for efficiency enhancement, may lead to considerable output spectrum distortion. Hence, an isolating Wilkinson power combiner is sometimes employed to tackle this issue. According to microwave theory, a lossy three-port network can be impedance matched and completely isolate two of its ports from one another. [35]. Unfortunately, the Wilkinson combiner effectively removes the load modulations due to the

outphasing action and significantly degrades the system's power efficiency. Similar to polar modulation, signal separation's non-linear properties introduce severe bandwidth expansion of the modulated signal. As a result, this structure is only appropriate for narrow-band applications. [36, 37].

2.3.3 Envelop tracking

Envelope tracking (ET) has been hailed as a prospective approach for wireless TXs owing to its potential to enable wideband modulation bandwidth and provide good linearity and efficiency even at large power back-off levels [38]. As demonstrated in Fig. 2.15, the TX comprises an I/Q modulator, which in contrast to its polar counterpart, does not suffer from bandwidth expansion. The drain voltage of a linear PA is modulated by the envelope signal, which is generated at the baseband. Compared to the previously discussed EER topology, the envelope signal here does not need to correspond perfectly to the original signal envelope. In fact, it provides the required (drain) voltage with some headroom to compromise efficiency and linearity. Although the deployment of envelope tracking for mobile applications has been successfully demonstrated [39, 40], further effort is required to overcome the challenges of wideband base station applications, specifically for the supply regulators.

2.4 Conclusion

This chapter briefly discusses the most commonly used transmitter performance metrics to quantify the performance of different transmitter implementations. Following that, descriptions and evaluations of traditional analog TX line-up architectures, including polar and analog Cartesian techniques, are provided regarding modulation bandwidth. After laying the groundwork, the next step is to develop their modern digital-intensive polar and Cartesian counterparts. These new notions pave a promising path to higher integration levels while opening up new opportunities to improve wireless systems' performance dramatically. After that, this chapter highlights the demand to enhance PBO efficiency and provides a quick overview of the most common efficiency enhancement methods. We are prepared to enter the realm of cutting-edge DTXs after laying this foundation of wireless systems.

Chapter 3

A Wideband Energy-Efficient Multi-Mode CMOS Digital Transmitter

This chapter is written based on [41, 42].

3.1 Introduction

In the past two decades, wireless communication networks such as cellular and WLAN have been considerably intertwined with our daily lives. To conform with the insatiable appetite for higher data rates of new applications, the next-generation communication systems exploit spectrally efficient modulations and carrier aggregation, in which channels can be juxtaposed, leading to large modulation bandwidths [43]. Moreover, high RF bandwidth is also essential to realize ubiquitous RF transmitters/receivers (TXs/RXs). Hence, they must be frequency agile to cover multiple frequency bands. On the other hand, high energy efficiency is critical for increased battery life and improved user experience.

To address these demands, digital transmitters (DTXs) have emerged as favorable alternative architectures as they supplant the functionality of the conventional analog-intensive TXs circuit blocks, such as; the baseband digital-to-analog converters (DAC), low-pass filter, mixer, and power amplifier (PA) with a single radio-frequency digital-to-analog converter (RF-DAC) block [29,44–55]. These DTXs consist of many unit cells comprising digital filters, bit-wise implicit mixers, and their digital power amplifiers (DPA). Consequently, contrary to their analog-intensive counterparts, DTXs can fully benefit from nanoscale CMOS integration scalability to provide compact die areas with higher power efficiency due to the high-speed switching nature of the core power devices, even in the face of reduced supply voltages. Moreover, these DTXs provide excellent reconfigurability and frequency agility, making them suitable for multi-mode/multi-band communication standards owing to their fully digital-intensive operation. Furthermore, it is also more straightforward to integrate these TXs as part of a system-on-a-chip (SoC) with non-RF fully digital circuits, such as modems and various application processors.

The DTXs are primarily classified as a polar or Cartesian (Quadrature/I/Q) architecture, as illustrated in Fig. 3.1. The former is based on the polar coordinate signal consisting of the amplitude (ρ) and phase (ϕ) information. In contrast, the latter operates based on the Cartesian coordinate system comprising the in-phase (I) and quadrature-phase (Q) information. In a polar DTX [29,44–49], the two baseband eigen vectors of $\rho\,[n]$ and $\phi\,[n]$ are generated from the baseband I/Q signals using a COordinate Rotation DIgital Computer (CORDIC). A digital PLL (DPLL) produces a phase or frequency modulated digital clock carrier employing the $\phi\,[n]$ information. The clock is fed to the RF-DAC unit cells that

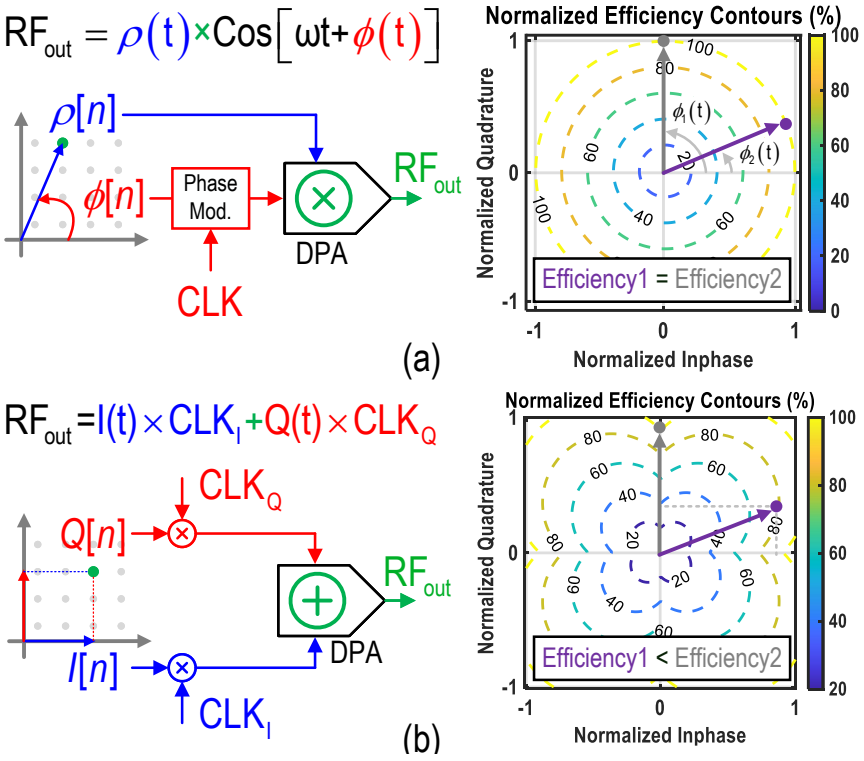


Figure 3.1: (a) Polar, (b) Cartesian DTX architectures. Their operational concepts and corresponding efficiency contours in the I/Q plane.

produce an RF output whose envelope is substantially proportional to the amplitude control word (ACW) or $\rho\,[n]$ by the ON/OFF switching of the RF-DAC unit cells.

Generally, the efficiency of the entire DTX chain is strongly dependent on its DPA efficiency. Since the phase component has a constant envelope, high-efficiency DPAs, for example, class-E, can be used in polar DTXs. They can operate efficiently since, as is clear from the drain efficiency diagram (Fig. 3.1(a)), their drain efficiency (DE) can be high and constant over the phase. However, converting the I/Q data to polar form using a CORDIC is complicated, as described in [12, 56, 57]. This is caused due to: 1) the complex implementation algorithm; 2) the high-frequency operation of the iteration within the CORDIC; 3) the CORDIC circuit nonlinearity in terms of quantization noise, and 4) the large signal bandwidth required for the phase path (about ten times), and the amplitude path (about

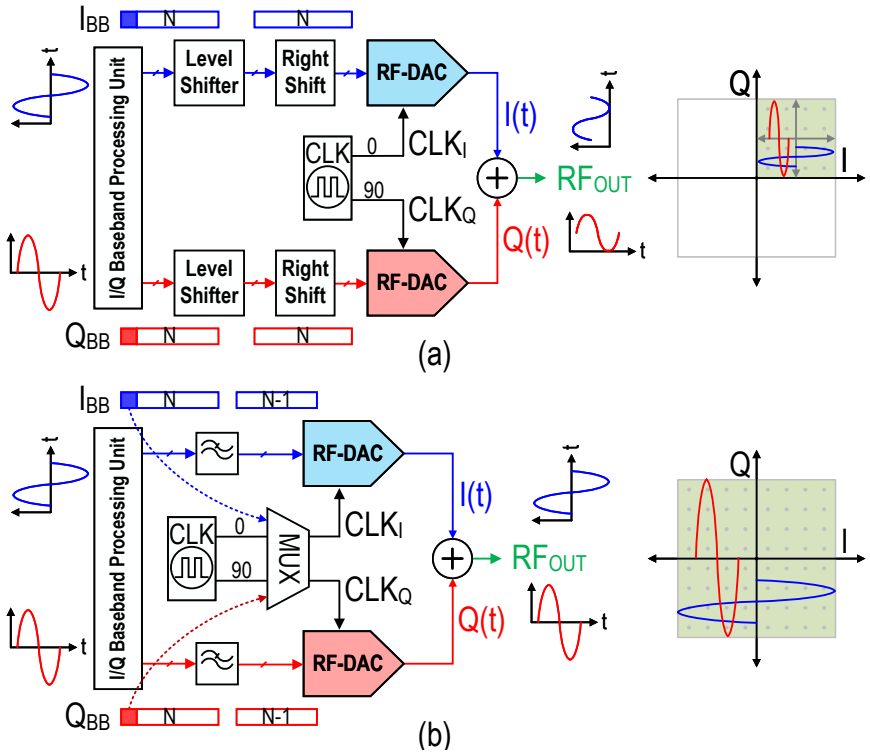


Figure 3.2: Concept of (a) un-signed and (b) signed DTXs, and their I/Q plane coverage comparison.

two to three times) when compared with the original signal bandwidth. More importantly, the phase and amplitude paths must recombine at their final DPA cells without any delay mismatch to avoid spectral regrowth.

In contrast, Cartesian DTX [50–55, 58] variants do not require a CORDIC, thus significantly lowering the computing cost. The upconverted $I_{\mathrm{BB}}/Q_{\mathrm{BB}}$ digital samples drive their respected RF-DACs that produce two RF signal components whose amplitudes are ideally proportional to the respective I/Q digital inputs. Subsequently, the two amplitude-modulated RF components are combined at the output to produce the desired composite RF signal. To facilitate a more digitally intensive realization, the I/Q combining can also be carried out in the digital domain while sharing a single power cell [50, 59]. Due to the linear summation of I/Q signal paths, Cartesian DTXs can manage large modulation bandwidth. Moreover, since the structure is equivalent for both the I and Q paths, synchronization is

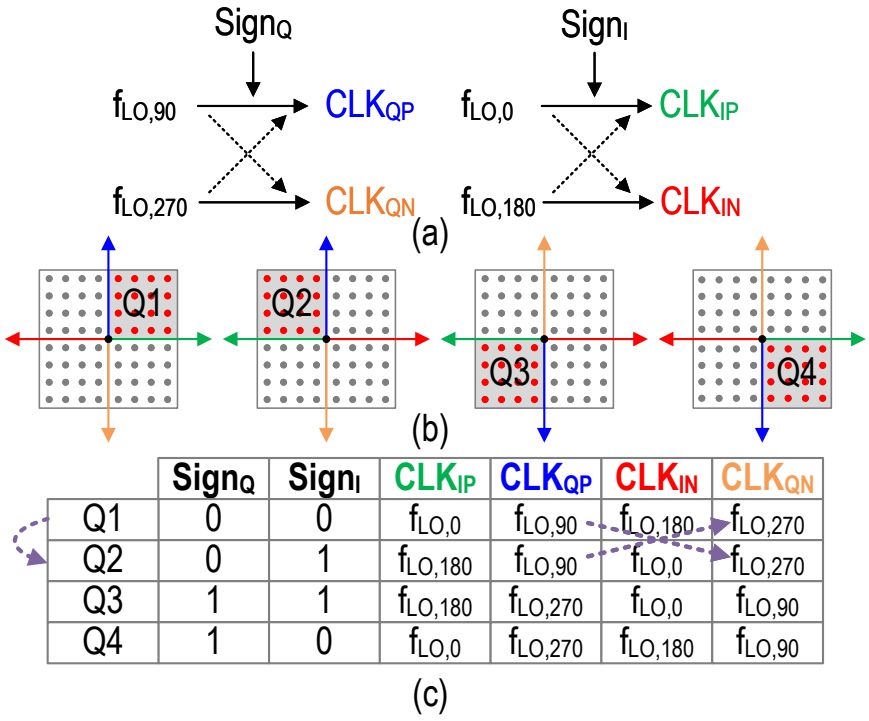
straightforward. Nevertheless, their drain efficiency (Fig. 3.1(b)) is on average lower than for their polar counterparts due to the linear summation of the two orthogonal I/Q vectors, yielding a 3-dB output power penalty at the orthogonal axes when using separate I and Q RF-DACs, and a $1/\sqrt{2}$ drop in efficiency at the diagonal axes.

By briefly reviewing polar and Cartesian architectures, we conclude that there is a great need for an alternative DTX structure to operate more efficient than Cartesian TX implementations while still managing large modulation bandwidth. In fact, such a DTX architecture should compromise polar and Cartesian features. In [41], we have recently introduced a multi-mode DTX capable of operating in both Cartesian and multi-phase modes to target applications requiring high spectral purity, low EVM, and large modulation bandwidth in a highly energy-efficient operation. This chapter elaborates on the DTX architecture, its analysis and system-/circuit-level design considerations, and measurement results. This chapter is organized as follows. First, Section 3.2 introduces the proposed multi-mode DTX. Next, Section 3.3 unveils the DTX modes of operation. The detailed DTX architecture and circuit design and implementation, together with its off-chip matching network, are provided in Section 3.5. Subsequently, Section 3.6 exhibits extensive measurement results of the prototype. Finally, in Section 3.7, we conclude this chapter.

3.2 Multi-Mode Digital Transmitter

3.2.1 Signed vs. Un-signed DTX Operation

The proposed multi-mode DTX is based on signed I/Q data. First, let us explore the difference between signed and un-signed DTX operations. The digital baseband I/Q data can be represented in signed or un-signed formats. The signed I/Q data consist of two explicit sign bits (Sign_I and Sign_Q) to distinguish the positive and negative I/Q values. Nevertheless, their un-signed counterpart does not explicitly have sign bits, thus effectively covering only the positive numbers. The N-bit signed data comprise one sign bit and N–1 bits representing the magnitude of the data, which is not the case in the N-bit un-signed scenario, as depicted in Fig. 3.2. Generally, a signed I/Q format is exploited in the digital baseband processing unit. However, the arrays of power cells in an RF-DAC can only process the magnitude part of its I/Q digital bitstreams. Therefore, the sign of I/Q data must be engaged in the RF-



	Sign$_Q$	Sign$_I$	CLK$_{IP}$	CLK$_{QP}$	CLK$_{IN}$	CLK$_{QN}$
Q1	0	0	$f_{LO,0}$	$f_{LO,90}$	$f_{LO,180}$	$f_{LO,270}$
Q2	0	1	$f_{LO,180}$	$f_{LO,90}$	$f_{LO,0}$	$f_{LO,270}$
Q3	1	1	$f_{LO,180}$	$f_{LO,270}$	$f_{LO,0}$	$f_{LO,90}$
Q4	1	0	$f_{LO,0}$	$f_{LO,270}$	$f_{LO,180}$	$f_{LO,90}$

(c)

Figure 3.3: (a) Conventional Cartesian DTX phase selector (sign-bit) operation. (b) Cartesian DTX four-quadrant and (c) its corresponding related swapped complementary clock pairs.

DAC phase operation to adequately cover all four quadrants of the constellation diagram. To address this issue, the RF-DAC can adopt the following approaches.

In the first approach (Fig. 3.2(a)), similar to the conventional I/Q baseband DAC operation, the I/Q RF-DAC exploits the un-signed I/Q bitstreams [60, 61]. Subsequently, they are converted to un-signed representations employing digital level shifters and logical right-shifts for proper signal scaling. Eventually, the I/Q un-signed data drive a pair of I/Q DACs. As illustrated in Fig. 3.2(a), in this context, the whole constellation diagram is shifted to the first quadrant by adding a DC offset to I and Q data. It is worth mentioning that an un-signed version is similar to the techniques used in a conventional current-steering DAC. Circuit-wise, the RF-DAC is often implemented based on arrays of double-balanced mixer unary cells. In this fully differential architecture, the ZERO state is achieved at mid-code wherein $D_I = D_Q = 2(N-1)-1$, which is located at the equilibrium point of the differential

pair at which RF_{OutP} and RF_{OutN} cancel each other, which is prone to mismatch. In this regard, as shown in Fig 3.2(a), by dismissing three quadrants of the constellation diagram, the inherent swing of the system is halved. Consequently, the output current of each cell does not become zero as the function of input data code, but it can only change phase (0°, 90°, 180°, and 270°). Therefore, the related efficiency and linearity performance are similar to a (analog) class-A PA in which 100% of the input signal is used (conduction angle = 360°), and the active element remains conducting all the time.

In the second approach (Fig. 3.2(b)), the I/Q RF-DAC unitizes the signed I/Q bitstreams [62–64]. This approach contrasts sharply compared with the conventional DAC operation. Here, due to exploring of the phase information along with its magnitude, we can utilize the signed I/Q data and directly apply them to the RF-DAC unit cells. The signed version requires a 1-bit phase modulator for each LO phase. In this respect, the sign information is retrieved by swapping the complementary quadrature clocks' phases using a multiplexer. Circuit-wise, the signed RF-DAC is often implemented using arrays of single-balanced mixer unary cells. In this approach, to represent the ZERO state, all power cells can be turned off. Therefore, the key advantage of this configuration is that the ZERO output is well-defined, and less prone to the mismatch between two paths, i.e., RF_{OutP} and RF_{OutN}. Moreover, the swing is doubled in the signed I/Q approach, leading to higher output power. Most importantly, the signed I/Q operation replicates an efficiency behavior similar to class-B, which is in contrast with the un-signed I/Q operation. Therefore, signed I/Q operation in DTX is preferable to achieve higher output power and overall system efficiency.

3.2.2 Signed Cartesian Operation Principle

The concept of using a Cartesian phase selector when working with signed I/Q data is demonstrated in Fig. 3.3. The phase selector operates directly on the quadrature clock signals ($f_{LO,0}$, $f_{LO,90}$, $f_{LO,180}$, $f_{LO,270}$). As illustrated, depending on the four states of the I/Q sign-bits, the related complementary clock pairs can be swapped. These phase-modulated LO clocks are then directly mixed with the up-sampled baseband data (I_{BB}, Q_{BB}) to cover the targeted constellation quadrants. For example, in the case of transition from the first quadrant ($Sign_Q$=0, $Sign_I$=0) to the second one ($Sign_Q$=0, $Sign_I$=1), since the sign of I is changed, the corresponding complementary clocks, CLK_{IP} and CLK_{IN}, are swapped (see

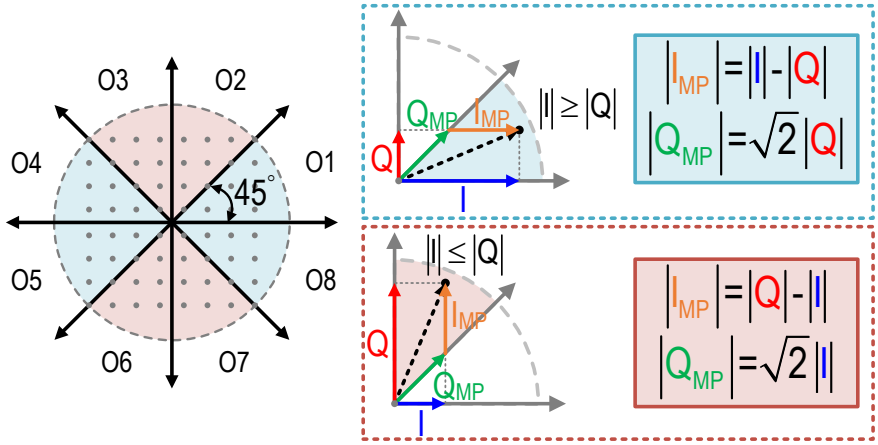


Figure 3.4: Multi-phase (eight-phase) operation baseband data mapping depending on the corresponding octant.

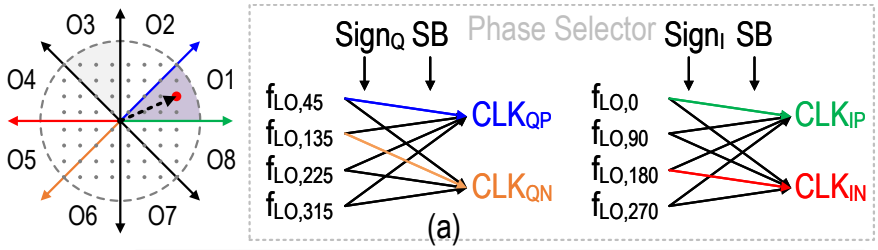
table in Fig. 3.3(c)). The rectangular-shaped RF LO clocks can be written using the Fourier series:

$$\Pi(t, T_0, d, \theta) = \sum_{n=-\infty}^{n=\infty} \frac{sin(\frac{n\pi d}{T_0})}{n\pi} e^{\frac{-j2n\pi}{T_0}(t-\frac{\theta}{2\pi}+\frac{d}{2})} \tag{3.1}$$

where T_0 is upconverting clock period, d is the duty cycle, and θ represents the relative time shift. The differential RF waveform is synthesized using the following equation:

$$\begin{aligned} RF_{Out} = &|I(t)| \times [\Pi(t, T_0, d, \theta_{\mathrm{I}}) - \Pi(t, T_0, d, \theta_{\mathrm{I}} + \pi)] \\ &+ |Q(t)| \times [\Pi(t, T_0, d, \theta_{\mathrm{Q}}) - \Pi(t, T_0, d, \theta_{\mathrm{Q}} + \pi)] \end{aligned} \tag{3.2}$$

Where $\theta_{\mathrm{I}} - \theta_{\mathrm{Q}} = \pm\frac{\pi}{2}$ depending on the quadrant. Therefore, the resulting waveform is created based on two orthogonal signals. The vectors related to $|I(t)|$ and $|Q(t)|$ provide the (positive or negative) amplitude of in-phase and quadrature signals. However, the negative values of $I(t)$ and $Q(t)$ are implemented by a 180° phase shift in the RF carrier clocks. Consequently, the desired $I(t)$ and $Q(t)$ vectors are created by recombining amplitude-modulated $|I(t)|$ and $|Q(t)|$ signal and the corresponding 1-bit resolution, two-state (bang-bang) phase-modulated I/Q LO clocks on the sign of the I/Q baseband signals.



	Sign$_Q$	Sign$_I$	SB	CLK$_{IP}$	CLK$_{QP}$	CLK$_{IN}$	CLK$_{QN}$
O1	0	0	0	$f_{LO,0}$	$f_{LO,45}$	$f_{LO,180}$	$f_{LO,225}$
O2	0	0	1	$f_{LO,90}$	$f_{LO,45}$	$f_{LO,270}$	$f_{LO,225}$
O3	0	1	1	$f_{LO,90}$	$f_{LO,135}$	$f_{LO,270}$	$f_{LO,315}$
O4	0	1	0	$f_{LO,180}$	$f_{LO,135}$	$f_{LO,0}$	$f_{LO,315}$
O5	1	1	0	$f_{LO,180}$	$f_{LO,225}$	$f_{LO,0}$	$f_{LO,45}$
O6	1	1	1	$f_{LO,270}$	$f_{LO,225}$	$f_{LO,90}$	$f_{LO,45}$
O7	1	0	1	$f_{LO,270}$	$f_{LO,315}$	$f_{LO,90}$	$f_{LO,135}$
O8	1	0	0	$f_{LO,0}$	$f_{LO,315}$	$f_{LO,180}$	$f_{LO,135}$

(b)

Figure 3.5: (a) Multi-phase (eight-phase) DTX phase selector (sign-bit) operation utilizing Sign_I, Sign_Q and Sector-Bit (SB). (c) Associated swapped complementary clock pairs based on the operating octant.

3.2.3 Signed Multi-phase Operation Principle

The signed Cartesian operation employs two orthogonal $I(t)$ and $Q(t)$ vectors. However, this technique can be extended to a more generalized multi-phase operation by mapping I/Q baseband signals into two non-orthogonal vectors [65–68]. In light of this, the phase modulation resolution of the corresponding up-converting clock signals is increased to four or more phases (2-bit or more). For example, as presented in Fig. (3.4), an eight-phase operation can be utilized. This architecture compromises polar and Cartesian features by mapping the I/Q signals into two non-orthogonal basis vectors with 45° relative phase difference and the magnitudes based on the corresponding octant defined as

$$\begin{cases} I + jQ = I_{MP} + Q_{MP}\left(\dfrac{1+j}{\sqrt{2}}\right) & |I| \geq |Q| \\ I + jQ = jI_{MP} + Q_{MP}\left(\dfrac{1+j}{\sqrt{2}}\right) & |I| < |Q| \end{cases} \tag{3.3}$$

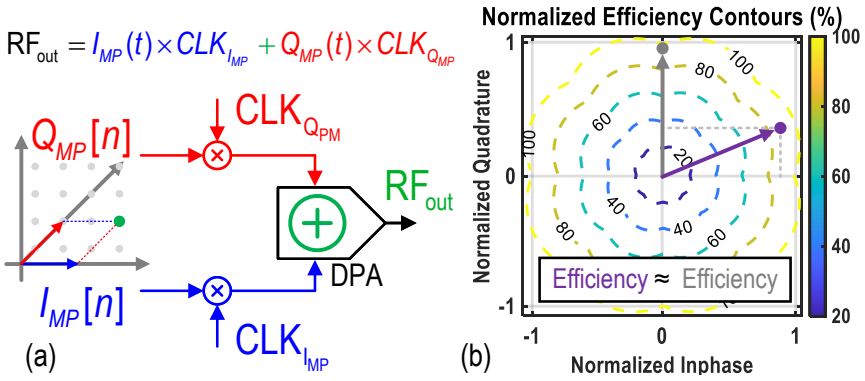


Figure 3.6: (a) Multi-phase DTX operational concept. Its corresponding efficiency contours reduced phase dependency compared to the Cartesian counterpart.

Besides, as illustrated in Fig. 3.5, a phase selector is exploited to modulate the LO clocks properly. As mentioned previously, the phase selector's controlling signals in Cartesian modes are I/Q sign bits. The multi-phase operation modes require 3-bits control signals to cover 8-octant. Two of which are $\text{Sign}_\text{I}/\text{Sign}_\text{Q}$ bits, and the third bit is generated in the digital domain based on the multi-phase mapping operation. Based on these three controlling bits, the associated LO clock pairs can be swapped, and thus the entire eight octants of the constellation diagram are covered.

The RF waveform again consists of the summation of two vectors:

$$\begin{aligned} RF_{Out} = &|I_{MP}(t)| \times [\Pi(t, T_0, d, \theta_{\text{I}_\text{MP}}) - \Pi(t, T_0, d, \theta_{\text{I}_\text{MP}} + \pi)] \\ &+ |Q_{MP}(t)| \times [\Pi(t, T_0, d, \theta_{\text{Q}_\text{MP}}) - \Pi(t, T_0, d, \theta_{\text{Q}_\text{MP}} + \pi)] \end{aligned} \tag{3.4}$$

Where $\theta_{\text{I}_\text{MP}} - \theta_{\text{Q}_\text{MP}} = \pm\frac{\pi}{4}$ depending on the octant. As illustrated in Fig. 3.6, this architecture inherits the advantages of the Cartesian DTX, such as wideband operation, symmetrical and synchronized I/Q paths with a drain efficiency behavior that approaches the polar case. As presented in Fig. 3.6, the DTX's efficiency enhances by employing two vectors that have a reduced phase difference.

The normalized efficiency per trajectory points of a 256-quadrature amplitude modulation (QAM) orthogonal frequency-division multiplexing (OFDM) signal applied to a polar, a signed Cartesian, and an eight-phase operation DTX and their corresponding normalized efficiency versus normalized output power are depicted in Fig. 3.7. In the polar DTX case,

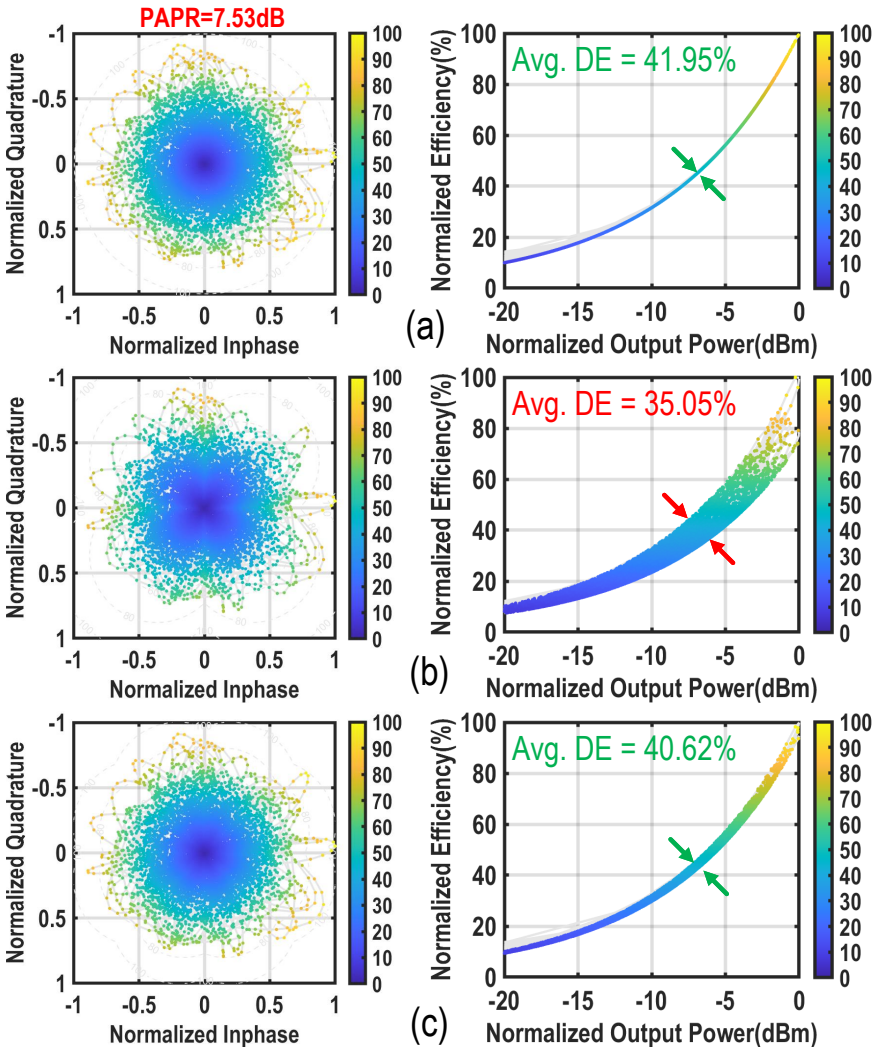


Figure 3.7: Normalized dynamic efficiency contour of a 256-QAM OFDM signal and its associated normalized efficiency versus normalized output power for a (a) polar (b) Cartesian, and (c) eight-phase operation DTX.

thanks to phase-independent efficiency for a given amplitude (Fig. 3.7(a)), its normalized efficiency versus normalized output power is confined, resulting in a relatively high average drain efficiency. Repeating the same experiment for the signed Cartesian scenario, the efficiency plot (Fig. 3.7(b)) is scattered due to its phase-dependent behavior. This feature

results in lower average drain efficiency. In comparison, due to its lower phase-dependency compared to Cartesian, the dynamic efficiency trajectory is more confined for the eight-phase operation (Fig. 3.7(c)), this plot is close to the polar case, resulting in a more acceptable average drain efficiency.

Theoretically, this principle can be extended to more phases [68, 69]. Nevertheless, this would burden the multi-phase clock generator and phase modulator, which increases the complexity while operating at a higher speed, deteriorating the achievable system efficiency of practical implementation.

The implication of the synchronous operation of the ρ and phase ϕ in a polar DTX, as well as the sign-bits and un-signed data in Cartesian and multi-phase operation DTXs, are illustrated in Fig.3.9, Fig.3.10, and Fig.3.11, respectively. Simulations show the output spectrum (100MHz), along with the EVM and ACPR, for different signal bandwidths (20MHz, 50MHz, 100MHz, and 200MHz) versus various timing mismatches. Accordingly, the EVM and ACPR degrade by increasing the timing mismatch. This synchronous recombination requirement is more stringent for a polar DTX than a Cartesian or multi-phase architecture, as its EVM and ACPR degrade more for the same timing mismatch and bandwidth. Moreover, consistently, this issue exacerbates by increasing the signal bandwidth.

3.3 Digital Transmitter Modes of Operation

The various operating modes of the proposed DTX are illustrated in Fig. 3.8. It is also including interleaving [51, 59, 60] and non-interleaving modes [62, 70], featuring Cartesian or multi-phase operation utilizing LO clocks with different duty cycles. The multi-phase mode exploits the I/Q to multi-phase mapping. The related LO clocks with the 45° phase difference are selected based on the octant where the I/Q baseband point is located (Fig. 3.5). In a non-interleaving mode (Fig. 3.8(d)), which is conventionally utilized in I/Q RF-DACs, the I and Q path combined in the RF output node, exhibiting an inferior image-rejection ratio. In the interleaving modes (Fig. 3.8(a)), for each DPA, the upconverted baseband signals are digitally combined while sharing a single power cell. Interleaving Cartesian with 25%-LO duty cycle (Fig. 3.8(b)) and interleaving multi-phase operation with 12.5%-LO duty cycle (Fig. 3.8(c)) are named Mode-1 and Mode-3, respectively. On the other hand, in the non-interleaving modes, one of the DPAs is allocated to only I (I_{MP}), and the other DPA

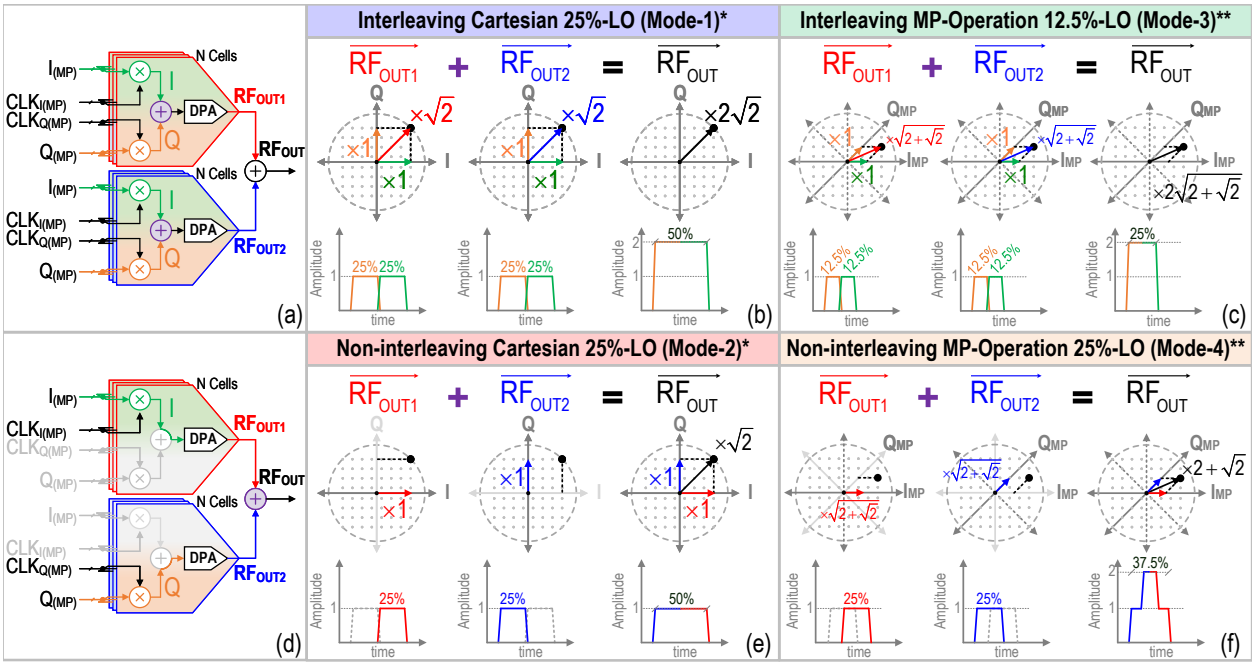


Figure 3.8: The overall operating modes of the proposed DTX. (a) Interleaving and (d) non-interleaving configurations. In the (b) Mode-1 and (e) Mode-2 cases the I/Q vectors are normalized to $\frac{D}{\pi\sqrt{2}}$. In the (c) Mode-3 and (e) Mode-4 scenarios the I_{MP}/Q_{MP} vectors are normalized to $\frac{Dsin\left(\frac{\pi}{8}\right)}{\pi}$.

is assigned to merely Q (Q_{MP}); thus, their outputs are combined at the output drain nodes of the power cell. The non-interleaving Cartesian with 25%-LO duty-cycle (Fig. 3.8(e)) is labeled as Mode-2 while Mode-4 represents non-interleaving multi-phase operation with 25%-LO duty-cycle (Fig. 3.8(f)). These different operational modes are mathematically analyzed and compared in the following.

For simplicity, the differential $RF_{Out}(t)$ in (3.2) and (3.4) can be redefined in a single-ended description as

$$RF_{Out}(t) = |A(t)| \times \Pi(t, T_0, d, \theta_A) + |B(t)| \times \Pi(t, T_0, d, \theta_B) \tag{3.5}$$

Where $|A(t)|$ and $|B(t)|$ generally represent $|I(t)|$ and $|Q(t)|$ in Cartesian modes of

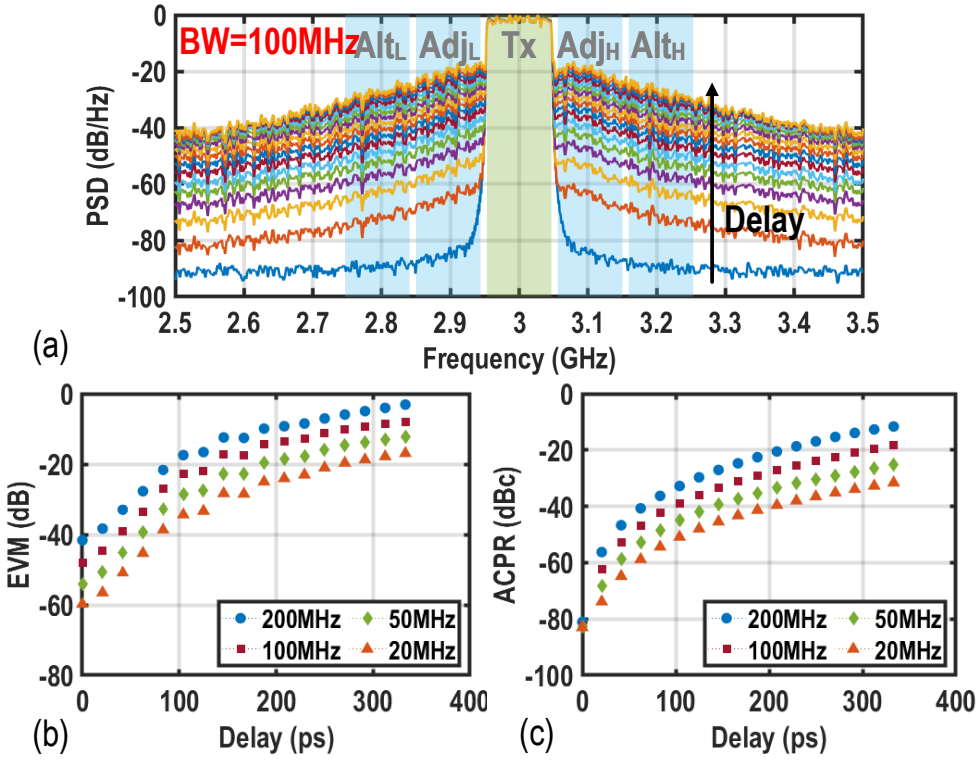


Figure 3.9:Polar DTX: Output spectrum of a 100MHz signal, and (b)-(c) EVM and ACPR of a 20/50/100/200MHz OFDM 64-QAM signal vs. amplitude and phase data timing mismatch.

operation or $|I_{MP}(t)|$ and $|Q_{MP}(t)|$ in multi-phase operation modes, respectively. Fig. 3.12 illustrates the different phases which can be selected based on θ_A and θ_B. Accordingly, depending on the corresponding quadrant in Cartesian (Fig. 3.12(a)), θ_A (θ_B) can be 0 or π ($\frac{\pi}{2}$ or $\frac{3\pi}{2}$), requiring an LO clock signal or its complementary version. Accordingly, shifting LO clocks by, e.g., half an RF cycle, corresponds to a phase shift of 180° in the fundamental component of (3.1). However, in the multi-phase operation scenarios, when the $RF_{Out}(t)$ shifts from one octant to another, θ_A and θ_B are multiplexed between 0, $\frac{\pi}{2}$, π, $\frac{3\pi}{2}$ and $\frac{\pi}{4}$, $\frac{3\pi}{4}$, $\frac{5\pi}{4}$, $\frac{7\pi}{4}$, respectively (Fig. 3.12(b)). Utilizing (3.1), the Fourier series of $RF_{Out}(t)$ can be expanded, and its fundamental component can be obtained by assuming $n = 1$ as

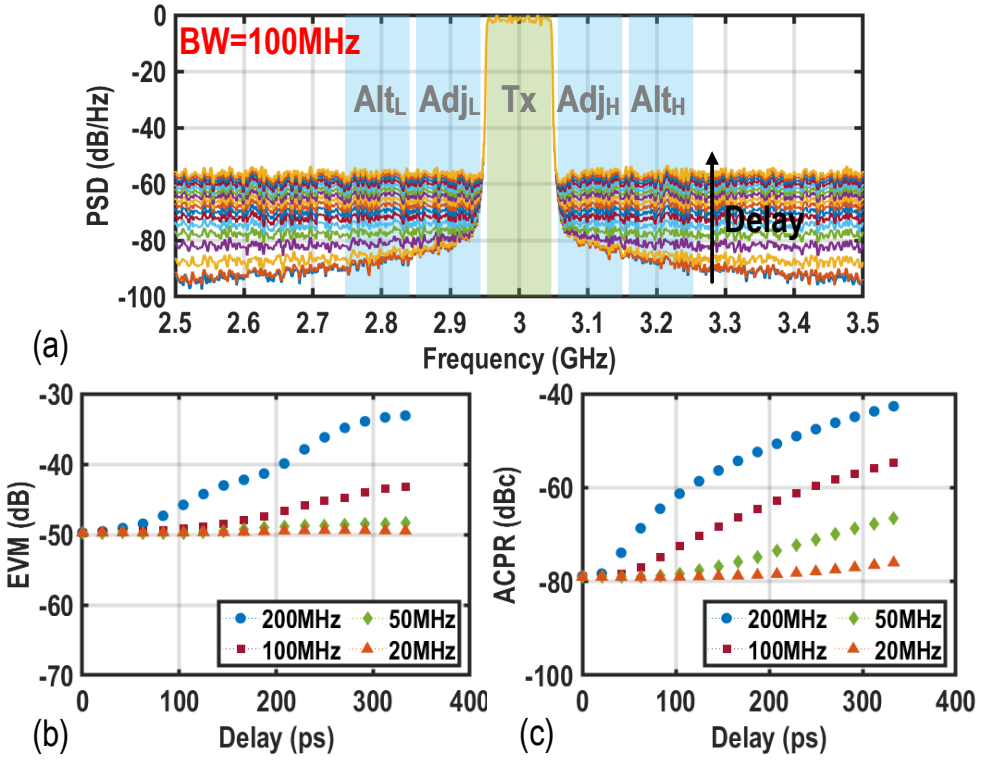


Figure 3.10:Signed Cartesian DTX: Output spectrum of a 100MHz signal, and (b)-(c) EVM and ACPR of a 20/50/100/200MHz OFDM 64-QAM signal vs. sign bits and un-signed data timing mismatch.

$$RF_{Out}(t)|_{n=1} = \frac{sin\left(\frac{\pi d}{T_0}\right)}{\pi}\left(|\mathrm{A}\,(\mathrm{t})|\,\mathrm{e}^{+\mathrm{j}\theta_\mathrm{A}} + |\mathrm{B}\,(\mathrm{t})|\,\mathrm{e}^{+\mathrm{j}\theta_\mathrm{B}}\right)\mathrm{e}^{\frac{-\mathrm{j}2\pi}{\mathrm{T}_0}\left(\mathrm{t}+\frac{\mathrm{d}}{2}\right)} \tag{3.6}$$

With simplifying assumption of $|A\,(t)| = |B\,(t)| = D$, the magnitude of the fundamental component, $|RF_{Out}(t)|_{n=1}$, is calculated as follows

$$|RF_{Out}(t)|_{n=1} = \frac{Dsin\left(\frac{\pi d}{T_0}\right)}{\pi}\left|e^{+j\theta_A} + e^{+j\theta_B}\right| \tag{3.7}$$

Where in Modes-1/-2 and Modes-3/-4, the maximum of D is 1 and $1/\sqrt{2}$, respectively. In the remainder of this section, the DTX's different modes of operation are explained by different clock duty cycles (d) and assumptions of operation in the first quadrant or octant

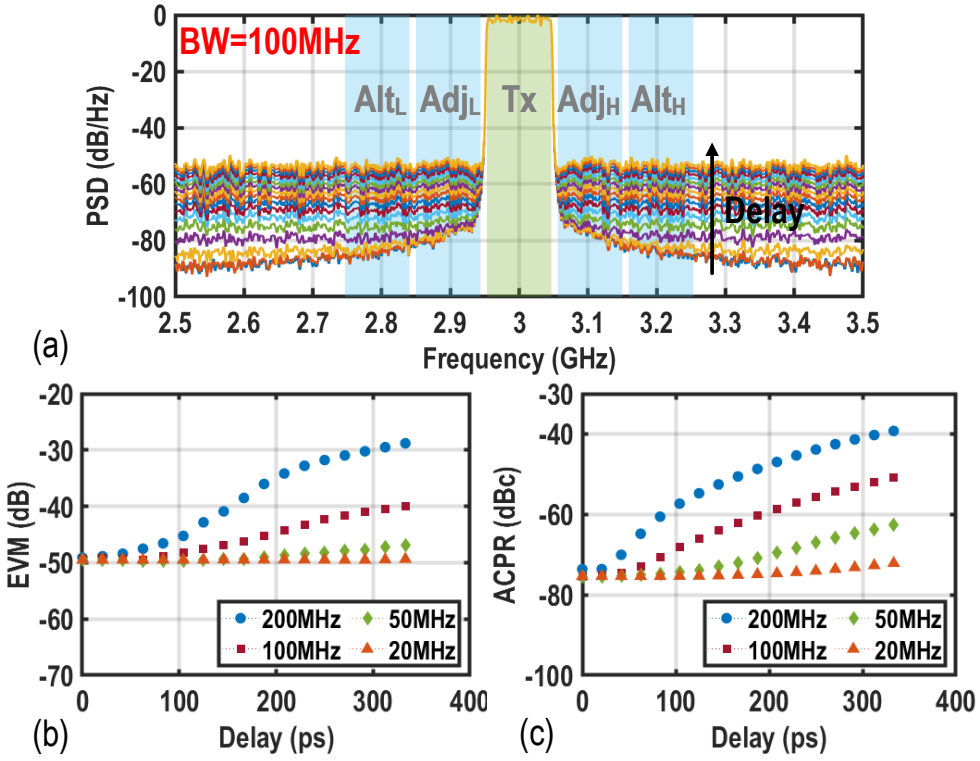


Figure 3.11:Signed eight-phase DTX: Output spectrum of a 100MHz signal, and (b)-(c) EVM and ACPR of a 20/50/100/200MHz OFDM 64-QAM signal vs. sign bits and un-signed data timing mismatch.

of I/Q plane for the Cartesian or multi-phase.

3.3.1 (Non)-interleaving Cartesian with 25%-LO duty-cycle (Mode-1/Mode-2)

According to Fig. 3.12(a), in Cartesian cases, θ_A and θ_B are equal to 0 and $\frac{\pi}{2}$, respectively, while d corresponds to $\frac{T_0}{4}$ for a 25%-LO duty cycle clock. Therefore, for Mode-1 (3.7) yields

$$|RF_{Out}(t)|_{n=1}^{Mode-1} = \frac{Dsin\left(\frac{\pi}{4}\right)}{\pi}\left|1+e^{\frac{+j\pi}{2}}\right| = \frac{D}{\pi} \tag{3.8}$$

In the Mode-2 scenario, since each DPAs is allocated to only I or Q, so the number of

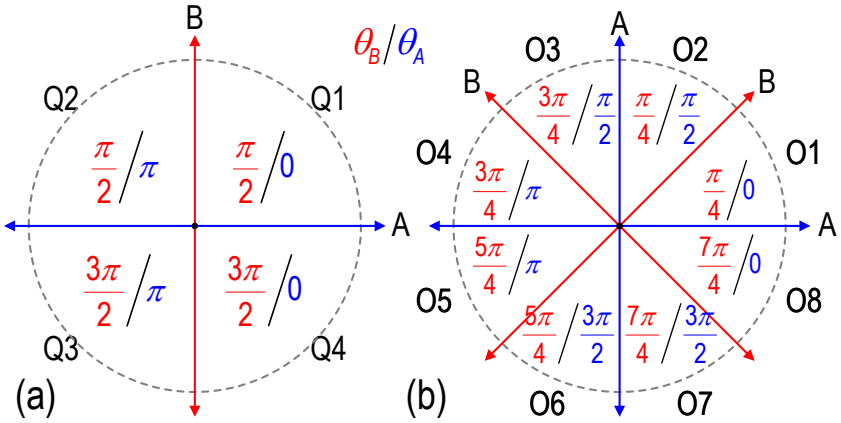


Figure 3.12: Relative phase shift of the rectangular-shaped RF LO associated with (a) Cartesian, and (b) eight-phase operation phase selector.

allocated power cells is halved compared to Mode-1, resulting in $|RF_{Out}(t)|_{n=1}^{Mode-2} = \frac{D}{2\pi}$.

3.3.2 Interleaving multi-phase operation with 12.5%-LO duty-cycle (Mode-3)

In a multi-phase operation case with a 12.5% LO duty cycle in the first octant, d, θ_A and θ_B corespond to $\frac{T_0}{8}$, 0, and $\frac{\pi}{4}$, respectively. Inserting these values in (3.7), after some algebraic abstraction, results in

$$|RF_{Out}(t)|_{n=1}^{Mode-3} = \frac{Dsin\left(\frac{\pi}{8}\right)}{\pi}\left|1+e^{\frac{+j\pi}{4}}\right| = \frac{D}{\pi\sqrt{2}} \tag{3.9}$$

3.3.3 Non-Interleaving multi-phase operation with 25%-LO duty-cycle (Mode-4)

In this case, θ_A, θ_B are the same as Mode-3 while d is equal to $\frac{T_0}{4}$ due to 25% LO duty cycle. Thus, (3.7) can be expressed by

$$|RF_{Out}(t)|_{n=1}^{Mode-4} = \frac{Dsin\left(\frac{\pi}{4}\right)}{\pi}\left|1+e^{\frac{+j\pi}{4}}\right| = \frac{D}{2\pi}\sqrt{\frac{2+\sqrt{2}}{2}} \tag{3.10}$$

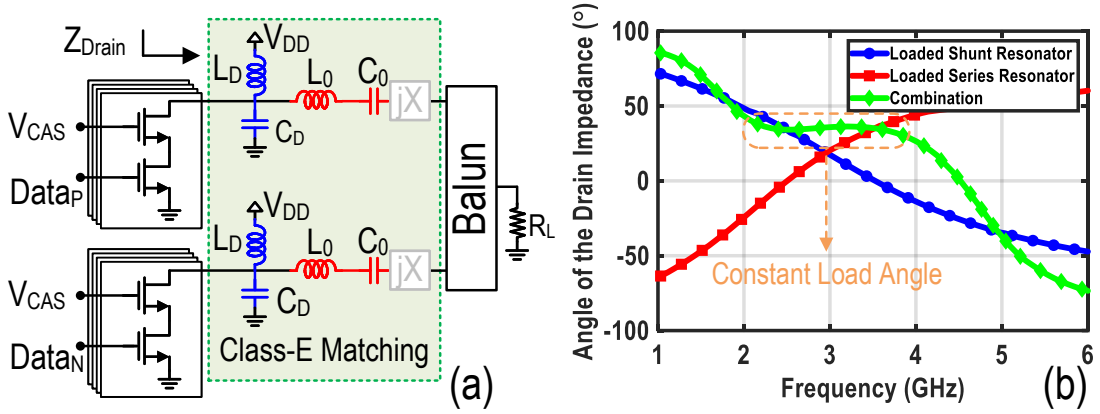


Figure 3.13: (a) General push-pull class-E DTX schematic, and (b) angle of the impedance seen by intrinsic drain [20].

It should be noted that, as mentioned in section 3.3.1, the $\frac{1}{2}$ factor is due to operating in a halved number of power cells in non-interleaving operation.

3.4 Wideband Off-Chip Matching Network

To achieve high efficiency, switch-mode PA topologies can be utilized in the DTX architecture. Among the switch-mode PAs, the class-E DPA has one of the more straightforward load networks. Moreover, it can theoretically provide up to 100% drain efficiency (DE) owing to the non-overlapping drain voltage and current waveforms while absorbing the drain capacitance in its load [71–74]. Furthermore, a planar Marchand balanced-to-unbalanced (balun) employing re-entrant coupled lines [20, 75, 76] is adopted to provide a wideband balanced loading condition from a single-ended antenna load for a push-pull class-E DPA operation. This section describes different techniques to mitigate the bandwidth limiting factors of the designated off-chip matching network.

3.4.1 Load Insensitive Reactance Compensated Parallel-Circuit Class-E DPA

A general schematic for a push-pull class-E power amplifier is plotted in Fig. 3.13(a). The load network consists of a parallel capacitance (C_D), a parallel dc-feed inductance (L_D),

a series tuned circuit (L_0, C_0), and a series reactance (X), which can be either capacitive or inductive, and the load resistance (R_L). Typically, the C_0 can represent the intrinsic device output capacitance and potentially some external circuit capacitance added by the load network. Generally, this structure is called RF-choke class-E for an infinite L_D. In this view, both the shunt susceptance ($B_{Shunt} = \omega.C_{\mathrm{D}}$) and the load reactance ($X_L = j\omega L_0 + 1/j\omega C_0 + jX$) will vary when the DPA operates away from the network's resonance frequency, resulting in violation of the class-E optimum loading condition. To have a wideband RF operation, the load angle seen by the intrinsic drain should remain constant over the designated RF bandwidth. It has been shown that with a finite dc-feed inductance and a normalized resonance frequency of the parallel resonator ($q_D = 1\Big/\omega_0\sqrt{L_D C_D}$) equal to 1.412, the output power for a given V_{DD} and R_L is maximum, and the series reactance X can be zero. This simplified structure is called parallel-circuit class-E [77–79]. It can be observed from Fig. 3.13(b) that the reactance of the series (L_0, C_0) and shunt resonant (L_D, C_D) circuits vary with frequencies, exhibiting an increase in the case of a series circuit and a decrease in the case of a loaded parallel circuit near the resonant frequency. In other words, the slope of the series circuit is positive, while the slope of the shunt circuit reactance is negative around the central frequency. With a proper choice of the circuit elements, a constant load angle seen by the intrinsic drain over a large RF bandwidth is accomplished. This technique results in an optimum $Q_{Series} = 1.026$ [78]. Although the wide drain efficiency and output power bandwidth are achieved for low Q_{Series} values, to achieve high efficiency in an ideal class-E, a high Q_{Series} factor is required to selectively pass the desired fundamental frequency and suppress all harmonics. This issue is overcome by suppressing the even harmonics with a push-pull configuration and a symmetrical (differential) matching network. Therefore, the non-ideal second harmonic impedance characteristics can be significantly enhanced, improving drain efficiency. Consequently, broadband high-efficiency can be realized using differential parallel-circuit class-E with reactance compensation.

3.4.2 Compensated Marchand Balun with Re-entrant Coupled Lines and Second-Harmonic Control

The push-pull class-E DPA is connected to a Marchand coupled transmission-line transformer [20, 80] to form the wideband balun operation of the power combiner. As illustrated in

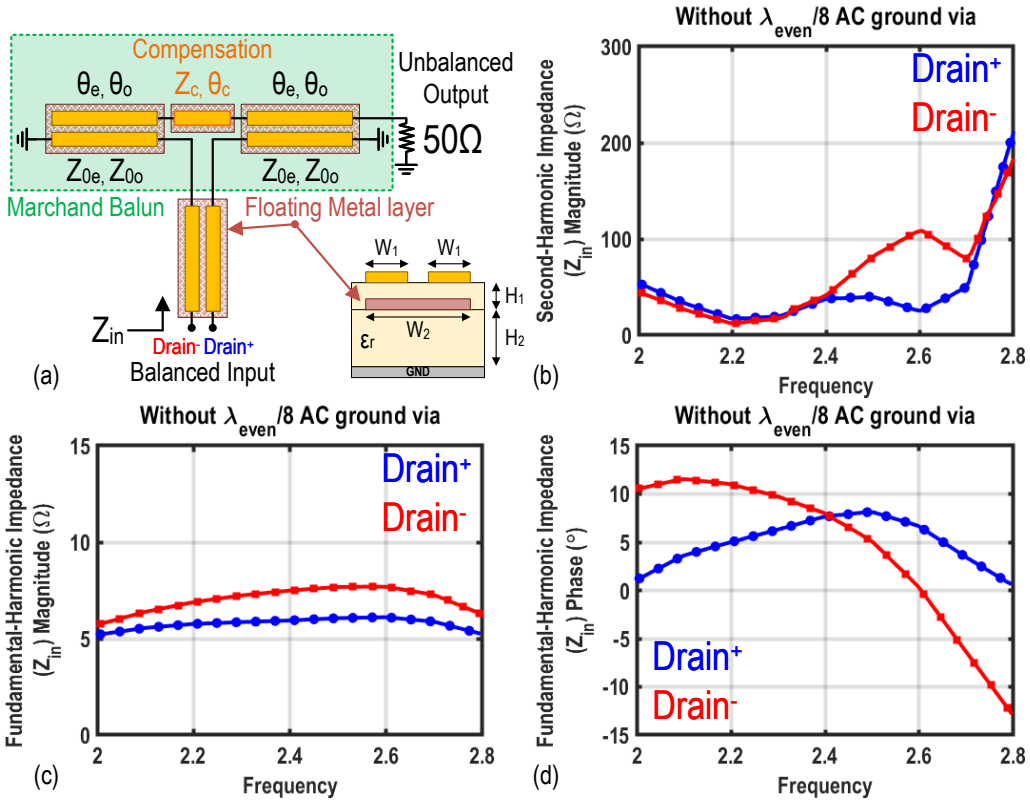


Figure 3.14: (a) Compensated Marchand balun with re-entrant coupled lines and without AC grounding at $\lambda/8$ for the second harmonic control (b) EM simulation of Fundamental and Second-harmonic impedance class-E load network with a floating island.

Fig. 3.15(a), the balun basically consists of an unbalanced, an open-circuited, two short-circuited, and balanced transmission line sections. Each section is approximately a quarter-wavelength long at the desired center frequency. Compared to a shorted coupled-line balun [75], this structure has less stringent requirements for even-mode characteristic impedance, Z_{0e}, generally Z_{0e} = 3-to-5 times of odd-mode characteristic impedance, Z_{0o}, is sufficient to obtain good performance for such baluns. The compensation term is used in broadband baluns, where the balanced output and its load reduced phase slope are maintained over a wide RF bandwidth [81].

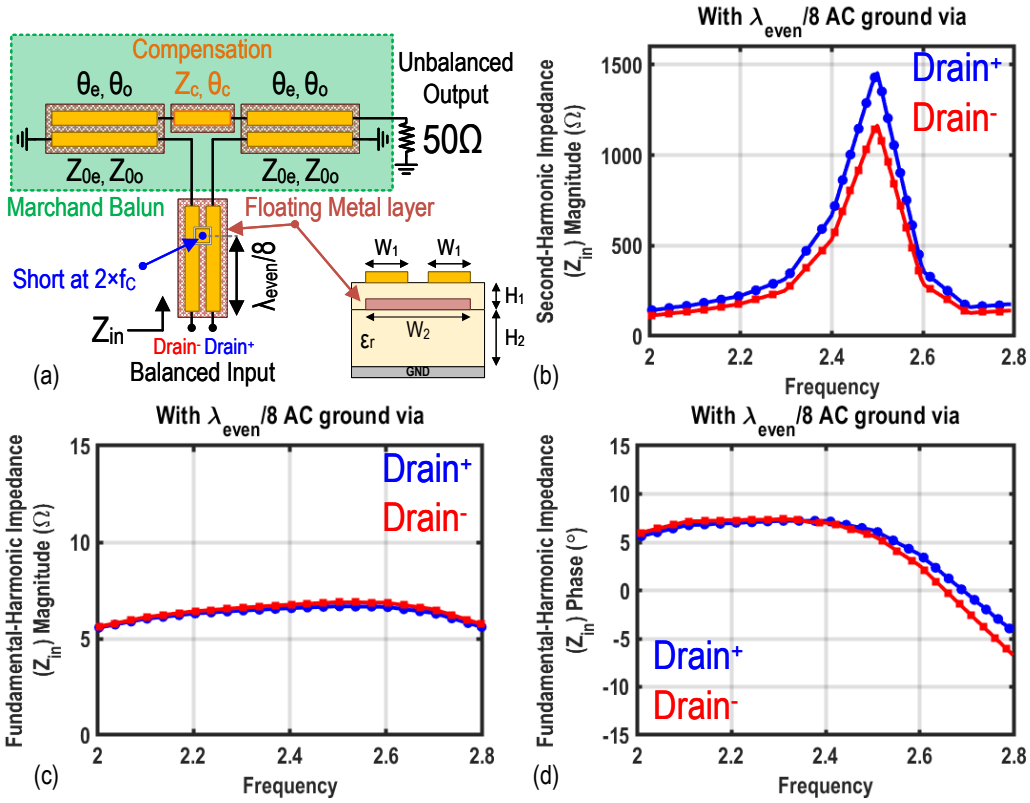


Figure 3.15: (a) Compensated Marchand balun with re-entrant coupled lines and AC grounding at $\lambda/8$ for the second harmonic control, using a via from the floating metal layer to the ground plane. (b) EM simulation of Fundamental and Second-harmonic impedance class-E load network.

Tight differential coupling with a high even-mode impedance is required to realize the wideband class-E load network with sufficiently low impedance. This feature is realized by employing re-entrant type coupled lines with a proper dielectric constant and dielectric layer thickness between and underneath the conductors, yielding a low-loss wideband balun. As depicted in its layer cross-section in Fig. 3.15(a), it consists of three conductors, two of which are deposited on the top surface of a two-layered dielectric substrate, and a floating third conductor is sandwiched between the two dielectrics. A well-controlled wideband 2^{nd} harmonic termination for class-E operation can be achieved by utilizing the orthogonality

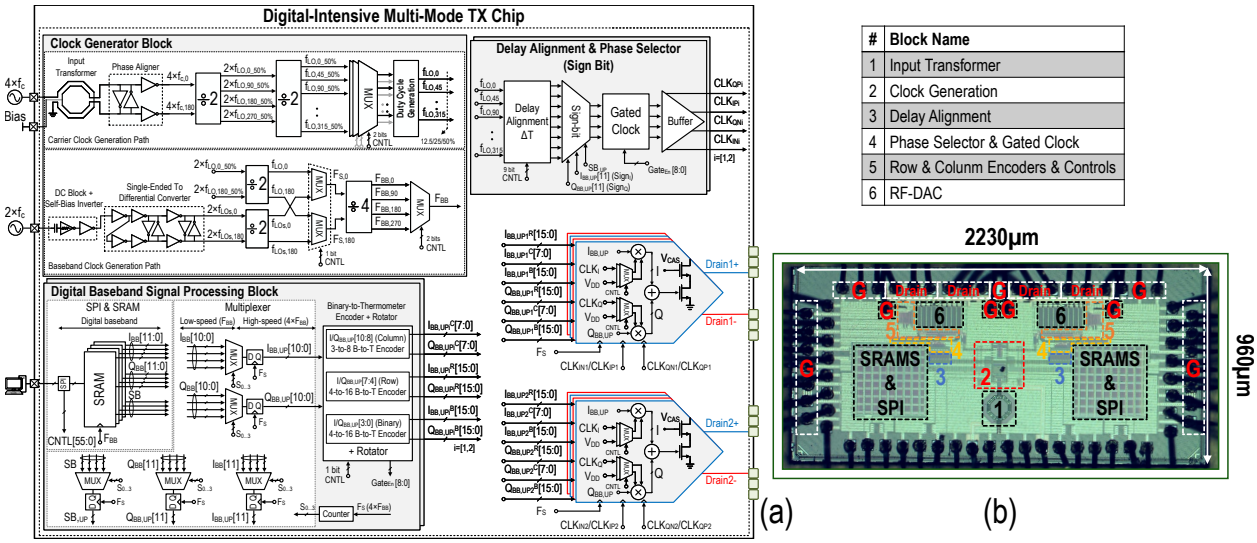


Figure 3.16: (a) The detailed block diagram of the implemented multi-mode CMOS chip. (b) Chip microphotograph.

between the fundamental (differential) signal and the in-phase (common-mode) behavior of the 2^{nd} harmonic signals. Consequently, the required open 2^{nd} harmonic for a digital class-E DPA can be realized by providing an even-mode short-circuited condition at $\lambda/8$ distance of the DPAs. Something that can be practically achieved by placing a simple via to ground in the center of the floating center plate conductor. Due to the tight coupling between the three conductors, the top metals are inherently forced to ground for their even-mode signals, thus seen as open-circuit by the DPA at the 2^{nd} harmonic (Fig. 3.15(b)). In the odd-mode, the center of the floating metal is virtually ground, barely affecting the odd-mode impedance levels.

3.5 Implementation Details

The DTX architecture features two separate parts, namely a multi-mode digital CMOS chip and an off-chip matching network. In the remainder of this section, various parts of our proposed DTX will be presented.

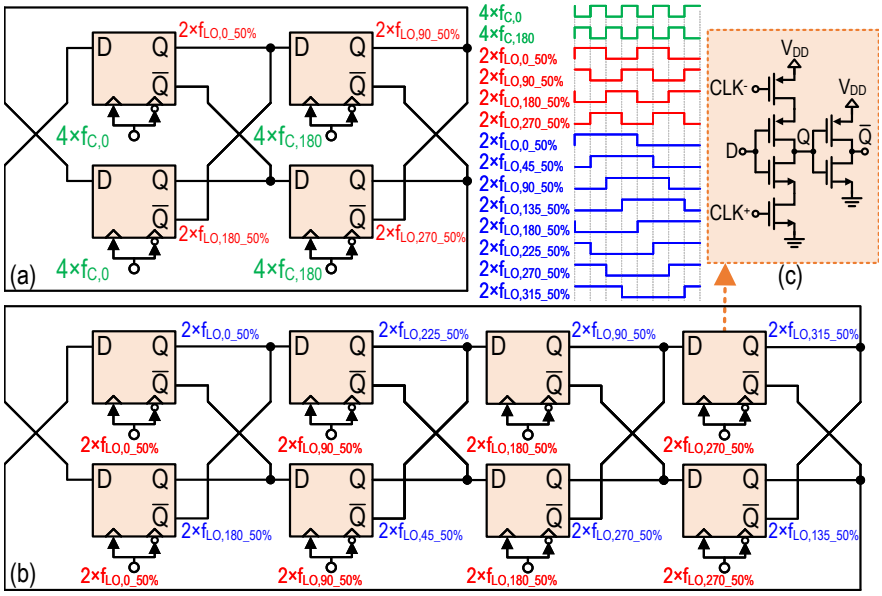


Figure 3.17: (a) Four-phase and (b) eight-phase divide-by-2 circuits with corresponding waveforms. (c) C^2MOS latch with swapped data/clock inputs.

3.5.1 Multi-Mode Digital TX CMOS Chip

The implemented chip overall system block diagram is depicted in Fig. 3.16(a). It is sub-categorized into the digital baseband signal processing block, the LO and sampling clock generation block, the delay alignment and phase (sign-bit) selector block, and the RF-DACs.

3.5.1.1 Clock Generation and Distribution

At the DTX input, an on-chip transformer converts an off-chip unbalanced local oscillator clock running at $4\times f_C$ to its balanced counterparts. The transformer's outer diameter is $150\mu m\times150\mu m$ with a 1:1 turns ratio, while the center tap is located at its secondary winding and connected to a common-mode voltage of $V_{DD}/2$. Although a recursive design is performed to achieve a transformer with negligible amplitude and phase mismatch to prevent any misalignment, a phase aligner comprising a back-to-back inverter pair is employed at the transformer output. These phased aligned differential high-speed clocks, i.e., $2\times f_{C,0}$ and $2\times f_{C,180}$, are applied to a divide-by-2 circuit to generate four complementary quadra-

ture clocks at $2\times f_C$ with 50% duty cycle and a relative phase difference in multiples of 90° ($f_{LO,0\_50\%}$, $f_{LO,90\_50\%}$, $f_{LO,180\_50\%}$, $f_{LO,270\_50\%}$ in Fig. 3.16(a)). The topology of this divider is shown in Fig. 3.17(a), which is implemented as a flip-flop-based frequency divider that consists of four C^2MOS latches arranged in a loop [70]. The back-to-back connection of Q and $\bar{Q}$ in the latches aligns the four differential clock phases and improves the quadrature-phase accuracy. It is worth noting that employing wider transistors can enhance the speed of C^2MOS latches as the supply voltage is fixed and set to $V_{DD} = 1.1$. Nonetheless, as depicted in Fig. 3.17(c), to boost the operating frequency of the divider, the data and clock inputs of C^2MOS latches are also swapped compared with a conventional C^2MOS latch to decrease the input-to-output delay of the latch and, consequently, the overall loop time excursion of the divider. These quadrature clocks are applied to a following divide-by-2 circuit to generate the desired carrier frequency at f_C with 50%-LO clocks and 45° phase differences (i.e., $f_{LO,k\_50\%}$, $k = 0, 45, \ldots, 315$). The architecture of the eight-phase-generator divide-by-2 is depicted in Fig. 3.17(b), implemented by extending the concept of the previous four-phase-generator divide-by-2 circuit. Multiples of 45° clock phases are generated by a ring divider comprising eight C^2MOS latches arranged in a loop. As depicted in Fig. 3.17(b), the four quadrature clocks generated by the previous divide-by-2 stage are employed as the clocks of the C^2MOS latches. The structure of the C^2MOS latches is as before, while its transistor sizing is adjusted based on the desired operational frequency. Depending on the intended operating mode, an arrangement whereby the 50%-LO clocks at f_C have 12.5%-LO or 25%-LO overlaps are selected. As illustrated in Fig. 3.18, the duty-cycle generation circuit produces the related eight-phase 12.5%-LO or 25%-LO clocks by bit-wise AND operation of the corresponding LO pairs. It is also worth mentioning that the AND gates are implemented in a symmetrical configuration to equalize the delays of the clocks [82].

An independent master/baseband clock can be generated using another off-chip single-ended clock running at $2\times f_C$. After an unbalanced-to-balanced conversion using an active unbalanced-to-balanced converter and a subsequent divide-by-2 circuit, the F_S clock is generated. This master clock is then applied to a divide-by-4 circuit to generate the F_{BB} clock.

To mitigate the crosstalk mainly caused by capacitive coupling, ground lines were placed in the middle of the quadrature LO lines. Besides, shielding is utilized to suppress the LO leakage and diminish the coupling from other routing lines, e.g., data routing, when multiple crossover lines occur.

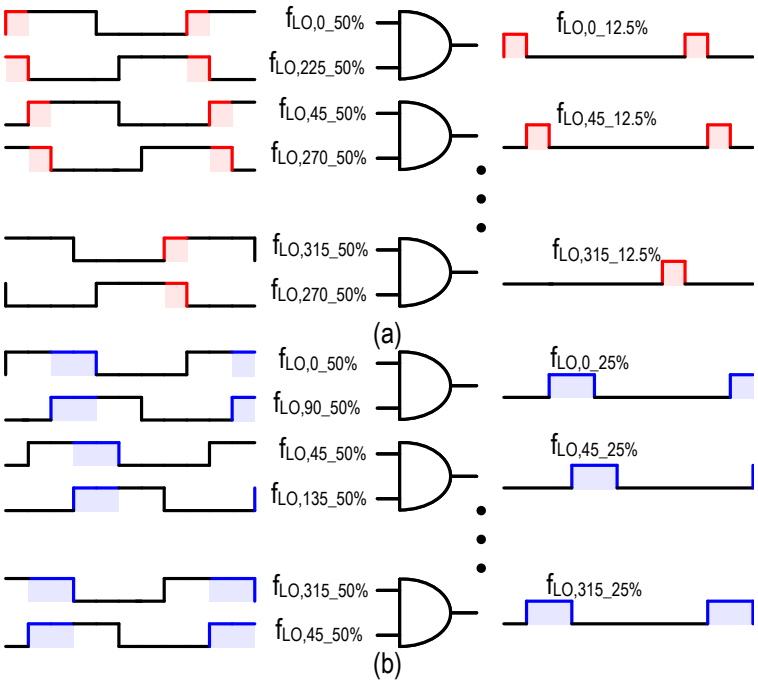


Figure 3.18: Related eight-phase 12.5%-LO or 25%-LO duty-cycle clocks generation by bit-wise AND operation of the corresponding LO pairs.

3.5.1.2 Delay alignment and phase selector

To compensate for different design variations, such as the process/voltage/temperature (PVT), frequency, and load variations on the phase relations, fine-tune phase aligners are adopted [57] and implemented, as shown in Fig. 3.19. The controls for these phase aligners are static and come from a serial-to-parallel interface (SPI). The absolute delay of each delay cell is controlled with a single bit by enabling or disabling NMOS and PMOS transistors in series with the supply/ground paths. The RF clock passes through 15 cascaded delay cells to arrive at the output, resulting in a total relative delay of 75ps with a resolution of roughly 5ps (Fig. 3.19(c)).

The delay alignment block is followed by a phase selector circuitry implemented by complementary NAND-gate-based multiplexers with input selection control signals to modulate the LO clock properly, as demonstrated in Fig. 3.20. In a Cartesian mode, these controlling signals are I/Q sign bits ($I_{\mathrm{BB,UP}}[11]$ ($\mathrm{Sign_I}$) and $Q_{\mathrm{BB,UP}}[11]$ ($\mathrm{Sign_Q}$)). The multi-phase

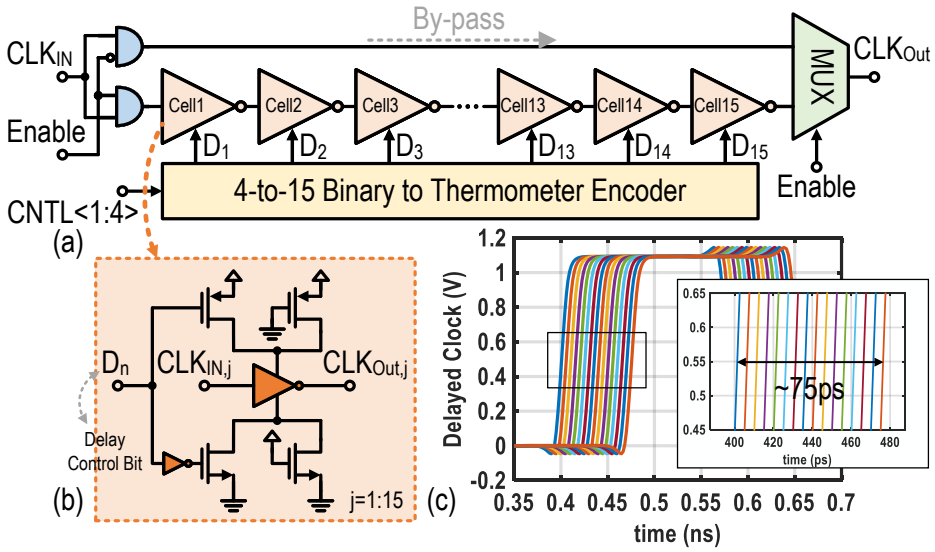


Figure 3.19: (a) Schematic of the 4-bit fine-resolution delay line, and (b) its delay-cells. (c) Delayed 3GHz clock simulation.

operation modes demand 3-bit selection control signals to cover 8-octant, as discussed earlier. Another controlling signal is employed in the phase selector controlling circuit to select between cartesian and multi-phase cartesian modes. To equalize the delays of the clocks, the NAND gates are implemented in a fully symmetrical configuration. Moreover, a back-to-back inverter pair is employed for further phase alignment of the complementary clock pairs.

3.5.1.3 The Un-signed 11-bit I/Q DPA floor plan

As a trade-off between the in-band linearity, far-out noise, power consumption, and the overall complexity of the DTX, a resolution of 12-bit per I/Q (including sign-bit) is selected for the DPA to meet the requirement of wireless communication standards. The quantization-noise-limited dynamic range (DR_{QN}) of the DPA, in terms of its resolution (N), the signal peak-to-average power ratio (PAPR), and oversampling ratio (OR), defined as $F_S/(2BW)$, is given by

$$DR_{QN}(dBc) = 6.02N + 1.76 + 10\log_{10}(OR) + 3.01 - PAPR \tag{3.11}$$

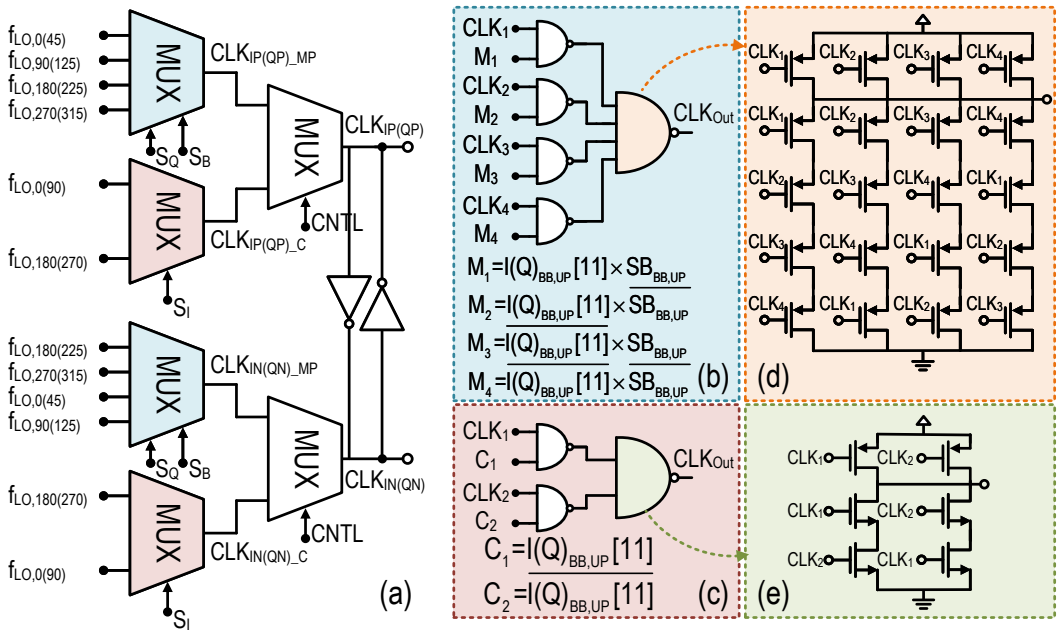


Figure 3.20: (a) Schematic diagram of the clock phase selector. (b), (c) NAND gate-based multiplexer implementation circuitry. (c), (d) 4-/2-input symmetrical NAND logic gate.

where the 3dB factor arises from the I and Q operation. This formula predicts a dynamic range of 68.9dBc, assuming a target BW and PAPR of 200MHz and 8.2dB, respectively, and the F_S of 600MHz. This is sufficient to fulfill the TX requirements of the current and next-generation wireless mobile networks. Moreover, the DTX comprises two identical 12-bit resolution I/Q banks. Fig. 3.21(a) depicts the implementation details and the floorplan of one of the I/Q banks. For each bank, the digital baseband data (I/Q_{BB}[11:0]) are stored on four parallel 1-K SRAM, clocked at F_{BB}, which are programmed through the low-speed SPI interface. The 12-bit digital I/Q baseband signals pass through multiplexers to up-sample by 4 (F_S=4×F_{BB}). $I/Q_{\mathrm{BB,UP}}$[10:0] represents the up-sampled un-signed binary digital codes segmented to 4-bit ($I/Q_{\mathrm{BB,UP}}$[3:0]) binary-weighted LSB and 7-bit ($I/Q_{\mathrm{BB,UP}}$[10:4]) thermometer-coded MSB cells. Moreover, the 7-bit MSB are split into 3-bit ($I/Q_{\mathrm{BB,UP}}$[10:8]) for column encoder and 4-bit ($I/Q_{\mathrm{BB,UP}}$[7:4]) for row encoder. Hence, the 128 MSB units of each part are distributed over 16 rows ($I/Q_{\mathrm{BB,UP^R}}$[15:0]) and 8 columns ($I/Q_{\mathrm{BB,UP^C}}$[7:0]). Furthermore, each part's LSB units comprise 16 small unit cells ($I/Q_{\mathrm{BB,UP^B}}$[15:0]) that

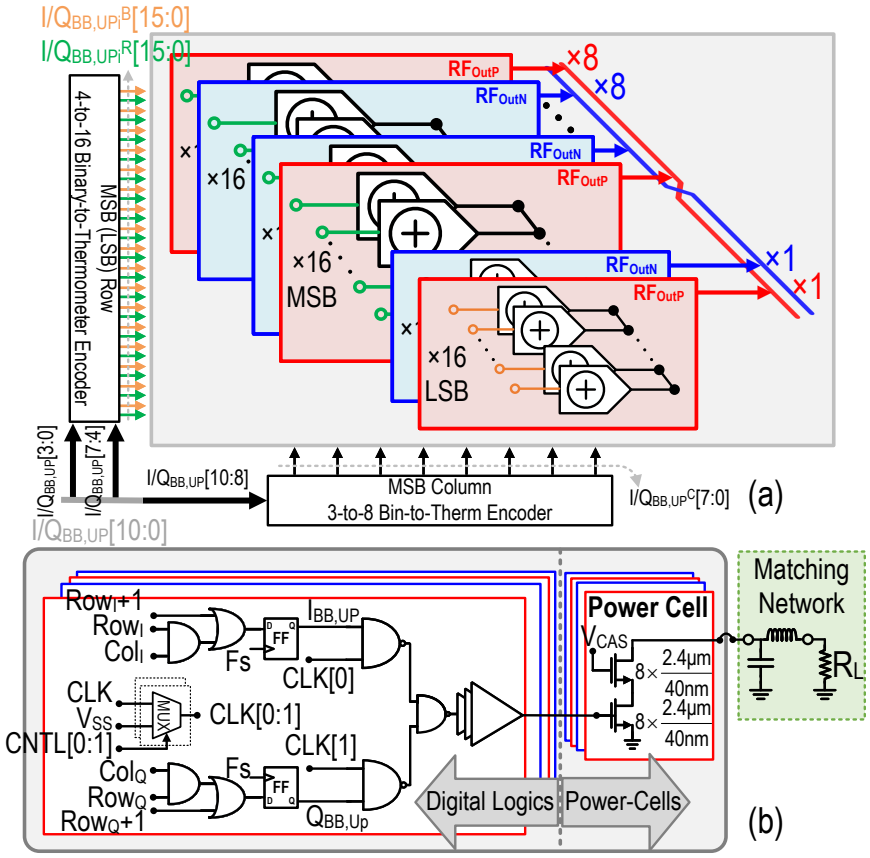


Figure 3.21: (a) Un-signed 11-bit I/Q DPA floor plan. (b) I/Q RF-DAC sub-cells.

occupy a column.

Instead of having two separate push-pull banks, every other column of the I/Q RF-DAC matrix is dedicated to the in-phase arrays and their 180° out-of-phase counterparts [82]. This technique reduces the overall I/Q RF-DAC core size for the same achievable output power, resulting in a highly compact area, smaller parasitics, minimal mismatch, and less power consumption, resulting in improved overall DTX efficiency. Swapped/cross-coupled power-lines for the in-phase and out-of-phase drain lines are utilized to equalize the parasitics in the primary output traces.

The I/Q RF-DAC sub-cell comprises the pure digital logic section and the power-cell part (Fig. 3.21(b)). The logic part consists of a decoding logic and a time synchronizer flip-flop

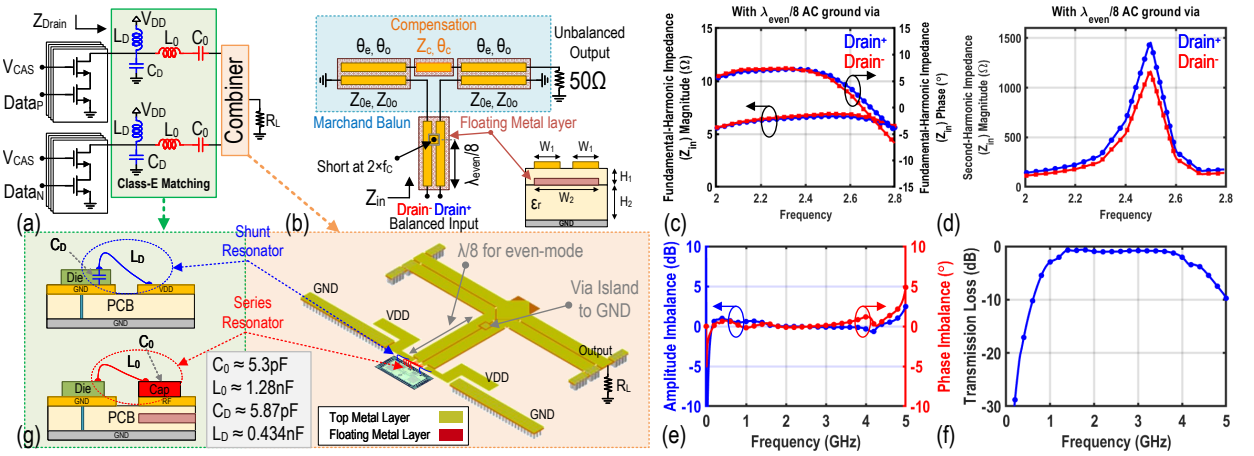


Figure 3.22: (a) General push-pull class-E schematic. (b) Compensated Marchand balun with re-entrant coupled lines and AC grounding at $\lambda/8$ for the second harmonic control, using a via from the floating metal layer to the ground plane. Electromagnetic simulation results of the (c)-(d) fundamental and second-harmonic impedance for the load network, and (e)-(f) amplitude/phase imbalance and transmission loss over the frequency. (g) The final realization of the re-entrant type Marchand balun and the side view of the wirebonding structure of the chip to the matching network.

followed by an I/Q mixing circuit. Depending on the operating mode, a multiplexer enables the appropriate clock pairs to fulfill the up-conversion. Furthermore, the synchronized digital data is upconverted by corresponding LO clocks using bit-wise NAND operation. Eventually, the upconverted I/Q bitstreams are combined by the subsequent NAND gate to fulfill I/Q interleaving and feed the following power cell inverter buffers. All digital circuits are implemented based on symmetrical gates to equalize the delay from the input to the output and the fanout for proceeding circuitry. This chip is combined with an off-chip class-E matching network. Meanwhile, since in class-E, the peak drain voltage is 3.66 times the supply voltage thus, a cascode topology is adopted in this design to prevent reliability violations.

Figure 3.16(b) exhibits the chip micrograph realized in the 40nm bulk CMOS process, while the corresponding block names are listed in the table. The chip occupies a die area of $2.23\times0.96\text{mm}^2$ with a core area of 0.72mm^2. Moreover, a dedicated SPI and the designated SRAMs are digitally synthesized and occupy an area of $2\times0.43\times0.43\text{mm}^2$, while decoupling capacitors and I/O pads occupy the remainder.

3.5.2 Wideband Marchand Balun and Matching Network

The Marchand balun, shown in Fig. 3.22, is fabricated on a two-layer customized build-up FR-4 material. The layer thickness of the top and bottom substrates for the re-entrant type coupled lines are H_1 = 0.2mm, and H_2 = 0.7mm, respectively, with ϵ_r = 4.6. The width of the top layer metal lines is W_1 = 1.5mm with S = 0.1mm spacing, and the width of the floating metal layer is W_2 = 3.1mm, resulting in Z_{0e} = 71Ω and Z_{0o}= 7.5Ω impedances for the DPA. The even- and odd-mode wavelengths at f_C = 2.5GHz are approximately λ_{even} = 59mm and λ_{odd} = 36mm. Moreover, to provide a second-harmonic open impedance for the class-E DPA, the via to ground in the center of the floating center plate conductor is practically implemented by placing one island with a through via from the top metal layer to the bottom ground plate at an optimized distance in front of the DPA, as shown in Fig. 3.22. The inductances of the shunt and series resonators are implemented by two and three parallel bondwires, respectively. Chip capacitors are used to complete the implementation of the series resonator.

Electromagnetic simulation results of the fundamental and second-harmonic impedance for the load network are plotted in Fig. 3.22(c)-(d), providing large second-harmonic impedance and balanced amplitude and phase for the differential to single-ended conversion. Fig. 3.22(e)-(f) show the amplitude and phase imbalance and transmission loss over the frequency. Accordingly, the transmission loss from the balanced input port to the unbalanced output port is less than 1.4dB in the 1.5-to-4GHz band (less than 1dB in the 1.6-to-3.8GHz band).

3.6 Experimental Results

The measurement setup is shown in Fig. 3.23. The DPAs, the SRAM, and digital circuitries operate on separate 1.1V domains. The baseband data of each DPA are generated in MATLAB and independently applied to the DTX using four parallel on-chip 1-K SRAMs running at F_S = 600MHz. The measured output powers include the matching loss, and the power consumption of all blocks (except SRAMs) is included in the reported system efficiency. The matching network is tuned according to the targeted DTX operation mode.

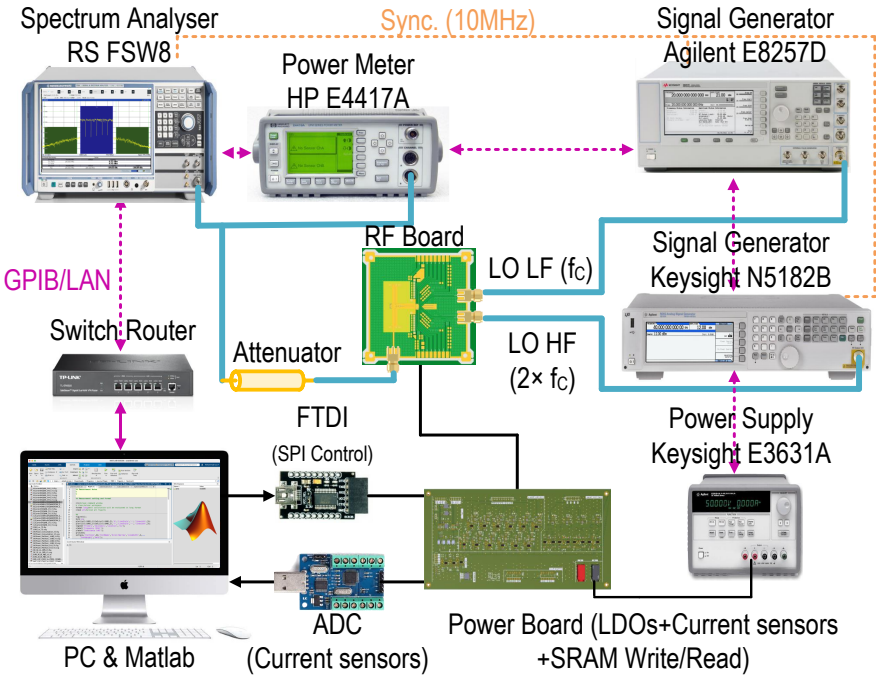


Figure 3.23: Measurement setup.

3.6.1 Static Measurements

3.6.1.1 Power/Efficiency Measurement Over the RF Bandwidth

The DTX is first characterized by static measurements. The output power is measured using a power meter. The measured peak output power (P_{Out}), drain efficiency (DE), and system efficiency (SE) for different operational modes versus frequency are shown in Fig. 3.24. In Mode-1, the proposed DTX delivers 23.18dBm peak P_{Out} at 2.1GHz with a DE and SE of 66.26% and 52.59%, respectively. The difference between the drain and system efficiency is caused by the fixed power consumption of circuit blocks that do not scale with the output power. Therefore, if the output power increases while the other blocks are unchanged, the SE becomes closer to the DE [83, 84]. The peak P_{Out} and DE vary in different operational modes. Namely, in Mode-1, the effective duty cycle of the combined vectors can be as high as 50% when using a 25% LO clock, while in Mode-4, the combined duty cycle reduces to 37.5%, yielding a significant efficiency improvement. Overall, the DTX achieves a 3dB

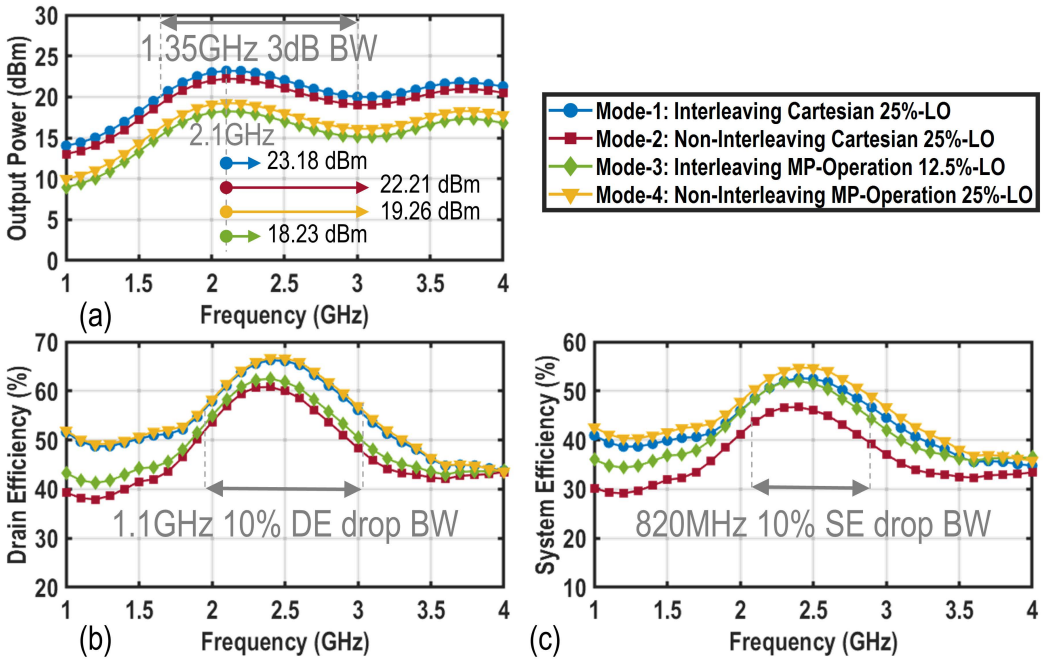


Figure 3.24: Measured (a) peak output power, (b) drain, and (c) system efficiencies versus operational frequency for different operational modes.

bandwidth of 1.35GHz in a 1.65-to-3GHz band while maintaining decent performance.

3.6.1.2 Power/Efficiency Measurement Over the I/Q plane

A 400-point static measurement is performed using 20 samples for each I/Q symbol (first I/Q quadrant) at 2.4GHz. In Fig. 3.25, measured DE contours for different operational modes are extracted for the four-quadrant plane. Generally, the Cartesian configuration has 4-petal-like efficiency contours along the diagonal lines of the I/Q plane. In contrast, the multi-phase operation has 8-petal-like efficiency contours where multiples of 22.5° lines are located, imitating polar contours, thus reducing the phase dependency of the efficiency. The dashed gray circle on the I/Q plane represents the average power region for a 160MHz 256-QAM OFDM signal. The enhanced efficiency performance is evident in multi-phase operation modes as it has higher efficiency on the gray circle than its Cartesian DTX.

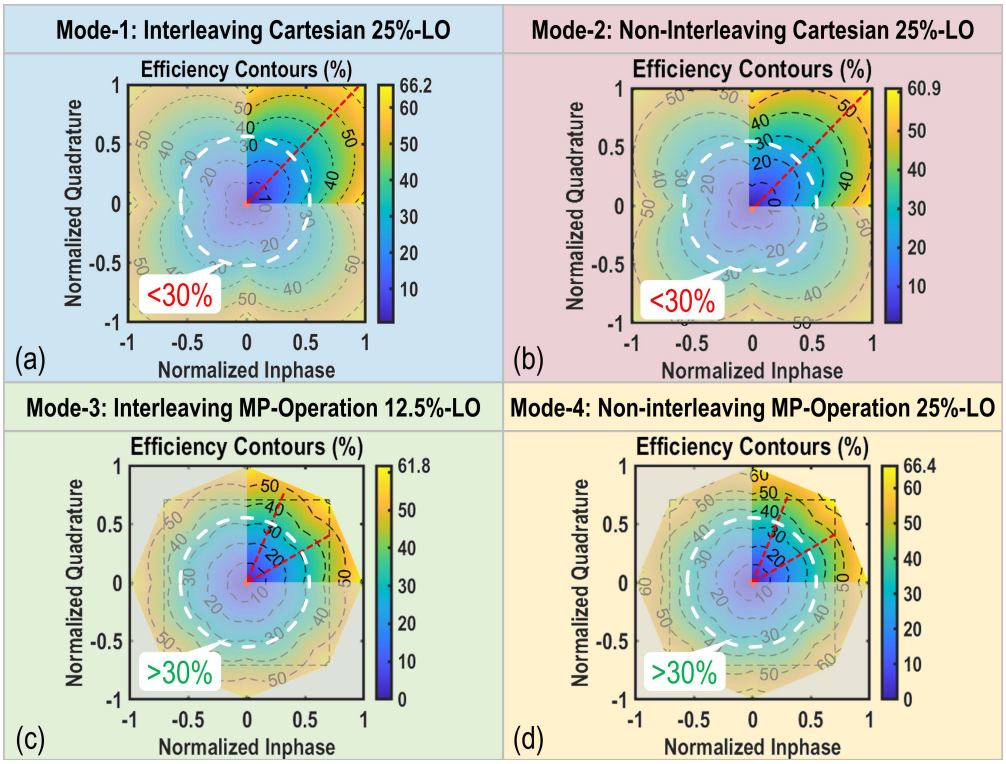


Figure 3.25: The measured drain efficiency contours of the 400-point static points using 20 samples for each I/Q symbol in the first I/Q quadrant at 2.4GHz extracted for the four-quadrant plane for different operational modes.

3.6.2 Complex modulated signal measurements

The DTX dynamic performance is verified by employing single-/multi-channel higher-order modulation schemes such as OFDM signals with different modulation bandwidths utilizing a simple memory-less digital pre-distortion (DPD). The spectral purity of a "4-channel×40MHz 64-QAM OFDM" signal with an aggregated bandwidth of 160MHz is applied to the DTX, and the performance is verified in different operational modes at f_C=2.4GHz. The measured spectrum of the signal in Mode-1 and the constellation diagram of Ch-4 are depicted in Fig. 3.26(a). The DTX achieves an average output power of more than 13.5dBm while maintaining the average drain and system efficiency of 30.34% and 24.9%, respectively. The ACLR is better than -42.18dBc, and the average EVM is -36.30dB. The ACLR and average

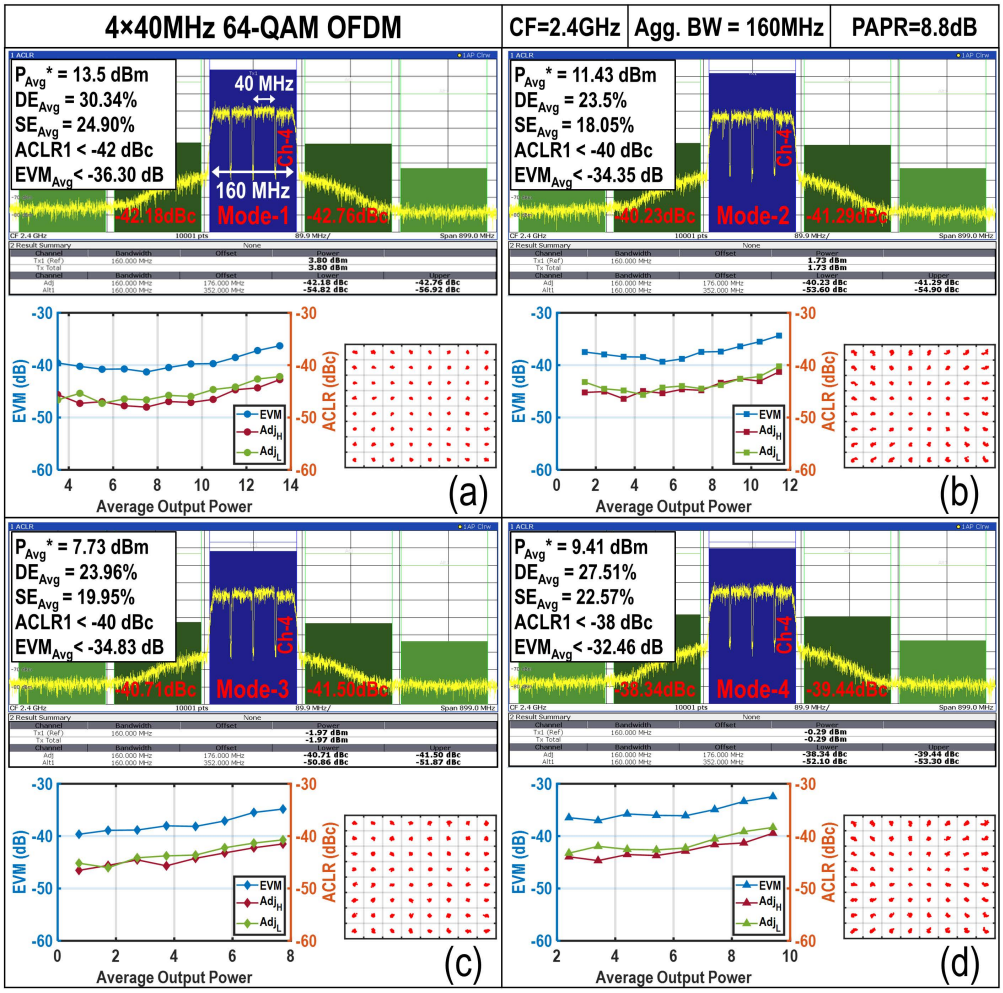


Figure 3.26: Measured spectrum of 4-channel×40MHz 64-QAM OFDM signal, constellation diagram of Ch-4 and ACLR and average EVM performances versus average output power for different operational modes.

EVM performances versus average output power are also exhibited in Fig. 3.26(a), reaching -39.7dB average EVM at 10.5dBm average output power, while the ACLR is better than -44.6dBc.

The DTX is examined with the same signal in Mode-2. Fig. 3.26(b) exhibits the measured spectrum of the signal and the constellation diagram of the Ch-4 using DPD. Accordingly, the

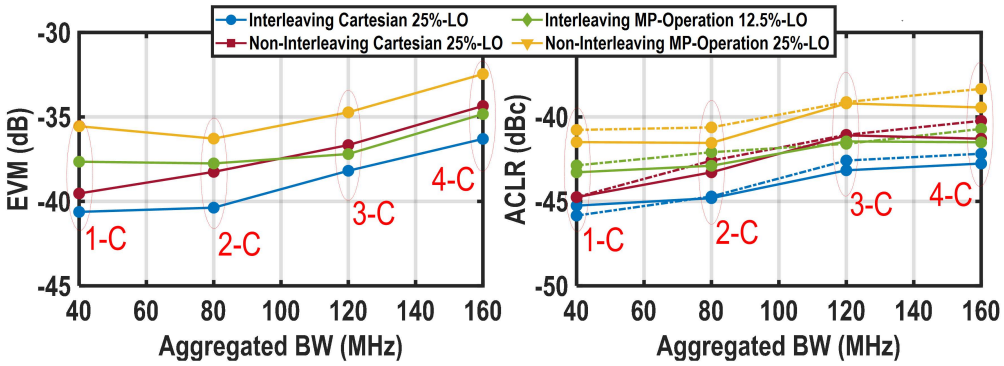


Figure 3.27: The average ACLR and EVM of the DTX in different modes of operation with various 1-to-4-channel×40MHz 64-QAM OFDM signals.

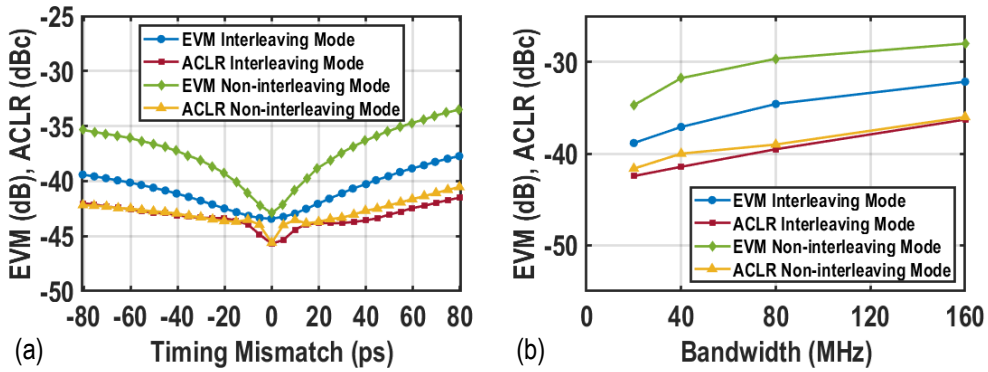


Figure 3.28: Measured (a) EVM and ACLR of a 20MHz 64-QAM OFDM signal versus DPAs timing mismatch and (b) EVM and ACLR with 60-ps timing mismatch versus signal bandwidth for interleaving and non-interleaving modes.

DTX delivers 11.43dBm average power while achieving an ACLR of better than –40.23dBc and an average EVM of -34.35dB. The measured average drain and system efficiencies are 23.5% and 18.05%, respectively. The ACLR and average EVM performances versus average output power are also exhibited, reaching -37.4dB average EVM at 8.43dBm average power, while the ACLR is better than -43.8dBc.

Figure 3.26(c) demonstrates the spectral purity of this signal and its Ch-4 constellation diagram when the DTX is configured in Mode-3. With more than 7.73dBm average power,

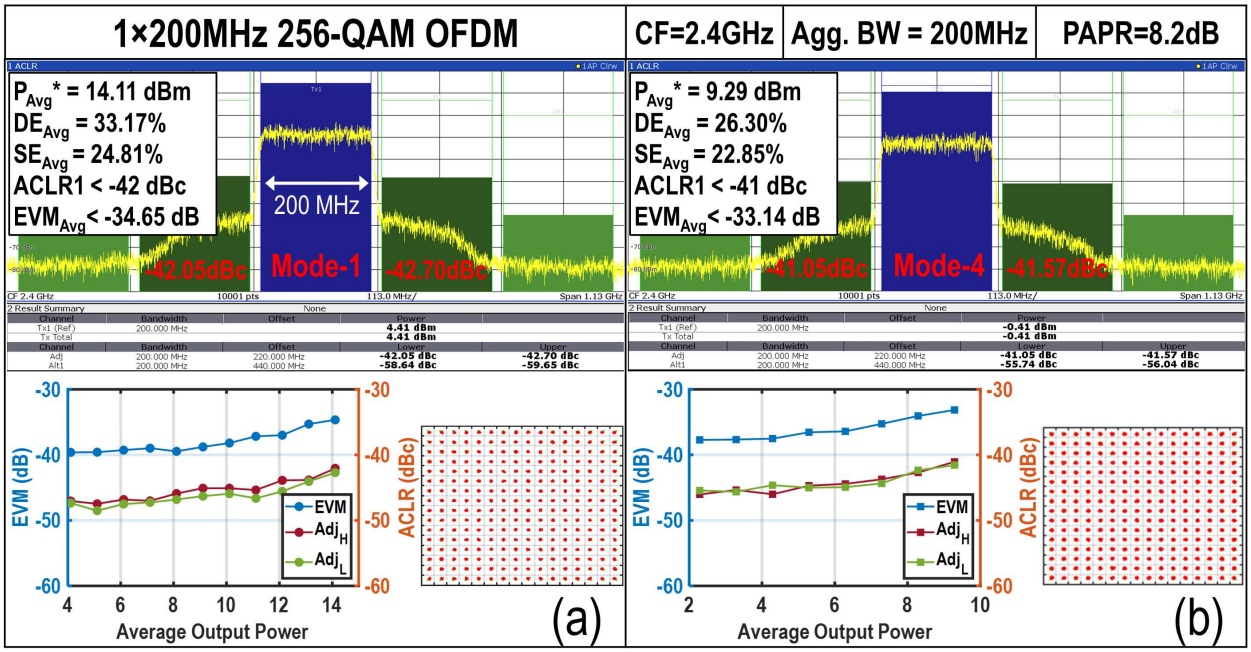


Figure 3.29: Measured spectrum of single-channel×200MHz 256-QAM OFDM signal, its constellation diagram, and ACLR and average EVM performances versus average output power for Mode-1/-4 operation.

the digital transmitter achieves an ACLR of better than -40.50dBc and an average EVM of -34.83dB. According to Fig. 3.26(c), the DTX reaches -38.3dB average EVM at 4.73dBm average output power, while the ACLR is better than -43.6dBc.

For the Mode-4 scenario, as shown in Fig. 3.26(d), the DTX delivers an average output power of more than 9.41dBm, and ACLR and average EVM of better than -38.34dBc and -32.46dB, respectively. The ACLR and average EVM performances versus average output power are also exhibited in Fig. 3.26(d), reaching -36.1dB average EVM at 6.41dBm average output power, while the ACLR is better than -42.2dBc.

Figure 3.27 presents the average EVM and ACLR performance of a contiguous multi-channel "40MHz 64-QAM OFDM" signal dependent on the number of carriers (aggregated bandwidth) in different modes of operation. Generally, the average EVM and ACLR of a 1-channel 64-QAM OFDM with an aggregated bandwidth of 40MHz are better than -35.5dB and -41.1dBc.

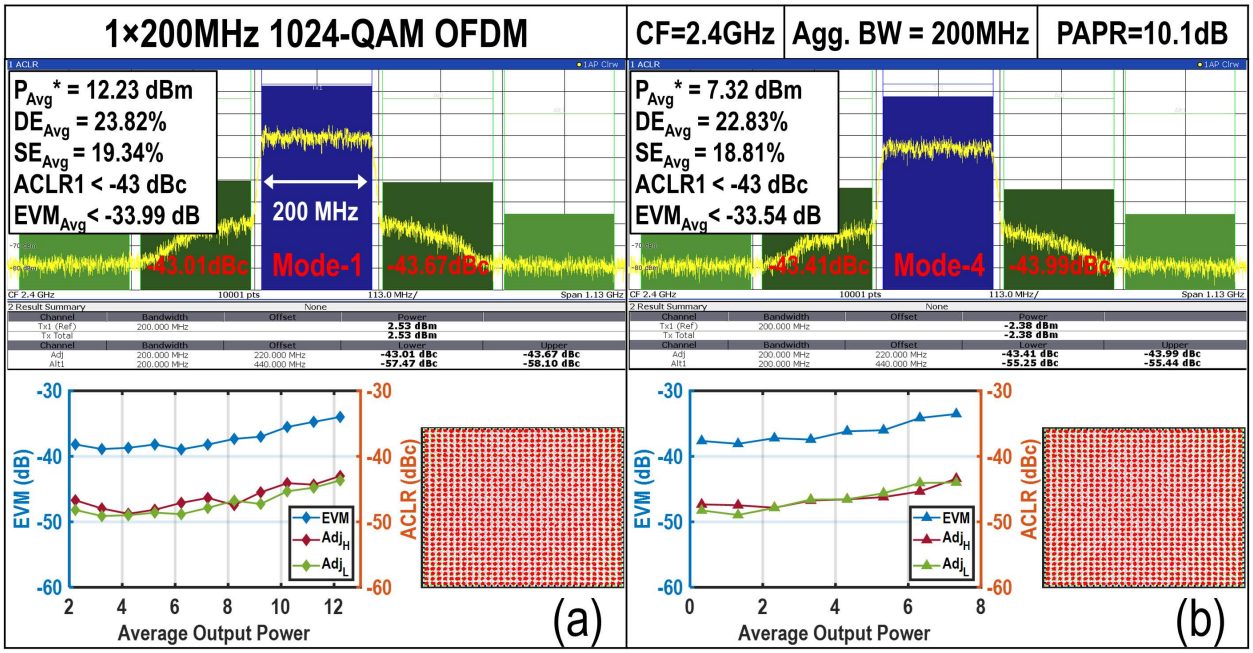


Figure 3.30: Measured spectrum of single-channel×200MHz 1024-QAM OFDM signal, its constellation diagram, and ACLR and average EVM performances versus average output power for Mode-1/-4 operation.

As shown in Fig. 3.19, fine-tuned phase aligners are adopted for each single DPA to compensate for the timing mismatch between them. Fig. 3.28(a) shows the EVM and ACLR of a 20MHz 64-QAM OFDM signal versus DPAs timing mismatch for an interleaving and non-interleaving mode. As illustrated, any timing mismatch will degrade the ACLR and EVM. Increasing the input signal bandwidth makes it even more challenging to achieve good linearity since it directly increases the impact of time alignment errors, as shown in Fig. 3.28(b).

The proposed DTX is then evaluated by a 200MHz "single-channel 256-QAM OFDM" signal in the Mode-1/(-4) scenario, and the performance is measured at 2.4GHz (Fig. 3.29). In this case, the average delivered output power is more than 14.11/(9.29)dBm, while the ACLR and EVM are better than -42.05/(-41.05)dBc and -34.66/(-33.14)dB, respectively. The ACLR and average EVM performances versus average output power are also exhibited in Fig. 3.29, reaching -37.2/(-36.4)dB average EVM at 11.1/(6.3)dBm average output power,

Table 3.1: Performance Summary And Comparison With State-Of-The-Art

Specifications	This Work		JSSC 2020 A. Bassat		JSSC 2017 M. Hashemi		JSSC 2017 W. Yuan	JSSC 2021 M.R. Beikmirza		JSSC 2022 Y. Li	JSSC 2020 S.W. Yoo		JSSC 2022 B. Yang	
Technology	CMOS 40nm		CMOS 28nm		CMOS 40nm		CMOS 130nm	CMOS 40nm		CMOS 55nm	CMOS 60nm		CMOS 40nm	
Architecture	Multi-mode DTX*		Polar		Polar		Multi-phase SCPA	Quadrature 4-way Doherty		Quadrature	TI-Doherty /Class G		Quadrature SCPA /Hybrid Doherty	
Die Area (mm^2)	2.1 (0.72 ‡)		4 ¥		0.45		3.7	3.55 (1.5 ‡)		1.83 (1.19 ‡)	3.36		2.2	
Supply (V)	0.95		1.4		0.5		3	1		1.2 / 2.4	2.5		1.2/2.4	
Frequency (GHz)	2.4		2.5	5	2.2 **		1.8	5.4		0.85	2.4		2.4	
3dB Power BW	1.35 GHz		N/A		1.5 GHz *		750 MHz	1.3 GHz		1 GHz *	N/A		1.1GHz **	
Peak P_{out} (dBm)	(Mode-1) 23.18	(Mode-4) 19.26	27	27	14.6		26	27.4		29.3	30		30.3	
Peak DE (%)	66.2	66.4	N/A	N/A	43.8		N/A	47.4		N/A	40.2		41.3	
Peak SE (%)	52.59	54.73	53	35	28.8 †		24.9	30.66		43.1	N/A		36.5	
Modulation	1024-QAM OFDM	1024-QAM OFDM	MCS11	MCS11	64-QAM @2GHz	64-QAM @2GHz	64-QAM LTE	256-QAM OFDM	256-QAM OFDM	64-QAM LTE	1024-QAM	64-QAM OFDM	256-QAM	1024-QAM
Bandwidth (MHz)	200	200	40	160	20	40	10	40	240	20	10	10	60	40
PAPR (dB)	10.1	10.1	6.9	7.8	8		5.1	8.64	9.68	8.29	6.8	10.9	6.98	9.86
Avg. P_{out} (dBm)	12.23	7.32	20.1	19.2	6.1 $		20.9	18.9	17.8	21.01	23.2	19.1	23.3	20.4
Avg. DE (%)	23.82	22.83	N/A	N/A	17.5 $		N/A	43.1	41.2	N/A	36.2%	30.3%	30.7%	22.6%
Avg. SE (PAE) (%)	19.34	18.81	(28.9)	(21.2)	14.3 $†		15.2	24.5	22.1	20.1	N/A	N/A	N/A	N/A
EVM (dB)	-33.99	-33.54	-35	-35	NA	-31	-29.1	-40	-32.2	-25.1	-44.5	-41.7	-31.9	-35.9
ACLR (dBc)	-43.0/-43.6	-43.4/-43.9	N/A	N/A	-43/-49	-40/-45	-30.3/-31.7	-47/-47	-39/-39	N/A	N/A	N/A	-32/-30	-35/-34
Linearization	DPD		DPD		NO		DPD	DPD		NO	NO		DPD	

• * Off-chip matching network. ** Estimated from reported figures and plots. ‡ Core area. ¥ Area including Digital front end, DPLL, and LB/HB DTX. † Excluding LO generation. $ For a 10MHz QAM signal with PAPR = 8-9dB.

while the ACLR is better than -45.3(-44.9)dBc.

Finally, to validate the capability of our proposed techniques, our proposed multi-mode DTX is examined with a 200MHz single-channel 1024-QAM OFDM signal at 2.4GHz. In Mode-1 (Fig. 3.30(a)), the average delivered output power is more than 12.23dBm, while the ACLR and EVM are better than -43.01dBc and -33.99dB, respectively. In the Mode-4 scenario (Fig. 3.30(b)), the average delivered output power is more than 7.32dBm, while the ACLR and EVM are better than -43.41dBc and -33.54dB, respectively. The ACLR and average EVM performances versus average output power are also exhibited in Fig. 3.30(a) and (b) for Mode-1 and -2, respectively. It indicates the DTX reaches -37/-36.1dB average EVM at 9.23/4.32dBm average output power, while the ACLR is better than -45.5/-46.5dBc, respectively.

The DTX performance is summarized and compared to that of the prior-art in Table 3.1.

Compared to the DTXs without efficiency enhancement techniques, the realized multi-mode digital transmitter exhibits the highest data rate, very decent average system efficiency, and high peak P_{Out}, suitable for the prevailing and next-generation wireless communication systems.

3.7 Conclusion

A wideband energy-efficient versatile transmitter has been demonstrated. It leverages the advantages of digitally-configured architecture to support a multi-mode/multi-band operation. It features various modes comprising Cartesian and multi-phase operation utilizing LO clocks with different duty cycles in the interleaving and non-interleaving configurations. The multi-phase architecture inherits the advantages of the Cartesian DTX, such as wideband operation, symmetrical and synchronized I/Q paths with a drain efficiency behavior approaching the polar counterparts. Realized in 40-nm bulk CMOS with an off-chip matching network, the DTX generates more than 23.18dBm peak P_{Out} from a 0.95V supply, with 66.26%/52.59% DE/SE in a 1–4GHz band. For a 200MHz single channel 1024-QAM OFDM signal at 2.4GHz in Mode-1/-4, the average delivered output power is 12.23/7.32dBm, while the ACLR and EVM are better than -43/-43dBc and -33.5/-33.9dB, respectively. Compared to the DTXs without efficiency enhancement techniques, the proposed DTX achieves state-of-the-art performance exhibiting the highest data rate, decent average system efficiency, and high peak power capability, making it an interesting candidate for wireless communication systems.

Chapter 4

A Wideband Multi-Mode Digital Doherty Transmitter in 40nm CMOS

This chapter is written based on [41, 85].

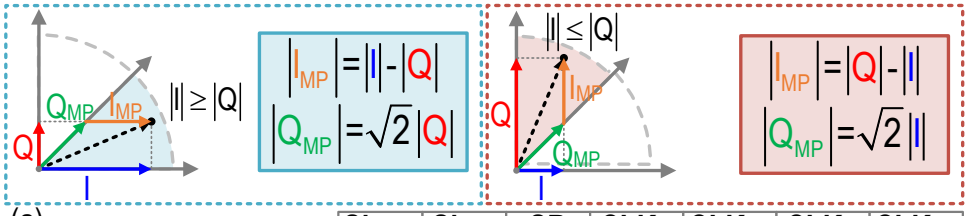
4.1 Introduction

Digital-intensive transmitters (TXs) push the digital/analog boundary towards the antenna interface. This is achieved by integrating all functions of the analog blocks into a single radio frequency digital-to-analog (RF-DAC) that directly converts the digital bits-in data to an RF-out signal. These DTXs are compatible with advanced CMOS processes, so they can be implemented with a compact die area, and directly interface to the digital back-end [86], while producing higher energy efficiency due to core devices' fast switching nature even at reduced supply voltages.

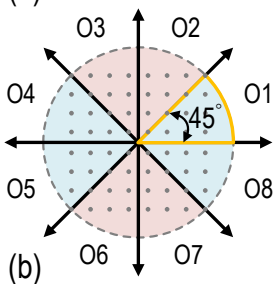
As addressed in chapter 3, traditionally DTXs are realized as a polar or Cartesian architecture. Polar DTXs [44, 45, 57] usually consist of several parts, including a COordinate Rotation DIgital Computer (CORDIC) and subsequent amplitude and phase modulators. CORDIC converts the Cartesian I and Q signals to their polar representation. Since this is a nonlinear operation yielding bandwidth expansion, limiting the achievable modulation bandwidth. Moreover, their phase and amplitude paths exploit heterogeneous circuits whose delays must be accurately aligned to avoid spectral regrowth at the final recombining stage. Nevertheless, polar DTXs generate merely amplitude data seeing ohmic loading in all phases. So for a given amplitude, the achievable drain efficiency (DE) is constant. In contrast, Cartesian DTXs [50, 54] do not need a CORDIC, phase modulators, or stringent time-synchronization circuits, exhibiting excellent compatibility with wideband communication systems. However, their linear combining of orthogonal I/Q vectors yields a complex loading condition that changes with the phase, resulting in a phase-dependent efficiency behavior.

Besides this, high data-rate signals typically have a high peak-to-average power ratio (PAPR), which compels a DTX to operate in power back-off (PBO), degrading its average efficiency if no efficiency enhancement technique is applied. A Doherty topology can provide this efficiency enhancement at low hardware complexity while being able to handle wideband complex modulated signals [20, 48, 82, 87]. In this regard, utilizing a low-loss off-chip Doherty power combiner increases the overall system efficiency, especially in PBO [20, 88].

To address the issues mentioned above, this chapter combines the previously introduced multi-mode operation approach in chapter 3, with an off-chip Doherty combiner. Multi-phase operation is utilized to compromise the polar and Cartesian features by mapping the I/Q



(a)



	$Sign_Q$	$Sign_I$	SB	CLK_{IP}	CLK_{QP}	CLK_{IN}	CLK_{QN}
O1	0	0	0	$f_{LO,0}$	$f_{LO,45}$	$f_{LO,180}$	$f_{LO,225}$
O2	0	0	1	$f_{LO,90}$	$f_{LO,45}$	$f_{LO,270}$	$f_{LO,225}$
O3	0	1	1	$f_{LO,90}$	$f_{LO,135}$	$f_{LO,270}$	$f_{LO,315}$
O4	0	1	0	$f_{LO,180}$	$f_{LO,135}$	$f_{LO,0}$	$f_{LO,315}$
O5	1	1	0	$f_{LO,180}$	$f_{LO,225}$	$f_{LO,0}$	$f_{LO,45}$
O6	1	1	1	$f_{LO,270}$	$f_{LO,225}$	$f_{LO,90}$	$f_{LO,45}$
O7	1	0	1	$f_{LO,270}$	$f_{LO,315}$	$f_{LO,90}$	$f_{LO,135}$
O8	1	0	0	$f_{LO,0}$	$f_{LO,315}$	$f_{LO,180}$	$f_{LO,135}$

Figure 4.1: (a) Eight-phase operation baseband data mapping, and (b) associated swapped complementary clock pairs based on the operating octant.

baseband signals into two non-orthogonal basis vectors with reduced relative phase differences between them. The amplitudes and required relative phases of these non-orthogonal basis vectors can be found by using the I/Q mapping as described in chapter 3. Consequently, this approach yields reduced complex loading compared to a Cartesian DTX resulting in an almost phase-independent efficiency behavior. Moreover, wideband and efficient DTX is achieved by employing a reactance compensated parallel-circuit push-pull class-E DPA [78, 79] output stage topology, combined with a wideband Marchand balun-based inverted two-way Doherty [20] power combiner exploiting re-entrant coupled lines with independent second-harmonic control.

4.2 Digital Doherty Transmitters Efficiency Comparison

In essence, in the context of an eight-phase operation, the I/Q baseband signals are mapped into two non-orthogonal basis vectors with a 45° relative phase difference, and the magnitudes are based on the corresponding octant defined in (Fig. 4.1(a)). Besides, a phase selector is required to modulate the LO clocks properly. Each octant's associated LO clock pairs are tabulated in Fig. 4.1(b) to cover the entire eight octants of the constellation diagram. To gain

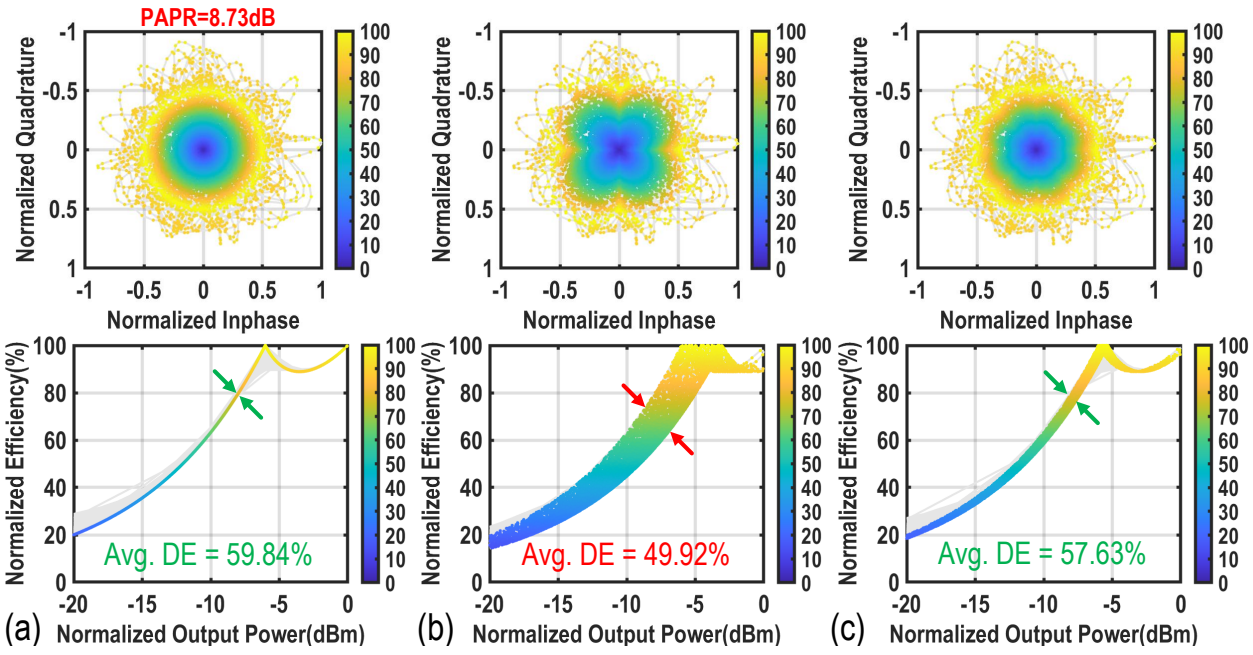


Figure 4.2: Normalized dynamic DE contour of an OFDM signal and its associated normalized DE versus normalized output power for a Doherty (a) polar (b) Cartesian, and (c) eight-phase operation DTX.

more insight, a normalized DE per trajectory point of an OFDM signal applied to a Doherty polar, Cartesian, and an eight-phase operation DTX and their corresponding normalized DE versus normalized output power are depicted in Fig. 4.2. In the polar DTX case, thanks to phase-independent efficiency for a constant amplitude (Fig. 4.2(a)), its normalized DE versus normalized output power is more confined, resulting in relatively higher average DE. As presented in Fig. 4.2(b), this plot is scattered in the Cartesian scenario due to phase-dependent efficiency behavior resulting in comparatively lower average DE. Set side by side, due to the relatively phase-independent efficiency behavior of the eight-phase operation, its corresponding plot is more confined than the Cartesian structure, slightly resembling the polar case, resulting in a somewhat higher average DE. Fig. 4.2 compares the corresponding average DE of each DTX, showing a theoretical DE improvement of 7.71% in multi-phase operation compared to Cartesian DTX. Moreover, in contrast to polar DTX, this architecture does not require the CORDIC, thus lowering the computing cost. In addition, synchronization is

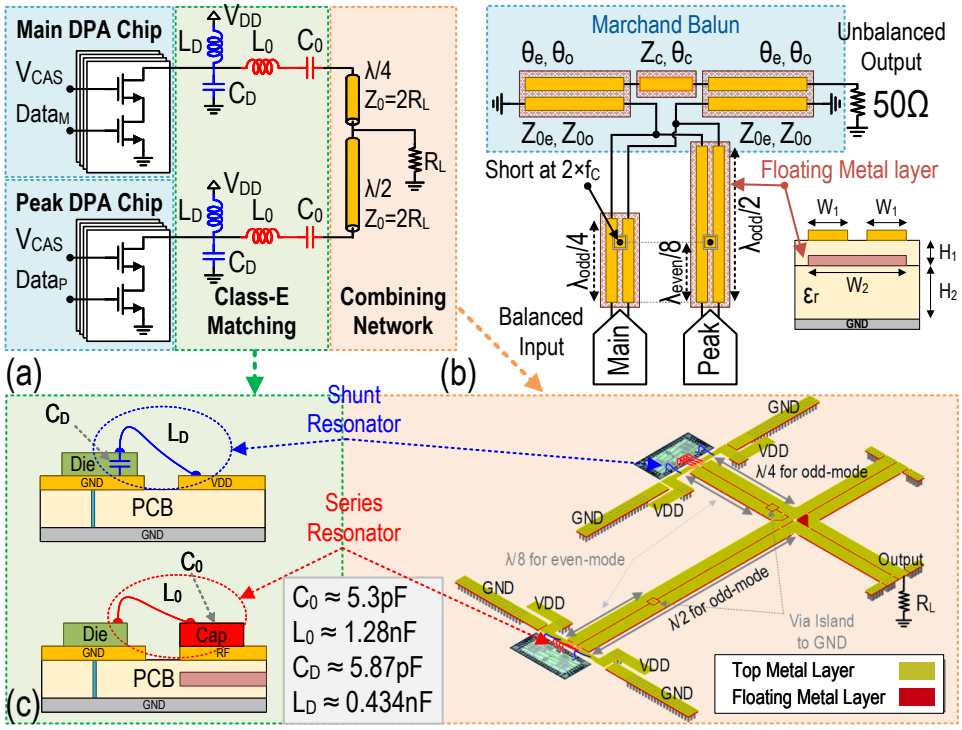


Figure 4.3: (a) Single-ended representation of the push–pull class-E Doherty DPA. (b) Doherty combining network structure. (c) Realization of the shunt and series resonators bondwiring and the Doherty combining network.

simple thanks to its symmetric architecture.

4.3 Wideband Doherty Matching Network

4.3.1 Reactance Compensated Parallel-Circuit Class-E DPA

The multi-mode CMOS chip in chapter 3 is combined with an off-chip Class-E matching network. The single-ended representation of the push-pull class-E DPA matching network topology with finite DC-feed inductance is shown in Fig. 4.3(a). A cascode power cell topology was adopted in this design to prevent reliability issues. It is shown [78] that the reactance of the series (L_0, C_0) and shunt resonant (L_D, C_D) circuits vary with frequencies,

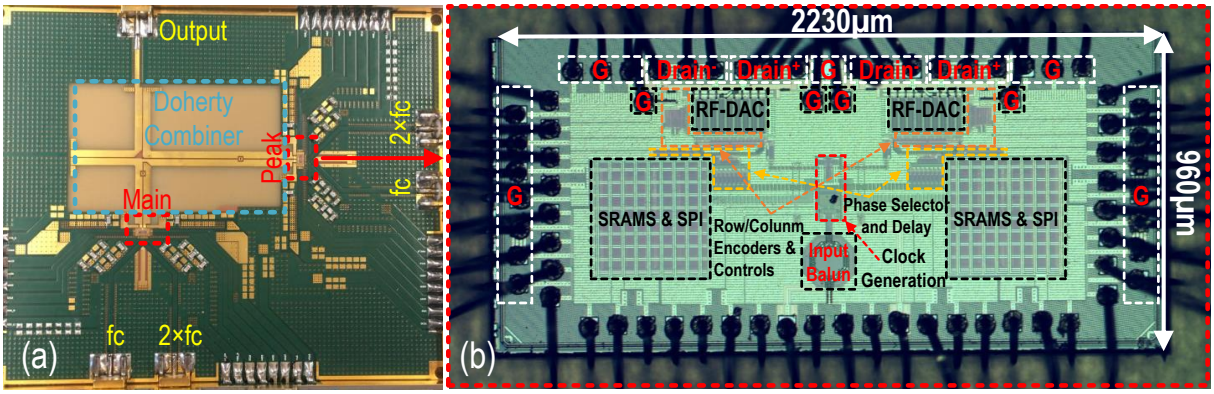


Figure 4.4: (a) Fabricated PCB (b) Die micrograph.

exhibiting an increase in the case of a series circuit and a decrease in the case of a loaded parallel circuit near the resonant frequency. To have a wideband RF operation, with a proper choice of the circuit elements, a constant load angle seen by the intrinsic drain over a large frequency bandwidth is accomplished.

4.3.2 Compensated Impedance Inverter

Figure 4.3(b) demonstrates the push-pull inverted Doherty configuration. This approach enlarges the bandwidth of the conventional Doherty combiner by adding a $\lambda/2$ transmission line (TL) in the output of the peak amplifier to compensate for the considerable variation of the magnitude and phase of the impedance seen by the main amplifier over the frequency [89].

4.3.3 Marchand Balun With Reentrant Coupled Lines and Second-Harmonic Control

A planar Marchand balun employing re-entrant coupled lines is implemented to provide a wideband balanced loading condition from a single-ended antenna load for the push-pull class-E DPA [20]. A planar Marchand balun employing re-entrant coupled lines fulfills the wideband balanced-to-unbalanced conversion. With a proper dielectric constant and dielectric layer thickness between and underneath the conductors, the re-entrant coupled lines provide higher even-mode impedance and tight differential coupling, yielding a low-loss wide-

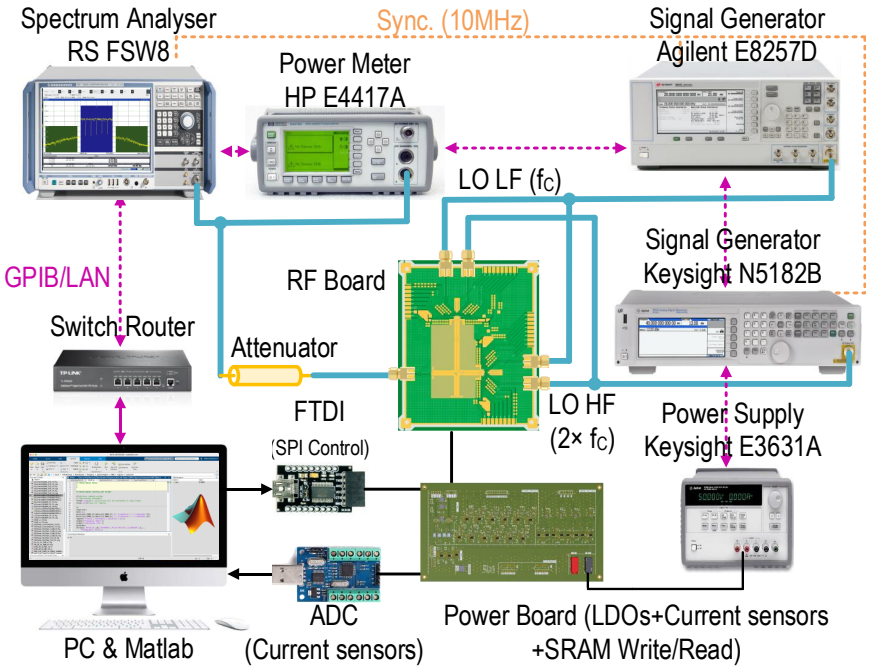


Figure 4.5: Measurement setup.

band balun. Furthermore, the network impedance provided to the differential digital class-E DPA should establish an open condition for all higher harmonics, particularly for the second harmonic. This feature is realized by providing an even-mode short-circuited condition at $\lambda/8$ distance of the DPAs, which is practically implemented by placing a simple via to ground in the center of the floating center plate conductor [20]. Due to the tight coupling between the three conductors, the top metals are inherently forced to ground for their even-mode signals, thus seen as open-circuit by the DPA at the 2^{nd} harmonic. In the odd-mode, the center of the floating metal is virtually ground, barely affecting the odd-mode impedance levels.

4.4 Fabrication and Measurement Results

The realized chip is wire-bonded to the off-chip two-way Doherty power combiner (Fig. 4.3(c)). L_0 indicates bondwires from the drain of the transistors to the off-chip passive combiner.

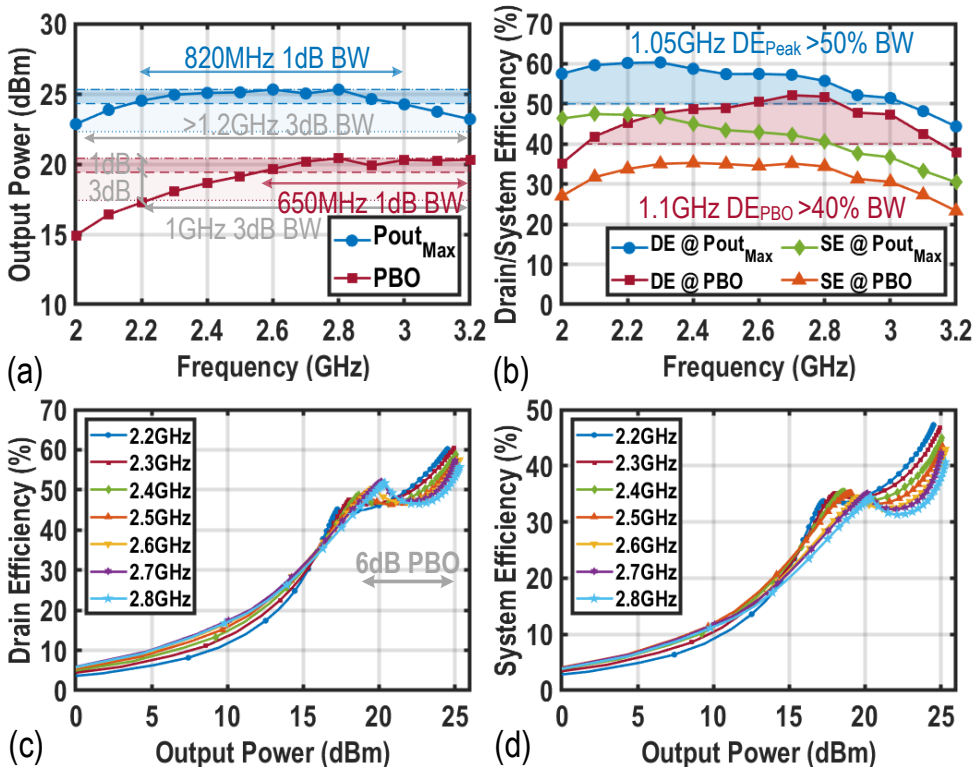


Figure 4.6: Measured Cartesian (a) output power, and (b) drain/system efficiencies at full power and power back-off vs. frequency, (c) drain, (d) system efficiency vs. output power at different frequencies.

Chip capacitors (C_0) are used to complete the implementation of the series resonator. The DC-feed inductance L_D, is also implemented using bondwires and connected to the bias lines. The baseband data of each DPA is independently applied to the DTX using four parallel on-chip 1-K SRAMs running at 600MHz.

4.4.1 Cartesian DTX Measurement Results

In a Cartesian mode, the measured peak and back-off output power over a 2-to-3.2GHz range are shown in Fig. 4.6(a), ranging from 22.8-to-25.3dBm, and 14.92-to-20.4dBm, respectively, operating from a 1V supply. The measured peak and back-off drain and system (bits-in-RF-out) efficiency (DE/SE) over the 2-to-3.2GHz range are shown in Fig. 4.6(b).

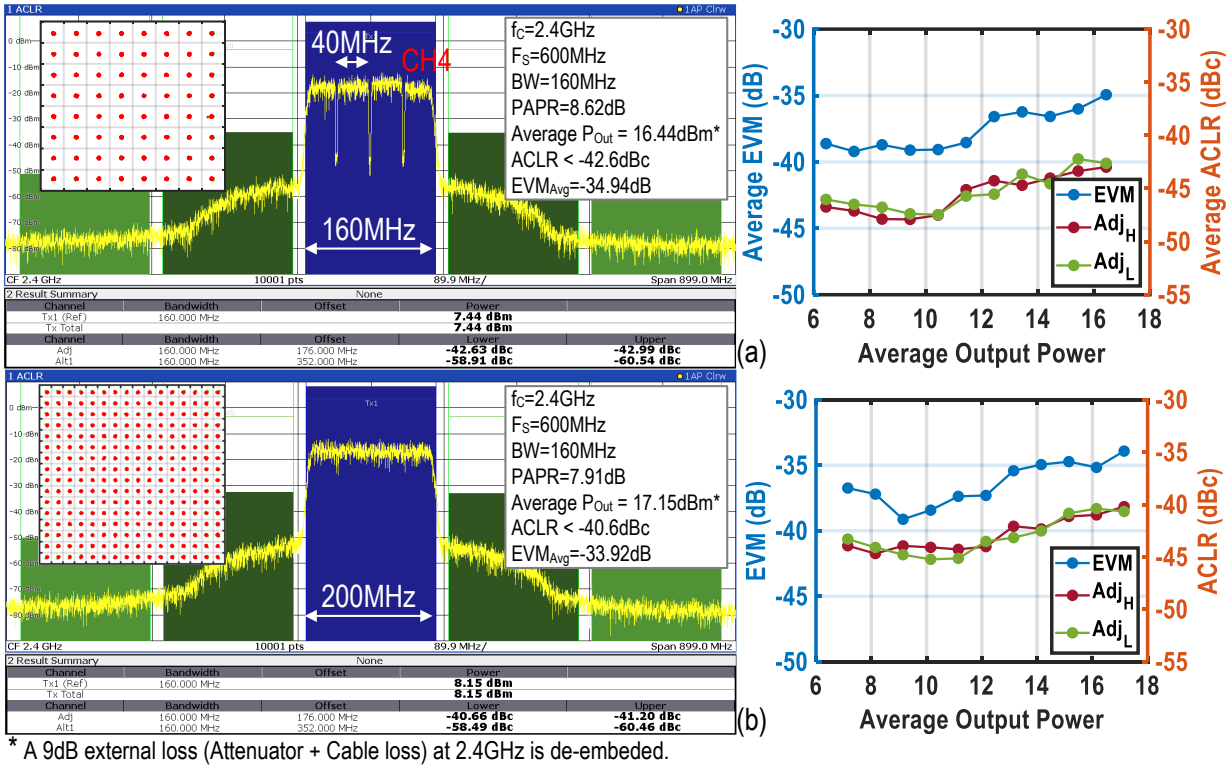


Figure 4.7: Measured results of (a) 4-channel×40MHz 64-QAM signal, and (b) single-channel 160MHz 256-QAM signal at 2.4GHz.

As can be seen, DE at peak power is more than 50% within the 2-to-3.05GHz frequency range. The DE at back-off power is more than 40% over a 1.1GHz span, equivalent to 43% relative bandwidth. The DE and SE are plotted versus output power in Fig. 4.6(c) and (d), respectively, illustrating a significant efficiency enhancement over the PBO range.

To demonstrate the carrier aggregation capability, the spectral purity of a 160MHz 4-channel 64-QAM OFDM signal is measured at 2.4GHz (Fig. 4.7(a)). With more than 16.44dBm average output power, our digital transmitter achieves an ACLR of better than -42.63dBc at an EVM of about -35dB when using a simple 2×one-dimensional memory-less DPD. The ACLR and EVM performances versus average output power are also shown, reaching better than -37dB EVM at 12dBm average power. For a 160MHz single-channel 256-QAM OFDM signal at 2.4GHz (Fig. 4.7(b)), the average delivered output power is

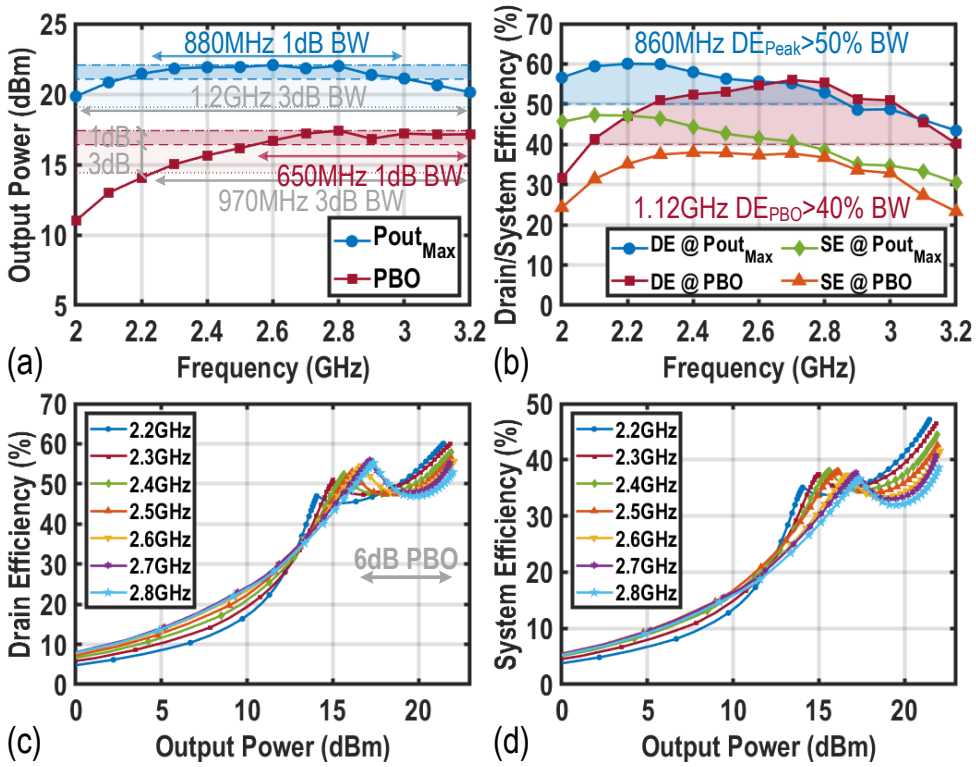


Figure 4.8: Measured eight-phase (a) output power, and (b) drain/system efficiencies at full power and power back-off vs. frequency, (c) drain, (d) system efficiency vs. output power at different frequencies.

17.15dBm (8.15dBm+9dB loss of attenuator/cable), while the ACLR and EVM are better than -40.6dBc and -33.9dB, respectively. The ACLR and EVM performances versus average output power show an EVM of better than -37dB at 12dBm average power.

4.4.2 Multi-phase DTX Measurement Results

In a multi-phase scenario, the measured peak and back-off output power over a 2-to-3.2GHz range are shown in Fig. 4.8(a), ranging from 19.84-to-22.1dBm, and 11-to-17.4dBm, respectively, operating from a 1V supply. The measured peak and back-off drain and system efficiency (DE/SE) are shown in Fig. 4.8(b). As can be seen, DE at peak power is more than 50% within the 2-to-2.86GHz frequency range. The DE at back-off power is more than 40%

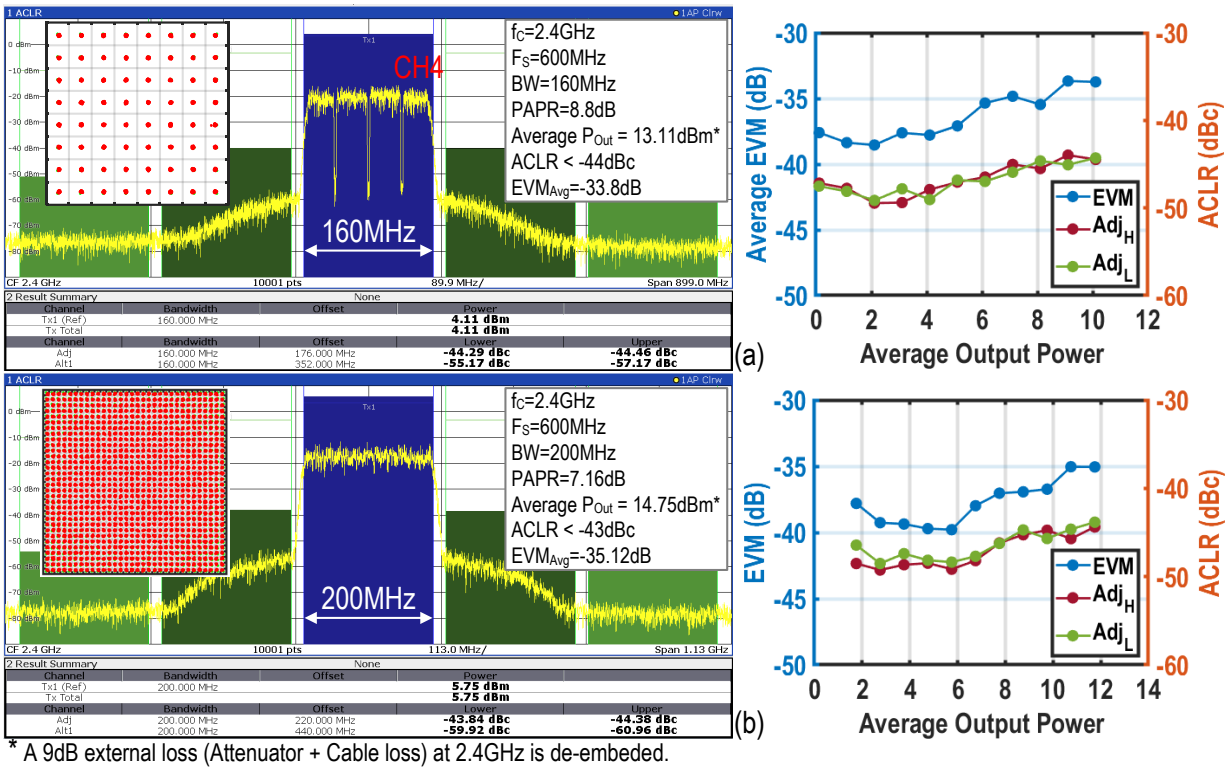


Figure 4.9: Measured results of (a) 4-channel×40MHz 64-QAM signal, and (b) single-channel 200MHz 1024-QAM signal at 2.4GHz.

over a 1.12GHz span, equivalent to 46.67% relative bandwidth. The DE and SE are plotted versus output power in Fig. 4.8(c) and (d), respectively, illustrating a significant efficiency enhancement over the PBO range.

A 4-channel×40MHz 256-QAM OFDM signal with an aggregated bandwidth of 160MHz is applied to the DTX, and the performance is verified at f_C= 2.4GHz using the simple fixed memoryless 2×1-D DPD. Fig. 4.9(a) exhibits the measured spectrum of the signal and its CH4 constellation diagram. Accordingly, the DTX delivers 13.11dBm average power while achieving an ACLR of better than -44.29dBc and an average EVM of -33.8dB. The measured average drain and system efficiencies are 42.8% and 32.2%, respectively. The ACLR and average EVM performances versus average output power are also exhibited, achieving -35.5dB average EVM at 6dBm average power while the ACLR is better than -46dBc. Furthermore,

Table 4.1: Performance Summary And Comparison With State-Of-The-Art

Specifications		This Work				ISSCC 2022 B. Khamaisi	JSSC 2021 B. Yang	TMTT 2019 M. Hashemi	JSSC 2021 M. Beikmirza	JSSC 2017 V. Vorapipat
Technology		CMOS 40nm				FinFET 16nm	CMOS 40nm	CMOS 40nm	CMOS 40nm	CMOS 65nm
DPA Architecture		Multi-phase Class-E		Cartesian Class-E		Polar	Quadrature SCPA/ Hybrid Doherty	Polar Class-E	Cartesian CMCD	Voltage Mode Doherty
Matching Network		Off-Chip				On-Chip	On-chip	Off-Chip	On-Chip	Off-chip
Die Area (mm^2)		2.1 (0.72 ‡)				1.2 ¥	2.2	0.45	3.55 (1.5 ‡)	1.62
Supply (V)		1				1.2	1.2/2.4	0.7	1	1.2/2.4
1dB RF Bandwidth		860MHz		820MHz		N/A	500MHz**	800MHz**	600MHz	300MHz
Relative RF BW		35.8%		34.1%		N/A	20.8%	32%	11.1%	33%
Peak P_{out} (dBm)		22.1		25.3		28.2	30.3	17.5	27.4	24
DE/SE (%)	Peak	57.97 / 44.41		58.7 / 44.9		N/A / 25%	41.3/36.5	54 / 34	47.4 / 30.6	N/A / 45
	6dB PBO	52.43 / 37.99		48.6 / 35.2		33 / 21%**	36.1/29.1	52 / 25	43.4 / 26.3	N/A / 34
Frequency (GHz)		2.4				2.4	2.4	2.5	5.4	0.9
Modulation scheme		1024-QAM OFDM	64-QAM OFDM	256-QAM OFDM	64-QAM OFDM	MCS11	256-QAM	64-QAM OFDM	256-QAM OFDM	256-QAM 802.11ac
Bandwidth (MHz)		200	4×40	160	4×40	40	60	32	240	40
PAPR (dB)		7.16	8.8	7.91	8.62	N/A	6.98	N/A	9.6	9
Avg. P_{out} (dBm)		14.75	13.11	17.15	16.44	20	23.3	N/A	17.8	14.7
Avg. DE/SE (%)		46.02 / 34.33	42.8/33.2	46.1 / 32.7	43.4 / 30.6	N/A / 16.6	30.7/N/A	N/A	41.2 / 22.1	N/A / 22
EVM (dB)		-35.12	-33.8	-33.92	-34.94	-35 (@7.3 PBO)	-31.9	-48	-32.2	-34.8
ACLR (dBc)		-43.84/-44.38	-44.29/-44.46	-40.6/-41.2	-42.6/-42.9	N/A	-32/-30	-48.5/-48.3	-39/-39	-40 / -40**
Linearization		Memory-less DPD				Memory-effect DPD	DPD	ILC DPD	Static DPD	Memory-less LUT

• ** Estimated from reported figures and plots. ‡ Core area. ¥ Area including Digital front end, DPLL, and LB/HB DTX.

a 200MHz single-channel 1024-QAM OFDM signal at 2.4GHz is generated (Fig. 4.9(b). The average delivered output power is 14.75dBm, while the ACLR and EVM are better than -43.84dBc and -35.12dB, respectively. The ACLR and average EVM performances versus average output power are also exhibited reaching –39.32dB average EVM at X6dBm average output power, while the ACLR is better than -48.24dBc.

The performance of the proposed DTX is summarized in Table 4.1. From this comparison, it works out that the proposed architecture exhibits the highest data rate, and high average efficiency.

4.5 Conclusion

In this chapter, a multi-phase inverted Doherty digital transmitter is realized to alleviate the notorious disadvantages of the polar and Cartesian DTXs. This architecture inherits the advantages of the Cartesian DTX, such as wideband operation, symmetrical and synchronized I/Q paths with a drain efficiency behavior that approaches the polar DTX. The off-chip power combiner enables wideband Doherty operation over the 2-to-3.2GHz frequency band with 22.1dBm peak output power while maintaining more than 57.97%/44.41% drain/system efficiency. Delivering 14.75dBm average output power with 46.02%/34.33% average drain/system efficiency for a 200MHz 1024-QAM OFDM signal, its EVM and ACLR are better than -35dB and -43dB, respectively, employing a simple DPD.

Chapter 5

A Wideband Four-Way Doherty Bits-In RF-Out CMOS Transmitter

This chapter is written based on [50, 82].

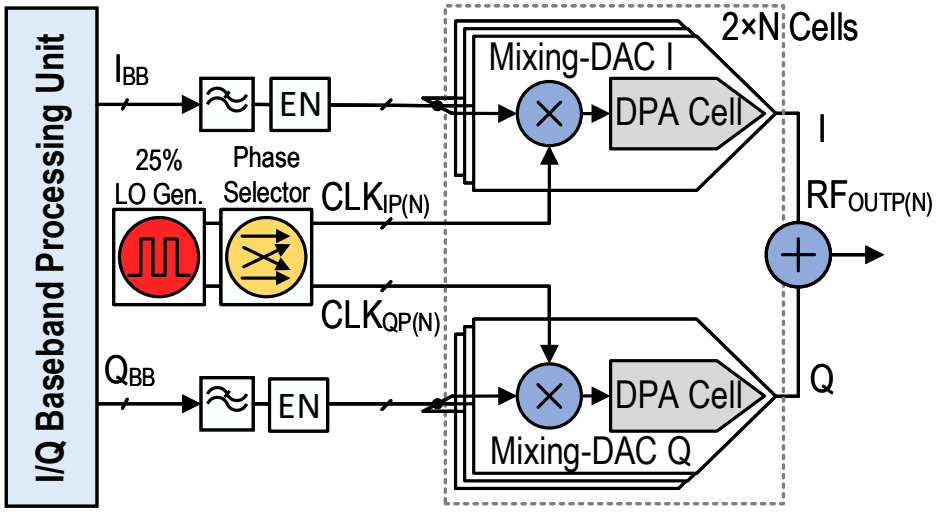
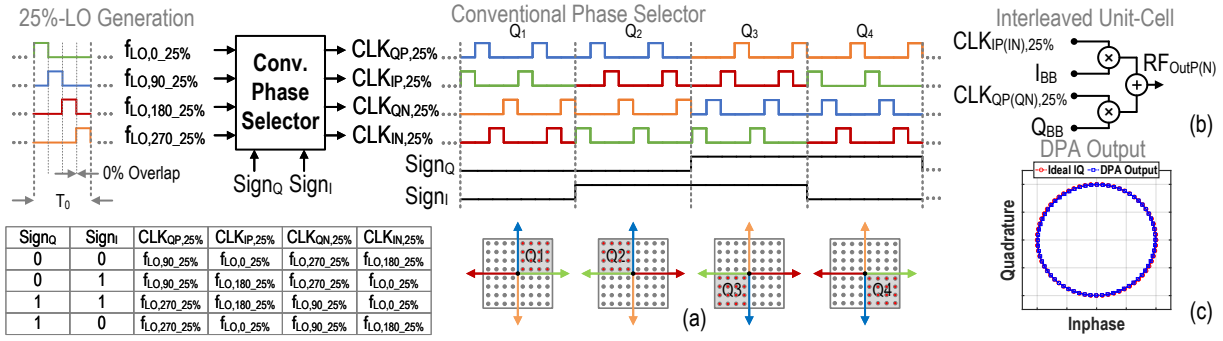


Figure 5.1: Conventional 25%-LO I/Q DTX with its signed I/Q phase selector.

5.1 Introduction

Over the last few years, digital transmitters (DTXs) have increasingly gained popularity as they supersede the circuit building blocks of conventional analog-intensive TXs with radio-frequency digital-to-analog converters (RF-DACs) [29, 47, 48, 53, 90–105]. These bits-in RF-out TXs feature digital interpolation filters and arrays of digital up-converters with their subsequent digital power amplifiers (DPAs). They offer several advantages: highly efficient operation, direct-digital synthesis (DDS) capability, frequency-agile operation, multi-mode/multi-band functionality, and nanoscale CMOS compatibility, enabling higher integration and reduced die area. Despite these benefits, next-generation DTXs must be augmented by circuit, system, and architectural innovations to satisfy the stringent requirements of modern communication standards. As a result, they must support spectrally efficient wideband modulation schemes, achieve low error vector magnitude (EVM), and meet TX spurious emission requirements. Generally, in-phase/quadrature (I/Q) DTXs are considered superior for wideband application over their polar counterparts due to their linear I/Q operation that avoids bandwidth expansion [59, 60, 62].

Nevertheless, I/Q DTXs can suffer from the interaction between their I and Q paths, especially at higher power levels, giving rise to an I/Q image, in-band nonlinearity, and



$Sign_Q$	$Sign_I$	$CLK_{QP,25\%}$	$CLK_{IP,25\%}$	$CLK_{QN,25\%}$	$CLK_{IN,25\%}$
0	0	$f_{LO,90\_25\%}$	$f_{LO,0\_25\%}$	$f_{LO,270\_25\%}$	$f_{LO,180\_25\%}$
0	1	$f_{LO,90\_25\%}$	$f_{LO,180\_25\%}$	$f_{LO,270\_25\%}$	$f_{LO,0\_25\%}$
1	1	$f_{LO,270\_25\%}$	$f_{LO,180\_25\%}$	$f_{LO,90\_25\%}$	$f_{LO,0\_25\%}$
1	0	$f_{LO,270\_25\%}$	$f_{LO,0\_25\%}$	$f_{LO,90\_25\%}$	$f_{LO,180\_25\%}$

Figure 5.2: 25%-LO with conventional phase selector operation. (a) Resulting up-converting quadrature clocks waveforms. (b) Idealized interleaved unit-cell. (c) Simulated single-sideband constellation diagram.

spectral regrowth. As depicted in Fig. 5.1, the DTX in [70] uses 25% quadrature clocks and a signed I/Q phase selector to alleviate the I/Q interaction. However, the I/Q interaction predominately remains due to the analog I/Q summation that is prone to mismatch and excessive output parasitics. The design reported in [52] applies an I/Q power-cell sharing method based on time-division multiplexing. In this approach, the up-converted I/Q signals are digitally added together while sharing a single power-cell, coined as I/Q-sharing architecture. Still, it requires 25%-LO, which is challenging to realize in the 5GHz band due to its excessive power consumption of the LO clocks. Alternatively, [106] deploys 50% clocks while adopting the phase selector of [70]. Nonetheless, employing 50% quadrature clocks due to their inherent overlap causes a non-orthogonal operation and distortion, entailing sophisticated digital pre-distortion (DPD).

On the other hand, modern communication standards employ modulation schemes such as 256- quadrature-amplitude modulation (QAM) orthogonal-frequency division multiplexing (OFDM). These modulation schemes feature a high peak-to-average-power ratio (PAPR) (e.g., >10dB) which requires the DTX to operate in deep power back-off (DPBO), degrading its average efficiency. Many efficiency enhancement techniques such as out-phasing [37, 107, 108], envelop-tracking (ET) [109], and Doherty [49, 87, 110–114] are currently adopted in various DPA topologies to enhance their efficiency at DPBO. Two-way Doherty DPAs (DDPAs) are popular due to their less complicated baseband processing and handling large

modulation bandwidth, but they typically enhance efficiency at 6-dB PBO. The N-way DDPA improves the efficiency at DPBO while maintaining the simplicity advantage of the DDPA configuration. However, it is incredibly challenging to implement an N-way DDPA since incorporating more DPA banks leads to excessive power combiner losses. In [87], a 3-way DDPA architecture with decent overall linearity/efficiency performance has been reported.

Recently in [50], we have introduced a 4-way DTX that achieves decent EVM, spectral purity, and efficiency at DPBO. It comprises a 50%-LO signed I/Q up-converter that facilitates close-to-perfect orthogonal I/Q summation. Moreover, it incorporates a push-pull low-loss 4-way DDPA to enhance its average efficiency. This chapter elaborates on the system-/circuit-level design considerations and extensive measurement results. Section 5.2 introduces the proposed 50%-LO signed I/Q technique. Section 5.3 unveils the compact 4-way DDPA. Section 5.4 describes the TX architecture, while Section 5.5 demonstrates the measurement results. Section 5.6 concludes the chapter.

5.2 50%-LO Signed I/Q Interleaved Up-Converter

5.2.1 Conventional Phase Selector Operation

5.2.1.1 25%-LO with Conventional Phase Selector Operation

Fig. 5.2 demonstrates the conventional phase selector operation concept with a 25%-LO clock [64]. Conventionally, to minimize the distortion due to the I/Q overlap, non-overlapping complementary quadrature clocks with a 25% duty cycle are required. In this context, the clock tree is typically implemented using a phase selector that operates directly on these short 25%-LO clocks ($f_{LO,0\_25\%}$, $f_{LO,90\_25\%}$, $f_{LO,180\_25\%}$, $f_{LO,270\_25\%}$). Depending on the four states of the I/Q sign-bits, the related complementary clock pairs can be swapped (Fig. 5.2(a)). Note that in this conventional approach, the Q sign-bit ($Sign_Q$) only acts on the QP/QN related clocks $CLK_{QP,25\%}/CLK_{QN,25\%}$, while the I sign-bit ($Sign_I$) only operates on the IP/IN related clocks $CLK_{IP,25\%}/CLK_{IN,25\%}$. For example, in the case of a transition from the first quadrant ($Sign_Q$=0, $Sign_I$=0) to the fourth one ($Sign_Q$=1, $Sign_I$=0), since the sign of Q is changed, the corresponding complementary clocks, $CLK_{QP,25\%}/CLK_{QN,25\%}$, are swapped (see table in Fig. 5.2). These 25% phase-modulated LO clocks are then directly mixed with the

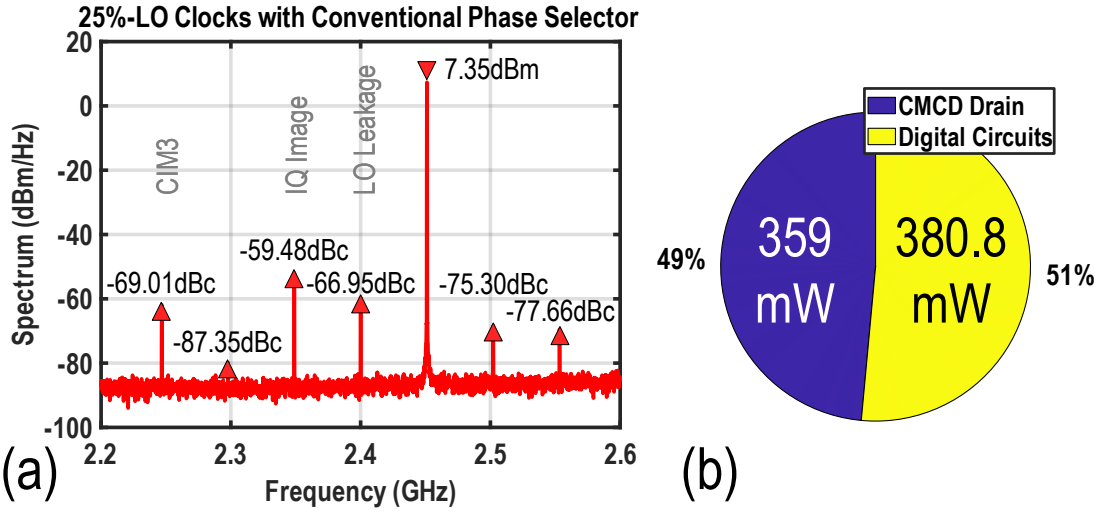


Figure 5.3: (a) Single-sideband spectrum with 100MHz tone-spacing at 2.4GHz employing 25%-LO clocks with the conventional phase selector. (b) Power consumption breakdown.

up-sampled baseband data (see Fig. 5.2(b)), driving in the subsequent power cells to cover the targeted constellation quadrants. Fig. 5.2(c) shows the simulated single-sideband constellation diagram of the conventional phase selector, indicating correct sign-bit operation without compression due to non-overlapping 25%-LO quadrature clocks. Nonetheless, since this phase selector exploits 25% quadrature LO clocks, it entails practical limitations and causes various issues in the DTX clock trees. Firstly, compared to using 50%-LO clocks, their rise/fall times in the clock tree must be very short, requiring faster buffers in the clock tree and consuming more DC power. Therefore, this approach is less attractive at higher frequencies. Secondly, compared to 50%-LO clocks, their 25% counterparts are not inherently symmetric and balanced, making them more prone to signal interference, DC offsets, and abrupt transient conditions (e.g., due to the changing sign-bits). These issues yield timing inaccuracies in practical implementations, which, in turn, give rise to performance nonidealities such as limited I/Q image rejection and unwanted spectral leakage spurs, especially at higher frequency bands [102, 115–117]. These TX spectral spurs increase the far-out spectral noise floor at receiver (RX) bands, which is detrimental. The single-sideband spectrum with 100MHz tone-spacing and the power consumption breakdown at 2.4GHz employing global 25%-LO clocks with conventional phase selector is presented in Fig. 5.3. Accordingly, its

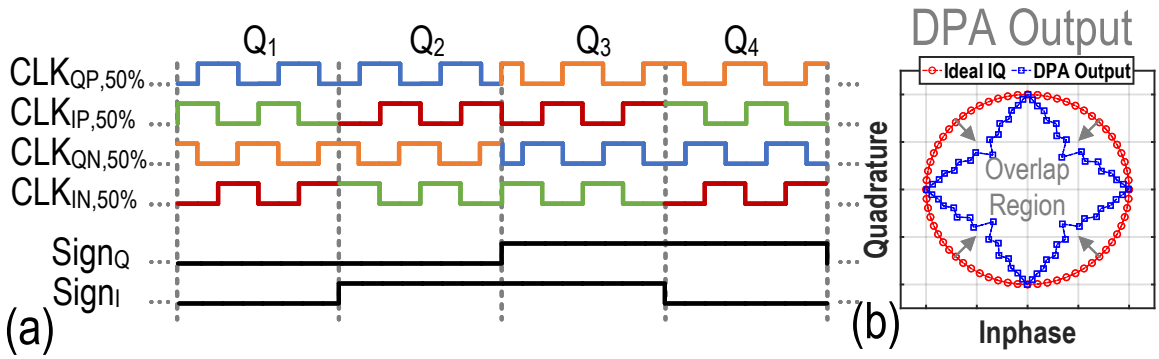


Figure 5.4: (a) Resulting up-converting quadrature clocks waveforms of 50%-LO with conventional phase selector operation. (b) Simulated single-sideband constellation diagram.

I/Q-image is -59dBc, while its digital circuit blocks consume 380.8mW. The performance of this conventional arrangement will be compared to the proposed method in section 5.2.2.

5.2.1.2 50%-LO With Conventional Phase Selector Operation

To address the issues mentioned above, Fig. 5.4(a) illustrates the resulting waveforms of applying the conventional phase selector to 50% quadrature LO clocks. Accordingly, this setup leads to a correct quadrant selection depicted in Fig. 5.4(b). However, it causes distortions due to an I/Q overlap which significantly deteriorates the image-rejection ratio, in-band linearity, and close-in spectral purity [106,118,119]. To mitigate this issue, 25% quadrature LO clocks are required when both I and Q are active. Therefore, 25% complementary quadrature LO clocks are generated by multiplying the adjacent 50%-LO clocks together (Fig. 5.5(a)). However, after applying these 25%-LO clocks to the up-sampled baseband data, as shown in Fig. 5.5(b), it turns out that the sign-bit operation is incorrect even when using these 25% non-overlapping clocks. Fig. 5.5(c) compares this latter case with the conventional phase selector using 25%-LO clocks. As illustrated, the resulting clock waveforms are correct in the first/third quadrant (alternate quadrant traverse). Nonetheless, the modified phase selector does not replicate the suitable clock waveforms in the second/fourth quadrant (adjacent quadrant traverse). The reason lies in the fact that both I and Q sign-bits change in an alternate quadrant traverse case, and thus, the clocks preserve their lead/lag phase relation.

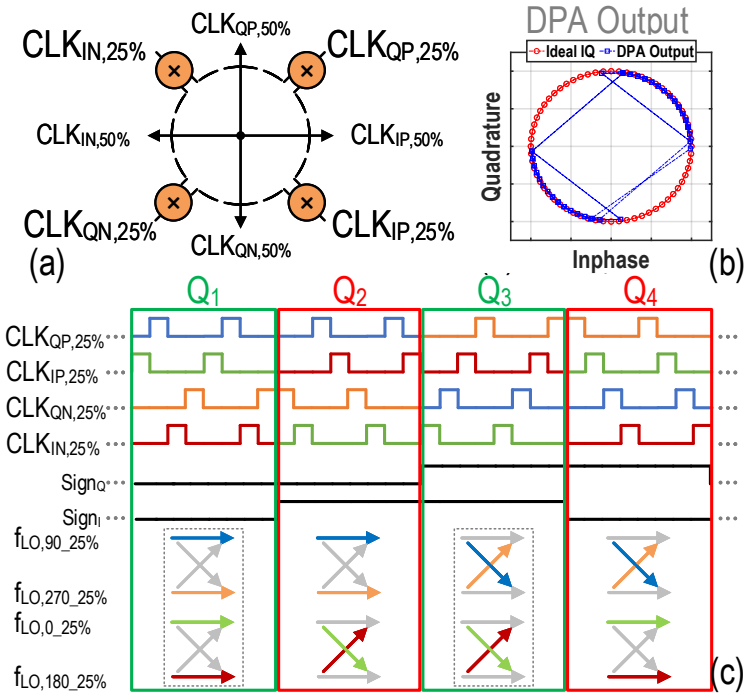
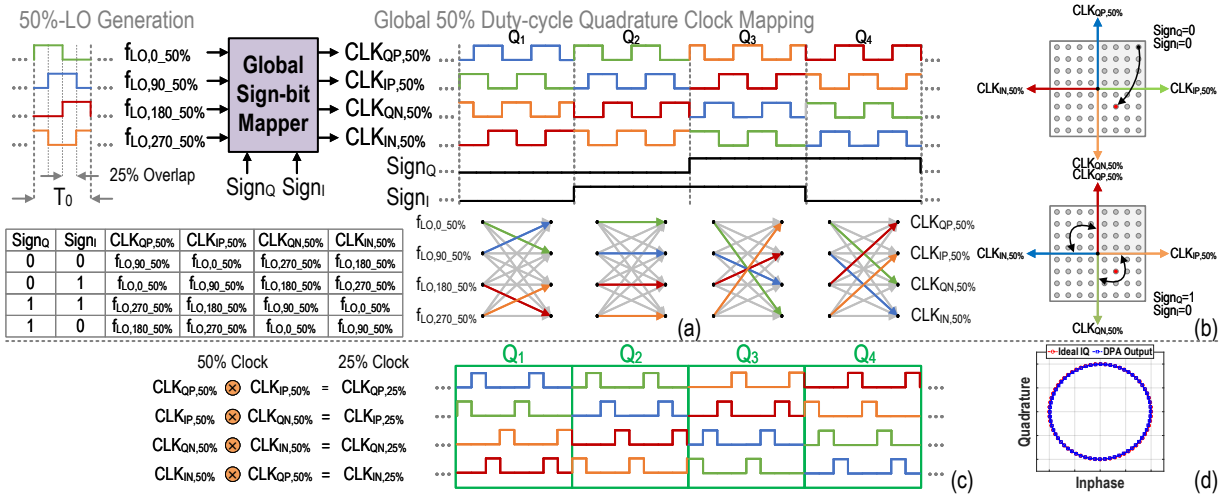


Figure 5.5: (a) A possible implementation diagram of 25% clock generation by multiplying the adjacent 50%-LO clocks. (b) Simulated single-sideband constellation diagram. (c) Resulting 25% quadrature clocks waveforms.

On the other hand, in an adjacent quadrant traverse condition, one of the I or Q sign-bits change. Therefore, the clocks do not preserve their lead/lag phase relation. To tackle this issue, we propose a new 50%-LO signed I/Q interleaved up-converter.

5.2.2 Proposed 50%-LO Signed I/Q Interleaved Up-converter

The proposed signed I/Q interleaved up-converter addresses this issue by exploiting global 50%-LO clocks, phase modulated by the sign-bits, along with a new single-sideband I/Q digital up-converter. In this method, the DTX quadrant selection (sign-mapping operation) is realized in two steps: 1) Global 50% duty-cycle quadrature clock mapping and 2) Local I/Q up-conversion and I/Q interleaving. The remainder of this section elaborates further on the details of these two steps and their design considerations.



$Sign_Q$	$Sign_I$	$CLK_{QP,50\%}$	$CLK_{IP,50\%}$	$CLK_{QN,50\%}$	$CLK_{IN,50\%}$
0	0	$f_{LO,90\_50\%}$	$f_{LO,0\_50\%}$	$f_{LO,270\_50\%}$	$f_{LO,180\_50\%}$
0	1	$f_{LO,0\_50\%}$	$f_{LO,90\_50\%}$	$f_{LO,180\_50\%}$	$f_{LO,270\_50\%}$
1	1	$f_{LO,270\_50\%}$	$f_{LO,180\_50\%}$	$f_{LO,90\_50\%}$	$f_{LO,0\_50\%}$
1	0	$f_{LO,180\_50\%}$	$f_{LO,270\_50\%}$	$f_{LO,0\_50\%}$	$f_{LO,90\_50\%}$

Figure 5.6: Proposed global 50% duty-cycle quadrature clock mapping operation. (a) Resulting up-converting quadrature clocks waveforms. (b) An example for the first quadrant to the fourth quadrant transition. (c) Resulting 25% clocks generated by multiplying the adjacent 50%-LO clocks. (d) Simulated single-sideband constellation diagram.

5.2.2.1 Step 1: Global 50% Duty-Cycle Quadrature Clock Mapping

Fig. 5.6(a) gives the graphical representation of this step. The DTX clock tree uses 50% square-wave LO clocks ($f_{LO,0\_50\%}$, $f_{LO,90\_50\%}$, $f_{LO,180\_50\%}$, $f_{LO,270\_50\%}$), and the conventional clock phase selector described above in Fig. 5.2 is replaced by the proposed sign-bit phase mapper. As illustrated, in the first step, based on the I/Q sign-bit states, the 50% quadrature clocks are swapped in a particular fashion that contrasts with the typical approach, whose complementary clocks are swapped. The table in Fig. 5.6 summarizes the phase mapping relations for the proposed 50%-LO clocks. In this approach, the I sign-bit impacts both the I-related clock signals ($CLK_{IP,50\%}/CLK_{IN,50\%}$) operation and, more importantly, the Q-related clocks ($CLK_{QP,50\%}/CLK_{QN,50\%}$). Similarly, the Q sign-bit affects both Q-/I-related clocks. For example, in the transition from the first quadrant to the fourth one, in the first step, 50%-LO clocks of CLK_{QP}/CLK_{QN} are swapped with CLK_{IN}/CLK_{IP}, respectively (Fig. 5.6(b)). The proposed 50%-LO quadrature sign-bit mapper scheme enables simple multiplication actions on the resulting clocks ($CLK_{QP,50\%}$, $CLK_{IP,50\%}$ $CLK_{QN,50\%}$, $CLK_{IN,50\%}$)

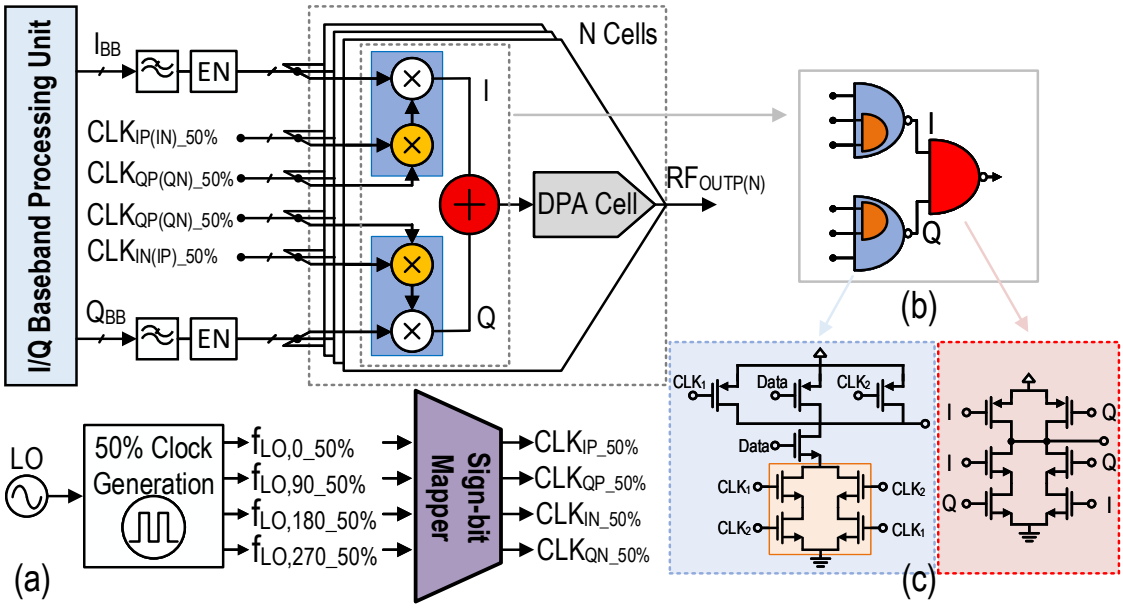


Figure 5.7: (a) Schematic diagram of the local 25%-LO clock generation, I/Q up-conversion, and interleaving. (b) NAND gate-based logical implementation circuitry. (c) 2-/3-input symmetrical NAND logic gates.

to adequately generate 25% up-converting LO clocks for the unit cells, which is described in the next step.

5.2.2.2 Step 2: Local I/Q Up-Conversion And I/Q Interleaving

To complete the up-conversion operation, the required 25%-LO clocks are generated by multiplying the appropriate pair of the phase-modulated 50%-LO quadrature clocks together. A possible implementation is illustrated in Fig. 5.6(c), showing the generation of the local 25%-LO clocks in each RF-DAC sub-cell ($\mathrm{CLK_{QP,25\%}}$, $\mathrm{CLK_{IP,25\%}}$, $\mathrm{CLK_{QN,25\%}}$, $\mathrm{CLK_{IN,25\%}}$), by bit-wise multiplying of their corresponding 50% clocks ($\mathrm{CLK_{QP,50\%}}$, $\mathrm{CLK_{IP,50\%}}$, $\mathrm{CLK_{QN,50\%}}$, $\mathrm{CLK_{IN,50\%}}$) with their clockwise adjacent clock ($\mathrm{CLK_{IP,50\%}}$, $\mathrm{CLK_{QN,50\%}}$, $\mathrm{CLK_{IN,50\%}}$, $\mathrm{CLK_{QP,50\%}}$), respectively. Accordingly, as illustrated in Fig. 5.6(c), the resulting 25% clocks replicate the required clock waveforms in all quadrants. Fig. 5.7(a) conceptually shows how the 25%-LO clock signals are generated and multiplied with their baseband signals, i.e., $\mathrm{I_{BB}}$ and $\mathrm{Q_{BB}}$, performing the up-conversion. The up-converted I/Q bitstreams are combined to fulfill I/Q

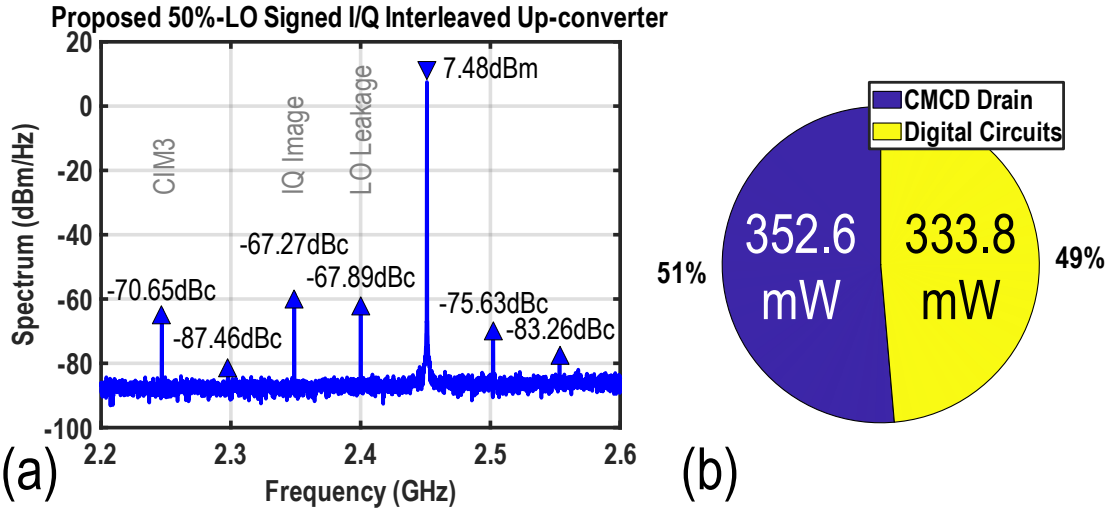


Figure 5.8: (a) Single-sideband spectrum with 100MHz tone-spacing at 2.4GHz employing the proposed 50%-LO signed I/Q interleaving up-converter. (b) Power consumption breakdown.

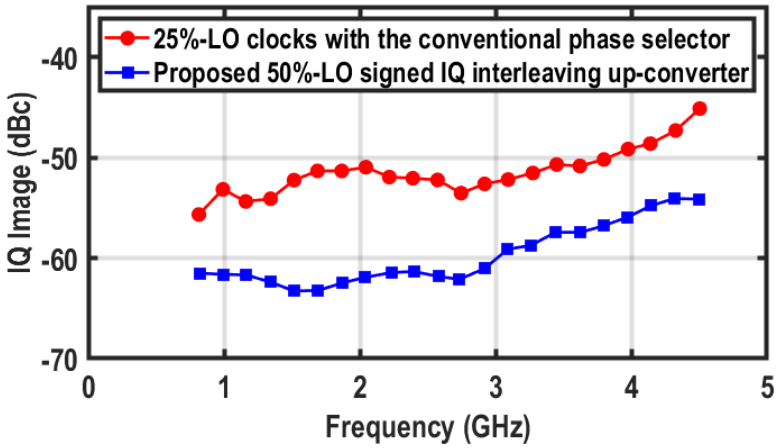


Figure 5.9: Measured (with the chip presented in chapter 3) single-sideband performance with 200MHz tone-spacing over frequency band employing 25%-LO clocks with the conventional phase selector and the proposed 50%-LO signed I/Q interleaving up-converter.

interleaving. Fig. 5.6(d) presents the simulation results of the proposed 50%-LO signed I/Q interleaved up-converter concept showing accurate sign-bit operation without compres-

sion. It is worth mentioning that the local 25%-LO clock generation and up-conversion are performed using 3-input NAND gates (Fig. 5.7(b)). As stated above, 50%-LO clocks are inherently symmetrical. Therefore, they will be less prone to electromagnetic couplings and interferences, especially when the clock lines are implemented symmetrically. In addition to these symmetrical conditions, the logic gates used for the sign-bit mapper, local I/Q up-conversion, and interleaving circuits are also fully symmetrical to their inputs. Most traditional logic gates do not have this feature. For example, a conventional NAND logic gate is inherently asymmetrical. Therefore, it does not offer precise symmetrical loading to the incoming phase-modulated clock lines. This arrangement jeopardizes the DTX operation due to interfering signals and leads to timing errors. A NAND gate circuitry comprising symmetrical logic gates is employed to address this issue, which provides symmetric input loading and transfer function (Fig. 5.7(c)). By making the clock tree and its loading fully symmetrical, the timing error is remarkably diminished. The single-sideband spectrum with 100MHz tone-spacing and the power consumption breakdown at 2.4GHz of the proposed global 50%-LO signed I/Q interleaved up-converter is presented in Fig. 5.8. Accordingly, the DPA's I/Q-image is -67dBc, while its digital circuit blocks consume 333.8mW. Compared to Fig. 5.3, the I/Q-image, and DC power consumption are boosted by 8dB, and reduced by 47mW, respectively, at 2.4GHz. Nevertheless, as illustrated in Fig. 5.9, at higher operational frequencies, employing global 25%-LO clocks becomes impractical, leading to performance degradation. Consequently, the proposed technique facilitates high-frequency I/Q up-conversion by utilizing symmetrical, balanced, and matched 50% quadrature LO clocks in a two-step I/Q phase modulator. Using 50%-LO clocks has benefits that significantly enhance orthogonal summation and system efficiency. Its advantages are: 1) It lowers the impact of the clock line electromagnetic couplings and parasitics; 2) It has more immunity to the duty-cycle distortion; 3) The LO signals in the clock trees are more robust to interfering signals due to their symmetrical operation and balanced loading; 4) It consumes less power, and; 5) It improves its in-band linearity and close-in/far-out spectral purity.

5.3 Doherty Power Combining Network

As mentioned in Section 5.1, to obtain highly efficient operation at DPBO and generate relatively high average RF power in CMOS technology, a compact 4-way Doherty digital

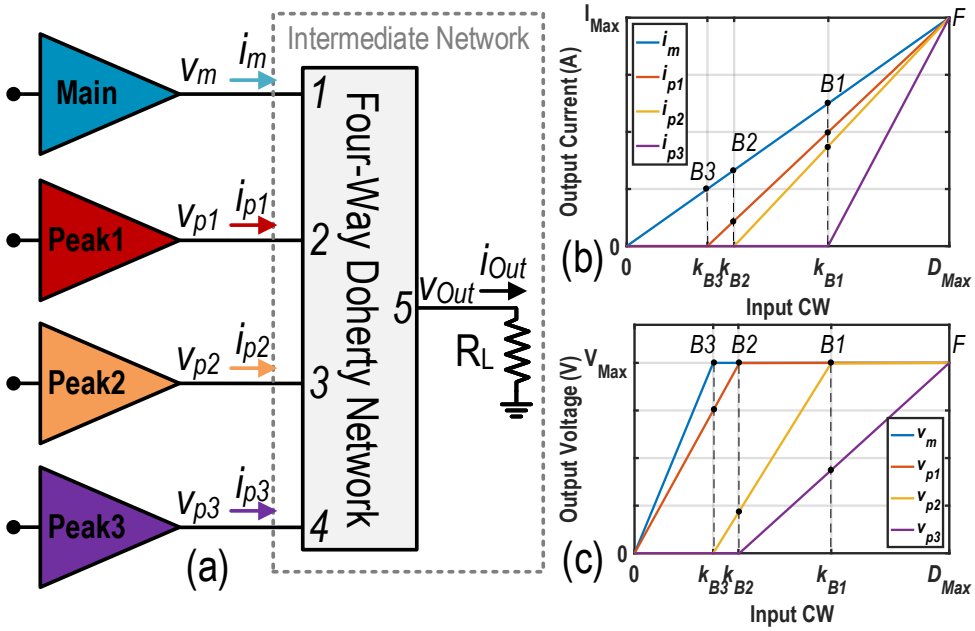


Figure 5.10: (a) General 4-way DPA with lossless power combining network. (b) and (c) Output current and voltage profiles versus input codeword.

power amplifier is introduced. Its power combining network comprises four input ports and one RF output for the 50Ω antenna connection. To facilitate the design of the 4-way combiner, an approach similar to [31] has been adopted to design various types of 4-way DDPA power combining networks. In this context, as shown in Fig. 5.10(a), first, the designated 5-port power combiner is considered as a 5-port black box. Next, its ports' current profiles are determined based on a given set of three free-to-choose peak efficiency power back-off points (i.e., k_{B1}, k_{B2}, and k_{B3} in Fig. 5.10(b)). The power combining network is assumed to be lossless and reciprocal. Nevertheless, an intermediate network that includes the power combining network and the DDPA load, R_L, is hypothetically considered to reduce the 5-port to 4-port configuration. The intermediate network is still reciprocal but no longer lossless because of the 50Ω lossy load component. The z-parameters can be expressed in terms of voltages and currents by solving (5.1), where the subscripts m and pi (i=1 to 3) represent the main and peak$i$ (i=1 to 3) DPAs, respectively. The second subscripts F, Bi (i=1 to 3) represent the full power and back-off points, which are related to its full power by

factors of ${k_{B1}}^2$, ${k_{B2}}^2$, and ${k_{B3}}^2$, respectively. The next step is to determine all of the voltage and current variables at the output of each DPA to determine the z-parameters of the intermediate network uniquely. It is worth noting that different sets of boundary conditions result in various power combining networks. In this work, however, the output current of all DPAs at their maximum, i.e., I_{Max}, is considered to be equal, which occurs at full power (F). Due to this boundary condition, the proposed DTX comprises four identical DPA banks to implement the main and peaking power devices. Furthermore, the corresponding peaking DPAs are off before their corresponding back-off points and are active beyond their related back-off point. Thus, the following boundary conditions are considered:

$$\begin{aligned} &i_{m,F} = i_{p1,F} = i_{p2,F} = i_{p3,F} = I_{Max} \\ &i_{p1,B3} = i_{p2,B3} = i_{p2,B2} = i_{p3,B1} = i_{p3,B2} = i_{p3,B3} = 0 \end{aligned} \tag{5.2}$$

On the other hand, to maximize the efficiency at full power and the three other back-off points Bi (i=1 to 3), the RF voltage amplitude at the output of the relevant devices (main, peak1, peak2, and peak3) has to be maximized at these points, as depicted in Fig. 5.10(c).

$$\begin{aligned} |v_{m,F}| = |v_{m,B1}| = |v_{m,B2}| = |v_{m,B3}| = |v_{p1,F}| = |v_{p1,B1}| \\ = |v_{p1,B2}| = |v_{p2,F}| = |v_{p2,B1}| = |v_{p3,F}| = V_{Max} \end{aligned} \tag{5.3}$$

The output power of the four-way DPA, assuming a lossless power-combining network, can be expressed as a function of its voltage and current variables:

$$P_{out} = \frac{1}{2} Re\left(v_m i_m^* + v_{p1} i_{p1}^* + v_{p2} i_{p2}^* + v_{p3} i_{p3}^*\right) \tag{5.4}$$

For the requirement of peak efficiency at the back-off points, the output power of the 4-way DPA at the back-off point has a fixed ratio to its full power:

$$\begin{bmatrix} z_{11} & z_{12} & z_{13} & z_{14} \\ z_{21} & z_{22} & z_{23} & z_{24} \\ z_{31} & z_{32} & z_{33} & z_{34} \\ z_{41} & z_{42} & z_{43} & z_{44} \end{bmatrix} = \begin{bmatrix} i_{m,F} & i_{p1,F} & i_{p2,F} & i_{p3,F} \\ i_{m,B1} & i_{p1,B1} & i_{p2,B1} & i_{p3,B1} \\ i_{m,B2} & i_{p1,B2} & i_{p2,B2} & i_{p4,B2} \\ i_{m,B3} & i_{p1,B3} & i_{p2,B3} & i_{p4,B3} \end{bmatrix}^{-1} \begin{bmatrix} v_{m,F} & v_{p1,F} & v_{p2,F} & v_{p3,F} \\ v_{m,B1} & v_{p1,B1} & v_{p2,B1} & v_{p3,B1} \\ v_{m,B2} & v_{p1,B2} & v_{p2,B2} & v_{p3,B2} \\ v_{m,B3} & v_{p1,B3} & v_{p2,B3} & v_{p3,B3} \end{bmatrix} \tag{5.1}$$

$$k_{B1}^2 = \frac{P_{out,B1}}{P_{out,F}} = \frac{Re\left(v_{m,B1}i_{m,B1}^*\right) + Re\left(\sum_{i=1}^{2} v_{pi,B1}i_{pi,B1}^*\right)}{Re\left(v_{m,F}i_{m,F}^*\right) + Re\left(\sum_{i=1}^{3} v_{pi,F}i_{pi,F}^*\right)} = \frac{Re\left(v_{m,B1}i_{m,B1}^* + v_{p1,B1}i_{p1,B1}^* + v_{p2,B1}i_{p2,B1}^*\right)}{Re(v_{m,F}i_{m,F}^* + v_{p1,F}i_{p1,F}^* + v_{p2,F}i_{p2,F}^* + v_{p3,F}i_{p3,F}^*)} \tag{5.5}$$

$$k_{B2}^2 = \frac{P_{out,B2}}{P_{out,F}} = \frac{Re\left(v_{m,B2}i_{m,B2}^* + v_{p1,B2}i_{p1,B2}^*\right)}{P_{out,F}} \tag{5.6}$$

$$k_{B3}^2 = \frac{Re\left(v_{m,B3}i_{m,B3}^*\right)}{P_{out,F}} \tag{5.7}$$

Additionally, each DPA current is linearly related to its input code when the DPA is active. Consequently, the main DPA currents at back-off points Bi (i=1 to 3) are:

$$\begin{aligned} i_m &= \frac{I_{Max}}{D_{Max}}\left(D_{in}\right) \Longrightarrow \\ i_{m,B3} &= \frac{I_{Max}}{D_{Max}}\left(k_{B3}D_{Max}\right) = k_{B3}I_{Max}, \\ i_{m,B2} &= k_{B2}I_{Max}, \text{ and } i_{m,B1} = k_{B1}I_{Max} \end{aligned} \tag{5.8}$$

where D_{Max} is the maximum input code of each DPA. Moreover, the peak1 DPA currents at back-off points $B2$ and $B1$ are:

$$\begin{aligned} i_{P1} &= \frac{I_{Max}}{D_{Max}\left(1-k_{B3}\right)}\left(D_{in} - k_{B3}D_{Max}\right) \Longrightarrow \\ i_{p1,B2} &= \frac{I_{Max}}{1-k_{B3}}\left(k_{B2} - k_{B3}\right), \\ i_{p1,B1} &= \frac{I_{Max}}{1-k_{B3}}\left(k_{B1} - k_{B3}\right) \end{aligned} \tag{5.9}$$

Additionally, the peak2 DPA current at back-off point $B1$:

$$\begin{aligned} i_{P2} &= \frac{I_{Max}}{D_{Max}\left(1-k_{B2}\right)}\left(D_{in} - k_{B2}D_{Max}\right) \Longrightarrow \\ i_{p2,B2} &= \frac{I_{Max}}{1-k_{B2}}\left(k_{B1} - k_{B2}\right) \end{aligned} \tag{5.10}$$

Moreover, the current profile of peak3 DPA is represented as:

$$i_{P3} = \frac{I_{Max}}{D_{Max}\left(1 - k_{B1}\right)}\left(D_{in} - k_{B1}D_{Max}\right) \tag{5.11}$$

To complete our set of equations, the reciprocal property of the intermediate network forces to have these relationships: $Z_{12} = Z_{21}$, $Z_{13} = Z_{31}$, $Z_{14} = Z_{41}$, $Z_{23} = Z_{32}$, $Z_{24} = Z_{42}$, and $Z_{34} = Z_{43}$. Afterward, the remaining unknown variables can be uniquely solved using the above independent equations for specific back-off levels k_{B1}, k_{B2}, k_{B3}, and phase relations between main and peak DPAs. The z-parameters of the intermediate network will then be defined. Next, its s-parameters of the intermediate network can be obtained from the already known 4-port z-parameter matrix. Therefore, the 5-port s-parameters of the power combining network can be derived from its 4-port s-parameters. Note that only the fifth port (which is connected to the load) needs to be reintroduced, and the remaining s-parameters are identical to those of the intermediate network. Since the power combining network is considered to be lossless, the s-parameters of (N+1)-port have the following properties:

$$\sum_{n=1}^{N+1} |s_{np}|^2 = 1 \ \forall p \ and \ \sum_{n=1}^{N+1} s_{np}s_{nq}^* = 0 \ \forall p \neq q \tag{5.12}$$

where N represents the power combining network number of ports excluding the load port. Using (5.12), the unknown variables are s_{5i} (i=1 to 5). The magnitude of s_{51} can be obtained:

$$|s_{51}| = \sqrt{1 - |s_{11}|^2 - |s_{21}|^2 - |s_{31}|^2 - |s_{41}|^2} \tag{5.13}$$

Thus, we can define $\angle s_{51} = \alpha$, and then s_{5i} for i=2 to 5 are defined as functions of α:

$$\begin{aligned}
&s_{11}s_{12}^* + s_{21}s_{22}^* + s_{31}s_{32}^* + s_{41}s_{42}^* + s_{51}s_{52}^* = 0 \Longrightarrow \\
&s_{52} = \frac{-1}{s_{51}^*}\left(s_{11}^*s_{12} + s_{21}^*s_{22} + s_{31}^*s_{32} + s_{41}^*s_{42}\right), \\
&s_{53} = \frac{-1}{s_{51}^*}\left(s_{11}^*s_{13} + s_{21}^*s_{23} + s_{31}^*s_{33} + s_{41}^*s_{43}\right), \\
&s_{54} = \frac{-1}{s_{51}^*}\left(s_{11}^*s_{14} + s_{21}^*s_{24} + s_{31}^*s_{34} + s_{41}^*s_{44}\right), \\
&s_{55} = \frac{-1}{s_{51}^*}\left(s_{11}^*s_{15} + s_{21}^*s_{25} + s_{31}^*s_{35} + s_{41}^*s_{45}\right)
\end{aligned} \tag{5.14}$$

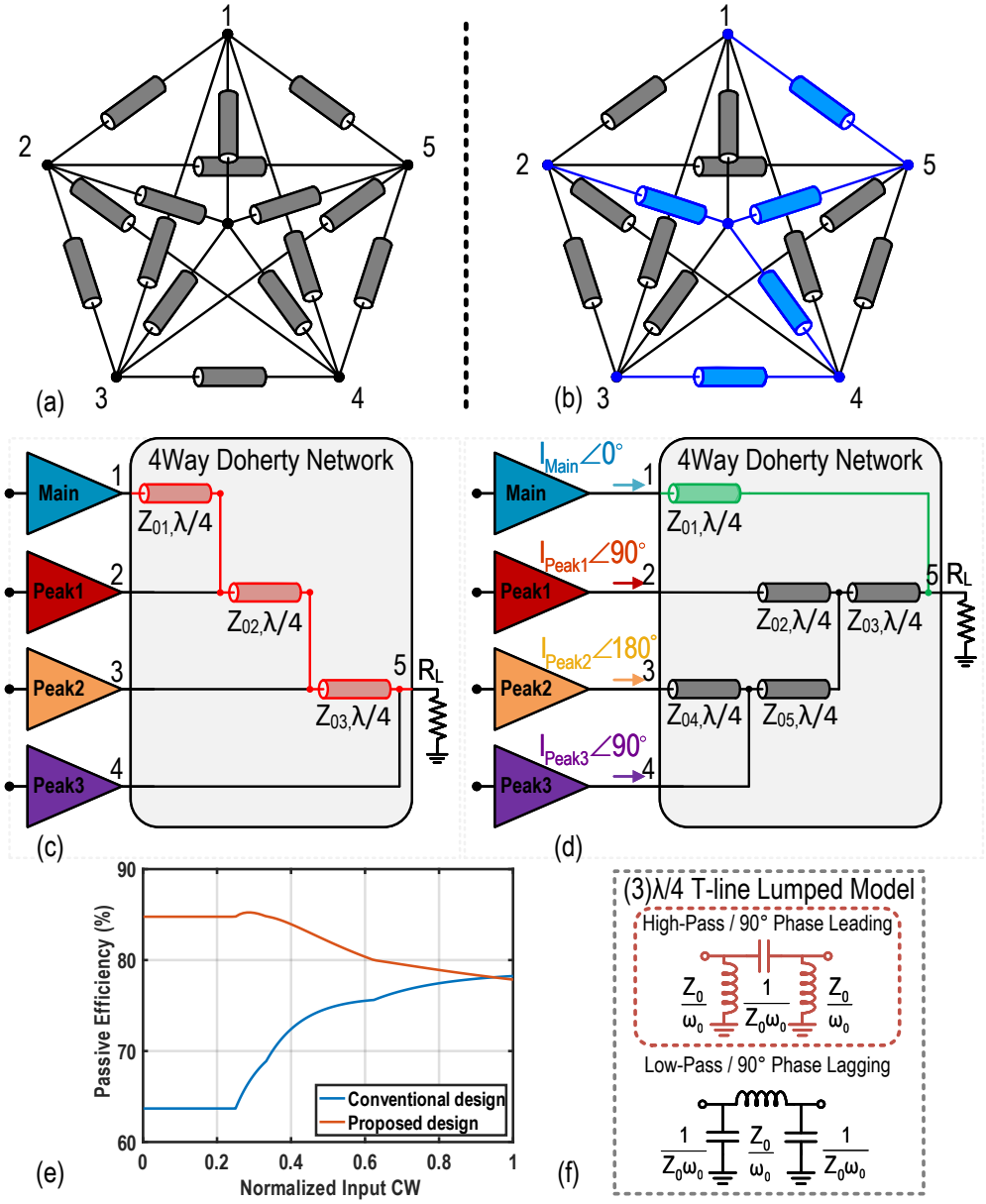


Figure 5.11: (a) General topology of the Doherty power combiner. (b) Selected topology. (c) Conventional 4-way Doherty parallel power combiner. (d) Proposed (on-chip) Doherty parallel combiner. (e) Simulated passive efficiency. (f) Lumped component model of the (3)$\lambda/4$ T-line.

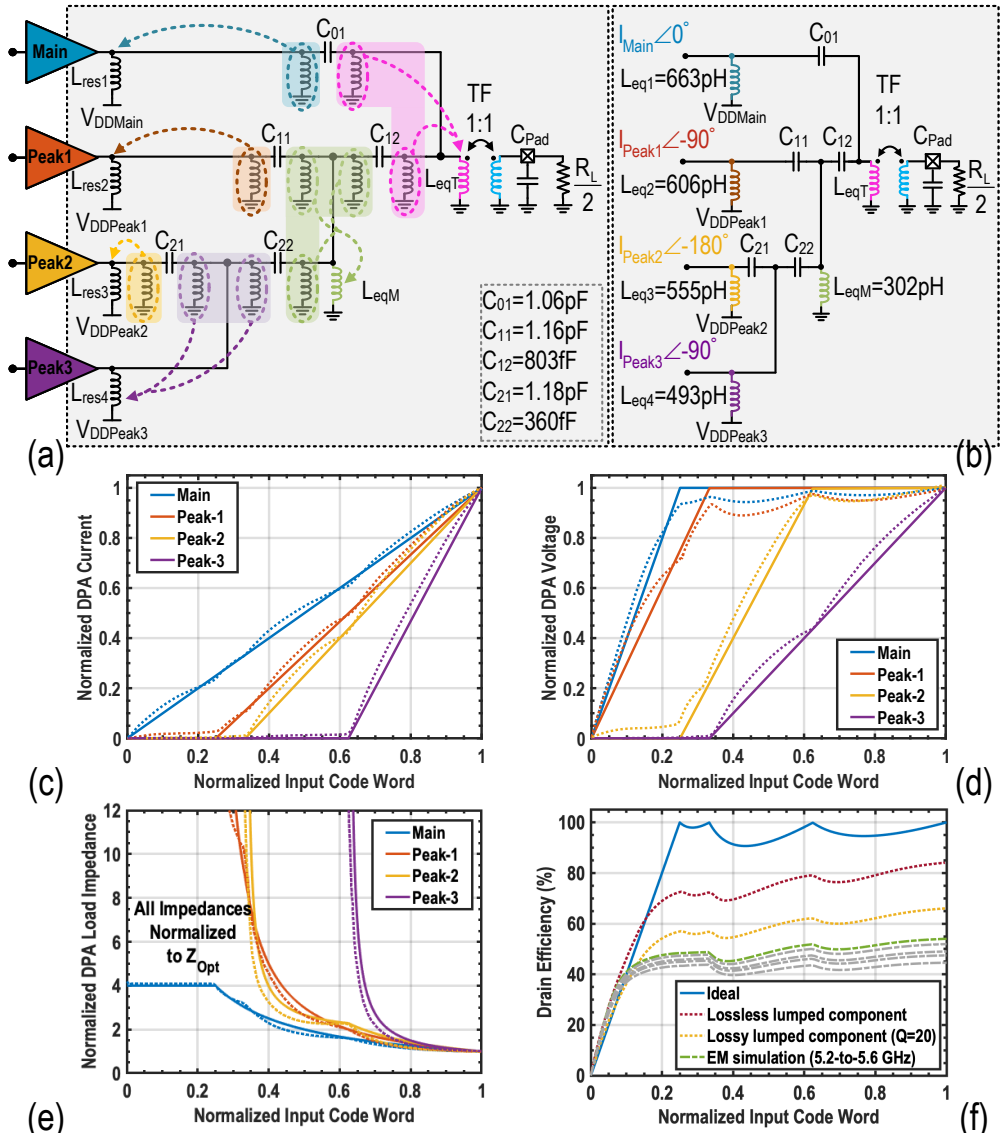


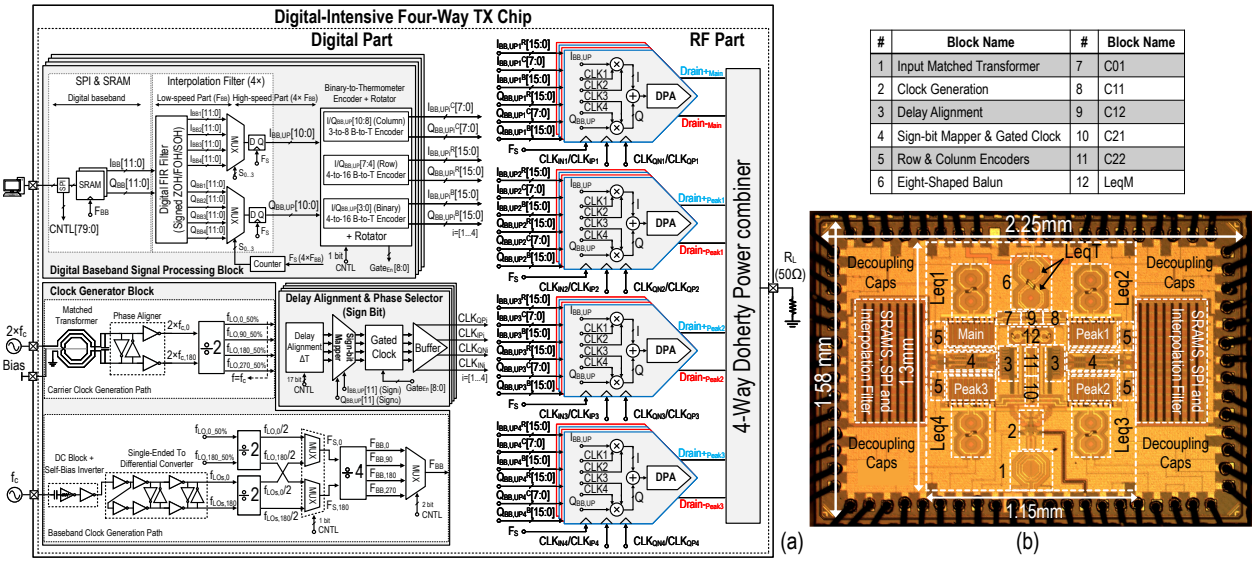
Figure 5.12: (a), (b) Implementation of the 4-way Doherty output impedance matching network with consolidated on-chip lumped elements for transmission lines. (c)-(f) Theoretical (colored solid lines) and simulation with real active power devices (colored dotted lines) results of the proposed 4-way Doherty output matching network at 5.4GHz (EM simulation results of DE in other frequencies are plotted in gray dotted lines in (f)).

Consequently, the s-parameters of the power combiner are known and only depend on the variable α. The phase of α may yield the optimum power combiner topology. Subsequently, the passive network topology of the power combiner can be extracted from the z-/y-parameters of the 5-port network (Z_C/Y_C). The general 4-way power combiner topology is shown in Fig. 5.11(a). It is worth mentioning that different passive topologies can be achieved by solving the equations for various phase relations that differ in terms of simplicity, operational bandwidth, and passive efficiency. In some cases, the values of Z_C/Y_C may become complex and not pure imaginary numbers, which indicate the network is not realizable by the $\lambda/4$ or $3\lambda/4$ transmission lines shown in Fig. 5.11(a). Since the 4-way Doherty network is considered as a black box, thus, any network whose z-/y-parameter is equal to the calculated z-/y-parameter, can be considered a feasible solution for the desired Doherty network. Fig. 5.11(c), and (d) depict two possible arrangements for the 4-way Doherty combiner based on $\lambda/4$-line impedance inverter. In this work, the structure in Fig. 5.11(d) is chosen [120] since, in contrast to the conventional Doherty parallel combiner, the selected configuration has the advantage of a relatively short RF path from the main DPA branch to the load. This arrangement directly improves the DPBO average efficiency (Fig. 5.11(e)). The z-parameter of this network is as follows:

$$Z_T = \begin{bmatrix} 0 & j\dfrac{Z_{01}Z_{02}}{Z_{03}} & 0 & 0 & -jZ_{01} \\ j\dfrac{Z_{01}Z_{02}}{Z_{03}} & 0 & j\dfrac{Z_{02}}{Z_{05}} & 0 & 0 \\ 0 & j\dfrac{Z_{02}Z_{04}}{Z_{05}} & 0 & -jZ_{04} & 0 \\ 0 & 0 & -jZ_{04} & 0 & 0 \\ -jZ_{01} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{5.15}$$

Where Z_{0i} (i=1 to 4) are the characteristic impedance of the $\lambda/4$-line impedance inverters. Assuming $\alpha = 90^\circ$, Z_C is calculated as:

$$Z_C = \begin{bmatrix} 0 & j17.319 & 0 & 0 & -j25 \\ j17.319 & 0 & j6.946 & 0 & 0 \\ 0 & j6.946 & 0 & -j22.37 & 0 \\ 0 & 0 & -j22.37 & 0 & 0 \\ -j25 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{5.16}$$



#	Block Name	#	Block Name
1	Input Matched Transformer	7	C01
2	Clock Generation	8	C11
3	Delay Alignment	9	C12
4	Sign-bit Mapper & Gated Clock	10	C21
5	Row & Colunm Encoders	11	C22
6	Eight-Shaped Balun	12	LeqM

Figure 5.13: (a) The detailed block diagram of the proposed 4-way Doherty I/Q digital transmitter. (b) Chip microphotograph.

Solving (5.15)-(5.16), the characteristic impedance value of the associated transmission lines can be obtained. Note that Z_{02}, Z_{03}, and Z_{04}, Z_{05}, have dependent relation. In our design, $Z_{01} = 25$, $Z_{02} = 22.86$, $Z_{03} = 33$, $Z_{04} = 22.37$, $Z_{05} = 73.63$. It should be emphasized that our proposed Doherty architecture contrasts with the approach in [87] since, in our work, the phase delay is digitally implemented using the quadrature clocks. Implementing such a transmission line of the Doherty DPA occupies silicon area and exhibits excessive losses, resulting in a significant deviation of its passive efficiency from the theoretical performance. To make the power combiner more compact, the transmission lines can be replaced either with a lumped low-pass or high-pass π-networks, as shown in Fig. 5.11(f). Nevertheless, in this work, the $\lambda/4$ transmission lines are approximated by lumped high-pass equivalent LC π-networks with a $-90°$ phase delay. These high-pass π-networks are equivalent to $3\lambda/4$ transmission lines that require different LO phase relations in the four identical DPA branches connected to the power combiner. Using the proper LO clocks' phases, the I/Q DPA banks' currents drive the 4-way DPA combiner, yielding the desired active-load modulation and in-phase power summation.

Fig. 5.12(a) also shows that the DPAs require RF chokes for the DC feed and 2nd-harmonic

termination. Employing the high-pass LC networks facilitates consolidating shunt inductors directly at the output of the DPAs into four inductors L_{eq1}-L_{eq4} that resonate out the associated DPA output capacitance and also provide DC biasing and only one extra inductor L_{eqM}. Moreover, high-pass LC networks allow incorporating the output balun into the DPA power combining network, yielding an even more compact power combiner. Furthermore, the capacitor in the high-pass network acts as an AC-coupled capacitor providing DC voltage isolation to the other DPAs enabling the incorporation of different supply voltages for the individual DPAs (indicated as V_{DDMain}, $V_{DDPeak1}$, $V_{DDPeak2}$, $V_{DDPeak3}$ in Fig. 5.12(b)). This technique can potentially improve the efficiency even at deeper power back-off regions. Fig. 5.12(d)-(f) demonstrates the theoretical and simulated results of the proposed 4-way Doherty output matching network. As shown in Fig. 5.12(f), with loss-less passive components and real active power devices, the DTX achieves an average drain efficiency of 76% throughout the 12dB PBO, while this value is 59.73% considering lossy inductors with a quality factor of Q=20. The DTX delivers an average drain efficiency of 49.73%, incorporating electromagnetic (EM) simulation of the complete structure. The physical layout floorplan of the proposed 4-way Doherty power combiner will be revealed and further discussed in section 5.4.

5.4 Implementation Details

An overview of the overall architecture is illustrated in Fig. 5.13(a). It comprises digital and RF parts. The digital part includes the digital baseband signal processing block, the LO and sampling clock generator block, the phase (sign-bit) selector block, and the digital I/Q interleave banks. Additionally, the RF part consists of digital power cells and the 4-way power combiner. In the remainder of this section, its building blocks will be sequentially disclosed, and their circuit design techniques will be described.

5.4.1 The Clock Generation And Distribution

An off-chip single-ended clock operating at $2\times f_C$ is applied to a matched on-chip transformer, which converts the unbalanced clock to its balanced counterpart. Fig. 5.14(a) exhibits the layout of the matched input transformer. A recursive design is performed to achieve matched

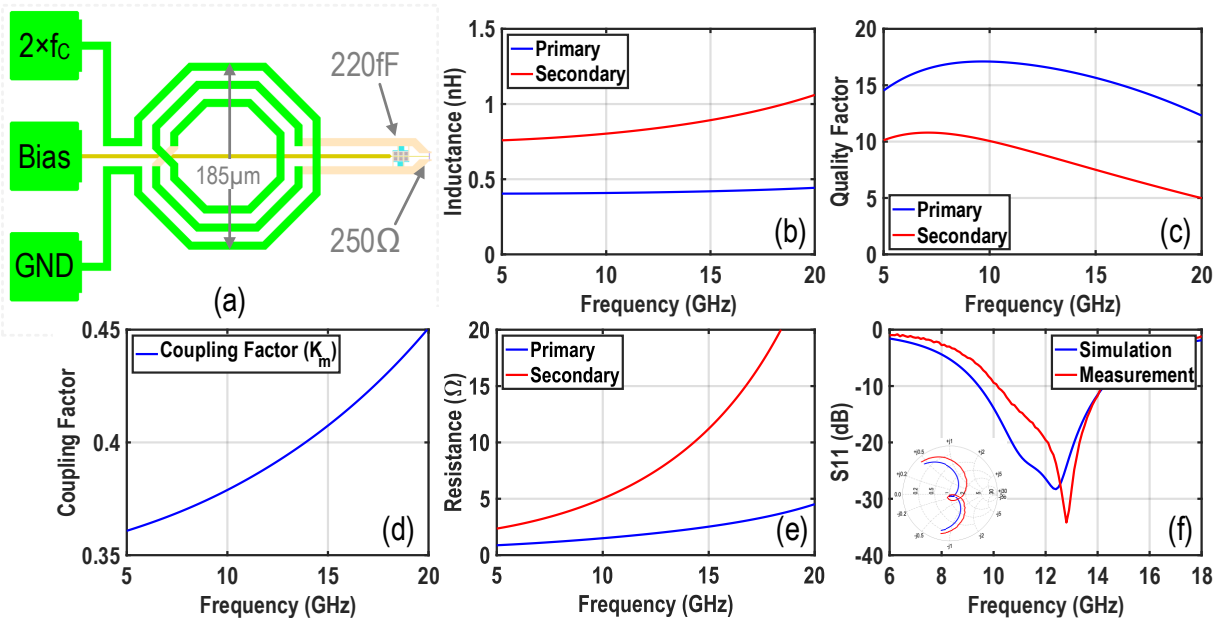


Figure 5.14: (a) Layout of the input unbalanced-to-balanced transformer. (b)-(e) EM simulation results of the input balun. (f) Simulated versus measured S_{11}.

wideband transformer with negligible amplitude and phase mismatch. The transformer's outer diameter is 185μm×185μm. The EM simulation results using Momentum^{TM} are plotted versus frequency in Fig. 5.14(b)-(e), including the magnetic coupling factor K_m, primary and secondary inductances L_P, and L_S, winding resistances R_P and R_S, quality factors Q_P and Q_S. At 12GHz, these parameters are K_m=0.389, L_P=412pH, L_S=832pH, R_P=1.9Ω, R_S=6.9Ω, Q_P=16.8, Q_S=9.1, respectively. The next stage has a large impedance. Thus, a parallel resistor of 250Ω and a capacitor of 220fF are added differentially to transform these differential loads into an optimum single-ended primary load, facilitating the matching condition. The EM simulation and measured s-parameter of Fig. 5.14(f) represent a good matching condition at the transformer input. Utilizing this matched transformer at the transmitter's input, the required power for the off-chip single-ended LO at 10.8GHz is 0dBm. Although the transformer's differential layout traces are completely symmetrical, a phase aligner comprising a back-to-back inverter pair is employed at the transformer output to prevent any misalignment. The phased aligned differential 2×f_C clocks, i.e., 2×$f_{C,0}$ and

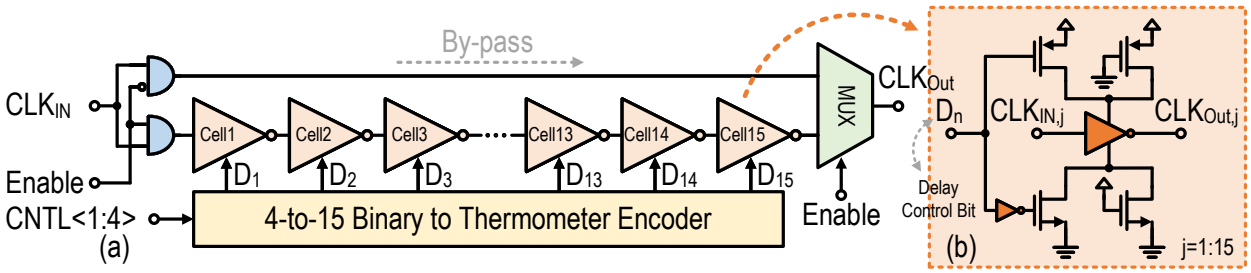


Figure 5.15: (a) Schematic of the 4-bit fine-resolution delay line, and (b) its delay-cells.

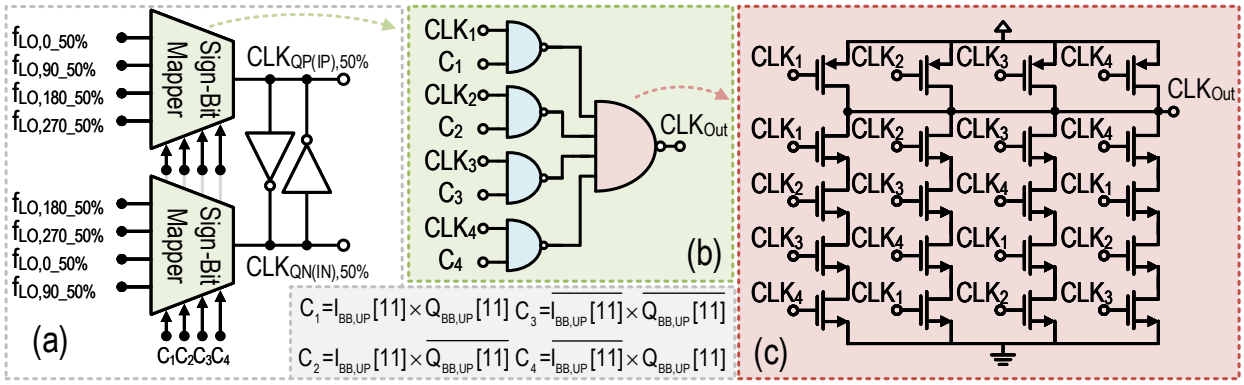


Figure 5.16: (a) Schematic diagram of the global 50%-LO quadrature clock mapper. (b) NAND gate-based multiplexer implementation circuitry. (c) 4-input symmetrical NAND logic gate.

$2\times f_{C,180}$, are applied to a divide-by-2 circuit to generate the desired 50%-LO clocks at f_C with a relative phase difference in multiples of 90 degrees. These complementary quadrature LO clocks are $f_{LO,0\_50\%}$, $f_{LO,90\_50\%}$, $f_{LO,0\_180\%}$, $f_{LO,270\_50\%}$ in Fig. 5.13(a). The divide-by-2 circuit is implemented as a flip-flop-based frequency divider that consists of four C^2MOS latches arranged in a loop [70]. All other divide-by-2 circuits also utilize the same structure. The transistor sizing, however, is adjusted based on its operational frequency.

On the other hand, the master/baseband sampling clocks (F_S/F_{BB}) are generated by employing two different approaches. In the first method, these clocks can be created from the existing carrier clock by applying one of its complementary clock pairs (e.g., $f_{LO,0\_50\%}/f_{LO,180\_50\%}$ or $f_{LO,90\_50\%}/f_{LO,270\_50\%}$) to another divide-by-2 circuit. By utilizing this arrangement, the

F_S clock operates at $f_C/2$, resulting in direct dependency of the baseband modulation bandwidth to its carrier operating frequency. In the second method, independent master/baseband clocks can be generated using another off-chip single-ended clock running at $2\times F_S$. Using an active unbalanced-to-balanced converter and a subsequent divide-by-2 circuit, the F_S clock is generated. This master clock is then applied to a divide-by-4 circuit to generate the F_{BB} clock. The following block is a multiplexer to select the appropriate baseband clock. It is worth mentioning that to mitigate the crosstalk mostly caused by capacitive coupling, ground lines were placed in-between the quadrature LO lines. Additionally, to suppress the LO leakage, shielding is utilized to diminish the coupling from other routing lines, e.g., data routing, when multiple crossover lines occur.

5.4.2 The Delay Alignment And The Phase (Sign-bit) Selector

5.4.2.1 The delay alignment

The required Doherty phase relations of the DPA branches are digitally implemented by appropriately swapping carrier quadrature clocks. To compensate for different design variations, such as the process/voltage/temperature (PVT), frequency, and load variations on Doherty phase relations, fine-tune phase aligners are adopted [29] and implemented as shown in Fig. 5.15. Their controlling signals are static and come from a serial-to-parallel interface (SPI). A binary-to-thermometer encoder converts the 4-bit input binary code (CNTL<1:4>) to a 15-bit thermometer code where each bit is used as a delay control bit for a delay cell. The delay line can be bypassed or employed by the Enable bit. The absolute delay of each delay cell is controlled with a single bit by enabling or disabling NMOS and PMOS transistors in series with the supply/ground paths. The RF clock passes through 15 cascaded delay cells to arrive at the output, resulting in a total relative delay of 85ps with a resolution of roughly 5.5ps, which is more than enough to compensate for the variation mentioned above.

5.4.2.2 The phase selector

The following stage is the carrier clock phase selector. As demonstrated in Fig. 5.16, it is implemented as four NAND-gate-based multiplexers with its input selection control signals of $Sign_I=I_{BB,up}[11]$ and $Sign_Q=Q_{BB,up}[11]$ (see Fig. 5.13(a)). As depicted in Fig. 5.13(b), four

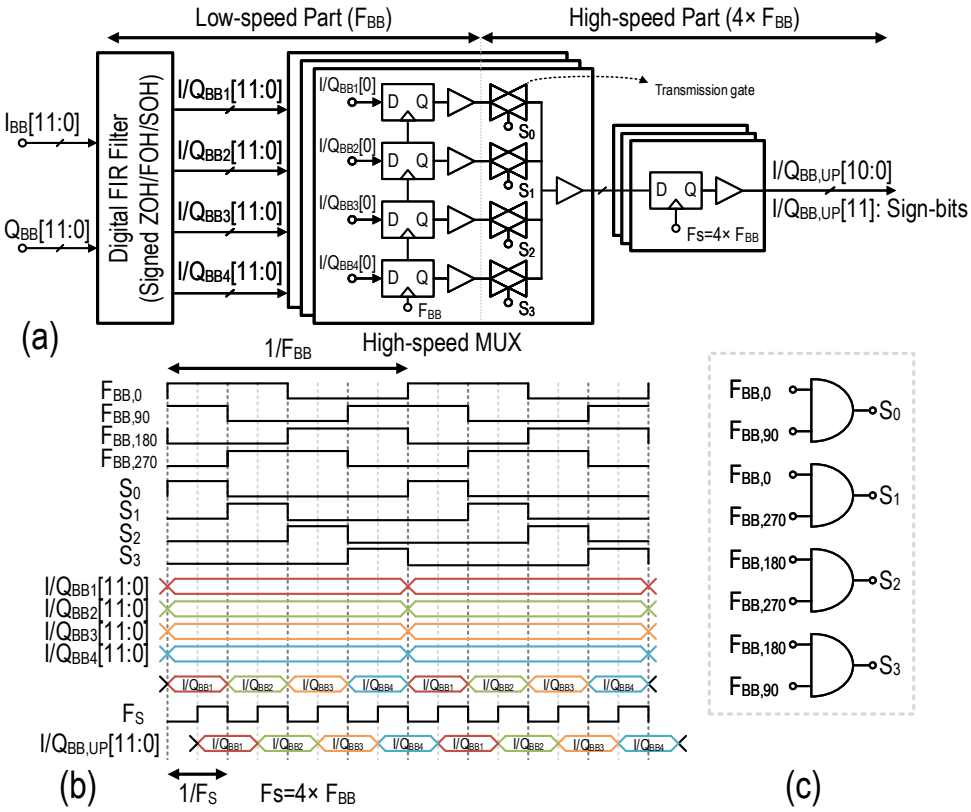


Figure 5.17: Interpolation filter and its high-speed MUX: (a) Detailed implementation. (b) Corresponding waveforms. (c) Generating MUX selection signals from different phases of the F_{BB} clock [59].

controlling signals of C_1, C_2, C_3, and C_4 are first generated by ANDing the corresponding I/Q sign-bits and subsequently applied to the phase mapper. Based on the four different states of the I/Q sign-bits, the 50% phase-modulated quadrature clocks fed to the DPA can adequately be swapped, and thus, the entire four-quadrant I/Q plane can be covered. To equalize the delays of the clocks, the NAND gates are implemented in a fully symmetric configuration (Fig. 5.16(c)). Moreover, due to employing 50%-LO clocks, a back-to-back inverter pair is employed to align further the phases of the complementary clock pairs.

5.4.3 The 11-bit I/Q DPA Floor Plan

The transmitter comprises four identical 12-bit resolution I/Q banks (including the sign-bit) that act as four I/Q RF-DACs. Fig. 5.18(a) depicts the implementation details and the floor-plan of one of the I/Q banks. For each bank, the digital I/Q baseband data (I_{BB}/Q_{BB}[11:0]) are stored on a 4K SRAM and clocked at F_{BB}, which are programmed through the low-speed SPI interface. The 12-bit digital I/Q baseband signals passed through a "signed" zero/first/second-order hold (ZOH/FOH/SOH) FIR filter to up-sample by a factor of 4 (F_S=4×F_{BB}) and low-pass filter the up-sampled I/Q baseband data, suppressing the sampling spectral replicas (SSR) [59]. Fig. 5.17, unveils the detailed multiplexer implementation and the corresponding waveforms. The DFF at the input of the MUX is clocked at F_{BB} and re-times the output data of the digital FIR filter (I/Q_{BB1}[i], I/Q_{BB2}[i], I/Q_{BB3}[i], I/Q_{BB4}[i], where i=0 to 11). As illustrated in Fig. 5.17(b), the pulse width of the selection signals driving the transmission gates (S_0 to S_3) are $1/F_S$, which are realized by bitwise ANDing of the proper F_{BB} clocks pairs (Fig. 5.17(c)). Accordingly, the multiplexer performs the 4×up-sampling and summing operation by generating three zeros and merely one sample of the input signal during one period of the baseband signal. The DFF at the output is clocked at F_S and re-times the up-sampled and interpolated I/Q data, resulting in ZOH function at F_S, and FOH/SOH suppression at multiples of F_{BB}. This FIR filter architecture contrasts with the approach in [59] since, in our work, it is implemented for signed baseband data. $I_{BB,UP}$[10:0], and $Q_{BB,UP}$[10:0] represent the interpolated un-signed binary digital codes that must be converted to corresponding thermometer codes to avoid nonmonotonic behavior and mid-code transition glitches. However, the pure thermometer-coded approach increases the complexity of the encoders, the chip area, interconnect parasitics, and power consumption. Thus, in this design, a segmented approach with 4-bit ($I/Q_{BB,UP}$[3:0]) binary-weighted LSB and 7-bit ($I/Q_{BB,UP}$[10:4]) thermometer-coded MSB cells is adopted. Therefore, the I/Q bank implementation requires 128 MSB, with an aspect ratio of W/L=19.2μm/40nm, which are realized as eight parallel cascoded transistors with an aspect ratio of W/L=2.4μm/40nm, and 16 LSB units with an aspect ratio of W/L=1.2μm/40nm. Moreover, the 7-bit MSB ($I/Q_{BB,UP}$[10:4]) are split into 3-bit ($I/Q_{BB,UP}$[10:8]) for a column encoder and 4-bit ($I/Q_{BB,UP}$[7:4]) for a row encoder. Hence, the 128 MSB units of each part are arranged such that they comprise 16 rows ($I/Q_{BB,UPR}$[15:0]) and 8 columns ($I/Q_{BB,UPC}$[7:0]). Furthermore, the LSB units comprise 16

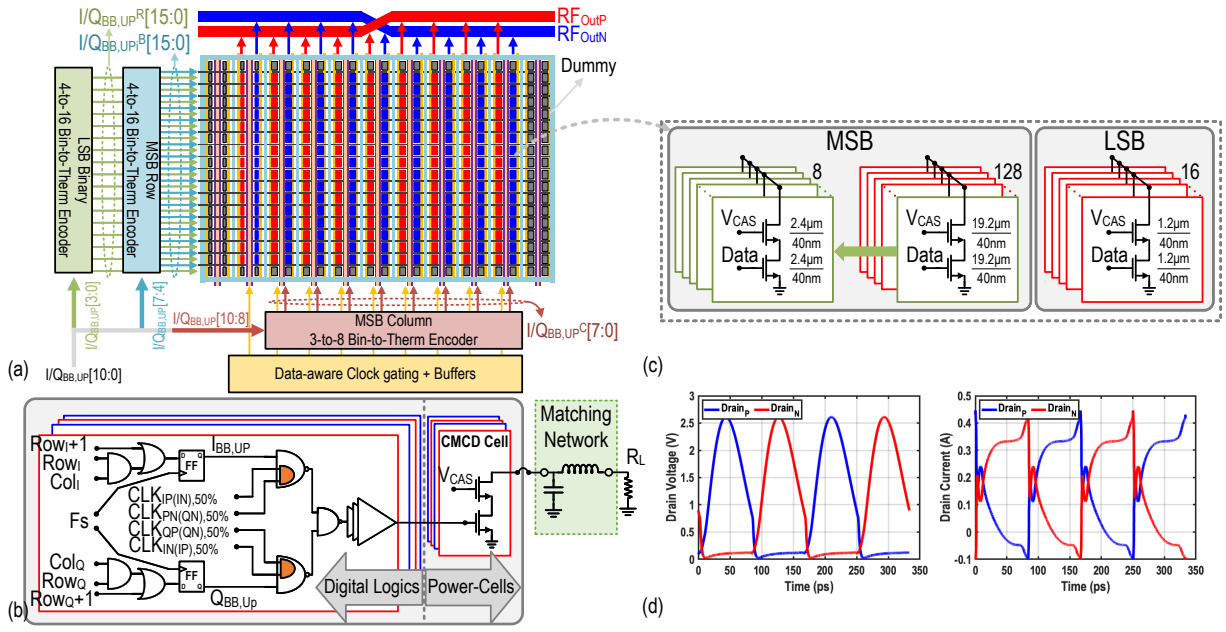


Figure 5.18: (a) 11-bit I/Q DPA floor plan. (b) I/Q RF-DAC sub-cells. (c) MSB and LSB power cells aspect ratios. (d) Simulated transient voltage and current waveforms.

small unit cells ($I/Q_{BB,UPB}[15:0]$) that occupy a column. In the I/Q RF-DACs floorplan, the "snake" traverse movements are performed among sub-cells to preserve continuity and improve the differential nonlinearities (DNL). Fig. 5.18(d) presents the simulated transient voltage and current waveforms of the final stage. As can be seen, the waveforms are no longer ideal square waves or half-sinusoids due to device parasitic capacitance. However, the overlap between high voltage and high current is a small fraction of the whole period.

Instead of having two separate push-pull banks, an interdigitated push-pull layout is implemented. In other words, every other column of the I/Q RF-DAC matrix is dedicated to the in-phase arrays and their 180 degrees out-of-phase counterparts. This technique reduces the overall I/Q RF-DAC core size for the same achievable output power resulting in a highly compact area, minimal mismatch, less parasitics and power consumption leading to an improved overall DTX efficiency. To equalize the primary output traces, swapped/cross-coupled routings for the in-phase and out-of-phase drain lines are utilized. A data-aware clock gating technique [12, 121] is also employed to reduce LO distribution power in the

back-off and enhance the system efficiency at these levels.

The I/Q RF-DAC sub-cells comprise two parts: a pure digital logic section and a power-cell part (Fig. 5.18(b)). The logic part consists of a decoding logic and a time synchronizer flip-flop followed by an I/Q implicit mixing circuit. The AND-OR decoder determines whether the designated cell should be activated. The master/slave DFF is employed to synchronize all I/Q RF-DAC unit cells to the master clock (F_S), diminishing undesirable spectral impurity related to an early-late arrival of each unit cell's input data. Before the mixing operation, the designated 25%-LO generation is performed using a 3-input NAND gate. Next, the synchronized digital data is up-converted by 25%-LO clocks using the bit-wise AND operation. Subsequently, the up-converted I/Q bitstreams are combined by the subsequent NAND gate to fulfill I/Q interleaving and fed to the power cell inverter buffers. As stated previously, the orthogonal summing of the I and Q paths is achieved by employing the complementary quadrature 25% LO clocks at this stage. As a result, the local 25% duty-cycle generation and up-conversion circuit are among the most crucial building blocks of the DPA chain. All critical digital logics are implemented based on symmetrical gates to equalize the delay from the input to the output and the fanout for proceeding circuitry. The power cells are current-mode class-D (CMCD) PAs [122, 123] driven by three-stage digital buffers. Meanwhile, since in the CMCD, the drain voltage can exceed 2-to-3 times the supply voltage thus, a cascode topology is adopted in this design to prevent reliability violations.

5.4.4 Doherty Power Combiner Floor Plan

Fig. 5.19(a) illustrates the Doherty power combiner floor plan. Its layout can be so compact that the 4-way combiner's inductors suffer from undesired magnetic couplings between the different Doherty branches. Consequently, 8-shaped inductors that offer self-cancellation of their electromagnetic field are implemented. As illustrated in Fig. 5.19(b), the inductors provide an opposite orientation of the magnetic flux for their coil loops to avoid unwanted magnetic coupling between the closely-spaced DPAs. As depicted in Fig. 5.19, to bridge a physical distance between the DPA banks, the series AC-coupling capacitors (C_{01}, C_{12}, ..., C_{22}) are implemented as distributed capacitors as depicted in Fig. 5.19. As illustrated, these distributed capacitors can be modeled by a series LC-network that provides the same susceptance at the fundamental frequency as the original floating capacitors in the high-pass

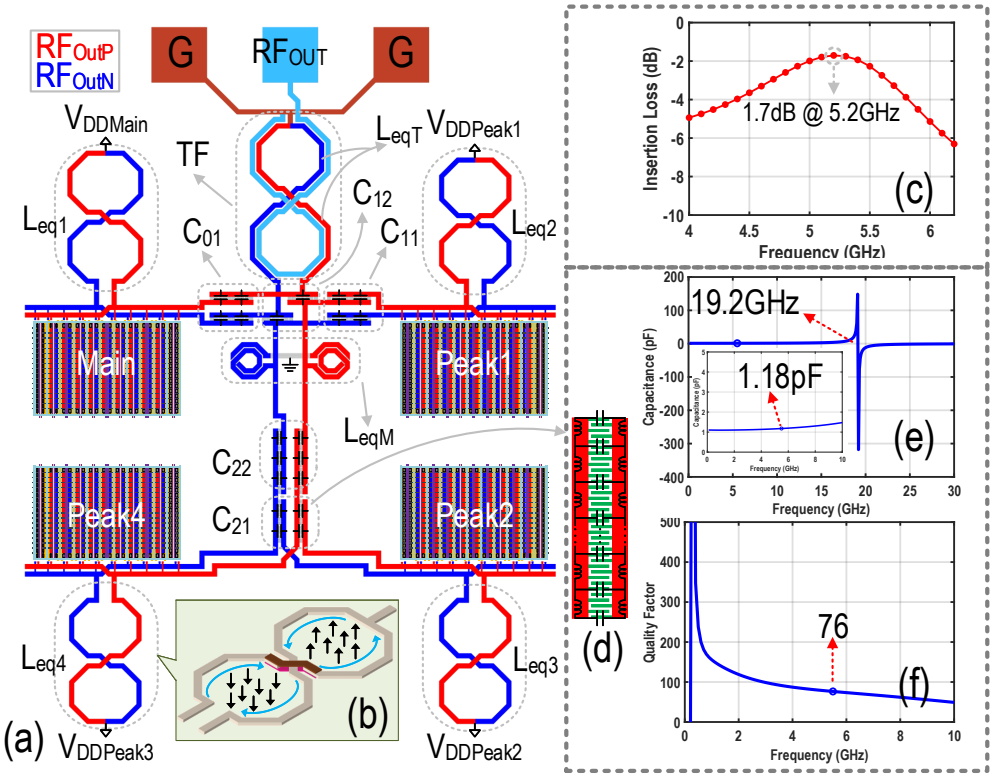


Figure 5.19: (a) Physical layout implementation of the four-way Doherty DTX configuration. (b) 8-shaped inductor's electromagnetic fields. (c) Simulated insertion loss of the Doherty network. (d) Implemented distributed series AC-coupling capacitors. (e) EM simulation of the C_{21} capacitance. (f) Quality factor of the C_{21}.

sections. The EM simulation results of the C_{21} are presented in Fig. 5.19(e), and (f). As depicted, the capacitance value is exactly 1.18pF, as the originally designed C_{21} value in the high-pass section, while the self-resonance frequency of the LC-network occurs at 19.2GHz, far enough from the designated operational bandwidth of the DTX. The quality factor of this capacitor is Q=76 representing its broadband operation. The EM simulated insertion loss is approximately 1.7dB at 5.2GHz.

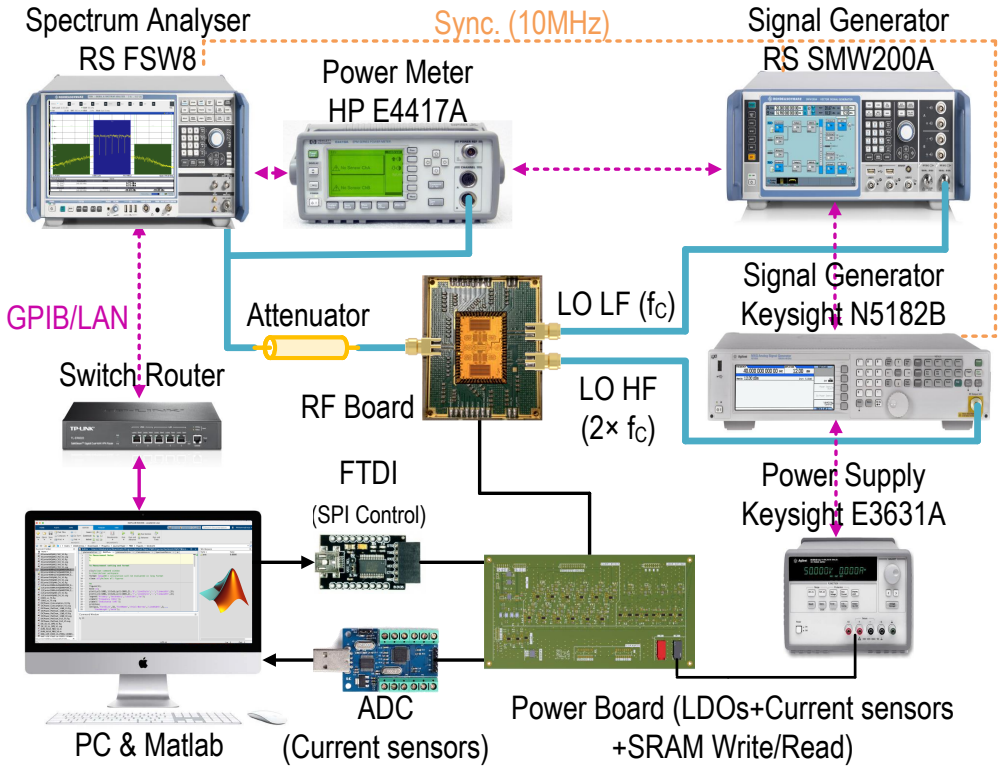


Figure 5.20: Measurement setup.

5.5 Experimental Results

The proposed DTX is designed and fabricated in the 40nm bulk CMOS. Fig. 5.13(b) exhibits the chip micrograph while the block names are specified in a table. The chip occupies an area of 2.25mm×1.58mm with a core area of 1.3mm×1.15mm as shown in Fig. 5.13(b). Moreover, the SPI, the designated SRAMs, and the low-speed part of the interpolation filter are digitally synthesized and occupy an area of 2×0.67mm×0.38mm while decoupling capacitors and I/O pads occupy the remainder. The measurement setup is shown in Fig. 5.20. The I/Q data are generated in MATLAB and then applied to the DTX using four on-chip 4K SRAMs (one SRAM for each I/Q DPA) running at F_S=675MHz. The power consumption of all blocks (except the SRAMs) is included in the reported system efficiency.

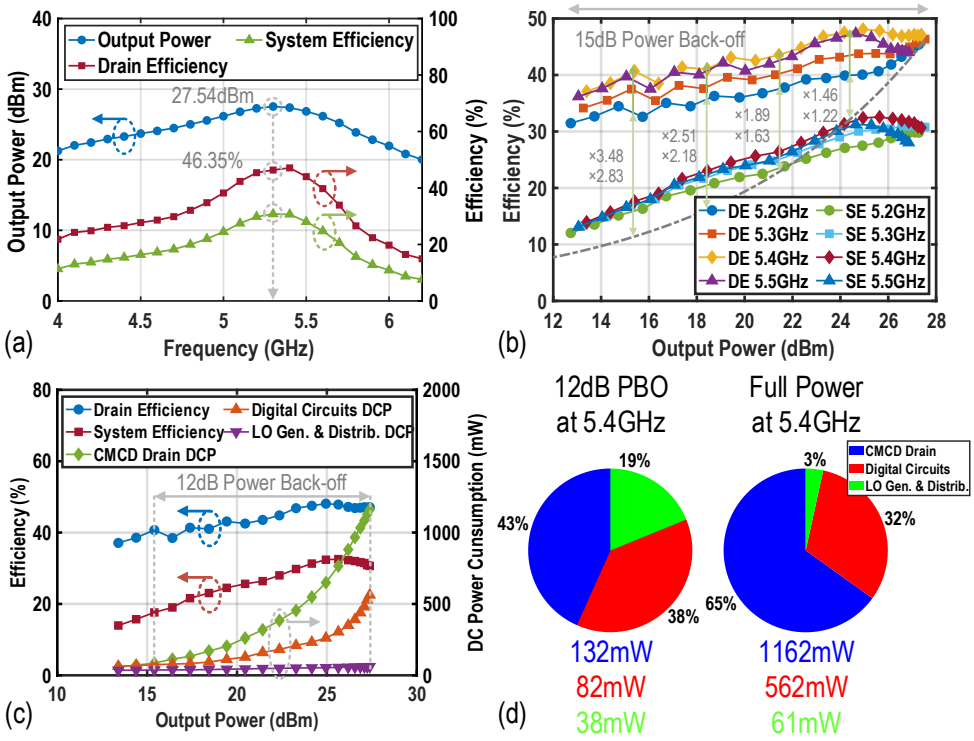


Figure 5.21: Measured (a) peak output power, drain, and system efficiencies versus operational frequency, (b) drain and system efficiencies versus output power at different frequencies, (c) Drain/system efficiencies, and the related DC power consumption versus power back-off at 5.4GHz, (d) power consumption breakdown at the full power and 12dB back-off at 5.4GHz frequency.

5.5.1 Static Measurements

The DTX is first characterized by static measurements. The output power is measured using a power meter. Fig. 5.21(a) presents the measured output power, drain efficiency (DE)[1], and system efficiency (SE)[2] over a 4-to-6.2GHz band under the static input condition of I_{BB}=Q_{BB}=2047 for all DPAs. The proposed bits-in RF-out transmitter generates 27.54dBm peak output power and 46.35% drain efficiency at 5.3GHz with a supply voltage of 1V ded-

[1] $DE(\%) = 100 \times \dfrac{P_{RF_{Out}}}{P_{DC-PowerCells}}$

[2] $SE(\%) = 100 \times \dfrac{P_{RF_{Out}}}{P_{DC-PowerCells} + P_{DC-All\ Blocks(Except\ SRAMS)}}$

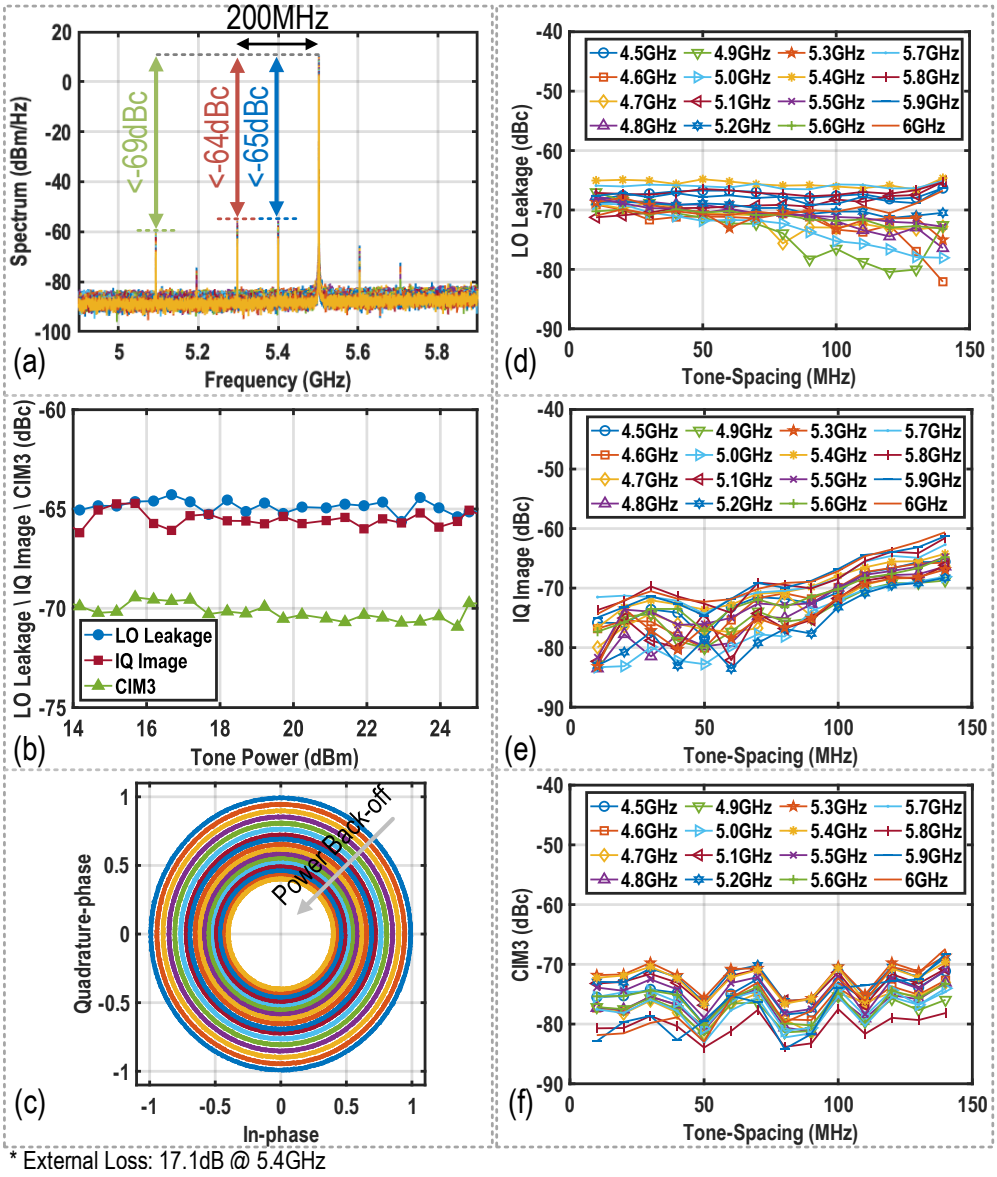


Figure 5.22: Measured (a) output spectrum of a single-tone test with 200MHz tone-spacing at 5.4GHz versus power back-off, (b) its corresponding LO leakage, I/Q image, and C-IMD3/H_{3BB}, and (c) I/Q trajectory. (d)-(f) Measured single-sideband performance over frequency band vs. tone-spacing.

icated to each DPA. It achieves a 3dB bandwidth of 1.3GHz in a 4.6-to-5.9GHz band, while the 1dB bandwidth is roughly 5-to-5.6GHz, maintaining decent performance. To measure the DTX PBO performance, the corresponding I_{BB}/Q_{BB} data are swept based on the current profile of the main and peak DPAs, as discussed in section 5.3. The measured drain and system efficiencies versus output power at different frequencies are presented in Fig. 5.21(b), yielding a drain efficiency of 37.35/35.47/33.49%, 40.33/38.11/36.95%, 43.49/41.06/40.6%, and 41.74/40.16/39.27% for 6/9/12dB PBOs at 5.2/5.3/5.4/5.5GHz, respectively. These results indicate that the realized compact 4-way Doherty digital transmitter maintains its decent drain and system efficiencies enhancement over DPBO. Fig. 5.21(c) demonstrates the drain/system efficiencies, and the related DC power consumption versus power back-off at 5.4GHz. Fig. 5.21(d) represents the power consumption breakdown at the full power and 12dB back-off at 5.4GHz frequency. As expected, the system efficiency degrades more in lower codewords as it includes the power consumption of circuit blocks that do not scale with the output power. However, utilizing more effective clock gating mitigates this issue.

5.5.2 Single-Sideband Signal Measurements

The performance of the proposed DTX versus power back-off is measured with a single-sideband signal at 5.4GHz with 200MHz tone-spacing, and the output spectrum and corresponding I/Q image, LO leakage, and C-IMD3/H_{3BB} suppression are demonstrated in Fig. 5.22(a) and (b), respectively. Hence, the uncalibrated I/Q image, LO leakage, and C-IMD3/H_{3BB} preserve their approximate value of -64/-65/-69dBc over the power back-off. Additionally, the I/Q trajectory depicted in Fig. 5.22(c) shows that the proposed 50%-LO signed I/Q interleave up-converter retains its orthogonal summation enhancement over the output power back-off, and it demonstrates correct sign-bit operation without compression. Moreover, the single-sideband performance over the frequency band of 4.5-to-6 GHz dependent on tone-spacing of 10-to-140MHz is presented in Fig. 5.22(d-f). The intrinsic LO leakage, I/Q image, and C-IMD3/H_{3BB} remain better than -64/-60/-67dBc, respectively, without calibration while measuring five different samples of the proposed DTX.

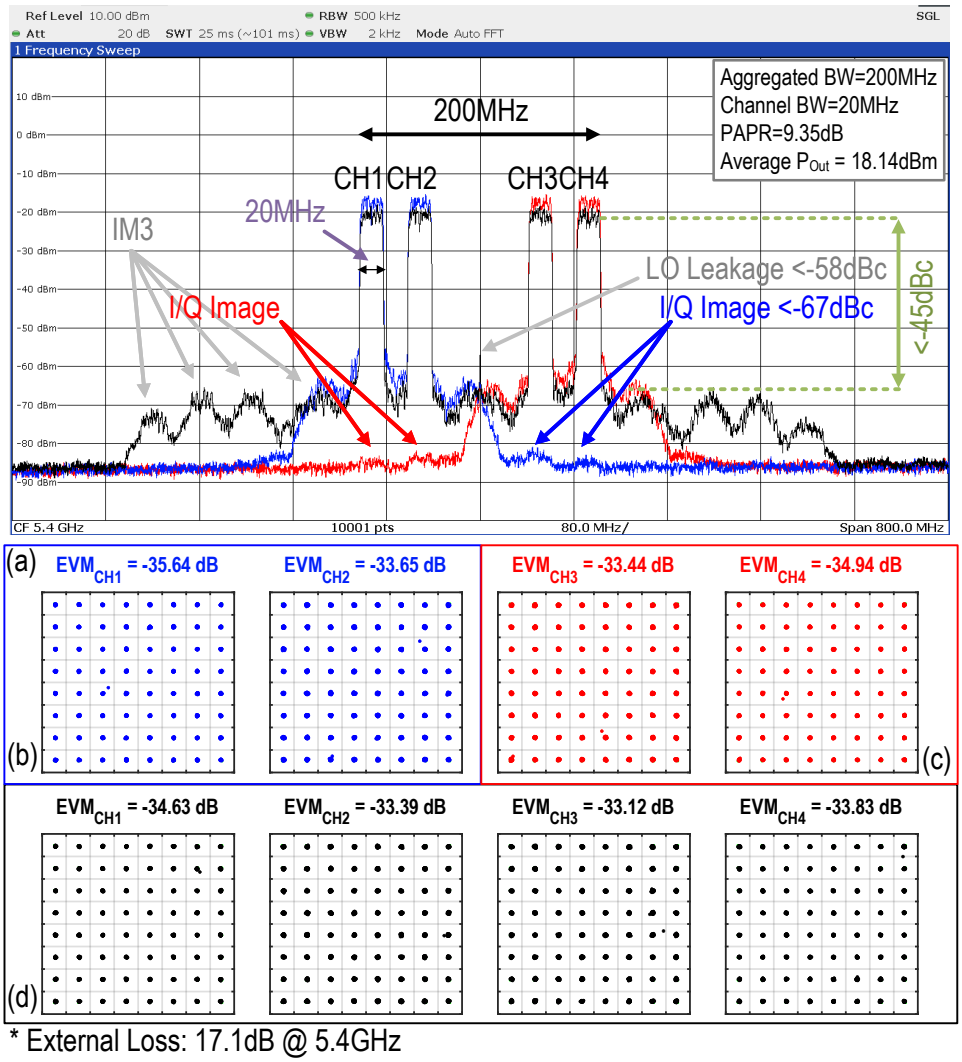


Figure 5.23: Measured (a) output spectrum of 2-/4-carrier 20MHz 64-QAM OFDM scenarios, (b)-(c) corresponding constellation points and EVM.

5.5.3 Complex Modulated Signal Measurements

The DTX dynamic performance is also verified by employing OFDM signals with different modulation bandwidths. A simple fixed memoryless 2×1-D DPD is employed for all complex

modulated signals in this work. The effect of the I/Q image on the performance of the multi-carrier scenarios is demonstrated in Fig. 5.23. In the first scenario, a 2-carrier "20MHz 64-QAM OFDM" signal, located at -90MHz (CH1) and -50MHz (CH2), respectively, away from f_C=5.4GHz, is applied to the DTX. Fig. 5.23(a) and (b) demonstrate the spectrum (blue) and its constellation diagrams with EVMs of -35.64dB and -33.65dB, respectively. In the second scenario, the TX signal is mirrored with respect to the carrier frequency, locating the channels at +50MHz (CH3) and +90MHz (CH4), respectively, away from f_C. Fig. 5.23(a) and (c) show the spectrum (red) and its constellation diagrams with EVMs of -33.44dB and -34.94dB, respectively. As illustrated, the channels' image component in the first scenario is located at the same position as the channels in the second scenario and vice-versa. Therefore, when operating four channels simultaneously, large image components dramatically deteriorate the EVM of each channel. The spectrum (black) and its constellation diagrams of the four-channel scenario are presented in Fig. 5.23(a) and (d), exhibiting that the channels' EVM has not been degraded significantly due to the decent I/Q image performance of the DTX.

The spectral purity of a single-carrier "40MHz 256-QAM OFDM" signal is measured at f_C=5.4GHz. The measured spectrum of the signal and its constellation diagram are depicted in Fig. 5.24(a) and (b). The DTX achieves an average output power of 18.9dBm while maintaining the average drain and system efficiencies of 43.11% and 24.51%, respectively. Utilizing the above-mentioned fixed memoryless 2×1-D DPD, the ACLR is better than -47dBc, and the EVM is -40.03dB. The ACLR and average EVM performances versus average output power are also exhibited in Fig. 5.24(c), reaching -45.14dB EVM at 12dBm average output power while the ACLR is better than -51dBc. These results indicate that the spectral purity and EVM of the proposed digital TX can meet the TX spectral emission requirements of the prevailing wireless communication standards.

A 6-carrier "40MHz 256-QAM OFDM" signal with an aggregated bandwidth of 240MHz is applied to the DTX, and the performance is verified at f_C= 5.4GHz using the simple fixed memoryless 2×1-D DPD. Fig. 5.25(a) exhibits the measured spectrum of the signal and its CH6 constellation diagram. Accordingly, the DTX delivers 17.82dBm average power while achieving an ACLR of better than -39dBc and an average EVM of -32.28dB. The measured average drain and system efficiencies are 41.23% and 22.17%, respectively. The ACLR and average EVM performances versus average output power are also exhibited in Fig. 5.25(c), achieving -37.55dB average EVM at 12dBm average power while the ACLR is better than

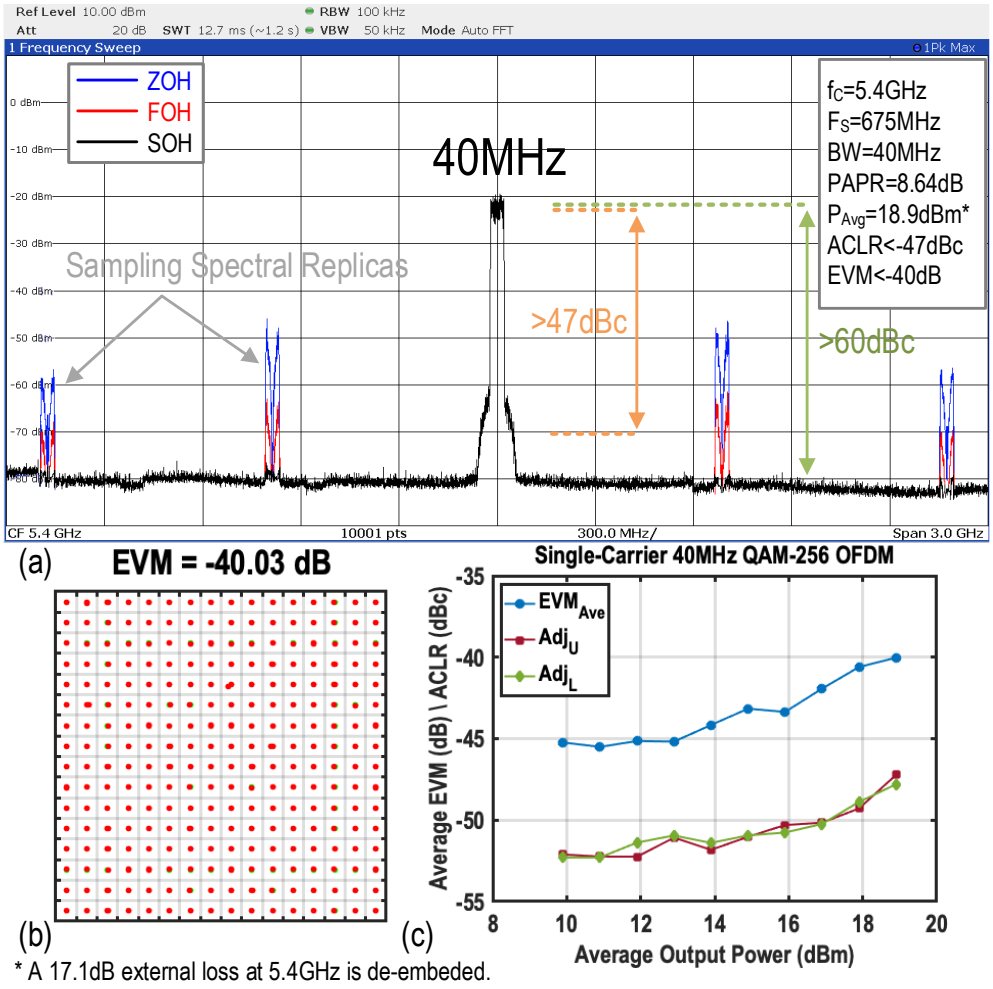


Figure 5.24: Measured (a) spectrum of single-carrier 40MHz 256-QAM OFDM signal, (b) constellation diagram and EVM. (c) ACLR and average EVM performances versus average output power.

-44dBc.

The effectiveness of signed ZOH, FOH, and SOH filters on the suppression of sampling spectral replicas is demonstrated in Fig. 5.26 where a 4-carrier "80MHz 512-QAM OFDM" signal with an aggregated bandwidth of 320MHz and F_S=675MHz is applied to the DTX, and the interpolation filter order is varied. The SOH filter achieves suppression of more than 30dB compared to ZOH for such a wideband signal.

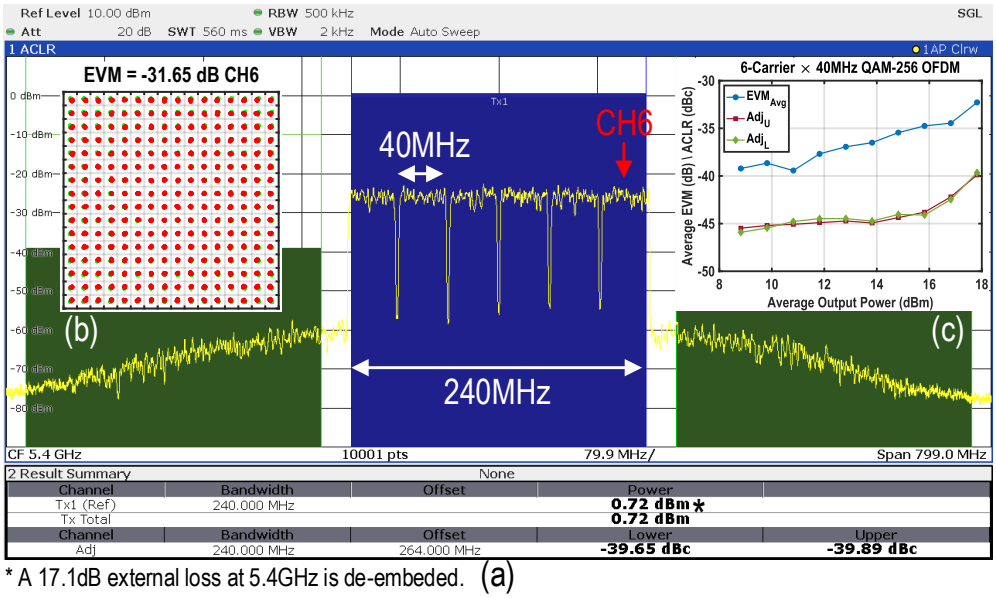


Figure 5.25: Measured (a) spectrum of 6-carrier 256-QAM OFDM signal, (b) the worst channel constellation diagram and EVM. (c) The ACLR and average EVM performances versus average output power.

The performance of our DTX is summarized and compared to that of the prior-art in Table 5.1. It indicates that the realized compact 4-way Doherty digital transmitter achieves excellent efficiency at 12dB DPBO at 5.4GHz while generating more than 27dBm peak power. The I/Q DTX can also support wide modulation bandwidth with high average output power and decent average drain and system efficiencies. Moreover, our 50%-LO signed-I/Q interleaved upconverter yields exceptional orthogonal I/Q summation compared to the other works.

5.6 Conclusion

This chapter demonstrates a compact wideband digital I/Q transmitter realized in a 40nm bulk CMOS. Introducing a 50%-LO signed I/Q interleaved up-converter and a compact four-way Doherty combiner, the proposed DTX achieves a spectrally pure operation, and simultaneously, it enhances its DPBO efficiency. The DTX generates more than 27.54dBm

5.6 Conclusion

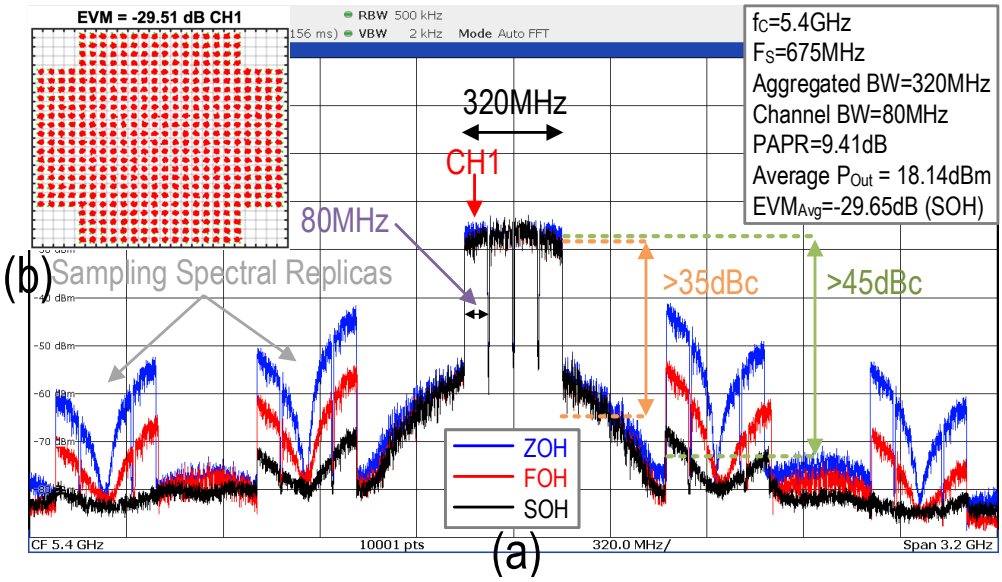


Figure 5.26: Measured (a) suppression of SSRs using ZOH/FOH/SOH filters. (b) the worst channel constellation diagram and EVM using SOH filter.

Table 5.1: Performance Summary And Comparison With State-Of-The-Art

Specifications		This Work		ISSCC 2021 A. Zhang		ISSCC 2021 B. Yang		JSSC 2020 S.W. Yoo		JSSCC 2020 A. Bassat		RFIC 2020 J. Sheth	TMTT 2019 D. Jung	JSSC 2020 D. Jung	JSSC 2020 Y. Yin	ISSCC 2016 P. Filho	TMTT 2017 W. Gaber	JSSC 2018 M.Mehrpoo	CICC 2020 Y.Shen	
Technology		CMOS 40nm		CMOS 65nm		CMOS 40nm		CMOS 60nm		CMOS 28nm		CMOS 65nm	CMOS 55nm	SOI 45nm	CMOS 40nm	CMOS 28nm	CMOS 28nm	CMOS 40nm	CMOS 40nm	
Architecture		Quadrature 4-way Doherty / CMCD		Current-Mode SHS		Quadrature SFCPA /Hybrid Doherty		TI-Doherty /Class G		Polar		4-way Doherty	Analog Doherty	Hybrid Doherty	Switched Transformer	RQDAC	DDRM	DDRM	IQ-Mapping DDRM	
Die Area		3.55mm² (1.5mm² ‡)		7.1mm²		2.2mm²		3.36mm²		4mm² ¥1		3mm²	6mm²	6mm²	0.8mm²	0.22mm² ‡	1.53mm²	0.21mm² ‡	1.1mm² ‡	
Supply		1V		N/A		1.2/2.4V		2.5V		1.4V		0.55V	5.5V	1.2V	1.1V	0.9V	3.6V	2V	2.5V	
Frequency		5.4GHz		5.4GHz		2.4GHz		2.4GHz		5GHz		5.25GHz	5.8GHz	2.3GHz	1.5GHz	2.4GHz	1GHz	3GHz	2.4GHz	
1-dB Power BW		5-5.6GHz		5.3-6.05GHz		2.3-2.8GHz*		N/A		N/A		4.5-5.25GHz*	5.4-6.1GHz*	2.1-2.5GHz*	1.3-3.5GHz	N/A	N/A	N/A	0.5-2GHz*	
Peak P_{Out}		27.4dBm		27dBm (5.7GHz)		30.3dBm		30dBm		27dBm		6.5dBm	27.2dBm	22.4dBm	21.4dBm	3.5dBm**	21dBm**	9.2dBm**	14.1dBm** @2GHz	
Efficiency (Drain/System)	Peak	47.4% / 30.66%		40.1% / N/A	5.4GHz	41.3% / 36.5%		40.2% / N/A		37% / N/A		42% / 26%	N/A / 24.5%	38.5% / N/A	N/A / 31.3%	N/A	N/A / 33%**	NA / 5.7%†	NA / 7.56%	
	3dB PBO	47.68% / 31.63%		32%* / N/A		37.5% / 32.9%		37.9% / N/A		31%* / N/A		36% / 20%*	N/A / 22*%	33%* / N/A	N/A / 28%*	N/A	N/A	N/A	N/A	
	6dB PBO	43.49% / 26.34%		26.3% / N/A		36.1% / 29.1%		38.8% / N/A		24%* / N/A		28% / 14%	N/A / 13*%	25%* / N/A	N/A / 27.7%	N/A	N/A	N/A	N/A	
	9dB PBO	41.06% / 23.1%		29.2% / N/A		30.9% / 23.7%		36.3% / N/A		18% / N/A		23% / 15%*	N/A / 8*%	18.7% / N/A	N/A / 18%*	N/A	N/A	N/A	N/A	
	12dB PBO	40.6% / 18.1%		19.1% / N/A		26.2% / 18.6%		29.4% / N/A		14%* / N/A		20%* / 7%*	N/A	13%* / N/A	N/A / 16.6%	N/A	N/A	N/A	N/A	
Modulation		240MHz 6×256-QAM OFDM	320MHz 4×512-QAM OFDM	20MHz 256-QAM	80MHz 64-QAM OFDM	60MHz 256-QAM	40MHz 1024-QAM	10MHz 1024-QAM	10MHz 64-QAM OFDM	20MHz MCS7	160MHz MCS11	1.6MHz 16-QAM	80MHz 256-QAM	40MHz 64-QAM	20MHz 64-QAM LTE	20MHz 64-QAM	40MHz 64-QAM WLAN	113MHz 64-QAM	160MHz 256-QAM	320MHz 256-QAM
Average P_{Out}(dBm)		17.82	18.16	22	18	23.3	20.4	23.2	19.1	21.1	19.2	2.9	17	15.3	15.2	-3.87	12	0.1	NA	5.15
Average Efficiency		41.23%(DE) 22.17%(SE)	41.12%(DE) 20.52%(SE)	27.4% (DE)	28.1% (DE)	30.7% (DE)	22.6% (DE)	36.2% (DE)	30.3% (DE)	26% (PE)	21% (PE)	34% (DE)	5.3% (PAE)	24.7% (DE)	25.3% (PAE)	1.7%* (SE)	11% (SE)	NA	NA	
EVM		-32.28dB	-29.65dB	-33.5dB	-30.4dB	-31.9dB	-35.9dB	-44.5dB	-41.7dB	-28dB	-35dB	-20dB	-34.8dB	-32dB	-32.5dB	-36dB	-30.3dB	-27dB	-36dB	-32dB
PAPR		9.68dB	9.41dB	4.4dB	8.4dB	6.98dB	9.86dB	6.8dB	10.9dB	5.9dB	7.8dB	3.6dB	6.3dB§	7.1dB	6.2dB	7dB	8.73dB	6.2dB	8dB	8dB
LO Leakage / IQ image / CIM3		<-58 / -60 / -67dBc		N/A		N/A		N/A		N/A		N/A	N/A	N/A	N/A	-59 / -44 / -50dBc	-44 / -39 / -26dBc	N/A / -45 / -56dBc	-52 / -54 / -55*dBc	
Linearization		DPD		N/A		DPD		No		DPD		DPD	MGTR	AM-AM LUT	DPD	DPD	DPD	No	No	

* Estimated from reported figures and plots. ** Off-chip matching network. ‡Core area. ¥1 Area including Digital front end, DPLL, and LB/HB DTX. †Excluding LO generation. § Measured at 3.9dB additional PBO.

with 46.35% drain efficiency in a 4-to-6.2GHz band. Its EVM and ACLR performance are better than -31dB and 39dB, respectively, for a 6-carrier "40-MHz 256-QAM OFDM" signal. The realized DTX can be reconfigured as a stand-alone DDS to support signals with 320MHz modulation bandwidth. Moreover, the proposed bits-in RF-out TX replicates the spectral purity performance of its state-of-the-art analog-intensive counterparts. Finally, it can perform as a high-power energy-efficient CMOS transmitter to target next-generation multi-band/multi-band applications requiring large modulation/aggregated bandwidth.

Chapter 6

A Low Complexity Digital Predistortion Technique For Digital Transmitters

6.1 Introduction

Modern sub-6GHz wireless communication systems continuously evolve to support more users and provide higher data-rates within the already overcrowded RF spectrum. To ensure high spectral efficiency, compact constellations and multiple access techniques based on orthogonal frequency division multiplexing (OFDM) are used. Nevertheless, this spectral efficiency is achieved at the expense of much stricter requirements on the spectral purity performance of the RF front-end. As previously discussed, the linearity and spectral purity performance of wireless transceivers are specified in standards using two metrics:

- In-band error vector magnitude (EVM), characterizing the error level between the ideal signal and the actual transmitted signal.
- Out-of-band adjacent channel leakage ratio (ACLR), addressing the interference emission level outside the transmission frequency band.

Nonlinear distortion is mainly caused by the transmitter PAs operating close to saturation for power efficiency considerations. Therefore, it is useful to linearize the PA to avoid any power leakage to adjacent channels, which would lower its ACPR. At the same time, a high in-band SNR must be ensured in the TX in favor of a low EVM.

Operating the PA in a linear mode with high PAPR signals will degrade its power efficiency. Accordingly, the power amplification stage design is often the result of a trade-off between linearity and power efficiency. Digital pre-distortion (DPD) is a linearization technique often used to improve the inherent trade-off between linearity and efficiency in PAs. As it is conceptually shown in Fig. 6.1, this is done by a pre-distorter preceding the PA offering a pre-correction to the driving signal so that the overall input-output transfer function becomes linear with respect to the original input signal.

The current state-of-the-art DTXs often use a Doherty PA to achieve high efficiency at output power back-off conditions. Thanks to their digital essence, DPD is the natural approach to achieve the required linearity performance in these DTX circuits. As previously stated, the RF-DACs in the DTXs comprise energy-efficient DPA arrays which are driven directly by digital control words that, unlike an analog PA, use fixed voltage levels to drive the gates. The output power is controlled by the overall effective width of the activated

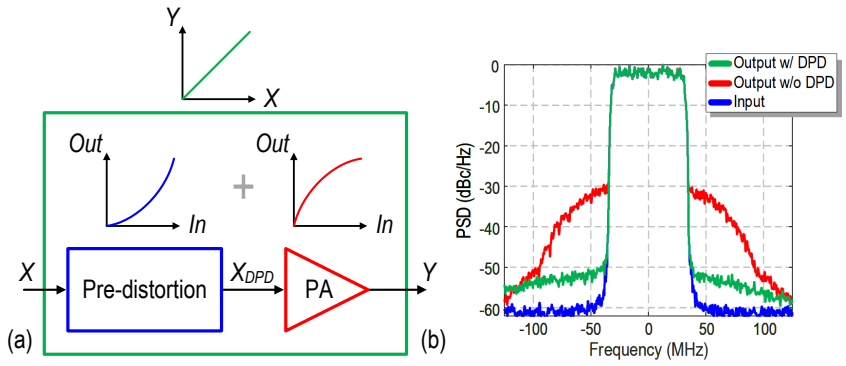


Figure 6.1: (a) Basic concept of predistortion, (b) example of the input/output spectrum of a nonlinear PA, with and without DPD [124].

devices, which varies according to the input amplitude code word (ACW). Otherwise stated, the effective R_{On} of the output stage changes nonlinearly with respect to the input code, thus creating the ACW-AM nonlinearity. Namely, the ACW-AM nonlinearity is the result of the code-dependent conductance of the drain node [12, 59, 125]. Furthermore, activating the switches and modulating the drain voltage, changes the voltage-dependent drain capacitance of the digital power switches. The change in the capacitance, in combination with the code-dependent conductance $(1/R_{On})$ of the output stage, causes ACW-PM nonlinearity [12, 29].

To address these issues, this chapter proposes a low complexity constellation-mapping DPD technique based on 1-D mapping of I and Q baseband signals.

6.2 The 2×1-D DPD Process

The pre-distortion approach utilized in this dissertation is based on a constellation-mapping-based DPD algorithm [70,126–128]. This work proposes a very simple, modified constellation-mapping DPD using an 1-D mapping of I_{BB-UP} and Q_{BB-UP}, so effectively, 2×1-D mapping. A complex modulated baseband data can be defined as:

$$\begin{aligned} IQ_{BB-UP} &= I_{BB-UP} + \mathrm{j} \times \mathrm{Q_{BB-up}} \\ &= A_{IQ}\left(I_{BB-UP}, Q_{BB-UP}\right) \angle \phi_{IQ}\left(I_{BB-UP}, Q_{BB-UP}\right) \end{aligned} \tag{6.1}$$

where I_{BB-UP} and Q_{BB-UP} are shown in Fig. 6.2(a). Moreover, A_{IQ} and ϕ_{IQ} represent

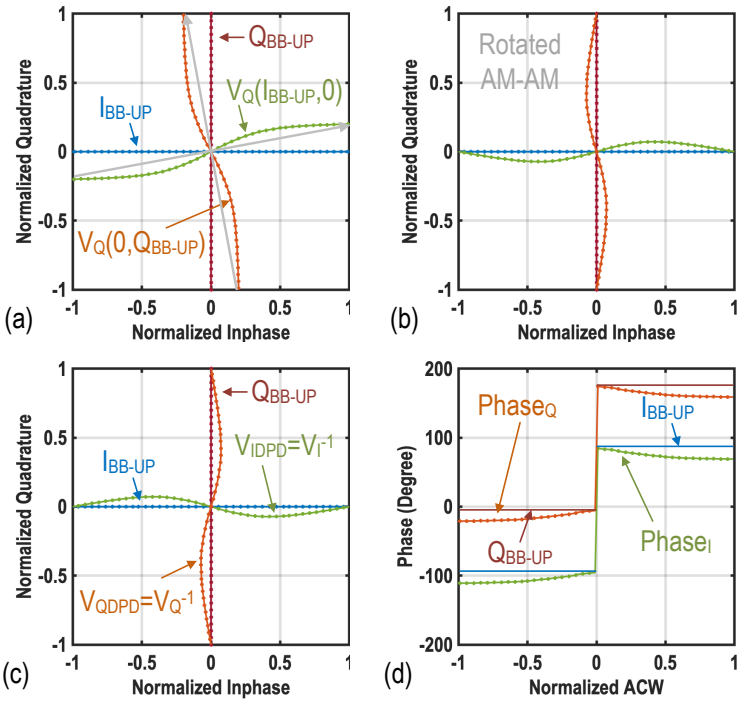


Figure 6.2: (a) Input codes along with their corresponding nonlinear output voltages (ACW-AM); (b) phase adjusted nonlinear output voltages; (c) DPD in-phase and quadrature input code mapping diagram; (d) output phase versus input code (ACW-PM).

the envelope and phase information of the corresponding baseband data, respectively. Thus, ideally, the modulated RF output of the RF-DAC is expressed as:

$$\begin{aligned} V_{IQ}\left(I_{BB-UP}, Q_{BB-UP}\right) &= IQ_{BB}\left(I_{BB-UP}, Q_{BB-UP}\right) \times \exp\left(\mathrm{j}\omega_0 \mathrm{t}\right) \\ &= A_{IQ} \times \exp\left(\mathrm{j}\left(\omega_0 \mathrm{t} + \phi_{\mathrm{IQ}}\right)\right) \end{aligned} \tag{6.2}$$

Nonetheless, since the RF-DAC acts like a nonlinear transmitter, the RF output of the RF-DAC can be rewritten as:

$$V_{IQ}\left(I_{BB-UP}, Q_{BB-UP}\right) = \left(V_I\left(I_{BB-UP}, 0\right) + \mathrm{j} \times \mathrm{V_Q}\left(0, \mathrm{Q_{BB-up}}\right)\right) \times \exp\left(\mathrm{j}\omega_0 \mathrm{t}\right) \tag{6.3}$$

where $V_I\left(I_{BB-UP}, 0\right)$ and $V_Q\left(0, Q_{BBUP}\right)$ are the corresponding nonlinear complex profiles of I_{BB-UP} and Q_{BB-UP}, which are normalized to their related input codes. These profiles

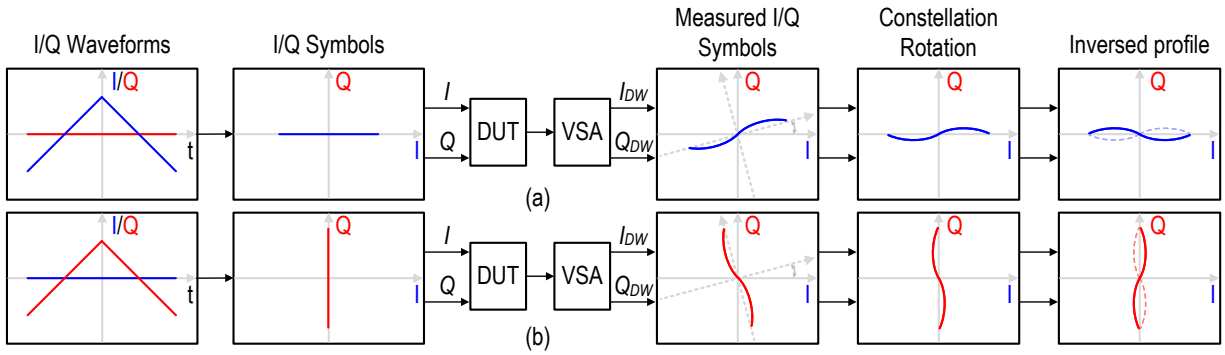


Figure 6.3: Practical, $V_I\left(I_{BB-UP}, 0\right)$ and $V_Q\left(0, Q_{BB-UP}\right)$ extraction: (a) in-phase (I) path ramp function while the quadrature (Q) path is zero; (b) quadrature (Q) path ramp function while the in-phase (I) path is zero.

are indicated in Fig. 6.2(a). In practice, $V_I\left(I_{BB-UP}, 0\right)$ and $V_Q\left(0, Q_{BB-UP}\right)$ are acquired as follows (Fig. 6.3): first, due to the orthogonal operation of the I/Q RF-DACs, I_{BB} and Q_{BB} are individually swept and fed to the I/Q DTX. In other words, a ramp function is applied to the in-phase (I) while the quadrature (Q) path is zero (Fig. 6.3(a)). The same process will be used for the quadrature path in which a ramp function is applied to the Q path while the I path is zero (Fig. 6.3(b)). In both cases, the subsequent RF output is down-converted, and the related baseband complex signals, i.e., $V_I\left(I_{BB-UP}, 0\right)$ and $V_Q\left(0, Q_{BB-UP}\right)$, are obtained. Then the $V_I\left(I_{BB-UP}, 0\right)$ and $V_Q\left(0, Q_{BB-UP}\right)$ should be rotated such that the maximum I/Q code-words and their corresponding point in the measured profiles are aligned (Fig. 6.2(b)). Next, the inverse function of $V_I\left(I_{BB-UP}, 0\right)$ and $V_Q\left(0, Q_{BB-UP}\right)$ are evaluated and depicted in Fig. 6.2(c). The in-phase and quadrature DPD profiles are as follows:

$$\begin{aligned} V_{IDPD}(I,Q) &= V_I^{-1}\left(I_{BB-UP}, 0\right) \\ &= I_{DPD-I} + \mathrm{j} \times \mathrm{Q}_{DPD-I} \end{aligned} \tag{6.4}$$

$$\begin{aligned} V_{QDPD}(I,Q) &= V_Q^{-1}\left(0, Q_{BB-UP}\right) \\ &= I_{DPD-Q} + \mathrm{j} \times \mathrm{Q}_{\mathrm{DPD\text{-}Q}} \end{aligned} \tag{6.5}$$

The following relationships are established between I_{BB-UP} and $V_{IDPD}\left(I,Q\right)$ as well as Q_{BB-UP} and $V_{QDPD}\left(I,Q\right)$:

$$\begin{aligned} I_{BB-UP} &= V_I\left(V_I^{-1}\left(I_{BB-UP}, 0\right)\right) \\ &= V_I\left(V_{IDPD}(I,Q)\right) \\ &= V_I\left(I_{DPD-I}, Q_{DPD-I}\right) \end{aligned} \tag{6.6}$$

$$\begin{aligned} Q_{BB-UP} &= V_Q\left(V_Q^{-1}\left(0, Q_{BB-UP}\right)\right) \\ &= V_Q\left(V_{QDPD}(I,Q)\right) \\ &= V_Q\left(I_{DPD-Q}, Q_{DPD-Q}\right) \end{aligned} \tag{6.7}$$

Therefore, in this DPD process, I_{BB-UP} and Q_{BB-UP} are individually mapped to $V_{IDPD}\left(I,Q\right)$ and $V_{QDPD}\left(I,Q\right)$, respectively. Specifically, this DPD process can be inferred as a 1-D mapping of two individual signals of I_{BB-UP} and Q_{BB-UP}, i.e., 2×1-D. In particular, since I and Q paths are orthogonal, the DPD does not require a 2-D exhaustive search of the entire constellation diagram, which is utilized in [118]. Consequently, due to orthogonality, the subsequent I_{DPD} and Q_{DPD} are obtained as follows

$$I_{DPD}\left(I_{BB-UP}, Q_{BB-UP}\right) = I_{DPD-I} + I_{DPD-Q} \tag{6.8}$$

$$Q_{DPD}\left(I_{BB-UP}, Q_{BB-UP}\right) = Q_{DPD-I} + Q_{DPD-Q} \tag{6.9}$$

Note that the DPD profiles of V_{IDPD} and V_{QDPD} are obtained only at the beginning of the measurement operation and will remain unchanged afterward. It should be pointed out that the ACW-AM and ACW-PM profiles are at the carrier frequency, and temperature dependent. Thus, its related DPD profiles must be updated for various frequency/temperature conditions. Moreover, for the digital Doherty PAs, transition points, where peak branches are activated, will appear as singularities in the ACW-AM and ACW-PM curves. Therefore, main and peak branches should be pre-distorted separately in the ACW-AM and ACW-PM LUTs to improve the DPD algorithm convergence.

Fig. 6.4 depicts the constellation mapping measurement setup structure. Using MATLAB, in-phase and quadrature randomized symbols (I_{Symb} and Q_{Symb}) are generated and supplied to the I/Q baseband modulator. This block creates QAM signals of I_{BB} and Q_{BB}. Then, to confine the modulation bandwidth, I_{BB} and Q_{BB} get pulsed-shaped using a root-raised-cosine (RRC) interpolation filter and up-sampled to the F_{S}. Afterward, I_{BB-UP} and

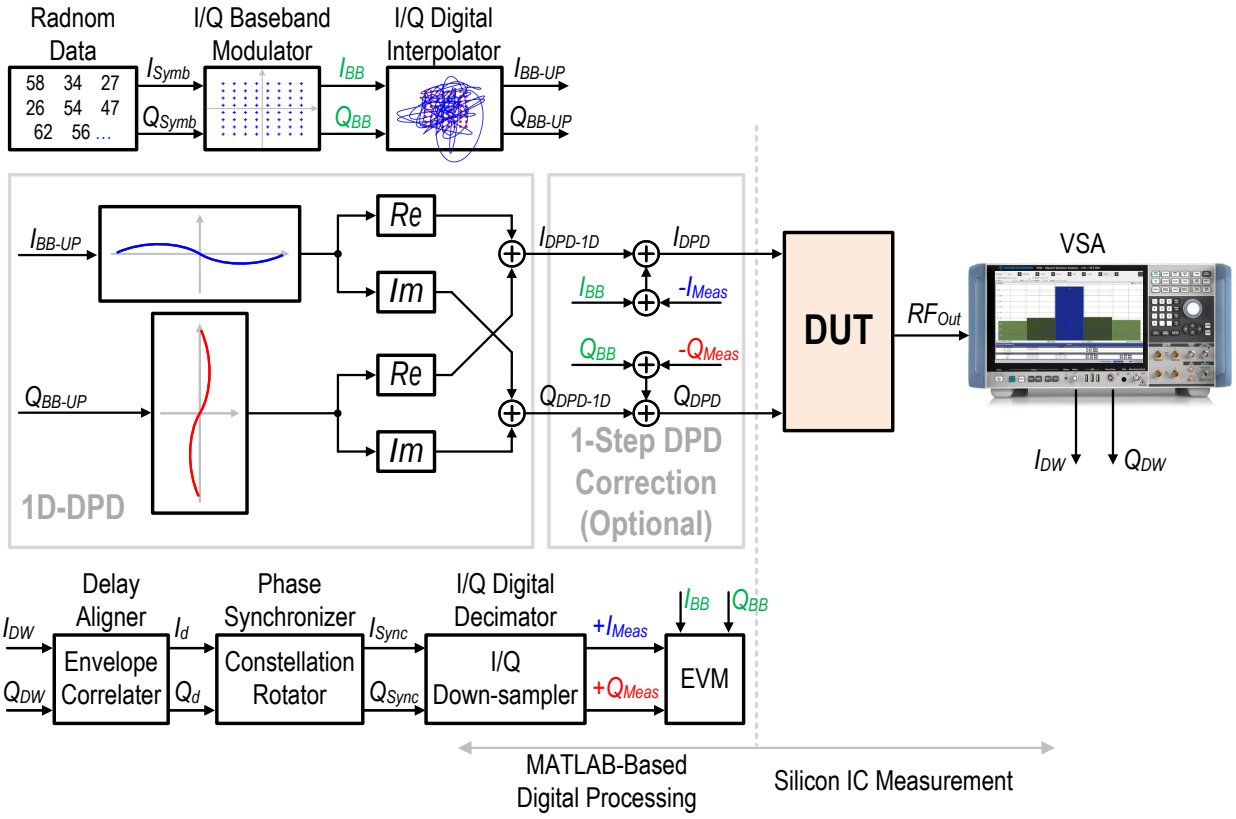


Figure 6.4: DPD measurements constellation mapping flow.

Q_{BB-UP} are mapped utilizing the abovementioned technique. Next, the pre-distorted signals (I_{DPD} and Q_{DPD}) are uploaded into two designated on-chip SRAMs. After that, the upconverted RF signal is down-converted using a vector signal analyzer (VSA), and the subsequent down-converted digital in-phase (I_{DW}) and quadrature (Q_{DW}) signals are fed back to MATLAB. Three important steps should be followed. First, the measurement time-delay should be calibrated. Then, the subsequent complex signal phase, i.e., $\phi_{IQ} = \angle(I_d + jQ_d)$, should be rotated such that the eventual phase, i.e., $\phi_{Sync} = \angle(I_{Sync} + jQ_{Sync})$ is the same as the original complex phase, i.e., $\phi_{BB-UP} = \angle(I_{BB-UP} + jQ_{BB-UP})$. Finally, I_{Sync} and Q_{Sync} are down-sampled utilizing an RRC decimation filter to recover the original I/Q baseband modulated signals, i.e., I_{Meas} and Q_{Meas}. Comparing the measured I_{Meas} and Q_{Meas}

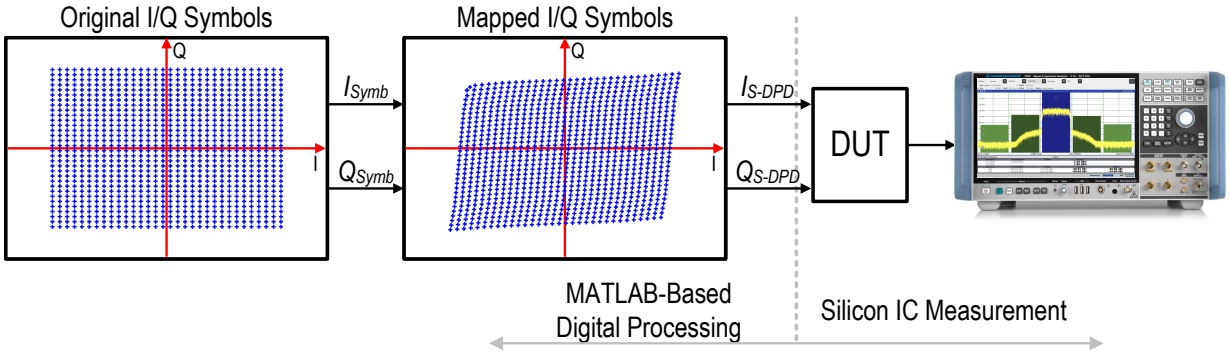


Figure 6.5: Mapped I/Q symbols.

with the original I_{BB} and Q_{BB}, the EVM is calculated. Using the DPD procedure discussed before, we can generate a universal mapped I/Q symbols (I/Q look-up table), as shown in Fig. 6.5.

6.3 Verification of the 2×1-D DPD Process

Examining this approach, a 1024-symbol constellation signal is created (Fig. 6.6(a)). Based on the Fig. 6.6(b) sweeping concept, the constellation diagram is continuously swept from the top-left to the top-right in a snake-like manner and traversed back again to its original point in order to preserve continuity. These signals are then up-sampled and interpolated using an RRC interpolation filter to produce I_{BB-UP} and Q_{BB-UP} (see their I/Q trajectories in Fig. 6.6(c), (d)). Next, the resultant signals are pre-distorted (I_{DPD} and Q_{DPD}) and loaded into on-chip SRAMs. Fig. 6.6(e) shows the effect of the I/Q DPD mapping on the I/Q trajectories of the original modulated signals, and their corresponding measured trajectories are demonstrated in Fig. 6.6(f). The RF output signal is down-converted, and its corresponding I/Q trajectories are exhibited in Fig. 6.6(g), demonstrating an excellent agreement with the original I/Q trajectories of Fig. 6.6. I_{Sync} and Q_{Sync} are then down-sampled and decimated to create the measured constellation diagram (Fig. 6.6)(h). Its related EVM is -46.91dB. It should be mentioned that, due to the limited data length of I_{DPD} and Q_{DPD}, which are repeatedly fed to the RF-DAC circuit from the first data point to the last, any discontinuity between the first data point and the last one creates an undesirable

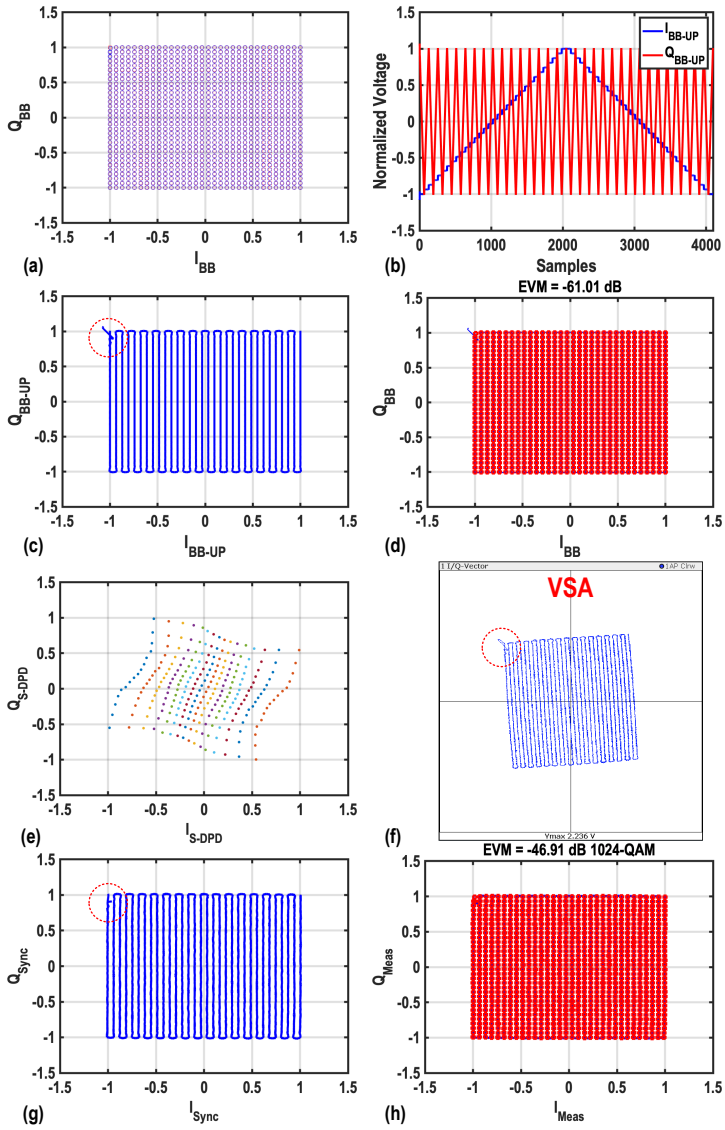


Figure 6.6: DPD measurements: (a) 1024-QAM constellation diagram (I_{BB}/Q_{BB}); (b) Trajectories of their related time domain waveforms; (c),(d) I_{BB-UP}/Q_{BB-UP} trajectories; (e) predistorted I_{DPD}/Q_{DPD} trajectories; (f) measured I_{DW}/Q_{DW} trajectories; (g) measured I_{Sync}/Q_{Sync} trajectories (h) measured 1024-point constellation.

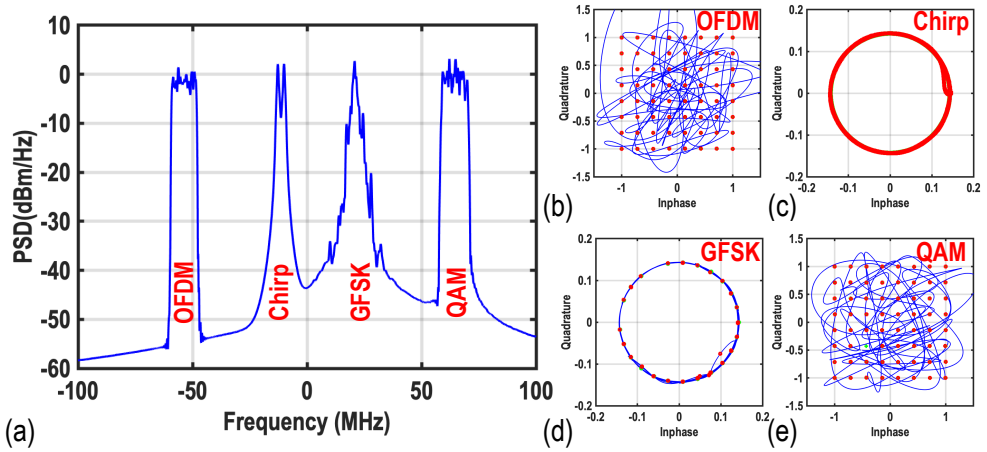


Figure 6.7: (a) Generated "multi-channel OFDM, Chirp, GFSK, and QAM signal" spectrum; (b)-(e) corresponding constellation diagrams.

spectral jump. To alleviate this issue and to preserve continuity, the data length of I_{BB} and Q_{BB} are doubled and applied to the RRC interpolation filter, and then only half of the data length of the subsequent I_{BB-UP} and Q_{BB-UP} are exploited and applied to the DPD lookup table. This technique is referred to as a wrap-around process. As a result, the beginning points of the I/Q trajectories of Fig. 6.6, indicated with circles, have been shaped in such a way as to ensure the continuity of the I/Q signals.

6.4 Measurement Results of the 2×1-D DPD Process

The measurements in this dissertation are performed using the constellation-mapping-based DPD algorithm presented in this chapter. Nevertheless, to test the proposed DPD approach further, the proposed DTX in chapter 5 is tested with different signals in the measurement setup shown in Fig. 5.20 conforming to the DPD process illustrated in Fig. 6.4. The I/Q data are generated in MATLAB and then applied to the DTX using four on-chip 4K SRAMs (one SRAM for each I/Q DPA) running at F_S=675MHz. The output signal is down-converted and digitized using R&S-FSW and downloaded onto a PC. The DPD algorithms are implemented in MATLAB.

First, a multi-channel signal is generated by combining OFDM, Chirp, GFSK, and QAM

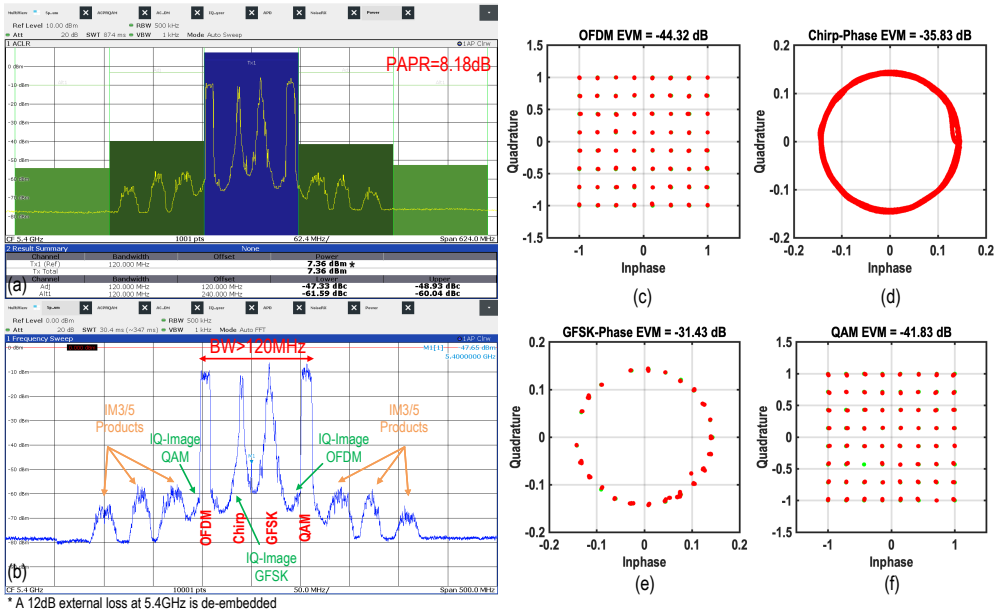


Figure 6.8: " Multi-channel OFDM, Chirp, GFSK, and QAM signal" measurement results, (a)-(b) spectrum with DPD; (c)-(d) corresponding constellation diagrams.

signals (Fig. 6.7(a)-(e)) with aggregated bandwidth of more than 120MHz at 5.4GHz and is applied to the chip and measured at 5.4GHz. Fig. 6.8(a)-(b) exhibits the measured spectrum of the signal when applying the DPD. The ACPR is better than -47.33dBc, while the alternate channel power ratio is better than -60.04dBc. The constellation diagrams are depicted in Fig. 6.8(c)-(f). The measured EVM is -44.32dB, -35.83dB, -31.43dB, and -41.83dB for 64-QAM OFDM, Chirp, GFSK, and 64-QAM channels, respectively. Moreover, the average power is 19.35dBm, while its related drain efficiency is 40%.

Second, the DTX is tested with six-channel×10MHz QAM and OFDM signals with aggregated bandwidth of more than 150MHz at 5.4GHz. Fig. 6.9(a)-(b) shows the measured spectrum of the signal with and without application of the DPD. The ACPR is better than -47.34dBc, while the constellation diagrams depicted in Fig. 6.9(c)-(d) present an EVM of -41.03/-40.01dB for channel-1/-6, respectively. The digital transmitter achieves an average output power of more than 19dBm while maintaining the average drain and system efficiency of more than 40% and 24%, respectively.

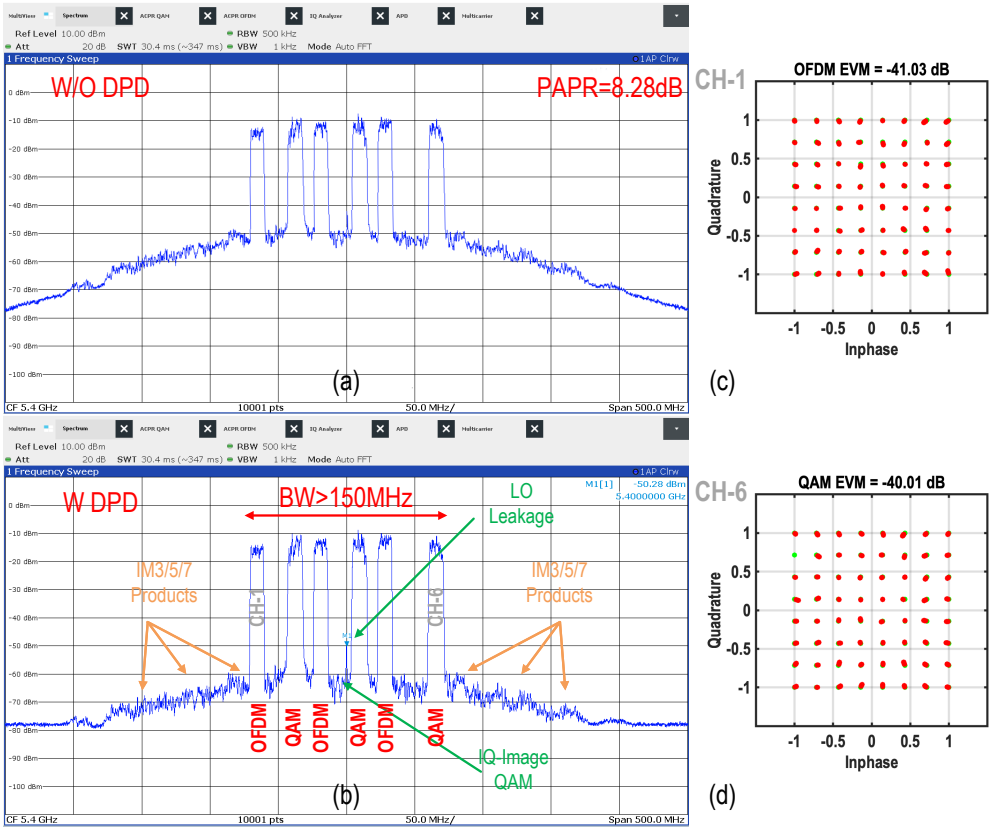


Figure 6.9: " multi-channel signal OFDM and QAM" measurement results, (a)-(b) spectrum with and without DPD; (c)-(d) channel-l/-6 constellation diagrams.

6.5 Conclusion

A switch-mode DPA typically shows significant static nonlinearities, which normally can be corrected using LUT-based DPD. This chapter presents a simple 2×1-D constellation-mapping-based DPD technique for the I/Q DTXs. Specifically, this DPD process can be inferred as a 1-D mapping of two individual signals of I and Q, i.e., 2×1-D. In particular, since I and Q paths are orthogonal, the DPD does not require a 2-D exhaustive search of the entire constellation diagram. The DPD is verified by a 1024-symbol modulation created based on a continuously snake-like manner sweeping of the constellation diagram. It is demonstrated that by using this technique, for a four-channel OFDM+Chirp+GFSK+QAM

signal with aggregated bandwidth of 120MHz, the ACPR is better than 47.3dBc. The EVMs are -44.32dB, -35.83dB, -31.43dB, and -41.83dB for 64-QAM OFDM, Chirp, GFSK, and 64-QAM channels, respectively while generating more than 19dBm power with better than 40% drain efficiency. To the best of the author's knowledge, it is the first reported signal measurement with the mentioned configuration. Furthermore, in a six-channel OFDM-QAM signal scenario with aggregated bandwidth of 150MHz, the ACPR is better than -47.3dBc, and EVM is better than -41/-40 for channel-1/-6, respectively.

It is worth mentioning that, as discussed in chapter 2 (section 2.2.2.2), the I and Q combination method has a significant impact on the I/Q interaction. In an analog domain combination method, the possible overlap between the I and Q signals causes unwanted I and Q interaction, degrading the EVM and linearity. Therefore, the proposed 2×1-D approach may experience some difficulties with compression when both I and Q are active and at their maximum code-word. However, in a more digitally-intensive realization, the I and Q combination can also be carried out in the digital domain, addressing the challenges of analog-intensive I and Q RF signals summation, yielding a more effective DPD process. Moreover, although the memory effects in a well-designed DPA are typically more minor than in an analog PA since only the bias connection of the final stage tends to contribute to these memory effects, future work may include memory effects in the proposed DPD process.

Chapter 7

Conclusion

This dissertation aims to advance the knowledge of the analysis, design, and implementation of wideband and energy-efficient digital-intensive transmitters. The work is motivated by the increasingly demanding wireless communication standards, together with the advances in circuit-design approaches invoked by CMOS process scaling and the desire to maximize the level of integration. These circumstances create the need to explore transmitter architectures beyond the level of the most established ones, which are exclusively analog up to date. To attain this goal, this thesis focused the research on digital transmitters managing wideband complex modulated signals to support multi-mode/multi-band communication standards. Moreover, along with generating adequate RF power, circuit innovations to improve efficiency at full power and back-off are presented to address the demand for high average efficiency for high PAPR signals. At the same time, to satisfy the inband signal accuracy and out-of-band spectrum emissions requirements, we introduce and investigate solutions that combine an innovative clocking scheme, high-order digital filters, and a low-complexity DPD technique requiring minimal computational power. The proposed techniques are examined with theoretical analysis, system-level and circuit simulations, design of integrated circuits and printed circuit boards, and measurements of fabricated prototype circuits. In this aspect, this final chapter concludes with the dissertation's most important findings by summarizing and reiterating the accomplishments achieved throughout the thesis in Section 7.1. Moreover, it offers several procedures to expand this work to the next level.

7.1 Thesis Outcome

- **A Wideband Energy-Efficient Multi-Mode CMOS Digital Transmitter**
  Chapter 3 presents a wideband, energy-efficient digital transmitter (DTX) suitable for multi-mode/multi-band wireless communication applications. It features various operational modes comprising Cartesian (Modes-1/2) and multi-phase (Modes-3/4) configurations utilizing LO clocks with different duty cycles in interleaving and non-interleaving configurations. The multi-phase operation compromises polar and Cartesian features by mapping the I/Q signals into two non-orthogonal basis vectors with 45° relative phase difference and a 3-bit phase selector scheme. The various operation modes are extensively analyzed and compared. Fabricated in a 40-nm CMOS process with an off-chip matching network, the proposed DTX occupies a core area of 0.72mm^2

and delivers 23.18dBm RF peak power at 2.1GHz from a 0.95V supply voltage, with drain/system efficiencies of 66.26/52.59%, respectively. Utilizing a simple memory-less digital pre-distortion (DPD) for a 160MHz four-channel 64-QAM OFDM signal, the DTX delivers an average P_{Out} of 13.5/11.4/7.7/9.4dBm, achieving an ACLR of better than -42/-40/-40/-38dBc and an average EVM of -36/-34/-34/-32dB, operating in modes-1/2/3/4, respectively. While transmitting a 200MHz single channel 256(1024)-QAM OFDM signal at 2.4GHz in Mode-1/-4, the average delivered output power is 14.11/9.29(12.23/7.32)dBm, while the ACLR and EVM are better than -42/-41(-43/-43)dBc and -34.6/-33.1(-33.5/-33.9)dB, respectively.

- **A Wideband Multi-Mode Digital Doherty Transmitter in 40nm CMOS**
  Chapter 4 provides the design and implementation details as well as the measurement results of a 40nm CMOS wideband digital Cartesian push-pull inverted Doherty operating in class-E followed by the first wideband multi-phase DTX applied in a two-way Doherty configuration. An off-chip inverted Doherty power combiner enhances the TX's average efficiency over a wide 2-to-3.2GHz frequency band. The DTX in Doherty Cartesian mode provides 25.3dBm peak power with a drain/DTX line-up efficiency (DE/SE) of 58.7%/44.9%, respectively, at 2.4GHz. When operated with a 160MHz 256-QAM OFDM signal, it achieves 46.1%/32.7% average DE/SE, with an ACLR and EVM better than -40.6dBc and -33.9dB, respectively, using a simple memory-less digital pre-distortion (DPD). The DTX in Doherty multi-phase operation provides 22.1dBm peak power with a drain/DTX line-up efficiency (DE/SE) of 57.97%/44.41%, respectively, at 2.4GHz. When operated with a 200MHz 1024-QAM OFDM signal, it achieves 46.02%/34.33% average DE/SE, with an ACLR/EVM better than -43dBc/-35dB, respectively, using a simple digital pre-distortion (DPD).

- **A Wideband Four-Way Doherty Bits-In RF-Out CMOS Transmitter**
  Chapter 5 presents a wideband, 12-bit four-way Doherty Cartesian digital transmitter (DTX) featuring an innovative 50%-LO signed I/Q interleaved up-conversion technique that enables close to perfect orthogonal I/Q summation. The DTX incorporates a compact 4-way lumped-element Doherty power combining network to enhance its average efficiency at deep power back-off (DPBO). It comprises a signed second-order hold (SOH) interpolation filter to significantly suppress the sampling spectral repli-

cas. The proposed DTX is realized in a 40nm bulk CMOS and delivers a peak output power of 27.54dBm with drain and system efficiencies of 46.35% and 30.77%, respectively, at 5.3GHz. At 12dB DPBO, the realized DTX demonstrates a drain efficiency of 41.74-to-39.27% in a 5.2-to-5.5GHz band, respectively. Its intrinsic I/Q image, LO leakage, and C-IMD3/H3BB for a 200MHz tone spacing over a 4.8-to-6.2GHz band are -64dBc, -65dBc, -69dBc, respectively, without calibration. Applying a simple memoryless 2×1-D digital pre-distortion, its error vector magnitude and adjacent channel leakage ratio are lower than -31dB and -39dBc, respectively, for a 6-carrier "40MHz 256-QAM OFDM" signal with 18dBm average output power and 41% average drain efficiency. The signed SOH functionality is verified employing 4-carrier×80MHz 512-QAM OFDM with spectral purity of better than -35dBc while its baseband sampling frequency is 675MHz.

- **A 2×1-D Digital Predistortion Technique**
  Chapter 6 establishes a basic understanding of the non-linearities of a digital TX and how to correct them. Accordingly, a straightforward modified constellation-mapping DPD technique based on 1-D mapping of I and Q baseband signals is introduced which does not require a 2-D exhaustive search of the entire constellation diagram. The DPD is verified by a 1024-symbol modulation created based on a continuously snake-like manner sweeping of the constellation diagram. The performance of the DPD is challenged by a four-channel OFDM+Chirp+GFSK+QAM signal with aggregated bandwidth of 120MHz, resulting in an ACPR of better than 47.3dBc. The EVMs are -44.32dB, -35.83dB, -31.43dB, and -41.83dB for 64-QAM OFDM, Chirp, GFSK, and 64-QAM channels, respectively while generating more than 19dBm power with better than 40% drain efficiency. To the best of the author's knowledge, it is the first reported signal measurement with the mentioned configuration. Furthermore, in a six-channel OFDM-QAM signal scenario with aggregated bandwidth of 150MHz, the ACPR is better than -47.3dBc, and EVM is better than -41/-40 for channel-1/-6, respectively.

7.2 Suggestions for Future DTX Developments

The research presented in this thesis introduces several novel circuit-level and system-level techniques for wideband and energy-efficient digital transmitters. The effectiveness of the proposed concepts has been demonstrated through various hardware realizations that achieve state-of-the-art performance. Nevertheless, a researcher's work is never done, and several questions remain unanswered, providing new ideas and opportunities for future research activities. In the following, some suggestions are given for further research and development:

- Despite the decent spectral performances already achieved with the DPD based on I/Q code mapping introduced in chapter 6, it is not yet entirely evident to what extent the linearity performance of the proposed DTXs can be improved. Thoroughly evaluating this issue would require a more advanced DPD process.

- The 50%-LO signed I/Q interleaved up-converter introduced in chapter 5 is implemented for a Cartesian I/Q DTX clock scheme. This technique can be extended to multi-phase operation to improve its performance and boost the frequency of operation.

- Development of new technologies and assembly techniques would, in the future, enable CMOS-GaN digital transmitters. This would open up unprecedented TX performance.

- In this thesis, the DTX is always loaded by a fixed 50Ω, which resembles the impedance of an antenna. Nonetheless, a practical antenna's impedance can be anything but 50Ω which would affect the output power, efficiency, EVM, and, most importantly, its linearity. This issue can be alleviated by adding impedance tuning circuitry, e.g., switch-capacitor banks. The research question would be how to do this in a compact area at low loss?

- The four-way power combiner in chapter 5 utilizes a first-order high-pass model for the transmission lines. The power combiner can also be implemented with higher-order high-/low-pass elements yielding the question of what is the best network configuration in terms of power, efficiency, and bandwidth?

- Future research can concentrate on digitally switchable matching networks to adjust the load impedance observed by the Main DPA in back-off. This feature would result in a digital Doherty with digitally adjustable back-off power efficiency peaks.
- This thesis demonstrated a step toward efficient, wideband DTXs, welcoming reconfigurable (multi-channel) communication with the potential effective data throughput from 100Mb/s up to 10Gb/s. Nevertheless, the chip-to-chip wire-line links that provide baseband data must be able to operate with equal flexibility. This demand intensifies the challenge of realizing high-speed, single-lane wire-line links for increasingly supply-limited technologies.
- To benefit more from the digital essence of the DTXs, and therefore their reconfigurability potential, artificial intelligence-assisted digital transmitters can be a future trend. Therefore, holistic design approaches need to be considered. Moreover, co-designing highly reconfigurable DTXs and AI/ML control algorithms offers various opportunities to enable reconfigurable, high-performance, robust operations by crossing different domains.

Appendix A

High-Speed Digital Interpolation Filters

This chapter comprehensively explains high-speed digital interpolation filters, which are utilized in this thesis.

A.1 Introduction

Generally, digital transmitters consist of three main units, namely the baseband processing or digital signal processing (DSP), sample-rate converter (SRC) or interpolation filter, and radio-frequency digital-to-analog converter (RF-DAC).

Figure A.1, demonstrates the simple block diagram of the digital I/Q TX. Accordingly, the four frequency variables are defined:

- The up-converting frequency of the RF-DAC, f_{RF} or f_0;
- The frequency of an on-chip local oscillator (LO), f_{LO};
- The up-sampling frequency of the SRC, f_{SRC};
- The sampling frequency of the DSP, f_B.

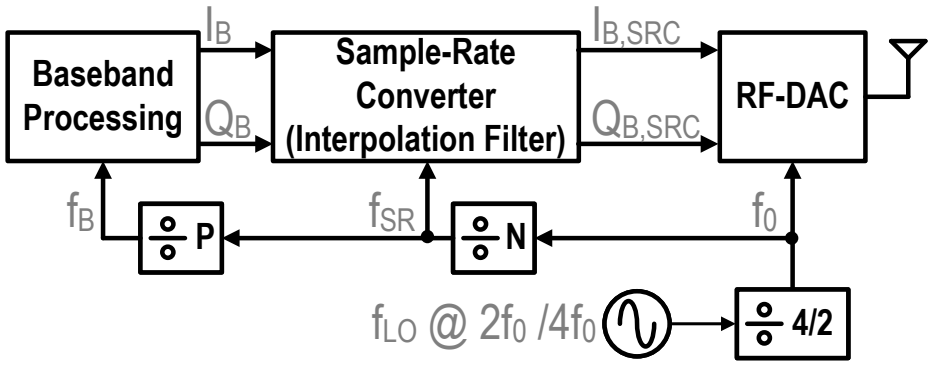


Figure A.1: Simple block diagram of digital I/Q TX.

In this context, the baseband signal of the in-phase digital baseband (I_B) and quadrature digital baseband (Q_B) are generated in the DSP unit while their corresponding sampling rate is f_B. I_B and Q_B signals are then fed to the SRC unit. This unit interpolates the aforementioned baseband signals. In other words, this unit is a sample-rate converter. The sampling frequency of the SRC unit is f_{SRC}. The up-sampling factor, or interpolation factor (L_{SRC}), is determined as follows:

$$L_{SRC} = \frac{f_{SRC}}{f_B} \tag{A.1}$$

In a conventional I/Q TX, the baseband signal is converted into an analog signal utilizing a digital-to-analog converter (DAC). This unit is a zero-order hold (ZOH) interpolator. Therefore, it produces spectral replicas at multiples of DAC's sampling frequency. In this context, the low-pass filter (LPF) is incorporated to suppress its corresponding spectral images. In the digital I/Q TX, however, LPF can not be exploited. Consequently, these replicas must be suppressed via the SRC unit. In other words, this unit with higher L_{SRC} causes these replicas to be far away from the desired operational frequency band. As a result, the eventual matching or power-combining network can easily restrain these spectral images.

A.2 System Considerations

According to Fig. A.1, all clocks in the digital baseband circuitry and the final RF fundamental clock are synchronized. As stated in [12], it is highly recommended to select f_{LO} to be $4\times f_0$. This selection can be explained as follows:

1. The energy of the LO resonating at $4\times f_0$ will not substantially leak to the fundamental frequency of the RF output;

2. The injection pulling of the fundamental frequency component of the RF output has a sufficiently weak $4\times f_0$ harmonic to disturb the LO resonant tank;

3. The $4\times f_0$ LO occupies less area than the $2\times f_0$ or even $1\times f_0$ LO due to its smaller inductor;

4. The divide-by-4 circuit is implemented using cascaded divide-by-two. Employing a divide-by-4 circuit will ameliorate the quadrature accuracy of the fundamental clocks since all the phases of the fundamental f_0 clock are derived from the same rising edge of the $4\times f_0$ master clock.

According to Fig. A.1, the up-sampling frequency of the SRC, f_{SRC}, as well as the sampling frequency of the DSP, f_B, are as follows:

$$f_{SRC} = \frac{f_0}{N} \tag{A.2}$$

$$f_B = \frac{f_{SRC}}{P} = \frac{f_0}{N \times P} \tag{A.3}$$

The f_{SRC} and f_B selections strongly depend on the types of SRC structure. This chapter concentrates on four simple interpolating digital filters, which will be discussed accordingly.

A.3 Interpolation Filters

A.3.1 Zero-Order Hold (ZOH)

The simplest type of interpolation filter is a ZOH. The up-sampled[1] I_B and Q_B are applied to a digital LPF of rectangular function[2]. Mathematically, the ZOH operation can be expressed as the convolution of the up-sampled signal with the boxcar function:

$$(I/Q)_{B,SRC}[n] = \text{upsample}\left((I/Q)_B[n]\right) * \Pi[n] \tag{A.4}$$

In the frequency domain, however, the rectangular function ($\Pi[n]$) performs as a digital LPF with a Sinc-shaped amplitude characteristic. In other words, the subsequent RF power spectrum is shaped by the Sinc function:

$$\text{Sinc}(f) = \text{sinc}^2\left(\frac{f - f_0}{f_B}\right) \tag{A.5}$$

Note that the ZOH operation creates spectral replicas at multiples of the sampling frequency, f_B, away from the f_0 carrier:

$$f_m = f_0 \pm m \times f_B \tag{A.6}$$

Where $m = 1, 2, \ldots$. In conclusion, the ZOH filter produces a Sinc-shaped filter in the frequency domain with its corresponding zeros located at f_m. As such, the spectral images are notched by the ZOH operation. Note that doubling f_B not only reduces the out-of-band emissions[3] but also lowers the amplitude of replicas by 6 dB.

A.3.2 First-Order Hold (FOH)

In order to reduce the amplitude of the related spectral replicas, a first-order hold (FOH) LPF digital filter is incorporated. The related digital LPF is a triangle function ($\Lambda[n]$) which can be obtained as the convolution of two identical $\Pi[n]$:

[1] The up-sampled signal with the up-sampling factor of L_{SRC} comprises original samples of the signal which are separated by (L_{SRC}-1) zeros.

[2] The rectangular function is a special case of the more general boxcar function.

[3] As in the sampling circuits such as analog-to-digital converter (ADC) and DAC, increasing the clock sampling rate by 2× will improve the quantization noise by 6 dB.

$$\Lambda[n] = \Pi[n] * \Pi[n] \tag{A.7}$$

In the FOH filter, the up-sampled I_B and Q_B are applied to a digital $\Lambda[n]$. Mathematically, the FOH operation can be expressed as the convolution of the up-sampled signal with $\Lambda[n]$:

$$(I/Q)_{B,SRC}[n] = \text{upsample}\left((I/Q)_B[n]\right) * \Lambda[n] \tag{A.8}$$

In the frequency domain, though, $\Lambda[n]$ performs as a digital LPF with a Sinc-to-power-of-two-shaped amplitude characteristic. In other words, the subsequent RF power spectrum is shaped by the Sinc2 function:

$$\text{Sinc2}(f) = \text{sinc}^4\left(\frac{f - f_0}{f_B}\right) \tag{A.9}$$

In this context, the FOH operation again creates spectral replicas at f_m frequencies indicated in A.6. Comparing A.5 and A.9, it is obvious that the suppression of FOH is superior to ZOH (see Fig. A.2(b)).

A.3.3 Second-Order Hold (SOH)

A second-order hold (SOH) digital filter is adopted so as to restrain the amplitude of the related replicas even more compared with the FOH counterpart. The related digital LPF is actually a quadratic function ($X^2[n]$) which can be obtained as the convolution of $\Pi[n]$ and $\Lambda[n]$ functions:

$$X^2[n] = \Pi[n] * \Lambda[n] \tag{A.10}$$

In the SOH filter, the up-sampled I_B and Q_B are applied to a digital $X^2[n]$. Mathematically, the SOH operation can be expressed as the convolution of the up-sampled signal with $X^2[n]$:

$$(I/Q)_{B,SRC}[n] = \text{upsample}\left((I/Q)_B[n]\right) * X^2[n] \tag{A.11}$$

In the frequency domain, though, $X^2[n]$ performs as a digital LPF with a Sinc-to-power-of-three-shaped amplitude characteristic. In other words, the subsequent RF power spectrum is shaped by the Sinc3 function:

$$\text{Sinc3}(f) = \text{sinc}^6\left(\frac{f - f_0}{f_B}\right) \tag{A.12}$$

In this context, the SOH operation again creates spectral replicas at f_m frequencies indicated in A.6. Comparing A.9 and A.12, it is obvious that the suppression of SOH is superior to FOH (see Fig. A.2(b)).

A.3.4 Third-Order Hold (TOH)

Finally, a third-order hold (TOH) digital filter is considered to overwhelm the amplitude of the related replicas even further compared with the SOH counterpart. The related digital LPF is simply a cubic function ($X^3[n]$) which can be obtained as the convolution of two identical $\Lambda[n]$ functions:

$$X^3[n] = \Lambda[n] * \Lambda[n] \tag{A.13}$$

In the TOH filter, the up-sampled I_B and Q_B are applied to a digital $X^3[n]$. Mathematically, the TOH operation can be expressed as the convolution of the up-sampled signal with $X^3[n]$:

$$(I/Q)_{B,SRC}[n] = \text{upsample}\left((I/Q)_B[n]\right) * X^3[n] \tag{A.14}$$

In the frequency domain, though, $X^3[n]$ performs as a digital LPF with a Sinc-to-power-of-four-shaped amplitude characteristic. In other words, the subsequent RF power spectrum is shaped by the Sinc4 function:

$$\text{Sinc4}(f) = \text{sinc}^8\left(\frac{f - f_0}{f_B}\right) \tag{A.15}$$

Under the condition presented, the TOH operation again creates spectral replicas at f_m frequencies indicated in A.6. Comparing A.15 and A.12, it is obvious that the suppression of TOH is superior to SOH (see Fig. A.2(b)).

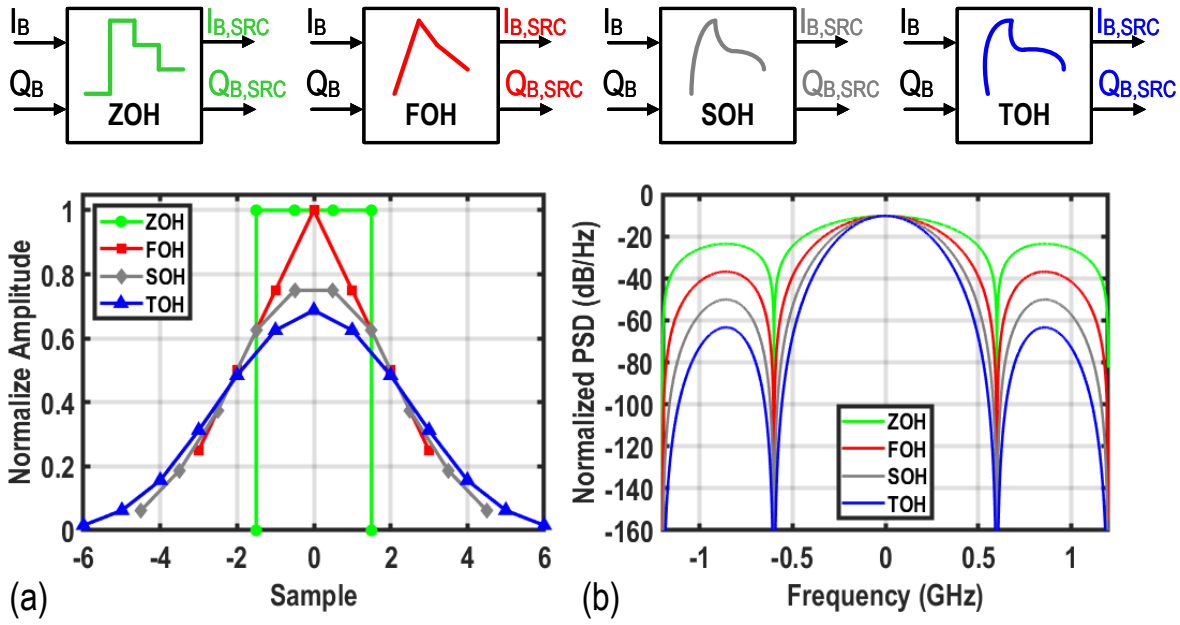


Figure A.2: (a) Impulse responses of ZOH, FOH, SOH, and TOH; (b) their corresponding frequency responses (L_{SRC}=4).

A.4 Impulse and Frequency Responses

Four types of interpolation schemes have been discussed in the previous sections. Fig. A.2(a) illustrates the impulse responses of ZOH, FOH, SOH, and TOH. The filters are deployed to up-sample the complex baseband signals at f_B by a factor of 4 up to f_{SRC}= f_0 and suppress the replicas located f_B away from the carrier below the modulator noise floor. The selection of f_B and the up-sampling factor balances the sampling spectral replicas (SSR) separation, data path power consumption, and the filter complexity. Fig. A.2(b) demonstrates their corresponding frequency responses, which indicate that TOH produces the best suppression of the image replicas among these four configurations. As a trade-off between the in-band amplitude distortion and out-of-band replica suppression, we can choose the ZOH, FOH, or SOH filters. For CA signals, (T)SOH should be selected as the amplitude roll-off distortion can be less important as the bandwidth of each channel relative to the aggregated bandwidth

is smaller. However, for single-carrier wideband signals, the in-band distortion can cause significant EVM degradation, requiring either to avoiding the SOH filter or using a digital pre-emphasis filter at the price of SSRs or complexity, respectively.

A.5 The Fundamental Equations for FIR Interpolation Filters

The impulse responses of the direct-form N-th order FIR filter [129] can be expressed as follows:

$$h[n] = \sum_{i=0}^{i=N} c_i \cdot \delta[n-i] = \begin{cases} c_i & 0 \leq n \leq N \\ 0 & \text{otherwise} \end{cases} \tag{A.16}$$

where c_i is the corresponding multiplier coefficient of each tapped delay line[4]. In other words, in a direct-form FIR filter, c_i is the filter's coefficient. In the case of a ZOH and up-sampling by a factor of N, c_i=1 and A.16 simplifies to $h_{ZOH}[n] = \sum_{i=0}^{i=N} \delta[n-i]$.

The FIR interpolation filter with an up-sampling ratio of L_{SRC} can be implemented in two different, well-known structure forms:

1. First, the input signal is up-sampled. The resultant signal is then passed through a low-pass filter (LPF) to smooth out the discontinuities[5].

2. In order to save power consumption and the filter cost, a poly-phase FIR filter can be exploited. It should be emphasized that the advantage of a poly-phase structure is the efficiently reduced arithmetic complexity and data storage.

Fig. A.3 illustrates and compares the previous approaches while the corresponding FIR filter is considered a 4×-FOH. The impulse responses of the corresponding triangle function ($\Lambda[n]$), i.e., FOH, in *direct-form* configuration are as follows:

[4]The input-output characteristic of a causal discrete-time FIR filter is $y[n] = \sum_{i=0}^{i=N} h_i \cdot x[n-i]$. The $x[n-i]$ are referred to as filter taps. Indeed, the direct-form FIR is a tapped delay line structure. Note that the N-th order FIR filter consists of N+1 filter taps.

[5]Note that, as indicated in the first report, the foregoing discontinuities are created in up-sampled operation due to the insertion of (L_{SRC}-1) zeros between each sample of the original input signal, i.e., $x[n]$.

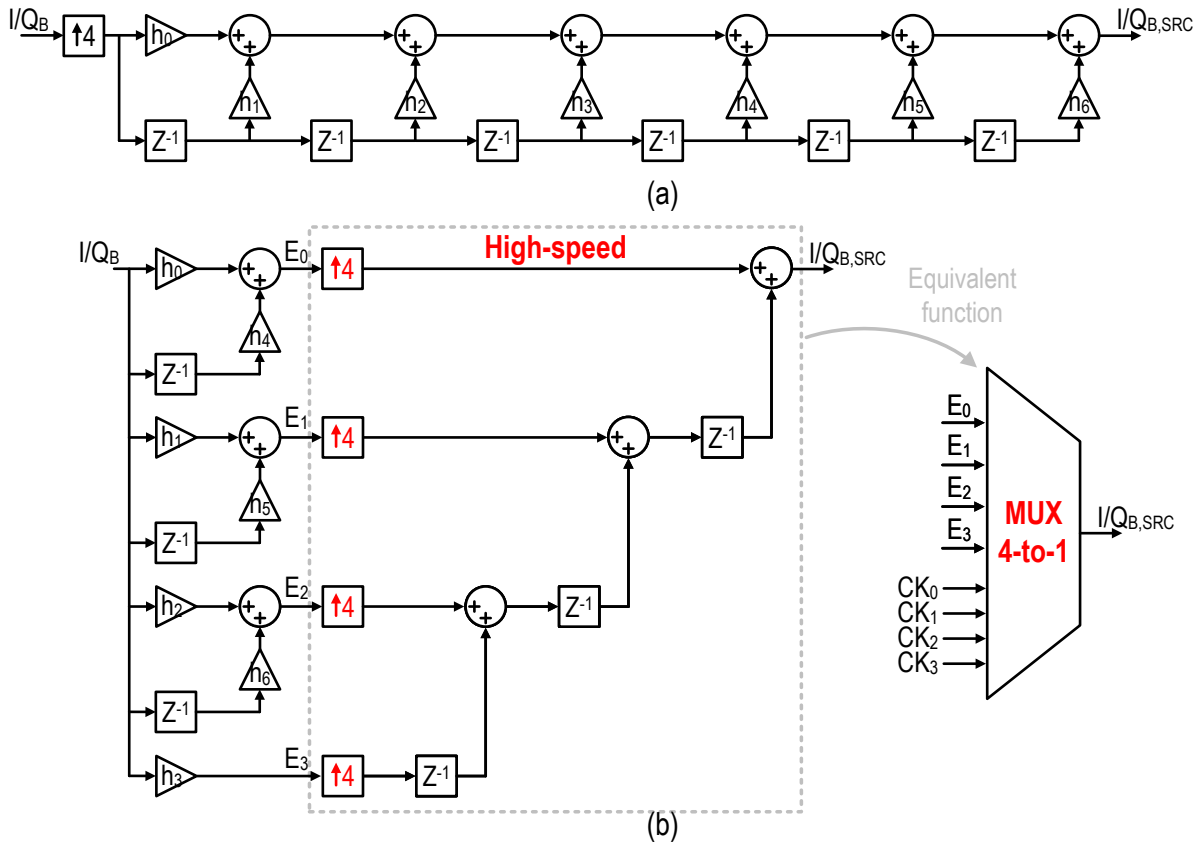


Figure A.3: Illustration of 4×-FOH (a) conventional direct-form FIR interpolation filter; (b) polyphase structure using high-speed delay elements; (c) corresponding 4-to-1 multiplexer used at high-speed section.

$$\begin{aligned} h_{\Lambda(4\times)}(n)\Big|_{DF} &= \sum_{i=0}^{i=n} c_i \cdot \delta[n-i] \\ &= c_0 \cdot \delta[0] + c_1 \cdot \delta[1] + c_2 \cdot \delta[2] + c_3 \cdot \delta[3] + c_4 \cdot \delta[4] + \\ &\quad c_5 \cdot \delta[5] + c_6 \cdot \delta[6] \end{aligned} \tag{A.17}$$

According to A.17 and Fig. A.3(a), the related 4×-FOH requires 7 multipliers, 6 adders, as well as 6 delay elements. All components are clocked at f_{SRC} frequency.

For N=4, the FOH coefficients are $c_3 = 1$, $c_{0...2} = c_{6...4} = 0.25$, 0.5, and 0.75. Similarly, the SOH coefficients are $c_{0...4} = c_{9...5} = 0.0625$, 0.1875, 0.375, 0.625, and 0.75 [59]. Note that deriving the coefficients in this manner, always results in only signed power-of-two terms, which can be implemented more power and area efficient using only adders and bit shift operation.

On the other hand, in poly-phase equivalent configuration, in order to save power/area, the corresponding FIR interpolation filter is decomposed into L_{SRC}, i.e., four parts. Each part consists of two sections; a low-speed part as well as a high-speed counterpart. The following mathematical equation expresses the "transfer function" of poly-phase 4×-FOH interpolation filter:

$$H_{\Lambda(4\times)}(z)\Big|_{PP} = E_0\left(z^4\right) + z^{-1}\cdot E_1\left(z^4\right) + z^{-2}\cdot E_2\left(z^4\right) + z^{-3}\cdot E_3\left(z^4\right) \tag{A.18}$$

where $z^{-1}...z^{-3}$ are only clocked at f_{SRC} and the rest, including $E_0...E_3$, are clocked at f_B. In Fig. A.3(b), this part can be discernible and is situated after 4× up-sampling components. Moreover, in A.18, $E_0...E_4$ can be expressed as follows:

$$\begin{aligned} E_0 &= h[0] + h[4]\cdot z^{-1} = c_0 + c_4\cdot z^{-1} \\ E_1 &= h[1] + h[5]\cdot z^{-1} = c_1 + c_5\cdot z^{-1} \\ E_2 &= h[2] + h[6]\cdot z^{-1} = c_2 + c_6\cdot z^{-1} \\ E_3 &= h[3] + 0\cdot z^{-1} = c_3 \end{aligned} \tag{A.19}$$

The previous A.19 represents the low-speed part of the related poly-phase FIR interpolation filter. As said previously, they are clocked at f_B as they are located before 4× up-sampling operations (see Fig. A.3(b)). Consequently, the poly-phase configuration consumes much less power than its direct-form equivalent.

It must be emphasized that the 4× up-sampling process generates three zeros and merely one sample of the input signal during one period of the baseband signal, i.e., $1/f_B$. As a result, the high-speed section of Fig. A.3(b) can be replaced by a 4-to-1 multiplexer (see Fig. A.3(c)). This modification makes the eventual poly-phase FIR interpolation filter even more compact. In other words, this conversion dramatically reduces the complexity of the higher-order poly-phase FIR interpolation filter. In this regard, the frequency of the multiplexer's control clocks, i.e., $CK_0...CK_3$, is f_B. Their corresponding duty cycle is 1/4, while

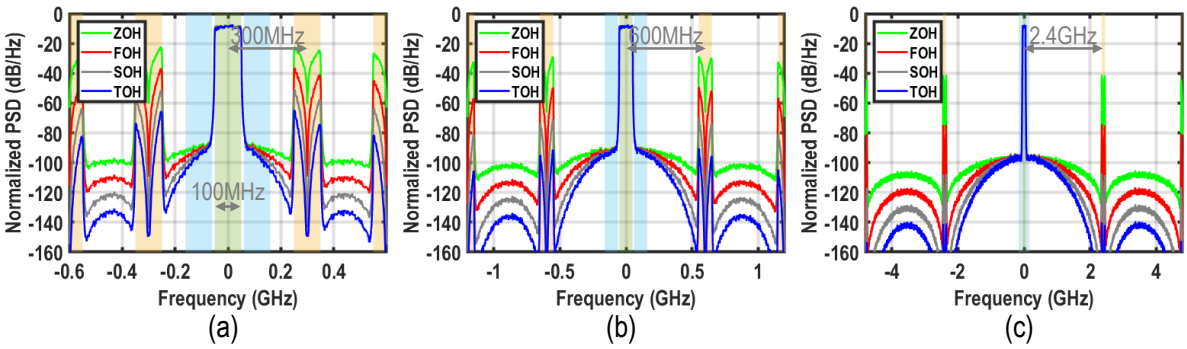


Figure A.4: Power spectral density of ZOH, FOH, SOH, and TOH interpolation filters applied to a pulse-shaped 256-QAM I/Q baseband signal with 100MHz bandwidth while their corresponding L_{SRC} is (a) 8, (b) 4, and (c) 1, respectively.

their relative phase difference is multiples of 90°. Note that the related sampling rate of the multiplexer output is f_0.

A.6 Power Spectral Density and Constellation Diagram

The up-sampling frequency of the SRC, f_{SRC}, and the sampling frequency of the DSP, f_B, can be selected based on how much the SRC unit can restrain its corresponding image replicas. Let us select f_{SRC} equal to the carrier frequency, i.e., f_{SRC}=f_0. As depicted in Fig.A.4(c), this selection guarantees that the spectral image level at the frequency of $2\times f_0$ would be as minimal as possible. In other words, the I/Q baseband signal interpolates to an "f_0" sample per second, and thus the related spectral image at $2\times f_0$ frequency will be notched[6]. However, the higher the SRC unit's operation frequency, the more power consumption increases. Therefore, if the SRC unit is not implemented properly, it can deteriorate the system efficiency.

Fig.A.4(a) and (b) depict the power spectral density (PSD) performance of the preceding four different interpolation filters while their corresponding up-sampling rates, L_{SRC}, are 8 and 4, respectively. The OFDM complex-modulated signal is selected as the I/Q baseband signal. Using A.2, for an up-converting frequency of f_0=2.4GHz, the corresponding sampling

[6]Sinc-shaped filter at multiple of sampling frequency away from f_0

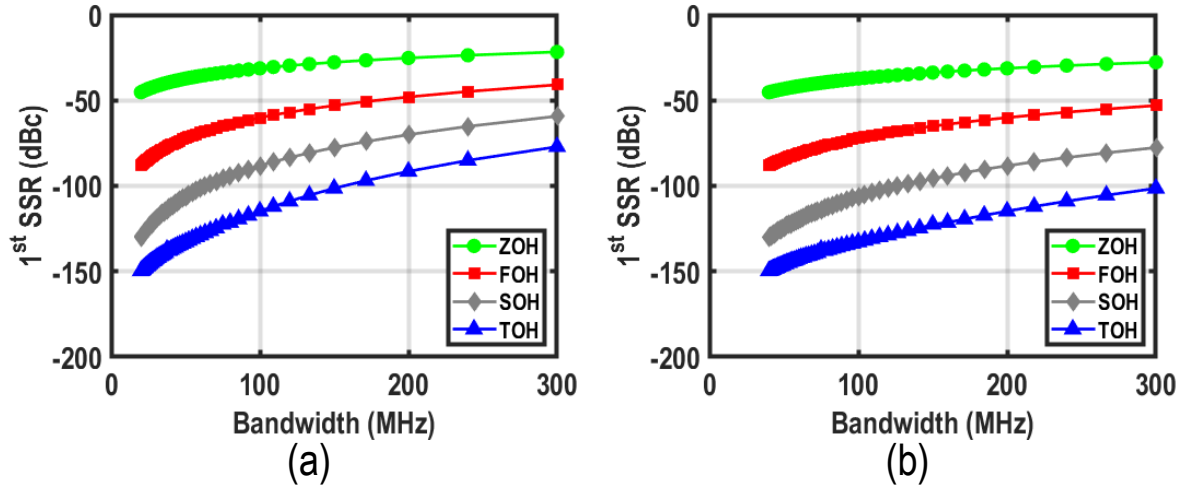


Figure A.5: First sampling spectral replica suppression performance of ZOH, FOH, SOH, and TOH interpolation filters applied to a pulse-shaped 256-QAM I/Q baseband depending on signal bandwidth while their corresponding L_{SRC} is (a) 8, and (b) 4.

frequency of the DSP, f_B, are 300MHz and 600 MHz, respectively. Generally, the sampling spectral replicas suppression is improved by increasing the sampling frequency.

FigureA.5(a) and (b) represent the simulation results of the first image replica suppression performance of ZOH, FOH, SOH, and TOH interpolation filters depending on the signal bandwidth while their corresponding L_{SRC} is 8 and 4, respectively. Accordingly, and as expected, the best replica image suppression is achieved by exploiting TOH. As clearly indicated in Fig.A.5(a), it is not impossible to opt FOH interpolation filter and obtain better than -41dBc of out-of-band spectra for a 300MHz signal bandwidth. Consequently, the TOH interpolation filter is the best option among these four filters. Based on the simulation results in Fig. A.5(a), if the TOH interpolation filter is selected, the out-of-band spectra of more than -77dBc is even possible using L_{SRC}=8.

In order to investigate this option, the system's error vector magnitude (EVM) is simulated and depicted in Fig. A.6. It seems that applying a very sharp TOH filter with L_{SRC}=8, which must restrain the spectral image replicas at multiples of f_B=300MHz away from f_0, deteriorates the in-band performance of the complex-modulated I/Q signal. On the other

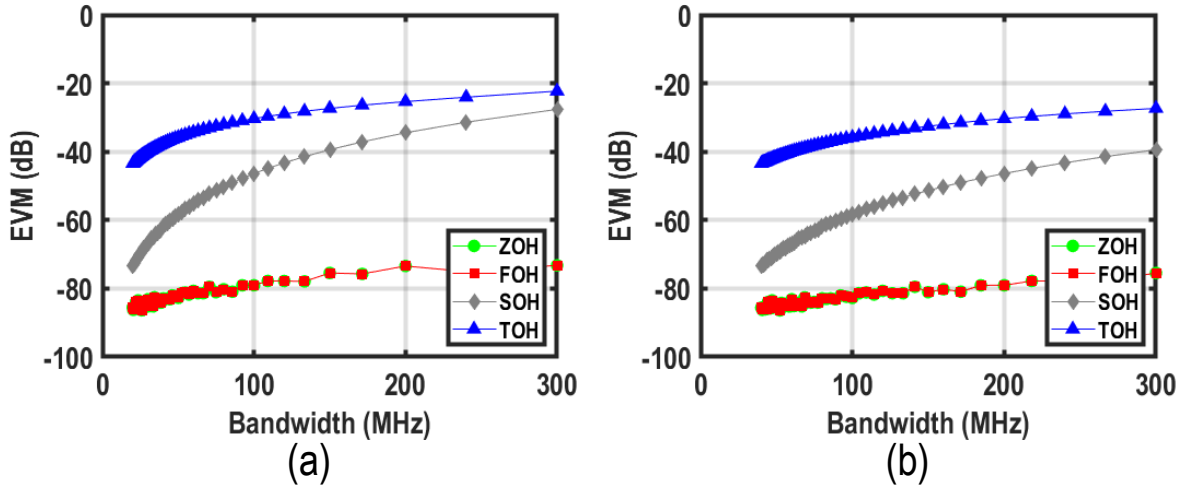


Figure A.6: EVM performance of ZOH, FOH, SOH, and TOH interpolation filters applied to a pulse-shaped 256-QAM I/Q baseband depending on signal bandwidth while their corresponding L_{SRC} is (a) 8, and (b) 4.

hand, if L_{SRC}=4 is selected, then the corresponding EVM will improve. Consequently, a TOH with L_{SRC}=4 can be selected as the SRC interpolation filter. Note that the in-band performance, EVM, of the linear interpolator filter, i.e., FOH, is -73dB indicating that if the I/Q bandwidth of the system is 300MHz while the f_B=600MHz is also selected, FOH would be the best choice. Generally, based on simulation results, the in-band performance of SOH and TOH is inferior compared to ZOH, and FOH, while their out-of-band spectra are superior.

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List of Acronyms

1D One-dimensional
2D Two-dimensional
2G Second Generation
3GPP 3rd Generation Partnership Project
5G Fifth Generation
ACLR Adjacent Channel Leakage-Ratio
ACPR Adjacent Channel Power-Ratio
ACW Amplitude-Code-Word
ADC Analog-to-Digital Converter
ADPLL All-Digital Phase-Locked Loop
AWGN Additive White Gaussian Noise
BPF Band Pass Filter
BW Bandwidth
Balun Balanced-unbalanced
BB Baseband
CA Carrier Aggregation
CL Carrier Leakage
CMCD Current-Mode Class-D
CMOS Complementary Metal-Oxide-Semiconductor
CORDIC COordinate Rotation DIgital Computer
CP Continuous Phase
CW Continuous Wave
DAC Digital-to-Analog Converter

DCO Digitally-Controlled Oscillator
DDS Direct-Digital Synthesizer
DE Drain Efficiency
DFE Decision Feedback Equalizer
DFF D Flip Flop
DNL Differential Non-Linearity
DPA Digitally Controlled Power Amplifier
DPBO Deep Power Back-Off
DPD Digital Predistortion
DR Dynamic Range
DRAC Digital-to-Radio-Frequency-Amplitude Converter
DSP Digital Signal Processing
DTX Digital Transmitter
EER Envelope-Elimination and Restoration
EM Electromagnetic
ET Envelope Tracking
EVM Error Vector Magnitude
FIR Finite Impulse Response
FOH First-Order-Hold
FTDI Future Technology Devices International
GFSK Gaussian Frequency-Shift Keying
HWTL Half Wave Transmission Line
I In-phase
IC Integrated Circuit
IF Intermediate Frequency
IIP_2 Second-order Intercept Point
IIP_3 Third-order Intercept Point
IM3 Third Inter-Modulation
IRF Image Rejection Filter
IRR Image Rejection Ratio
LDO Low-Drop-Out voltage regulator
LINC Linear Amplification using Nonlinear Components

LO Local Oscillator
LPF Low-Pass Filter
LSB Least Significant Bit
LTE Long-Term Evolution
MSB Most Significant Bit
NR New Radio
OFDM Orthogonal Frequency-Division Multiplexing
OOB Out-of-Band
OR Oversampling Ratio
PA Power Amplifier
PAE Power-Added Efficiency
PAPR Peak-to-Average Power-Ratio
PBO Power Back-Off
PDF Probability Density Function
$\mathbf{P_{DC}}$ Direct Current Power
$\mathbf{P_{Out}}$ Output Power
$\mathbf{P_{Sat}}$ Saturated Power
PLL Phase-Locked Loop
PN Phase Noise
PVT Process, Voltage, and Temperature
Q Quadrature
QAM Quadrature Amplitude Modulation
QWTL Quarter Wave Transmission Line
RF Radio Frequency
RF-DAC Radio Frequency Digital-to-Analog Converter
RRC Root Raised Cosine
RX Receiver
SAW Surface Acoustic Wave
SE System Efficiency
SEM Spectrum Emission Mask
SMPA Switched-Mode Power Amplifier
SOC System-on-Chip

SOH Second-Order-Hold
SOI Silicon On Insulator
SPI Serial Peripheral Interface
SRAM Static Random Access Memory
SRC Sample-Rate Converter
SSB Single-Sideband
SSR Sampling Spectral Replica
TL Transmission Line
TOH Third-Order-Hold
TX Transmitter
VCO Voltage-Controlled Oscillators
VGA Variable Gain Amplifier
VSA Vector Signal Analyzer
WLAN Wireless Local Area Network
ZOH Zero-Order-Hold

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Summary

The demand for faster mobile access and higher data throughput drives the evolution of wireless cellular communication, requiring larger modulation bandwidths and higher-order modulations and necessitating more efficient and flexible transmitter systems.

Simultaneously, the advancements in nano-scale CMOS technologies have made transistors smaller and better suited for digital signal processing, with improved high-frequency performance for RF mixed-signal circuits.

These advancements impact wireless RF transceivers creating the need to explore transmitter architectures beyond the level of the most established ones, which are exclusively analog up to date, by pushing them towards incorporating more digital circuitry. Consequently, the primary research question addressed in this is: "What are the potential performance advantages when the strength of (high-speed) digital CMOS is utilized within an RF front-end?"

To answer this research question, this thesis proposes new architectures for digital-intensive transmitter line-ups. These architectures aim to enhance linearity, bandwidth, and power efficiency, and enable the full utilization of CMOS technology in digital operations within the RF front-end.

Chapter 1 summarizes the development of modern communication standards and the advancements in nano-scale CMOS technology. It indicates that the rise of advanced CMOS technology has led to a growing interest in digital-intensive solutions over conventional analog-intensive alternatives.

Chapter 2 establishes the foundational knowledge required to understand the fundamentals of traditional transmitters and power amplifiers. It also briefly discusses the transition from analog-intensive to digital-intensive TX line-ups. Additionally, this chapter introduces

approaches for improving the efficiency of wireless systems when dealing with complex modulation signals, such as quadrature amplitude modulation (QAM) or orthogonal frequency division multiplexing (OFDM) signals.

Chapter 3 begins with a comprehensive comparison between signed and unsigned DTX operations. It then delves into an extensive system-level discussion of the principles behind signed Cartesian and multi-phase operations. Based on these discussions, a versatile transmitter that supports multi-mode/multi-band operation and enhances energy efficiency is demonstrated. The transmitter utilizes a digitally-configured architecture and features various modes, including Cartesian and multi-phase configurations, with different duty cycles of LO clocks in interleaving and non-interleaving configurations. The different modes of operation are mathematically analyzed, and their power and efficiency performances are compared. The chapter provides detailed information on the DTX architecture, circuit design and implementation, and off-chip matching network, along with extensive measurement results of the prototype. The results show that the multi-phase architecture inherits the advantages of the Cartesian DTX, such as wideband operation and symmetrical and synchronized I/Q paths, with a drain efficiency behavior similar to polar counterparts.

Chapter 4 combines the multi-mode operation approach introduced in Chapter 3 with an off-chip Doherty combiner to enhance the overall system efficiency over a wideband. The chapter presents the design, implementation details, and measurement results of the first-ever wideband multi-phase DTX in a two-way Doherty configuration. Multi-phase operation is employed to balance the polar and Cartesian characteristics by mapping the I/Q baseband signals into two non-orthogonal basis vectors with reduced relative phase difference, and magnitudes based on an appropriate I/Q mapping described in Chapter 3. This approach leads to reduced complex loading compared to a Cartesian DTX, resulting in a less phase-dependent efficiency behavior. The chapter also discusses the achievement of a wideband and efficient DTX through the use of a reactance-compensated parallel-circuit push-pull class-E digital power amplifier (DPA), combined with a wideband Marchand balun-based inverted two-way Doherty power combiner that exploits re-entrant coupled lines with independent second-harmonic control.

Chapter 5 elaborates on the considerations for system and circuit-level design and presents extensive measurement results of the first fully-digital four-way Doherty transmitter. It introduces two novel techniques: a 50%-LO signed I/Q interleaved up-converter and

a compact four-way Doherty combiner, aiming to achieve spectrally pure operation and enhance deep back-off efficiency. The limitations of conventional phase selector operation with different clock duty cycles are explained. The proposed signed I/Q interleaved up-converter addresses these issues by utilizing global 50%-LO clocks phase-modulated by the sign-bits, along with a new single-sideband I/Q digital up-converter. The DTX quadrant selection (sign-mapping operation) is accomplished in two steps: 1) Global 50% duty-cycle quadrature clock mapping and 2) Local I/Q up-conversion and I/Q interleaving. The chapter also comprehensively explains a systematic approach to designing a four-way power combining network. Moreover, the transmitter architecture is described, followed by a demonstration of the measurement results.

Chapter 6 provides essential knowledge about the non-linearities of digital transmitters and how to address them. It introduces a modified constellation-mapping digital predistortion (DPD) technique that simplifies the DPD process into individual 1-D mappings of the I and Q signals, i.e., 2×1-D. Due to the orthogonality of the I and Q paths, the DPD algorithm does not require an exhaustive 2-D search of the complete constellation diagram. The same DPD algorithm is applied to the four-way Doherty DTX (described in Chapter 5), and the measurement results are presented.

Chapter 7 summarizes the key findings of the dissertation and provides suggestions for future developments.

Samenvatting*

De behoefte aan een steeds sneller mobiel internet met hogere data capaciteit is de drijvende kracht achter de evolutie van draadloze netwerken. Grotere bandbreedten en geavanceerdere modulatietechnieken zijn dan ook nodig, welke steeds efficiëntere en flexibelere zendsystemen vereisen. Tegelijkertijd heeft de vooruitgang in nanoschaal-CMOS technologie ervoor gezorgd dat transistoren kleiner en beter geschikt zijn voor digitale signaalverwerking. Hiermee zijn verbeterde hoogfrequente prestaties mogelijk met analoog-digitaal-gemengde schakelingen.

Deze ontwikkelingen hebben veel invloed op de volgende generatie draadloze zendontvangers. Er is namelijk een toenemende noodzaak om naar nieuwe zenderarchitecturen te zoeken die gebruik maken van digitale schakelingen, ook op de plaatsen waar tot nu toe alleen maar analoge schakelingen gebruikt worden. De onderzoeksvraag van dit proefschrift is dan ook: "Wat zijn de te behalen prestatievoordelen als de kracht van digitale CMOS wordt benut in een hoogfrequent-zender?"

Om deze onderzoeksvraag te beantwoorden, worden er in dit proefschrift nieuwe digitaal-intensieve zenderarchitecturen geïntroduceerd die gebruik maken van (snelle) digitale CMOS-technologie om verbeteringen in: lineariteit, bandbreedte en vermogensefficiëntie van RF zenders te realiseren.

Hoofdstuk 1 vat de ontwikkeling van moderne communicatiestandaarden en de vooruitgang van nanoschaal CMOS-technologie samen. Het toont aan dat de opkomst van ge-

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avanceerde CMOS-technologie heeft geleid tot een groeiende interesse voor digitaal-intensieve oplossingen t.o.v. de conventionele analoog-intensieve alternatieven.

Hoofdstuk 2 geeft de basiskennis die nodig is om de werking van traditionele radiozenders en vermogensversterkers te begrijpen. Ook behandelt het beknopt de transitie van analoog-intensieve naar digitaal-intensieve zenders. Daarnaast geeft dit hoofdstuk een aantal methoden om de efficiëntie van draadloze systemen te verbeteren als deze werken met complex gemoduleerde signalen, zoals *quadrature-amplitude-modulation (QAM)*, of *orthogonal frequency-division multiplexing (OFDM)*.

Hoofdstuk 3 begint met een vergelijking van digitale zenders (DTX) die wel of geen extra voorteken (teken-bit) gebruiken om de polariteit van het zendsignaal te beschrijven. Het vervolgt met een discussie op systeemniveau over de beginselen van een cartesische zender met voorteken (*signed Cartesian*) en de meer-fase zender. Op basis van deze discussie wordt een radiozender geïntroduceerd die zowel meerdere modi als frequentiebanden kan ondersteunen bij een verbeterde energie-efficiëntie. Deze radiozender maakt gebruik van een digitale architectuur die zowel de cartesische, meer-fase en *interleaved* operatie met verschillende arbeidscycli van lokale oscillator (LO)-kloksignalen mogelijk maakt. Deze verschillende modi worden geanalyseerd, waarbij een vergelijking op basis van uitgangsvermogen en efficiëntie gemaakt wordt. Het hoofdstuk bevat verder informatie over de DTX-architectuur, het ontwerp, de bijbehorende realisatie, het externe impedantie-aanpassingsnetwerk en de meetresultaten van dit prototype. De resultaten tonen aan dat de meer-fase architectuur de voordelen van de cartesische werking bezit, zoals de breedbandwerking en symmetrische en gesynchroniseerde I/Q-paden, terwijl ook de *drain*-efficiëntie van de polaire zender wordt benaderd.

Hoofdstuk 4 combineert de multi-modus aanpak, zoals geïntroduceerd in hoofdstuk 3, met een extern Doherty-netwerk, om de systeemefficiëntie breedbandig te verhogen. Dit hoofdstuk geeft het ontwerp, de realisatie en de meetresultaten van de eerste gerapporteerde breedbandige meer-fase DTX in een tweeweg-Doherty-configuratie. Deze meer-fase operatie combineert de voordelen van zowel polaire als cartesische zenders, door de I/Q-basisbandsignalen af te beelden op twee niet-orthogonale vectoren met een kleiner faseverschil (zie ook hoofdstuk 3). Deze aanpak geeft, vergeleken met een cartesische DTX, een lagere reactieve belasting, wat de fase-afhankelijkheid van de efficiëntie vermindert. Hoofdstuk 4 behandelt ook een breedbandige energie-efficiënte DTX, die gebaseerd is op een geïnverteerd-

tweeweg-*push-pull*-klasse-E-Doherty-zender. Deze Doherty-zender maakt gebruik van een vermogenscombinatie-netwerk gebaseerd op een Marchand-*balun* met breedbandig gecompenseerde *re-entrant* gekoppelde lijnen met vrije controle over de tweede harmonische afsluiting.

Hoofdstuk 5 geeft 's werelds eerste volledig digitale vierweg-Doherty-zender met zijn ontwerpoverwegingen op systeem- en schakelingniveau en zijn meetresultaten. Het introduceert twee nieuwe technieken om een zuiver spectrum en verbeterde efficiëntie in *back-off* mogelijk te maken, namelijk: digitale frequentie-omvorming met 50% LO-klokken in combinatie met *signed-interleaved* I/Q operatie en een zeer compact vierweg-Doherty-netwerk. De beperkingen van de conventionele digitale frequentie-omvorming met kloksignalen van verschillende arbeidscycli worden besproken. De voorgestelde *signed-interleaved* I/Q operatie lost deze problemen op door gebruik te maken van 50% LO-klokken voor de globale klokdistributie die fase-gemoduleerd worden door de teken-bits, samen met een nieuwe enkelzijbands I/Q digitale frequentie-omvorming. De DTX-kwadrantselectie wordt bereikt in twee stappen: 1) kwadratuur klokafbeeldingen met 50% arbeidscyclus voor de globale klokdistributie; 2) lokale I/Q frequentie-omvorming en *interleaved* I/Q-operatie. Dit hoofdstuk geeft ook een systematische aanpak voor het ontwerpen van een vierweg-Doherty-netwerk, verder beschrijft het de zenderarchitectuur, gevolgd door de meetresultaten.

Hoofdstuk 6 geeft inzicht in de niet-lineariteiten van digitale radiozenders en hoe deze te corrigeren. Het introduceert een techniek voor digitale voorvervorming (DPD) door een afbeelding te maken van de constellatie, waarmee het DPD-proces vereenvoudigd kan worden tot twee individuele eendimensionale afbeeldingen van de I- en Q-signalen (2×1D). Door de orthogonaliteit van de I- en Q-signaalpaden hoeft het DPD-algoritme geen volledige 2D-afbeelding van het constellatiediagram te maken. Dit DPD-algoritme is toegepast op de vierweg-Doherty-DTX van hoofdstuk 5, de behaalde meetresultaten worden gerapporteerd en besproken.

Hoofdstuk 7 vat de belangrijkste conclusies van het proefschrift samen en geeft suggesties voor vervolgonderzoek.

List of Publications

Journals:

- **M. Beikmirza**, Y. Shen, L. C. N. de Vreede and M. S. Alavi, "A Wideband Energy-Efficient Multi-Mode CMOS Digital Transmitter," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 3, pp. 677-690, March 2023, doi: 10.1109/JSSC.2022.3222028.
- **M. Beikmirza**, Y. Shen, L. C. N. de Vreede and M. S. Alavi, "A Wideband Four-Way Doherty Bits-In RF-Out CMOS Transmitter," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3768-3783, Dec. 2021, doi: 10.1109/JSSC.2021.3105542.

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- **M. Beikmirza**, L. C. N. de Vreede and M. S. Alavi, "A Low-Complexity Digital Predistortion Technique For Digital I/Q Transmitters," *2023 IEEE/MTT-S International Microwave Symposium - IMS 2023*, San Diego, CA, USA, 2023.
- **M. Beikmirza**, Y. Shen, L. C. N. de Vreede and M. S. Alavi, "A Wideband Two-Way Digital Doherty Transmitter in 40nm CMOS," *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, Denver, CO, USA, 2022, pp. 975-978, doi: 10.1109/IMS37962.2022.9865506.
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Mohammad Reza Beikmirza
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About the Author

Mohammadreza Beikmirza received the B.Sc. and M.Sc. degrees in electrical engineering from the Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran, in 2014 and 2016, respectively. He is currently pursuing a Ph.D. degree with the Delft University of Technology, Delft, The Netherlands. His current research interests include digital-intensive transmitters and RF/monolithic microwave integrated circuits and systems design.

He was the recipient of the Amirkabir University of Technology best undergraduate thesis award 2015, IEEE Iran section best undergraduate thesis award 2015, Platinum award (first place) of the Huawei RFIC Contest 2021, and a co-recipient of the ISE president best paper award 2021.

Propositions

accompanying the thesis

Advanced Bits-In RF-Out Transmitters

By

Mohammadreza Beikmirza

1. A digital-intensive RFIC design can perform very close to its theoretical description. However, the radiated signals are analog. Chapters 1 and 2 in this thesis.

2. The multi-phase TXs employ the linear vector summation as in Cartesian TXs, preserving signal integrity for wideband operation while mimicking polar drain efficiencies. See this thesis in chapters 3 and 4.

3. The advent of digital-intensive approaches enables the reinvention of old architectures such as Doherty. This thesis chapters 4 and 5.

4. Artificial intelligence has the potential to turn regular humans using it, into superhumans. However, just like “with great power comes great responsibility,” AI must be used responsibly and ethically to profit from its benefits while avoiding the temptations of its “dark side”.

5. Corona pandemic liberated many jobs and events from their geographic location. This liberation should be preserved for international conferences that should (continue to) allow both physical and virtual attendance.

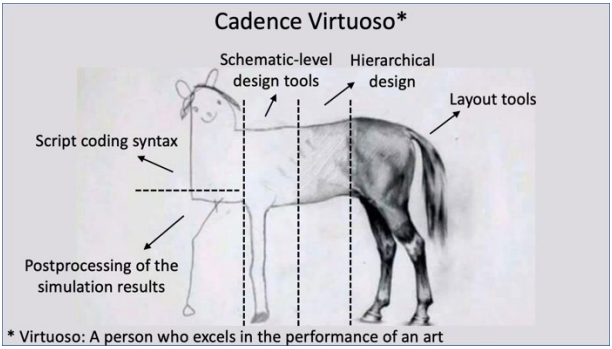
6. The bigger the project, the more co-authors are included in the paper, but not necessarily more scientific contributions are added.

7. The only thing that seems to be distributed adequately in the world is intelligence since no one complains about having (much) less than others.

8. Social Media introduced their first lie by their given name.

9. During your Ph.D. study, it is better to do a little that is continued with passion than a lot going nowhere.

10. Virtuoso from Cadence is a true “virtuoso” for full-custom IC design in layout and hierarchical levels. However, it loses its talent as it proceeds further in schematic-level design tools, easy-to-use coding, and simulation results postprocessing.



11. As AI becomes more sophisticated, it raises questions about the added value of providing propositions with a Ph.D. dissertation, as AI will eventually surpass humans in their ability to generate novel and thought-provoking ones.

    As an example, below are propositions generated by chatGPT about the relationship between Ph.D. students and advisors:

    - Ph.D. students and their advisors have a love-hate relationship. The students love their advisors for their endless support, guidance, and opportunities for growth. The advisors, on the other hand, hate the students for the endless revisions, rewrites, and late-night email reminders.

    - Ph.D. students and their advisors have a symbiotic relationship, much like that of a clownfish and anemone - the advisor provides protection and support, while the Ph.D. student adds color and excitement to the academic world.

These propositions are regarded as opposable and defendable, and have been approved as such by the promotor Prof. dr. L.C.N. de Vreede and copromotor dr. M.S. Alavi