# Thermomechanical Oriented Reliability Enhancement of Si MOSFET Panel-Level Packaging Fusing Ant Colony Optimization With Backpropagation Neural Network

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# Thermomechanical Oriented Reliability Enhancement of Si MOSFET Panel-Level Packaging Fusing Ant Colony Optimization With Backpropagation Neural Network

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***Abstract*— Considerable advancements in power semiconductor devices have resulted in such devices being increasingly adopted in applications of energy generation, conversion, and transmission. Hence, we proposed a fan-out panel-level packaging (FOPLP) design for 30-V Si-based metal–oxide–semiconductor field-effect transistor (MOSFET). To achieve superior reliability of packaging, we applied the nondominated sorting genetic algorithm with elitist strategy (NSGA-II) and ant colony optimization–backpropagation neural network (ACO–BPNN) to optimize the design of redistribution layer (RDL) in FOPLP. We first quantified the thermal resistance and thermomechanical coupling stress of the designed package under thermal cycling loading. Next, NSGA-II and ACO–BPNN were used to optimize the size of the RDL blind via. Finally, the effectiveness of the proposed reliability optimization methods was verified by performing thermal shock reliability aging tests on the prepared devices.**

***Index Terms*— Ant colony neural network, fan-out panel-level packaging (FOPLP), genetic algorithm, power device, reliability optimization.**

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## I. Introduction

With the demand for lower carbon emission, highly efficient power semiconductors are being increasingly adopted in energy generation, conversion, and transmission systems. Such power semiconductor devices are being used in high-speed train traction systems, electric vehicles and their charging stations, aircraft and spacecraft, renewable energy generation and smart power grid, air conditioning, and house appliances [1]. Because of the safety-critical nature of these applications and the typical power semiconductor device failures in power electronics systems [2], stringent reliability requirements have been proposed for device packaging [3]. The high switching speed, low switching loss, and high switching frequency of metal–oxide–semiconductor field effect transistor (MOSFET) power devices have considerably improved the power density and efficiency of power electronics systems. However, these attributes and applications of MOSFETs in power electronic systems are highly relied on package-level reliability [4], [5], [6], [7]. The commonly used discrete device packaging technology is transistor outline (TO) packaging, and module packaging technologies include planar interconnection, press pack, chip embedded package, 3-D interconnection, and hybrid package [8], [9].

The small-sized power MOSFETs exhibit a reduced switching loss at high temperatures, unlike its insulated gate bipolar transistor (IGBT) counterpart. Therefore, in this study, a fan-out panel-level packaging (FOPLP) design was proposed for a 30-V Si-based power MOSFET. FOPLP is one of the novel electronics packaging technologies in which printed circuit board (PCB) processing is combined with chip packaging [10]. In this case, the conventional bonding wire is replaced by the redistribution layer (RDL) to reduce parasitic inductance and ON-state resistance. Next, double-sided cooling is adopted to reduce thermal resistance, improve the heat dissipation performance of the package, and realize the miniaturization of the package size. However, the rising of potential risk in RDL under thermomechanical coupling loading should be minimized to guarantee the package-level reliability.

As one of the most popular multiobjective optimization algorithms, the nondominated sorting genetic algorithm with

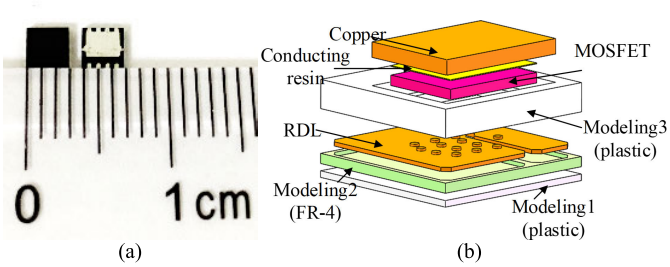


Fig. 1. (a) FOPLP MOSFET power devices. (b) Its 3-D model.

elitist strategy (NSGA-II) has demonstrated significant performance improvements in solving efficiency [11], which can produce a number of high-quality solutions in a single run. Besides, NSGA-II has become a benchmark algorithm to evaluate the other multiobjective optimization algorithms [12]. Ant colony and genetic algorithms are the most commonly used optimization methods in electronics package reliability. Multiobjective optimization algorithms are always combined with a finite-element (FE) simulation to optimize packaging materials, structures, and processes, in which the FE simulation is used to calculate the fitness function values, and the result is then optimized by an appropriate algorithm [13]. Implementing these optimization methods in a simple packaging structure is relatively easy because of fast computation speed and low computer memory requirement. However, they have many limitations in solving the reliability optimization of advanced packages with complex structures under multiphysics working conditions.

In this study, a thermomechanical coupling model was first constructed to quantify RDL thermal resistance and thermomechanical stress of a designed FOPLP MOSFET power device. Next, to improve the optimization computational efficiency, the genetic algorithms and ant colony algorithm were proposed to optimize the size of RDL blind via. Finally, the effectiveness of the proposed optimization methods was verified by performing thermal shock aging tests on the reliability-enhanced packages as designed.

## II. Two-Objective Optimization With Nondominated Sorting Genetic Algorithm

In this section, the packaging process of the designed FOPLP MOSFET was introduced. Then, thermal resistance and thermomechanical stress function were built. Finally, the NSGA-II algorithm is proposed to optimize the RDL size for reducing the steady-state thermal resistance and thermomechanical stress.

### A. Packaging Process of the FOPLP MOSFET Power Device

As shown in Fig. 1(a), the prepared FOPLP MOSFET power device is a small-sized package with a width of less than 3 mm. Its 3-D model is shown in Fig. 1(b), which consists of a Si MOSFET chip, RDL, Cu heat dissipation plate, plastic molding 1 and 3, and FR4 molding 2.

The packaging process of the FOPLP MOSFET power device is shown in Fig. 2.

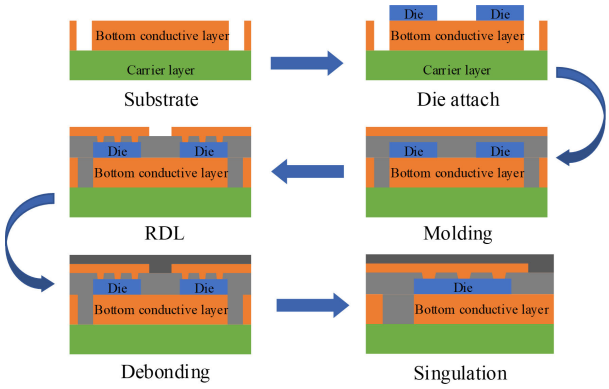


Fig. 2. Packaging process of the FOPLP MOSFET power device.

TABLE I
Properties of the Materials Used in the Packaging

| Material | Modulus $E$ (GPa) | Poisson ratio $\nu$ | Coefficient of thermal expansion $\alpha$ (ppm/K) | Thermal conductivity $k$ (W/mK) |
|---|---|---|---|---|
| Si | 131 | 0.3 | 4.1 | 124 |
| Plastic | 9 | 0.35 | 28 | 0.65 |
| FR-4 | 20.4 | 0.11 | 12.5 | 0.38 |
| Conducting resin | 4.41 | 0.3 | 40 | 2.5 |
| Cu | See[17] | 0.36 | 17 | 390 |

1) The bottom conductive layer was mounted on the carrier.
2) The Si MOSFET die with drain–source voltage $V_{DS}$ = 30 V, ON-state resistance $R_{DS(ON)}$ = 3.7 mΩ, and size = 1.96 × 1.5 mm was fixed on the bottom conductive layer by conductive resin.
3) The plastic encapsulation material and copper foil were molded on the carrier.
4) The vias were established by drilling through the plastic encapsulation material and copper foil using a laser drilling system, and then, the copper was filled into the vias by metal deposition and plating, therefore forming the RDL.
5) The surface heat-sink layer was pressed with a plastic sealing material.
6) The bottom carrier layer was removed, the solder pads on the surface of the device were treated with electroplating tin, and the board is cut into individual devices.

The mechanical and thermal properties of the materials used in the packaging are listed in Table I [14], [15]. As Young's modulus of metal changes with temperature, we assign six Young's moduli to the RDLs at temperatures of −38 °C, 0 °C, 38 °C, 76 °C, 114 °C, and 152 °C, which covered the temperature range of thermal cycling. Young's moduli of copper-based RDL at various temperatures are referred from [16] and [17].

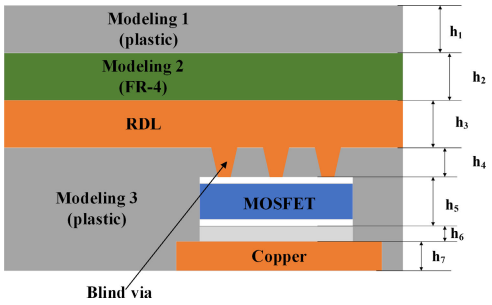


Fig. 3. Cross section of the FOPLP MOSFET power device.

### B. Steady-State Thermal Resistance Modeling

As shown in Fig. 3, the embedded device has two paths to transfer the heat, which can be regarded as a parallel thermal resistance with the upper and lower parts. The total thermal resistance $R_0$ can be expressed as follows:

$$R_0 = \frac{R_{\text{up}} \times R_{\text{down}}}{R_{\text{up}} + R_{\text{down}}} \tag{1}$$

where $R_{\text{up}}$ is the thermal resistance of the upward heat transfer of the module and $R_{\text{down}}$ is the thermal resistance of downward heat transfer of the module.

By considering the thermal spreading effect [13], the thermal resistance ($R_d$) of one-way heat transfer in the power device can be expressed as follows:

$$R_d = \sum_{i=1}^{n} \frac{h_i}{k_i A_i} \tag{2}$$

where $n$ is the number of layers of packaging and $h_i$, $k_i$, and $A_i$ are the thickness, thermal conductivity, and equivalent heat transfer area of the $i$th layer, respectively.

As shown in Fig. 3, two layers exist for the corresponding $R_{\text{down}}$ in this device. According to (2), $R_{\text{down}}$ can be expressed as follows:

$$R_{\text{down}} = \sum_{i=6}^{7} \frac{h_i}{k_i A_i}. \tag{3}$$

Taking the following thermal spreading effect into consideration, the equivalent heat transfer area $A_6$ can be expressed by the following equation:

$$A_6 = \left(l_c + \frac{k_5 h_6}{k_6}\right)^2 \tag{4}$$

where $l_c$ is the side length of the die in the package.

In this study, the thermal resistance calculation of blind vias layer can be simplified by separating the blind via from the molding and then calculating the parallel thermal resistance between the molding and the blind vias. The thermal resistance of the blind via part can be approximated as follows:

$$R_m = \frac{h_4}{k_3 A_m} \tag{5}$$

where $R_m$ is the thermal resistance of the blind via and $A_m$ is the contact area between the blind via and the chip.

Because the heat transfer area of the blind via overlaps with the above equivalent heat transfer area $A_4$, the thermal resistance of the molding layer $R_g$ can be obtained as follows:

$$R_g = \frac{h_4}{k_4 A_4}. \tag{6}$$

Therefore, we have the following expression on $R_{\text{up}}$:

$$R_{\text{up}} = \sum_{i=1}^{3} \frac{h_i}{k_i A_i} + \frac{R_m \times R_g}{R_m + R_g}. \tag{7}$$

Total thermal resistance $R_0$ can be calculated by substituting $R_{\text{up}}$ and $R_{\text{down}}$ into (1).

### C. Thermomechanical Stress Modeling

The failure of the power device packaging caused by the temperature cycle is related to the volume average inelastic working energy density ($W$), which can be described by the Darveaux model [18], [19] as follows:

$$\begin{cases} N_0 = \lambda_1 W^{\lambda_2} \\ da/dN = \lambda_3 W^{\lambda_4} \end{cases} \tag{8}$$

where $N_0$ is the number of thermal cycles for generating the initial crack, $\lambda_1$–$\lambda_4$ are the fitting coefficients, $a$ is the length of the characteristic crack, and $a_c$ is the width of the chip.

$W$ is related to the stress ($F$) generated in the cycle, and the function is shown as follows:

$$F = \frac{V_i}{\Delta h_i} W \tag{9}$$

where $V_i$ and $\Delta h_i$ are the volume and the deformation value of the $i$th layer, respectively.

In the power device, $\Delta h_i$ caused by the thermal expansion can be expressed as follows:

$$\alpha_i = \frac{\Delta h_i}{h_i \Delta T} \tag{10}$$

where $\alpha_i$ is the thermal expansion coefficient of the $i$th layer. The stress $F_i$ caused by thermal expansion satisfies the following expression:

$$\begin{aligned} E_i &= \frac{F_i h_i}{S_i \Delta h_i} \\ \Rightarrow F_i &= \frac{E_i S_i \Delta h_i}{h_i} = E_i S_i \alpha_i \Delta T \end{aligned} \tag{11}$$

where $E_i$ is Young's modulus of the $i$th layer. Finally, based on a single-blind via, the volumetric average inelastic working energy density can be expressed as follows:

$$\begin{aligned} W_i &= \frac{F_i \Delta h_i}{V_i} \\ \Rightarrow W_i &= \frac{E_i \alpha_i \Delta T S_i \Delta h_i}{\frac{1}{4}\pi d^2 h_i} \\ &= 8 E_i \alpha_i^2 \Delta T^2 \left(1 + \frac{2h}{d}\right) \end{aligned} \tag{12}$$

where $d$ is the small basal diameter of cone-shaped via.

TABLE II
SIZE RANGE OF RDL BLIND VIA

| Dimension | Lower limit (μm) | Upper limit (μm) |
|---|---|---|
| $h$ | 30 | 55 |
| $d$ | 80 | 140 |

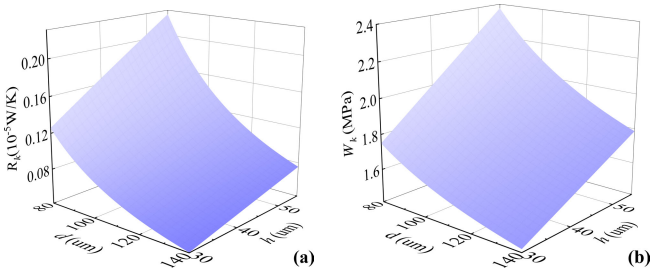


Fig. 4. Surface contour of (a) $R_k$ versus $d$ and $h$ and (b) $W_k$ versus $d$ and $h$.

### D. Multiobjective Optimization

The depth and diameter of the RDL blind via are used as optimization variables. Decreasing both the steady-state thermal resistance and thermomechanical stress is the objective. The multiobjective optimization mathematical model of power device packaging is established and can be expressed as follows:

$$\begin{cases} \min R_k \\ \min W_k \\ h_{\min} \le h \le h_{\max} \\ d_{\min} \le d \le d_{\max} \end{cases} \tag{13}$$

where $R_k$ is the thermal resistance of the RDL blind via layer, $W_k$ is the volume average inelastic working energy density, $h$ is the depth of the blind via, and $d$ is the diameter of the blind via. The range of $d$ and $h$ is shown in Table II.

NSGA-II algorithm is a global optimization algorithm that can resolve the linear and nonlinearity mathematical problem. NSGA-II algorithm was selected in this study for the reason that we expect that the proposed multiobjective optimization method can realize more complex packaging designs. The parameters for NSGA-II were initially selected according to [20] and [21], and then, they were adjusted for this study. The final parameters are set as follows: the optimal frontier individual coefficient is 0.6, the population size is 100, and the maximum iteration step is 10 000. To guarantee convergence of the algorithm, the maximum number of iteration steps is set as the individual coefficient of the larger optimal front and is expressed as the proportion of the individuals in the optimal front of the population. These values range from 0 to 1 and do not affect the solution result and the population size, and they are just the presentation form of the solution. Finally, the coefficient of 0.6 is selected to present a superior multiobjective optimization front. The optimal solution calculated by NSGA-II is that $d$ is 140 $\mu$m and $h$ is 30 $\mu$m. Fig. 4 presents the surface contour relationship between $R_k$, $W_k$, $d$, and $h$.

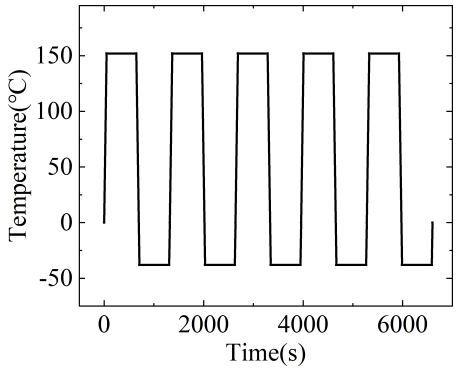


Fig. 5. Thermal cycling condition set based on JESD22-A106B.

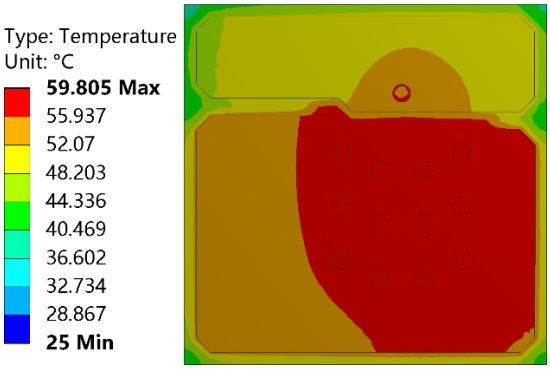


Fig. 6. Thermal dissipation simulation result on Si MOSFET chip.

## III. Optimization Design With Ant Colony Optimization–Backpropagation Neural Network

In this section, its thermal dissipation and thermomechanical stress are first simulated with ANSYS FE simulation. Then, with the assistance of the ant colony optimization–backpropagation neural network (ACO–BPNN) method, the RDL size is optimized accordingly.

### A. Simulation Condition

Referring to the JEDEC JESD22-A106B [22], Fig. 5 shows the thermal cycling conditions selected for this study. A temperature range of −38 °C to 152 °C and 60 s of the conversion time between high and low temperatures are set. Besides, a total of five thermal cycles are simulated.

### B. Thermal Dissipation Simulation

The internal thermal conductivity structure of the prepared FOPLP MOSFET power device is described in Section II. In the thermal simulation, the Si MOSFET chip is the heat source with an estimated power loss of 35.7 W. The simulation begins at 25 °C, with convective heat transfer coefficient set at 15 W/m$^2$·°C. Fig. 6 shows the heat dissipation simulation result for the prepared FOPLP MOSFET power device, in which the junction temperature of Si MOSFET chip is estimated at about 60 °C.

### C. Thermomechanical Simulation

Fig. 7 presents a thermomechanical simulation result of stress distribution on RDL during thermal cycling. The maximum stress occurred at the edges of the RDL. It can be

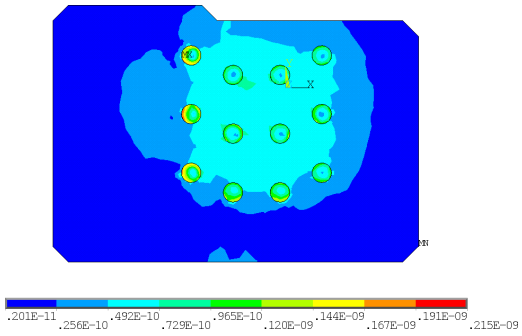


Fig. 7. Plastic work distribution on RDL during the thermal shock test.

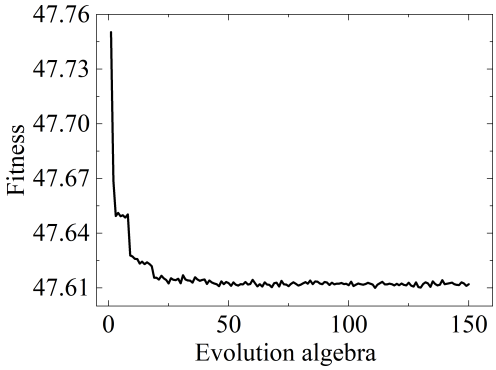


Fig. 8. Fitness evolution curve.

seen that the produced heat from the Si MOSFET chip intensively affects the RDL because it is directly attached to the die. Furthermore, the difference of coefficient of thermal expansion (CTE) between plastic, Si, and copper is the root cause to generate thermomechanical stress, which will result in interface delamination [22].

The plastic deformation of the Cu-based RDL under thermomechanical coupled loading belongs to the main reliability issue for FOPLP packaging devices. Because of the indirect contact between Cu and Si chips in the packaging structure and the apparent difference in CTE, the thermal shock test will take an adverse effect on the interconnection between the Cu column and the Si MOSFET chip, which causes the failure of the device.

### D. ACO–BPNN

The ACO–BPNN method used in this study was conducted in MATLAB R20121a. The steps of ACO–BPNN were described as follows. First, an ACO algorithm is used to determine the value of independent variables. Next, the fitness value is calculated, and the ACO neural network prediction algorithm is used to predict the junction temperature of Si MOSFET chip and the plastic work on RDL. Finally, the prediction results are fed back to the optimization algorithm, and the iteration continues.

In this study, we conducted 150 simulations as the training set of the neural network, and those simulations covered all size ranges of blind vias. The temperature and stress with each blind via were obtained according to our training set through the ACO algorithm iteration. The input data for the neural network model are $d$ and $h$ of each RDL blind via, and the outputs are corresponding plastic work and junction temperature. Other considerations for the model include the number of hidden layers = 9, the number of nodes at each of the hidden layers = 3, the maximum number of network training = 1000, and the minimum mean square error = 0.00004. A stochastic gradient descent (SGD) optimization algorithm was used for training the model and the learning rate = 0.01.

The operation of the ACO algorithm is detailed as follows.

*Step 1 (Initializing Algorithm Parameters):* The parameters of algorithm were initialized as follows: 1) the number of ants $m$ is 20; 2) the maximum number of iterations $G$ is 150; 3) the pheromone evaporation coefficient *Rho* is 0.9; 4) the transfer probability constant $P_0$ is 0.2; and 5) the step size of the local search step is 0.1.

*Step 2 (Generating the Ant's Initial Position):* The value of its fitness function was calculated and set as the initial pheromone path, and next, we calculated the transition state probability.

*Step 3 (Updating Ant Location):* The ant location in the colony was updated by conducting a local search when the state transition probability was less than the transition probability constant. The global search was then undertaken to generate new ant locations, and boundary conditions were processed using the boundary absorption method. Finally, we updated the ant location within range.

*Step 4 (Calculating the New Ant Location's Fitness):* The new ant location's fitness was calculated to determine whether an ant had moved. The pheromone path was updated if the movement was detected.

*Step 5 (Processing Iteration):* Stopped the process and considered the optimized value as an output if the termination condition was satisfied; otherwise, the process continued.

Next, through the iteration of the ant colony algorithm, the path with the highest concentration of accumulated pheromone was determined to obtain the optimal solution. The fitness evolution curve obtained by iteration is shown in Fig. 8.

The optimization results of ACO–BPNN method reveal that the optimal heat dissipation with the junction temperature of 46.52 °C and plastic work with the thermomechanical stress of $1.27 \times 10^{-10}$ MPa were obtained when the diameter $d$ and depth $h$ of RDL blind via were 140 and 30 $\mu$m, respectively. The effect of optimization is described in Table III. The proposed ACO–BPNN method can lower the junction temperature by 3.2% and plastic work by 14.8%, compared to the

TABLE III
COMPARISON OF THE JUNCTION TEMPERATURE AND CUMULATIVE PLASTIC WORK BEFORE AND AFTER OPTIMIZATION BY THE ACO–BPNN METHOD

| performances | Before optimization | After ACO-BPNN | Percentage improvement by ACO–BPNN |
|---|---|---|---|
| Junction Temperature $T_j$ (°C) | 48.06 | 46.52 | 3.2% |
| Plastic work $W$ ($10^{-10}$MPa) | 1.49 | 1.27 | 14.8% |

TABLE IV
TEST SAMPLES WITH DIFFERENT RDL DESIGNS

| No. | RDL designs | sample quantity |
|---|---|---|
| Group 1 | $h$=30um, $d$=80um | 10 |
| Group 2 | $h$=30um, $d$=120um | 10 |
| Group 3 | $h$=30um, $d$=140um | 10 |
| Group 4 | $h$=55um, $d$=80um | 10 |
| Group 5 | $h$=55um, $d$=120um | 10 |
| Group 6 | $h$=55um, $d$=140um | 10 |

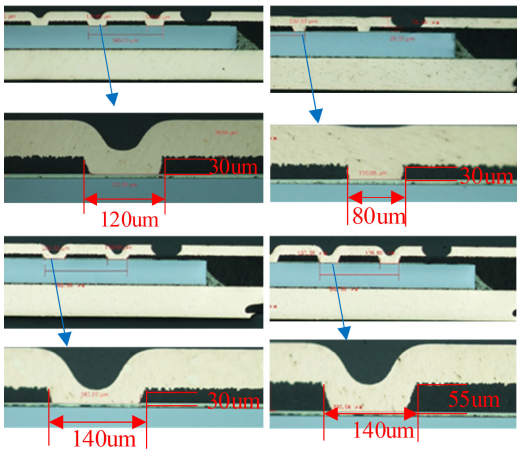


Fig. 9. Different designs of RDL blind via.

benchmark structure with $h = 40\ \mu$m and $d = 80\ \mu$m. Thus, $d$ is negatively correlated with the cumulative plastic work, while $h$ is positively correlated with the cumulative plastic work, which is consistent with the optimization results by NSGA-II.

## IV. EXPERIMENTAL RESULTS AND DISCUSSION

### A. Test Sample Preparation and Aging Experiment

To verify the proposed optimization methods' effectiveness, six group samples with various RDL sizes were designed and fabricated. The selected $h$ and $d$ were agreed with the range listed in Table II, which includes the initial and optimized structures. The RDL designs are listed in Table IV. The cross-sectional morphologies of RDL are shown in Fig. 9. Six group samples with ten devices in each group were subjected to a thermal shock test.

The scheme of thermal shock reliability aging test is described as follows: a thermal shock test chamber (HITACHI, EC-106MHHP, Japan) was used to conduct the aging test on the aforementioned six groups of power devices. The test condition is the same as shown in Fig. 6, and the electrical measurements were conducted after every 400 cycles until 1200 cycles. The static electrical parameters measured by the test system (PowerTECH, QT-3101 and QT-4100, China) include ON-state resistance [$R_{DS(ON)}$], gate–source drive current ($I_{GSS}$), threshold voltage ($V$th), and drain–source (D–S) leakage current ($I_{DSS}$).

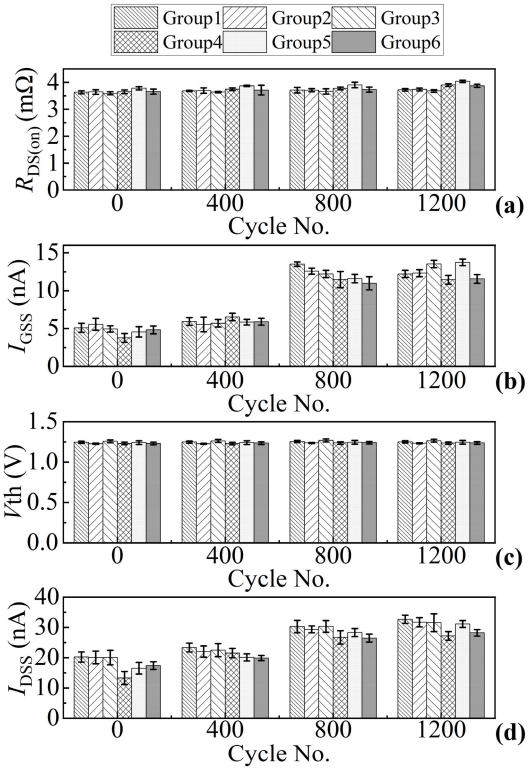


Fig. 10. Static electrical parameters versus cycle No. during thermal shock test. (a) $R_{DS(ON)}$. (b) $I_{GSS}$. (c) $V$th. (d) $I_{DSS}$.

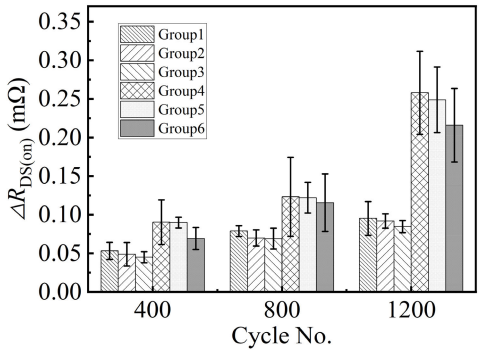


Fig. 11. $R_{DS(ON)}$ increment after temperature shock test.

### B. Results and Discussion

After the aforementioned thermal shock reliability aging test, various static electrical parameters of six group samples were measured, as shown in Fig. 10. The gradual failures of all test samples were observed, which resulted in $R_{DS(ON)}$ raised slightly, $V$th remaining relatively stable, and $I_{GSS}$ and $I_{DSS}$ increased steadily in the initial temperature cycle, but they increased considerably between 400 and 800 cycles. Thermal shock test, as a package-level aging test, will cause the degradations of the packaging materials and interconnection interfaces [23], which triggered the increasing $R_{DS(ON)}$, $I_{GSS}$, and $I_{DSS}$. However, the power cycle does not damage the chip itself, so $V$th was unchanged with the cycle number.

As shown in Fig. 11, the $R_{DS(ON)}$ increment of different groups of test samples increased to various degrees after

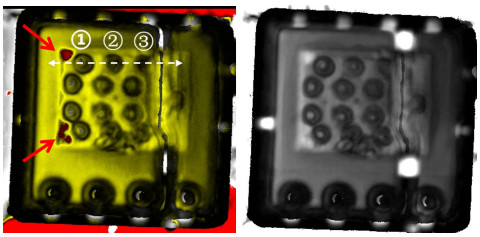


Fig. 12. SAM imaging of degraded test sample.

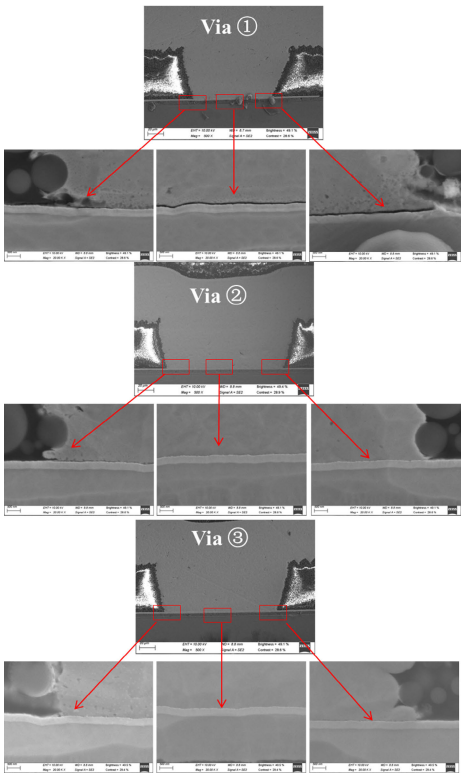


Fig. 13. SEM imaging of RDL blind via as marked in SAM image.

1200 cycles. The results show the following: 1) the $R_{DS(ON)}$ increment of test samples with larger RDL via depth $h$ is greater than those with smaller one and 2) with the greater the RDL blind via diameter $d$, the test samples had lower $R_{DS(ON)}$ increment. According to (12), as presented in Section II-C, the designed device package with larger the blind via diameter and the smaller the blind via depth has lower volume average inelastic working energy density under thermomechanical coupled loading. Generally, the aforementioned results indicate that $R_{DS(ON)}$ is highly related to the cumulative plastic work of the device under thermal shock test [24]. Furthermore, the thermomechanical oriented reliability of the designed FOPLP MOSFET power device can be enhanced by optimizing the diameter and depth of RDL blind via.

### C. Failure Analysis

In order to confirm the failure mode and mechanism, the failure analysis was carried out for the optimized samples ($d = 140$ $\mu$m and $h = 30$ $\mu$m) that underwent 1200 thermal shock cycles through both the scanning acoustic microscope (SAM) and scanning electron microscope (SEM). As shown in Fig. 12, the delamination was detected at the edge between the plastic molding and MOSFET chip, and there may be some cracks in the RDL blind via.

Furthermore, SEM imaging was performed on the RDL blind via at the edge of MOSFET chip, as shown in Fig. 13. It can be clearly seen that there are obvious cracks occurred at the edge of the blind via, especially those located at the edge of MOSFET chip, which led to an increase of leakage current and resistance. Coupling with the thermomechanical simulation results as shown in Fig. 8, this evidence can clearly prove that the cumulative thermomechanical stress during the thermal shock testing is the root cause of the static electrical performance degradation of the prepared MOSFET FOPLP power device.

## V. Conclusion

In this study, we applied the NSGA-II and ACO–BPNN to optimize the design of a 30-V Si MOSFET FOPLP power device. The dual-objective reliability optimization of reducing thermal resistance and thermomechanical stress was realized. The proposed method was verified by performing a thermal shock reliability aging test on the designed devices. The conclusions from the study results are summarized as follows. First, both NSGA-II and ACO–BPNN can achieve multiobjective optimization, among which NSGA-II exhibits a fast optimization calculation efficiency when the mathematical model is known, while ACO–BPNN relies on training data obtained through the FE simulation, which requires considerable calculation. However, ACO–BPNN can be used to optimize the complex packaging design in which mathematical models are rare. Six group samples with various RDL sizes were fabricated to verify the effectiveness of the optimizations; the optimized sample exhibited the smaller degradation after the thermal shock test. Second, as the cumulative plastic work determines the thermomechanical oriented reliability of the FOPLP power device, a reasonable RDL structure design, such as increasing the blind via diameter and reducing the depth, can reduce the cumulative plastic work of the FOPLP package under the thermal shock usage condition, which will inhibit the increase of the ON-resistance and improve the reliability of the device package.

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